Feasibility of an Electro-Optic Link for Bondpad-less CMOS Lab-on-Chips

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***Abstract*—This paper explores the feasibility of developing CMOS-based lab-on-chips to analyse the properties of a fluid, without the need for bond wires. Both inductive and electro-optical schemes are suggested as possible solutions. Specifically, this paper details a novel approach in achieving electro-optical modulation in unmodified, commercially-available CMOS technology. By exploiting the plasma dispersion effect, it is shown how mid-infrared light can be modulated using parasitic structures designed in a CMOS integrated circuit. Both the fundamental theory and practical realisation are supported with measured data from an experimental setup.**

***Index Terms*—lab-on-chip, CMOS, electro-optic, bondpad-less, wireless, free carrier absorption**

I. Introduction

Lab-on-Chip (LOC) technology is becoming increasingly used in a wide variety of applications ranging from simple chemical sensing to the study of chemotaxis in micro-organisms as well as other highly complex applications. Often the chemical composition of the fluid flowing in a microfluidic channel can be probed by means of an integrated sensor such as the ion-sensitive field effect transistor (ISFET) device [1]. A high level of integration allows microfluidic systems to achieve high density, lower power dissipation and low cost [1], [2].

The problem that we focus here is the critical issue of the interface between the integrated circuits (ICs) and the fluid flowing through the microfluidic channels, Fig.1(a). Traditionally, the IC requires wirebonds for power and communication and these are isolated typically using an epoxy-based encapsulant [3] (see Fig.1(c)). For LOC assembly, this needs to be planarised/patterned (to allow the sensors to be in contact with the fluid) and accurately aligned/mounted with the microfluidic platform [4]. Although LOC systems can be packaged in such a way, the encapsulant often fails, which in turn will damage the underlying IC. This makes such methods undesirable for large scale production as epoxy encapsulation, in addition to being extremely labour intensive, comes with a limited time-span. Here we investigate whether there is a way in which to render the wire-bonds unnecessary and transmit all data and power to and from the IC wirelessly.

A wireless data/power transmission system would be particularly attractive in the case where all communication transpires through the underside of the IC. Not only that this allows for an easily replaceable ICs, but it frees the top surface of the die to remain open and clear for fluid flow. If the power and data are transferred from above there still is no need for physical contact between the IC and external transceiver, so the implications are not too dire.

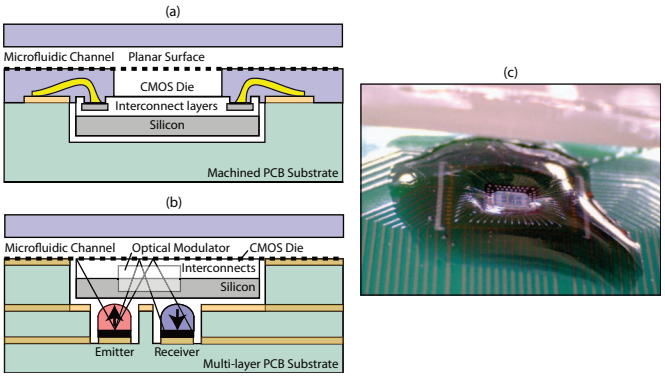


Fig. 1. (a) Cross section of a typical CMOS-based LOC platform with wire bonds encapsulated using the traditional approach, (b) The proposed electro-optical scheme, (c) Photo of a CMOS chip encapsulated using epoxy to insulate the bondwires from the top chip surface.

An additional benefit that would render the system even more attractive comes from the possibility to implement it in any standard CMOS technology, i.e. without any modifications or post fabrication steps. This would allow any research team to use wireless communication between IC and board without any restriction on technology whatsoever. Ideally the technology will be implementable using the most universally accessible processes using only basic structures such as well and diffusion pn-junctions.

In this paper an electro-optic based technology that fulfils all these criteria is presented and compared to a possible alternative - to use inductive coupling (Section II). Subsequently the theoretical basis for its operation is discussed (Section III) and engineering challenges related to taking the design from concept to silicon are described along with measured results that prove the concept (Section IV). Finally, an overview of the possible implications of this technology is presented.

II. System Overview

The platform presented herein delivers power and communicates data (to and from the chip) using light (electro-optical approach). It consists of structures to recover power, receive data and transmit data - based on an infra-red (IR) electro-optic modulator. An alternative approach would be to implement a platform based on inductive coupling [5],

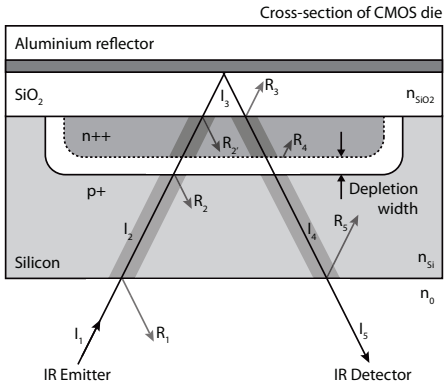


Fig. 2. Design configuration for the proposed system of communication. I_x represents the 'x'th part of an example beam's trajectory (the index changes every time the beam crosses from one material to another – Air, Si doped or not, SiO_2), R is the reflection coefficient, n is the refractive index and the shaded areas in I_2 and I_4 are areas where the beam is subject to optical losses due to free carrier absorption. Image from [6].

however the constraint is that all components would have to be integrated (i.e. no off-chip discretes). The concept of an optical link is illustrated alongside the traditional approach (i.e. using wirebonds and encapsulation) in Fig. 1.

The most challenging and novel aspect of the design is the data read-out function. As silicon is an indirect bandgap material, structures to directly emit light cannot be easily implemented, particularly within the constraints of standard CMOS technology. This can however be achieved by using an electro-optic modulator affecting a set of IR beams generated off-chip [6]. The basic idea is that for mid-IR radiation silicon is essentially transparent (the band gap in silicon correspond to $\approx 1.07\mu m$, at room temperatures), but for the effect of free carrier absorption which attenuates through-passing beam [7]. Specifically in the set-up proposed in Fig.1(b), an off-chip IR LED emits light from the underside of the die (see Fig. 2), the set of beams propagate through the substrate with little optical loss and then hit the highly doped regions (e.g. n^{++} region in Fig.2) where they suffer absorption. At the pn-junction the free carrier concentration can be controlled by carrier injection, accumulation or depletion by changing the biasing across the junction terminals. Hence the light intensity can be controlled by external bias. Once the beam has exited the junction area, it continues to propagate upwards until it hits a reflective metal layer. The radiation then starts its descending pathway back towards the underside of the die, suffers optical loss once again and eventually exits the die ipsilaterally to the emitter that generated it and falls on the detector. On the other hand, data read-in can be easily achieved by simply using a photodiode that can collect incoming EM radiation in the visible spectrum. Power transmission is achieved by using an integrated photodiode operating as a solar cell (with the relevant power recovery circuitry). Use of photodiodes for data read-in and as power recovery is already widespread and well understood [8], [9]. In contrast, inductive coupling methods resort to using integrated and external coil pairs in order to perform these functions [5].

In general, both IR and inductive coupling approaches to full-wireless ICs will suffer from low efficiencies. In the inductive case they pertain mostly to coupling efficiency and cross-talk [5], whilst in the optical case the weakness of the free-carrier absorption phenomenon for data read-out and the relatively low efficiency of silicon for optical power recovery [8] seem to be the main issues. At the same time it is noteworthy that the optical system has the advantage of a very clear separation between data read-in and read-out channel groups, as they occur in completely different wavelength ranges. Careful geometrical layout can then minimise cross-talk across each channel group for further improvements in performance. Also quite importantly, there is no need for large on-chip inductors.

III. Fundamental Theory of Operation

At the heart of the optical communication platform sits the modulator which uses the plasma dispersion effect, in which the concentration of free charges in silicon changes the real and imaginary parts of the refractive index [7], [10]. The phenomenon can be described by equation (1), derived in [11].

$$\Delta\alpha = \left(\frac{e^3\lambda^2}{4\pi^2c^3\epsilon_0 n}\right)\left[\frac{\Delta n_e}{m_{ce}^{*2}\mu_e} + \frac{\Delta n_h}{m_{ch}^{*2}\mu_h}\right] \tag{1}$$

where e the electron charge, ϵ_0 the electric constant, c the speed of light in a vacuum, λ the through-passing light wavelength, n the refractive index, m_{cx}^* the effective mass of the indicated carrier (x=e for electron, x=h for hole), n_{x} free carrier concentration and μ_{x} carrier mobility. The effect is proportional to free carrier concentration and is thus directly linked to doping concentrations, as the free carrier concentrations are approximately equal to the doping concentrations ($n_{\mathrm{x}} = N_{\mathrm{x}}$). This detail is of crucial importance since in traditional CMOS ICs the substrate is typically very lightly doped ($\sim 10^{15}\mathrm{cm}^{-3}$) whilst in well or diffusion layers concentrations are as high as $10^{20}\mathrm{cm}^{-3}$ or even $10^{21}\mathrm{cm}^{-3}$, see Fig.3(c). This immediately implies that a mid-IR wavelength will be able to traverse a die substrate with minimal optical loss before reaching the heavily doped regions.The dependence of the phenomenon on the doping concentrations is shown in Fig. 3.

In a very narrow region around the metallurgical point the beam passes through without any loss because of charge depletion. By modulating the width of the depletion region via application of appropriate reverse bias voltages the degree of optical loss suffered by the IR beam along the path can be changed. The connection between bias voltage V_{bias} and depletion region width W, for an abrupt junction, is given by equation [12]:

$$W = \sqrt{\frac{2\epsilon_0\epsilon_r}{e}\left(\frac{N_A+N_D}{N_AN_D}\right)\left[\frac{kT}{e}\ln\left(\frac{N_AN_D}{n_i^2}\right) + V_{\mathrm{bias}}\right]} \tag{2}$$

where W is the depletion region width, e_0 and e_r, k and e are the usual universal constants, T is the temperature, n_i the intrinsic carrier concentration of silicon and N_x the

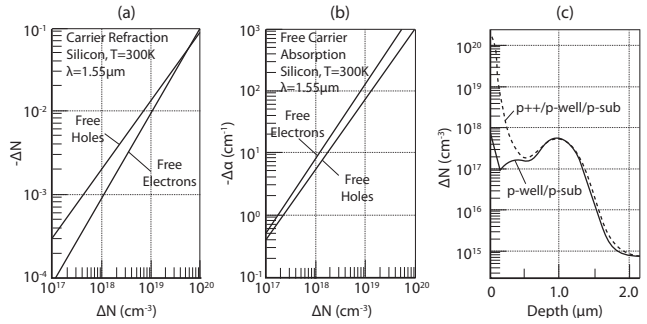


Fig. 3. Electro-optical properties of doped silicon and a typical doping profile of a CMOS technology. Shown are: (a, b) Perturbation in the refractive index and absorption coefficient of silicon as a function of free carrier concentration for light wavelength $\lambda = 1.55\,\mu$m and temperature $T = 300\,$K (redrawn from: [10]), (c) Doping profile (doping concentration vs. depth from the silicon surface) of a typical CMOS technology.

acceptor (x=A) or donor (x=D) concentrations at the eges of the depletion region.

By then mathematically setting up the geometry, assigning the proper values to the variables of equations (1) and (2), and testing for given ΔV one may then start generating preliminary theoretical results [11], Table I. Furthermore, the energy per 'bit toggling' is equal to the energy required to charge the modulator's capacitance from the lower bound of ΔV to the upper bound (or discharging from upper bound to lower) and will depend strongly on geometry.

TABLE I
CALCULATED VALUES FOR CHANGE IN ABSORBANCE DUE TO A REVERSE BIAS MODULATION OF 5 V FOR $\lambda = 1.55\,\mu$M FOR A STEP JUNCTION (EQ. 2) AND EXPONENTIALLY GRADED DOPING PROFILE (FIG. 4).

	step	junction	model	exp.graded
N_D [cm^{-3}]	10^{20}	10^{20}	10^{19}	10^{20}
N_A [cm^{-3}]	10^{20}	10^{19}	10^{19}	$5 \cdot 10^{17}$
$\Delta I/I$	0.23%	0.06%	0.025%	0.01%

To add further complication, diffusion junctions as well as the horizontal and vertical components of well junctions all tend to have different net doping concentrations at the edges of their respective depletion regions. This makes the choice of junction type particularly important. Furthermore, the reverse bias voltages that can be applied to the pn-junction are limited by the breakdown. Another issue concerns the exact geometrical layout of the emitter–modulator–detector triplet. Care must be taken so that there is as little direct emitter–detector communication as possible in order to prevent the detector from having to contend with an elevated level of baseline activity. If more than one channel for data-out communication is used then the modulators have to be aligned and laid out in such way that all beams from the emitter that hit a certain detector cross through the same modulator. It is possible to design configurations that allow one emitter to service several modulators simultaneously. The size of each element in the emitter, modulator and detector multiplet will be essentially low-limited by the thickness of the die as that

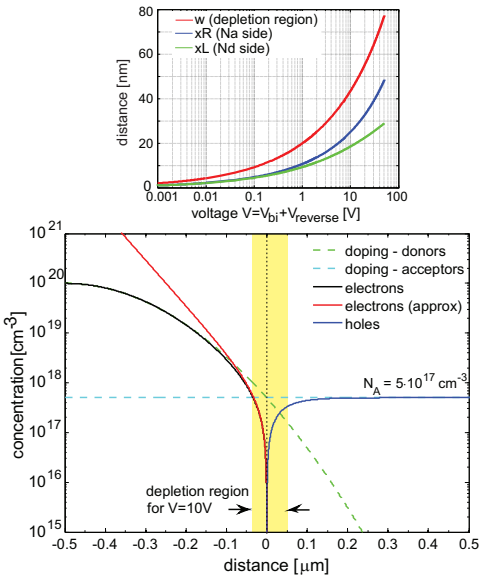


Fig. 4. Calculation of the depletion width vs. reverse bias voltage (top) for an exponentially graded doping profile (bottom), assuming n+ diffusion (surface donor concentration $N_D = 10^{20}$ cm^{-3}) into a p-well ($N_a = 5 \cdot 10^{17}$ cm^{-3}). This is an approximation for diffusion-to-well structures. The fee electron concentration follows approximately Gaussian distribution (black line), which is approximated in the junction area with an exponential function in order to simplify integration of Poisson equation [13].

is the primary determinant of beam fan-out (for the modulator and the detector), and by the power we are willing or forced to spend in generating the outgoing beam in order to operate the system (emitter). The upper bounds will be determined by noise (dark current for the detector), die area considerations and/or bit toggle energy considerations (modulator) and die area (indirectly) and/or static power dissipation (emitter).

As for power transfer and data read-in, it turns out that the most practical way to implement them is by using photodiodes that harness visible light, ideally using junctions with low contrast between p and n region doping concentrations and hence wider depletion regions and by extension a larger photon collecting volume [14]. Moreover, because in this part of the spectrum silicon is opaque the most efficient location for the relevant emitters is above the surface of the die, possibly even over the fluid channel. Beyond this geometrical/physical set of problems lie further challenges in converting the incoming photon energy into a stable and usable voltage. This implies the use of a power management unit (PMU) of which examples abound [8], [9]. Further discussion of PMUs is outside the scope of this paper.

IV. Integrated Circuit and Measured Results

A test chip has been designed and fabricated in an unmodified $0.35\mu m$ 2P4M (commercially-available) CMOS technology. This included an array of test devices based on parasitic pn-junctions using different structures, for example multiple n-diffusion stripes within a single p-well, or grids of n-well regions within a p-well/p-substrate [6]. The laboratory tests under the configuration seen in Fig. 5 have shown

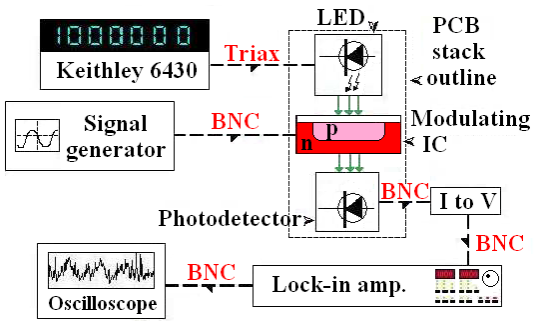


Fig. 5. Instrument configuration for testing the optical modulator with the help of an Amplitude Modulated signal at fixed carrier frequency. A Keithley sourcemeter provides the DC bias for the LED. Any detected signal that persists over the lock-in amplifier's integration period and is at the reference frequency should appear as a DC signal at the oscilloscope screen.

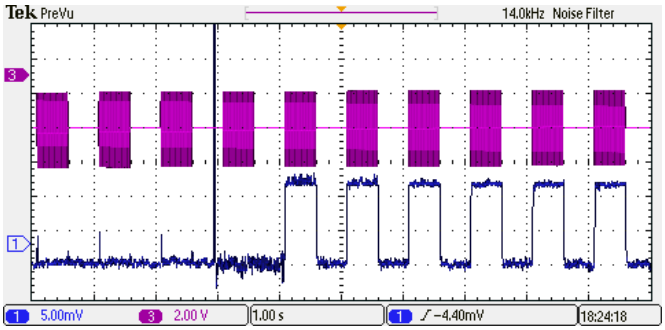


Fig. 6. Sample proof-of-concept result. The purple trace is the test signal fed to the optical modulator (1Hz square wave modulated by a 1kHz carrier). The blue trace is the output measured from the photodetector (see Fig. 5). Early on the time axis the LED providing light to the test set-up is kept off and the photodetector detects nothing. At the point where the large vertical bar appears the LED has gone online and the Lock-in amplifier is in overload. Eventually the lock-in amplifier accommodates itself to the new signal level and the output of the photodetector begins to follow the input signal closely.

that the proposed concept of the data read-out mechanism is indeed feasible. The major difficulty was to extract the very weak signal from noise in the optical output and very strong electrical pick-up from the signal-generator, and for that purpose we used a Lock-in amplifier and tuned it to the 2nd harmonic – result shown in Fig. 6. The test modulator structures are encased in a PCB sarcophagus which let no light other than that from the test LED penetrate through to the chamber containing the test IC and the detector. The LED and the detector lie contralaterally with respect to the test IC, therefore the IR beam crosses the test IC only once, not twice as should be the case in the final design.

Measured results demonstrated the speeds of up to 100bps with a $1.55\,\mu$m LED. With improvements in the quality of the test set-up (including beam alignment quality etc.) it is not inconceivable that the need for a lock-in amplifier can be eliminated and consequently that data transfer can be sped up significantly.

V. Conclusions and Possible Applications

A novel technique pertaining to optical data communication and power transfer perpendicular to the plane of an IC in basic, standard CMOS was presented. The technique is based on standard solar cell-type configurations for data read-in and power transfer and on the electroabsorption type of electro-optic modulator for data read-out. Some of the engineering challenges were discussed and measured results of the first prototype were shown that prove that the concept is indeed viable. It was speculated that this way of communication paves the way for truly wireless ICs for use in microfluidic applications or for that matter in any lab-on-chip application where the flexibility of having an easily replaceable part is necessary. Finally, it is worth mentioning that all challenges that lie between the present time and rendering the system commercially available are of an engineering nature and once solved shall unlock the full potential of this approach.

Acknowledgment

The authors would like to acknowledge EPSRC grant EP/G070466/1 for supporting this work.

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