Fault behaviour and fault detection in islanded inverter-only microgrids

by
Maria Brucoli

A Thesis Submitted for the Degree of Doctor of Philosophy and for the Diploma of Imperial College

Control and Power Group
Department of Electrical and Electronic Engineering
Imperial College London
2008

Abstract

The increase in popularity of the microgrid concept requires the analysis and solution of the numerous technical issues arising from the operation and integration of the microgrid into the original distribution network. The work presented in this thesis is centred on the study of the fault behaviour of inverter-only microgrids and on the development of a suitable fault detection technique.

This task is approached by first understanding the behaviour of a microgrid during a fault and the factors affecting it. A complete description and analysis of the key elements in the study of microgrid fault behaviour is presented. Then, three microgrid models with different inverter control methods (i.e. Synchronous Reference Frame control, Natural Reference Frame control and droop control) and with various current limiting strategies are built in PSCAD and their fault behaviour is simulated, analyzed and compared.

It is found that the control of the inverter is able to shape the response of the microgrid in the event of a fault. The constraints to this capability are the inverter's ratings (current and voltage limits) and the characteristic changes in the network introduced by faults. Moreover, it is found that the control in the Natural Reference Frame gives better fault response, in terms of voltage control and simplicity in implementation, compared with the popular control in the Synchronous Reference Frame.

The behaviour of the system is then further analyzed by developing quasi steady-state inverter models suitable for numerical fault analysis. The models are developed starting from the inverter control and analyzing how it changes in the event of a fault. By combining control gains and circuit parameters, they result in being capable of capturing the key features of inverters' fault behaviour. Depending on the control strategy, some of these models are balanced and therefore are directly applicable in numerical fault analysis based on sequence components. Others are unbalanced and therefore require a fault analysis based on a direct phase coordinates representation of the network. Examples on how to perform numerical fault analysis calculations with balanced and unbalanced models are given and the numerical results well compare with the ones obtained from time-domain simulations using PSCAD.

From the knowledge of the microgrid fault behaviour developed analyzing the responses in time-domain simulations and by using the developed inverter models to numerically calculate voltages and currents in the microgrid during different faults at various locations, a fault detection strategy based on voltage sequence components is proposed. Indeed, it is the behaviour of the inverter control during faults which makes the monitoring of voltage sequence components the best discriminator between normal operation and fault operation. The three building blocks of the fault detection strategy which are capable of a fast extraction and comparison of voltage sequence components are described and then the performance of the fault detection strategy for different faults and microgrid operating conditions is tested in PSCAD and discussed. Finally, examples are given on how this voltage detection can be used in the design of a microgrid protection system.

Contents

List of Figures **8**

List of Tables **16**

List of Symbols **18**

List of Abbreviations **20**

Acknowledgements **21**

1 Introduction **22**

1.1 Background and scope 22

1.2 Overview 23

1.3 Thesis structure 25

2 Distribution networks, distributed generation and microgrids: the impact on power systems protection **27**

2.1 Introduction 27

2.1.1 Distribution networks and distributed generation overview 28

2.1.2 Microgrids 29

2.1.3 Conventional distribution network protection 30

2.2 Impact of DG on distribution network protection 33

2.2.1 Impact on fault current levels 33

2.2.2 Impact on overcurrent protection 35

2.2.3 Approaches to the design of a suitable protection system for distribution networks with DG 37

2.3 Protection issues with DG and microgrids 42

2.3.1 Protection for faults outside the microgrid 42
2.3.2 Protection for faults inside the microgrid when the microgrid is connected to the distribution grid 44
2.3.3 Protection for faults inside the microgrid when islanded 44
2.4 Protection issues with islanded inverter-only microgrids 45
2.4.1 Fault currents in islanded inverter-only microgrids and impact on overcurrent protection 45
2.4.2 Approaches to the design of a suitable protection system for islanded inverter-only microgrids 50
2.5 Conclusion 52

3 Microgrid network topology and control 54
3.1 Microgrid network topology 55
3.1.1 Inverter-interfaced DG topologies 55
3.1.2 Microgrid earthing 59
3.1.3 Microgrid network configuration 62
3.2 Inverter control and operation 66
3.2.1 Control of a stand-alone inverter 67
3.2.2 Control of parallel-connected inverters 70
3.2.3 Unbalanced operation of an inverter 73
3.3 Microgrid network models 77

4 Fault response of islanded inverter-only microgrids 80
4.1 Microgrid supplied by a single inverter controlled in the SynRF 81
4.1.1 Control of a stand-alone inverter in the SynRF 81
4.1.2 Control in the SynRF and unbalanced operation 84
4.1.3 Control in the SynRF and current limiting 86
4.1.4 System description: Model 1 95
4.1.5 Fault response of a microgrid supplied by a single inverter controlled in the SynRF and with current limiting in the SynRF: Case 1 102
4.1.6 Fault response of a microgrid supplied by a single inverter controlled in the SynRF and with current limiting in the NatRF 110
4.2 Microgrid supplied by a single inverter controlled in the NatRF 118

4.2.1 Control of a stand-alone inverter in the NatRF 118
4.2.2 Control in the NatRF and unbalanced operation 121
4.2.3 Control in the NatRF and current limiting 123
4.2.4 System description: Model 2 124
4.2.5 Fault response of a microgrid supplied by a single inverter controlled in the NatRF and with current limiting in the NatRF 124
4.3 Comparison of the different fault responses in an islanded microgrid supplied by a single inverter 129
4.4 Microgrid supplied by two parallel-connected inverters 133
4.4.1 Control of two parallel-connected inverters 133
4.4.2 Droop control and unbalanced operation 134
4.4.3 Droop control and current limiting 135
4.4.4 System description: Model 3 135
4.4.5 Fault response of a microgrid supplied by two parallel-connected inverters: Case 6 135
4.5 Conclusion on fault response of islanded inverter-only microgrids 142

5 Modelling and fault analysis of islanded inverter only-microgrids 147
5.1 Inverter models for fault analysis studies 148
5.1.1 Fault models of stand-alone multi-loop controlled inverter 148
5.1.2 Fault models of parallel-connected inverters 157
5.2 Fault analysis studies in a microgrid 162
5.3 Fault analysis in sequence components 168
5.4 Fault analysis in direct phase coordinates 174
5.4.1 Microgrid supplied by a single inverter controlled in the SynRF . . . 175
5.4.2 Microgrid supplied by a single inverter controlled in the NatRF . . . 177
5.4.3 Microgrid supplied by two parallel-connected inverters 179
5.5 Discussion on inverter fault models 184

6 A Fault detection technique suitable for islanded inverter-only microgrids 189
6.1 Protection in traditional electricity networks: a microgrid prospective . . . 190
6.2 Fault detection in islanded inverter-only microgrids 191

6.2.1 Microgrid supplied by a single inverter 191
6.2.2 Microgrid supplied by two parallel-connected inverters 198
6.3 Voltage detection methods, their performance and application to fault detection in microgrids 208
6.3.1 Voltage sag detection method based on $dq\gamma$ transformation 208
6.3.2 Voltage sag detection method based on a 90-degree phase shift operator 211
6.3.3 Comparison of detection methods 212
6.3.4 A fault detection technique based on voltage sequence components . 216
6.4 Voltage-based fault protection in an islanded inverter-only microgrid: two illustrative examples 217
6.4.1 Voltage-based fault protection in a microgrid supplied by a single inverter 217
6.4.2 Voltage-based fault protection in a microgrid supplied by two parallel-connected inverters 222
6.5 Conclusions 227

7 Conclusion and future work **229**
7.1 Concluding remarks 229
7.2 Author's contribution 231
7.3 Suggestions for future work 233

Author's Publication **236**

Bibliography **246**

A Three-phase transformations **247**
A.1 Symmetrical Components 247
A.2 Clarke and Park transformations 249
A.3 System unbalance in the StatRF and in the SynRF 250
A.4 Harmonic components in the SynRF 253

B Frequency-domain transformations **254**

C Derivation of the voltage dq components for unbalanced faults for comparison of different voltage detection methods **257**

C.1 Single phase-to-ground fault ($1\phi g$) 257
C.2 Phase-to-phase fault (2ϕ) 258
C.3 Double phase-to-ground fault ($2\phi g$) 259

List of Figures

2.1 A simple example microgrid 29
2.2 Radial coordination of inverse and instantaneous overcurrent elements . . . 32
2.3 Recloser and sectionalisers in a distribution network 33
2.4 Relay protection zone without and with DG 35
2.5 Example of false tripping 36
2.6 Impact of DG on recloser and fuse coordination 36
2.7 Example of faults outside the microgrid 43
2.8 Example of a more complex microgrid network 45
2.9 Impact of microgrids on inverse time/current characteristics coordination . 49

3.1 Block diagram of a typical inverter-interfaced DG unit 55
3.2 Three-phase, three-leg, three-wire voltage source inverter with a delta/wye grounded transformer 56
3.3 Three-phase, three-leg, four-wire voltage source inverter with split DC link capacitors 57
3.4 Three-phase, four-leg, four-wire voltage source inverter 57
3.5 Parallel operation of two inverters 59
3.6 Solidly interconnected neutral conductor grounded at the substation only [54] 60
3.7 Neutral conductor grounded at the substation and at the source of alternate power supply (separately derived source) [54] 61
3.8 LV distribution network with microgrid 62
3.9 Microgrid (shown in red) with SS on the primary transformer side 64
3.10 Microgrid (shown in red) with 3-pole SS on the secondary transformer side 64
3.11 Microgrid (shown in red) with 3-pole SS on the secondary transformer side after the “non critical”loads 65

3.12 Microgrid (shown in red) with 4-pole SS 65
3.13 Multi-loop control of a stand-alone inverter 68
3.14 Equivalent two-terminal circuit of a stand-alone inverter with multi-loop control 69
3.15 Output impedance Bode diagram 70
3.16 Power droop controller 72
3.17 Three-phase four-wire LC output filter 73
3.18 Control voltage vector trajectories for balance and unbalanced operation . . 77
3.19 Microgrid supplied by a single inverter 78
3.20 Microgrid supplied by two parallel-connected inverters 79

4.1 Equivalent block diagrams in SynRF of the LC filter 83
4.2 Multi-loop control of a stand-alone inverter in the SynRF 84
4.3 Control scheme for positive and negative sequence components in the SynRF [67] 86
4.4 Bode diagram of P+Resonant controller for $k_i = 1, 10, 100$ and $k_p = 1$ . . . 87
4.5 Reference inductor currents $i^*_{L_d}$ and $i^*_{L_q}$ for a phase-to-phase fault (ab) with no current limiting compared with saturation limits 88
4.6 Saturated reference inductor currents $i^*_{Lsat_d}$ and $i^*_{Lsat_q}$ for a phase-to-phase fault (ab) with current limiting 89
4.7 Tracking anti-windup PI controller 90
4.8 Saturated reference inductor currents $i^*_{Lsat_d}$ and $i^*_{Lsat_q}$ with back-calculation anti-windup for a phase-to-phase fault (ab) 90
4.9 SynRF ($dq\gamma$ coordinates) voltage and current control loops with current limiting in the SynRF 92
4.10 SynRF ($dq\gamma$ coordinates) voltage and current control loops with instantaneous current limiting in the NatRF 94
4.11 SynRF ($dq\gamma$ coordinates) voltage and current control loops with RMS current limiting in the NatRF 95
4.12 Circle diagram of inverter output current i_0 and inverter inductor current i_L in $dq\gamma$ coordinates 98
4.13 Inverter's response to a 20% power unbalance on phase a and on phase b . . 99
4.14 Inverter's response to a 20% power unbalance on the same phase a 100

4.15 Inverter's response to normal balanced operation 100
4.16 Circle diagram of inverter output phase current $\bar{I}_{0_a}$ and inverter inductor phase current $\bar{I}_{L_a}$ 101
4.17 Response to a 3ϕ fault at point F_3 of a microgrid supplied by a single inverter (control and current limiting in the SynRF) 103
4.18 Response to a 2ϕ fault at point F_3 of a microgrid supplied by a single inverter (control and current limiting in the SynRF) 103
4.19 Response to a $2\phi g$ fault at point F_3 of a microgrid supplied by a single inverter (control and current limiting in the SynRF) 104
4.20 Response to a $1\phi g$ fault at point F_3 of a microgrid supplied by a single inverter (control and current limiting in the SynRF) 104
4.21 Reference inverter bridge voltage v_i^* in dq coordinates for a $2\phi g$ fault at point F_3 in a microgrid supplied by a single inverter (control and current limiting in the SynRF): without instantaneous voltage limiting (blue line), with voltage limiting algorithm as in [76] (red line) 106
4.22 Reference inverter bridge voltage v_i^* in $\alpha\beta$ coordinates for a $2\phi g$ fault at point F_3 in a microgrid supplied by a single inverter (control and current limiting in the SynRF): without instantaneous voltage limiting (blue line), with voltage limiting algorithm as in [76] (red line) 107
4.23 Comparison of v_{i_a}, v_{i_b} and $v_{i_c}$for a $2\phi g$ fault at point F_3 in a microgrid supplied by a single inverter (control and current limiting in the SynRF): (a) Without instantaneous voltage limiting, (b) With voltage limiting algorithm as in [76] 108
4.24 SynRF voltage and current control loops with instantaneous per-phase voltage limiting in the NatRF 109
4.25 Comparison of v_{i_a}, v_{i_b} and $v_{i_c}$for a $2\phi g$ fault at point F_3 in a microgrid supplied by a single inverter (control and current limiting in the SynRF): (a) Without instantaneous voltage limiting, (b) With instantaneous per-phase voltage limiting 109
4.26 Response to a 3ϕ fault at point F_3 of a microgrid supplied by a single inverter (control in the SynRF and instantaneous current limiting in the NatRF) 111

4.27 Response to a 2ϕ fault at point F_3 of a microgrid supplied by a single inverter (control in the SynRF and instantaneous current limiting in the NatRF) 111
4.28 Response to a $2\phi g$ fault at point F_3 of a microgrid supplied by a single inverter (control in the SynRF and instantaneous current limiting in the NatRF) 112
4.29 Response to a $1\phi g$ fault at point F_3 of a microgrid supplied by a single inverter (control in the SynRF and instantaneous current limiting in the NatRF) 112
4.30 Comparison of v_{i_a}, v_{i_b} and $v_{i_c}$for a $2\phi g$ fault at point F_3 in a microgrid supplied by a single inverter controlled in the SynRF: (a) with current limiting in the SynRF, (b) With instantaneous current limiting in the NatRF 113
4.31 Response to a 3ϕ fault at point F_3 of a microgrid supplied by a single inverter (control in the SynRF and RMS current limiting in the NatRF) . . 115
4.32 Response to a 2ϕ fault at point F_3 of a microgrid supplied by a single inverter (control in the SynRF and RMS current limiting in the NatRF) . . 115
4.33 Response to a $2\phi g$ fault at point F_3 of a microgrid supplied by a single inverter (control in the SynRF and RMS current limiting in the NatRF) . . 116
4.34 Response to a $1\phi g$ fault at point F_3 of a microgrid supplied by a single inverter (control in the SynRF and RMS current limiting in the NatRF . . 116
4.35 Comparison of v_{i_a}, v_{i_b} and $v_{i_c}$for a $2\phi g$ fault at point F_3 in a microgrid supplied by a single inverter controlled in the SynRF: (a) with current limiting in the SynRF, (b) With RMS current limiting in the NatRF 117
4.36 Equivalent block diagram in NatRF of the LC filter 119
4.37 Multi-loop control of a stand-alone inverter in the NatRF 120
4.38 NatRF (*abc* coordinates) voltage and current control loops with RMS current limiting in the NatRF 125
4.39 Response to a 3ϕ fault at point F_3 of a microgrid supplied by a single inverter (control in the NatRF and instantaneous current limiting in the NatRF) 126

4.40 Response to a 2ϕ fault at point F_3 of a microgrid supplied by a single inverter (control in the NatRF and instantaneous current limiting in the NatRF) 127
4.41 Response to a $2\phi g$ fault at point F_3 of a microgrid supplied by a single inverter (control in the NatRF and instantaneous current limiting in the NatRF) 127
4.42 Response to a $1\phi g$ fault at point F_3 of a microgrid supplied by a single inverter (control in the NatRF and instantaneous current limiting in the NatRF) 128
4.43 Response to a 3ϕ fault at point F_3 of a microgrid supplied by a single inverter (control in the NatRF and RMS current limiting in the NatRF) . . 130
4.44 Response to a 2ϕ fault at point F_3 of a microgrid supplied by a single inverter (control in the NatRF and RMS current limiting in the NatRF) . . 130
4.45 Response to a $2\phi g$ fault at point F_3 of a microgrid supplied by a single inverter (control in the NatRF and RMS current limiting in the NatRF) . . 131
4.46 Response to a $1\phi g$ fault at point F_3 of a microgrid supplied by a single inverter (control in the NatRF and RMS current limiting in the NatRF) . . 131
4.47 Response to a 3ϕ fault at point F_3 of a microgrid supplied by two parallel-connected inverters 136
4.48 Response to a 2ϕ fault at point F_3 of a microgrid supplied by two parallel-connected inverters 137
4.49 Response to a $2\phi g$ fault at point F_3 of a microgrid supplied by two parallel-connected inverters 138
4.50 Response to a $1\phi g$ fault at point F_3 of a microgrid supplied by two parallel-connected inverters 139
4.51 Microgrid response (two parallel-connected inverters) to a 3ϕ fault at point F_3: (a) Fundamental active and reactive powers, (b) Generated voltage references, (c) Generated frequency references 140
4.52 Microgrid response (two parallel-connected inverters) to a $1\phi g$ fault at point F_3: (a) Fundamental active and reactive powers, (b) Generated voltage references, (c) Generated frequency references 141

4.53 Response to a $1\phi g$ fault at point F_1 of a microgrid supplied by two parallel-connected inverters (droop control with multi-loop control in NatRF and RMS current limiting in the NatRF) 143
4.54 Reproduced from Figures 4.23 and 4.45 145
4.55 Reproduced from Figures 4.41 and 4.45 146

5.1 Multi-loop control of a stand-alone inverter with current limiting 149
5.2 Equivalent two-terminal circuit of a stand-alone inverter with current limiting 149
5.3 Three-phase four-leg SynRF controlled inverter fault model: equivalent phase networks 151
5.4 Three-phase four-leg SynRF controlled inverter fault model: equivalent sequence networks 153
5.5 Equivalent phase networks of a three-phase four-leg inverter controlled in the NatRF for a $1\phi g$ fault. 155
5.6 Equivalent phase networks, as current sources, of a three-phase four-leg phase inverter controlled in the NatRF for a $1\phi g$ fault 158
5.7 Equivalent phase networks of two parallel-connected inverters controlled in the NatRF for a 3ϕ fault at F_3 160
5.8 Equivalent sequence networks of two parallel-connected inverters controlled in the NatRF for a 3ϕ fault at F_3 161
5.9 Equivalent phase networks of two parallel-connected inverters controlled in the NatRF for a $1\phi g$ fault at F_3 163
5.10 Equivalent sequence networks of two parallel-connected inverters controlled in the NatRF for a $1\phi g$ fault at F_3 164
5.11 Equivalent phase networks of two parallel-connected inverters controlled in the NatRF for a $1\phi g$ fault at F_1 165
5.12 Equivalent per-phase circuit representation of the microgrid, including the parallel impedances of the inverter. 167
5.13 Equivalent per-phase circuit representation of the microgrid supplied by two inverters 167
5.14 Equivalent circuit for fault analysis studies based on sequence components for a microgrid supplied by a stand-alone inverter 168

5.15 Equivalent circuit for fault analysis studies based on sequence components for a microgrid supplied by two parallel-connected inverters 169
5.16 Inverter output voltage (v_0) and inductor current (i_L) during a 3ϕ fault in a microgrid supplied by a single inverter controlled in the SynRF 171
5.17 Inverter output voltage (v_0) and inductor current (i_L) during a $1\phi g$ fault in a microgrid supplied by a single inverter controlled in the SynRF 172
5.18 Inverter output voltages (v_{0_1}, v_{0_2}) during a 3ϕ fault in a microgrid supplied by two parallel-connected inverters 173
5.19 Inverter output voltages (v_{0_1}, v_{0_2}) during a $1\phi g$ fault in a microgrid supplied by two parallel-connected inverters 175
5.20 Inverter output voltage (v_0) and inductor current (i_L) during a 3ϕ fault in a microgrid supplied by a single inverter controlled in the NatRF 178
5.21 Inverter output voltage (v_0) and inductor current (i_L) during a $1\phi g$ fault in a microgrid supplied by a single inverter controlled in the NatRF 180
5.22 Phase-to-earth (v_{ag}, v_{bg}, v_{cg}) and phase-to-neutral (v_{an}, v_{bn}, v_{cn}) voltages at fault point during a $1\phi g$ fault at F_3 in a microgrid supplied by two parallel-connected inverters 182
5.23 Phase-to-earth (v_{ag}, v_{bg}, v_{cg}) and phase-to-neutral (v_{an}, v_{bn}, v_{cn}) voltages at fault point during a $1\phi g$ fault at F_1 in a microgrid supplied by two parallel-connected inverters 184
5.24 Interaction between faulted network and inverter controlled as a constant current source 186

6.1 Microgrid supplied by a single inverter: relay configuration and fault locations 192
6.2 Microgrid supplied by two parallel-connected inverters: possible relay configuration 199
6.3 Block diagram of voltage detection method based on $dq\gamma$ transformation . . 209
6.4 Block diagram of detection method with a notch filter 210
6.5 Bode diagram of the notch low-pass filter in Figure 6.4 210
6.6 Block diagram of detection method with phase shift filter 211
6.7 Detection times for a three-phase fault with voltage drop to 60% nominal value 213

6.8 Detection times for a three-phase fault with voltage drop to 40% nominal value . . . 213
6.9 Detection times for a phase-to-phase fault (b-c) . . . 214
6.10 Detection times for a double phase-to-ground fault (b-c-g) . . . 214
6.11 Detection times for a phase-to-ground (a-g) fault . . . 215
6.12 Positive sequence detector block . . . 216
6.13 Negative sequence detector block . . . 216
6.14 Zero sequence detector block . . . 217
6.15 Operation of a single inverter microgrid for varying load with no current limiting . . . 220
6.16 Operation of a single inverter microgrid for overloads which do cause current limiting . . . 220
6.17 Behaviour of V_n at R_1, R_2 and R_3 for different unbalanced faults at F_3 in a single inverter microgrid for varying loads: (a) 2ϕ fault, (b) $2\phi g$ fault, (c) $1\phi n$ fault, (d) $1\phi g$ fault . . . 221
6.18 Behaviour of V_n and V_{0e} at R_1, R_2 and R_3 for different unbalanced faults at F_3 in a two-inverters microgrid for varying loads: (a) 2ϕ fault, (b) $2\phi g$ fault, (c) $1\phi n$ fault, (d) $1\phi g$ fault . . . 225

A.1 Symmetrical components and decomposition of an unbalanced three-phase set of voltage vectors . . . 248
A.2 Clarke transformation from three-phase *abc* to two phase $\alpha\beta$ stationary system . . . 250
A.3 Park transformation from the StatRF to the SynRF . . . 251
A.4 Positive and negative sequence components in the StatRF . . . 252
A.5 Voltage vector trajectory for balanced and unbalanced operation in the $\alpha\beta$ plane . . . 252

List of Tables

2.1 Fault current levels for different types of generators 34
2.2 Fault currents for a three-phase fault in a grid-connected microgrid with one inverter-interfaced DG source 46
2.3 Fault currents for a three-phase fault in a grid-connected microgrid with two inverter-interfaced DG sources 46
2.4 Fault currents for a three-phase fault in an islanded microgrid supplied by one inverter-interfaced DG source 47
2.5 Fault currents for a three-phase fault in an islanded microgrid supplied by two inverter-interfaced DG sources 47
2.6 Normal operation in a grid-connected microgrid 48
2.7 Normal operation in an islanded microgrid 48

3.1 Microgrid parameters 78

4.1 Case studies in the analysis of fault response of islanded inverter-only microgrids 81

5.1 Equivalent Fault Impedances 169

6.1 Load unbalanced operation in a microgrid supplied by a single inverter controlled in the NatRF 193
6.2 3ϕ fault in a microgrid supplied by a single inverter controlled in the NatRF (values in yellow are chosen as indicators of the presence of a fault) 195
6.3 2ϕ fault in a microgrid supplied by a single inverter controlled in the NatRF (values in yellow are chosen as indicators of the presence of a fault) 196
6.4 $2\phi g$ fault in a microgrid supplied by a single inverter controlled in the NatRF (values in yellow are chosen as indicators of the presence of a fault) 196

6.5 $1\phi n$ fault in a microgrid supplied by a single inverter controlled in the NatRF (values in yellow are chosen as indicators of the presence of a fault) 197
6.6 $1\phi g$ fault in a microgrid supplied by a single inverter controlled in the NatRF (values in yellow are chosen as indicators of the presence of a fault) 197
6.7 Load unbalanced operation in a microgrid supplied by two parallel-connected inverters 200
6.8 3ϕ fault in a microgrid supplied by two parallel-connected inverters (values in yellow are chosen as indicators of the presence of a fault) 202
6.9 2ϕ fault in a microgrid supplied by two parallel-connected inverters (values in yellow are chosen as indicators of the presence of a fault) 203
6.10 $2\phi g$ fault in a microgrid supplied by two parallel-connected inverters (values in yellow are chosen as indicators of the presence of a fault) 204
6.11 $1\phi n$ fault in a microgrid supplied by two parallel-connected inverters (values in yellow are chosen as indicators of the presence of a fault) 205
6.12 $1\phi g$ fault in a microgrid supplied by two parallel-connected inverters 206
6.13 Zero sequence component of the phase-to-earth voltages for unbalanced operation and $1\phi g$ faults 207
6.14 Detection times for faults at F_1 218
6.15 Detection times for faults at F_2 218
6.16 Detection times for faults at F_3 219
6.17 Detection times for faults at F_1, parallel-connected inverters 223
6.18 Detection times for faults at F_2, parallel-connected inverters 223
6.19 Detection times for faults at F_3, parallel-connected inverters 224
6.20 Detection times for faults at F_4, parallel-connected inverters 224

Table of Symbols

C_f	-	Filter capacitance [F]
F	-	Feed-forward gain of the voltage controller
G	-	Inverter voltage gain
G_C	-	Current control loop regulator
G_{CC}	-	Current control closed loop transfer function
G_V	-	Voltage control loop regulator
i_L	-	Inverter inductor current [A]
i_{L_n}	-	Inverter neutral inductor current [A]
i_{Lsat}	-	Inverter saturated inductor current [A]
I_n	-	Nominal inverter output current [A]
i_0	-	Inverter output current [A]
L_{cc}	-	Coupling inductance [H]
L_{ccn}	-	Coupling neutral inductance [H]
L_f	-	Filter inductance [H]
L_l	-	Inverters interconnecting inductance [H]
L_{line}	-	Line inductance [H]
L_{linen}	-	Line neutral inductance [H]
L_n	-	Filter neutral inductance [H]
m_p	-	Real power droop gain of the power controller
n_q	-	Reactive power droop gain of the power controller
p	-	Instantaneous real power [W]
P	-	Real average Power [W]
P_{max}	-	Real power rating of the inverter [W]
q	-	Instantaneous reactive power [VAr]
Q	-	Reactive average power [VAr]
Q_{max}	-	Reactive power rating of the inverter [VAr]

R_{cc}	-	Coupling resistance [Ω]
R_{ccn}	-	Coupling neutral resistance [Ω]
R_f	-	Filter resistance [Ω]
R_g	-	Earthing resistance [Ω]
R_l	-	Inverters interconnecting resistance [Ω]
R_L	-	Load resistance [Ω]
R_{line}	-	Line resistance [Ω]
R_{linen}	-	Line neutral resistance [Ω]
R_n	-	Filter neutral resistance [Ω]
S	-	Apparent Power [VA]
S_{inv}	-	Nominal inverter output rating [VA]
V_{DC}	-	DC bus voltage [V]
v_i	-	Inverter bridge voltage [V]
V_n	-	Nominal inverter output voltage [V]
v_0	-	Inverter output voltage [V]
x_{abc}	-	Label for a general variable x expressed in the NatRF
$x_{\alpha\beta\gamma}$	-	Label for a general variable x expressed in the StatRF
$x_{dq\gamma}$	-	Label for a general variable x expressed in the SynRF
x_{pn0}	-	Positive, negative and zero sequence components for a general variable x
x^*	-	Reference value for a general variable x
Z_0	-	Inverter output impedance [Ω]
ω	-	System frequency [rad/sec]
ω_c	-	Cut-off frequency [rad/sec]
ω_n	-	Nominal frequency reference of the inverter [rad/sec]

List of Abbreviations

AC	-	Alternating Current
CHP	-	Combined Heat and Power
DC	-	Direct Current
DG	-	Distributed Generation
FCL	-	Fault Current Limiter
LOM	-	Loss of Mains
LV	-	Low Voltage
MV	-	Medium Voltage
NatRF	-	Natural Reference Frame
PMU	-	Phasor Measurement Unit
PV	-	Photovoltaic
RMU	-	Ring Main Unit
SS	-	Static Switch
SSTS	-	Solid Sate Transfer Switch
StatRF	-	Stationary Reference Frame
SVM	-	Space Vector Modulation
SynRF	-	Synchronous Reference Frame
UPS	-	Uninterruptible Power Supply
VSI	-	Voltage Source Inverter
3ϕ	-	Three-phase fault
2ϕ	-	Double phase fault
$2\phi g$	-	Double phase-to-ground fault
$1\phi g$	-	Single phase-to-ground fault
$1\phi n$	-	Single phase-to-neutral fault

Acknowledgements

I would like to express my deepest sense of gratitude to my supervisor Prof. Tim Green for giving me the opportunity to conduct this research and for his support, guidance, and encouragement throughout my PhD. His impressive knowledge, technical skills and creative thinking have been source of inspiration to me. Grazie Professore!

My special thanks go to Dr. Carlos Hernandez-Haramburo, Dr. Milan Prodanović and Dr. Nagaraju Pogaku for unlocking the secrets of power electronics and microgrids and for offering me assistance whenever I needed it. I am also grateful to Dr. John McDonald for our enlightening discussions on fault analysis and English language.

I wish to express my sincere gratitude to my PhD fellows and the whole Control and Power Group who made my staying over these years stimulating and enjoyable.

For all the inspiration, support, positive energy and friendship I am indebted to the Power Systems Ladies of the Group: Francoise, Sree and Vera.

Over these years the support and love of my family has been very important to me. I am therefore grateful to my loving husband Khalid and my dearest mother Annarosa.

If today I am an electrical engineer at the end of her PhD studies it is only because of my father Prof. Michele Brucoli. His exceptional humanity and inspirational academic life will always guide my steps. This thesis is dedicated to Him.

Chapter 1

Introduction

1.1 Background and scope

In recent years the number of small de-centralized power generators connected to the medium (MV) and low voltage (LV) distribution networks has increased. The term distributed generation (DG) defines an electric power source directly connected to the distribution network or to the customer side of the meter, which is small in size compared to conventional power plants, not centrally dispatched and not centrally planned [1,2]. Major drives behind the popularity of DG include the deregulation of the electricity market, the technical advances in small scale generation and the efforts of national governments to reduce gaseous emission and increase the production of green power.

The introduction of DG is changing the shape and the operation of the traditionally passive distribution networks which are now required to accommodate power generation [1–4]. The successful implementation of DG requires, first, the study of the impact on the network of the different DG power sources which include various technologies like synchronous generators, induction machines and power electronic interfaces. Second, it requires the development of solutions which can resolve the conflicts resulting from the connection of DG (e.g. voltage control, network protection and equipment upgrading).

The microgrid concept has been proposed as a possible answer to the coordinated integration and operation of DG [5, 6]. The main idea behind the microgrid concept is to group local power generators and loads and operate them as a single controlled entity within the main distribution network. For example, a microgrid can be operated in grid-connected mode or in islanded mode, it can be designed to meet local customers' needs (e.g. enhance local reliability or improve power quality) or it can be operated to meet grid's requirements (e.g. provision of ancillary services).

It is expected that power electronics will have a crucial role in microgrids [5–7]. Indeed, many DG sources cannot be directly connected to the network because they do not produce grid-compatible AC power. Some of them like photovoltaic (PV) units and fuel cells produce DC power while others like microturbines and variable-speed wind turbines produce power at frequencies different from the one of the distribution network (e.g. 50Hz in the U.K.) As a result, all these power units require some form of power electronics interface which can couple them with the distribution network. Another reason behind the importance of power electronic devices in microgrids lies in the flexibility of the control of these devices which can provide frequency and voltage control, synchronization functions and fast disconnection. These are all important aspects in the operation of microgrids as single controllable units. It follows that in future, distribution networks will contain more electronically-coupled power sources and that these types of sources will represent a substantial proportion of the generation mix in microgrids.

The high proportion of power electronic devices, in particular of inverters, requires the analysis of their control, operation and response to different events in the microgrid. However, while there is a well established body of work on power systems based on power generated by synchronous machines, there is a limited knowledge on the behaviour of power systems dominated by inverter-interfaced power generation. As a result, this thesis focuses on the study of islanded inverter-only microgrids, which are microgrids disconnected from the main grid and supplied only by inverter-interfaced DG sources.

The scope of the presented research work is three-fold. The first goal is to understand the behaviour of inverter-only microgrids in the event of a fault and analyze the main factors shaping the fault response. The second goal is to develop models which are capable of capturing the principle features of the inverter fault response and which can be used in numerical fault analysis. The third and final goal is to develop a fault detection strategy suitable for inverter-only microgrids.

1.2 Overview

The introduction of DG and the formation of microgrids have a profound impact on the operation of the protection system of the distribution network and this generates new requirements which the protection system has to satisfy [4, 8]. In particular, the formation and operation of a microgrid require a suitable protection system capable of adapting

to different microgrid operating modes (namely grid-connected and islanded) and to the different types of DG source which can be found in a microgrid [8].

In an islanded inverter-only microgrid where the only source of power comes from inverter-interfaced units, the detection and clearing of faults can be problematic because of the reduced fault current environment. Usually, faults in distribution networks are associated with high fault currents which are detected by overcurrent-based protection devices. Synchronous generators in the power system are capable of supplying such high currents. In contrast, inverters are usually designed to supply a very limited current (in the region of twice the inverter's nominal current). As a result, inverters' limited fault current capabilities make it difficult to detect the presence of a fault through overcurrent [8].

The fault protection of islanded inverter-only microgrids requires first an extended investigation into the fault behaviour of microgrids and in particular into the factors affecting the behaviour of inverters in the event of a fault. To date, little is known of the behaviour of inverters in the event of a fault apart from the general agreement that they provide only small currents. This simplicistic assumption is clearly not sufficient for the design of a protection system for two main reasons. First, there are a number of approaches to the control of inverters and therefore there is quite a lot of flexibility in the way inverters can supply a limited fault current. Second, as the inverters are the only source of power in the islanded microgrids under study, their response in the event of a fault is going to deeply affect the overall response of the microgrid.

As a result, this thesis first investigates the factors affecting the behaviour of microgrids in the event of a fault by analyzing inverter fault behaviour and the interactions with the microgrid network. In the thesis, an incremental approach is chosen where first a very simple microgrid supplied by a single inverter is considered. Then a more complex model with two parallel-connected inverters is introduced. The fault behaviour of the two microgrid models is investigated through time-domain simulations in the software PSCAD. This initial simulation work is quite important as it requires the analysis of all the possible factors (e.g. microgrid network topology, inverter current limiting and voltage ratings) influencing the behaviour of inverters and of the microgrid as a whole.

Nevertheless, studies based on time-domain simulations cannot be considered as exhaustive, most of all when there is not a consolidated body of work on inverter fault behaviour as there is for example for synchronous machines. Therefore suitable models

for inverters under fault conditions are developed in the thesis. As will be shown, the availability of these simplified but complete models brings several advantages. First, the developed models clearly illustrate the significance of different factors (e.g. control gains and filter parameters) which affect the overall behaviour of inverters in the event of a fault. Later this knowledge could be used to design alternative control strategies. Second, they can act as a first step towards the development of standardised fault models for inverter-interfaced DG sources (such as already exist for synchronous machines). A third advantage of the development of fault models for inverters is the possibility of performing numerical fault analysis. Indeed, the thesis shows how to integrate these models into quasi-steady state fault analysis studies. Ultimately these models can be used by power utility engineers for fault analysis and fault protection studies.

Finally the thesis demonstrates that in islanded inverter-only microgrids with reduced fault currents, faults can still be detected by measuring voltage sequence components. This proposed fault detection strategy is based on the analysis of the response of inverters during faults, on the time-simulations run in PSCAD and on the application of the inverter fault models in numerical fault analysis to compute the microgrid response to balanced and unbalanced faults at different locations. As the microgrid protection system is required to have fast operation, different fast-acting voltage detection techniques are compared and the ones more suitable for the evaluation of sequence components are chosen and implemented in PSCAD. Finally, the performance of the proposed fault detection is tested and discussed. Examples of how a protection system based on voltage can be implemented are given and the protection requirements of different microgrid models are described.

1.3 Thesis structure

The thesis is organized into the following chapters.

Chapter 2 starts with a literature review on distribution networks, DG, microgrids and the impact of DG on the protection system. Then, the focus is placed on the particular protection requirements of microgrids and on the approaches proposed so far. An example based on simulations of some microgrid models in PSCAD illustrates the difficulties in implementing an overcurrent-based protection system in islanded inverter-only microgrids.

Chapter 3 describes the different elements which need to be considered before inves-

tigating the microgrid fault behaviour: inverter DG topologies, earthing arrangements, microgrid network architecture, inverter control and inverter operation.

Chapter 4 shows and analyzes the fault response of islanded inverter-only microgrids. In particular three microgrid models (two supplied by a single inverter and one supplied by two parallel-connected inverters) are considered in order to investigate the impact of different inverter control strategies.

Chapter 5 develops inverter fault models and applies them in numerical fault analysis. The developed models are validated through comparison with the results of PSCAD time-domain simulations.

Chapter 6 develops and tests a fault detection strategy based on voltage sequence components. The final part of the chapter shows how a microgrid protection system based on voltage detection can be implemented.

Chapter 7 concludes the thesis, states the author's contribution and outlines possible future research work.

Chapter 2

Distribution networks, distributed generation and microgrids: the impact on power systems protection

2.1 Introduction

At the present time, one of the challenges faced by power engineers is to find solutions to integrate new forms of power generation like DG within the existing synchronous machine-based power system. In this Chapter a review and analysis of the impact of DG, and more specifically of microgrids, on the protection system of a distribution network is given. New key concepts are introduced along with a description of well established technologies like overcurrent relays and protection practices in distribution networks.

Following a description of common problems encountered by the protection system when DG is present and a review of some proposed solutions, the Chapter analyzes the protection requirements of microgrids. In particular, the focus is placed on inverter-only microgrids. With the help of the simulation software PSCAD, fault currents in a grid-connected microgrid with one or two locally connected DG units are compared with the fault currents in the same microgrid operating in islanded mode. Difficulties in using overcurrent protection in inverter-only microgrids are discussed and finally a review of the limited available research on microgrid fault protection is given.

2.1.1 Distribution networks and distributed generation overview

The function of the electricity distribution network is to deliver electrical energy from the transmission network delivery point to each customer [9]. On the basis of this function, the distribution network is usually designed to operate in a radial configuration, in which the power flows in one direction only and little redundancy exists. The liberalization of the energy market together with the global trend of reducing greenhouse gas emissions and the technical advances of small scale energy generation have powered the introduction of DG into the distribution network [1, 2]. As a result, distribution networks with DG are being transformed from passive to active networks.

DG technologies available on the market range from traditional power sources like diesel generators to new technologies like microturbines, fuel cells, photovoltaic systems and wind turbines [2]. As a result, DG requires different generator technologies. Synchronous generators are typically used by internal combustion engines, gas turbines, solar thermal and biomass plants. Induction generators are extensively used in wind farms while power electronic converters are used to interface photovoltaic systems, fuel cells and microturbines. As wind turbines have become variable-speed, they also have included some power electronics. Overall the term DG refers to an extremely heterogeneous group of power generators.

Sometimes the term DG is associated with renewable energy resources however not all DG technologies are environmentally friendly. Nevertheless the introduction of small scale, local energy generation in the distribution network brings several benefits like [2]:

- diversification of energy sources,
- reduction in gaseous emissions,
- possible reduction of energy losses in distribution networks,
- private production of electrical energy,
- provision of services (power quality and reliability) to meet local customers needs.

Besides these benefits, there are some technical issues raised by the integration of DG into the existing distribution network (e.g. voltage control and network protection) which need to be addressed. Indeed, as DG is installed, the network becomes fed by multiple sources

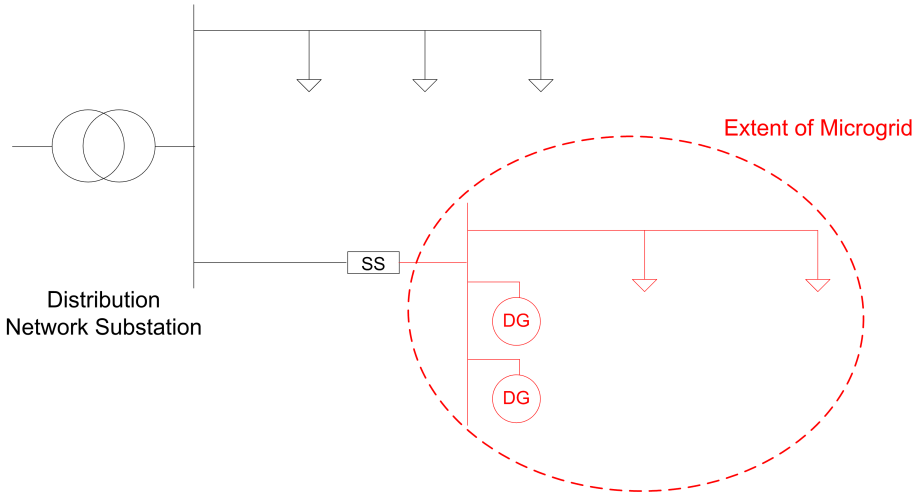


Figure 2.1: A simple example microgrid

but its topology, control and protection were all designed assuming that power flows in one direction only. The connection of DG affects the network performance and stability in a number of ways as it has been reported in the literature [1–4]. In particular, Section 2.2 is going to describe and analyze the impact of DG on distribution network protection.

2.1.2 Microgrids

The microgrid concept has been introduced as a possible approach to coordinated network integration and operation of DG [5]. Although there isn't a standard definition, a microgrid can be considered as a cluster of loads and DG sources capable of operation as a single controllable unit [6]. Usually, a microgrid is a small part of the MV (usually ≈1-69 kV) or LV (usually ≤1 kV) distribution network [5] where the power and possibly also the heat demand are supplied by local small (≤100 kW) power resources (including PV units, micro turbines, fuel cells, etc.) and storage devices (e.g. flywheel and batteries) [7]. A microgrid is interconnected to the remaining network through a separation device like a solid state static switch (SS) which is capable of quickly disconnecting or connecting the microgrid [6]. Figure 2.1 illustrates a basic example of a microgrid connected to the distribution network through a SS.

As a single controllable unit, a microgrid can be operated either in grid connected or in islanded (autonomous) mode depending on factors like planned disconnection, grid outages or economical convenience [10, 11]. When operating in grid connected mode, the DG sources are controlled as constant power sources so that they inject into the network a

set amount of power while using the grid voltage and frequency as a reference. In islanded mode the sources are controlled in order to maintain the voltage and frequency within acceptable limits. This flexibility of operation is only made possible through the extensive use of power electronics as an interface between the DG sources and the network [6].

Although the operation of a microgrid poses a series of technical, operational and economical challenges [6, 12], it provides an effective integrated connection of DG into the network [5]. Therefore all the benefits of DG operation can be extended to microgrids. Moreover, as a single controllable unit, a microgrid can be operated to satisfy particular customers' needs like enhancement of local reliability, uninterruptible power supply, increased efficiency and environmental and economic benefits [6, 11].

For all these reasons, the microgrid concept is considered to be a key player in the future of the distribution networks and as a result there is a big effort by the research and industry community from all over the world to make this concept a reality. Large scale projects are running in Europe (Microgrids and More Microgrids), in USA (the CERTS Microgrid and the GE Global Research Microgrid), in Japan (NEDO Microgrid project), in Canada and in UK (Supergen Microgrids Work Package) [5].

The challenges in the development of a microgrid are very broad and span the range from network voltage and frequency control [6, 7] to unit commitment for fuel minimization [11]. Among them, this research work is focused on understanding how an islanded microgrid supplied by DG interfaced with inverters behaves in the event of a fault and which fault detection strategies can be used when the available fault current is limited by the inverter's reduced current capabilities.

2.1.3 Conventional distribution network protection

The primary purpose of power system protection is to ensure the safety of people, personnel and equipment during the operation of the power system [13]. A good protection system should be designed following these principles:

- Reliability: a protection system should operate correctly. By correct operation is meant the ability to discriminate between faults and events which do not require any action.
- Selectivity: a protection system should isolate the fault by disconnecting the minimum section of the network.

- Speed: a fault has to be cleared in the minimum possible time in order to avoid dangerous situations for people and damage to equipment.

Different network topologies require different protection schemes. The distribution network is usually operated radially therefore overcurrent protection is considered to be a good compromise between performance and cost. Directional relays are also required for looped networks because of the bi-directional nature of the power flow. Protection schemes commonly used in transmission networks like unit or distance protection [13] are not frequently found in distribution networks.

The main principle on which overcurrent protection is based is that faults in the network generally produce very high currents in comparison to nominal load values. Moreover, faults in different parts of the network cause currents of different magnitudes because of the varying impedance between power source and fault point [13]. The coordination of protective devices within a grading path is important in order to achieve good service continuity and selectivity through the minimisation of disconnected plant. In the event of a fault, devices are coordinated so that the one nearest to the fault operates first. In this way the fault is isolated while power is still supplied to as many unaffected loads as possible. As the power flow is unidirectional, this coordination is relatively easy to achieve as faults further down the feeder have lower fault current because of the higher impedance between source and fault.

The devices based on overcurrent protection which are commonly used in distribution networks are overcurrent relays, fuses, reclosers and sectionalisers. Overcurrent relays are classified based on their time/current operating characteristics as: definite-current, definite-time and inverse-time. Definite-current relays operate instantaneously when the current reaches a preset value. In contrast, definite-time relays operate in a fixed time as the current reaches the limit. Inverse-time relays operate in a time which is inversely proportional to the fault current. As an example, Figure 2.2 shows the coordinated operating characteristics of four overcurrent relays in a radial feeder. Each relay is supplied with an instantaneous element and a time inverse element. In the event of a fault, their time coordination is set in a way that the nearest device to the fault opens first.

An important feature in distribution networks which affects the design of the protection systems is the transient nature of the majority of faults (around 80-90%) [9]. A common practice is to disconnect and re-connect the faulted circuit a number of times in

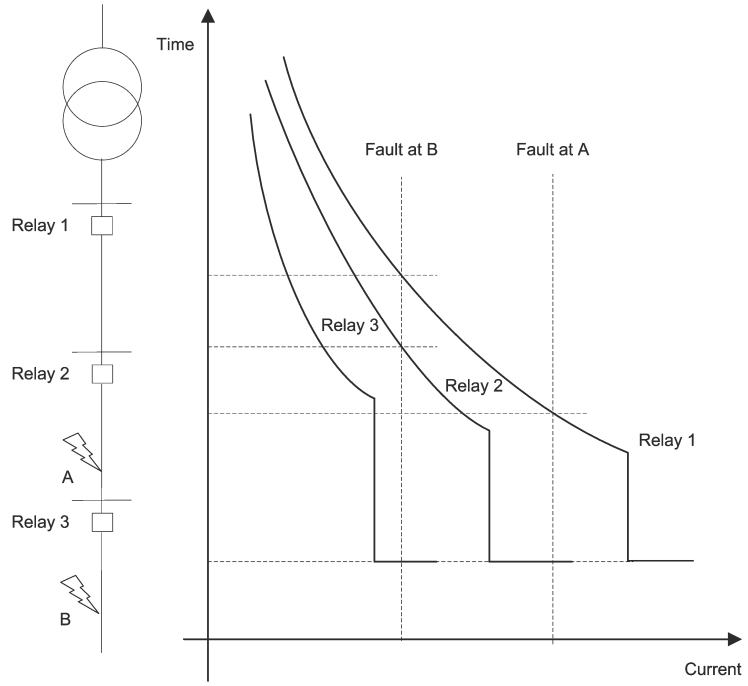


Figure 2.2: Radial coordination of inverse and instantaneous overcurrent elements

order to allow the clearing of the fault without permanently disconnecting the faulted part of the network. This practice is made possible by using a recloser which is a device capable of detecting and interrupting an overcurrent and then automatically closing to re-energize the feeder. Usually a recloser has different inverse time/current operating characteristics to allow fast and slow operation [13]. If the clearing process is unsuccessful and the fault is permanent, then the coordination between the recloser and devices like sectionalisers and fuses permits the selective isolation of the fault [13].

Figure 2.3 shows a typical configuration with a recloser and sectionalisers on derived feeders. A sectionaliser is a disconnector which is not capable of breaking fault current but can carry it. It counts the number of passages of fault current, during the opening and closing sequence of the recloser, and trips off as soon as a set limit is reached when the recloser is open [13]. When the fault in Figure 2.3 is detected, the recloser trips off thus giving the fault a chance to clear. After a set time, the recloser closes and detects whether the fault is still present or not. If the fault is still present the recloser trips off again for a longer set time. If once the recloser is closed again, the fault is still present, then the recloser opens again and the sectionaliser on the faulted feeder trips off.

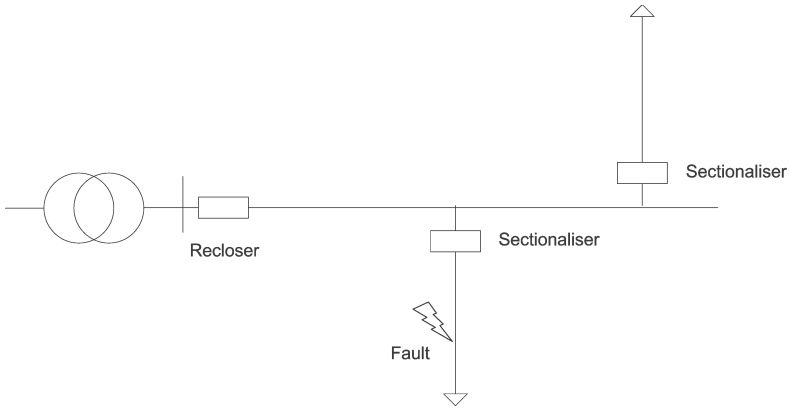


Figure 2.3: Recloser and sectionalisers in a distribution network

Another popular configuration uses a recloser and fuses at the load sides. A fuse is a device with an inverse time/current characteristic which is capable of interrupting fault current by the melting of one of the fuse's components. The zone of operation of a fuse is limited by a lower curve based on the minimum melting time of the fuse and an upper curve based on the maximum fault clearing time of the fuse. The coordination between recloser and fuses is based on the principle that the fuse should operate only for a permanent fault on the load feeder. In order to achieve this, the fast curve of the recloser should lie below the minimum melting time characteristic of the fuse in the rage of fault currents for which they are coordinated and the total clearing time characteristic of the fuse should be below the slow curve of the recloser. The recloser usually goes trough a sequence of two fast operations and, if the fault is permanent the fuse operates before the third opening [13].

2.2 Impact of DG on distribution network protection

2.2.1 Impact on fault current levels

The introduction of DG alters the topology of the distribution network and the power flow patterns. As described, overcurrent protection is widely used in distribution networks, therefore an analysis of the impact of DG on the protection system has got to start from the analysis of the impact of DG on fault current levels.

The way in which DG influences fault current levels depends on the type of generator, on the generator size and location. Table 2.1 provides some typical fault current levels for different types of generator [4]. The fault current contribution of a DG system with

Table 2.1: Fault current levels for different types of generators

Type of generator	**Fault current into shorted bus terminals as percent of rated output current**
Inverter	100 - 200%
Separately excited synchronous generator	Starting at 500 - 1000% for the first few cycles and decaying to 200 - 400%
Induction generator and self excited synchronous generator	Starting at 500 - 1000% for first few cycles and decaying to a negligible amount within 10 cycles

power electronic converter is limited by the actions of its control which usually limits the supplied fault current to a value equal two times the nominal current [14]. In [15] it is clearly stated that *"solid-state inverters do not behave like rotating generators. Solid-state inverters have no inertia and can respond immediately to changes in the ac power system. These inverters generally sense a short circuit by an associated voltage drop, rather than by actually sensing short circuit current"*. As this voltage drop is sensed, the response is dependent on the implemented control scheme which limits the current to a maximum value. This small contribution to the fault current is positive from the point of view of the existing coordination of the protection system but can become an issue when an island is formed and, in the event of a fault, the current produced is small and comparable with nominal values. This problem will be discussed later in Section 2.4.

A synchronous generator is able to feed prolonged fault currents. The supplied fault current increases as the generator' size increases. On the other hand, induction generators behave differently to synchronous machines because they receive their excitation from the line. So, for example, if a three phase fault occurs at the terminals of the machine, the excitation is completely lost and the machine will feed the fault for a few cycles because of its gradually decaying rotor flux excitation.

Usually, installing a DG system in the distribution system increases the value of the fault current at the fault point thus requiring some upgrading of the equipment of the network. Indeed, with DG in the network, the number of parallel circuits is increased and therefore the equivalent Thevenin impedance of the network is reduced. Moreover the

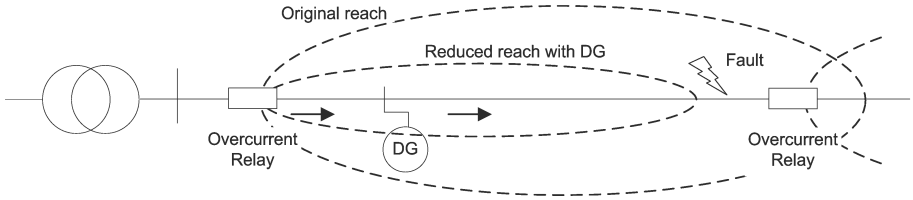


Figure 2.4: Relay protection zone without and with DG

presence of DG alters the original radial topology and passive nature of the distribution network by, in some cases, reversing the flow of current in the event of a fault [16–18].

2.2.2 Impact on overcurrent protection

The presence of DG on a feeder affects the operation of the existing protection system by increasing the fault current level, as described in the previous Section, causing bi-directional power flow and varying the network topology. The following Sections briefly describe some of the issues regarding the impact of DG on overcurrent protection.

Prevention of overcurrent relay operation (Under-reach)

The installation of DG on a feeder can alter the current seen by the feeder protection thus preventing the correct operation of the overcurrent relay [19]. This problem is referred to as protection under-reach. Overcurrent relays are set to protect a certain section of a feeder, this means that they are set to operate for a minimum current which corresponds to a fault at the end of the protected section of the feeder. This is sometimes referred to as the "reach"of the device [17]. When DG is present between the relay and the fault, a fault at the end of the protection zone will produce an increased current at the fault point but a decreased current at the relay point. So, the relay will react as if the fault is further down the feeder, outside its protection zone and therefore will not operate, as shown in Figure 2.4. The reduction of the fault current at the relay point becomes more pronounced as the size of DG increases and as the fault moves far away from the DG.

False tripping

As mentioned before, the presence of DG causes a bi-directional power flow in the network which can cause mal-coordination between the protective devices. Figure 2.5 shows that a fault on feeder 1 is also fed by the DG on the adjacent feeder 2. In order to clear this

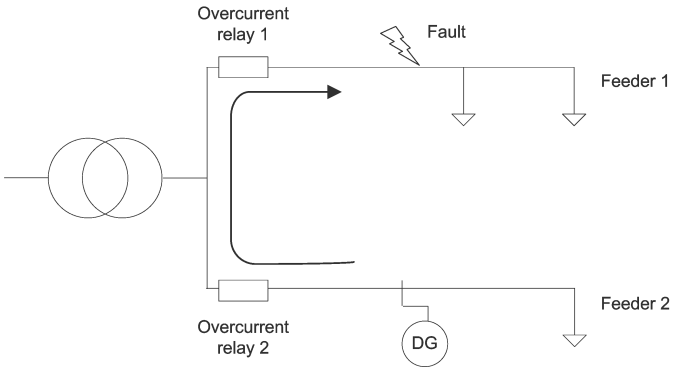


Figure 2.5: Example of false tripping

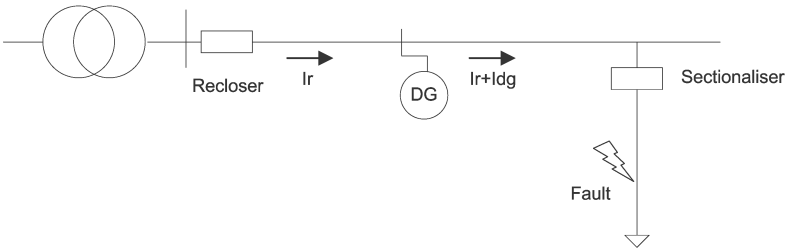


Figure 2.6: Impact of DG on recloser and fuse coordination

fault, only relay 1 should initiate the tripping of its breaker however, because of the DG fault contribution, relay 2 also sees a fault current. As a result, both breakers open and loads on the healthy feeder 2 are disconnected. This problem can be solved by equipping breakers with directional relays [4].

Reclosing

Reclosing and DG are incompatible for several reasons. First, as soon as the recloser opens, DG has to be disconnected as well, in order to give the fault arc sufficient time to dissipate [20]. If DG disconnects late, there is a chance that the fault may take longer to clear, thus creating further stress to the equipment and a longer interruption for customer loads. DG can even prevent the arc extinction and change a transient fault into a permanent one.

Second, the presence of DG increases the fault current at the point of fault, therefore, for a fault on a feeder with a fuse, the fuse sees more current ($I_r + I_{dg}$) than the recloser (I_r) as shown in Figure 2.6. As a result of this disparity, the coordination between the two devices is lost and the fuse may blow before the recloser can operate properly [21].

Third, DG should be disconnected before the recloser closes in order to avoid an

out-of-phase reclosure [17]. Indeed, once the recloser, which directly provides connection between the DG unit and the distribution grid, trips off, the embedded generator accelerates or decelerates and soon is out of phase with the utility source of supply. When the reclosure happens, the two systems are out of synchronism and the interconnection can cause damage to the DG and disruption to the network. In order to avoid this problem, a reclosure interval of 1.0 s or more should be used [17].

Unintentional Islanding

The operation of protection devices in the event of a fault results in the disconnection of a network section from the main grid supply. If DG is present in the disconnected area, then power supply in this area might still be possible. This possibility depends on the ratings of the DG units and on the load demand in the formed island. The term used to describe this condition in which a part of the network is energized by DG while being disconnected from the main grid supply is "islanding".

Unless the network and DG have been carefully planned and designed to operate in islanded mode, as in microgrids, unplanned islanding can be very dangerous for people and equipment [2]. As a result standards such as Engineering Recommendation G59/1 [22] and IEEE P1547 [23] do not permit islanding operation and recommend a series of methods to detect this loss of mains (LOM) and require disconnection of DG units. Usually a change in voltage or frequency is enough to detect LOM however it may happen that the formed island is quite well balanced and therefore alternative methods for detecting LOM have to be used [2]

2.2.3 Approaches to the design of a suitable protection system for distribution networks with DG

In order to reduce to a minimum the adverse impact of DG, the relevant DG interconnection standards and the distribution network operators usually require DG units to disconnect as soon as abnormal conditions arise in the system. According to the IEEE P1547 [23] a DG should disconnect in the event of a contingency in the network. The standard gives reference voltage and frequency windows and the DG units have to disconnect within a set time as soon as the system voltage and frequency go outside the specified range. Moreover, as mentioned previously, the standard does not allow DG units to operate in islanded mode. Similar requirements can be found in the Engineering

Recommendation G59/1 [22] and in the IEEE Standard for PV systems [15].

These standards can be considered quite dated as they have been written assuming only a small presence of DG units in the distribution network. However as the number and size of DG units increase in the network, the standards' approach of disconnecting DG in the event of a disturbance can have a serious impact on the performance of the power system [18, 24]. Indeed as the system is undergoing a disturbance (e.g. a frequency deviation) it is generally not advisable to disconnect even more generation and thereby exacerbating the disturbance [25]. System disturbances may even cause DG nuisance tripping because of the restrictive settings of the disconnecting devices. So for example, a voltage drop caused by a fault on an adjacent feeder may trigger the undervoltage trip of protection devices placed at a DG unit [24].

These restrictive disconnection rules not only undermine the performance of the power system but also limit the potential of DG to improve the reliability and the quality of power supplied in the event of a disturbance. Moreover, if DG units are required to be disconnected and islanding cannot be tolerated, then islanded microgris cannot be formed and therefore the advantages of operating them cannot be passed to customers and network operators.

A sign of the need for updating DG connection standards comes from the recent development of new transmission grid codes requiring fault ride-through capabilities of wind farms [26, 27]. Wind power has experienced an incredible annual rate growth of around 20% [27] in recent years. Previously, when the concentration of wind energy was fairly low, wind farms would disconnect from the power system during a fault. Now, however, the high level of wind penetration has raised the need to review grid codes in order to preserve the stability of the system. Many grid codes now require wind farms to remain connected during network faults according to a voltage versus time curve [26]. One of them, the E.ON Netz grid code, goes even further by specifying the amount of reactive current which should be supplied by the wind turbine during the fault.

It can be easily predicted that as DG becomes as diffused in the distribution network as wind power is in the transmission network, the old DG interconnection standards will be revised to allow more flexible operation of DG during network disturbances. As support for this prediction, islanded operation is currently being considered and the IEEE SCC21 is working on a guide for the operation and integration of islanded systems in the distribution

network [28].

Overall, the increase of penetration of DG requires a more sophisticated approach, compared with the simple DG disconnection philosophy, in which first the system impact of DG is assessed and then suitable interconnection standards proposed. Therefore, assuming that DG units are going to remain connected during network disturbances, the following Sections describe approaches to the integration of DG into the protection system of distribution networks.

Network fault analysis

If simple DG disconnection is no longer an option, new methods of integrating DG with the protection system have to be developed. The study of the impact of DG on the protection system and the resulting proposal of suitable solutions for the integration of DG in the protection system has to start from the analysis of the system behaviour in the event of a fault [4, 18]. In general the fault contribution of one single small DG unit is not large however the aggregated contribution of DG units can alter the short circuit level in the distribution network [4]. Therefore in the presence of multiple DG units, even inverter-interfaced DG units, which usually are ignored because of their limited fault current capabilities (see Table 2.1), have to be considered and included in fault analysis [29].

In traditional passive and radial distribution systems where the power comes from one single source which is the substation, fault calculations are quite simple and require very little computational effort. The introduction of DG brings two main challenges in fault analysis. First, as the network is now active with bidirectional power flows, fault calculations now require the use of network analysis methods thus increasing the computational effort. Fault analysis based on the Z_{bus} method can be used [30], however, more commonly the impact of DG is analyzed with simulation packages like PSCAD or SimPower Systems for Matlab/Simulink [31]. Second, DG includes many different technologies whose response in the event of a fault may not be well known. Synchronous and induction machines have been extensively studied and modelled, but very little is known about the fault response of inverter-interfaced DG units.

So far, only two studies [29,32] have tried to include the fault contribution of inverter-interfaced grid-connected DG units. In [29] the authors develop some form of approximated

model which is integrated into a quasi steady-state load flow method. The results of this method compare well with those from simulation and the authors have produced a rather original and innovative piece of work in this field. However the derivation of the inverter's model is not completely rigorous as it is based on observation of the inverter's response during simulations in EMTP. Moreover, little is mentioned about the inverter's control and its response in fault conditions. On the other hand, the fault analysis with inverter-interfaced DG presented in [32] does not provide an efficient method or any insight because the calculations are done by solving the state-space representation of the system, including the inverters, through numerical integration.

In both studies [29,32], the inverters retain the grid connection therefore the system fault behaviour is dominated by the contribution from the grid. To date, there are no reported studies on the analysis of fault behaviour of islanded microgrids supplied by inverter-interfaced DG units where the fault response is strongly dictated by the inverter control. More work is clearly needed to develop simplified but complete models which can capture the fault behaviour of inverters and then which can be integrated in numerical fault analysis.

Advances in protection of distribution networks with DG

Various methods have been proposed to facilitate the coordinated operation of the network protection system in the presence of DG. One possible approach is to prevent or reduce the increased fault current levels caused by DG (mainly synchronous machine units) using a Fault Current Limiter (FCL) [33]. An FCL is an additional current limiting impedance which reduces the contribution to fault current by DG units. Under normal operation, the impedance of the FCL is very small and therefore its presence does not influence the normal operation of the system. If a fault occurs and an excessive fault current flows in the system, the FCL detects it and introduces a large impedance in the line. The use of FCLs minimize the impact of DG units during faults without having to modify the coordination of the existing protection schemes or change protection devices [34]. However, there are still some costs associated with the implementation of FCL, the impact on reclosing seems still to be unsolved and studies are required to select the right limiting impedance [33,35].

Another approach to integrate DG into the distribution network protection system is to redesign the protection schemes with DG in mind. Some methods focus on existing

protection practices [21, 36, 37], while others propose protection schemes based on new concepts like phasor measurement units (PMU) [16], fault transient directional relays [38] and multi-agent systems [39].

In [21] the problem of coordination between reclosers and fuses is achieved by using microprocessor-based reclosers but even so, DG units downstream of the recloser have to be disconnected before the first reclose in order to avoid out-of-phase reclosure. The solution proposed in [36] is based on adaptively changing the relay pick up current depending on the total amount of power injected by DG. The idea of adaptively changing the protection settings as the level of DG changes is quite interesting but the authors do not give a detailed explanation of how this can be achieved and a more detailed study would be needed. Distance relaying applied to an 11kV network to facilitate the connection of DG is described in [37]. The main proposed idea is to use the available 11kV ring main unit (RMU) and add some extra information to incorporate a distance relay. However this solution is strictly dependent on the presence of RMUs in the network which, as the authors themselves state, is not yet widespread.

Turning now to new technologies, in [16] an adaptive protection scheme based on the use of PMUs and aimed at keeping most of the DG connected in the event of a fault is proposed. The scheme requires the division of the network into several zones which are capable of islanded operation. The zones are inter-connected with breakers capable of remote communication and synchronization-check functions. A main relay is placed at the substation with the function of receiving signals measured with PMUs from breakers and DG. The main relay will process the data, start the fault clearing process and follow this by system restoration. Although this protection scheme proposes a more complete and correct approach to the integration of DG, it requires the use of communication, the installation of PMUs and the capability of DG units to operate also in islanded mode.

Communication is also needed to implement the protection scheme based on directional overcurrent transients which is proposed in [38]. As communication has a limited presence in distribution network, these proposed protection schemes do not have an immediate application. Similarly the agent-based protection proposed in [39], which is based on communication and requires an extensive use of data processing tools like wavelet transformation and neural networks, does not seem to offer a cheap and easy to implement solution.

Overall, it can be said that there is a lot of interest in the development of improved or new protection systems to accommodate DG. However, many of the proposed solutions require the installation of new equipment and also the use of communication. Therefore their successful implementation depends on the willingness of operators of distribution networks to invest in the system.

2.3 Protection issues with DG and microgrids

The previous paragraphs in general described the impact of DG into the protection system of the distribution network. If the penetration of DG is such that microgrids can be formed, then the protection system needs to be designed not only to operate correctly with DG but also to satisfy the particular protection requirements of microgrids in grid-connected and islanded mode. This is not an easy task because network topology and power flows can change dramatically from grid-connected to islanded operation. As a result, the protection system may have different settings or even different working principles (i.e. overcurrent, distance, etc.) depending on the microgrid mode of operation.

The protection issues raised by the operation of a microgrid inside a distribution network [8] can be summarized as:

- protection for faults outside the microgrid;
- protection for faults inside the microgrid when the microgrid is connected to the distribution grid;
- protection for faults inside the microgrid when islanded.

The following paragraphs will discuss each of these issues in turn.

2.3.1 Protection for faults outside the microgrid

One of the main advantages of operating a microgrid is the possibility of supplying critical loads even in the event of network disturbances. References [6, 8, 40] propose the use of a fast acting disconnecting device like a SS capable of isolating the microgrid from the rest of the network. This SS has the important role of discriminating between events which require the disconnection of the microgrid and events which do not require any action. Moreover it has to act very quickly, 0.5 to 2 cycles [40], in order not to have any conflicting operation with the remaining protection system in the distribution network.

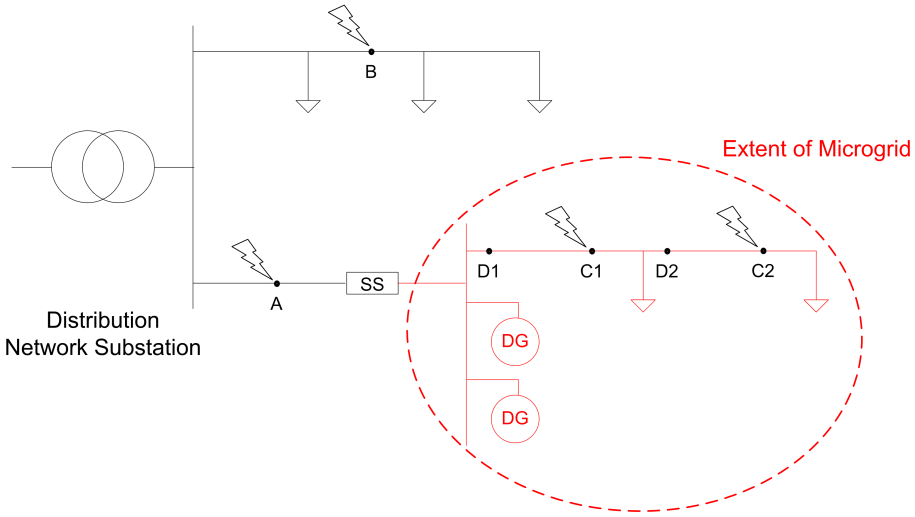


Figure 2.7: Example of faults outside the microgrid

In Figure 2.7, three possible faults located around and in a microgrid are shown, each of them requiring different actions. Faults on the feeder between the distribution network substation and the SS, like fault A in Figure 2.7, require immediate disconnection of the microgrid from the network in order to keep supplying power to customers and to stop "feeding"the fault. On the other hand, a fault on another part of the network like fault B in Figure 2.7, does not require any disconnection. Indeed, maintaining the connection between the utility which is experiencing some form of disturbance and the microgrid is desirable [18, 24, 25]

The discrimination between the two types of fault based on information (such as voltage and current) at the microgrid disconnection point is not always easy. Usually, a fault generates a voltage drop and a high current but identifying its location is not straight forward. If the microgrid has a robust design and can reliably supply loads, then the issue of discrimination is not very serious and some nuisance separations can be tolerated. In this case, the SS can be easily set to operate if the voltage goes outside a certain range regardless the position of the fault. This strategy can create some problems if the microgrid is exporting power or if the formation of a microgrid requires some form of load shedding [8]. Therefore, generally speaking, the microgrid should be islanded only for faults on the feeder between the distribution substation and the SS. A solution to this problem can be the use of some communication link between the substation and the SS [8].

2.3.2 Protection for faults inside the microgrid when the microgrid is connected to the distribution grid

The protection of grid-connected microgrids from internal faults has much in common with the general issue of protection in the presence of DG as discussed in Section 2.2 and as a result, some of the approaches described in Section 2.2.3 can be used. However the presence of the SS and the opportunity for disconnecting the microgrid add a new dimension to the problem of protection for faults inside grid-connected microgrids.

First the SS has to be able to make a distinction between faults inside and faults outside the microgrid in order to take appropriate action. Indeed for a fault inside a grid-connected microgrid, like fault C1 (or C2) in Figure 2.7, the choice of tripping or not the SS requires different protection strategies. If for a fault at location C1 (or C2), it is chosen to keep the connection with the distribution grid, then approaches to fault protection like the ones described in Section 2.2.3 can be used. On the other hand, if it is decided to open the SS and disconnect the microgrid, then the fault becomes equivalent to a fault in an islanded microgrid which will be discussed in the next Section. The choice of disconnecting the microgrid for internal faults could be advantageous as the protection scheme and the settings are the same for microgrids in grid-connected and islanded modes of operation, as described in [40].

2.3.3 Protection for faults inside the microgrid when islanded

An islanded microgrid can be considered as a completely new network which operates independently from the main grid. From the point of view of the protection system, in the event of a fault, the islanded microgrid is likely to have new current flows as the main grid fault current supply is lost and now only microgrid DG units contribute to fault current. For a fault at C1 (or C2) in Figure 2.7, the islanded microgrid will not experience different fault current directions from the grid-connected case as the DG units are placed right at the beginning of the microgrid feeder. The only difference will be in the magnitude of the fault currents depending on the type of DG units (i.e. synchronous generators, induction generators or inverters). On the other hand if the microgrid is more complex with more feeders and scattered DG sources along them, see Figure 2.8, then fault currents are likely to be different in magnitude and directions from the grid-connected case.

If the DG units present in the microgrid are synchronous machine-based, then there

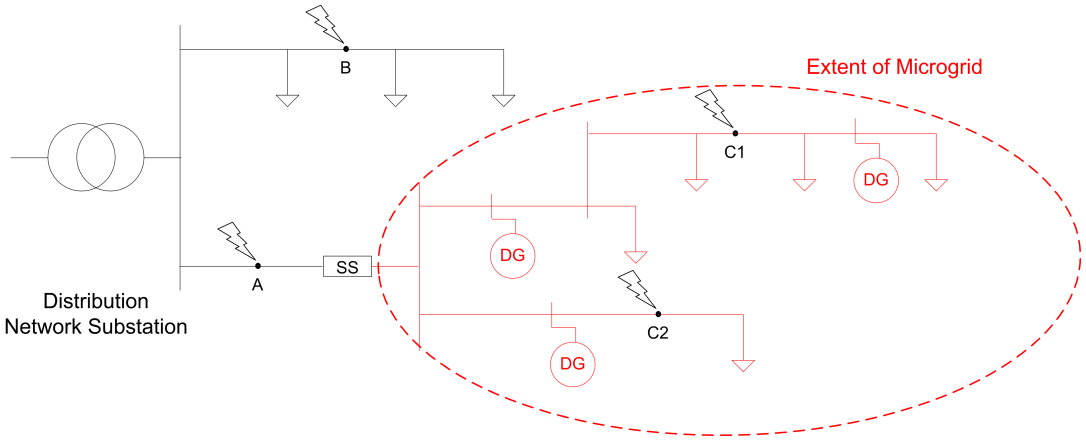


Figure 2.8: Example of a more complex microgrid network

may be enough fault current to operate the existing overcurrent protection system. However, as the network topology has changed, the coordination could be lost and some form of alternative solution (e.g. change of settings) might have to be put in place. This is a quite challenging problem as the network is required to have a protection system which has to work properly in both grid-connected and islanded mode. Nevertheless, the availability of fault current in islanded mode makes possible to use the same protection system albeit with adaptive settings to cope with two different conditions. For the case of an islanded microgrid which is supplied by inverter-interfaced DG units only, the existing overcurrent protection devices do not operate correctly as there is not enough fault current to operate them [8, 41]. The following Sections are going to describe in more detail the protection issues raised by islanded inverter-only microgrids.

2.4 Protection issues with islanded inverter-only microgrids

2.4.1 Fault currents in islanded inverter-only microgrids and impact on overcurrent protection

The ability of an inverter to process overload currents and therefore the available inverter fault current are not standard values and very much depend on the inverter's manufacturer [42,43]. Every inverter model is designed for a range of current and each has a specification for how much overcurrent over a length of time the inverter can supply. Generally inverters can supply a maximum current in the event of a fault that is typically only twice the nominal inverter load current [14]. Higher fault current capability can be achieved by

Table 2.2: Fault currents for a three-phase fault in a grid-connected microgrid with one inverter-interfaced DG source

	3ϕ fault at $C1$			3ϕ fault at $C2$		
	$I_a[A]$	$I_b[A]$	$I_c[A]$	$I_a[A]$	$I_b[A]$	$I_c[A]$
$D1$	811.6	812.2	811.3	430	431.2	430
$D2$	0	0	0	424.8	425.9	424.6

Table 2.3: Fault currents for a three-phase fault in a grid-connected microgrid with two inverter-interfaced DG sources

	3ϕ fault at $C1$			3ϕ fault at $C2$		
	$I_a[A]$	$I_b[A]$	$I_c[A]$	$I_a[A]$	$I_b[A]$	$I_c[A]$
$D1$	817.8	818.5	817.4	433.8	434.4	433.6
$D2$	0	0	0	428.3	429.13	428.0

increasing the rating of the inverter. However, as a result, costs are increased [42, 43].

In order to illustrate the differences between fault currents in a typical distribution network and fault currents in an islanded inverter-only microgrid, the distribution network with the microgrid shown in Figure 2.7 was built in the simulation package PSCAD and a three-phase fault was applied first at location C1 and then at location C2. The following four case studies are considered:

- Grid-connected microgrid with one inverter-interfaced DG source
- Grid-connected microgrid with two inverter-interfaced DG sources
- Islanded (SS open) microgrid with one inverter-interfaced DG source
- Islanded (SS open) microgrid with two inverter-interfaced DG sources

The main distribution network in Figure 2.7 is assumed to have a short circuit level of 100 MVA at 20 kV and at the substation there is a 20/0.415 kV delta/wye grounded transformer. Each DG unit is interfaced with a 17 kVA inverter with a nominal output current of 23.6 A. In the microgrid there are two resistive loads of 5.76 kW (three-phase) each connected along the line.

Tables 2.2 and 2.3 show the fault currents (peak phase value) at points D1 and D2 (where overcurrent protection relays could possibly be located) for a three-phase fault

Table 2.4: Fault currents for a three-phase fault in an islanded microgrid supplied by one inverter-interfaced DG source

	3ϕ fault at $C1$			3ϕ fault at $C2$		
	$I_a[A]$	$I_b[A]$	$I_c[A]$	$I_a[A]$	$I_b[A]$	$I_c[A]$
$D1$	66.24	66.24	66.24	66.29	66.31	66.23
$D2$	0.014	0.007	0.004	65.49	65.48	65.45

Table 2.5: Fault currents for a three-phase fault in an islanded microgrid supplied by two inverter-interfaced DG sources

	3ϕ fault at $C1$			3ϕ fault at $C2$		
	$I_a[A]$	$I_b[A]$	$I_c[A]$	$I_a[A]$	$I_b[A]$	$I_c[A]$
$D1$	132.68	132.69	132.65	132.68	132.69	132.67
$D2$	0.02	0.01	0	131.48	131.52	131.50

applied at points C1 or C2 when the microgrid (with one or two DG sources) is connected with the distribution network. These values should be compared with the corresponding ones for the islanded microgrid supplied by one (see Table 2.4) or two parallel connected inverter-interfaced DG units (see Table 2.5). In grid-connected mode, fault currents are almost independent of the number of DG sources connected in the microgrid, with a fault current around 430 A for a fault at C2 and a fault current around 815 A for a fault at C1 (see Tables 2.2 and 2.3). In contrast, Tables 2.4 and 2.5 show that fault currents are very much affected by the number of DG sources in the islanded microgrid. Independently of the location, a fault in an islanded microgrid with one DG source produces a fault current around 66.2 A while with two DG sources the fault current is around 132.50 A. The available fault current in the islanded inverter-only microgrid is really small compared with that in grid-connected mode. A microgrid supplied by one single inverter has a fault current equal to $\frac{1}{12}$ of the corresponding fault current in grid-connected mode. For two parallel inverters the ratio rises to $\frac{1}{6}$ as both inverters are injecting current into the network.

Tables 2.2, 2.3, 2.4 and 2.5 should be compared with Tables 2.6 and 2.7 which show currents at locations D1 and D2 during normal loading conditions for a grid-connected microgrid (supplied by one or two inverters) and an islanded microgrid (supplied by one or two inverters). While there is a substantial difference between fault currents and normal

Table 2.6: Normal operation in a grid-connected microgrid

	Microgrid with one DG			Microgrid with two DGs		
	$I_a[A]$	$I_b[A]$	$I_c[A]$	$I_a[A]$	$I_b[A]$	$I_c[A]$
$D1$	21.8	21.8	21.8	21.9	21.9	21.9
$D2$	10.8	10.8	10.8	10.9	10.9	10.9

Table 2.7: Normal operation in an islanded microgrid

	Microgrid with one DG			Microgrid with two DGs		
	$I_a[A]$	$I_b[A]$	$I_c[A]$	$I_a[A]$	$I_b[A]$	$I_c[A]$
$D1$	21.71	21.71	21.72	21.63	21.63	21.62
$D2$	10.79	10.79	10.79	10.76	10.76	10.74

operation currents when the microgrid is connected to the distribution network, for an islanded microgrid this difference is much smaller. Moreover as microgrid loads approach the inverters' ratings, such difference in currents become even smaller.

As a result, a conventional overcurrent-based fault protection scheme would be difficult to implement as there is not much difference between normal operation and fault operation in terms of current magnitude. Reference [41] carries out a review of the impact of reduced fault current environments like the one of an islanded inverter-supplied microgrid on overcurrent protection systems. The results from the simulations in PSCAD can be used to understand this impact and the difficulties in using traditional overcurrent-based fault protection.

First, reduced fault currents (see Tables 2.4 and 2.5) and small differences between fault currents and normal operation currents (see Table 2.7) in islanded microgrids result in longer fault clearing times and potential discrimination problems. Figure 2.9 shows two inverse time/current characteristics which are assumed to be corresponding to two overcurrent relays at locations D1 and D2. Times t1 and t2 in Figure 2.9 are the tripping times for faults at C1 and C2 respectively when the microgrid is operating in grid-connected mode. For simplicity these two curves are going to be referred as D1 and D2. Times t3 and t4 are the tripping times for faults at C1 and C2 in an islanded microgrid supplied by two inverters. From Figure 2.9 it can be seen that lower fault currents correspond to longer tripping times (t3 and t4) compared to the tripping times (t1 and t2) for grid-connected

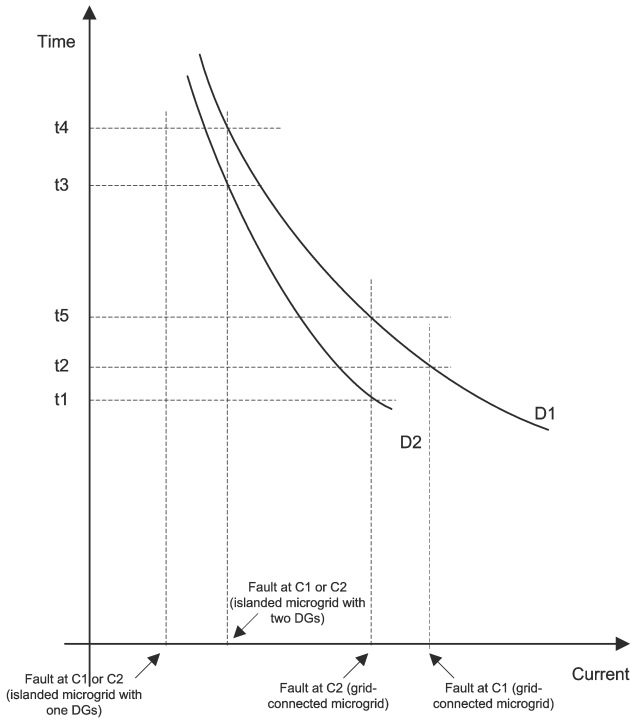


Figure 2.9: Impact of microgrids on inverse time/current characteristics coordination

microgrid operation. Moreover faults in the islanded microgrid supplied by one DG source may go undetected or correspond to tripping times much longer than t3 and t4.

Second, the restrictive fault current environment in an islanded microgrid can reduce the selectivity of the protection system. In grid-connected mode a fault at C1 and a fault at C2 produce different fault currents at locations D1 and D2 and therefore it is possible to design a selective protection system. So for example, a fault at C1 is detected and cleared only by the device at D1. While a fault at C2 corresponds to a tripping time t1 on the curve D2 which is lower than the corresponding time t5 on D1 (see Figure 2.9). As a result, there is enough discrimination margin between devices along the line and the device at D2 is the first to clear the fault. In contrast, in an islanded microgrid faults at different locations produce reduced fault currents with the same magnitude (see Tables 2.4 and 2.5 and Figure 2.9) thus creating problems to device coordination. So for example, a fault at C2 in an islanded microgrid supplied by one or two inverters can potentially operate both devices as the discrimination margin between the two curves D1 and D2 is reduced for smaller fault currents.

Finally the small difference between current magnitudes for faults at different lo-

cations in islanded microgrids can also compromise the use of instantaneous relays as described in [41].

2.4.2 Approaches to the design of a suitable protection system for islanded inverter-only microgrids

Reduced fault current environment in islanded inverter-only microgrids can be problematic when designing an overcurrent-based fault protection scheme. As a result, alternative approaches to the design of a suitable protection system are required. To date, little research has been published on this topic. Fault protection in a microgrid with reduced fault currents has been considered for the first time in [44]. The microgrid considered by the authors is an LV (0.4 kV) radial network, connected to the main distribution network through a 20/0.4 kV delta/wye grounded transformer. The microgrid contains a range of DG units including a flywheel. The approach used in [44] is to design a protection system capable of:

- disconnection of the microgrid in the event of a fault between the main power supply point and the transformer;
- correct operation for faults inside the microgrid during grid-connected and islanded operation.

As the available fault current in islanded mode is rather small, the authors propose to use a flywheel as a source of current in the event of a fault (3-5 p.u. depending on ratings). With sufficient fault current in both grid-connected and islanded mode, the proposed protection scheme is based on traditional overcurrent protection with the option of inter-tripping the DG units and the option of using differential protection to achieve a faster disconnection of the microgrid for external faults.

The presence of a flywheel definitely facilitates the design of a typical overcurrent protection scheme which the authors demonstrate in [44] to be working efficiently for various contingencies. However, the installation of a flywheel cannot be considered as a general solution to the problem of fault protection in islanded microgrids as it is effectively only a mean to increase the available fault current. Moreover the use of a flywheel opens up a series of additional problems. First, the provision of increased fault current comes with a cost as the flywheel is interfaced to the network via a 200kW inverter. Second, reference [45] show how important and difficult is the development of accurate system models for the

correct control and operation of the flywheel during microgrid faults. Finally, additional case studies should be carried out to reveal the interactions between the flywheel and the other DG sources present in the microgrid in the event of a fault. Indeed, the presence of DG sources is mentioned in the description in [44], but then they are not considered during fault current calculations. It would be of interest to determine if the overcurrent non-directional protection system proposed by the authors' works well when all DG sources infeeds are considered.

A second study on protection of islanded microgrids with reduced fault currents is presented in [40] by the CERTS consortium. The microgrid under study is supplied by inverter-only DG units and connected to the main supply through a fast acting SS. The protection philosophy is to have the same protection for both islanded and grid-connected modes. Therefore, in the event of a fault in grid-connected mode, the static switch opens to create an island. Then if the fault is within the microgrid, the protection is designed to detect and clear it. In particular, the authors claim that single phase-to-ground faults can be detected by using differential current and zero sequence current and phase-to-phase faults can be detected with the negative sequence component of the current. The settings for the negative and zero sequence currents are then calculated considering a degree of unbalanced operation (20%) in order to avoid any false tripping.

The main criticism to this proposed fault protection approach is that no further explanation on the reasons behind the choice of using differential, zero and negative sequence current is given. Moreover, the extension of this work to another microgrid results in being difficult as no explanation is given on the factors influencing the fault behaviour of inverter-interfaced DG sources or the fault behaviour of the microgrid as a whole. No information is given on the current limiting or control of the inverters during fault operation and even other published literature on the CERTS microgrid control does not help in understanding what happens to the microgrid in the event of a fault. As a result, even if the fault protection seems to work well in the CERTS microgrid, it is rather difficult if not impossible to apply it to any other microgrid.

Other references to protection for microgrids with inverter-interfaced DG sources can be found in [46] and in [41]. In [46] the authors consider a microgrid supplied by two inverter-interfaced DG units and propose the use of voltage drops as a way to discriminate between faults inside or outside the microgrid. The use of voltage as an alternative way

to detect the presence of a fault is definitely worth investigating for microgrid protection purposes [6]. However the authors of [46] consider only a grid-connected microgrid and do not explain if their voltage detection strategy would work in islanded inverter-only microgrids. Moreover their proposed fault detection strategy is supported by very few general simulations and very little system modelling.

After an analysis of the impact of reduced fault current on overcurrent protection, a review of some possible protection approaches which use voltage as an alternative way to detect the presence of a fault is presented in [41]. Different fast acting voltage detection techniques are compared and then it is proposed to use them to trigger an adaptive overcurrent-based protection scheme. This concept of voltage restrained overcurrent protection is not new [13], however it could well suit microgrids where low fault currents need new and more suitable time/current relay characteristics. Nevertheless no further work is carried out by the authors in order to demonstrate the applicability of their proposal.

2.5 Conclusion

The content of this Chapter has served four purposes: (i) to give an overview of the many issues regarding the operation of DG and microgrids with respect to the existing protection system; (ii) to describe some proposed solutions for protection systems in the presence of DG and microgrids; (iii) to highlight the need for more research into the study of inverter-only microgrid fault behaviour and (iv) into the development of a suitable fault detection strategy.

From the point of view of protection systems, the introduction of decentralized power generating units in a traditionally passive distribution network alters the fault current flows and magnitudes. The scale of this alteration mainly depends on the technology of the power generators, on their size and on their location. DG units can cause malfunctioning of the protection system and can require the upgrading of some protection devices.

Current approaches to the design of a suitable protection system to integrate DG include the use of FCL, adaptive protection and communication. However, at the moment, little is known about how to integrate different types of DG power sources, in particular inverters, in fault analysis studies. As a result, there is a strong need to understand the behaviour of inverters in the event of a fault and to be able to model them.

The problem of microgrid fault protection adds more dimensions to the general prob-

lem of protection in the presence of DG. Indeed, the protection system has to be designed to operate correctly for different microgrid operating modes (grid-connected and islanded modes). Additionally, the protection system is required to disconnect the microgrid quickly from the main electricity distribution network in the event of a fault.

Protection of islanded inverter-only microgrids has been considered in the final part of the Chapter. Section 2.4.1 has shown the differences in fault currents between grid-connected and islanded microgrids. Then it has demonstrated how difficult it is to design overcurrent protection in islanded inverter-only microgrids. As a result, alternative ways to detect the presence of a fault have to be investigated.

In Section 2.4.2, the review of the few proposed solutions to microgrid fault protection has highlighted the importance of basing any protection choice on the analysis and study of the behaviour of the system in the event of a fault.

Chapter 3

Microgrid network topology and control

The shape, size, generation mix and load mix of a microgrid can vary quite a lot as there is not a strict definition of what can be considered a microgrid. In this thesis a low voltage (240 V phase-to-neutral) islanded microgrid supplied only by inverter-interfaced DG units is considered. The first purpose of this Chapter is to describe the microgrid network topology. This includes an analysis of the different ways DG sources can be interfaced through inverters, a description of earthing arrangements which can be used in a microgrid and the description of the different network configurations which a microgrid can have depending on its connection point with the main distribution grid.

The second part of this Chapter is devoted to the description of the control of stand-alone and parallel-connected inverters. The study of inverter control is of particular importance as inverter-interfaced DG units are the only source of power in the microgrid under study.

An incremental approach is chosen to be used in the study of microgrid fault behaviour. Therefore, two islanded microgrid network models are considered: in the first one the power is supplied by one inverter-interfaced DG unit (stand-alone); in the second one two parallel-connected inverter-interfaced DG sources are considered. The two models are described at the end of this Chapter.

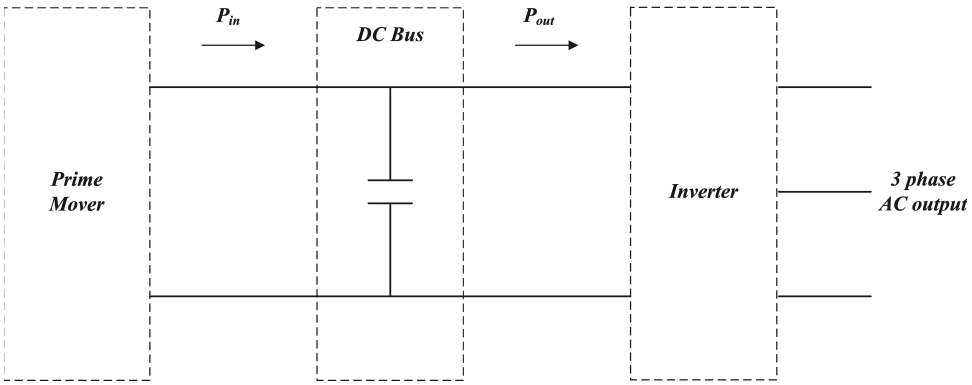


Figure 3.1: Block diagram of a typical inverter-interfaced DG unit

3.1 Microgrid network topology

3.1.1 Inverter-interfaced DG topologies

A typical DG unit with an inverter interface is shown in Figure 3.1. The primary mover (fuel cell, PV cell, etc.) produces DC power which is stored in the DC bus. The inverter is then responsible for the conversion of DC power in AC power which is then supplied to loads. For these types of applications voltage source inverters are often used [47].

In a synchronous machine-based power system, in the event of load or supply transients, the inertia of the generators is capable of supplying or absorbing the short-term power variation. In contrast, inverter-interfaced DG units have a very low energy storage and cannot cope with sudden high changes in power demand. This behaviour is explained by considering the DG unit in Figure 3.1. Each prime mover has a dynamic response to changes in power demand which depends on the prime mover technology. For example, a Capstone microturbine has a time constant around 10-20 seconds while a fuel cell may take few minutes to respond fully to a requested change in the amount of power produced [48]. As a result, the prime mover does not generally have an instantaneous power tracking capability and any change in load is first picked up by the inverter which uses the energy storing capability of the DC bus. The inverter can supply the extra required power, subject to its current limits, for a very limited time as the energy stored on the DC bus is quickly depleted. Therefore it is important to have a suitable sized energy storage located at the DC bus to ensure that the required energy is immediately available [7, 48]. If this condition is satisfied then the DC bus voltage is quite stiff and the prime mover together with the DC bus can be considered as a DC voltage source [48]. The resultant DG unit

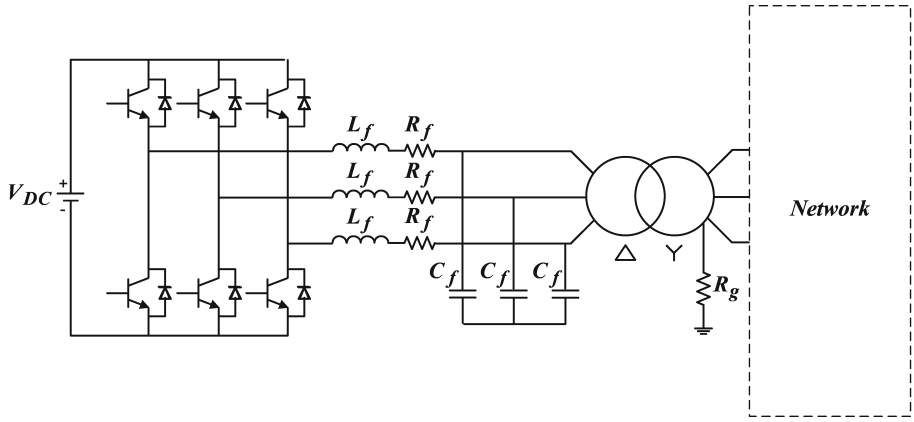


Figure 3.2: Three-phase, three-leg, three-wire voltage source inverter with a delta/wye grounded transformer

can then be approximated as a DC voltage source, V_{DC}, connected to the network through an inverter.

Low voltage end-of-users distribution networks, where microgrids are likely to be formed, are usually designed with four wires in order to be able to supply three-phase and single-phase loads. An inverter can provide a neutral connection to the three-phase four-wire system in three different ways [49]:

- through a connection via a delta/wye grounded transformer;
- using split DC link capacitors and connecting the mid-point of the DC link to the neutral point;
- using a four-leg topology and connecting the mid-point of the fourth leg through an inductor to the neutral output terminal.

Figures 3.2, 3.3 and 3.4 show the three different network connections for inverters together with the output LC filter (L_f, R_f, C_f) and the coupling impedance (L_{cc}, R_{cc}).

The approach of the split DC-link capacitors is not very convenient because it does not sufficiently utilize the available DC link voltage V_{DC} [50]. This is because with the split DC link configuration the maximum available peak value of the phase-to-neutral output voltage is equal to $\frac{V_{DC}}{2}$ (see Figure 3.3), while with the four leg configuration the maximum amplitude of the phase-to-neutral voltage with a four-leg inverter is equal to $\frac{V_{DC}}{\sqrt{3}}$ (see Figure 3.4). Moreover, the neutral current flowing through the split DC link capacitors of Figure 3.3 requires higher capacitance thus increasing costs [50].

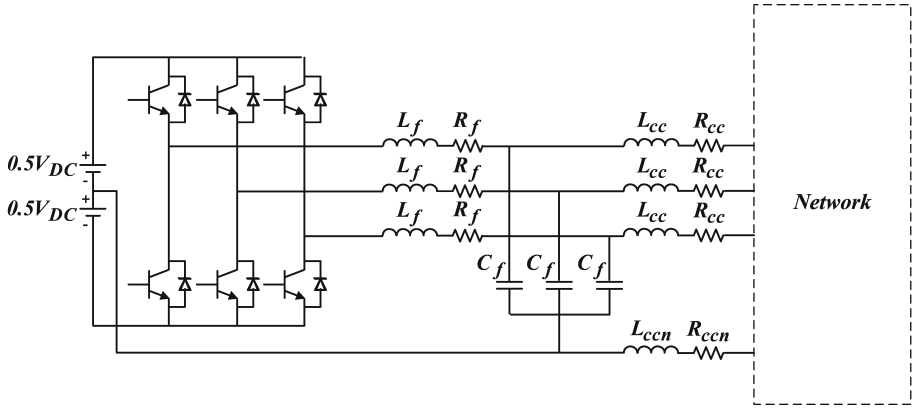


Figure 3.3: Three-phase, three-leg, four-wire voltage source inverter with split DC link capacitors

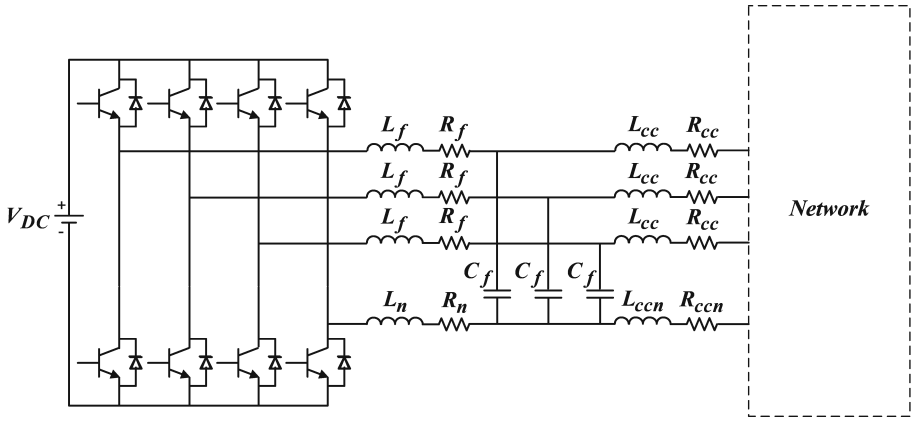


Figure 3.4: Three-phase, four-leg, four-wire voltage source inverter

As a result of these drawbacks, the most common way of interfacing the DG source to the network is via a three-leg inverter with a transformer or a four-leg inverter. The connection via a transformer is often required by the distribution network operator as the transformer acts as an isolating device. In particular the transformer can prevent the injection of DC current and some winding arrangements, such as the delta/wye grounded (see Figure 3.2), prevent any fault current contribution from the DG source to earth faults. However, the use of an isolation transformer is not required by the general standards on DG interconnection [22,23]. The IEEE standard on PV systems in the Annex F [15] specifically states that the use of a *"dedicated distribution transformer"* for the interconnection to the main distribution network is not required. Similarly in [3] it is clearly identified that the application of *"transformless"* inverters should be further pursued. From the point of view of microgrids, both the three-leg inverter with transformer and the four-leg inverter are used as possible interfaces [6]. However, depending on the level of load unbalance present in the microgrid, the four-leg topology is preferred to the transformer configuration as it provides control over the neutral current [51].

A basic microgrid would be formed by local loads supplied by a single inverter-interfaced DG unit controlled in stand-alone mode. Control techniques for stand-alone inverters will be described in Section 3.2.1. As the load size of the microgrid increases, the supply of power from a single inverter presents some problems. First, the power ratings of inverters are limited by factors like performance, efficiency and cost [52]. Second, the use of one single power unit reduces the reliability of the system because if the unit fails the whole system will be affected. For these reasons, a modular approach using inverters connected in (near) parallel is preferred. The modular approach resolves the limitations of high rating stand-alone inverters and gives to the microgrid flexibility in terms of supply of future demand and use of different available renewable sources. Figure 3.5 shows a possible microgrid topology with two parallel inverters, connected through an impedance $R_l + j\omega L_l$ supplying a local network. Control techniques for parallel-connected inverters, together with their advantages and disadvantages, are going to be described in Section 3.2.2.

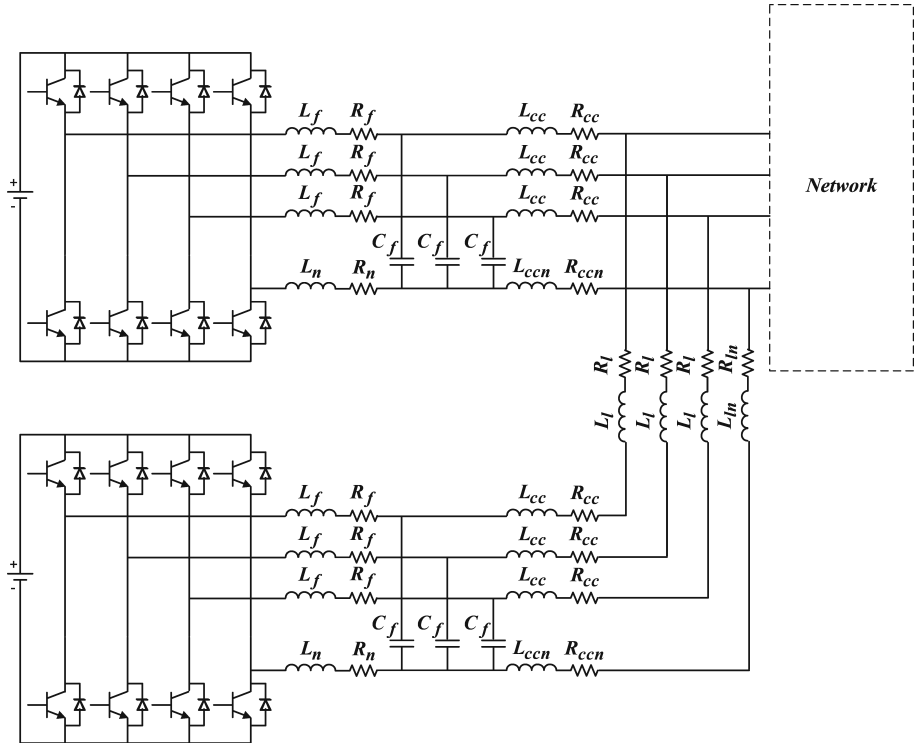


Figure 3.5: Parallel operation of two inverters

3.1.2 Microgrid earthing

For the purpose of analyzing the fault response of an islanded inverter-only microgrid, it is very important to consider the earthing arrangements. As with any electrical systems, the correct earthing procedures are essential for the safety and correct operation of the microgrid. In particular, in a microgrid, the earthing has to deal with both grid-connected and islanded mode. Indeed, as soon as an islanded microgrid is formed, a new earthing system is formed as well which has to satisfy the same requirements as the grid-connected mode.

Various standards such as IEEE 142 [53] and IEEE 446 [54] consider the issue of earthing of emergency and stand-by generation and can be used to understand the problem of earthing of a microgrid. These standards use the US National Electrical Code (NEC) concept of a "separately derived source"which is a source which does not have any direct electrical connection, including a neutral conductor, with any other electrical system. The NEC requirement is that separately derived sources should be locally connected to earth. So, in other words, if the neutral conductor is supplied by the substation transformer sec-

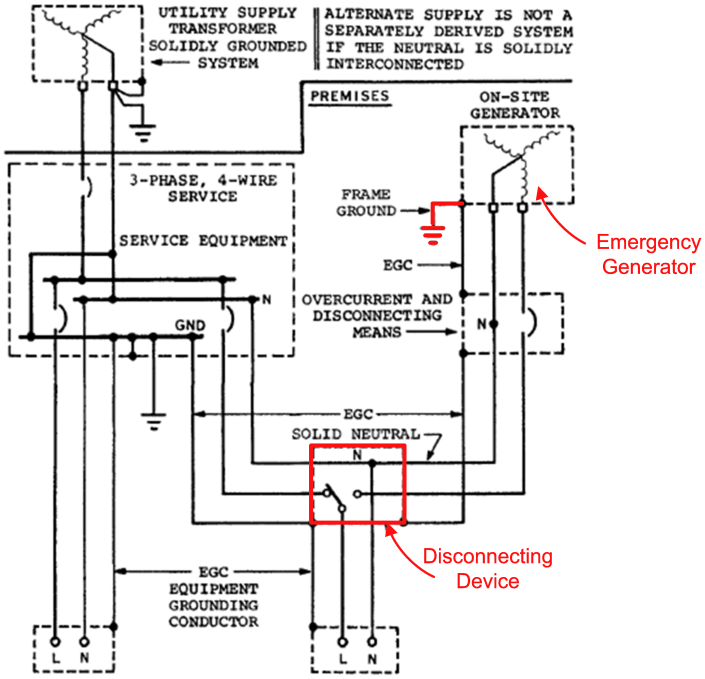


Figure 3.6: Solidly interconnected neutral conductor grounded at the substation only [54]

ondary to the emergency generator, then this neutral conductor should not be connected to earth locally. Figure 3.6 shows a system in which the neutral is not affected by the disconnecting device and is therefore not grounded locally. On the other hand, if the emergency system is electrically separated from the main grid, then the neutral conductor has to be locally earthed because the main earth source at the substation has been disconnected, see Figure 3.7.

These two examples can be readily applied to the microgrid problem. Here, if the island is formed by opening a breaker placed at the primary side of the substation transformer or by opening a breaker at the secondary side which does not disconnect the neutral conductor, then earth source is still present and therefore no extra local earth connection of the DG neutral has to be performed. On the other hand, if the substation transformer is completely disconnected from the microgrid, then the remaining part of the earthing system may not be sufficient and additional earthing may be required.

Now moving to the specific case of a microgrid, it is important to analyze the different earthing arrangements in LV networks. The work undertaken in [55] provides a good reference source in order to understand the issues involved in the choice and in the design

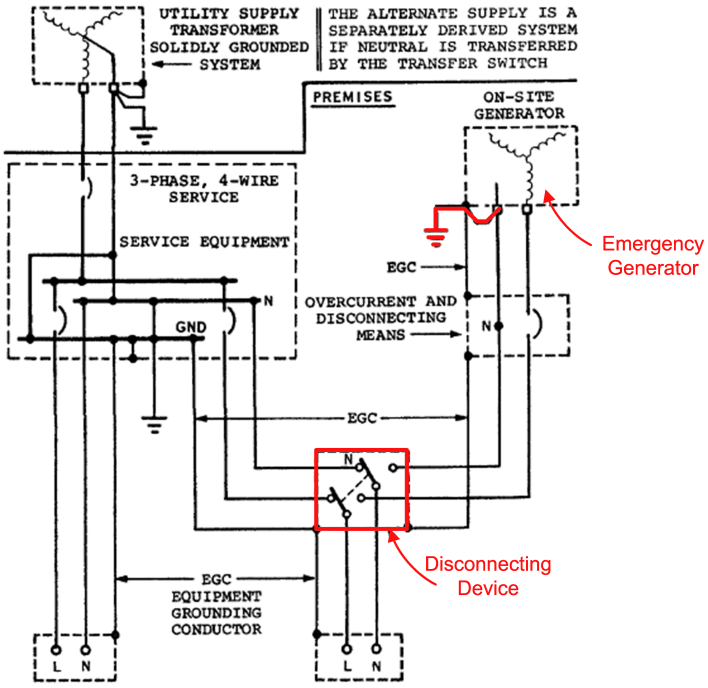


Figure 3.7: Neutral conductor grounded at the substation and at the source of alternate power supply (separately derived source) [54]

of a safe earthing system in a microgrid and its impact on fault currents. Two different earthing arrangements have been proposed [55]:

- TT
- TN-C-S (Protective multiple earthing)

In the TT earthing arrangement the neutral conductor is connected to earth at one point (usually at the substation) and the protective earth (PE) conductor is locally connected to earth. On the other hand, in the TN-C-S arrangement the neutral and the PE conductors are combined together and frequently connected to earth throughout the distribution network. At the customer's supply point in the TN-C-S system, the network operator provides the two conductors separately. The major difference between the two earthing arrangements is apparent in the different fault current magnitudes for an insulation fault. In a TT system, the fault current is small because of the high impedance in the fault loop whereas in a TN-C-S system the fault current flows back through the reduced impedance of the neutral conductor and therefore it is high in magnitude. Based on the fact that the TN-C-S is commonly used in the U.K. and in the study presented in [55], the TN-C-S

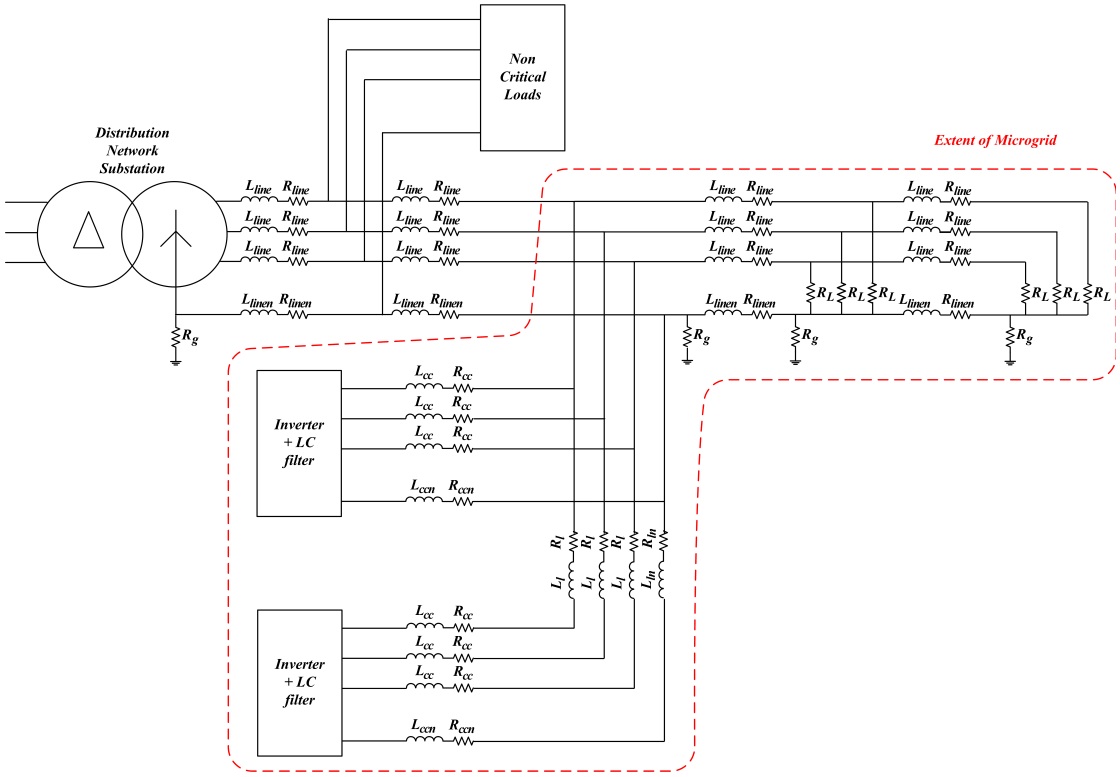


Figure 3.8: LV distribution network with microgrid

system is chosen as the earthing arrangement in the LV network where the microgrid is formed.

3.1.3 Microgrid network configuration

This Section describes the possible network configurations a microgrid can have depending on its connection to the main distribution grid. From the simple microgrid diagram shown in Figure 2.1, a more detailed network diagram of the microgrid and the surrounding distribution network is shown in Figure 3.8. The two diagrams in Figures 2.1 and 3.8 are equivalent apart from the SS which has been temporarily omitted in the detailed network diagram.

In Figure 3.8, the power is supplied by a substation delta/wye grounded transformer to two feeders: in one feeder there is the microgrid, while in the other there are loads which are considered as "non critical". The distribution network is radial with a four-wire configuration. Following the discussion in Section 3.1.2, the distribution network under study has a TN-C-S system with the neutral conductor connected to earth at the

substation and at other points along the lines through resistances (R_g). Each line section has an impedance given by R_{line} and L_{line} and the microgrid is assumed to have two resistive loads R_L. The two DG units in Figure 2.1 are more explicitly represented in Figure 3.8 as two inverters with LC output filters, connected to the distribution feeder through coupling impedances (R_{cc} and L_{cc}). Overall the microgrid includes two DG units and two resistive loads connected along a radial feeder. The red line in Figure 3.8 shows the extent of this microgrid.

So far, the specific connection point of the microgrid to the distribution network and the SS have not been mentioned. Nevertheless they can deeply affect the shape and the extent of a microgrid. In the work presented in [55], the authors suggest that a disconnecting switch should be placed before the primary side of the substation transformer as shown in Figure 3.9. This arrangement facilitates the earthing of islanded microgrids. Indeed, the microgrid earthing arrangements are left intact as the secondary of the transformer with its grounded star is still electrically part of the islanded microgrid. Reference [55] shows how to design a grounding system compatible for grid-connected and islanded operation by following conventional techniques. Although this approach offers a simple solution which can be directly applied by network design engineers, there are some arguments against it. The first regards the fact that the secondary of the transformer is still energised even if the primary is disconnected from the main grid. As a result, core losses are created. The second argument regards the shape of the microgrid itself. With this arrangement, the microgrid shown in red in Figure 3.9 has to have a transformer at the point of connection with the main distribution grid. The non essential loads in Figure 3.9 have to be considered part of the microgrid as well and some form of load-shedding has to be implemented. The connection of a microgrid through a transformer can be expensive and restrictive to the possible extent of a microgrid.

Another solution is to place the SS after the secondary side of the transformer as it is done in the CERTS microgrid [6]. Figures 3.10 and 3.11 show a possible location just after the transformer and a location which includes only the critical loads. The SS opens only the three phase conductors thus keeping unchanged the earthing system of the microgrid. The part of the networks in red in Figures 3.10 and 3.11 are the resulting microgrids. Once again, the problem with these configurations is that a transformer is needed to interconnect the microgrid. Moreover, if the configuration in Figure 3.11 is used,

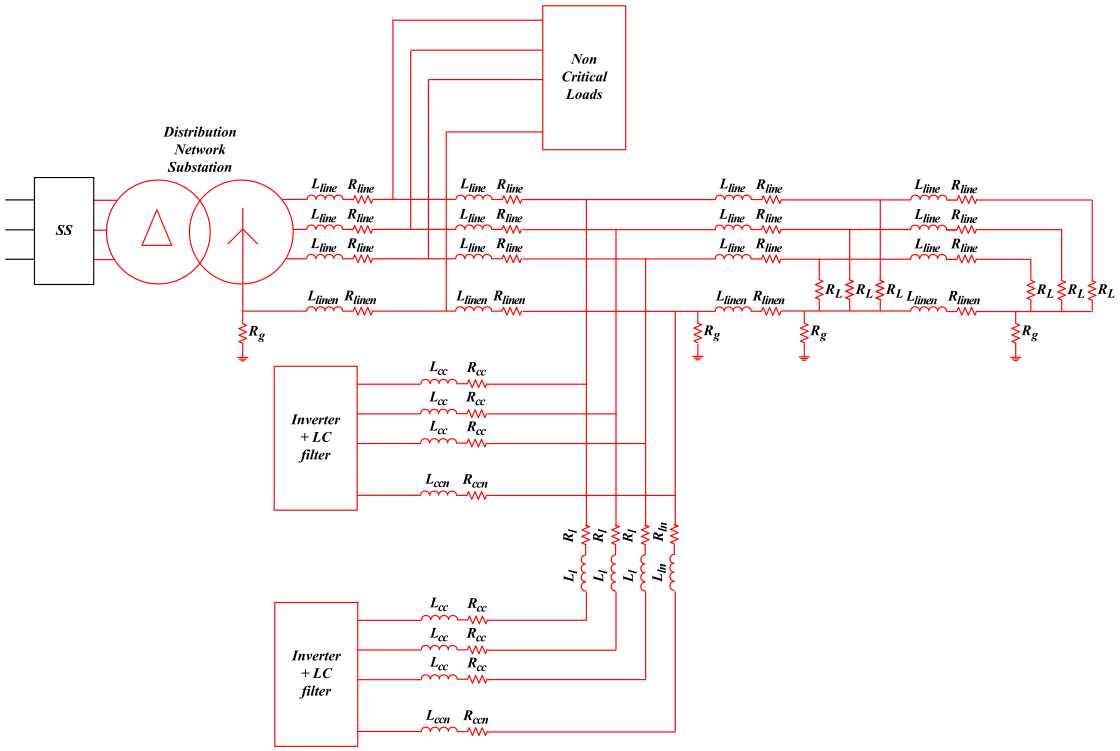


Figure 3.9: Microgrid (shown in red) with SS on the primary transformer side

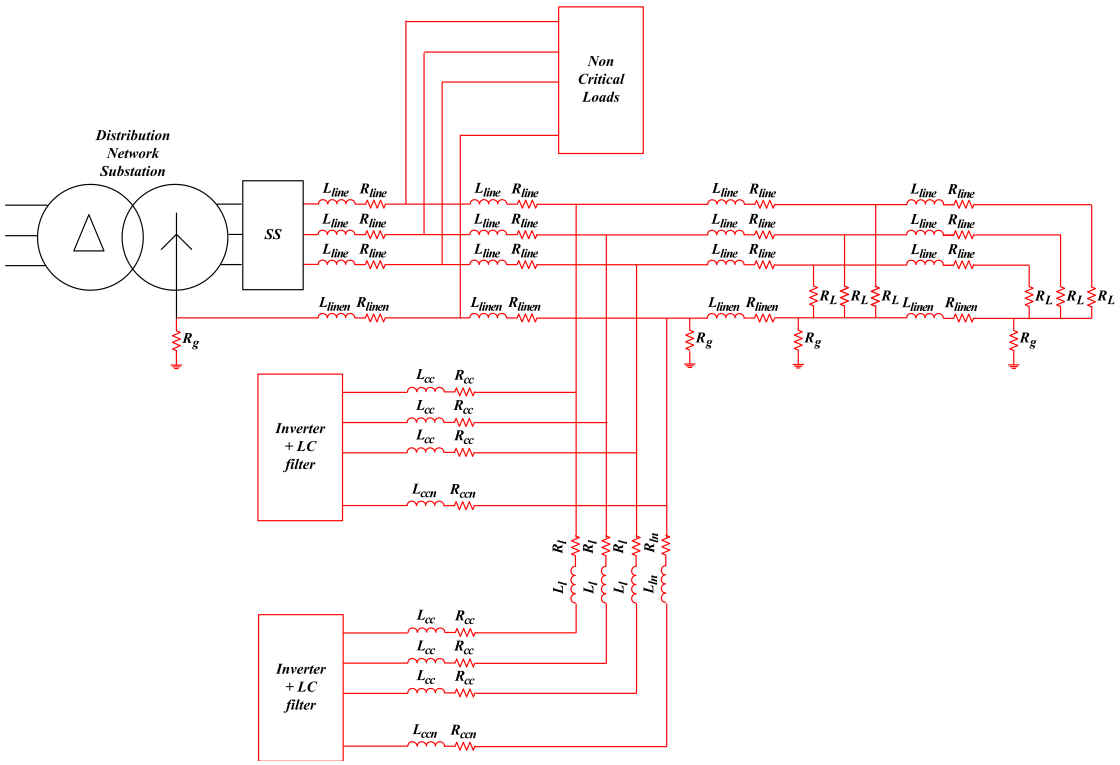


Figure 3.10: Microgrid (shown in red) with 3-pole SS on the secondary transformer side

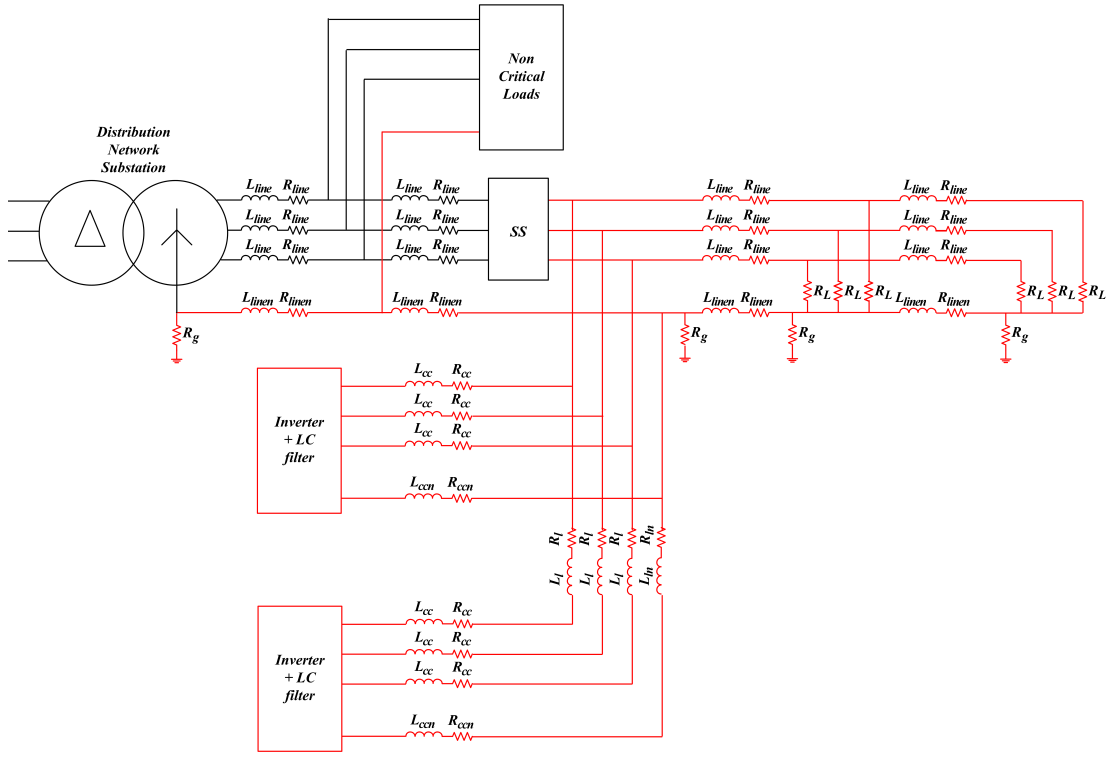


Figure 3.11: Microgrid (shown in red) with 3-pole SS on the secondary transformer side after the "non critical"loads

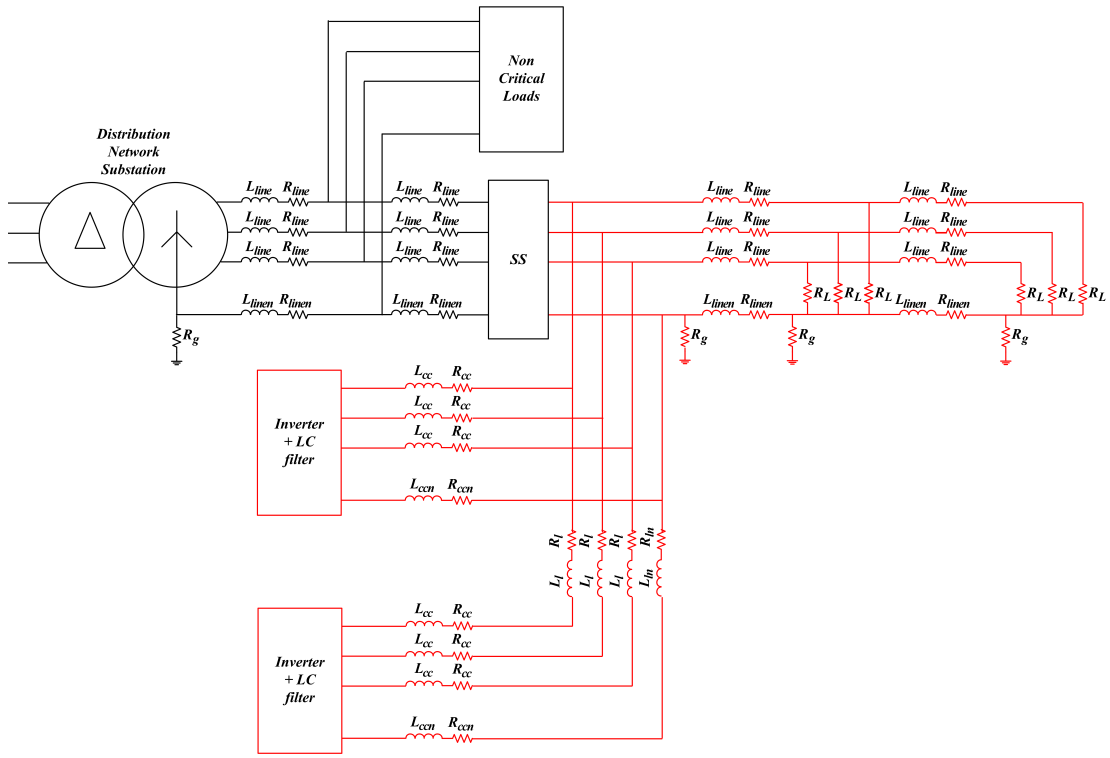


Figure 3.12: Microgrid (shown in red) with 4-pole SS

the ground fault current path can involve parts of the network which are not part of the microgrid.

A further solution to the microgrid connection consists of having a four-pole SS which completely disconnects the microgrid from the network, see Figure 3.12. This is equivalent to having a separately derived source which is a popular solution with UPS systems. However, the obvious inconvenience is that there is a need to check the suitability of the earth of the remaining system and possibly a need to re-design it. This is not a straight forward task especially for microgrids supplied by inverter-interfaced DG units whose fault behaviour and equivalent zero sequence impedances are not well known. Moreover, the earthing is required to be suitable for grid-connected as well as islanded operation. A possible solution suggested in [8] requires a high speed insertion of a grounding connection as soon as the microgrid is disconnected from the utility. However this solution is likely to require some form of communication between the SS and the additional grounding device.

In conclusion, there is no clear standard or accepted practice on how a microgrid should be formed and interconnected to the distribution network [6]. Therefore each specific case has to be considered and analyzed on its own with regards to the practices of the distribution network operator and relevant standards.

In this research work, the two microgrid models under study (see Section 3.3 for a detailed description) are formed by opening a 4-pole switch as shown in Figure 3.12. This choice is suitable for the incremental approach used in this thesis which starts from the study of a very basic microgrid system with one inverter only and then can be extended to more complex systems. Finally, as the focus is on the analysis and modelling of inverter-only microgrids and on the design of a suitable fault detection strategy, the design of the microgrid earthing system is not included and it is assumed that an adequate one exists.

3.2 Inverter control and operation

Being the only power sources in the microgrid under study, inverters play a fundamental role in shaping the fault behaviour. One of the main differences between conventional synchronous machines and inverters lies in the flexibility of the operation of inverters which can be controlled in different ways to achieve various objectives. As a consequence, if the fault behaviour of synchronous machines is well defined, the fault behaviour of inverters is not and varies with the choice of control.

The following Sections describe some of the most popular strategies adopted in the control of inverters. Understanding them is of primary importance as in Chapter 4 it will be illustrated how these control strategies can produce different responses in the event of a fault.

As the microgrid under study supplies LV customers, the presence of unbalanced loads is likely. Therefore the operation of inverters with unbalanced loading is going to be described as well. This particular issue turns out to be important for the purpose of analyzing the response of inverters in the event of unbalanced faults and then for designing suitable fault detection methods.

3.2.1 Control of a stand-alone inverter

A stand-alone Voltage Source Inverter (VSI) is the basic building block of a microgrid. Its primary role is to maintain a regulated voltage and frequency supply to loads under all loading conditions and transients. In achieving this, the role of the internal control system of the inverter is critical.

Even before the introduction of the concepts of DG and microgrid, inverters had been a key component in Uninterruptible Power Supply (UPS) systems. As UPS systems operate as stand-alone units, the theory and experience in the control of their inverters can be directly applied to the control and operation of inverters for DG units in islanded power systems like microgrids.

A first type of inverter control was based on a simple voltage regulation loop using Sinusoidal Pulse Width Modulation (SPWM) [49]. This approach was able to produce a good steady-state output voltage, however its performance with load changes and loads drawing harmonically distorted currents was poor. Since this first approach, many different solutions have been proposed over the years to improve the inverter control [49]. In particular, the use of a multi-loop control structure with an outer voltage loop and an inner current loop has become a popular choice [56, 57] and now it is also frequently adopted in stand-alone inverters for DG applications [58, 59]. From the basic multi-loop structure, different combinations of control variables and feedforward decoupling schemes can be used to improve the dynamic performance and the stability of the inverter [56, 57].

Figure 3.13 shows a simple single-phase diagram of the control of an inverter sup-

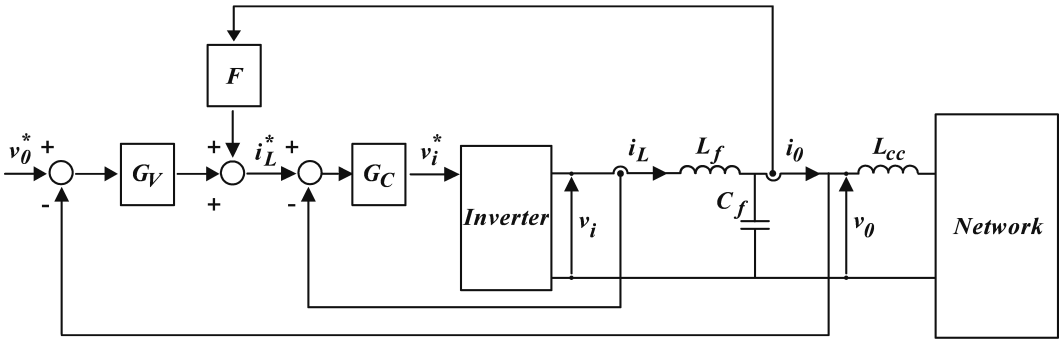


Figure 3.13: Multi-loop control of a stand-alone inverter

plying a microgrid network such as that adopted in this research work. It is possible to see the outer voltage control loop which regulates the output capacitor voltage v_0 and sets the reference for the inner control loop for inductor current, i_L. The reference value for the output filter voltage, v_0^* is usually kept constant (in magnitude and frequency) for a single inverter system but may vary according to droop settings [60] if the inverter is operated in parallel with other inverters. Figure 3.13 also shows the inverter bridge voltage v_i and the feedforward transfer function F for the output current, i_0 which reduces the disturbance introduced by load changes. Blocks $G_V(s)$ and $G_C(s)$ are the voltage and current regulators.

The multi-loop control of a stand-alone inverter can be implemented in various reference frames. One of the most popular solutions adopted in the literature [61], is the control in the Synchronous Reference Frame ($dq\gamma$ coordinates). These new coordinates result from the Clarke and Park transformation of the original phase variables (see Appendix A for a more detailed description). If only the Clarke transformation is applied [58], then the control is implemented in the Stationary Reference Frame ($\alpha\beta\gamma$ coordinates). If no transformation is involved, the control is simply implemented in the Natural Reference Frame (abc coordinates) as in [62]. In Chapter 4 it will be shown how inverters with identical control structures (such as that in Figure 3.13) but different reference frames behave in the event of a fault.

It is common practice to summarise the control performance by expressing the relation between the output voltage v_0 and the reference v_0^* and the load current i_0. Taking the model in Figure 3.13 and replacing the current control loop with its closed-loop transfer

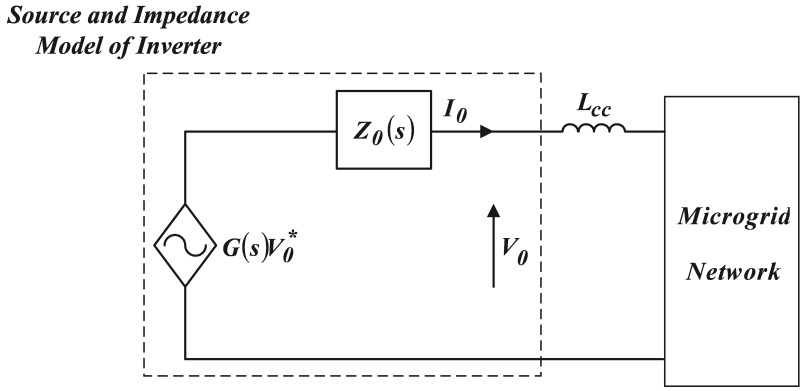


Figure 3.14: Equivalent two-terminal circuit of a stand-alone inverter with multi-loop control

function $G_{CC}(s)$, the relationship can be expressed as [59]

$$V_0(s) = G(s)V_0^* - Z_0(s)I_0(s) \tag{3.1}$$

where

$$G(s) = \frac{G_V(s)G_{CC}(s)}{sC_f + G_V(s)G_{CC}(s)} \tag{3.2}$$

is the inverter voltage gain and

$$Z_0(s) = -\frac{FG_{CC}(s) - 1}{sC_f + G_V(s)G_{CC}(s)} \tag{3.3}$$

is the output impedance. The inverter is therefore modelled as an equivalent two-terminal circuit as shown in Fig. 3.14.

As the parameters of the inverter equivalent model depend on the control gains and on the LC filter, the control of the inverter can be designed in order to achieve some specific goals. Ideally, first, the output voltage should follow the reference around the frequency range of interest (which in this case is the system fundamental frequency) with unity gain and no phase offset. From (3.2) it can be see that if $G_{CC}(s) \approx 1$ and if $G_V(s) > sC_f$ in the range around the system fundamental frequency, then $G(s) \approx 1$. Second, the output voltage should also be immune to any load current influence. Indeed, the load current is considered as a disturbance and low output impedance Z_0 across a specific frequency range is required to reject disturbances at those frequencies. From equation (3.3) it can be seen that if $G_{CC}(s) \approx 1$ and if $F \approx 1$, around the frequency range of interest, then $Z_0(s) \approx 0$. However, normally $F < 1$ in order to prevent accidentally creating $F > 1$ which over-compensates the disturbance and can be destabilising. As an example, Figure 3.15

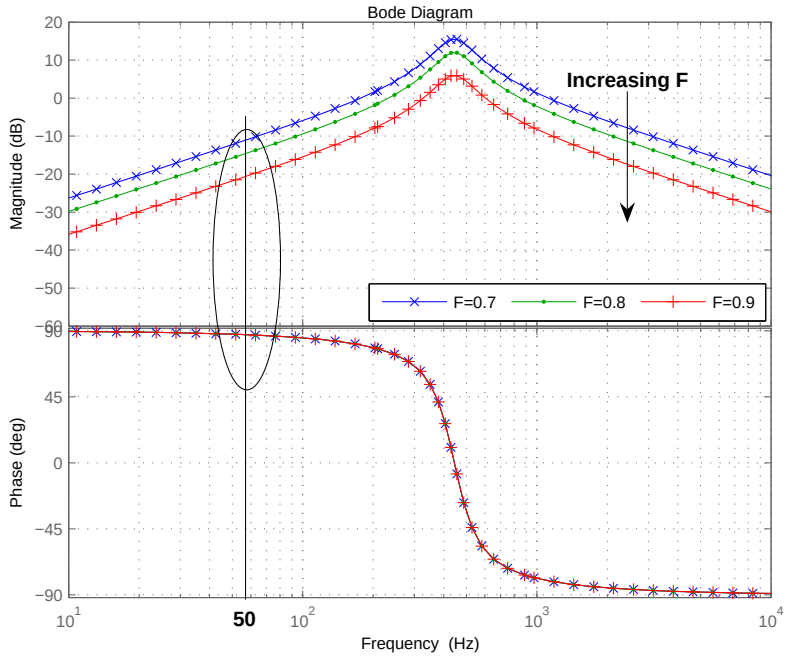


Figure 3.15: Output impedance Bode diagram

shows the Bode plot of the output impedance $Z_0(s)$ for different values of F, assuming $G_{CC}(s) \approx 1$, C_f equal to 50 μ F and using a PI controller ($G_V(s) = 0.05 + 390/s$) in the voltage loop. As predicted, an increase in F reduces Z_0. Moreover it can also be seen that around the system frequency (50Hz) the output impedance has an inductive nature.

The representation of the inverter as a two-terminal circuit whose parameters depend on the control and on the output LC filter will be extensively used in Chapter 5 as a way to model the behaviour of the inverter in the event of a fault.

3.2.2 Control of parallel-connected inverters

The main goal of the control of parallel-connected inverters is to supply power at a regulated voltage and frequency while maintaining good power sharing among the inverters. In the case of a stand-alone inverter, the voltage and frequency references are fixed and there is no possibility for the inverter to be overloaded under normal operation as its power rating has been chosen to suit the microgrid load demand. In contrast, in a microgrid with several inverters, the power (active and reactive) has to be shared among inverters according to their ratings to avoid over-loading individual inverters.

Many different strategies to control parallel inverters have been proposed in the literature. They can be broadly divided between the approaches which use communication links and those which do not [52]. One control technique which uses communications is the master-slave configuration where one inverter operates in voltage control mode (the master) and the others (the slaves) operate in current control mode [52]. The master controls the output voltage and generates a current command for the slave units transmitted via a communication link and good load sharing can be achieved. However, reliance on communication is considered to compromise the reliability of the system because a failure of the communication link can bring the whole system down.

One method which does not use any communication, which is based on local measurements and which has gained considerable attention in DG applications is the droop control method [60,63]. The droop control technique is derived from the operation of conventional synchronous machine-based power systems where the flows of active and reactive power are regulated through the system frequency and voltage respectively. Inverters do not present this natural coupling neither between the frequency and the active power nor between the output voltage and the reactive power. Nevertheless, these two couplings can be artificially introduced through the use of a droop-based control technique as proposed in [60, 63]. According to this control technique, the inverter reference frequency is decreased if there is any increase in the load real power and vice versa. Similarly, the sharing of reactive power is regulated by an increase or a decrease in the inverter reference voltage. Figure 3.16 shows a power controller scheme based on droop control. Here the active (p) and the reactive (q) powers supplied by the inverter are calculated and averaged. The resulting signals P and Q are used to calculate the inverter reference frequency ω^* and output reference voltage v_0^* according to two droop characteristics (see the two characteristics P/ω and Q/v in Figure 3.16). The power controller scheme in Figure 3.16 is then added as an external additional loop to the two-loop control structure in Figure 3.13.

The calculation of the instantaneous active and reactive power components p and q can be performed in the Synchronous Reference Frame (SynRF) from the measured value of the output voltage v_0 and the load current i_0 as follows [63]:

$$p = v_{0_d} i_{0_d} + v_{0_q} i_{0_q} \tag{3.4}$$

$$q = v_{0_q} i_{0_d} - v_{0_d} i_{0_q} \tag{3.5}$$

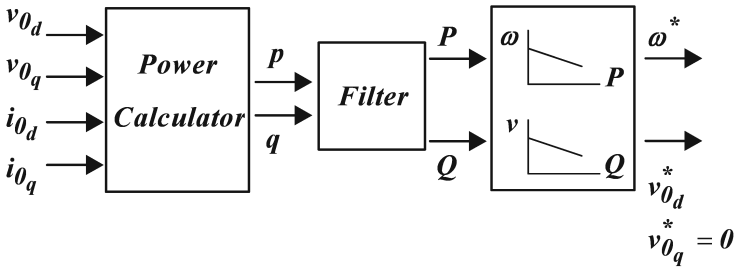


Figure 3.16: Power droop controller

As shown in Figure 3.16, the average values P and Q are obtained by passing the instantaneous powers p and q through a low-pass filter. Therefore, P and Q are determined as:

$$P = \frac{\omega_c}{s + \omega_c} p, \quad Q = \frac{\omega_c}{s + \omega_c} q. \tag{3.6}$$

The inverter output frequency ω^* and output reference voltage v_0^* are then controlled by the droops characteristics which are defined by equations (3.7) and (3.8):

$$\omega^* = \omega_n - m_p P \tag{3.7}$$

$$v^*_{0_d} = V_n - n_q Q, \quad v^*_{0_q} = 0 \tag{3.8}$$

where ω_n and V_n are the nominal frequency and the nominal output voltage respectively. The droop gains m_p and n_q are calculated as:

$$m_p = \frac{\Delta\omega}{P_{max}} \tag{3.9}$$

$$n_q = \frac{\Delta V}{Q_{max}} \tag{3.10}$$

where $\Delta\omega$ and ΔV are the maximum frequency and voltage deviations allowed and P_{max} and Q_{max} are the maximum active and reactive powers which can be delivered by the inverter. In order to have good load sharing, the frequency and voltage droop gains can be selected as follows [64]:

$$m_{p_1} S_1 = m_{p_2} S_2 = ... = m_{p_n} S_n \tag{3.11}$$

$$n_{q_1} S_1 = n_{q_2} S_2 = ... = n_{q_n} S_n \tag{3.12}$$

where m_{p_i}, n_{q_i} and S_i are the frequency gain, the voltage gain and the apparent power rating of the ith inverter respectively. More sophisticated techniques to select droop gains

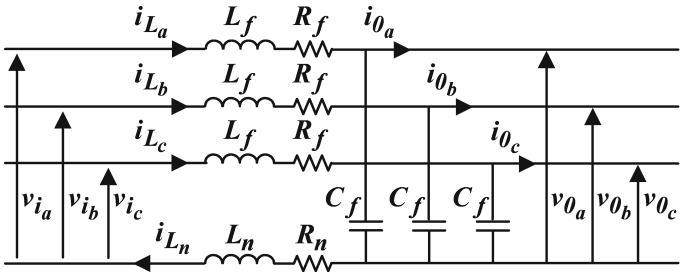


Figure 3.17: Three-phase four-wire LC output filter

than the one based on equations (3.11) and (3.12) have been proposed in the literature [11,65,66]. For example, in [11] the droop gains are chosen according to economic benefits and updated in real time through a (relatively slow) communication link. Taking a different approach, as droop gains have an impact on the stable operation of the system, in [65] they are chosen to ensure system stability. Economic benefit and system stability are both used as design criteria in [66] where droop gains are selected and optimised in real time.

3.2.3 Unbalanced operation of an inverter

Inverters are usually designed and controlled under the assumption that they supply a balanced load. However unbalanced load operation in a microgrid is likely to happen. Indeed, unbalanced operation in a microgrid can be caused by unevenly distributed single-phase loads (a very common event in LV distribution networks) and by unbalanced faults. As this research work is focused on understanding the general fault behaviour of inverter-only microgrids, the following Sections summarize the most important aspects of the impact of unbalanced loading on the operation, design and control of inverters.

Load unbalance and inverter operation

An unbalanced load in a microgrid draws a set of unbalanced load currents while the inverter is still required to provide a set of balanced output voltages v_{0_a}, v_{0_b} and v_{0_c}. The impact of load unbalance on an inverter's operation can be analyzed by considering the inverter LC output filter, see Figure 3.17. For an unbalanced load, the output load currents i_{0_a}, i_{0_b} and i_{0_c} can be expressed in terms of sequence components (see Appendix A for a more detailed description of sequence components) as:

$$\begin{bmatrix} i_{0_a} \\ i_{0_b} \\ i_{0_c} \end{bmatrix} = \begin{bmatrix} i_{0_{a_p}} + i_{0_{a_n}} + i_{0_{a_0}} \\ i_{0_{b_p}} + i_{0_{b_n}} + i_{0_{b_0}} \\ i_{0_{c_p}} + i_{0_{c_n}} + i_{0_{c_0}} \end{bmatrix} \tag{3.13}$$

Because the inverter output voltage is controlled in order to be balanced, it can be expressed in terms of the positive sequence component only as:

$$\begin{bmatrix} v_{0_a} \\ v_{0_b} \\ v_{0_c} \end{bmatrix} = \begin{bmatrix} v_{0_{ap}} \\ v_{0_{bp}} \\ v_{0_{cp}} \end{bmatrix} \tag{3.14}$$

Now, it can be demonstrated that during unbalanced loading the inverter bridge voltages v_{i_a}, v_{i_b} and v_{i_c} that must be provided are unbalanced and with magnitudes which depend on the load currents i_{0_a}, i_{0_b} and i_{0_c}. From Figure 3.17 the following equations can be written:

$$\begin{bmatrix} v_{i_a} \\ v_{i_b} \\ v_{i_c} \end{bmatrix} = \begin{bmatrix} L_f(\frac{di_{0_a}}{dt} + C\frac{d^2v_{0_a}}{dt^2}) + v_{0_a} + L_n\frac{di_{L_n}}{dt} \\ L_f(\frac{di_{0_b}}{dt} + C\frac{d^2v_{0_b}}{dt^2}) + v_{0_b} + L_n\frac{di_{L_n}}{dt} \\ L_f(\frac{di_{0_c}}{dt} + C\frac{d^2v_{0_c}}{dt^2}) + v_{0_c} + L_n\frac{di_{L_n}}{dt} \end{bmatrix} \tag{3.15}$$

where the neutral current i_n is given by:

$$i_{L_n} = i_{0_a} + i_{0_b} + i_{0_c} + C\frac{dv_{0_a}}{dt} + C\frac{dv_{0_b}}{dt} + C\frac{dv_{0_c}}{dt} \tag{3.16}$$

By substituting (3.13) and (3.14) into (3.15), the inverter bridge voltage v_i can be expressed as a function of sequence components as follows:

$$\begin{bmatrix} v_{i_{ap}} \\ v_{i_{bp}} \\ v_{i_{cp}} \end{bmatrix} = \begin{bmatrix} L_f(\frac{di_{0_{ap}}}{dt} + C\frac{d^2v_{0_a}}{dt^2}) + v_{0_a} \\ L_f(\frac{di_{0_{bp}}}{dt} + C\frac{d^2v_{0_b}}{dt^2}) + v_{0_b} \\ L_f(\frac{di_{0_{cp}}}{dt} + C\frac{d^2v_{0_c}}{dt^2}) + v_{0_c} \end{bmatrix} \tag{3.17}$$

$$\begin{bmatrix} v_{i_{an}} \\ v_{i_{bn}} \\ v_{i_{cn}} \end{bmatrix} = \begin{bmatrix} L_f\frac{di_{0_{an}}}{dt} \\ L_f\frac{di_{0_{bn}}}{dt} \\ L_f\frac{di_{0_{cn}}}{dt} \end{bmatrix} \tag{3.18}$$

$$\begin{bmatrix} v_{i_{a_0}} \\ v_{i_{b_0}} \\ v_{i_{c_0}} \end{bmatrix} = \begin{bmatrix} (L_f + 3L_n)\frac{di_{0_{a_0}}}{dt} \\ (L_f + 3L_n)\frac{di_{0_{b_0}}}{dt} \\ (L_f + 3L_n)\frac{di_{0_{c_0}}}{dt} \end{bmatrix} \tag{3.19}$$

From equations (3.18) and (3.19) it can be observed that the unbalanced load requires inverter bridge voltages with negative and zero sequence components in addition to the positive sequence term in equation (3.17). Moreover, it also possible to observe that the neutral current i_{L_n}, supplied by the inverter is equal to three time the zero sequence component i_{0_0} of the load current.

Load unbalance and inverter design and control

During unbalanced operation, the inverter is required to produce a set of unbalanced voltages v_{i_a}, v_{i_b} and v_{i_c} and to carry a neutral current as well. Now the implications for the design and control of the inverter are analyzed.

From Figure 3.13 it can be seen that the output of the current control loop, which is the reference inverter bridge voltage v_i^*, is fed into the block called "Inverter". One of the components inside this block is a modulator which is responsible of generating, from the reference voltage v_i^*, the switching sequences for the inverter which then synthesizes v_i. Space Vector Modulation (SVM) [47] is commonly used as a modulation technique for four-leg inverters [50] and therefore it is assumed to be implemented in the modulator. From the theory of SVM, for a given DC-link voltage, the trajectory of the maximum amplitude of the synthesized balanced bridge voltage, v_i, is a circle with radius $\frac{1}{\sqrt{2}}V_{DC}$. The magnitude of the inverter bridge voltage is limited by the DC-link voltage and therefore not all voltages can be reproduced by the inverter.

Now, back to inverter unbalanced operation, expanding equations (3.17), (3.18) and (3.19) with their sinusoidal variation and combining yields:

$$\begin{aligned} v_{i_a}(t) &= V_{i_p}\cos(\omega t+\theta_{i_p}) + V_{i_n}\cos(\omega t+\theta_{i_n}) + V_{i_0}\cos(\omega t+\theta_{i_0}) \\ v_{i_b}(t) &= V_{i_p}\cos(\omega t+\theta_{i_p}-\frac{2}{3}\pi) + V_{i_n}\cos(\omega t+\theta_{i_n}+\frac{2}{3}\pi) + V_{i_0}\cos(\omega t+\theta_{i_0}) \\ v_{i_c}(t) &= V_{i_p}\cos(\omega t+\theta_{i_p}+\frac{2}{3}\pi) + V_{i_n}\cos(\omega t+\theta_{i-n}-\frac{2}{3}\pi) + V_{i_0}\cos(\omega t+\theta_{i_0}) \end{aligned} \quad (3.20)$$

where V_{i_p}, V_{i_n} and V_{i_0} are respectively the amplitudes of the voltage positive, negative and zero sequence components and θ_{i_p}, θ_{i_n} and θ_{i_0} are respectively the phases of the voltage positive, negative and zero sequence components.

In Appendix A it is shown how a set of three-phase unbalanced voltages like the one in (3.20) becomes equivalent in the Stationary Reference Frame (StatRF) to three vectors: one vector $\bar{V}_p$ rotating counter-clockwise at the angular speed of ω, deriving from the positive sequence component; one vector $\bar{V}_n$ rotating clockwise at an angular speed of ω, deriving from the negative sequence component; one vector $\bar{V}_\gamma$ along the γ axis which moves forth and back (the zero sequence component). The magnitudes of these vectors

are given by:

$$|\bar{V}_p| = \sqrt{\frac{3}{2}} V_{i_p} \tag{3.21}$$

$$|\bar{V}_n| = \sqrt{\frac{3}{2}} V_{i_n} \tag{3.22}$$

$$|\bar{V}_\gamma| = \sqrt{3} V_{i_0} \tag{3.23}$$

Combining the positive and negative sequence voltages gives a rotating vector $\bar{V}_{i_{\alpha\beta}}$ with an elliptical trajectory with a major radius equal to $|\bar{V}_p| + |\bar{V}_n|$ and a minor radius equal to $|\bar{V}_p| - |\bar{V}_n|$. The presence of a zero sequence component results in a skewed ellipse.

Figure 3.18 compares the trajectories described in the $\alpha\beta$ plane by the inverter bridge voltage for balanced (in red) and unbalanced (in blue) operation. In order to be able to reproduce the inverter bridge voltage even in the event of an unbalanced operation, the ellipse has to be inside the red circle. Therefore the following condition has to be satisfied:

$$|\bar{V}_p| + |\bar{V}_n| \leq \frac{1}{\sqrt{2}} V_{DC} \tag{3.24}$$

which then becomes equivalent to:

$$V_{i_p} + V_{i_n} \leq \frac{1}{\sqrt{3}} V_{DC}. \tag{3.25}$$

For a given load unbalance, it is possible to determine a value of V_{DC}, bigger than the one needed for simple balanced operation, which satisfies (3.25) and therefore makes possible the synthesization of unbalanced inverter bridge voltages [50].

Turning now to the neutral current and its impact in the design of the inverter, it has been shown that during unbalanced operation i_{L_n} is equal to three times i_{0_0} (the zero sequence component of the load current). The inverter is supposed to supply the neutral current through its fourth leg. If the switches in the fourth leg have the same rating as the switches in the other three legs, then the maximum allowed zero sequence component of the output current is one third of the nominal per-phase output current [50].

Finally, it should be pointed out that at the very beginning of Section 3.2.3, it was assumed that the inverter is capable of supplying a balanced set of output voltages v_{0_a}, v_{0_b} and v_{0_c} even to unbalanced loads. Consequently it has been assumed that the control of the inverter in Figure 3.13 is able to follow the reference v_0^* and it is not affected by unbalanced signals coming from i_L and i_0. This assumption is not always true as the performance of the control of an inverter is affected by unbalanced operation [58, 67].

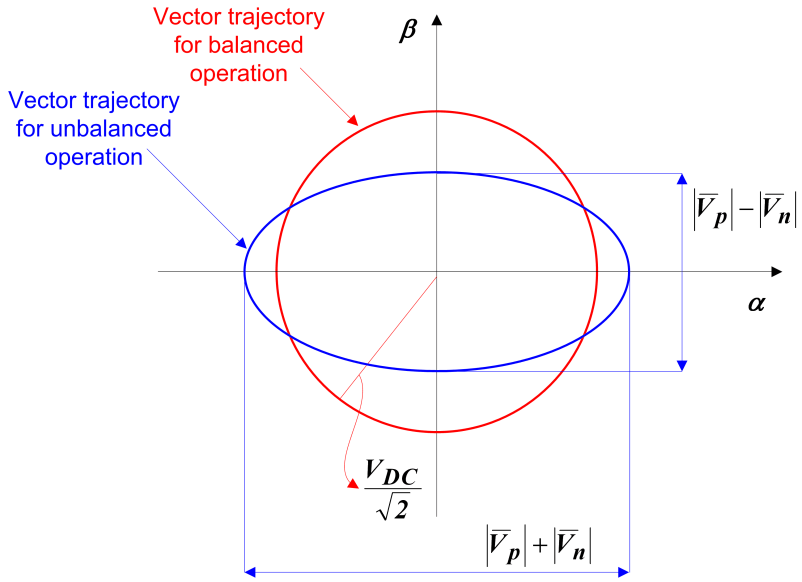


Figure 3.18: Control voltage vector trajectories for balance and unbalanced operation

Chapter 4 will shown the impact of unbalanced operation on different control strategies and some solutions for producing a balanced set of output voltages.

3.3 Microgrid network models

This Chapter has presented a general overview of the different issues affecting microgrid network topology and control. In this Section the two microgrid network models chosen for use throughout this thesis to investigate fault behaviour and fault detection strategies are described.

Figure 3.19 shows the first microgrid network model where the power is supplied by one inverter only. The microgrid is assumed to be part of a LV distribution network from which it got separated with a 4-pole SS as in Figure 3.12. The power is supplied by a three-phase four-leg inverter which is connected to the network through an LC filter (L_f, R_f, C_f) and a coupling impedance (L_{cc}, R_{cc}). The network is a 240 V, 50 Hz, four-wire system with two resistive loads (L_1 and L_2) connected along the line which are assumed to be of 5.6 kW (three-phase) each. As the original LV distribution network is assumed to have a TN-C-S earthing arrangement, the neutral conductor of the microgrid in Figure 3.19 is grounded at multiple points. The microgrid network parameters together with the LC filter and coupling impedance can be found in Table 3.1.

Table 3.1: Microgrid parameters

Microgrid parameters			
Parameter	Value	Parameter	Value
L_f	1.35 mH	L_{line}	0.30 mH
C_f	50 μF	R_{line}	0.36 Ω
R_f	0.1 Ω	L_{linen}	0.30 mH
L_n	0.67 mH	R_{linen}	0.36 Ω
R_n	0.05 Ω	L_l	0.30 mH
L_{cc}	0.35 mH	R_l	0.23 Ω
R_{cc}	0.03 Ω	L_{ln}	0.30 mH
L_{ccn}	0.35 mH	R_{ln}	0.23 Ω
R_{ccn}	0.03 Ω	R_g	10 Ω

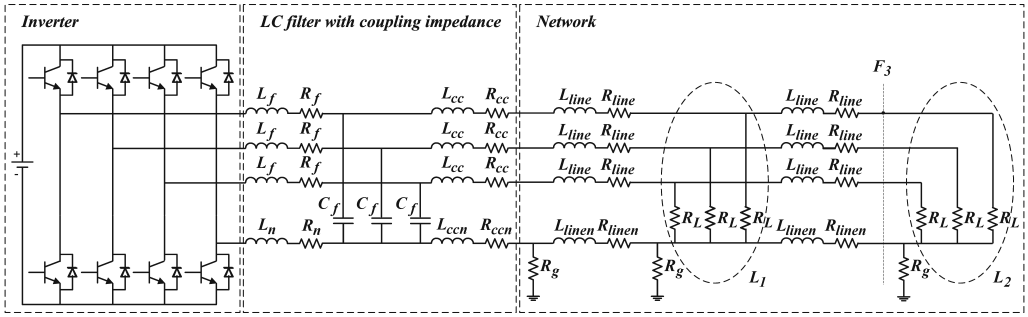


Figure 3.19: Microgrid supplied by a single inverter

The inverter is controlled according to the multi-loop structure in Figure 3.13. In Chapter 4 this control will be implemented first in the Synchronous Reference Frame (SynRF) and then in the Natural Reference Frame (NatRF). The investigation of two different reference frame implementations for the inverter control is done in order to show the influence they have in shaping the response of the inverter and microgrid in the event of a fault.

Figure 3.20 shows the second microgrid network model which is going to be studied. This time the power is supplied by two inverters which are connected through an impedance (L_l, R_l), see Table 3.1. The inverters are identical to the one in Figure 3.19 but with droop functions, see Figure 3.16, added to the multi-loop control structure in Figure 3.13. The model in Figure 3.20 is the extension of the basic model in Figure 3.19. In the next Chapter the differences which parallel inverter operation brings compared with stand-alone operation will be investigated.

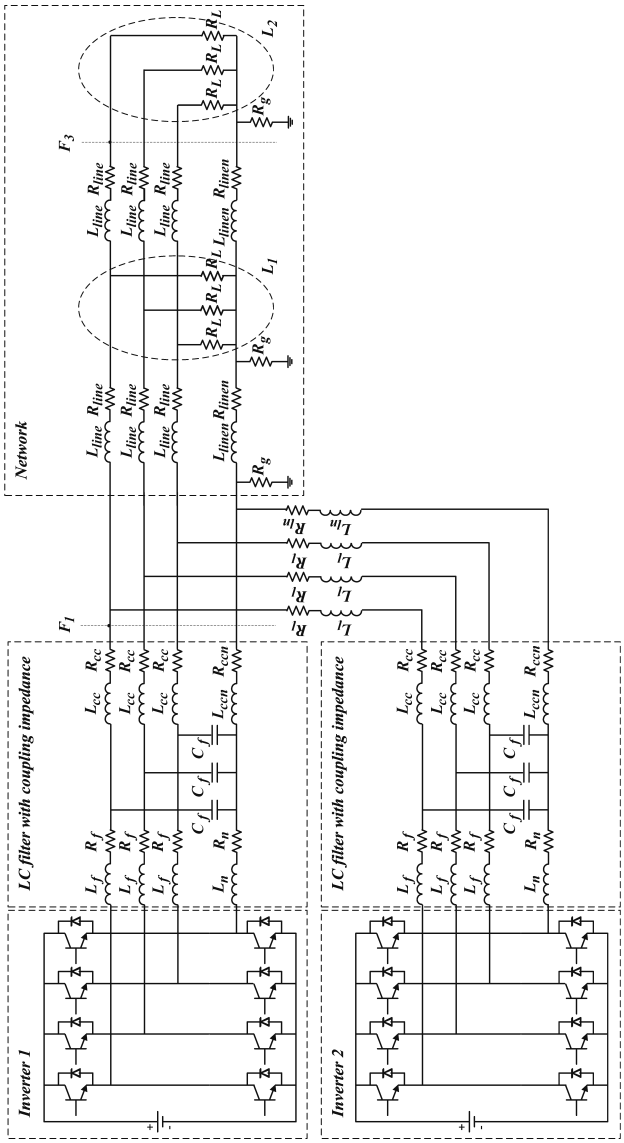


Figure 3.20: Microgrid supplied by two parallel-connected inverters

Chapter 4

Fault response of islanded inverter-only microgrids

The flexibility associated with power electronics interfaces of DG units brings endless possibilities [68] to the operation and control of these systems together with a series of challenges. One of them is the study of their response to network faults. In an islanded microgrid supplied only by inverter-interfaced DG units, the inverter's response to a fault condition is going to dominate the behaviour of the whole system, as shown in studies published in [69, 70]. The purpose of this work is to give an insight into the way some particular inverters respond in the event of a fault, the factors affecting this response and the approach which should be used in order to study it. This is an original approach as it is for the first time that in the study of microgrid fault behaviour and protection the focus is on the control of the inverter.

The analysis is conducted by considering the following three microgrids:

- **Model 1**: a microgrid supplied by a single inverter (see Figure 3.19) controlled in the SynRF;
- **Model 2**: a microgrid supplied by a single inverter (see Figure 3.19) controlled in the NatRF;
- **Model 3**: a microgrid supplied by two parallel-connected inverters (see Figure 3.20) with droop control.

For each model, the inverter control is described with respect to balanced and unbalanced operation and current limiting. Depending on the current limiting strategy implemented in the inverter (current limiting in the SynRF, instantaneous current limiting in the NatRF

and RMS current limiting in the NatRF), each microgrid model can generate different case studies as summarized in Table 4.1.

Table 4.1: Case studies in the analysis of fault response of islanded inverter-only microgrids

		Inverter control	Current limiting
Model 1	Case 1	SynRF	SynRF
	Case 2	SynRF	Instantaneous NatRF
	Case 3	SynRF	RMS NatRF
Model 2	Case 4	NatRF	Instantaneous NatRF
	Case 5	NatRF	RMS NatRF
Model 3	Case 6	Droop	RMS NatRF

The three microgrid models, including the inverter controllers with the different current limiting strategies, are built in the PSCAD software and various faults (balanced and unbalanced) are simulated. In particular, for each case study in Table 4.1, the following faults are considered:

- a three-phase fault (3ϕ);
- a double phase fault (2ϕ) involving phases b and c;
- a double phase-to-ground fault ($2\phi g$) involving phases b and c;
- a single phase-to-ground fault (1ϕ) involving phase a.

From the analysis and the comparison of the different fault responses, the factors which shape the fault behaviour in microgrids are identified.

4.1 Microgrid supplied by a single inverter controlled in the SynRF

4.1.1 Control of a stand-alone inverter in the SynRF

As described in Section 3.2.1, the multi-loop control of a stand-alone inverter can be implemented in different reference frames. Here the implementation in the SynRF is chosen. From the inverter output LC filter in Figure 3.17, the following equations can be

written:

$$\begin{aligned} v_{i_a} &= R_f i_{L_a} + L_f \frac{di_{L_a}}{dt} + v_{0_a} + R_n i_{L_n} + L_n \frac{di_{L_n}}{dt} \\ v_{i_b} &= R_f i_{L_b} + L_f \frac{di_{L_b}}{dt} + v_{0_b} + R_n i_{L_n} + L_n \frac{di_{L_n}}{dt} \\ v_{i_c} &= R_f i_{L_c} + L_f \frac{di_{L_c}}{dt} + v_{0_c} + R_n i_{L_n} + L_n \frac{di_{L_n}}{dt} \end{aligned} \tag{4.1}$$

$$i_{L_a} - i_{0_a} = C_f \frac{dv_{0_a}}{dt} \tag{4.2}$$

$$i_{L_b} - i_{0_b} = C_f \frac{dv_{0_b}}{dt} \tag{4.3}$$

$$i_{L_c} - i_{0_c} = C_f \frac{dv_{0_c}}{dt} \tag{4.4}$$

and

$$i_{L_n} = i_{L_a} + i_{L_b} + i_{L_c} \tag{4.5}$$

By substituting (4.5) into (4.1) and neglecting the filter resistances R_f and R_n, the LC filter equations can be re-arranged as follows:

$$\begin{bmatrix} \dot{i}_{L_a} \\ \dot{i}_{L_b} \\ \dot{i}_{L_c} \end{bmatrix} = \begin{bmatrix} \frac{L_f+2L_n}{L_f(L_f+3L_n)} & -\frac{L_n}{L_f(L_f+3L_n)} & -\frac{L_n}{L_f(L_f+3L_n)} \\ -\frac{L_n}{L_f(L_f+3L_n)} & \frac{L_f+2L_n}{L_f(L_f+3L_n)} & -\frac{L_n}{L_f(L_f+3L_n)} \\ -\frac{L_n}{L_f(L_f+3L_n)} & -\frac{L_n}{L_f(L_f+3L_n)} & \frac{L_f+2L_n}{L_f(L_f+3L_n)} \end{bmatrix} \begin{bmatrix} v_{i_a} - v_{0_a} \\ v_{i_b} - v_{0_b} \\ v_{i_c} - v_{0_c} \end{bmatrix} \tag{4.6}$$

$$\begin{bmatrix} \dot{v}_{0_a} \\ \dot{v}_{0_b} \\ \dot{v}_{0_c} \end{bmatrix} = \begin{bmatrix} \frac{1}{C_f} & 0 & 0 \\ 0 & \frac{1}{C_f} & 0 \\ 0 & 0 & \frac{1}{C_f} \end{bmatrix} \begin{bmatrix} i_{L_a} - i_{0_a} \\ i_{L_b} - i_{0_b} \\ i_{L_c} - i_{0_c} \end{bmatrix} \tag{4.7}$$

By applying the Clarke transformation to (4.6) and (4.7), the system equations become:

$$\begin{bmatrix} \dot{i}_{L_\alpha} \\ \dot{i}_{L_\beta} \\ \dot{i}_{L_\gamma} \end{bmatrix} = \begin{bmatrix} \frac{1}{L_f} & 0 & 0 \\ 0 & \frac{1}{L_f} & 0 \\ 0 & 0 & \frac{1}{L_f+3L_n} \end{bmatrix} \begin{bmatrix} v_{i_\alpha} - v_{0_\alpha} \\ v_{i_\beta} - v_{0_\beta} \\ v_{i_\gamma} - v_{0_\gamma} \end{bmatrix} \tag{4.8}$$

$$\begin{bmatrix} \dot{v}_{0_\alpha} \\ \dot{v}_{0_\beta} \\ \dot{v}_{0_\gamma} \end{bmatrix} = \begin{bmatrix} \frac{1}{C_f} & 0 & 0 \\ 0 & \frac{1}{C_f} & 0 \\ 0 & 0 & \frac{1}{C_f} \end{bmatrix} \begin{bmatrix} i_{L_\alpha} - i_{0_\alpha} \\ i_{L_\beta} - i_{0_\beta} \\ i_{L_\gamma} - i_{0_\gamma} \end{bmatrix} \tag{4.9}$$

Finally the Park transformation can be applied to (4.8) and (4.9) and the system equations can be expressed in the SynRF (or in $dq\gamma$ coordinates) as:

$$\begin{bmatrix} \dot{i}_{L_d} \\ \dot{i}_{L_q} \\ \dot{i}_{L_\gamma} \end{bmatrix} = \begin{bmatrix} 0 & \omega & 0 \\ -\omega & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{L_d} \\ i_{L_q} \\ i_{L_\gamma} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_f} & 0 & 0 \\ 0 & \frac{1}{L_f} & 0 \\ 0 & 0 & \frac{1}{L_f+3L_n} \end{bmatrix} \begin{bmatrix} v_{i_d} - v_{0_d} \\ v_{i_q} - v_{0_q} \\ v_{i_\gamma} - v_{0_\gamma} \end{bmatrix} \tag{4.10}$$

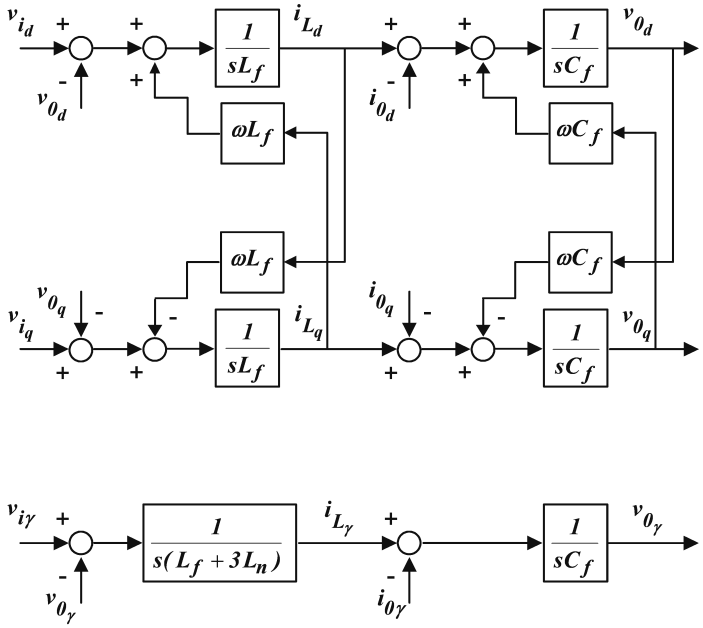


Figure 4.1: Equivalent block diagrams in SynRF of the LC filter

$$\begin{bmatrix} \dot{v}_{0_d} \\ \dot{v}_{0_q} \\ \dot{v}_{0_\gamma} \end{bmatrix} = \begin{bmatrix} 0 & \omega & 0 \\ -\omega & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_{0_d} \\ v_{0_q} \\ v_{0_\gamma} \end{bmatrix} + \begin{bmatrix} \frac{1}{C_f} & 0 & 0 \\ 0 & \frac{1}{C_f} & 0 \\ 0 & 0 & \frac{1}{C_f} \end{bmatrix} \begin{bmatrix} i_{L_d} - i_{0_d} \\ i_{L_q} - i_{0_q} \\ i_{L_\gamma} - i_{0_\gamma} \end{bmatrix} \tag{4.11}$$

Figure 4.1 shows the block diagram interpretation of (4.10) and (4.11). As a result of the transformations, the original LC filter in $dq\gamma$ coordinates is equivalent to three models, one for each coordinate. Consequently the control system in Figure 3.13 implemented in $dq\gamma$ coordinates becomes equivalent to three multi-loops: one for the d component, one for the q component and one for the γ component. Figure 4.2 shows the equivalent multi-loop control in $dq\gamma$ coordinates.

The output reference voltage v_0^* is transformed in $dq\gamma$ coordinates into references $v_{0_d}^*$, $v_{0_q}^*$ and $v_{0_\gamma}^*$. Reference $v_{0_\gamma}^*$ is zero as the inverter is controlled to supply a balanced three-phase set of output voltages. Also, reference $v_{0_q}^*$ is set to zero as it is a common practice to align the output voltage to the d axis and therefore have zero component on the q axis. Figure 4.2 shows the de-coupling terms which have been added to de-couple the control of the d and q axes. Output current and voltage feedforward terms are shown as well together with a saturation block in each loop which represents the action of the control to limit the amount of inductor current supplied by the inverter.

During balanced operation, the original sinusoidal phase variables become equivalent

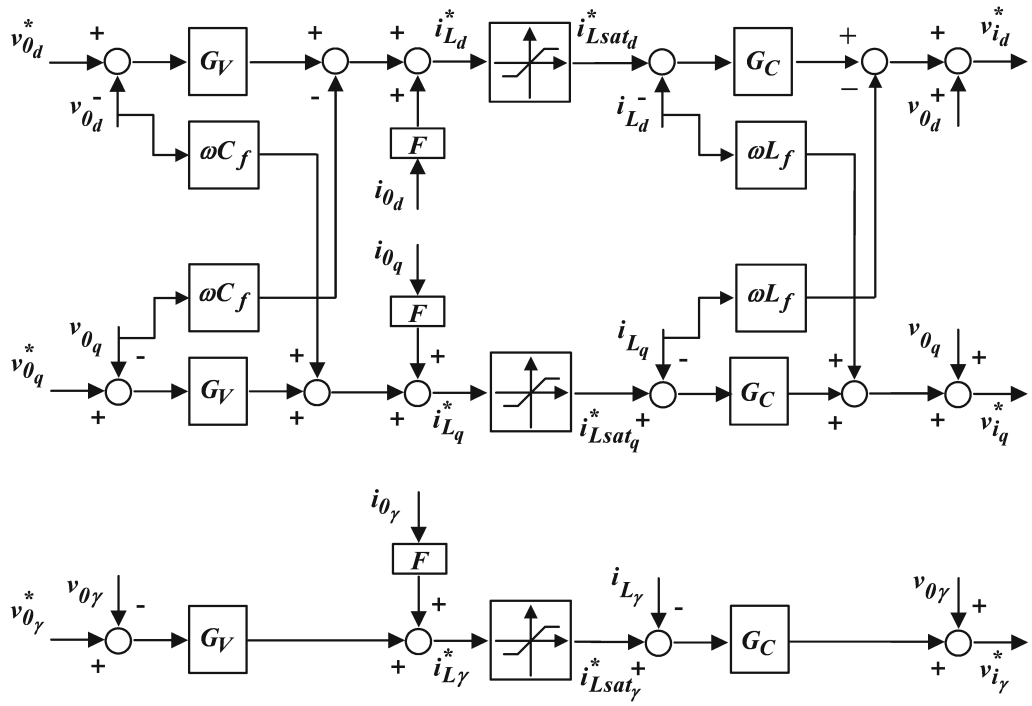


Figure 4.2: Multi-loop control of a stand-alone inverter in the SynRF

to DC signals in the SynRF (see Appendix A for the full detailed derivation). Another consequence of balanced operation is that there would be no γ component and the control would reduce to the d and q component control loops in Figure 4.2. As dq components are DC signals, they can be easily controlled by PI regulators in the voltage and current loops. This is the main reason behind the popularity of the control of inverters in $dq\gamma$ coordinates. In the microgrid modelled in PSCAD, the voltage and current controllers in d and q loops are therefore PI regulators.

4.1.2 Control in the SynRF and unbalanced operation

A microgrid can be unbalanced during normal operation and in the event of unbalanced faults. During these conditions, the inverter is still required to produce a balanced set of output voltages v_{0_a}, v_{0_b} and v_{0_c} while the output current required by the loads or by the fault is unbalanced as described in Section 3.2.3. A detailed derivation of the $dq\gamma$ components of unbalanced variables can be found in Appendix A.

The presence of unbalance affects the control in the SynRF in two ways. First the negative sequence component introduces a 2ω ripple, where ω is the system angular

frequency. Then the zero sequence component introduces a γ component which now has to be handled by the third loop in Figure 4.2.

Regarding the presence of negative sequence components, the problem is that while PI regulators in the d and q loops work well with simple DC signals, they do not give zero steady-state error with DC signals added to a 2ω ripple. One solution to this problem can be to design a controller with a high gain around 2ω in order to suppress any disturbances at that frequency [50]. A second solution uses a modified Park transformation to control the negative sequence component of the output voltage [58]. Here the negative sequence component of v_0 is obtained in $dq\gamma$ coordinates by modifying the Park transformation as follows:

$$\begin{bmatrix} v_{0_{d_n}} \\ v_{0_{q_n}} \\ v_{0_\gamma} \end{bmatrix} = \begin{bmatrix} cos(\omega t) & -sin(\omega t) & 0 \\ sin(\omega t) & cos(\omega t) & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_{0_\alpha} \\ v_{0_\beta} \\ v_{0_\gamma} \end{bmatrix} \tag{4.12}$$

The new transformation in (4.12) corresponds to a SynRF which rotates in the opposite direction to the original SynRF at the angular frequency $-\omega$. In the new reference frame, the negative sequence component of the voltage will produce a DC component while the positive sequence voltage will give a 2ω ripple.

Based on the modified Park transformation, reference [67] proposes a control scheme shown in Figure 4.3. Here the input variables X_α and X_β are transformed from the StaRF to the SynRF with the Park transformation (labelled as "$dq\gamma^+$"in Figure 4.3) and with the modified Park transformation (labelled as "$dq\gamma^-$"). Four integral controllers ($\frac{k_i}{s}$), two for the positive and two for the negative sequence components are used together with two simple proportional regulators (k_p). This method, together with other proposed control strategies [58], is quite effective in controlling negative sequence components, however this good performance requires a higher complexity in the inverter control structure.

Regarding the presence of zero sequence components, the four-leg topology of the inverter makes it possible to have a third control loop which can regulate the zero sequence component during unbalanced operation. The reference voltage $v^*_{0_\gamma}$ is equal to zero as the output voltage is balanced and the γ sequence loop generates the correct inverter voltage v_{i_γ} to achieve a balanced v_0 even with unbalanced currents.

The main difference between the dq and the γ control loops in Figure 4.2 is that the γ components of current and voltage are not DC signals but sinusoidal in form. As a result, the common PI regulators cannot achieve zero error. A possible solution to this problem

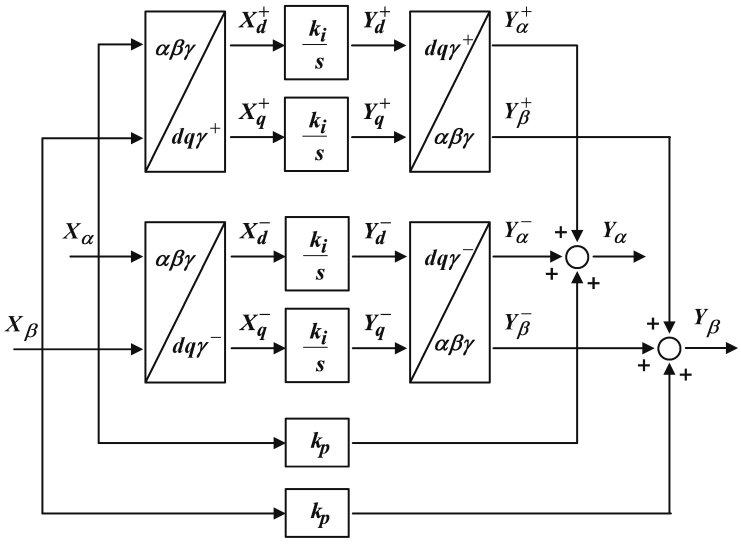


Figure 4.3: Control scheme for positive and negative sequence components in the SynRF [67]

can be the use of a controller which has got an infinite gain at the fundamental frequency and no attenuation at other frequencies. For this purpose a P+Resonant regulator can be used [58]. The transfer function of this regulator is defined as:

$$G(s) = k_p + \frac{2k_i s}{s^2 + \omega^2} \tag{4.13}$$

and Figure 4.4 shows its Bode plot for different values of k_i and $k_p = 1$. The first term in (4.13) is a proportional gain which is designed in the same way as for a PI regulator. The second term is a second order generalized integrator [71] which achieves very high gain in a narrow band centered around ω, often referred as the resonant frequency. The width of the band depends on the k_i coefficient as shown in Figure 4.4: a high k_i determines a wider band. As a result, with the use of P+Resonant regulators in the γ loop, it is possible to regulate sinusoidal signals. It should be noted that for the purpose of implementation, a more realistic version of the P+Resonant controller has to be adopted, as explained in [72].

4.1.3 Control in the SynRF and current limiting

As discussed in Sections 2.2.1 and 2.4.1, inverters are usually designed to supply a maximum current of typically only twice their nominal value in the event of a network fault. Here three possible current limiting strategies are going to be described:

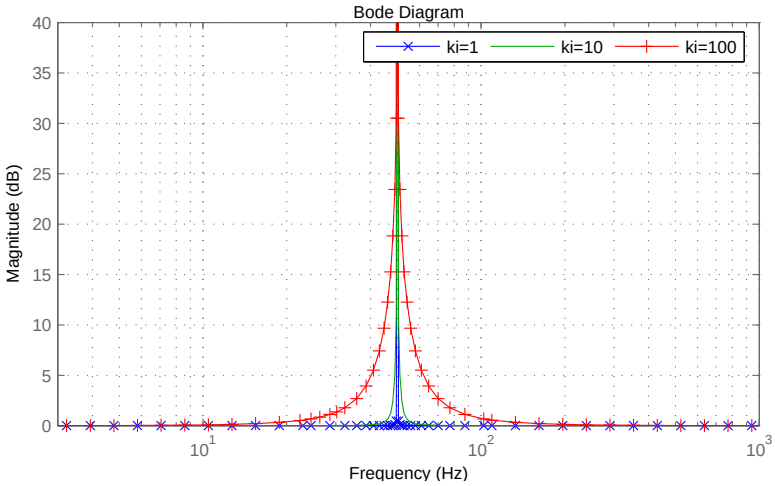


Figure 4.4: Bode diagram of P+Resonant controller for $k_i = 1, 10, 100$ and $k_p = 1$

- current limiting in the SynRF (Case 1 in Table 4.1);
- instantaneous current limiting in the NatRF (Case 2 in Table 4.1);
- RMS current limiting in the NatRF (Case 3 in Table 4.1).

Current limiting in the SynRF

A first approach to current limiting is to limit in the SynRF ($dq\gamma$ coordinates) the current supplied by the inverter, which is the inductor current, i_L, by introducing three saturation blocks as shown in the multi-loop control structure in Figure 4.2. The saturation block in the current loop of the d component, for example, is designed to have a band defined by an upper and a lower hard limit. The reference inductor current, $i^*_{L_d}$, generated by the voltage control loop is passed through the saturation block which limits its value if it is outside the reference band. The output of the saturation block is labelled $i^*_{Lsat_d}$. Similarly $i^*_{L_q}$ and $i^*_{L_\gamma}$ are limited.

This simple current limiting presents three major problems. The first one is related to the presence of 2ω ripple in $i^*_{L_d}$ and $i^*_{L_q}$ during unbalanced operation, which causes problems when passing through the saturation blocks. Assuming unbalanced operation, $i^*_{L_d}$ and $i^*_{L_q}$ can be expressed as:

$$i^*_{L_d} = \sqrt{\frac{3}{2}} I_{L_p} cos(\theta_{L_p}) + \sqrt{\frac{3}{2}} I_{L_n} cos(2\omega t + \theta_{L_n}) \tag{4.14}$$

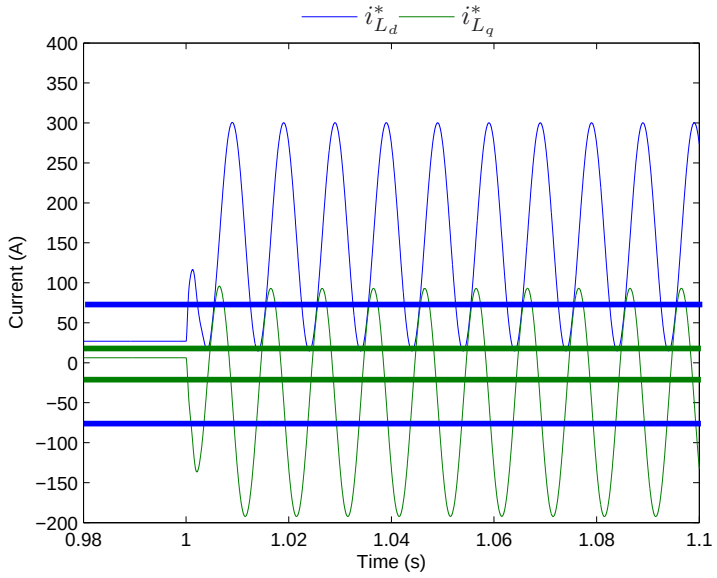


Figure 4.5: Reference inductor currents $i^*_{L_d}$ and $i^*_{L_q}$ for a phase-to-phase fault (ab) with no current limiting compared with saturation limits

$$i^*_{L_q} = \sqrt{\frac{3}{2}} I_{L_p} sin(\theta_{L_p}) - \sqrt{\frac{3}{2}} I_{L_n} sin(2\omega t + \theta_{L_n}) \tag{4.15}$$

where I_{L_p} and I_{L_n} are the amplitudes of the positive and negative sequence components of the inductor current and θ_{L_p} and θ_{L_n} are the phases of the positive and negative sequence current components (see also Appendix A). Equations (4.14) and (4.15) show that $i^*_{L_d}$ and $i^*_{L_q}$ have waveforms not generally symmetrical around the x axis and that, depending on the type of fault, they can have large ripples.

As an example, Figure 4.5 shows the reference inductor currents $i^*_{L_d}$ and $i^*_{L_q}$ for a phase-to-phase fault (ab) in the microgrid with no current limiting . It can be seen that they contain a constant DC term plus a 2ω term which is caused by the negative sequence component. In the same Figure, the hard limits in the saturation blocks in the d (in blue) and q (in green) loops are drawn in order to clearly show that the ripples in $i^*_{L_d}$ and $i^*_{L_q}$ make the reference currents swing in and out the saturation blocks' reference bands.

If current limiting is implemented by simply placing two saturation blocks as shown in Figure 4.2 and $i^*_{L_d}$ and $i^*_{L_q}$ are limited within their reference bands, the resulting saturated signals $i^*_{Lsat_d}$ and $i^*_{Lsat_q}$ have a clipped waveform shape, see Figure 4.6, which causes highly distorted inverter output voltages and currents.

The second problem in the limiting of current in $dq\gamma$ coordinates relates to the

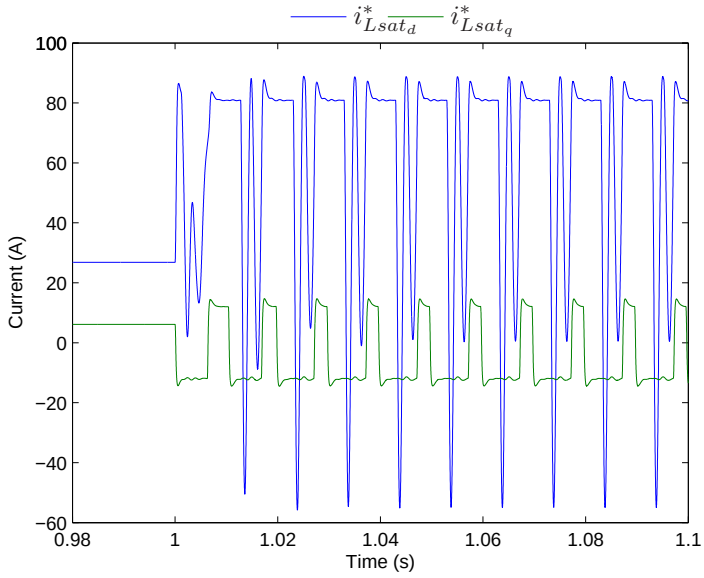


Figure 4.6: Saturated reference inductor currents $i^*_{Lsat_d}$ and $i^*_{Lsat_q}$ for a phase-to-phase fault (ab) with current limiting

presence of saturation blocks and PI regulators. As saturation is reached, the feedback loop is broken because the output of the saturation block is no more influenced by its input. The integral action of the PI controller drifts to very large values (the integrator winds up) and causes large overshoots and settling times as the system desaturates. This phenomenon can be observed in Figure 4.6. Here it is possible to note some large oscillations in $i^*_{Lsat_d}$ after each desaturation.

There are various control techniques which can be used in order to prevent the wind up of the integrator value [73]. Figure 4.7 shows the structure of the tracking or back-calculation anti-windup applied to a PI controller. The method consists of re-computing the integral term once the controller saturates. The term $\frac{1}{K_a}$ is usually called the tracking time constant and it determines the rate at which the integral term is reduced. Figure 4.8 shows the saturated reference inductor currents the tracking anti-windup is implemented in the voltage loop of the inverter control. As can be seen, the oscillations are reduced however there will still be some distortion in the output voltage and current waveforms when transformed into phase quantities.

The third problem relates to the limiting of the γ component of the inductor current. Assuming unbalanced operation, $i^*_{L_\gamma}$ can be expressed as:

$$i^*_{L_\gamma} = \sqrt{3} I_{L_0} cos(\omega t + \theta_0) \tag{4.16}$$

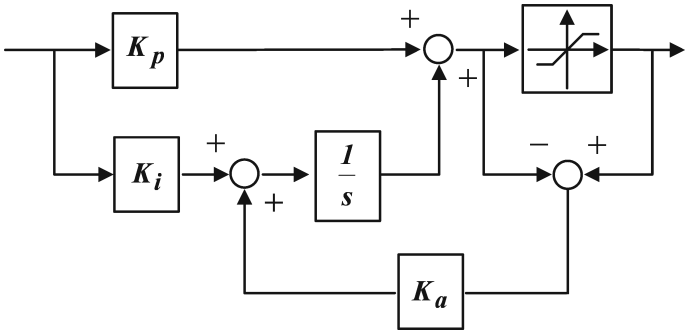


Figure 4.7: Tracking anti-windup PI controller

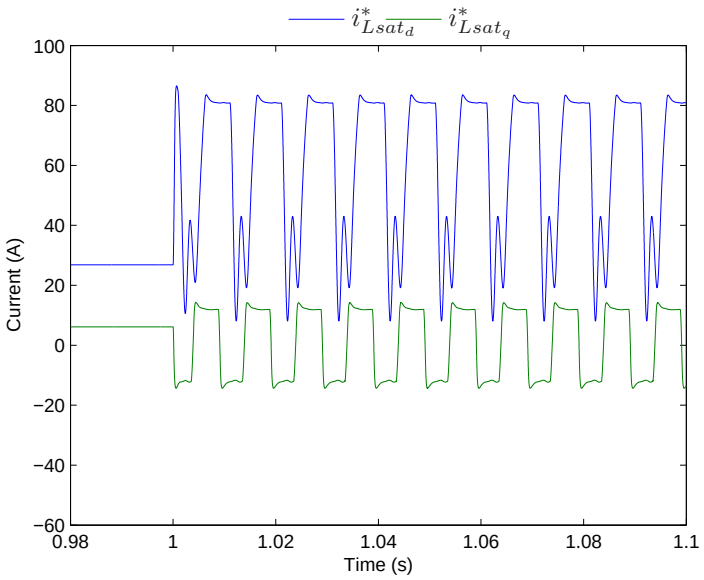


Figure 4.8: Saturated reference inductor currents $i^*_{Lsat_d}$ and $i^*_{Lsat_q}$ with back-calculation anti-windup for a phase-to-phase fault (ab)

where I_{L_0} and θ_0 are the magnitude and the phase angle of the zero sequence component of the inductor current. In the event of a fault, the limiting of $i^*_{L_\gamma}$ with a saturation block with hard limits produces distorted waveforms as $i^*_{L_\gamma}$ is a sinusoidal signal. Moreover if $i^*_{L_\gamma}$ is limited to a constant value, it produces a DC component which is added to the inductor phase currents.

From the above discussion it is clear that current limiting in the SynRF is not a straight forward process. The inverter's requirement to protect its circuitry by limiting the supplied current has to be integrated with the requirements of the network to which the inverter is supplying power. Moreover there is not a specific standard, which regulates the behaviour of inverters in the event of network faults, that can be used as a reference. For what concerns the distortion of the waveforms produced by the inverter when current limiting, the closest standards which could potentially be applied are the ones on power quality for distributed generation and electrical distribution systems [23, 74]. In particular the EN 50160 standard [74], which regulates the voltage quality, could be generally applied to islanded microgrids. However the limits set by the standard on voltage harmonic distortion do not apply to inverter fault response as those limits refer to "normal operating conditions" [75]. Indeed, the standard does not consider "voltage quality events" like faults [75]. This is an important limitation which rules out the application of this standard in the regulation of the inverter fault response. Nevertheless, it can be safely assumed that in the event of a fault the inverter should be expected to produce undistorted waveforms while limiting the supplied current.

It can also be assumed that the inverter should be expected to behave in a "predictable" way. As this Chapter will show, the flexibility in the inverter's control can potentially produce many different fault responses. From the point of view of fault detection, this variety in responses is not auspicious. In contrast, a well controlled and predictable inverter response in the event of a fault makes it possible to design a suitable fault detection method capable of capturing the particular footprint (e.g. voltage drop and voltage sequence components) produced by the inverter in the microgrid. As the inverter's control is quite flexible, it is possible to design a control strategy which combines inverter's requirements (e.g. current limits) and network's requirements (e.g. no waveform distortion and fault detection) thus giving a well defined response for different microgrid network faults.

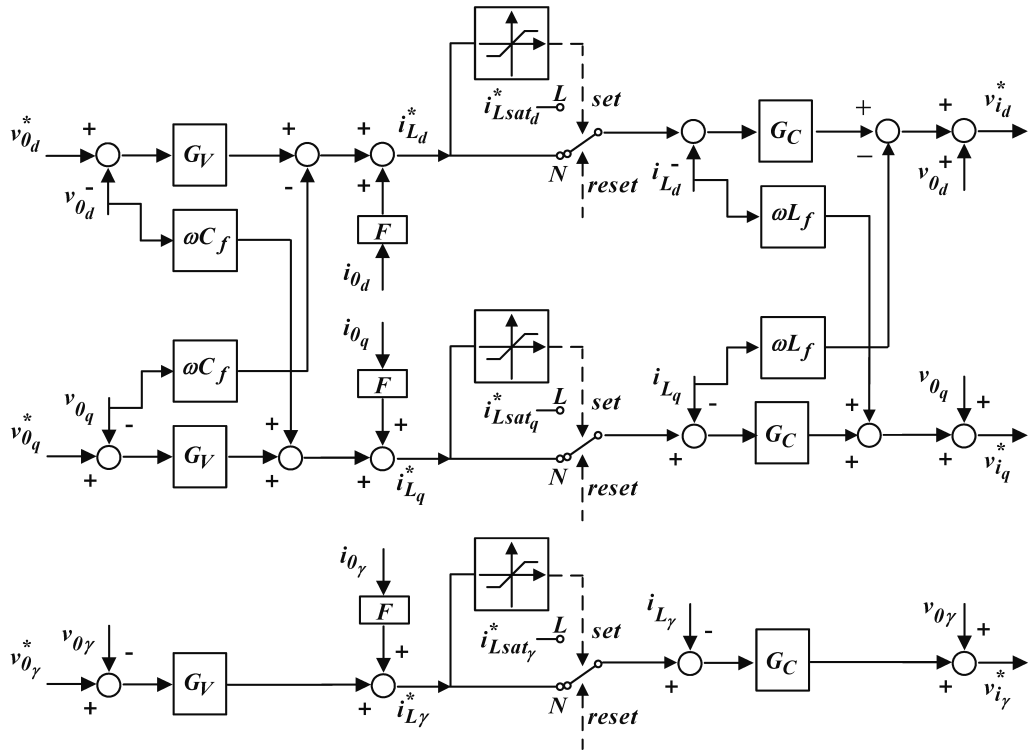


Figure 4.9: SynRF ($dq\gamma$ coordinates) voltage and current control loops with current limiting in the SynRF

Based on this design principle, the current limiting in $dq\gamma$ coordinates is chosen to be done by using three saturation blocks and limiting $i^*_{L_d}$, $i^*_{L_q}$ and $i^*_{L_\gamma}$ to three fixed values $i^*_{Lsat_d}$, $i^*_{Lsat_q}$ and $i^*_{Lsat_\gamma}$ as soon as they reach the hard limits in the saturation blocks. Figure 4.9 shows the resulting modified approach to current limiting in the SynRF which is going to be implemented in this Chapter. Under normal operation, each switch is closed on position N. However, as soon as one component of the inductor current reaches the limit in its saturation blocks, then a signal is generated which makes the switch move from N to L position. After the fault is cleared and the microgrid goes back to normal operation, each switch has to go back to position N. The resetting strategy is not going to be considered in this thesis, however possible approaches could be based on impedance and voltage measurements.

The hard limits in the saturation blocks would have to be chosen in order to allow unbalanced operation. In particular, unbalanced loading produces values of $i^*_{L_d}$, $i^*_{L_q}$ and $i^*_{L_\gamma}$ similar to the ones in equations (4.14), (4.15) and (4.16). An admissible level of load unbalance in the network, here assumed as 20% as in [40], should not trigger any current

limiting. Section 4.1.4 will illustrate how to take into account unbalance and design the hard limits in the saturation blocks.

The fixed limits $i^*_{Lsat_d}$ and $i^*_{Lsat_q}$ have to be chosen according to the rating of the inverter as Section 4.1.4 will describe. On the other hand, here it is chosen not to supply any γ component of the inductor current in the event of a fault. Thus $i^*_{Lsat_\gamma}$ is equal to zero.

The switching of $i^*_{L_d}$, $i^*_{L_q}$ and $i^*_{L_\gamma}$ to $i^*_{Lsat_d}$, $i^*_{Lsat_q}$ and $i^*_{Lsat_\gamma}$ can be done separately (i.e. each inductor current component is switched as soon as it hits the hard limit) or simultaneously (i.e. as one current reaches its limit, the control switches the other current components to their fixed values). However some faults (e.g. single phase-to-ground) may not cause the switching of all three currents. Moreover, phase faults in a microgrid supplying unbalanced faults may not trigger the limit on $i^*_{L_\gamma}$, therefore allowing the injection of zero sequence current by the inverter. As a result, in order to have a uniform and predictable response for any type of fault, it is chosen to simultaneously switch all three switches in Figure 4.9 as soon as one current reaches the hard limit in its saturation block.

By keeping the values of $i^*_{L_d}$ and $i^*_{L_q}$ equal to a fixed value and $i^*_{L_\gamma}$ equal to zero, the inverter behaves in the event of a fault like a constant positive sequence current source. This supplied current is free from any waveform distortion. At the same time the current limiting makes sure that the current in each inverter leg does not exceed its maximum value.

It should be noted that, once the value of $i^*_{L_d}$, $i^*_{L_q}$ and $i^*_{L_q}$ are kept constant, the voltage feedback loop is completely broken because the output of the saturation block is no more influenced by its input. This break in the loop reduces the two loop control of the inverter to a single current loop. The consequences of this will be analyzed later in this Chapter and modelled in Chapter 5.

Instantaneous current limiting in the NatRF

Another approach to current limiting in inverters is to limit the inductor current in the NatRF. This limiting can be done on an instantaneous basis or on an RMS basis. Figure 4.10 shows how instantaneous current limiting in the NatRF can be implemented when controlling the inverter in the SynRF. Here $i^*_{L_d}$, $i^*_{L_q}$ and $i^*_{L_\gamma}$ are transformed back in the NatRF, the resulting $i^*_{L_a}$, $i^*_{L_b}$ and $i^*_{L_c}$ are individually limited by three saturation blocks

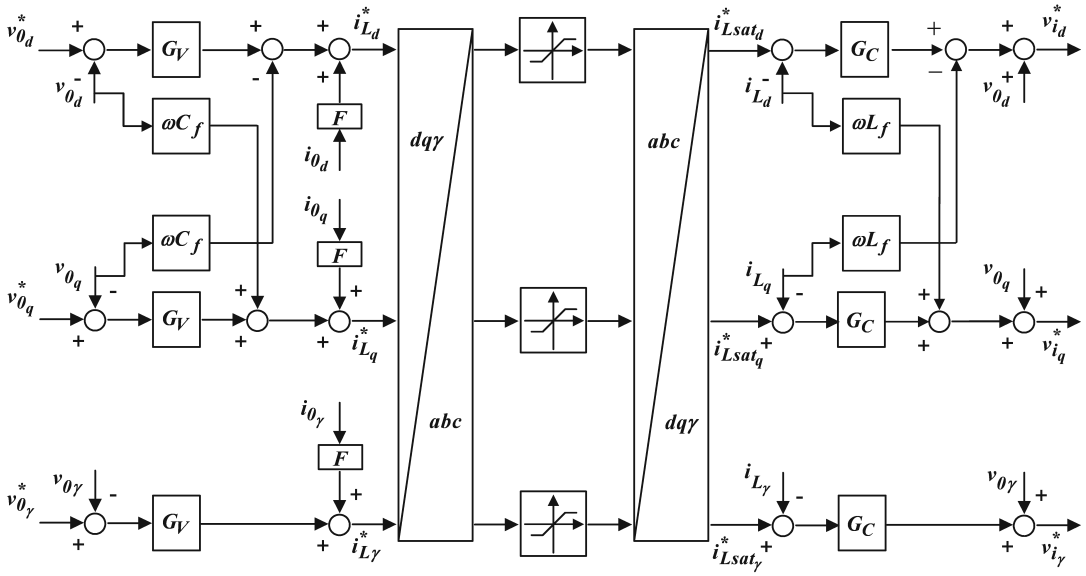


Figure 4.10: SynRF ($dq\gamma$ coordinates) voltage and current control loops with instantaneous current limiting in the NatRF

containing simple upper and lower hard limits. The phase inductor reference currents are instantaneously limited by cutting any parts of the sinusoidal waveforms outside the limit bands of the saturation blocks. After being limited, the inductor currents are transformed back in the SynRF.

The choice of hard limits in the saturation blocks is much simpler compared to the previous limiting strategy. Indeed the hard limits are simply chosen to be equal to twice the inverter nominal current. This current limiting strategy is easier to implement compared to the previous one as it directly limits the magnitude of each phase inductor current. However it requires additional reference frame transformations and can produce distorted output waveforms.

RMS current limiting in the NatRF

A third approach to current limiting in the NatRF on an RMS basis is shown in Figure 4.11. Here $i^*_{L_d}$, $i^*_{L_q}$ and $i^*_{L_\gamma}$ are again transformed back in the NatRF and the resulting $i^*_{L_a}$, $i^*_{L_b}$ and $i^*_{L_c}$ are passed through three saturation blocks like the ones described in Figure 4.10. The output of each saturation block generates a signal which operates a switch. Under normal operation, each switch is closed on position N. As soon as a current in one phase (for example phase a) reaches a pre-set limit in the saturation block, then the output of the block makes the corresponding switch to move from N to L position. As

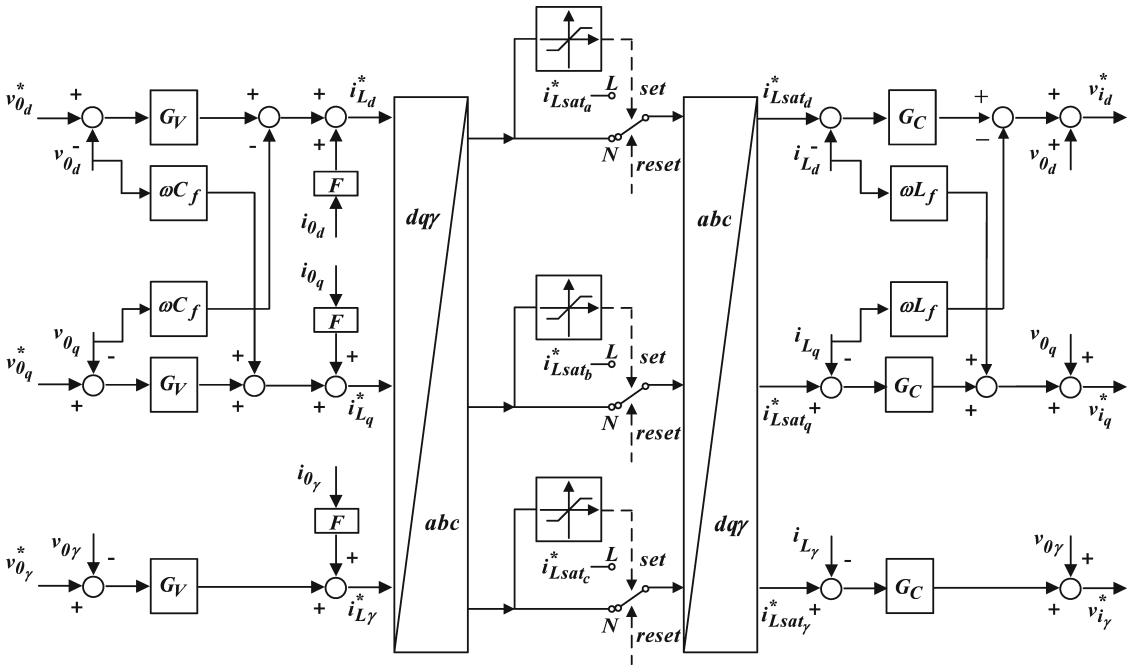


Figure 4.11: SynRF ($dq\gamma$ coordinates) voltage and current control loops with RMS current limiting in the NatRF

a result, the inverter goes into current limiting in phase a: the voltage control loop is broken and $i^*_{L_a}$ becomes equal a fixed sinusoidal reference inductor current, $i^*_{Lsat_a}$, equal to twice the inverter nominal current. This inverter mode of operation will continue until the conditions for the normal operation of the inverter are restored in the microgrid (e.g. the fault is cleared). A "reset"command will then operate the switch and close it back to its normal operating position N. This resetting strategy is not going to be discussed in this thesis. The RMS current limiting in the NatRF requires additional reference frame transformations and the implementation of a switching strategy from normal operation to current limiting operation, however it can avoid the generation of distorted output waveforms.

The fault responses of the microgrid with the three limiting techniques in Figures 4.9, 4.10 and 4.11 are going to be simulated and compared in Sections 4.1.5 and 4.1.6.

4.1.4 System description: Model 1

The purpose of this Section is to describe all the data needed and the design choices which have to be made in order to build the first microgrid model, Model 1 in Table 4.1.

The microgrid model is shown in Figure 3.19. A general description of the microgrid

network has been given in Section 3.3 and Table 3.1 contains all the parameters including the LC filter and the coupling impedance. The power is supplied by one 17 kVA inverter with a DC bus voltage equal to 700 V. The DG source is considered as ideal and the DC bus dynamics neglected as in [29, 32]. Moreover, the switching process of the inverter is also neglected on the assumption that high switching frequencies are used [63]. The voltage and current controllers in the d and q loops are PI regulators while a P+Resonant and P regulator are respectively used in the γ voltage and current control loop. The current loops are designed with a bandwidth around 1600 Hz while the voltage loops have a 400 Hz bandwidth.

Usually, the inverter's rating S_{inv} is chosen to be a bit above the maximum power, P_{max}, supplied by the prime mover in order to be able to supply reactive power if necessary. A general rule which can be applied is [48]:

$$S_{inv} = \frac{P_{max}}{cos\varphi} \tag{4.17}$$

where $cos\varphi$ is the system power factor. From this rating it is possible to calculate the inverter nominal current I_n:

$$I_n = \frac{S_{inv}}{3 * V_n} \tag{4.18}$$

where V_n is the nominal phase voltage which is 240 V. Here P_{max} is assumed to be 15 kW and the inverter's rating, S_{inv}, is 17 kVA. The inverter is therefore capable of supplying a nominal current I_n equal to 23.61 A and a maximum fault current equal to 47.22 A, which is twice I_n. It is important to notice that I_n refers to the inverter output current i_0. However the current limiting strategies are concerned with limiting the value of the inductor current i_L which is effectively the current which flows in the inverter legs. Therefore given a maximum value for the output current, the corresponding maximum value for the inductor current has to be determined.

In order to implement in PSCAD the first current limiting strategy in the SynRF, see Figure 4.9, the fixed values $i^*_{Lsat_d}$, $i^*_{Lsat_q}$ and the hard limits in the three saturation blocks have to be determined. The values $i^*_{Lsat_d}$ and $i^*_{Lsat_q}$ are calculated from the maximum inverter fault current I_n according to the following procedure. Assuming the inverter to operate at full power (e.g. $P = 15kW$ and $Q = 8kVAr$), from equations (3.4) and (3.5) it is possible to calculate i_{0_d} and i_{0_q}. The values of v_{0_d} and v_{0_q} are set by the voltage control loop and are equal to 415 V and 0 V respectively. By substituting the values of p, q, v_{0_d}

and v_{0_q} into (3.4) and (3.5), the output current are equal to:

$$i_{0_d} = 36.14A \tag{4.19}$$

$$i_{0_q} = -19.27A \tag{4.20}$$

The values of i_{L_d} and i_{L_q} can be calculated by considering the equations in (4.10) and (4.11). In steady-state operation the derivative terms become zero and therefore the relations can be written as:

$$0 = \omega i_{L_q} + \frac{1}{L}(v_{i_d} - v_{0_d}) \tag{4.21}$$

$$0 = -\omega i_{L_d} + \frac{1}{L}v_{i_q} \tag{4.22}$$

$$i_{0_d} = i_{L_d} \tag{4.23}$$

$$0 = -\omega v_{0_d} - \frac{1}{C}(i_{0_q} - i_{L_q}) \tag{4.24}$$

The maximum corresponding values of i_{L_d} and i_{L_q} for a full power operation are 36.14 A and -12.75 A respectively. In the event of a fault, $i^*_{Lsat_q}$ is chosen to be fixed and equal to -12.75 A. The value of $i^*_{Lsat_d}$ can be then found by considering the maximum available fault current as follows:

$$\sqrt{\frac{3}{2}}47.22\sqrt{2} = \sqrt{i^{*2}_{0_d} + i^{*2}_{0_q}} \tag{4.25}$$

which gives $i^*_{Lsat_d}$ equal to 79.48 A. Finally it has been chosen to keep the value of $i^*_{Lsat_\gamma}$ equal to zero.

It should be noted that the choice of fixed values for $i^*_{L_d}$ and $i^*_{L_q}$ is not unique. The specification which is usually given is that the inverter can supply a maximum current twice its nominal value. In order to calculate the corresponding dq components of the inductor current, it has been assumed that the output voltage v_0 is controlled to be aligned to the d axis and that the magnitude of i_0 is equal to twice the maximum inverter current. However, the corresponding values of $i^*_{L_d}$ and $i^*_{L_q}$ are not unique and this can be seen by considering Figure 4.12. Here the output current i_0 is represented by a red circle of constant radius. The second blue circle represents the possible inductor currents i_L where the dq components have been obtained from the following equations:

$$i_{L_d} = i_{0_d} \tag{4.26}$$

$$i_{L_q} = i_{0_q} + \omega C v_{0_d} \tag{4.27}$$

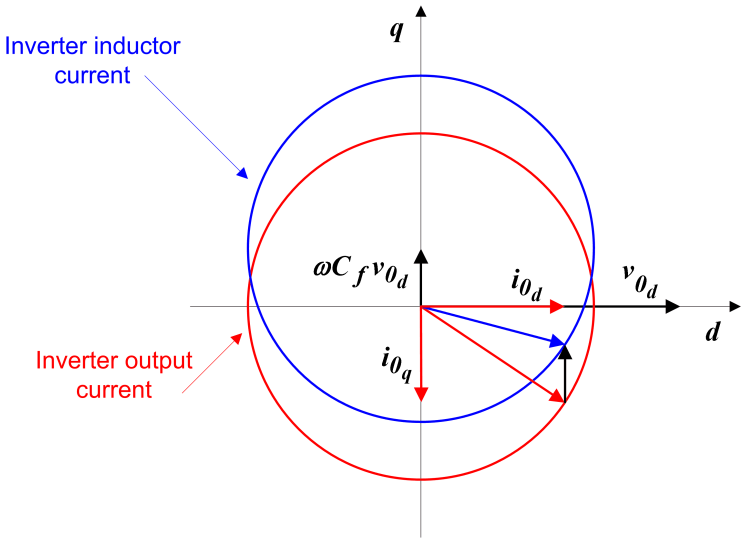


Figure 4.12: Circle diagram of inverter output current i_0 and inverter inductor current i_L in $dq\gamma$ coordinates

Equations (4.26) and (4.27) can be considered as the parametric equations of the circle in Figure 4.12 which describes the vector of the inductor current.

The limits inside the three saturation blocks in Figure 4.9 have to be chosen in such a away that for unbalanced operation the $dq\gamma$ components of the inductor current are passed through the saturation blocks without being affected by the current limiting. As the microgrid is part of the LV distribution network, some form of unbalanced load can be present. Therefore, it is assumed that there can be a power unbalance of 20% as in [40]. Here load unbalance is defined as the percentage difference between the maximum per-phase load power and the minimum per-phase load power over the total three-phase load [40, 50]. So for example, a 20% unbalance in phase a of load L_1 in the microgrid would be defined as follow:

$$P_a = P_b + 0.2P_{tot} \quad , \; Q_a = Q_b + 0.2Q_{tot} \tag{4.28}$$

$$P_b = P_c \quad , \; Q_b = Q_c \tag{4.29}$$

$$P_a + P_b + P_c = P_{tot} \quad , \; Q_a + Q_b + Q_c = Q_{tot} \tag{4.30}$$

where P_a, P_b and P_c are the active powers relative to phases a, b and c, Q_a, Q_b and Q_c are the reactive powers relative to phases a, b and c, P_{tot} and Q_{tot} are the total active and reactive powers of the three-phase load. Now, assuming that each load (L_1 and L_2) in the example microgrid can possibly be equal to half of the inverter nominal power, different

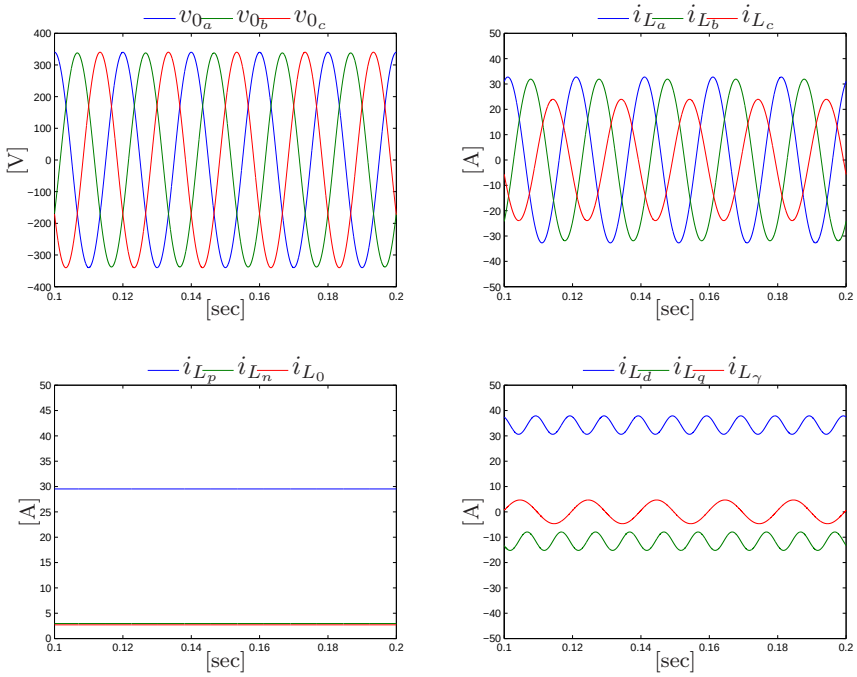


Figure 4.13: Inverter's response to a 20% power unbalance on phase a and on phase b

unbalanced loading conditions can be considered and simulated in PSCAD. Figure 4.13 shows the inverter response to a 20% load unbalance on phase a in L_1 and a 20% load unbalance on phase b in L_2. Figure 4.14 shows the inverter response to a 20% load unbalance on phase a in L_1 and in L_2. This response can be compared with the one for a balanced operation which is shown in Figure 4.15. As predicted, the presence of unbalance in the network generates a ripple in i_{L_d} and i_{L_q} and a γ component which represents the zero sequence component of the inductor current (multiplied by a $\sqrt{3}$ factor). In particular the biggest ripple and values of i_{L_d}, i_{L_q} and i_{L_γ} correspond to the unbalance on the same phase. Therefore the limits in the saturation blocks are chosen so that the values of i_{L_d}, i_{L_q} and i_{L_γ} in Figure 4.14 do not cause any current limiting (i.e. the bands defined by the hard limits in the saturation blocks include the signals in Figure 4.14).

Overall it can be said that the limiting of currents in $dq\gamma$ coordinates is not a trivial task. In this Section some specific design choices have been made and described. However it is hoped that the given description of the process behind the design choices and the discussion on difficulties encountered can in general guide the design of a suitable current limiting strategy in $dq\gamma$ coordinates.

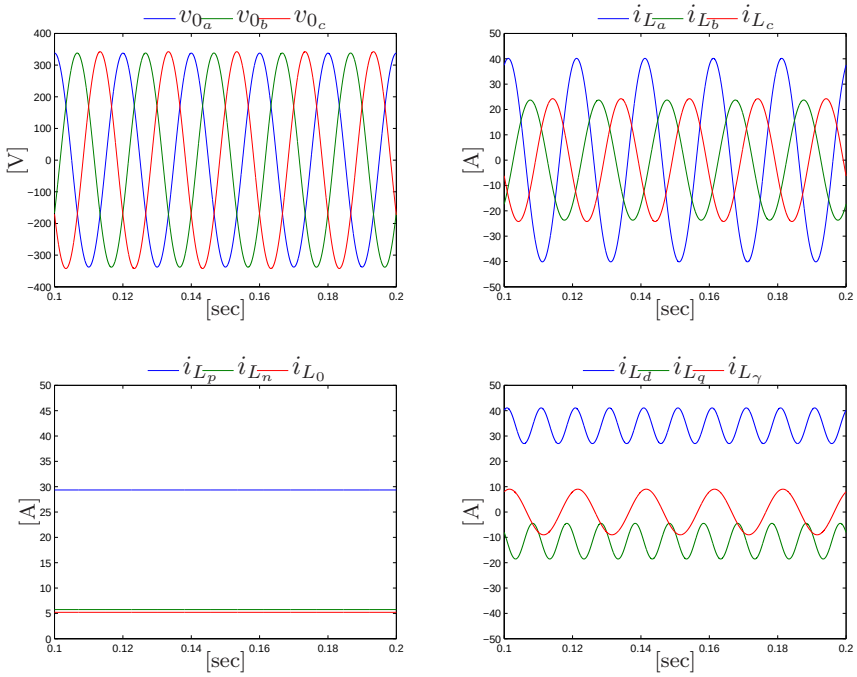


Figure 4.14: Inverter's response to a 20% power unbalance on the same phase a

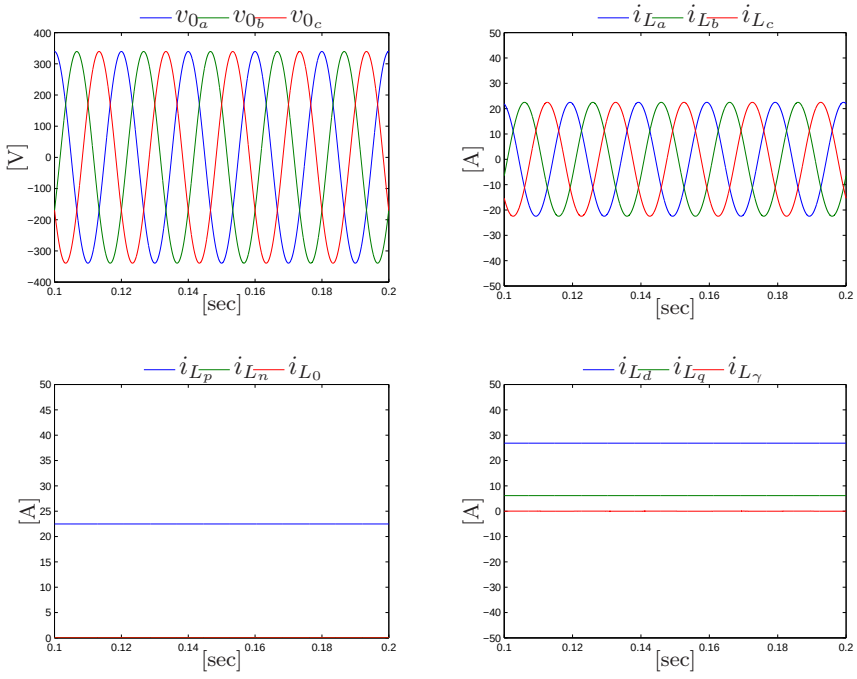


Figure 4.15: Inverter's response to normal balanced operation

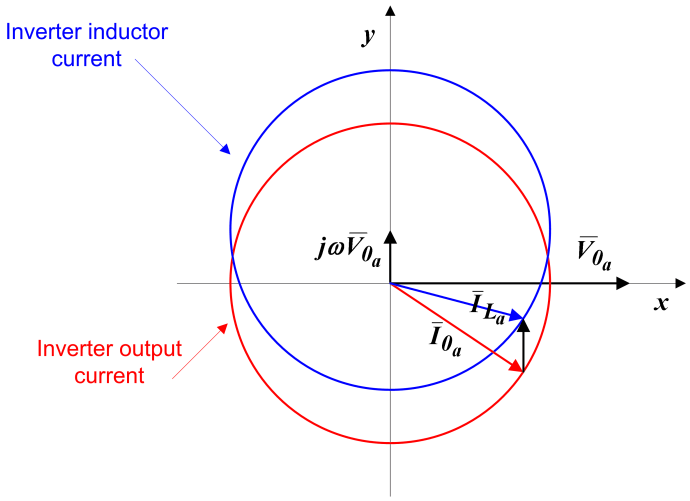


Figure 4.16: Circle diagram of inverter output phase current $\bar{I}_{0_a}$ and inverter inductor phase current $\bar{I}_{L_a}$

The second type of current limiting to be implemented in the microgrid model is the instantaneous limiting in the NatRF, see Figure 4.10. The choice of hard limits in the saturation blocks is based on the maximum inductor current which the inverter can supply. As before, the inverter nominal current is 23.61 A, which refers to the inverter output current, and resulting maximum available current is 47.22 A. Now the relationship between inductor and output phase currents can be simply written as:

$$\bar{I}_{L_a} = \bar{I}_{0_a} + j\omega C\bar{V}_{0_a} \tag{4.31}$$

Given a fixed magnitude of $\bar{I}_{0_a}$, from equation (4.31) a circle diagram can be drawn, see Figure 4.16, which shows the behaviour of $\bar{I}_{L_a}$ for various $\bar{V}_{0_a}$. Here it is chosen to have the maximum reference inductor current relative to phase a aligned with the x axis and as a result from equation (4.31) its maximum value is 47.07 A.

Finally the implementation of the RMS current limiting, see Figure 4.11, is done by using the same hard limits in the saturation blocks which have been calculated for the instantaneous current limiting. The fixed sinusoidal reference currents $i^*_{Lsat_a}$, $i^*_{Lsat_b}$ and $i^*_{Lsat_c}$ are set equal to a balanced positive sequence set of currents whose magnitude is equal to 47.07 A and whose phases are determined by the frequency reference in the inverter control.

4.1.5 Fault response of a microgrid supplied by a single inverter controlled in the SynRF and with current limiting in the SynRF: Case 1

The responses of a microgrid supplied by one single inverter with control and current limiting in the SynRF to a series of faults were simulated in PSCAD. The faults were a bolted three phase (3ϕ) fault (see Figure 4.17), a double phase (2ϕ) fault involving phases b and c (see Figure 4.18), a bolted double phase-to-ground ($2\phi g$) fault again involving phases b and c (see Figure 4.19) and a a single phase-to-ground ($1\phi g$) fault involving phase a (see Figure 4.20). Each fault was always applied at point F_3 (Figure 3.19), at time t=1s. Voltages v_{0_a}, v_{0_b} and v_{0_c} represent the phase-to-neutral voltages at the output of the inverter's filter; i_{L_a}, i_{L_b} and i_{L_c} are the controlled inductor currents; v_a, v_b and v_c are the phase-to-neutral voltages at point F_3 (note that this explains why for faults involving ground the voltages of the faulted phases are not equal to zero, see Figures 4.19 and 4.20); i_a, i_b and i_c are the phase currents at point F_3. From now on, all double phase and double phase-to-ground faults are assumed between phases b and c while single phase faults are assumed to involve phase a. Moreover, all faults are assumed to be bolted unless otherwise stated.

The first thing to be noticed from Figures 4.17, 4.18, 4.19 and 4.20 is the high speed of response of the system compared to that of synchronous machine-based power systems. Traditionally in a synchronous machine-based power network, the time scale of a fault can be divided into three periods: subtransient (first cycle), transient (3-10 cycles) and steady-state. Synchronous generators are modelled as constant voltage sources with a series reactance, whose value differs according to these different time periods. In contrast, the microgrid goes through a transient which lasts less than one cycle. During this very short transient the current is actively limited by the instantaneous (hard) current limits inside the saturation blocks and then by the current limiting strategy as described in Section 4.1.3. The fault transient of an inverter-only microgrid does not exhibit any of the typical features (e.g. slow response and initial high peak currents) of fault response of synchronous machine-based power systems. This completely different behaviour is caused by the high bandwidth of the current control loop which dominates the dynamic response of the inverter and of the microgrid as a whole. Indeed, being a microgrid disconnected from the electricity grid, its dynamics are completely dependent on the inverter's control

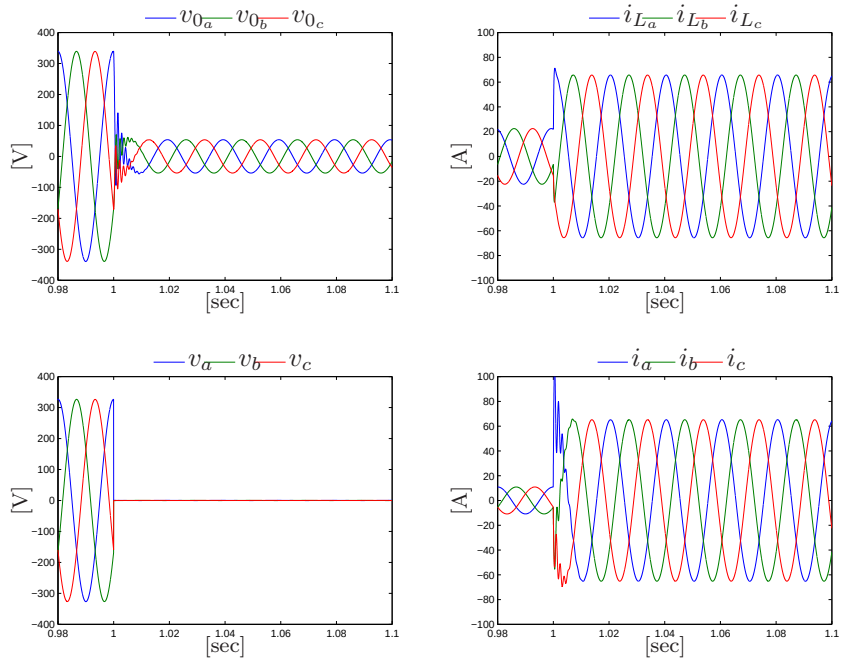


Figure 4.17: Response to a 3ϕ fault at point F_3 of a microgrid supplied by a single inverter (control and current limiting in the SynRF)

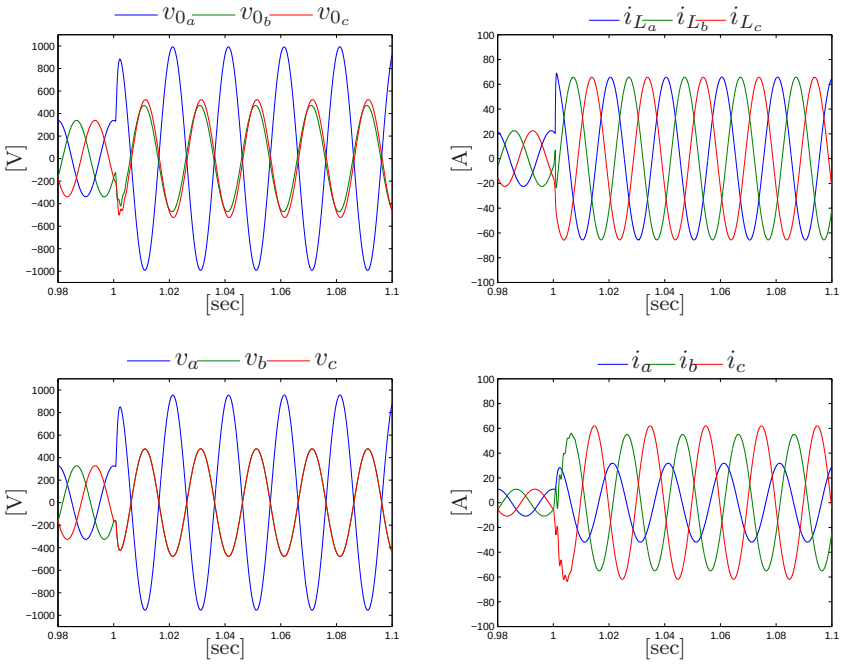


Figure 4.18: Response to a 2ϕ fault at point F_3 of a microgrid supplied by a single inverter (control and current limiting in the SynRF)

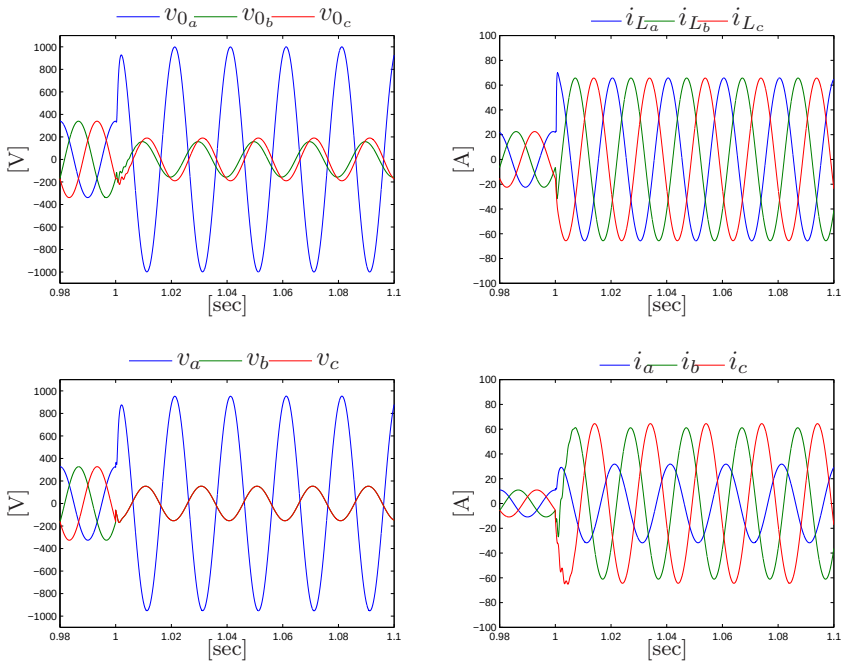


Figure 4.19: Response to a $2\phi g$ fault at point F_3 of a microgrid supplied by a single inverter (control and current limiting in the SynRF)

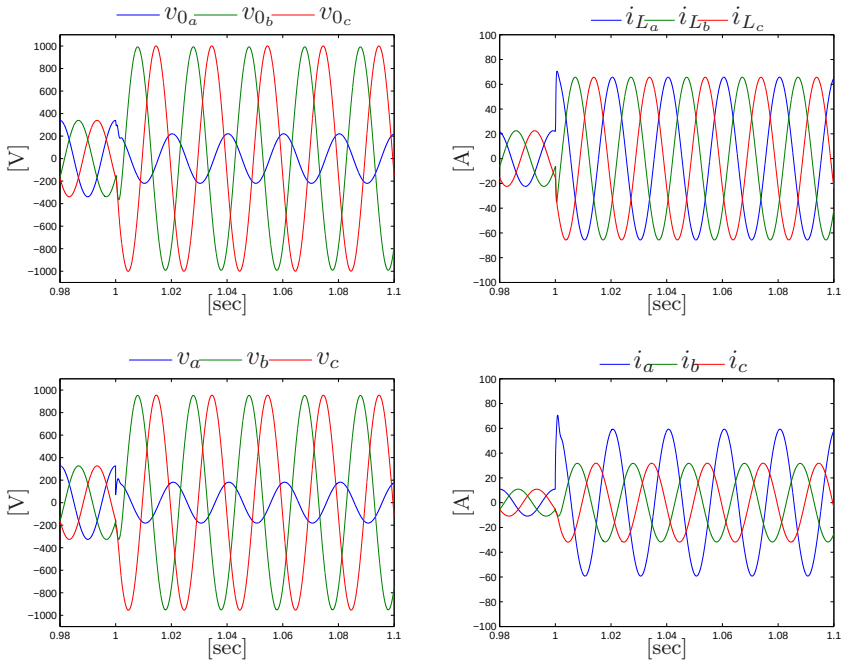


Figure 4.20: Response to a $1\phi g$ fault at point F_3 of a microgrid supplied by a single inverter (control and current limiting in the SynRF)

and that can be implemented in a number of different ways.

Here, in the event of a fault, the inverter behaves as a constant current source as the reference inductor currents $i^*_{L_d}$, $i^*_{L_q}$ and $i^*_{L_\gamma}$ are switched to a constant value. The voltage feedback loop is therefore broken and the two-loop control is reduced to a current loop which is designed to have a very fast response. As a result, irrespective of the fault type, the inverter supplies to each phase a current which is twice the inverter nominal current value.

Figures 4.17, 4.18, 4.19 and 4.20 show that the behaviour of the network voltages are highly dependent on the fault type. For example, the balanced three phase fault leads to a uniform undervoltage while the single phase-to-ground fault produces a large overvoltage on the healthy phases. This behaviour is explained by considering the inverter supplied microgrid as equivalent to a constant current source with a parallel impedance whose value depends on the type of fault. As the inverter injects a fixed amount of current, the impedance presented by the faulted network will determine the voltage.

Inverter voltage limiting

When building the microgrid model, the switching of the inverter has been neglected and the inverter average model developed in [50] has been used. As a result, the inverter bridge voltage v_i has been allowed to vary freely depending on the inverter control and the network and ignoring inverter limitations. However, the overvoltages shown in Figures 4.18, 4.19 and 4.20 are not physically realizable because of the physical limit on the inverter DC bus voltage.

As described in Chapter 3, in SVM the generated reference voltage vector $\bar{V}^*_{i_{\alpha\beta}}$ has to be inscribed in a circle of radius $\frac{V_{DC}}{\sqrt{2}}$. For V_{DC} equal to 700 V, the resulting maximum value of $\bar{V}^*_i$ is 494.4 V which then corresponds to 404 V in *abc* coordinates. Moreover, as the inverter used has four legs, another limit has to be placed on $\bar{V}^*_{i_\gamma}$ as described in [50].

One of the techniques used to limit v^*_i consists of limiting the magnitude of $\bar{V}^*_{i_{dq}}$ to its maximum while maintaining the original phase of $\bar{V}^*_{i_{dq}}$. This can be done with the

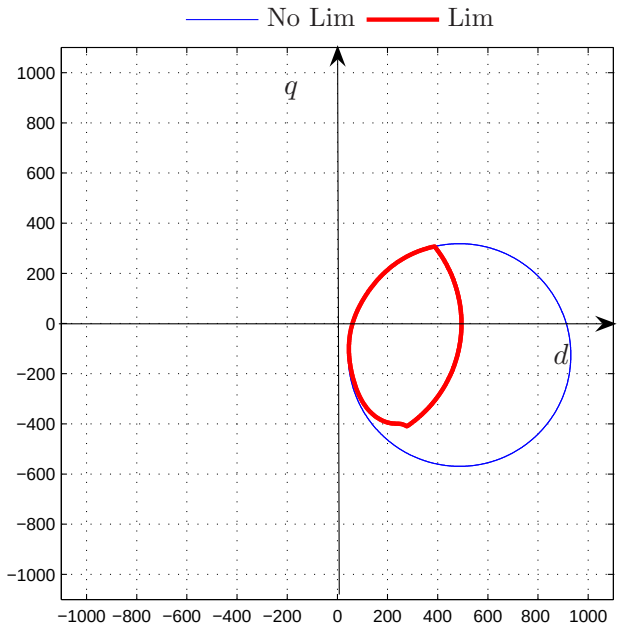


Figure 4.21: Reference inverter bridge voltage v_i^* in dq coordinates for a $2\phi g$ fault at point F_3 in a microgrid supplied by a single inverter (control and current limiting in the SynRF): without instantaneous voltage limiting (blue line), with voltage limiting algorithm as in [76] (red line)

following algorithm [76]:

$$if \quad \left(v_{i_d}^*\right)^2 + \left(v_{i_q}^*\right)^2 \geq \frac{V_{DC}^2}{2} \tag{4.32}$$

$$then \quad \theta = \tan^{-1}\frac{v_{i_q}^*}{v_{i_d}^*} \tag{4.33}$$

$$v_{isat_d}^* = \frac{V_{DC}}{\sqrt{2}}\cos\theta \tag{4.34}$$

$$v_{isat_q}^* = \frac{V_{DC}}{\sqrt{2}}\sin\theta \tag{4.35}$$

$$elseif \quad v_{isat_d}^* = v_{i_d}^* \tag{4.36}$$

$$v_{isat_q}^* = v_{i_q}^* \tag{4.37}$$

Figure 4.21 shows the trajectory of $\bar{V}_{i_{dq}}^*$ for a bolted double phase-to-ground fault with no voltage limiting (in blue) and with the limiting according to this algorithm (in red). Figure 4.22 shows the corresponding behaviour of $\bar{V}_{i_{\alpha\beta}}^*$. The values of $\bar{V}_{i_{dq}}^*$ and $\bar{V}_{i_{\alpha\beta}}^*$ were obtained by simulating the fault in PSCAD first with Model 1 and current limiting in the SynRF and then by implementing the voltage limiting algorithm.

The behaviour of the dq components in Figure 4.21 is caused by the unbalance in

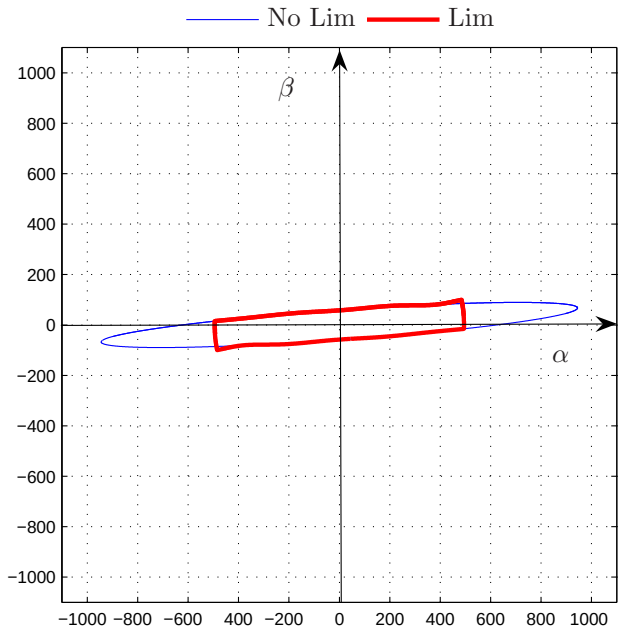


Figure 4.22: Reference inverter bridge voltage v_i^* in $\alpha\beta$ coordinates for a $2\phi g$ fault at point F_3 in a microgrid supplied by a single inverter (control and current limiting in the SynRF): without instantaneous voltage limiting (blue line), with voltage limiting algorithm as in [76] (red line)

the reference inverter bridge voltage. Similarly to equations (4.14) and (4.15), the dq components of v_i^* can be expressed as:

$$v_{id}^* = \sqrt{\frac{3}{2}} V_{i_p} cos(\theta_{i_p}) + \sqrt{\frac{3}{2}} V_{i_n} cos(2\omega t + \theta_{i_n}) \tag{4.38}$$

$$v_{iq}^* = \sqrt{\frac{3}{2}} V_{i_p} sin(\theta_{i_p}) - \sqrt{\frac{3}{2}} V_{i_n} sin(2\omega t + \theta_{i_n}) \tag{4.39}$$

where V_{i_p} and V_{i_n} are the magnitudes of the positive and negative sequence components and θ_{i_p} and θ_{i_n} are the phase angles of the positive and negative sequence components of the reference bridge voltage. Equations (4.38) and (4.39) describe a circle of centre $(\sqrt{\frac{3}{2}} V_{i_p} cos(\theta_{i_p}); \sqrt{\frac{3}{2}} V_{i_p} sin(\theta_{i_p}))$ and radius $\sqrt{\frac{3}{2}} V_{i_n}$, which is the circle in blue in Figure 4.21.

As described in Section 3.2.3, for an unbalanced fault, the trajectory of $\bar{V}_{i_{\alpha\beta}}^*$ is a skewed ellipse. This well compares with the ellipse in Figure 4.22. For the particular fault simulated ($2\phi g$), the vector $\bar{V}_{i_{\alpha\beta}}^*$ goes outside the reference circle of radius $\frac{V_{DC}}{\sqrt{2}}$ and therefore the voltage limiting algorithm acts and brings the voltage within its maximum limit. It is interesting to note that a complete description by vector $\bar{V}_{i_{\alpha\beta}}^*$ around the red

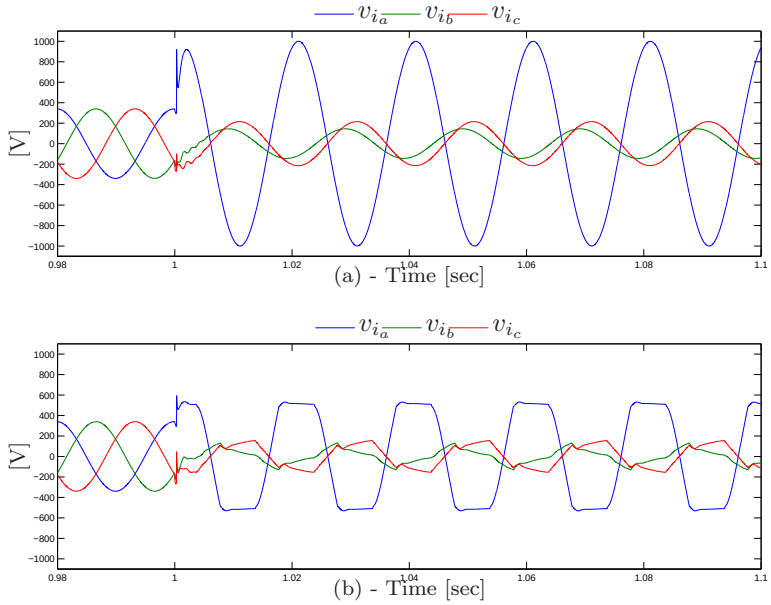


Figure 4.23: Comparison of v_{i_a}, v_{i_b} and v_{i_c} for a $2\phi g$ fault at point F_3 in a microgrid supplied by a single inverter (control and current limiting in the SynRF): (a) Without instantaneous voltage limiting, (b) With voltage limiting algorithm as in [76]

trajectory in Figure 4.22 corresponds to vector $\bar{V}^*_{i_{dq}}$ describing twice the red trajectory in Figure 4.21. This is caused by the double frequency term in (4.38) and (4.39).

Figure 4.23 compares the inverter output phase voltage v_i for the same bolted double phase-to-ground fault without and with voltage limiting. The phase voltage v_{i_a} is now quite reduced and the inverter is capable of reproducing it, however, the waveforms are no longer sinusoidal. Moreover, the limiting algorithm acts similarly to a saturation block, therefore the integral part of the current controller winds-up. In order to avoid this, proportional regulators could be used in the current loop.

The limiting of voltage described so far is concerned with the inverter's capability rather than the network's requirements. For example, in Figure 4.23 the resulting v_{i_a} supplied to the network is greater than the nominal voltage value and would not be acceptable to the network or its customers. So another approach to the limitation of voltage would be to actively limit $v^*_{i_a}$, $v^*_{i_b}$ and $v^*_{i_c}$ with three saturation blocks as shown in Figure 4.24. The limit can be chosen according to the requirements of the network and loads.

Active limiting also uses saturation blocks and so it is better to use proportional

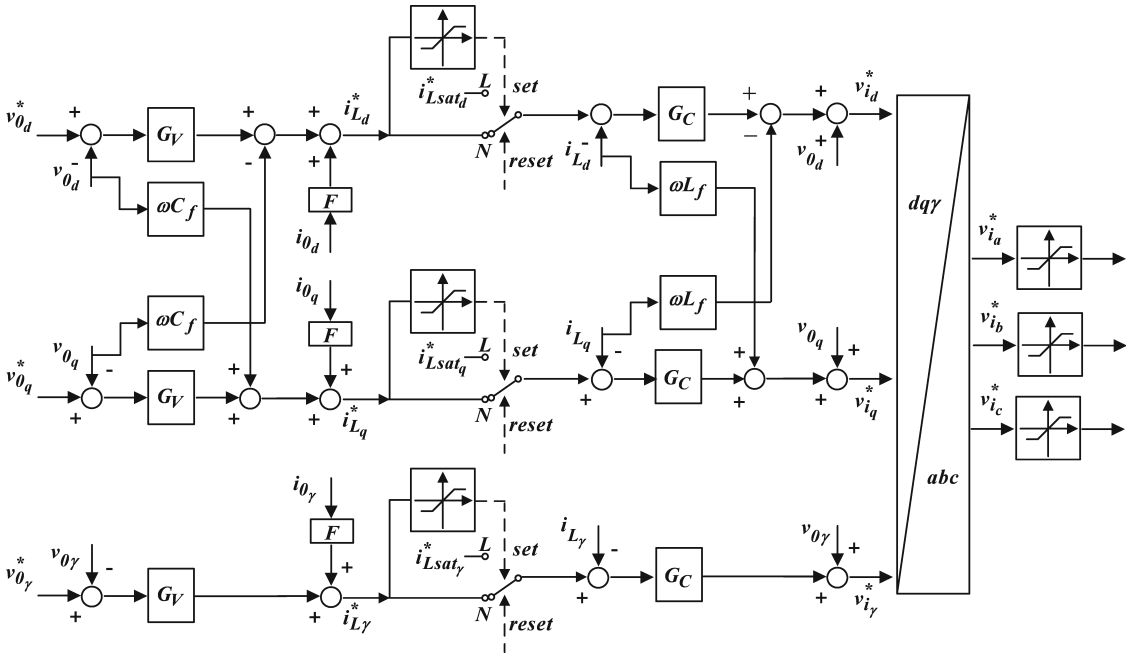


Figure 4.24: SynRF voltage and current control loops with instantaneous per-phase voltage limiting in the NatRF

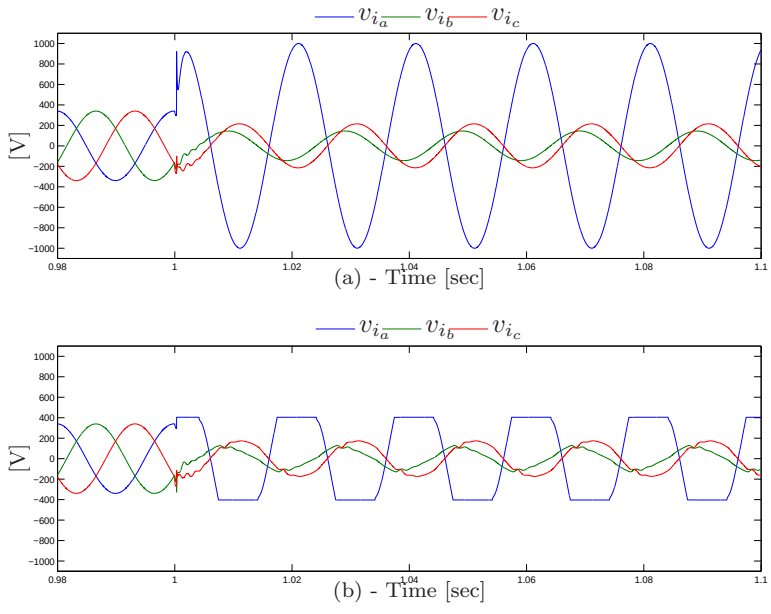


Figure 4.25: Comparison of v_{i_a}, v_{i_b} and v_{i_c} for a $2\phi g$ fault at point F_3 in a microgrid supplied by a single inverter (control and current limiting in the SynRF): (a) Without instantaneous voltage limiting, (b) With instantaneous per-phase voltage limiting

controllers in the current control loops in order to avoid the wind-up phenomenon. Figure 4.25 compares the response for a bolted double phase-to-ground fault without and with voltage limiting on $v_{i_a}^*$, $v_{i_b}^*$ and $v_{i_c}^*$. The response with voltage limiting and proportional controller is rather good and v_{i_a} is limited to a chosen value with little effect on v_{i_b} and v_{i_c}. However, the produced waveforms are distorted.

In order to satisfy both inverter's and network's voltage limits, the limiting on $\bar{V}_{i_{dq}}$ according to the presented algorithm and the limiting on v_{i_a}, v_{i_b} and v_{i_c} can be cascaded one after the other.

4.1.6 Fault response of a microgrid supplied by a single inverter controlled in the SynRF and with current limiting in the NatRF

The purpose of this Section is to illustrate the impact of the other two current limiting strategies (instantaneous and RMS limiting in the NatRF) on the inverter's response in the event of a fault.

Instantaneous current limiting in the NatRF: Case 2

Figures 4.26, 4.27, 4.28 and 4.29 show the response of the microgrid with instantaneous current limiting in the NatRF to the same four faults considered in Section 4.1.5.

As was the case of control and current limiting in the SynRF, the response of the system is very fast, but because the limiting of the inductor phase current i_L is now done on a per-phase base, the response in terms of voltage and current is rather different. A bolted three-phase fault requires instantaneous current limiting in the three phase inductor currents and produces three equal third harmonic phase-to-neutral voltages at the fault point, v_a, v_b and v_c, see Figure 4.26. This is an interesting behaviour considering that a three-phase fault is a balanced fault and should not generate any voltage, let alone third harmonic voltage, at the fault point. However, for this microgrid model, the instantaneous current limiting produces distorted waveforms which include third harmonic components. The sum of the three currents at the fault point, i_a, i_b and i_c, is not zero and the resulting sum current, which flows back through earthing resistances R_g, contains third harmonic. As a result, the phase-to-neutral voltages at fault point, which are equal to the voltage drop across R_g, are equal to a third harmonic voltage.

Figures 4.27, 4.28 and 4.29 show that in the event of an unbalanced fault the faulty phases are current limited while the control of the output voltage is maintained on the

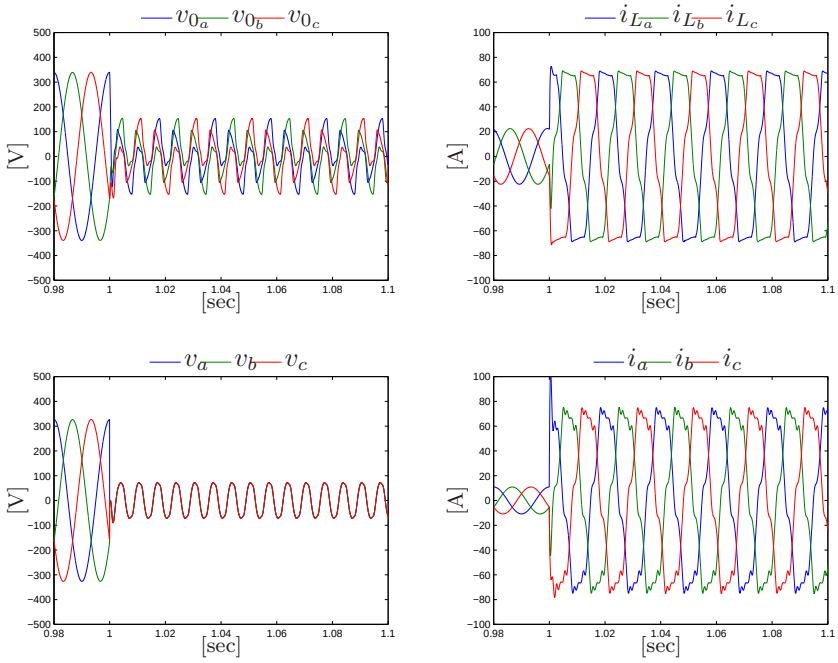


Figure 4.26: Response to a 3ϕ fault at point F_3 of a microgrid supplied by a single inverter (control in the SynRF and instantaneous current limiting in the NatRF)

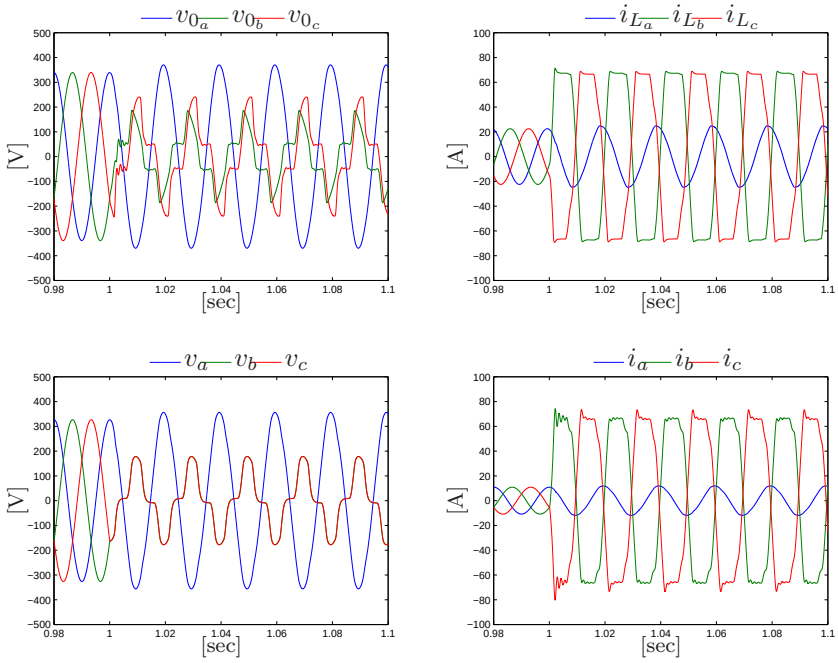


Figure 4.27: Response to a 2ϕ fault at point F_3 of a microgrid supplied by a single inverter (control in the SynRF and instantaneous current limiting in the NatRF)

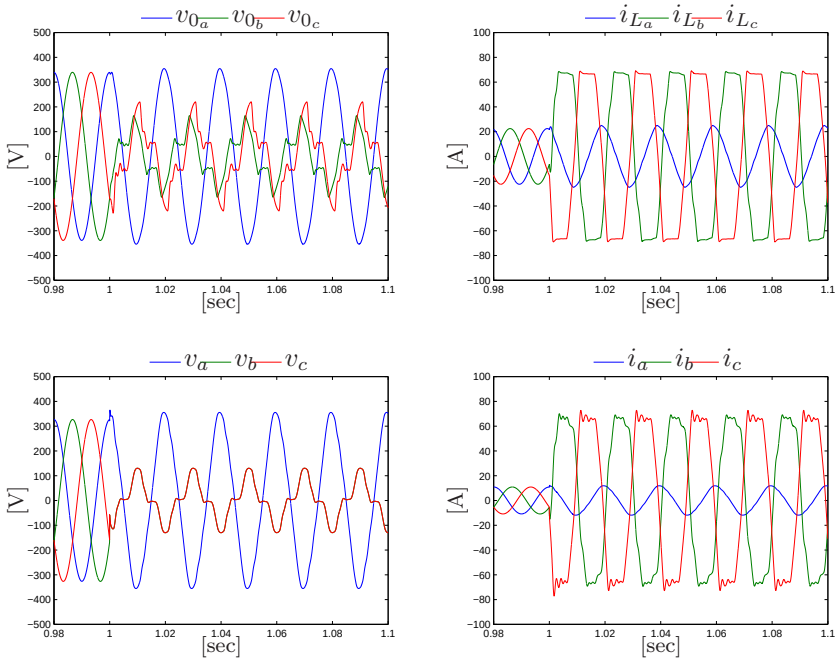


Figure 4.28: Response to a $2\phi g$ fault at point F_3 of a microgrid supplied by a single inverter (control in the SynRF and instantaneous current limiting in the NatRF)

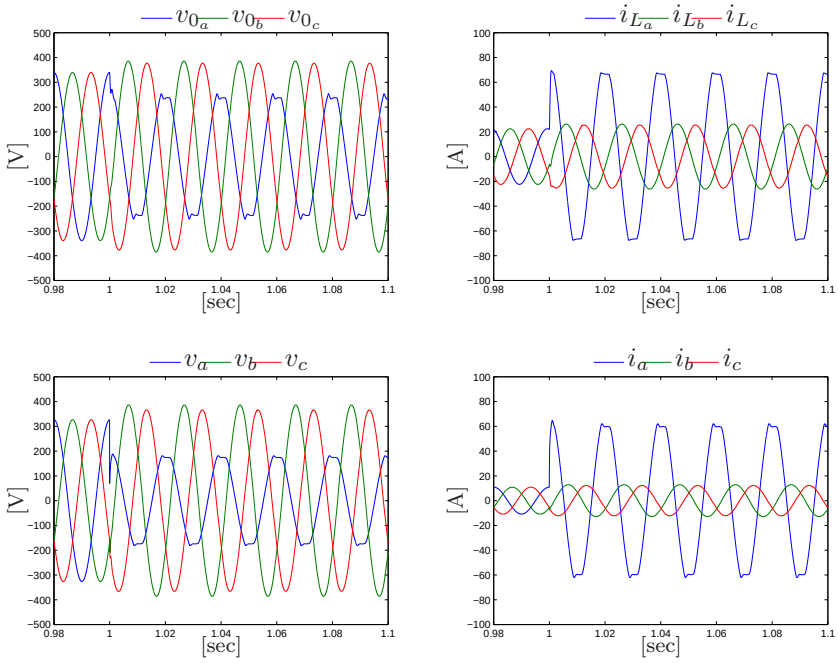


Figure 4.29: Response to a $1\phi g$ fault at point F_3 of a microgrid supplied by a single inverter (control in the SynRF and instantaneous current limiting in the NatRF)

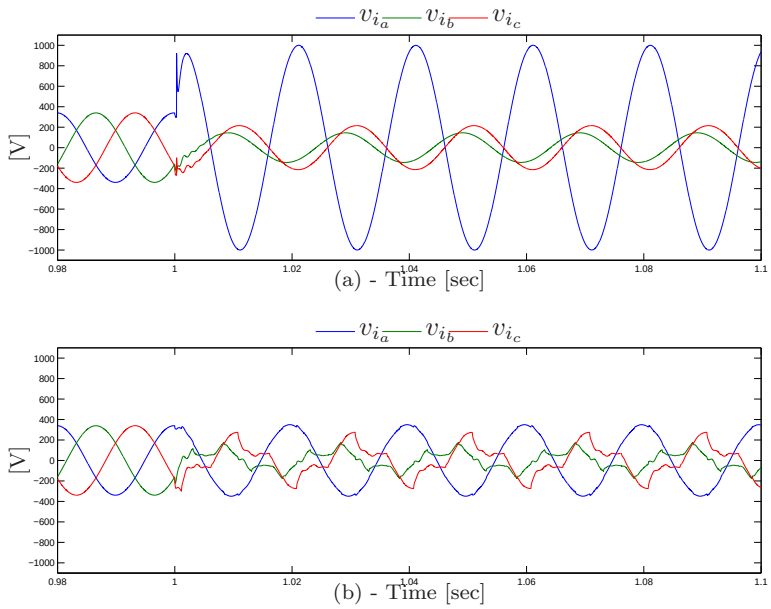


Figure 4.30: Comparison of v_{i_a}, v_{i_b} and v_{i_c} for a $2\phi g$ fault at point F_3 in a microgrid supplied by a single inverter controlled in the SynRF: (a) with current limiting in the SynRF, (b) With instantaneous current limiting in the NatRF

healthy ones. Thus the inverter cannot be viewed simply as three current sources. Compared with responses in Figures 4.18, 4.19 and 4.20 (see Pages 103 and 104), the instantaneous current limiting in the NatRF, which acts on each phase, does not produce big overvoltages and the voltage in the healthy phases does not increase beyond inverter's capabilities. As an example, these two different behaviours can be compared in Figure 4.30 which shows the responses of the inverter to a $2\phi g$ fault with average current limiting in the SynRF and with instantaneous current limiting in the NatRF.

Another positive attribute of instantaneous current limiting is the lack of any switching in the inverter control from the normal multi-loop voltage control state to a current limit state. As a result, no setting or re-setting strategy for the switching between one control to the other has to be designed, as it has to be done for the current limiting in the SynRF, see Figure 4.9, and the RMS current limiting in the NatRF, see Figure 4.11. With instantaneous current limiting in the NatRF, the inverter goes back into normal operation with multi-loop voltage control as soon as the fault is cleared.

On the other hand, instantaneous current limiting in the NatRF presents some problems. The first one is related to the waveform distortion produced by the saturation

blocks. As discussed in Section 4.1.3, at the moment, there is no standard available which specifies what is the permitted level of harmonic distortion in a microgrid in the event of a fault. However it is reasonable to assume that the waveforms in Figures 4.26, 4.27, 4.28 and 4.29 could not be acceptable by the network.

A second problem is connected to the control of voltage in the healthy phases. For an unbalanced fault they do not experience a big rise, however, they are not perfectly controlled either (e.g. see the small increase in v_{0_b} and v_{0_c} in Figure 4.29). This behaviour is a combined effect of the voltage control trying to control the $dq\gamma$ components of the output voltage rather than v_{0_a}, v_{0_b} and v_{0_c} on an individual basis and of the wind-up of the integrators in the PI regulators in the voltage loops.

Finally, the last problem is the computational effort required by instantaneous current limiting in the NatRF. Indeed, inductor reference currents are transformed from the SynRF to the NatRF and back. These two additional transformations would not be needed if the whole inverter control could be implemented in the NatRF.

RMS current limiting in the NatRF: Case 3

Figures 4.31, 4.32, 4.33 and 4.34 show the response of the microgrid with RMS current limiting in the NatRF to a 3ϕ fault, a 2ϕ fault, to a $2\phi g$ fault and a $1\phi g$ fault respectively. Overall, the response is improved compared with both current limiting in the SynRF and instantaneous current limiting in the NatRF. Indeed, RMS current limiting in the NatRF limits the inductor current of each faulted phase to a constant sinusoidal reference current while maintaining the control over voltage on healthy phases. As a result, RMS current limiting does not produce any waveform distortion as the instantaneous current limiting in the NatRF does. Moreover, the overvoltages observed with the limiting in SynRF are avoided and therefore there is no distortion caused by voltage limiting. For example, Figure 4.35 compares the inverter bridge voltage, v_i during a $2\phi g$ fault at F_3 for current limiting in the SynRF and RMS current limiting in the NatRF.

Only one example of overvoltages arises and that is for the voltage of faulty phases in the event of a 2ϕ fault, see Figure 4.32. For a 2ϕ fault, currents $i^*_{L_b}$ and $i^*_{L_c}$ are controlled and kept constant to $i^*_{Lsat_b}$ and $i^*_{Lsat_c}$ which are two currents equal in magnitude but with 120° phase difference. The phase-to-neutral voltages at the fault point, v_b and v_c, are equal and given by the voltage drop across $R_L/2$ caused by the flowing of the sum of i_b

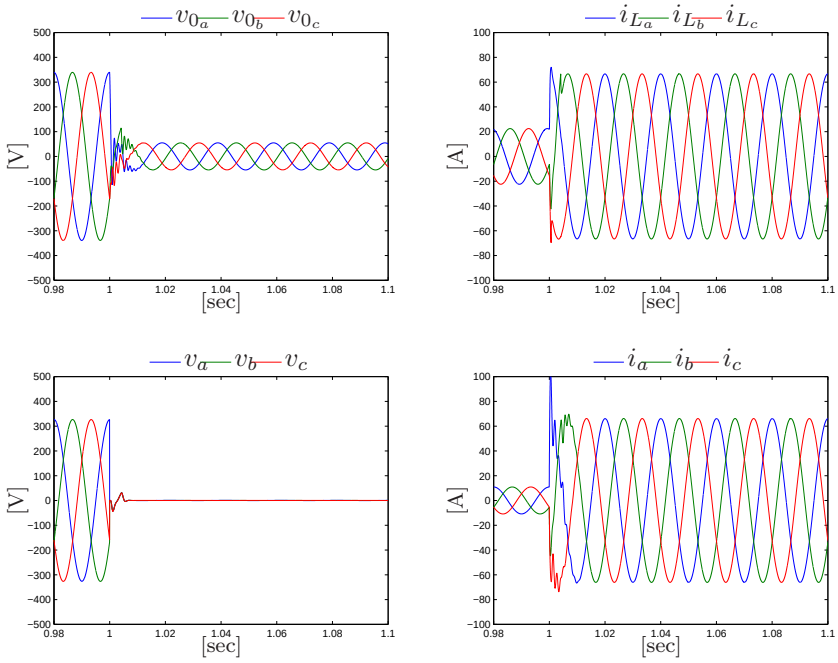


Figure 4.31: Response to a 3ϕ fault at point F_3 of a microgrid supplied by a single inverter (control in the SynRF and RMS current limiting in the NatRF)

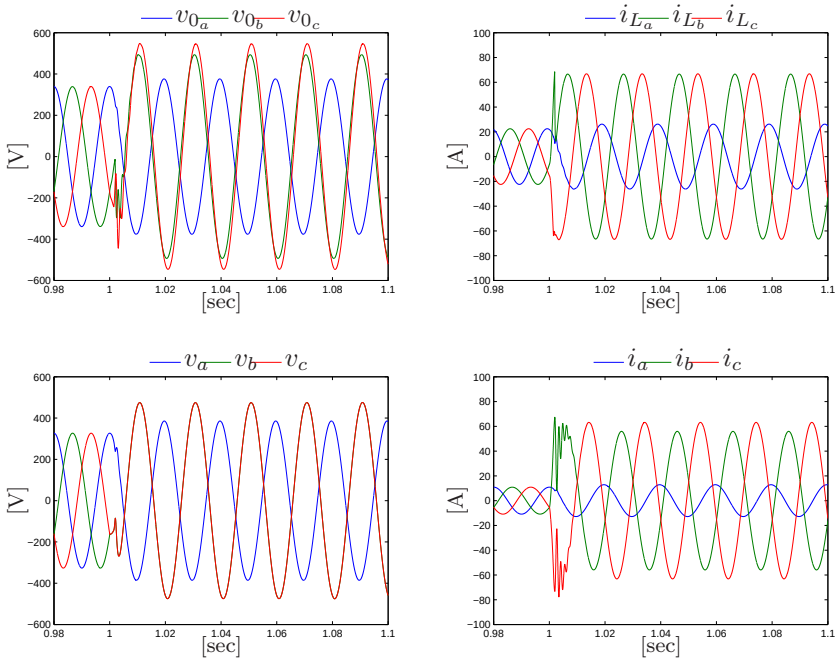


Figure 4.32: Response to a 2ϕ fault at point F_3 of a microgrid supplied by a single inverter (control in the SynRF and RMS current limiting in the NatRF)

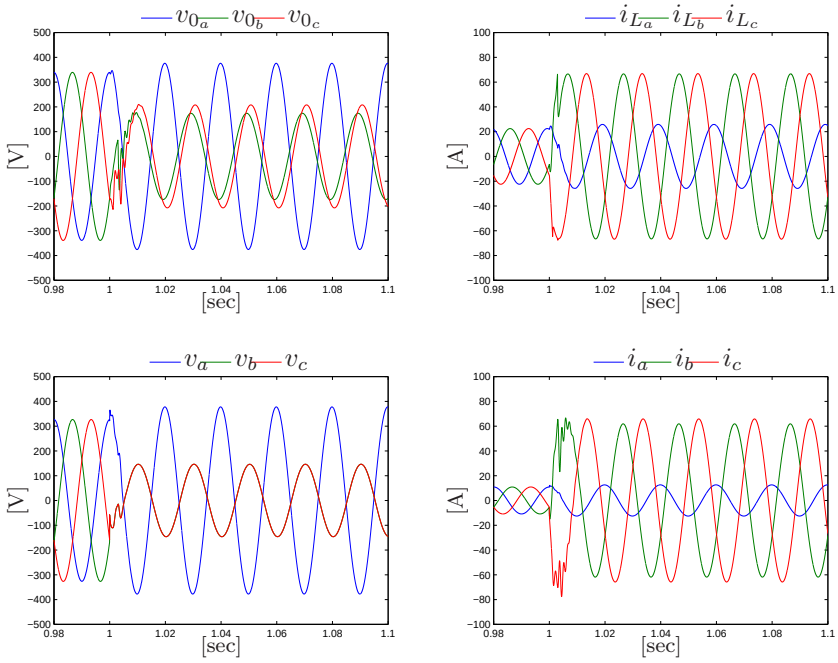


Figure 4.33: Response to a $2\phi g$ fault at point F_3 of a microgrid supplied by a single inverter (control in the SynRF and RMS current limiting in the NatRF)

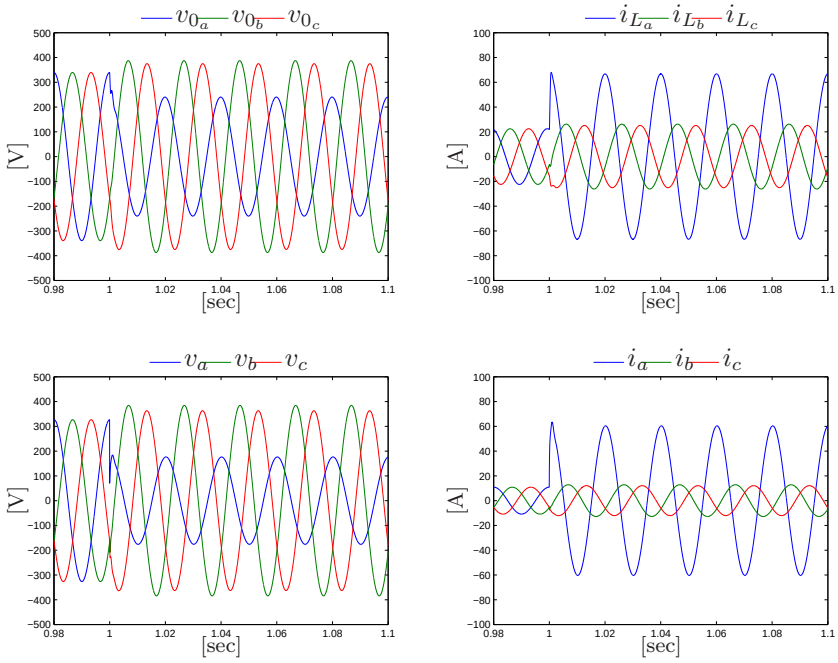


Figure 4.34: Response to a $1\phi g$ fault at point F_3 of a microgrid supplied by a single inverter (control in the SynRF and RMS current limiting in the NatRF

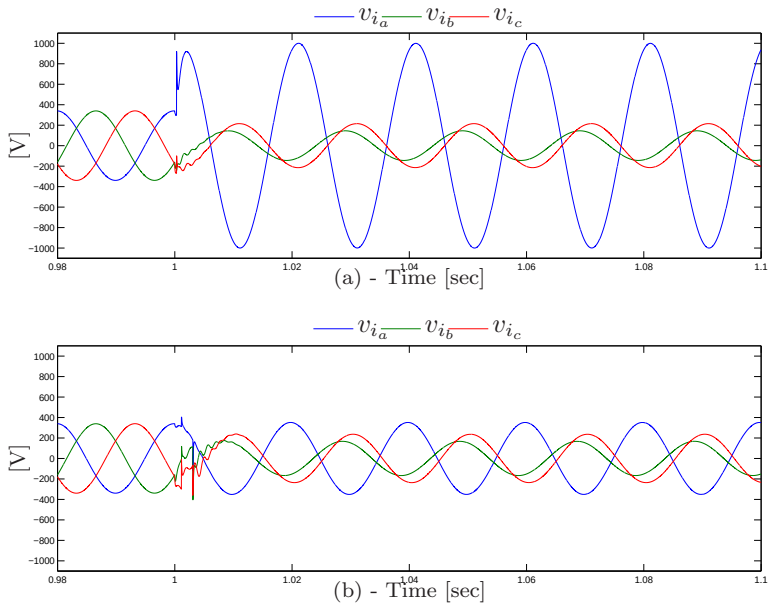


Figure 4.35: Comparison of v_{i_a}, v_{i_b} and v_{i_c} for a $2\phi g$ fault at point F_3 in a microgrid supplied by a single inverter controlled in the SynRF: (a) with current limiting in the SynRF, (b) With RMS current limiting in the NatRF

and i_c. This sum is not small because the two phases are current controlled. It follows that v_b and v_c experience an overvoltage which is then felt all over the microgrid network up to v_{0_b} and v_{0_c}. These values of v_{0_b} and v_{0_c} are outside inverter's voltage rating and therefore voltage limiting as described in Section 4.1.5 will act and produce distorted waveforms. It has to be noted that phase-to-phase faults are not common in distribution networks and therefore the response of the inverter to this type of fault could be tolerated. Alternatively overvoltages could be reduced by reducing the magnitude of the reference currents $i^*_{Lsat_a}$, $i^*_{Lsat_b}$ and $i^*_{Lsat_c}$.

The RMS current limiting in the NatRF is capable of controlling the voltage of the healthy phases however it does not keep it exactly equal to its reference value (e.g. see Figure 4.34). This problem has already been observed and described for instantaneous current limiting in the NatRF. Similarly, also RMS current limiting requires additional reference frame transformations.

Overall, the RMS current limiting in the NatRF shows that it is possible to devise the control strategy which can produce a good fault response of the microgrid in terms of control of overvoltage on the healthy phases and absence of waveform distortion. Ad-

ditional control effort is still needed in order to improve the control of voltage during faults.

4.2 Microgrid supplied by a single inverter controlled in the NatRF

The microgrid model which is going to be now considered in this Section (i.e. Model 2 in Table 4.1) is identical to the one analyzed so far with the difference that now the inverter control is not in the SynRF but in the NatRF (*abc* coordinates). The following paragraphs describe how this type of control works for balanced and unbalanced operation, how current limiting is implemented and then how the microgrid with an inverter controlled in the NatRF responds to different types of fault.

4.2.1 Control of a stand-alone inverter in the NatRF

As for the control in the SynRF, the starting point for the control implementation is to consider the inverter output LC filter, see Figure 3.17. From equations (4.6) and (4.7) the block diagram of the filter in the NatRF can be derived and is shown in Figure 4.36. In the NatRF the filter comprises three models, one for each coordinate, which are coupled (e.g. v_{i_b} appears in phase a and phase c models) because of the presence of the neutral conductor. By considering the filter block diagram, the control system in Figure 3.13 was adapted to the NatRF where it becomes equivalent to three multi-loops, one for each phase. Figure 4.37 shows this multi-loop control in the NatRF.

The implementation in the NatRF does not require any reference frame transformation therefore the output phase voltages v_{0_a}, v_{0_b} and v_{0_c} are directly regulated by three voltage control loops. The reference voltages $v^*_{0_a}$, $v^*_{0_b}$ and $v^*_{0_c}$ are three sinusoidal signals equal to the desired output values. As in the control in the SynRF, output current i_0 and output voltage v_0 feedforward terms are used. Figure 4.37 also shows the de-coupling terms used in order to cancel the coupling effect of the neutral conductor in the LC filter and three saturation blocks placed to limit the phase inductor currents supplied by the inverter.

The control in the NatRF is quite straight forward to understand and implement however it has never been as popular as the one in the SynRF because of its poor control performance with sinusoidal control signals. In the control in the SynRF, simple PI reg-

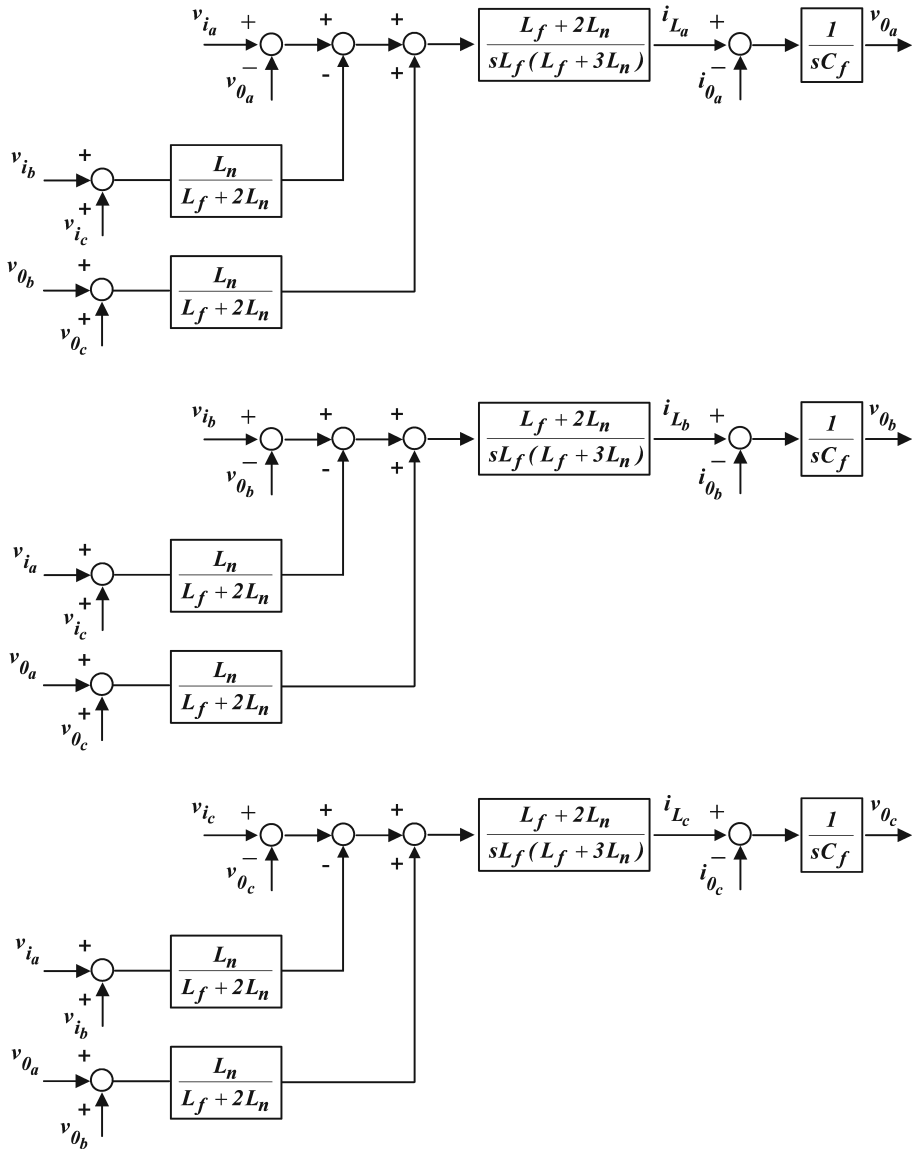


Figure 4.36: Equivalent block diagram in NatRF of the LC filter

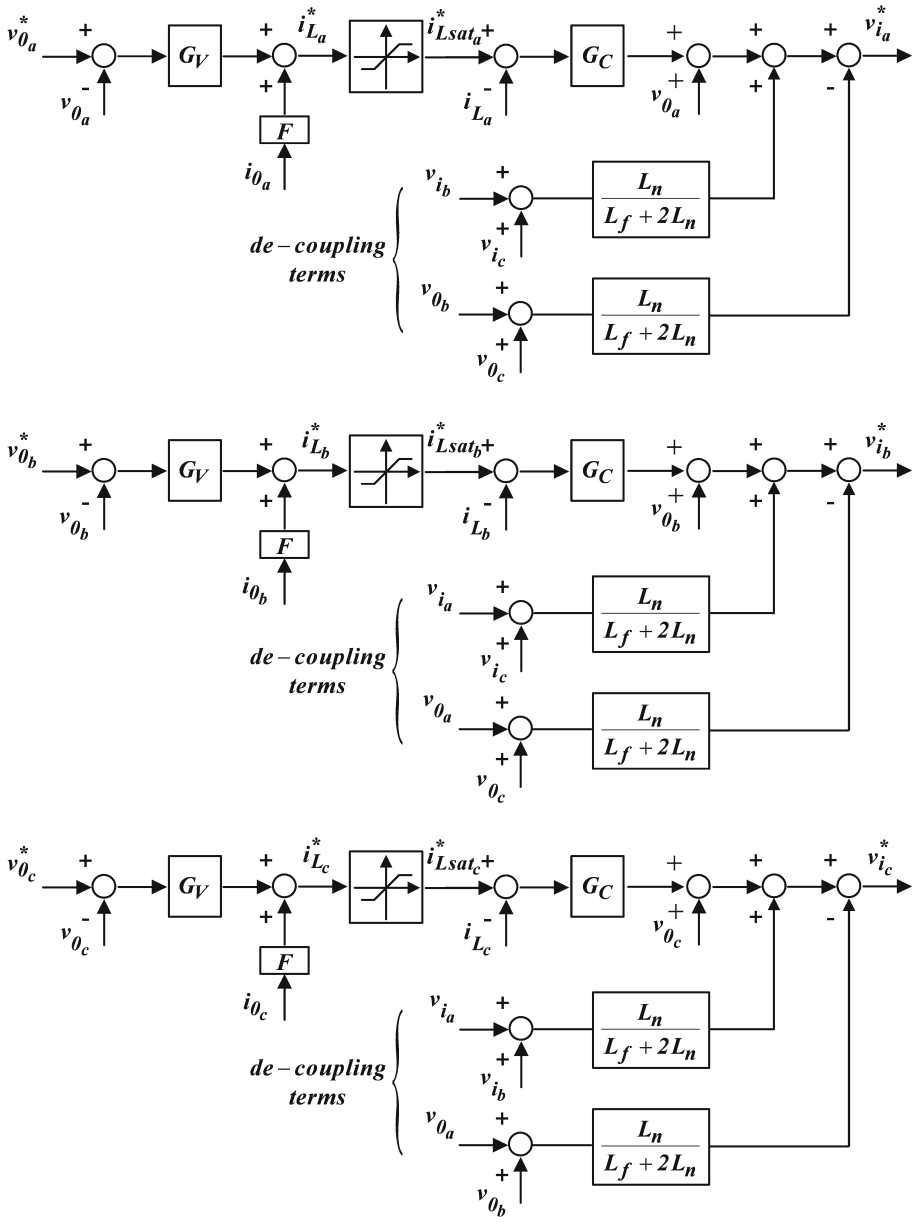


Figure 4.37: Multi-loop control of a stand-alone inverter in the NatRF

ulators are able to achieve zero steady-state error, however, here the same PI regulators cannot achieve that with sinusoidal control signals. This was the general attitude until studies in [72, 77, 78] introduced frequency-domain transformations demonstrating how control systems in SynRF can be transformed in the StatRF and then in the NatRF and in particular how PI regulators in the SynRF become equivalent to P+Resonant controllers in the NatRF. Indeed, as PI regulators are able to achieve zero steady-state error with DC control signals in the SynRF, P+Resonant regulators are able to achieve zero steady-state error with sinusoidal control signals in the NatRF. A full description of these frequency-domain transformations can be found in Appendix B. Following the studies in [72, 77, 78], the control in the NatRF is gaining popularity in the control of stand-alone inverters [79], in the control of grid-connected inverters [80, 81] and in particular where there is the need of good synchronization during unbalanced grid operation [82].

Here, in order to achieve zero steady-state error in the voltage control loop in Figure 4.37, G_V is therefore chosen as a P+Resonant regulator while simple proportional regulators are used in the current loops.

4.2.2 Control in the NatRF and unbalanced operation

In the event of unbalanced operation, the inverter is required to produce a balanced set of output voltages v_{0_a}, v_{0_b} and v_{0_c}. Control in the SynRF with PI regulators used in the first model (see Figure 4.2) is not capable of handling negative sequence components and requires a third control loop to control the zero sequence components. In order to understand how the control in the NatRF with three P+Resonant regulators in the voltage control loops behaves during unbalanced operation and how its performance compares with the one of the first model with PI regulators in the SynRF, frequency-domain transformations are used as in [72, 77, 78].

As previously discussed in Section 4.1.2, one possible solution to the control of negative sequence components in the SynRF is to use a more complex structure like the one in Figure 4.3, which uses the Park and the modified Park transformations. By using the frequency-domain transformation it is possible to transform this control structure from the SynRF to the NatRF.

In general, if the control system is made by one regulator h_{dq}^{+} implemented in the positive SynRF and one regulator h_{dq}^{-} in the negative SynRF, the following two sets of

equations can be written:

$$\begin{bmatrix} y_a^+(t) \\ y_b^+(t) \end{bmatrix} = \sqrt{\frac{3}{2}} \begin{bmatrix} 1 & \frac{1}{\sqrt{3}} \\ 0 & \frac{2}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} cos(\omega_o t) & -sin(\omega_o t) \\ +sin(\omega_o t) & cos(\omega_o t) \end{bmatrix} \left\{ \left[h_{dq}^+(t) \right] * \left\{ \begin{bmatrix} cos(\omega_o t) & +sin(\omega_o t) \\ -sin(\omega_o t) & cos(\omega_o t) \end{bmatrix} \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} x_a(t) \\ x_b(t) \end{bmatrix} \right\} \right\} \tag{4.40}$$

$$\begin{bmatrix} y_a^-(t) \\ y_b^-(t) \end{bmatrix} = \sqrt{\frac{3}{2}} \begin{bmatrix} 1 & \frac{1}{\sqrt{3}} \\ 0 & \frac{2}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} cos(\omega_o t) & sin(\omega_o t) \\ -sin(\omega_o t) & cos(\omega_o t) \end{bmatrix} \left\{ \left[h_{dq}^-(t) \right] * \left\{ \begin{bmatrix} cos(\omega_o t) & -sin(\omega_o t) \\ +sin(\omega_o t) & cos(\omega_o t) \end{bmatrix} \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} x_a(t) \\ x_b(t) \end{bmatrix} \right\} \right\} \tag{4.41}$$

where $x_a(t)$ and $x_b(t)$ are the measured input variables and $y_a(t)$ and $y_b(t)$ are the controlled variables. The first set is relative to the positive sequence controller while the second one is relative to the negative sequence synchronous frame controller. Following the methodology in [77], the two controllers can be expressed in the StatRF as:

$$\begin{bmatrix} Y_\alpha^+(s) \\ Y_\beta^+(s) \end{bmatrix} = \begin{bmatrix} H_{dq}^+(s+j\omega_o) & -jH_{dq}^+(s+j\omega_o) \\ +H_{dq}^+(s-j\omega_o) & jH_{dq}^+(s-j\omega_o) \\ jH_{dq}^+(s+j\omega_o) & (H_{dq}^+(s+j\omega_o) \\ -jH_{dq}^+(s-j\omega_o) & +H_{dq}^+(s-j\omega_o) \end{bmatrix} \begin{bmatrix} X_\alpha(s) \\ X_\beta(s) \end{bmatrix} \tag{4.42}$$

$$\begin{bmatrix} Y_\alpha^-(s) \\ Y_\beta^-(s) \end{bmatrix} = \begin{bmatrix} H_{dq}^-(s+j\omega_o) & jH_{dq}^-(s+j\omega_o) \\ +H_{dq}^-(s-j\omega_o) & -jH_{dq}^-(s-j\omega_o) \\ -jH_{dq}^-(s+j\omega_o) & (H_{dq}^-(s+j\omega_o) \\ jH_{dq}^-(s-j\omega_o) & +H_{dq}^-(s-j\omega_o) \end{bmatrix} \begin{bmatrix} X_\alpha(s) \\ X_\beta(s) \end{bmatrix} \tag{4.43}$$

As can be seen, in the StatRF, the difference between a positive SynRF regulator and a negative sequence one lies in sign of the cross-coupling terms. In Figure 4.3 only the integral part of the controller is implemented separately in the two reference frames, therefore, the equivalent two regulators in stationary reference frame are given by:

$$H_{\alpha\beta}^+(s) = \begin{bmatrix} \frac{K_i s}{s^2+\omega_o^2} & -\frac{K_i \omega_o}{s^2+\omega_o^2} \\ \frac{K_i \omega_o}{s^2+\omega_o^2} & \frac{K_i s}{s^2+\omega_o^2} \end{bmatrix} \tag{4.44}$$

$$H_{\alpha\beta}^-(s) = \begin{bmatrix} \frac{K_i s}{s^2+\omega_o^2} & \frac{K_i \omega_o}{s^2+\omega_o^2} \\ -\frac{K_i \omega_o}{s^2+\omega_o^2} & \frac{K_i s}{s^2+\omega_o^2} \end{bmatrix} \tag{4.45}$$

In the original control system in Figure 4.3 the outputs from the positive and negative sequence controllers are summed together with the output from the proportional controller. Therefore the final equivalent StatRF controller is given by:

$$H_{\alpha\beta}(s) = \begin{bmatrix} K_p + \frac{2K_i s}{s^2+\omega_o^2} & 0 \\ 0 & K_p + \frac{2K_i s}{s^2+\omega_o^2} \end{bmatrix} \tag{4.46}$$

The P+Resonant controller $K_p + \frac{2K_i s}{s^2+\omega_o^2}$ has an infinite gain at both positive and negative frequency and therefore can achieve zero steady-state error for both positive and negative sequence regulation. Finally, the stationary frame controller can be further transformed into the natural reference frame as follows:

$$H_{ab}(s) = \begin{bmatrix} 1 & \frac{1}{\sqrt{3}} \\ 0 & \frac{2}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} K_p + \frac{2K_i s}{s^2+\omega_o^2} & 0 \\ 0 & K_p + \frac{2K_i s}{s^2+\omega_o^2} \end{bmatrix} \begin{bmatrix} 1 & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} \end{bmatrix} \tag{4.47}$$

The system in (4.47) is the equivalent in the NatRF of the control system in Figure 4.3.

In a four-wire system, a zero sequence regulator is included as well. Appendix B shows how it is possible to transform the control system for a four-wire inverter from the SynRF to the NatRF. If a P+Resonant controller is included as well in the γ control loop, then the equivalent controller matrix in the NatRF of the control system in Figure 4.3 is given by:

$$H_{abc}(s) = \begin{bmatrix} K_p + \frac{2K_i s}{s^2+\omega_o^2} & 0 & 0 \\ 0 & K_p + \frac{2K_i s}{s^2+\omega_o^2} & 0 \\ 0 & 0 & K_p + \frac{2K_i s}{s^2+\omega_o^2} \end{bmatrix} \tag{4.48}$$

The controller matrix in (4.48) corresponds to three P+Resonant controllers, one for each coordinate, which is exactly what it is used in the voltage control loops in Figure 4.37. Therefore, using three P+resonant regulators in the NatRF, yields a control scheme which is able to handle negative [67] and zero sequence component [58]. As a result, the performance during unbalanced operation of the control system in the NatRF with P+Resonant regulators is better than PI regulators in the positive SynRF only, see Figure 4.2.

4.2.3 Control in the NatRF and current limiting

The current limiting strategies which are going to be considered and implemented in the inverter control in the NatRF are:

- instantaneous current limiting in the NatRF (Case 4 in Table 4.1);
- RMS current limiting in the NatRF (Case 5 in Table 4.1).

The discussion in Section 4.1.3 and the system description in Section 4.1.4 have shown that current limiting in the NatRF is much easier to implement than current limiting in the SynRF. In an inverter controlled in the NatRF, the instantaneous current limiting in the NatRF is implemented as shown in Figure 4.37. Here, the phase inductor reference

currents $i^*_{L_a}$, $i^*_{L_b}$ and $i^*_{L_c}$ are individually limited by three saturation blocks containing upper and lower hard limits. The method is identical to the one described for the inverter controlled in the SynRF, see Figure 4.10, however now no additional reference frame transformations are needed as the whole control is implemented in the NatRF.

Figure 4.38 shows the RMS current limiting in the NatRF applied to the inverter control in the NatRF. Once again, this limiting strategy is identical to the one implemented in the control in the SynRF, see Figure 4.11, with the difference that no additional reference frame transformations are required.

4.2.4 System description: Model 2

The microgrid model considered here is identical to the microgrid model analyzed in Section 4.1. Therefore all the network and inverter data needed to build Model 2 in PSCAD can be found in Section 4.1.4. The only difference between the two models lies in the reference frame implementation of the multi-loop control of the inverter. In particular for the inverter control in the NatRF, three P+Resonant regulators are used in the voltage control loops while three P regulators are chosen for the current control loops. For each P+Resonant regulator, the resonant frequency, ω, is the system frequency (50 Hz) and the gains are chosen in order to have a bandwidth around 400 Hz. Each proportional regulator in the current control loop is chosen to give a bandwidth around 1600 Hz.

The design of instantaneous and RMS current limiting in the NatRF follow the same procedure described in Section 4.1.4. Therefore for instantaneous current limiting (see Figure 4.37), the hard limits inside the saturation blocks are equal to $\pm$47.07 A. For the RMS current limiting (see Figure 4.38), the hard limits in the saturation blocks are again equal to $\pm$47.07 A and $i^*_{Lsat_a}$, $i^*_{Lsat_b}$ and $i^*_{Lsat_c}$ are set equal to a balanced positive sequence set of currents with 47.07 A magnitude and phases determined by the inverter internal frequency reference.

4.2.5 Fault response of a microgrid supplied by a single inverter controlled in the NatRF and with current limiting in the NatRF

The purpose of this section is to describe and discuss the fault response of a microgrid supplied by an inverter controlled in the NatRF and with the two different current limiting strategies.

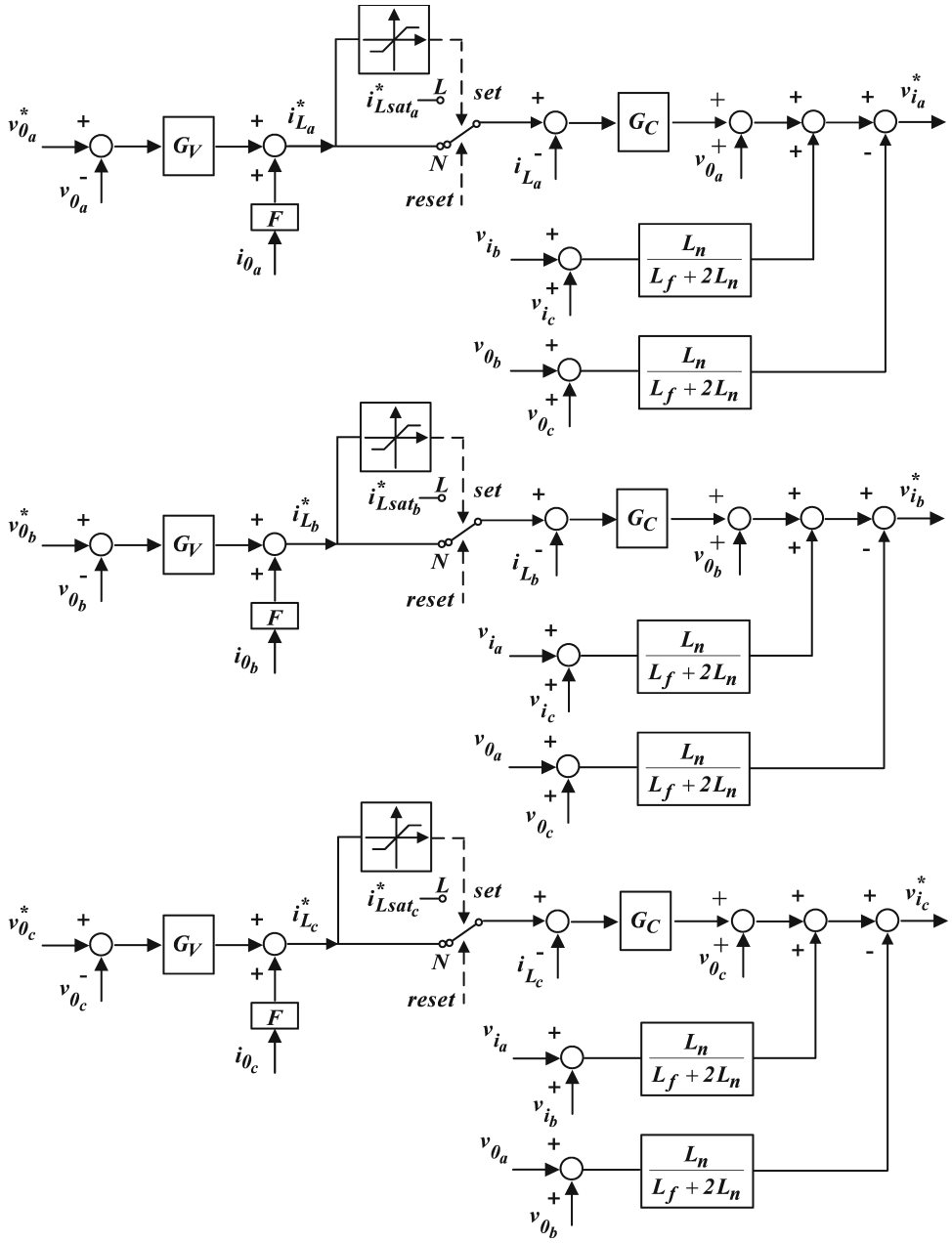


Figure 4.38: NatRF (*abc* coordinates) voltage and current control loops with RMS current limiting in the NatRF

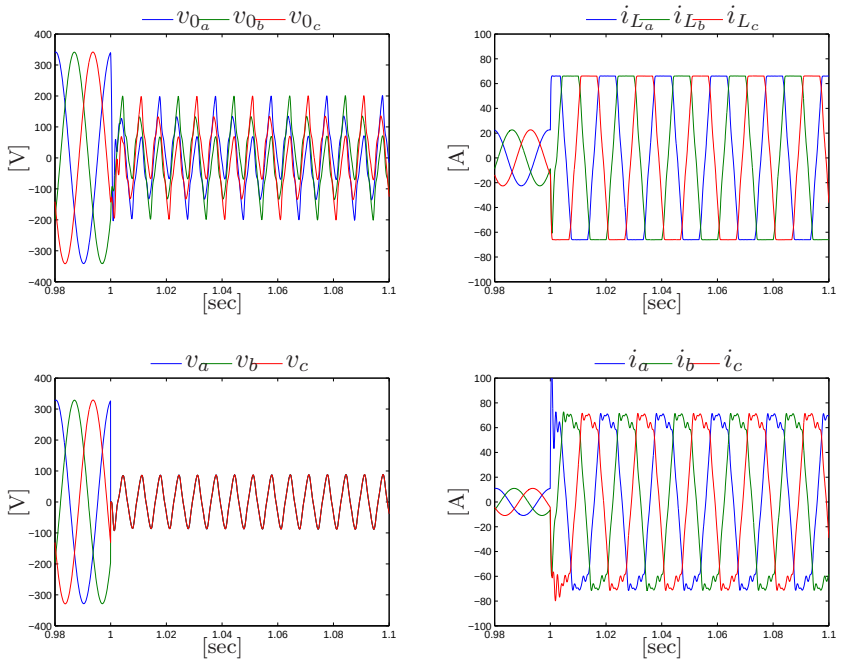


Figure 4.39: Response to a 3ϕ fault at point F_3 of a microgrid supplied by a single inverter (control in the NatRF and instantaneous current limiting in the NatRF)

Instantaneous current limiting in the NatRF: Case 4

Figures 4.39, 4.40, 4.41 and 4.42 show the response of the microgrid to a 3ϕ fault, a 2ϕ fault, a $2\phi g$ fault and a $1\phi g$ fault applied at point F_3 at time t=1s. As for the control in the SynRF, the first thing to be noticed is the high speed of the response of the inverter in the event of a fault compared to the response of synchronous machines. This is caused by the high bandwidth of the control loops which dominate the dynamic response of the inverter and the microgrid network.

For a three-phase fault, the phase inductor currents are instantaneously limited and the resultant distorted waveforms contain third harmonic component. As explained for Figure 4.26 (see Page 111), the third harmonic current is responsible for the voltages v_a, v_b and v_c at fault point, see Figure 4.39. It is interesting to note that the use of reference frame transformations and the control in the SynRF are capable of "smoothing" the current and voltage wave shapes compared with the control and instantaneous current limiting in the NatRF which limits i_{L_a}, i_{L_b} and i_{L_c} very neatly and produces a higher harmonic content. Similarly for a 2ϕ fault (see Figure 4.40) and a $2\phi g$ fault (see Figure 4.41) the

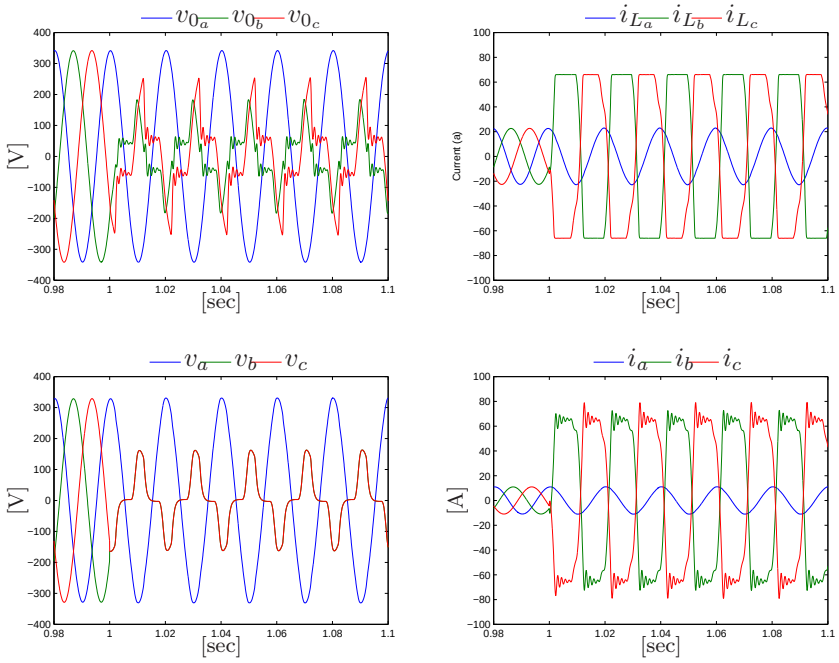


Figure 4.40: Response to a 2ϕ fault at point F_3 of a microgrid supplied by a single inverter (control in the NatRF and instantaneous current limiting in the NatRF)

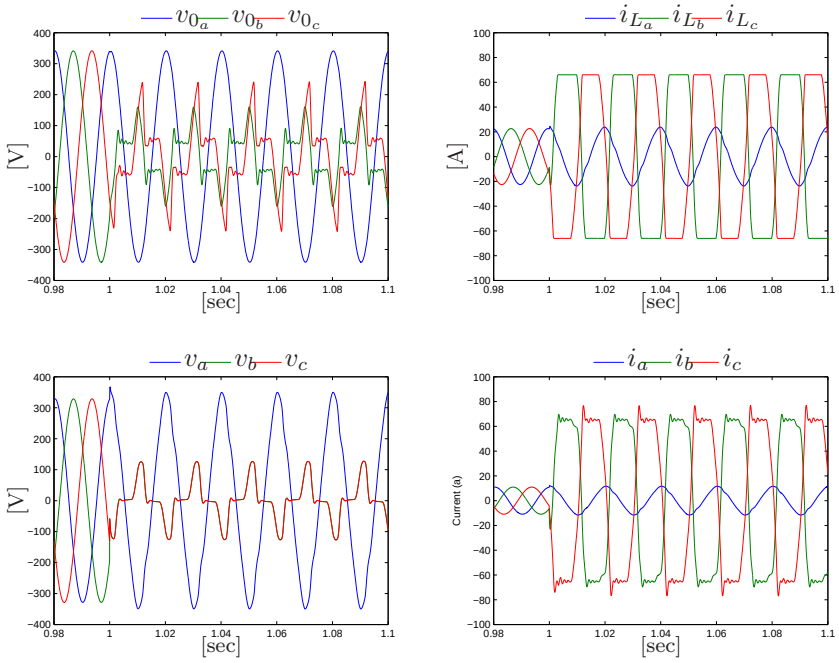


Figure 4.41: Response to a $2\phi g$ fault at point F_3 of a microgrid supplied by a single inverter (control in the NatRF and instantaneous current limiting in the NatRF)

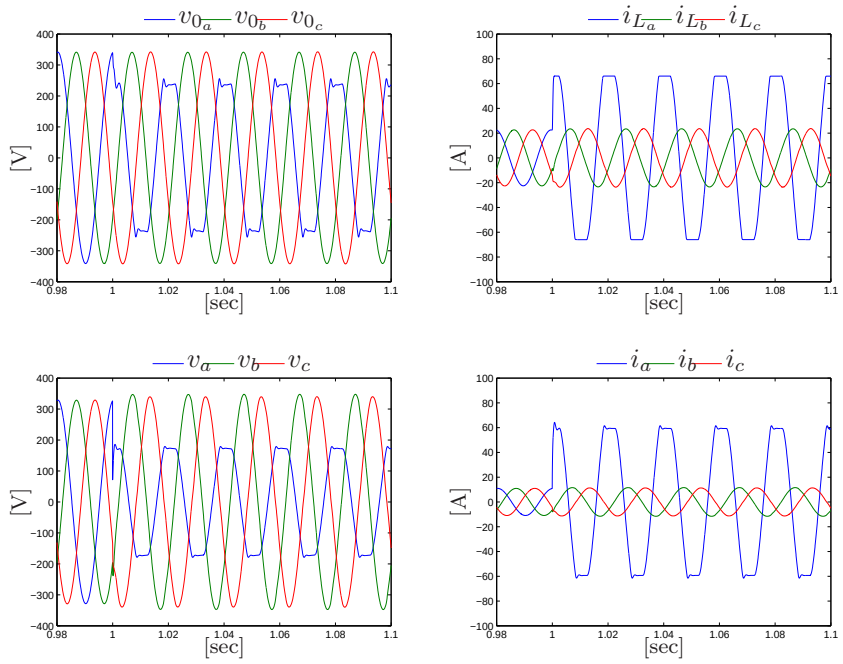


Figure 4.42: Response to a $1\phi g$ fault at point F_3 of a microgrid supplied by a single inverter (control in the NatRF and instantaneous current limiting in the NatRF)

control in the NatRF is not capable of controlling the harmonic content in the produced waveforms compared with the control in the SynRF (see Figures 4.27 and 4.28 on Pages 111 and 112).

During unbalanced faults, the de-coupled control of the inverter output voltages v_{0_a}, v_{0_b} and v_{0_c} and the current limiting applied to each individual inductor phase current make it possible to control phases independently in the event of a fault. This brings two major benefits to the fault response of the inverter. First, the current limiting on individual phase currents avoids overvoltages on healthy phases which were experienced with current limiting in the SynRF. So for example, for a $1\phi g$ fault, see Figure 4.42 the current is only limited in phase a while v_{0_b} and v_{0_c} do not experience any voltage rise. For the same type of fault but with current limiting in the SynRF, see Figure 4.20 on Page 104, v_{0_b} and v_{0_c} would rise well above the inverter voltage capabilities and would then need to be limited as described in Section 4.1.5.

Second, the de-coupled control of v_{0_a}, v_{0_b} and v_{0_c} is capable of keeping the output voltage of each healthy phase equal to its reference value. Considering again the response in Figure 4.42, after the fault is applied, v_{0_b} and v_{0_c} are still kept equal to their pre-fault

values and do not experience little deviations from their pre-fault values as it was observed for instantaneous current limiting in the NatRF applied to the control in the SynRF, see Figure 4.29 on Page 112. Healthy inverter output voltages are also not affected for 2ϕ and $2\phi g$ faults, see Figures 4.40 and 4.41. This behaviour could be advantageous when the number of disrupted single phase customers has to be kept to a minimum.

The implementation of the control and instantaneous current limiting in the NatRF is straight forward compared to the other methods discussed so far, does not need any reference frame transformation and does not need any switching strategy from voltage control to current control in the event of a fault and after a fault. On the other hand, it introduces distorted waveforms into the network.

RMS current limiting in the NatRF: case 5

Figures 4.43, 4.44, 4.45 and 4.46 show results for similar faults but with RMS current limit. This type of current limiting brings the same advantages, in terms of fault response, observed in the previous Case 4 with the additional advantage of not producing any distorted waveform. The de-coupled control limits the current only in the faulty phases while controlling the voltage in the healthy ones. The only voltage which goes above the inverter voltage limits is the one experienced by faulty phases b and c for a 2ϕ fault (see Figure 4.44). This overvoltage would be limited by the inverter voltage limiting, thus producing distorted waveforms. Alternatively the amount of current supplied by the inverter could be limited to less than twice the inverter nominal current. A similar behaviour was observed and discussed while describing the response to the same fault in a microgrid controlled in the SynRF with RMS current limiting (see Figure 4.32 on Page 115).

In contrast to instantaneous current limiting, the RMS current limiting in the NatRF requires a fault-mode re-setting strategy, see Figure 4.38, in order to bring the inverter back to normal operation after the fault is cleared.

4.3 Comparison of the different fault responses in an islanded microgrid supplied by a single inverter

Sections 4.1 and 4.2 have described two popular control strategies for stand-alone inverters (control in the SynRF and control in the NatRF) and have then illustrated the responses

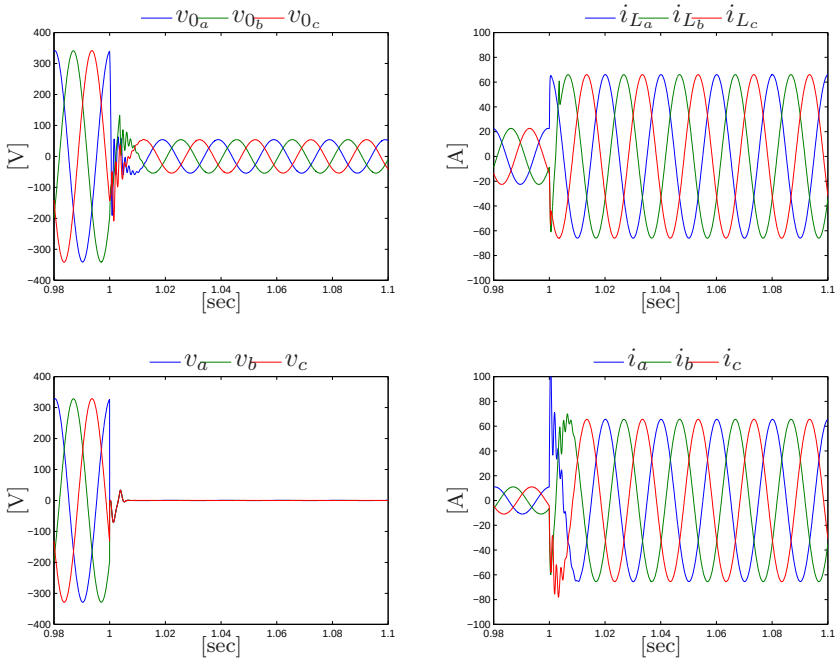


Figure 4.43: Response to a 3ϕ fault at point F_3 of a microgrid supplied by a single inverter (control in the NatRF and RMS current limiting in the NatRF)

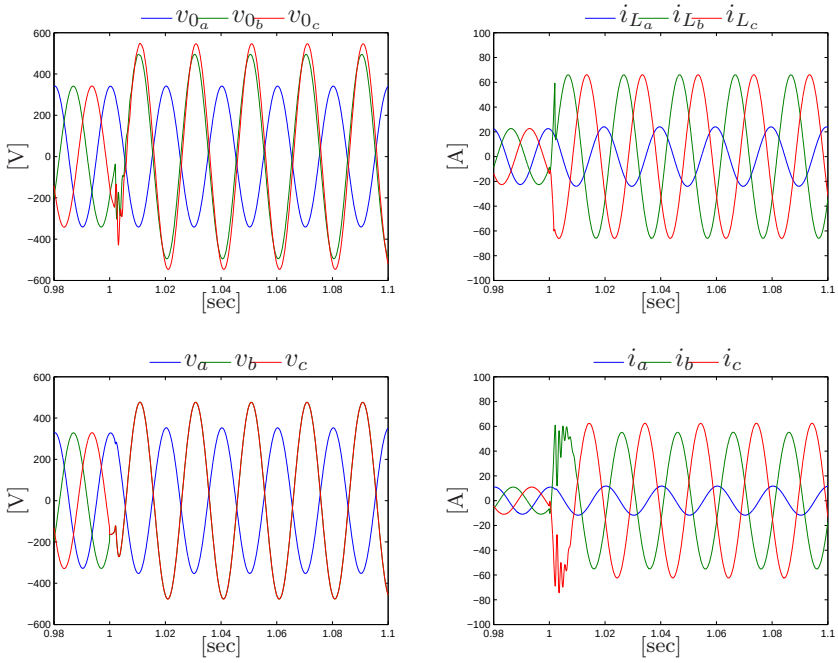


Figure 4.44: Response to a 2ϕ fault at point F_3 of a microgrid supplied by a single inverter (control in the NatRF and RMS current limiting in the NatRF)

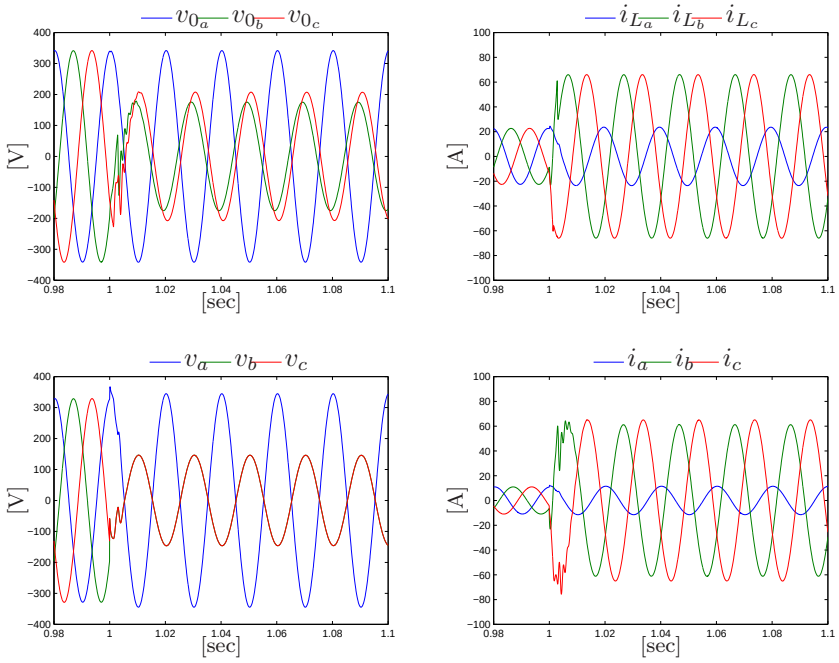


Figure 4.45: Response to a $2\phi g$ fault at point F_3 of a microgrid supplied by a single inverter (control in the NatRF and RMS current limiting in the NatRF)

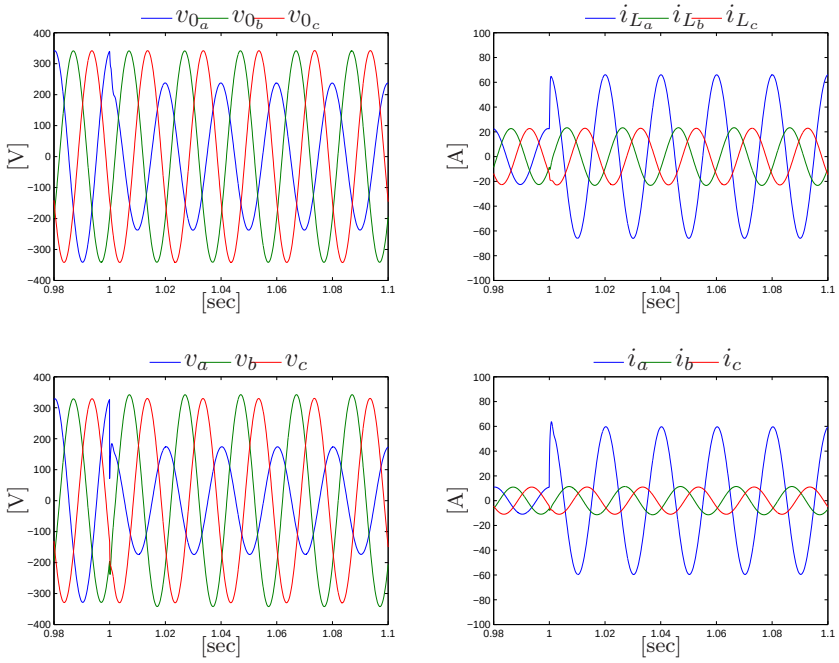


Figure 4.46: Response to a $1\phi g$ fault at point F_3 of a microgrid supplied by a single inverter (control in the NatRF and RMS current limiting in the NatRF)

of microgrids supplied by a single inverter with these two control strategies to various types of fault. While describing and analyzing these responses, the focus has been placed on the limitations of the inverter (i.e. current and voltage ratings), on the requirements of the microgrid network (i.e. waveform distortion and possibility of supplying customers during faults) and on the general level of difficulty in implementing the different controls. It was found that the control strategies behave in completely different ways.

The control in the SynRF with current limiting in the SynRF resulted in implementation difficulties and gave a very bad response for unbalanced faults. Under control in the SynRF, the overall magnitude and phase of the inverter output voltage and inductor current are controlled. As a result, the current limiting in the SynRF results in the current being limited in all three phases and the inverter becoming equivalent to a current source. This current limiting is not easy to implement because of the behaviour of the control in the SynRF during unbalanced operation. Additional difficulties are caused by the presence of saturation blocks in the control loops which requires the use of techniques to avoid the windup of the integral part of the PI controller in the voltage loop. Moreover, even the design of the limits on $i^*_{Lsat_d}$, $i^*_{Lsat_q}$ and $i^*_{Lsat_\gamma}$ is not unique and requires a series of choices as Section 4.1.4 has described.

Simulations showed that the control and current limiting in the SynRF do not give a good response in terms of output voltage. The overvoltages in Figures 4.18, 4.19 and 4.20 (see Pages 103 and 104) cannot be generated by the inverter because of the limitations imposed by the DC link bus voltage. A voltage limiting technique within the inverter has to be implemented which then produces distorted waveforms. As pointed out in Section 4.1.3, currently there are no standards which regulate the response of inverters in the event of a fault, however it can be assumed that the generation of distorted waveforms for all types of unbalanced faults cannot be tolerated by the microgrid network.

The implementation of instantaneous and RMS current limiting in the NatRF inside the inverter SynRF control resulted in completely different fault responses. In particular, the current limiting on individual phase currents limits the overvoltages on healthy phases and makes it possible, to a certain extent, to control of the voltage on these phases. However implementing these two strategies requires extra transformations.

Recent academic studies have demonstrated that the inverter control in the NatRF can give a very good response during balanced and unbalanced operation [79–82]. The

study presented in this Chapter showed that the fault response with control in the NatRF is better than the one with control in the SynRF. Overall, the de-coupled control in the NatRF is able to control the healthy inverter output phase voltages while limiting the current in faulty phases. Moreover, the implementation of the control and current limiting does not require any additional reference frame transformation compared with the previous cases.

The two current limiting strategies in the NatRF have both positive and negative points. The instantaneous current limiting does not need any mode re-setting strategy and does not produce any overvoltages. On the negative side, it produces distorted waveforms. The RMS current limiting produces clean sinusoidal waveforms but then requires some mode re-setting strategy and then it can produce overvoltages for a 2ϕ fault, which have to be limited by the inverter.

Based on these observations, the control in the NatRF is preferable to that in the SynRF for inverter operation during a fault and RMS current limiting is preferred over instantaneous current limiting. Inverter control in the NatRF with RMS current limiting in the NatRF will be adopted in the next Section 4.4.1 where two parallel-connected inverters are considered.

4.4 Microgrid supplied by two parallel-connected inverters

4.4.1 Control of two parallel-connected inverters

The purpose of considering a microgrid supplied by two inverters is to analyze the impact of multiple inverters on the fault behaviour of the microgrid. The model which is considered here (i.e. Model 3 in Table 4.1) is shown in Figure 3.20. The two inverters are identical and are interconnected through an impedance $Z_l = R_l + j\omega L_l$. As described in Section 3.2.2, the difference between the control of parallel inverters and the control of a stand-alone inverter is in the third outer loop, the droop loop, which regulates the reference voltage $v_{0_d}^*$ and frequency ω^* for the multi-loop control structure in Figure 3.13. As a result, each inverter in Figure 3.20 is controlled by a three-loop control structure. The voltage and control loops are chosen to be implemented in the NatRF for the reasons discussed in Section 4.3.

4.4.2 Droop control and unbalanced operation

As the fault response of a microgrid with two parallel inverters is going to be simulated and analyzed, it is important to understand the impact of unbalanced operation on the droop loops. From the droop control scheme in Figure 3.16, it can be seen that the operation of the droop loop is going to be affected by unbalanced load operation through the use of instantaneous active and reactive powers determined with equations (3.4) and (3.5). In particular, during unbalanced operation, the resulting voltages and currents in the SynRF contain a 2ω ripple together with the DC component (see Appendix A). As a result, the inverter output voltage v_0 and current i_0 can be expressed as:

$$\begin{aligned} v_{0_d} &= \sqrt{\frac{3}{2}}V_{0_p}cos(\theta_{v_p}) + \sqrt{\frac{3}{2}}V_{0_n}cos(2\omega t + \theta_{v_n}) \\ v_{0_q} &= \sqrt{\frac{3}{2}}V_{0_p}sin(\theta_{v_p}) - \sqrt{\frac{3}{2}}V_{0_n}sin(2\omega t + \theta_{v_n}) \\ i_{0_d} &= \sqrt{\frac{3}{2}}I_{0_p}cos(\theta_{0_p}) + \sqrt{\frac{3}{2}}I_{0_n}cos(2\omega t + \theta_{0_n}) \\ i_{0_q} &= \sqrt{\frac{3}{2}}I_{0_p}sin(\theta_{0_p}) - \sqrt{\frac{3}{2}}I_{0_n}sin(2\omega t + \theta_{0_n}) \end{aligned} \tag{4.49}$$

In Sections 4.1.2 and 4.2.2 it has been described how the controls in the SynRF and in the NatRF respond to unbalanced operation. The NatRF control with P+Resonant gives a better response therefore v_{0_d} and v_{0_q} should not have any negative sequence component or at worst a very small one. Nevertheless to keep the discussion general, here it is assumed that both V_{0_p} and V_{0_n} are present.

Using equations (3.4) and (3.5), the instantaneous active and reactive power can be calculated as:

$$\begin{aligned} p = &\frac{3}{2}V_{0_p}I_{0_p}cos(\theta_{v_p} - \theta_{0_p}) + \frac{3}{2}V_{0_p}I_{0_n}cos(2\omega t + \theta_{v_p} + \theta_{0_n}) \\ &+ \frac{3}{2}V_{0_n}I_{0_p}cos(2\omega t + \theta_{v_n} + \theta_{0_p}) + \frac{3}{2}V_{0_n}I_{0_n}cos(\theta_{v_n} - \theta_{0_n}) \end{aligned} \tag{4.50}$$

$$\begin{aligned} q = &\frac{3}{2}V_{0_p}I_{0_p}sin(\theta_{v_p} - \theta_{0_p}) + \frac{3}{2}V_{0_p}I_{0_n}sin(2\omega t + \theta_{v_p} + \theta_{0_n}) \\ &+ \frac{3}{2}V_{0_n}I_{0_p}sin(2\omega t + \theta_{v_n} + \theta_{0_p}) + \frac{3}{2}V_{0_n}I_{0_n}sin(\theta_{v_n} - \theta_{0_n}) \end{aligned} \tag{4.51}$$

The unbalance produces a 2ω ripple in p and q. The low pass filter placed in each droop loop is able to eliminate the double frequency component in p and q, thus leaving only the average power P and Q in order to achieve average power sharing between inverters even during unbalanced operation. If the inverters are connected through an impedance, as they

are in the microgrid model under study, this average power sharing does not result in an equal sharing of the unbalanced power component [83]. The effects of this behaviour will be discussed in Section 4.4.5 when considering faults which do not cause current limiting.

4.4.3 Droop control and current limiting

As discussed in Section 4.3, RMS current limiting in the NatRF (see Figure 4.38) is chosen as the current limiting strategy in each inverter. In the event of a fault, the current is supplied by two inverters which are both able to supply twice their nominal current. As a result, the two inverters together can supply a current four times bigger than their nominal current. The increased fault current capacity could generate a situation where, in the event of a fault, the inverters do not have to limit their current as the fault current is below their combined capabilities. Section 4.4.5 will illustrate and discuss the impact of this increase in fault current on the microgrid fault response.

In the event of faults which require a considerable fault current, the control of faulted phases is switched to current control while voltage control is kept in the healthy phases.

4.4.4 System description: Model 3

The network and inverter parameters of the microgrid model can be found in Table 3.1 which also includes the values of the inverters' interconnecting impedance Z_l. The inverters are identical with the same specifications as the previous ones and their voltage and current control loops are designed as the ones described in Section 4.2.4. Using equations (3.9) and (3.10), the frequency droop gain m_p is chosen to give a 0.3% frequency droop at the maximum real power output, while the voltage droop gain n_q is chosen to give a 2% voltage droop at the maximum reactive power. As the inverters are equally rated, the droop gains for each inverter are identical. The filter in Figure 3.16 is a low-pass filter with a cut-off frequency around 5 Hz.

The design of the current limiting in each inverter is identical to the one for RMS current limiting in the NatRF described in Section 4.2.4.

4.4.5 Fault response of a microgrid supplied by two parallel-connected inverters: Case 6

Figures 4.47, 4.48, 4.49 and 4.50 show the response of the microgrid supplied by two parallel inverters with droop control to the standard faults considered for the previous

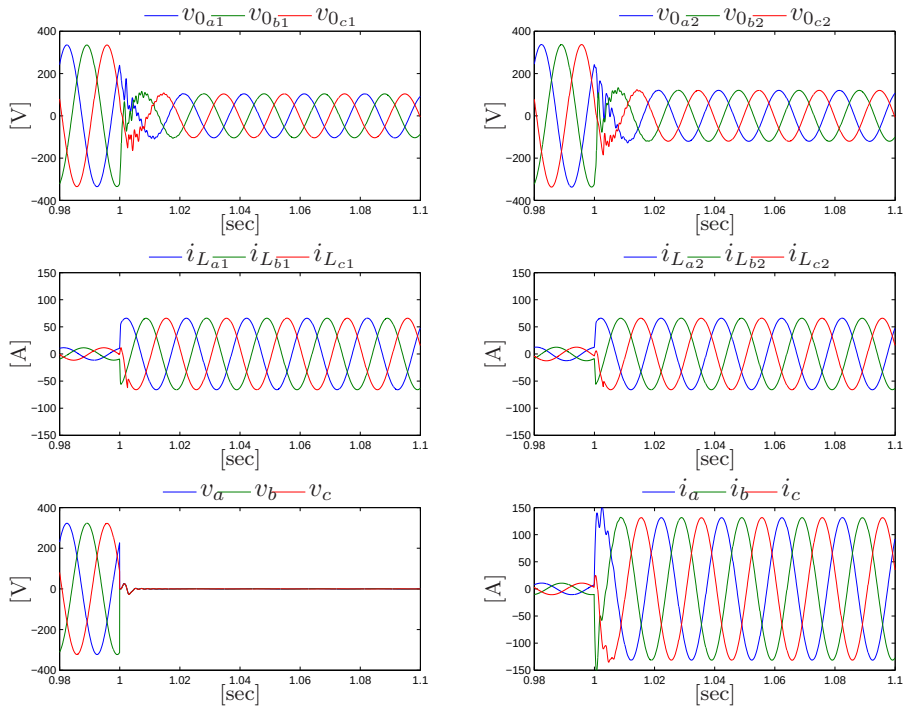


Figure 4.47: Response to a 3ϕ fault at point F_3 of a microgrid supplied by two parallel-connected inverters

models. Faults are applied at point F_3, see Figure 3.20, in the microgrid at time t=1s.

From the control point of view, it can be said that in the event of a fault, the outer voltage and frequency droop loops generate new voltage and frequency references because the active and reactive power supplied will change. As the current limiting strategy is on a per-phase base, any change introduced by the voltage droop loop will only affect the healthy phases while a change in frequency affects both healthy and faulty phases. From Figures 4.47, 4.48, 4.49 and 4.50 it can be seen that the fault response is again fast (less than one cycle). However the presence of the droop loops and the slow dynamics of the filters in them should have an impact on the speed of the fault response of inverters. Indeed the slow dynamics of the droop loops can be seen in Figures 4.51 and 4.52 where the fundamental powers P and Q, the reference voltage $v_{0_d}^*$ and the reference frequency ω^* for the two inverters in the event of a three-phase and a single phase-to-ground faults are shown. As expected, the droop loops responses are rather slow as the filter is designed with a bandwidth around 5 Hz. However the droop gains m_p and n_q are quite small and therefore changes in $v_{0_{d1}}^*$, $v_{0_{d2}}^*$, ω_1^* and ω_2^* are small as well and do not substantially affect

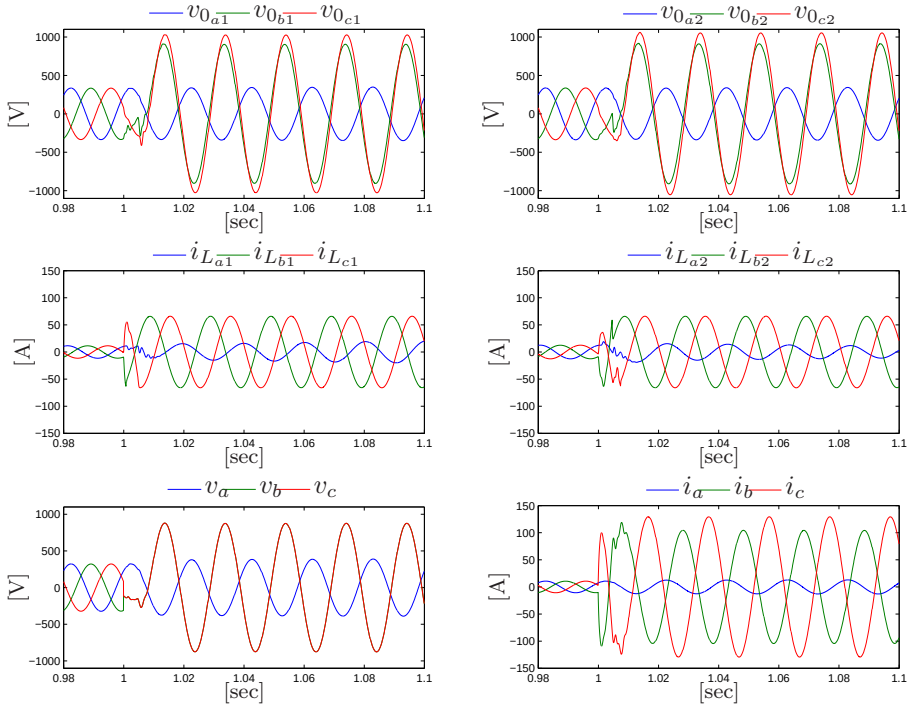


Figure 4.48: Response to a 2ϕ fault at point F_3 of a microgrid supplied by two parallel-connected inverters

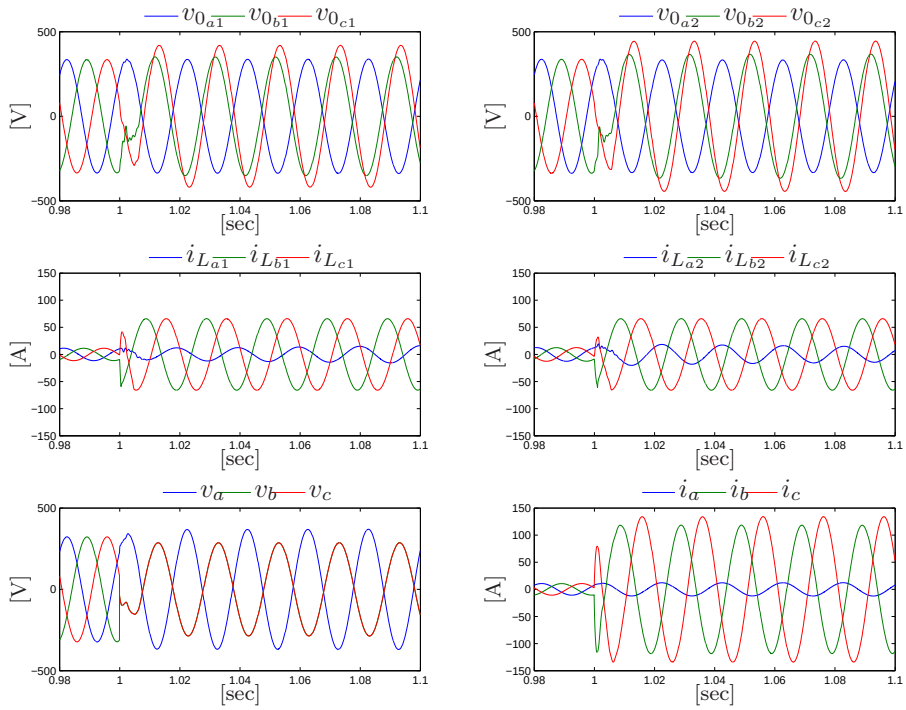


Figure 4.49: Response to a $2\phi g$ fault at point F_3 of a microgrid supplied by two parallel-connected inverters

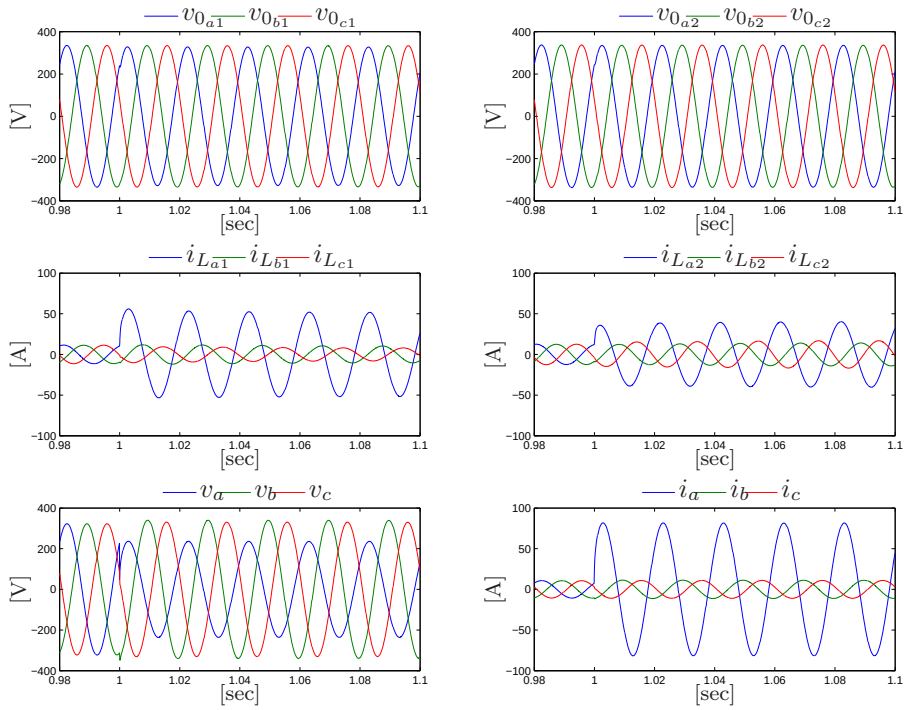


Figure 4.50: Response to a $1\phi g$ fault at point F_3 of a microgrid supplied by two parallel-connected inverters

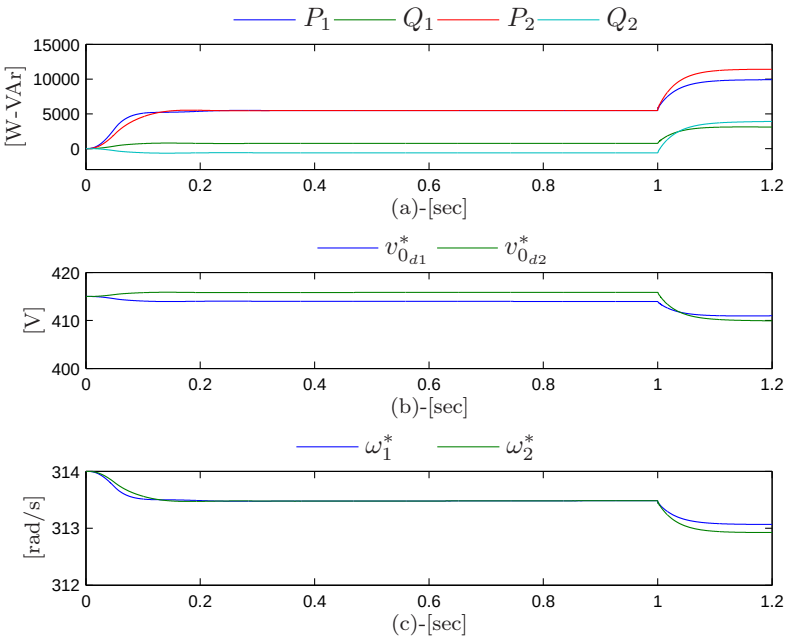


Figure 4.51: Microgrid response (two parallel-connected inverters) to a 3ϕ fault at point F_3: (a) Fundamental active and reactive powers, (b) Generated voltage references, (c) Generated frequency references

the fault response of the microgrid. This is the reason why at a first glance the effect of the droop control cannot be seen in Figures 4.47, 4.48, 4.49 and 4.50.

Besides the fault dynamics of droop loops, Figure 4.51 also shows that for a 3ϕ fault the inverters supply an increased amount of active power (i.e. P_1 and P_2) compared with the pre-fault operation. This behaviour is quite different to that of a conventional power system where a 3ϕ fault results in a very small active power supplied by generators. Here, the increased active power is given by the losses in the line resistances, which in a distribution network are higher in value than the reactances, caused by the flow of the fault current injected by the two inverters. The equivalent microgrid fault models, which are going to be developed and discussed in the next Chapter, can explain this particular behaviour and the role of line parameters in it.

As the inverters have the voltage and current loops implemented in the NatRF with RMS current limiting, their responses should be compared with those of a stand-alone inverter microgrid in Figures 4.43, 4.44, 4.45 and 4.46 (see Pages 130 and 131). For a 3ϕ fault, see Figure 4.47, both inverters are switched to current control as soon as the reference inductor currents hit their limit and the resulting fault current is twice the value

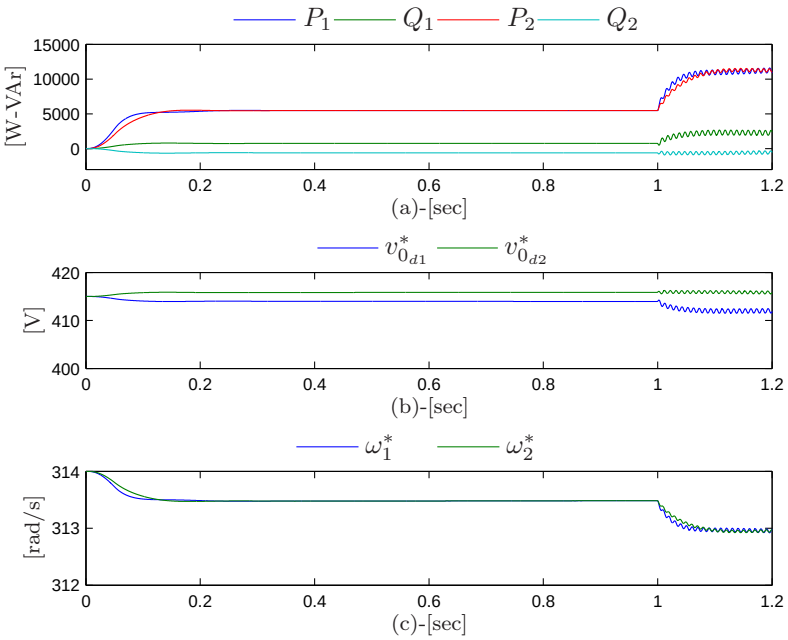


Figure 4.52: Microgrid response (two parallel-connected inverters) to a $1\phi g$ fault at point F_3: (a) Fundamental active and reactive powers, (b) Generated voltage references, (c) Generated frequency references

for the single inverter microgrid in Figure 4.43 (see Page 130). It should be noted that the output phase voltages of inverter 1 are visibly lower than the one of inverter 2. This effect cannot be caused by the voltage droop as the voltage control feedback is broken when the current control is switched on. Once again, in Chapter 5, this behaviour will be analyzed by the development of an inverter fault model.

For a 2ϕ and a $2\phi g$ fault, see Figures 4.48 and 4.49, the control of phases b and c is switched to current while phase a is still voltage controlled. The two voltage droop loops generate new references $v^*_{0_{d1}}$ and $v^*_{0_{d2}}$, however, as their change is small, no visible change in $v_{0_{a1}}$ and $v_{0_{a2}}$ can be seen in Figures 4.48 and 4.49. Same thing can be said about ω^* which can be considered constant. During the faults phases b and c are current controlled and each inverter injects a current twice the nominal value. This causes an increase in the voltages which go beyond the inverters' capabilities. As a result, the built-in voltage limiting strategy will be activated as described in Section 4.1.5. This behaviour was also observed in Figure 4.44 (see Page 130) for a 2ϕ fault in a microgrid supplied by a single inverter. In order to prevent the action of the voltage limit, a solution could be to reduce the amount of current supplied by each inverter after the current limiting is triggered.

The response of the microgrid to a $1\phi g$ fault at F_3 is quite different compared with the previous ones in Figures 4.47, 4.48 and 4.49 and compared with the one in Figure 4.46 (see Page 131) for a $1\phi g$ fault in a single-inverter microgrid. The difference is that this time the reference inductor current of phase a does not hit the limit and therefore during the fault all phases remain voltage controlled. Indeed the required fault current is well within the combined capabilities of the two inverters. However, the unbalanced load caused by the $1\phi g$ fault is not shared equally between the two inverters and $i_{L_{a1}} > i_{L_{a2}}$. Changes in $v^*_{0_{d1}}$, $v^*_{0_{d2}}$, ω^*_1 and ω^*_2 are again very small, see Figure 4.52, and therefore do not visibly affect the response of the two inverters.

If the position of the $1\phi g$ fault becomes closer to the inverters, the required current will increase and inverter current limiting will be triggered. Figure 4.53 shows the response of the microgrid to a $1\phi g$ fault at location F_1 (defined in Figure 3.20). In this case the first inverter goes into current limiting while the second one does not. Again, this asymmetric behaviour arises because the two inverters are not forced to share the unbalanced load.

Overall, the main difference between the droop control fault response and the stand-alone control fault response does not lie in the control but rather on the combined capability of parallel inverters to supply current in the event of a fault.

4.5 Conclusion on fault response of islanded inverter-only microgrids

This Chapter has described, with the help of time-domain simulations, how different the response of islanded inverter-only microgrids can be depending on the design of the inverter control and how the choices made in the control (e.g. reference frame implementation, current and voltage limiting) can shape such response.

From this analysis it has been demonstrated that certain control strategies give a better response for the microgrid network. In particular, the widely used control in the SynRF produces undesirable overvoltages and consequently distorted waveforms. A much better fault response is given by control in the NatRF which gives the flexibility to limit the current on the faulty phases while keeping control over the voltage on the healthy ones. The improved response of the NatRF control is shown in Figure 4.54 where Figures 4.23 and 4.45 are presented side by side for the reader's convenience. In particular, from Figure 4.54 it is possible to compare, for a $2\phi g$ fault, the overvoltage in the healthy phase

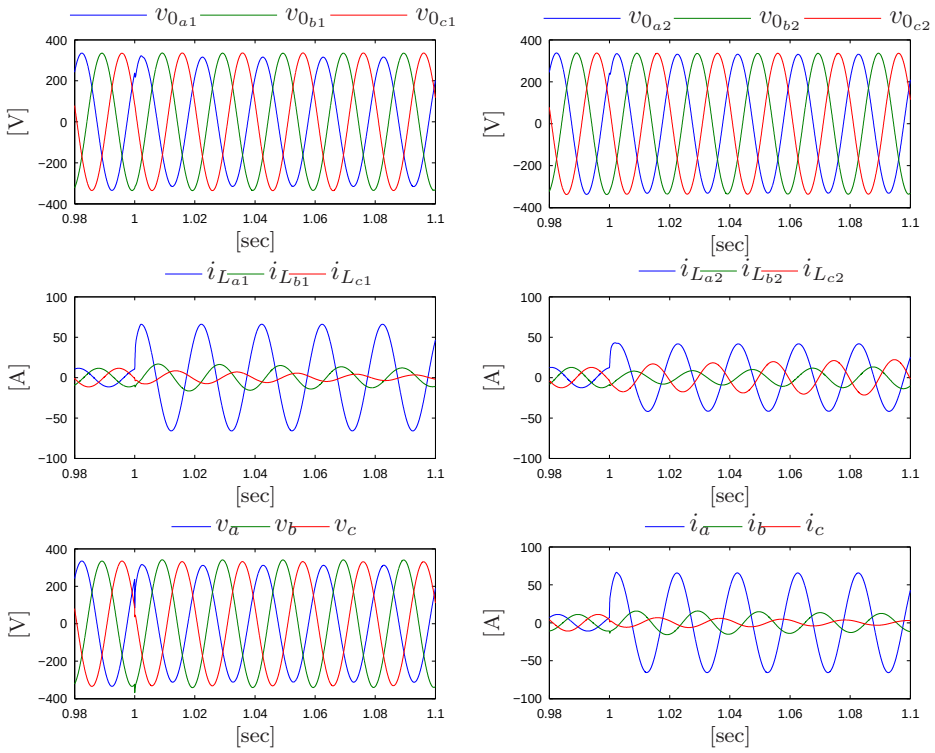


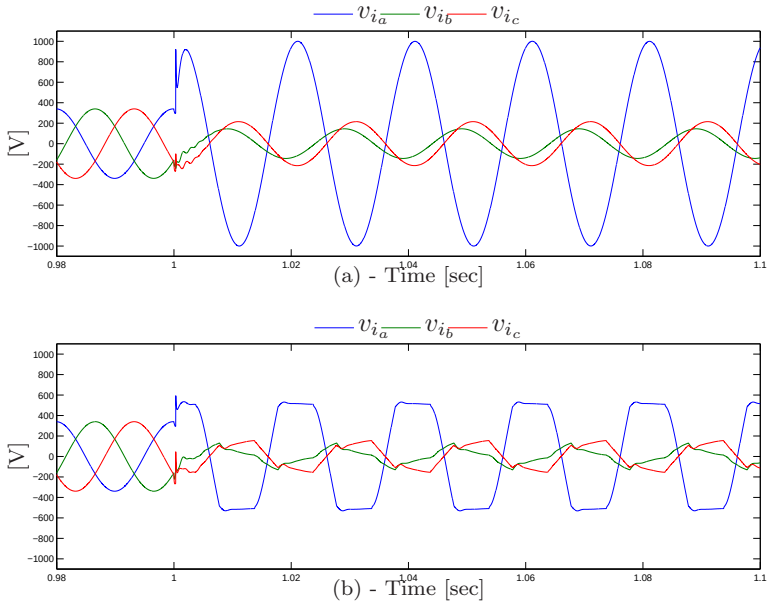
Figure 4.53: Response to a $1\phi g$ fault at point F_1 of a microgrid supplied by two parallel-connected inverters (droop control with multi-loop control in NatRF and RMS current limiting in the NatRF)

a caused by the control in the SynRF with current limiting in the SynRF, the resulting distorted waveforms of the inverter bridge voltages caused by the inverter voltage limiting and the controlled output voltage on phase a with control in the NatRF.

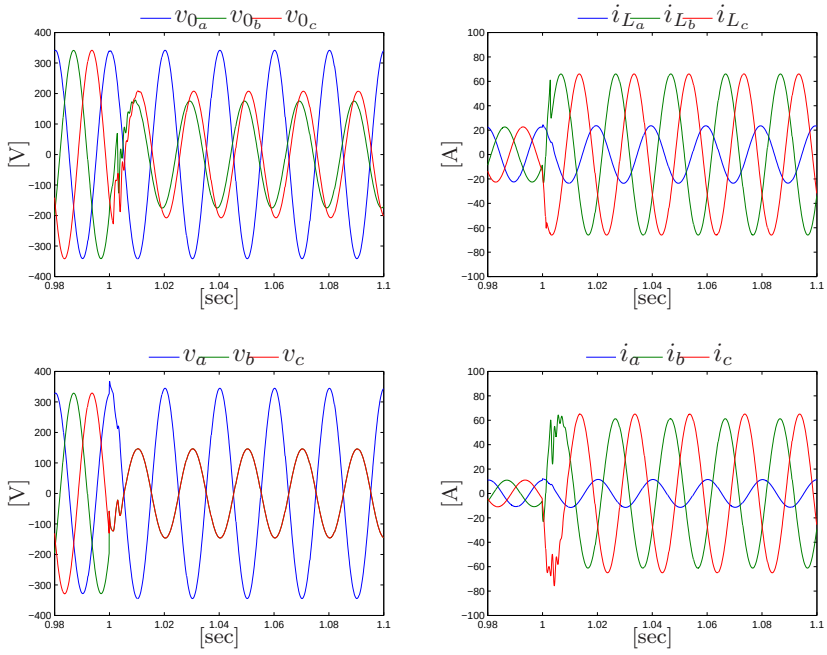
Simulations in the Chapter also showed that RMS current limiting is preferable over the instantaneous limiting as it avoids waveform distortion. This can be now seen in Figure 4.55 which combines for easy comparison Figures 4.41 and 4.45. Figure 4.41 show the response for to a $2\phi g$ fault of the control in the NatRF with instantaneous current limiting while Figure 4.45 shows the response with control in the NatRF and RMS current limiting respectively. The RMS current response shows that there is control on healthy phase voltages and no harmonically distorted output.

Difficulties in the integration of inverter's requirements (i.e. current and voltage limits) with network's requirements (i.e. voltage control, waveform distortion and predictable fault response) have been highlighted as well. This integration is made even more challenging by the lack of guiding principles (e.g. standards on inverter-only microgrid fault behaviour) and lack of information from inverter' manufacturers. Nevertheless the flexibility associated with the control of inverters can address the inverter's and the network's requirements and even produce a desired inverter fault response.

Finally, it has to be recognized that the time-domain simulations have only given a simple quantitative idea of the behaviour of the example islanded inverter-only microgrids. The use of example simulations is not sufficient to understand the interactions between the inverter and the network. There is a need to develop simplified models which can capture the behaviour of the microgrid and help the design engineer to understand the system. The modelling of inverter-interfaced DG units and their integration in a fault analysis method is the topic of the next Chapter.

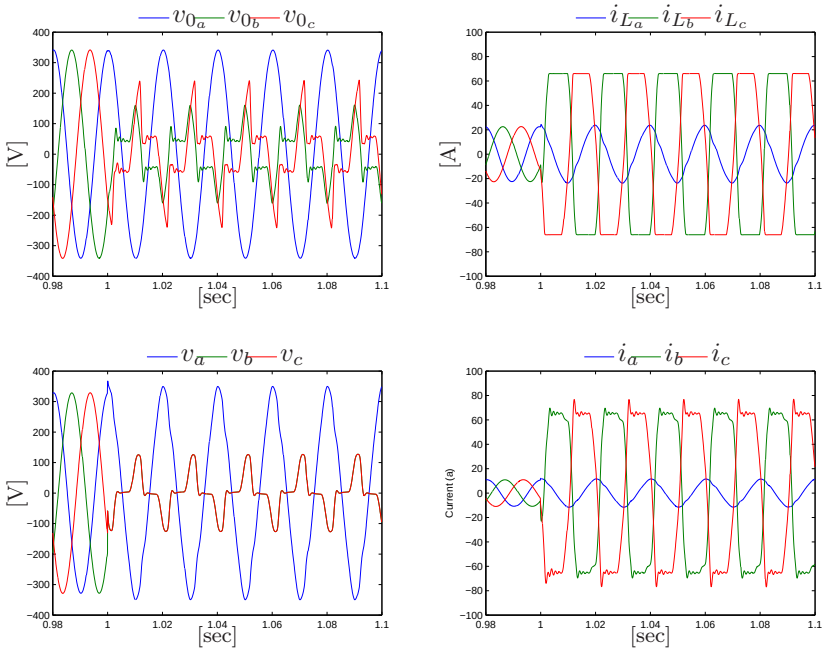


Comparison of v_{i_a}, v_{i_b} and v_{i_c} for a $2\phi g$ fault at point F_3 in a microgrid supplied by a single inverter (control and current limiting in the SynRF): (a) Without instantaneous voltage limiting, (b) With voltage limiting algorithm as in [76]

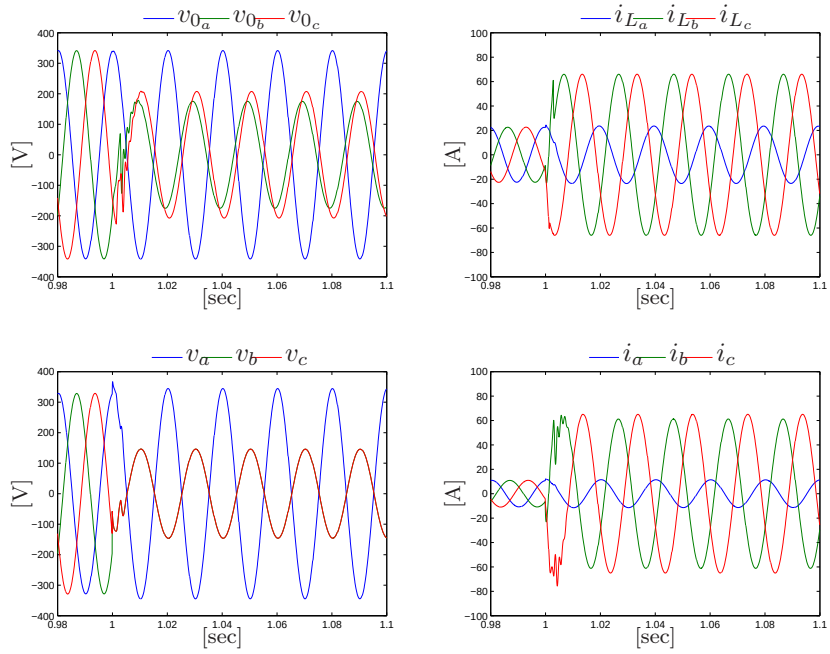


Response to a $2\phi g$ fault at point F_3 of a microgrid supplied by a single inverter (control in the NatRF and RMS current limiting in the NatRF)

Figure 4.54: Reproduced from Figures 4.23 and 4.45



Response to a $2\phi g$ fault at point F_3 of a microgrid supplied by a single inverter (control in the NatRF and instantaneous current limiting in the NatRF)



Response to a $2\phi g$ fault at point F_3 of a microgrid supplied by a single inverter (control in the NatRF and RMS current limiting in the NatRF)

Figure 4.55: Reproduced from Figures 4.41 and 4.45

Chapter 5

Modelling and fault analysis of islanded inverter only-microgrids

The study of fault behaviour in power networks is a well established field. The techniques used, however, have been developed for conventional synchronous machine-based generation and do not consider the new forms of DG sources with converter interfaces. Fault analysis of microgrids dominated by inverter-interfaced DG continues to be hampered by the lack of agreed and appropriate models for this new form of generation. Indeed, the inverter representations used are generally complex, making it difficult to visualise the link between inverter control and subsequent fault behaviour of the microgrid.

The relevance of the inverter control in the fault response of the microgrid has been analyzed in Chapter 4 through use of time-domain simulations with the PSCAD software. It has been shown how different reference frame implementations and current limiting strategies can shape the currents and the voltages in the microgrid. However, the results shown in Chapter 4 are not sufficient to completely understand the inverter's fault behaviour and its interactions with the network because they can only give intuitive ideas about them. The purpose of this Chapter is therefore to develop simple but sufficiently complete mathematical fault models of inverters which can be used in traditional fault analysis.

Starting from the description of the inverter control features, three different inverter models (control in the SynRF, control in the NatRF and droop control) are developed. These models are shown to be able to provide a clear interpretation of the fault behaviour of the microgrid, as determined using PSCAD in Chapter 4. Indeed, they incorporate the underlying interactions between the inverter dynamics and the microgrid network. Finally,

the models are used in quasi steady-state fault calculations, whose results are consistent with those obtained using PSCAD. This provides a further demonstration of the ability of the developed models to reflect the basic phenomena that affect the fault behaviour of inverter-dominated microgrids.

5.1 Inverter models for fault analysis studies

In an islanded microgrid only supplied by inverter-interfaced DG units, the inverters' response to a fault condition will dominate the behaviour of the whole system. An understanding of inverter behaviour under fault conditions can be developed by starting with the simple equivalent model of a stand-alone multi-loop controlled inverter and then analyzing how it changes in the event of a fault. First, this general fault model will be adapted to the two control schemes (SynRF and NatRF) described in Chapter 4 so that for each of them an equivalent model which captures the inverter's fault behaviour is available. Then droop control and its impact on the developed fault model will be analyzed as well.

5.1.1 Fault models of stand-alone multi-loop controlled inverter

It is common practice to summarise the control strategy of an individual inverter by expressing the relation between output voltage v_0, reference v_0^* and load current i_0 as in equation (3.1). Figure 3.14 showed the equivalent inverter two-terminal circuit, where $G(s)$ is the inverter voltage gain (see equation (3.2)) and $Z_0(s)$ is the output impedance (see equation (3.3)).

As previously explained in Chapter 4, under fault conditions, inverters can supply a current of only around two times their nominal current. The current is limited by placing a saturation block in the control loop in order to limit the reference inductor current i_L^* as shown in Figure 5.1. In the event of a fault, the current in the network increases and as saturation is reached, the voltage feedback loop is broken because the output of the saturation block is no more influenced by its input. This break in the loop reduces the two-loop control of the inverter to a single current loop control. Therefore, from Figure 5.1 and considering the saturation block, the following relationship can be written:

$$V_0(s) = (G_{CC}(s)I_{Lsat}^* - I_0(s))\frac{1}{sC_f} \tag{5.1}$$

where I_{Lsat}^* is the reference maximum inductor current. Equation (5.1) can be re-arranged

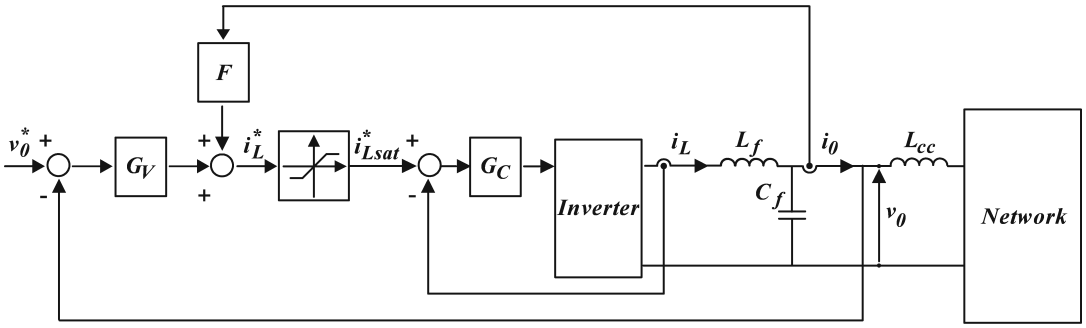


Figure 5.1: Multi-loop control of a stand-alone inverter with current limiting

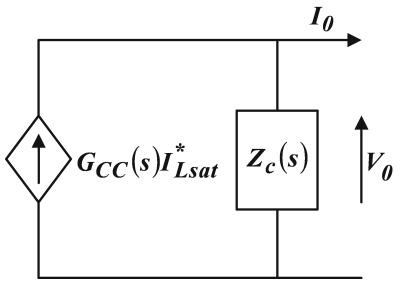


Figure 5.2: Equivalent two-terminal circuit of a stand-alone inverter with current limiting

as

$$I_0(s) = G_{CC}(s)I_{Lsat}^* - sC_fV_0(s) \tag{5.2}$$

and the equivalent circuit of the inverter is shown in Figure 5.2, where $Z_c(s) = \frac{1}{sC_f}$. At the operating frequency, the transfer function $G_{CC}(s)$ has a gain close to unity, therefore the inverter behaves like a constant current source with a parallel impedance.

As the voltage loop is broken, the response of the inverter is dominated by the current control loop which is usually designed with a high bandwidth (around 1.6 kHz). Therefore the transient which the inverter undergoes in the event of a fault lasts less than one cycle. It should be noted here that any voltage limiting on the inverter bridge is not being considered at this point, this is because the inverter is controlled and operated so that the voltage limit is never reached and therefore distorted waveforms are not produced.

Stand-alone inverter controlled in the SynRF

From the general model shown in Figure 5.2, an equivalent fault model for a stand-alone four-leg inverter controlled in the SynRF can be developed by considering the inverter's

response to different faults. As discussed in Section 4.1.1, the control of a stand-alone four-leg inverter in the SynRF requires three loops identical to the one in Figure 5.1, one for each coordinate. Three saturation blocks are placed in each loop, see Figure 4.9, and the chosen current limiting strategy is devised so that as soon as one of the reference inductor currents $I^*_{L_d}$, $I^*_{L_q}$ and $I^*_{L_\gamma}$ reaches its saturation limit, the control switches all the reference inductor currents to a corresponding fixed constant value $I^*_{Lsat_d}$, $I^*_{Lsat_q}$ and $I^*_{Lsat_\gamma}$. This approach is a good compromise between the inverter's own limited current ratings and the requirements of a predictable inverter response in the event of a fault.

Once the values of $I^*_{L_d}$, $I^*_{L_q}$ and $I^*_{L_\gamma}$ are kept constant, the voltage feedback loop is broken and the inverter is now operating as a controlled current source. From Figures 4.1 and 4.9, taking into account the break in the voltage control loop, the following equations can be written:

$$\begin{aligned} V_{0_d} &= (G_{CC}(s)I^*_{Lsat_d} - I_{0_d} + \omega C_f V_{0_q})\frac{1}{sC_f} \\ V_{0_q} &= (G_{CC}(s)I^*_{Lsat_q} - I_{0_q} - \omega C_f V_{0_d})\frac{1}{sC_f} \\ V_{0_\gamma} &= (G_{CC}(s)I^*_{Lsat_\gamma} - I_{0_\gamma})\frac{1}{sC_f} \end{aligned} \tag{5.3}$$

From these equations it can be seen that in the event of a fault the inverter becomes equivalent to three controlled current sources, one for each coordinate, with an equivalent two-terminal circuit representation as shown in Figure 5.2. The only difference is that the d and q components are coupled through the action of the capacitors.

The next step is to derive the equivalent inverter fault model in the NatRF. The transformation of equations (5.3) from the SynRF to the StatRF and then to the NatRF is done according to the transformations described in Section 4.2.2 and in Appendix B. This derivation would lead to a rather complex and coupled system in the NatRF. However, the closed current loop transfer function has a unity gain at the system operating frequency and therefore equations (5.3) can be simply written in the NatRF as:

$$\begin{aligned} V_{0_a} &= (I^*_{Lsat_a} - I_{0_a})\tfrac{1}{sC_f} \\ V_{0_b} &= (I^*_{Lsat_b} - I_{0_b})\tfrac{1}{sC_f} \\ V_{0_c} &= (I^*_{Lsat_c} - I_{0_c})\tfrac{1}{sC_f} \end{aligned} \tag{5.4}$$

From equations (5.4) it can be seen that in the NatRF in the event of a fault, the inverter

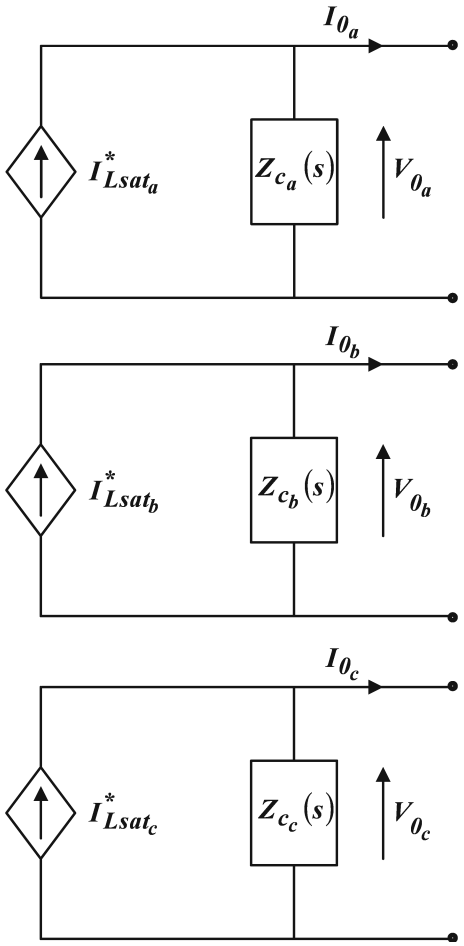


Figure 5.3: Three-phase four-leg SynRF controlled inverter fault model: equivalent phase networks

behaves like three current sources (one for each phase) with a parallel constant impedance. Figure 5.3 shows these equivalent phase circuits where $Z_{c_a}(s) = Z_{c_b}(s) = Z_{c_c}(s) = Z_c(s)$. The instantaneous values of the current sources can be calculated from $I^*_{Lsat_d}$ and $I^*_{Lsat_q}$ as follows:

$$\begin{aligned} i^*_{Lsat_a}(t) &= \sqrt{\frac{2}{3}} I^*_{Lsat_{dq}} cos(\omega t + \phi_{dq}) \\ i^*_{Lsat_b}(t) &= \sqrt{\frac{2}{3}} I^*_{Lsat_{dq}} cos(\omega t + \phi_{dq} - \frac{2}{3}\pi) \\ i^*_{Lsat_c}(t) &= \sqrt{\frac{2}{3}} I^*_{Lsat_{dq}} cos(\omega t + \phi_{dq} + \frac{2}{3}\pi) \end{aligned} \tag{5.5}$$

where $I^*_{Lsat_{dq}} = \sqrt{I^{*^2}_{Lsat_d} + I^{*^2}_{Lsat_q}}$,$\phi_{dq} = \arctan \frac{I^*_{Lsat_q}}{I^*_{Lsat_d}}$ and $I^*_{Lsat_\gamma} = 0$, as decided in Section 4.1.4. The three current sources form a positive sequence three-phase system therefore overall the inverter can be considered as a constant positive sequence current source with a parallel impedance. The choice of $I^*_{Lsat_d}$ and $I^*_{Lsat_q}$ determines the magnitude and phase of the current. For the particular model considered in Section 4.1.4, $I^*_{Lsat_d} = 79.48$ A and $I^*_{Lsat_q} = -12.75$ A which give a magnitude $I^*_{Lsat_{dq}}$ equal to 80.49 A and a phase angle ϕ_{dq} equal to $-9.14°$.

Fault studies are often undertaken using sequence-component models. The model in Figure 5.3 expressed in the NatRF can be converted to sequence components by first re-writing the equations in (5.4) in compact form as:

$$(I^*_{Lsat_{abc}} - I_{0_{abc}}) = Y_{c_{abc}} V_{0_{abc}} \tag{5.6}$$

where $Y_c = \frac{1}{Z_c(s)}$. By writing $I^*_{Lsat_{abc}}$, $I_{0_{abc}}$ and $V_{0_{abc}}$ in terms of their sequence components $I^*_{Lsat_{pn0}}$, $I_{0_{pn0}}$ and $V_{0_{pn0}}$, equation (5.6) becomes:

$$A(I^*_{Lsat_{pn0}} - I_{0_{pn0}}) = Y_{c_{abc}} A V_{0_{pn0}} \tag{5.7}$$

where A is the Fortescue's transformation matrix (see Appendix A). Multiplying both sides in equation (5.7) by by A^{-1} yields:

$$(I^*_{Lsat_{pn0}} - I_{0_{pn0}}) = Y_{c_{pn0}} V_{0_{pn0}} \tag{5.8}$$

The term $Y_{c_{pn0}}$ is the sequence components admittance matrix and is given by:

$$Y_{c_{pn0}} = A^{-1} Y_{c_{abc}} A = \begin{bmatrix} Y_{c_p} & 0 & 0 \\ 0 & Y_{c_n} & 0 \\ 0 & 0 & Y_{c_0} \end{bmatrix} \tag{5.9}$$

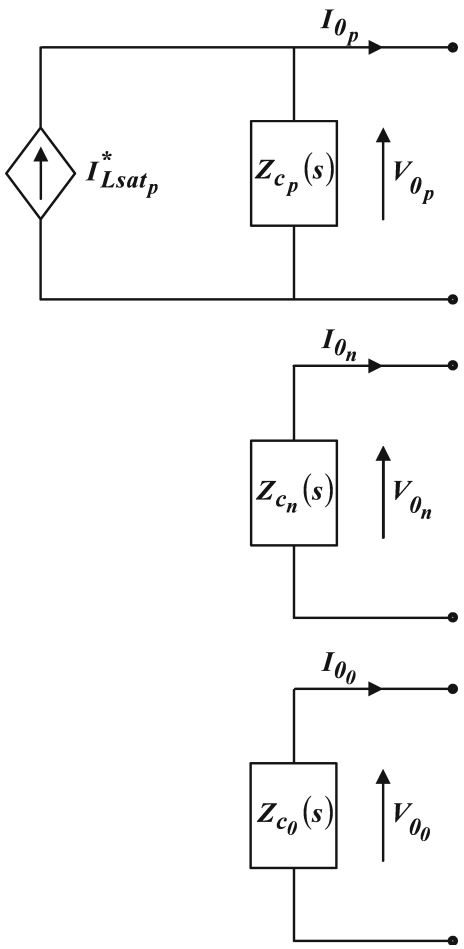


Figure 5.4: Three-phase four-leg SynRF controlled inverter fault model: equivalent sequence networks

where $Y_{c_p} = Y_{c_n} = Y_{c_0} = Y_c$. Equation (5.8) describes three networks (positive, negative and zero sequence) formed of a current source and a parallel impedance. Because in the original inverter model only positive sequence current is generated, $I^*_{Lsat_n}$ and $I^*_{Lsat_0}$ are equal to zero and therefore the sequence circuit representation of the inverter shown in Figure 5.4 has only one current source. Note that $Z_{c_p}(s) = Z_{c_n}(s) = Z_{c_0}(s) = Z_c(s)$.

Stand-alone inverter controlled in the NatRF

A stand-alone inverter controlled in the NatRF requires three equivalent multi-loop controllers. The key difference between control in the SynRF and control in the NatRF is the ability of the control in the NatRF to regulate the voltage of each phase independently. Here the RMS current limiting in the NatRF, see Figure 4.38, is adopted. As discussed in Section 4.3, with this current limiting strategy, it is possible to keep control over the voltage of the healthy phases while actively limiting the current in the faulty ones without distorted waveforms.

Because the phases are controlled independently, the fault model of the inverter is strongly dependent on the type of fault. Here, the derivation of inverter model for a $1\phi g$ fault is described and inverter models for other faults can be developed using the same approach. For a $1\phi g$ fault, phase a is current limited and therefore its equivalent circuit is similar to the one in Figure 5.2, while phases b and c are voltage controlled and have an equivalent circuit like the one pictured in Figure 3.14. The resulting equivalent fault model of the inverter in phase coordinates is shown in Figure 5.5.

In the circuit corresponding to phase a, the current source is given by $G_{CC}(s)I^*_{Lsat_a}$, where $I^*_{Lsat_a}$ is twice the nominal inverter current and the parallel impedance $Z_{c_a}(s)$ is equal to $Z_c(s)$. The closed loop transfer function of the current loop can be expressed as:

$$G_{CC}(s) = \frac{K_I N(s)}{1 + K_I N(s)} \tag{5.10}$$

where K_I is the proportional controller in the current loop and $N(s)$ is dependent on the LC output filter parameters. During the design stage, $N(s)$ is chosen as $\frac{L_f+2L_n}{sL_f(L_f+3L_n)}$ in order simplify the procedure to obtain the controllers' parameters, but now, its full expression has to be used. $N(s)$ can be derived by substituting (4.5) into equations (4.1)

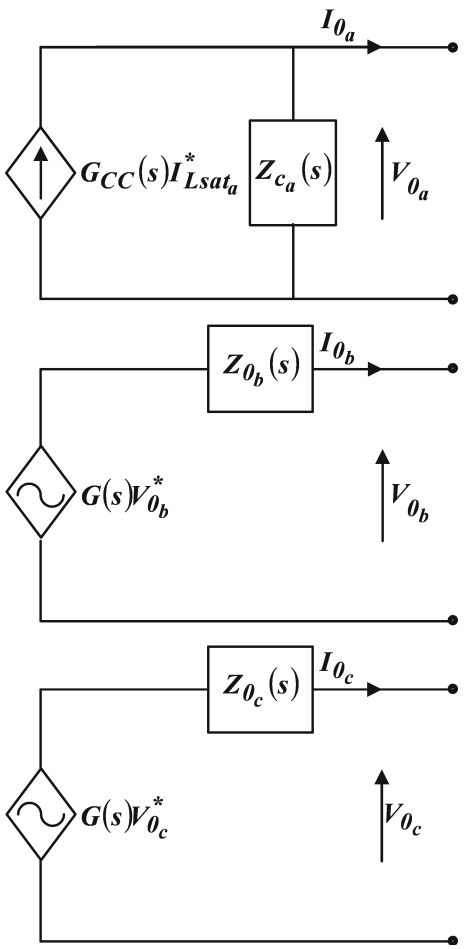


Figure 5.5: Equivalent phase networks of a three-phase four-leg inverter controlled in the NatRF for a $1\phi g$ fault.

and re-arranging them in the frequency domain as:

$$\begin{aligned} V_{i_a} &= (R_f + sL_f)I_{L_a} + V_{0_a} + (R_n + sL_n)(I_{L_a} + I_{L_b} + I_{L_c}) \\ V_{i_b} &= (R_f + sL_f)I_{L_b} + V_{0_b} + (R_n + sL_n)(I_{L_a} + I_{L_b} + I_{L_c}) \\ V_{i_c} &= (R_f + sL_f)I_{L_c} + V_{0_c} + (R_n + sL_n)(I_{L_a} + I_{L_b} + I_{L_c}) \end{aligned} \tag{5.11}$$

which can then be written in matrix form as:

$$\begin{bmatrix} V_{i_a} - V_{0_a} \\ V_{i_b} - V_{0_b} \\ V_{i_c} - V_{0_c} \end{bmatrix} = B \begin{bmatrix} I_{L_a} \\ I_{L_b} \\ I_{L_c} \end{bmatrix} \tag{5.12}$$

where the matrix B is defined as:

$$B = \begin{bmatrix} (R_f + R_n + s(L_f + L_n)) & (R_n + sL_n) & (R_n + sL_n) \\ (R_n + sL_n) & (R_f + R_n + s(L_f + L_n)) & (R_n + sL_n) \\ (R_n + sL_n) & (R_n + sL_n) & (R_f + R_n + s(L_f + L_n)) \end{bmatrix} \tag{5.13}$$

Multiplying both terms in (5.12) by B^{-1}, the inductor currents can be expressed as a function of the voltage drop across the filter inductance as:

$$\begin{bmatrix} I_{L_a} \\ I_{L_b} \\ I_{L_c} \end{bmatrix} = B^{-1} \begin{bmatrix} V_{i_a} - V_{0_a} \\ V_{i_b} - V_{0_b} \\ V_{i_c} - V_{0_c} \end{bmatrix} \tag{5.14}$$

where the matrix B^{-1} is defined as

$$B^{-1} = \begin{bmatrix} \frac{sL_f+2sL_n+R_f+2R_n}{D(s)} & \frac{-(R_n+sL_n)}{D(s)} & \frac{-(R_n+sL_n)}{D(s)} \\ \frac{-(R_n+sL_n)}{D(s)} & \frac{sL_f+2sL_n+R_f+2R_n}{D(s)} & \frac{-(R_n+sL_n)}{D(s)} \\ \frac{-(R_n+sL_n)}{D(s)} & \frac{-(R_n+sL_n)}{D(s)} & \frac{sL_f+2sL_n+R_f+2R_n}{D(s)} \end{bmatrix} \tag{5.15}$$

and the denominator $D(s)$ of each element in matrix B^{-1} is

$$D(s) = R_f^2 + 2sR_fL_f + 3R_fR_n + 3sR_fL_n + 3sR_nL_f + s^2L_f^2 + 3s^2L_fL_n. \tag{5.16}$$

Finally, from equations (5.14), (5.15) and (5.16) ,the relationship between the phase inductor current I_L and the relative phase voltage drop for each phase is given by:

$$I_{L_x} = N(s)(V_{i_x} - V_{0_x}) \tag{5.17}$$

where $x = a, b, c$ and $N(s)$ is

$$N(s) = \frac{sL_f + 2sL_n + R_f + 2R_n}{R_f^2 + 2sR_fL_f + 3R_fR_n + 3sR_fL_n + 3sR_nL_f + s^2L_f^2 + 3s^2L_fL_n} \tag{5.18}$$

For the control in the SynRF, the full expression of $N(s)$ would be $\frac{1}{sL_f+R_f}$ for the d and q loops and $\frac{1}{s(L_f+3L_n)+R_f+3R_n}$ for the γ loop. The resulting closed loop transfer function for each loop would have to be determined as in (5.10) where K_I is substituted by the current loop controller $G_C(s)$. Finally, equations in (5.3) would have to be transformed from the SynRF to the NatRF in order to have the equivalent inverter fault model in the NatRF. However, as in the SynRF the value of G_{CC} at system frequency is very close to unity, this whole procedure is simplified by assuming $G_{CC}(j50) = 1$.

In the circuits corresponding to phases b and c in an inverter controlled in the NatRF, the voltage sources are given by $G(s)V_{0_b}^*$ and $G(s)V_{0_c}^*$ where $G(s)$ is the inverter voltage gain and $V_{0_b}^*$ and $V_{0_c}^*$ are the nominal reference phase voltage values. The inverter voltage gain is calculated as in equation (3.2) and the series connected output impedances are given by:

$$Z_{0_b(s)} = Z_{0_c(s)} = Z_0(s) = -\frac{FG_{CC}(s) - 1}{sC_f + G_V(s)G_{CC}(s)} \tag{5.12}$$

Finally, the developed per-phase inverter fault model can be further transformed by substituting the circuits of phase b and c with their Norton equivalent circuit. As a result a three-phase four-leg inverter controlled in the NatRF can be represented as three equivalent phase current sources with a parallel impedance as shown in Figure 5.6.

5.1.2 Fault models of parallel-connected inverters

The presence of two parallel inverters supplying a microgrid mainly affects the total available amount of current which can be supplied in the event of a fault. As described and illustrated in Section 4.4.5, in the event of a fault the reference voltage and frequency droop loops have very slow dynamics and generate new references $v_{0_d}^*$ and ω^* which can be considered approximately equal to their values before the fault. This happens because the droop gains m_p and n_q are specifically designed to give small changes. For fault analysis, the two inverters can be considered as controlled by the multi-loop structure in Figure 5.1 with constant v_0^* and ω^*.

As the voltage and current loops were chosen to be implemented in the NatRF (see Section 4.4.1), the equivalent inverter fault model depends on the type of fault. In the event of a 3ϕ fault both inverters switch to current control in all three phases, thus becoming equivalent to two current sources in parallel with an impedance and interconnected through Z_l. Using same fault modelling as the single inverter controlled in the NatRF, the equiv-

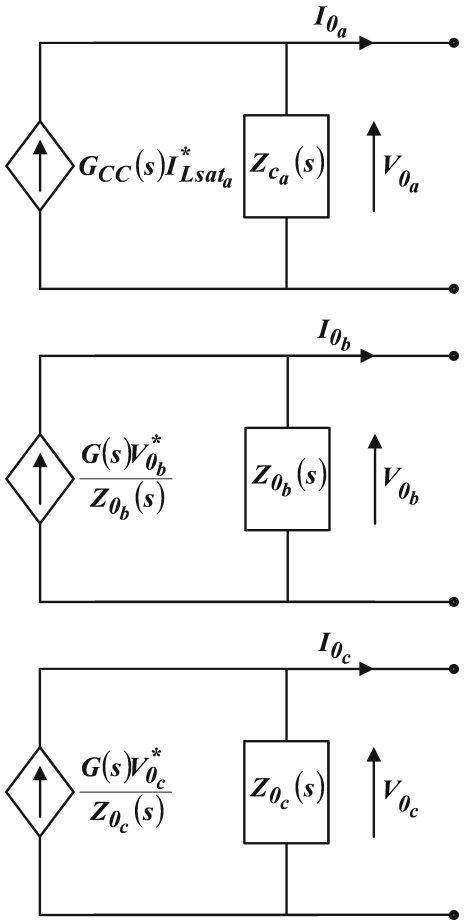


Figure 5.6: Equivalent phase networks, as current sources, of a three-phase four-leg phase inverter controlled in the NatRF for a $1\phi g$ fault

alent fault model of two parallel inverters is shown in Figure 5.7. Here it is assumed that the two inverters are of the same rating and control. Consequently, the reference inductor currents for each phase are equal ($I^*_{Lsat_{a1}} = I^*_{Lsat_{a2}}, I^*_{Lsat_{b1}} = I^*_{Lsat_{b2}}, I^*_{Lsat_{c1}} = I^*_{Lsat_{c2}}$), the parallel impedances are identical to Z_c and the closed loop transfer function G_{CC} is that of equation (5.10).

As the phase networks in Figure 5.7 are symmetrical and the inverters behave like balanced, positive sequence current sources, the model in Figure 5.7 can be expressed in sequence components as in Figure 5.8. It is interesting to note that if there was no interconnecting impedance Z_l, the two inverters would be equivalent in the positive sequence to a current source equal to $\frac{2G_{CC}I^*_{Lsat_p}Z_{c_p}}{Z_{c_p}+Z_{cc}}$ with a parallel impedance equal to $\frac{Z_{c_p}+Z_{cc}}{2}$. With the inverters connected before the coupling impedance Z_{cc}, the equivalent fault model would be made of a positive sequence current source twice $I^*_{Lsat_p}$ with a parallel impedance half Z_{c_p}.

In the event of a 2ϕ and a $2\phi g$ fault, the inverters switch to current control in the faulted phases. Therefore the inverters' fault models are derived like the one in Figure 5.5: the healthy phase is equivalent to a voltage source with a series impedance, the faulted phases are equivalent to a current source with a parallel impedance. All the parameters of these fault models should be derived as it has been done for the stand-alone inverter controlled in the NatRF.

The behaviour of parallel inverters for 1ϕ faults depends on the location of the fault. In Section 4.4.5 it has been shown that a 1ϕ fault at F_3 does not cause any current limiting in the inverters as the two inverters together are capable of supplying the required fault current. In this case, the control is not affected and the two inverters can be considered as two three-phase voltage sources in series with an impedance. Figure 5.9 shows the equivalent per-phase inverter fault model where $Z_{0_a}(s) = Z_{0_b}(s) = Z_{0_c}(s) = Z_0(s)$ and $G(s)$ is calculated as in (3.2). The voltage references for each inverter generated by the droop loops are different because of the presence of Z_l. However this difference can be neglected for a fault current calculation and therefore the two voltage sources are considered identical.

Figure 5.10 shows the equivalent sequence networks of the model in Figure 5.9. Depending on the type of regulator used in the voltage control loop of each phase, the two inverters can be capable of supplying a balanced positive sequence set of voltages or

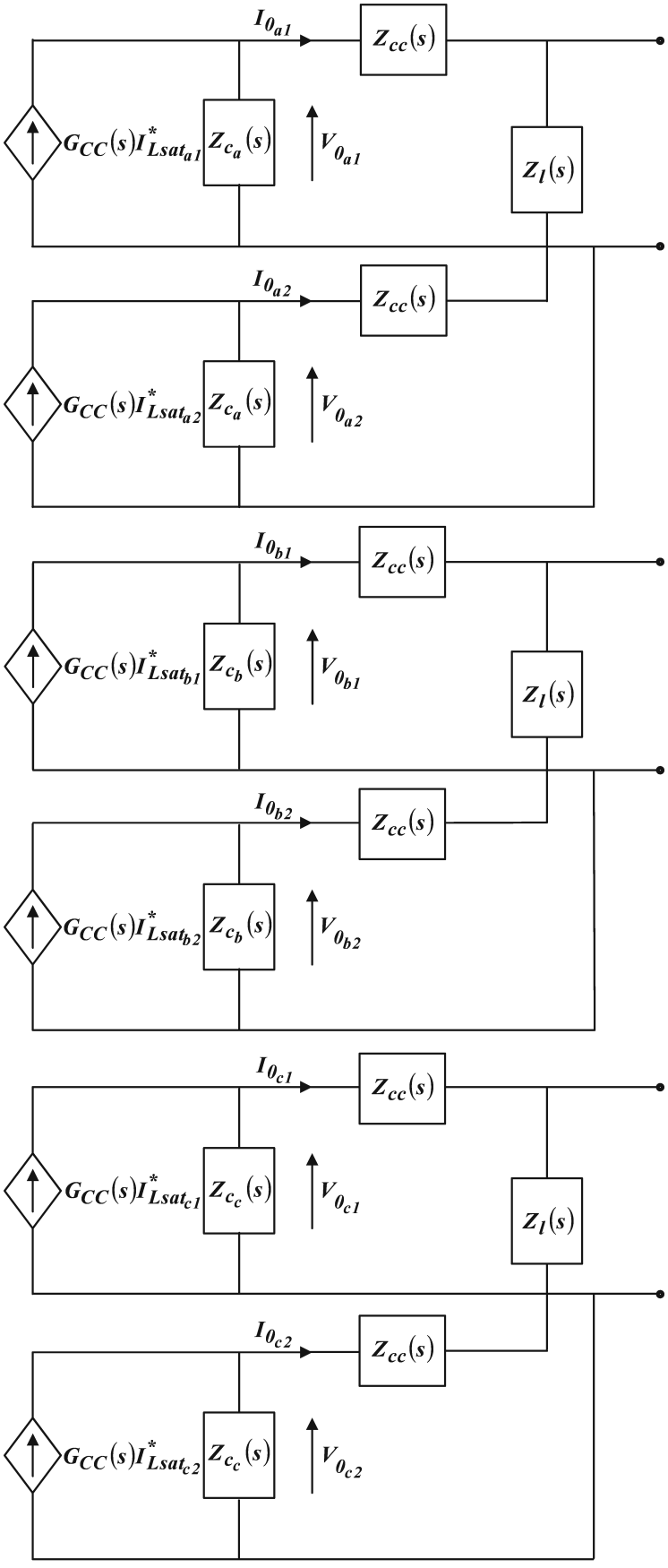


Figure 5.7: Equivalent phase networks of two parallel-connected inverters controlled in the NatRF for a 3ϕ fault at F_3

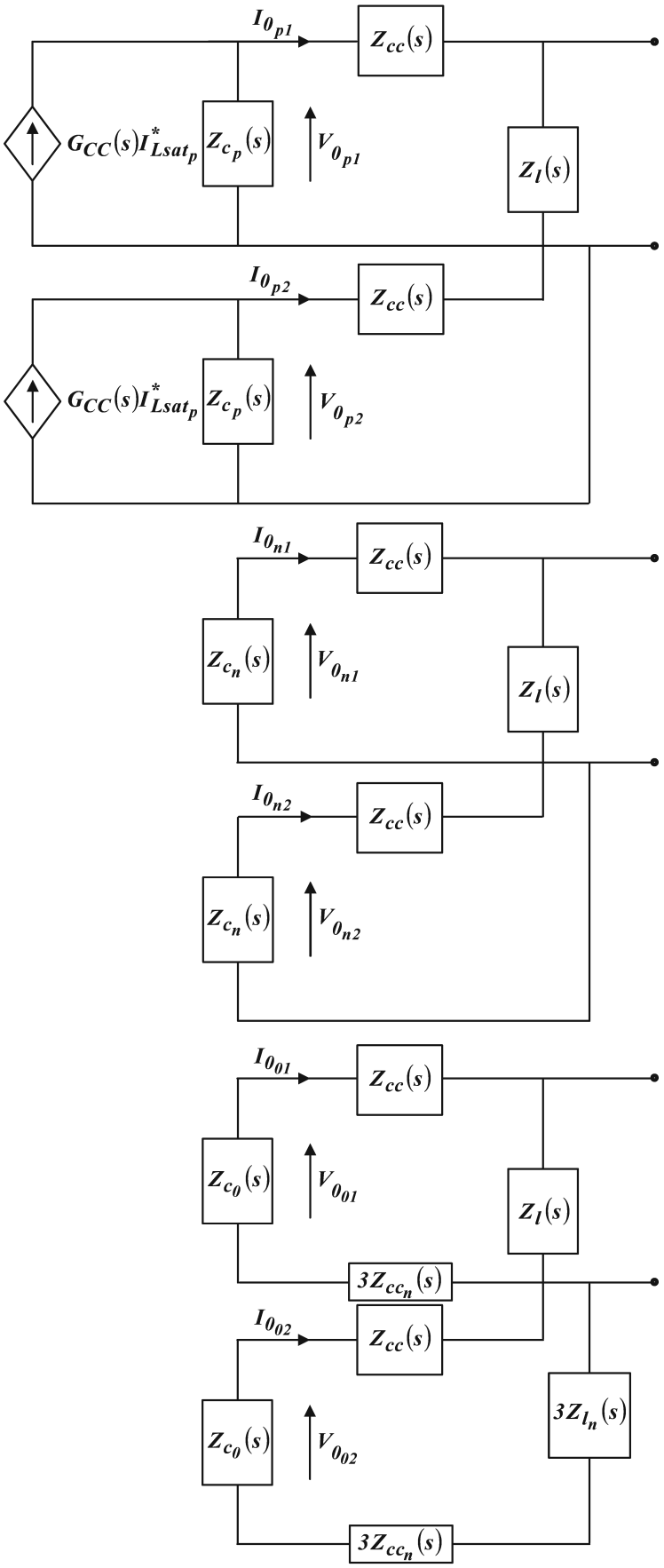


Figure 5.8: Equivalent sequence networks of two parallel-connected inverters controlled in the NatRF for a 3ϕ fault at F_3

not. Indeed, as discussed in Section 4.2.2, if P+Resonant regulators are used, then the negative and zero sequence components are suppressed and the inverters' output is not affected by unbalanced operation. On the contrary, if simple proportional regulators are used, then there will be a small negative and zero sequence component in v_0.

Single phase-to ground faults closer to inverters can cause current limiting in one or in both inverters. This asymmetric behaviour is caused by the inability of the droop control to share equally unbalanced loads. Indeed the $1\phi g$ can be seen as in increase in load in phase a which is not equally shared by the two inverters. As a result, the current limit is triggered in one inverter while the other one is still voltage controlled. Nevertheless the methodology and modelling approach used here can still be used to model this particular behaviour and the resulting model of the two inverters is shown in Figure 5.11.

5.2 Fault analysis studies in a microgrid

From a first qualitative description given in Section 5.1, the fault models for stand-alone and parallel-connected inverters seem to agree with the behaviour shown during the PSCAD simulations. However a more rigorous quantitative validation of these models has to be done. Here it is chosen to validate these models by comparing the results obtained from the time-domain simulations in PSCAD with the ones obtained by using the models in numerical fault analysis.

Although the proposed fault models have been derived in the frequency-domain, here they are considered as quasi steady-state models that are valid after the initial fault transient settles until the fault clears or until the inverter is disconnected because the fault has not cleared within the expected time. The models are computed at the system frequency (50Hz) and then integrated into a quasi steady-state fault analysis.

The traditional fault analysis technique based on sequence components cannot be applied to both SynRF and NatRF inverter fault models as it relies on a network whose only point of unbalance is the fault. Some equivalent models of the inverter controlled in the NatRF are asymmetrical and therefore sequence components fault analysis cannot be used for these cases. It can only be used with balanced inverter fault models such the ones in Figures 5.4, 5.8 and 5.10. Sequence components-based fault analysis in inverter-only microgrids is proposed in [84]. Section 5.3 illustrates how to perform these calculations and then compares the results obtained with those obtained from PSCAD.

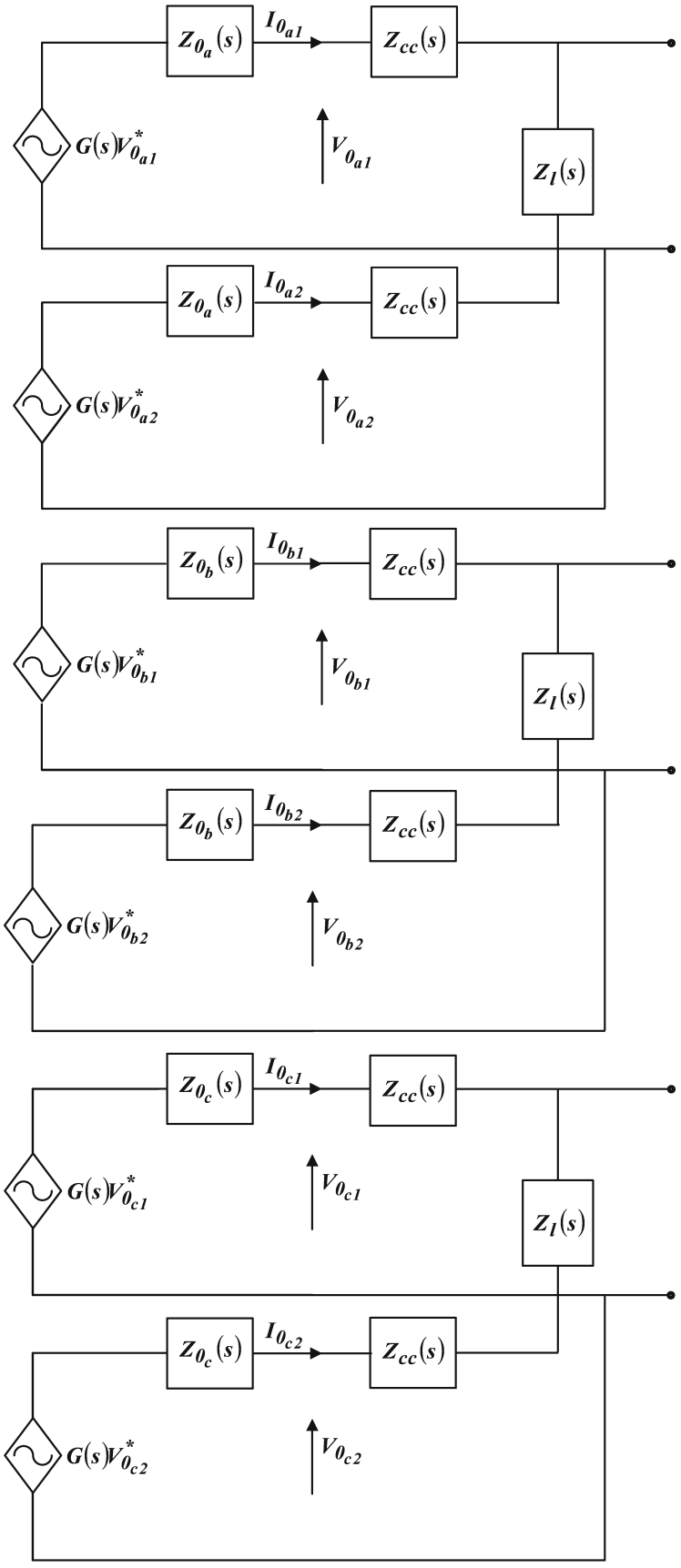


Figure 5.9: Equivalent phase networks of two parallel-connected inverters controlled in the NatRF for a $1\phi g$ fault at F_3

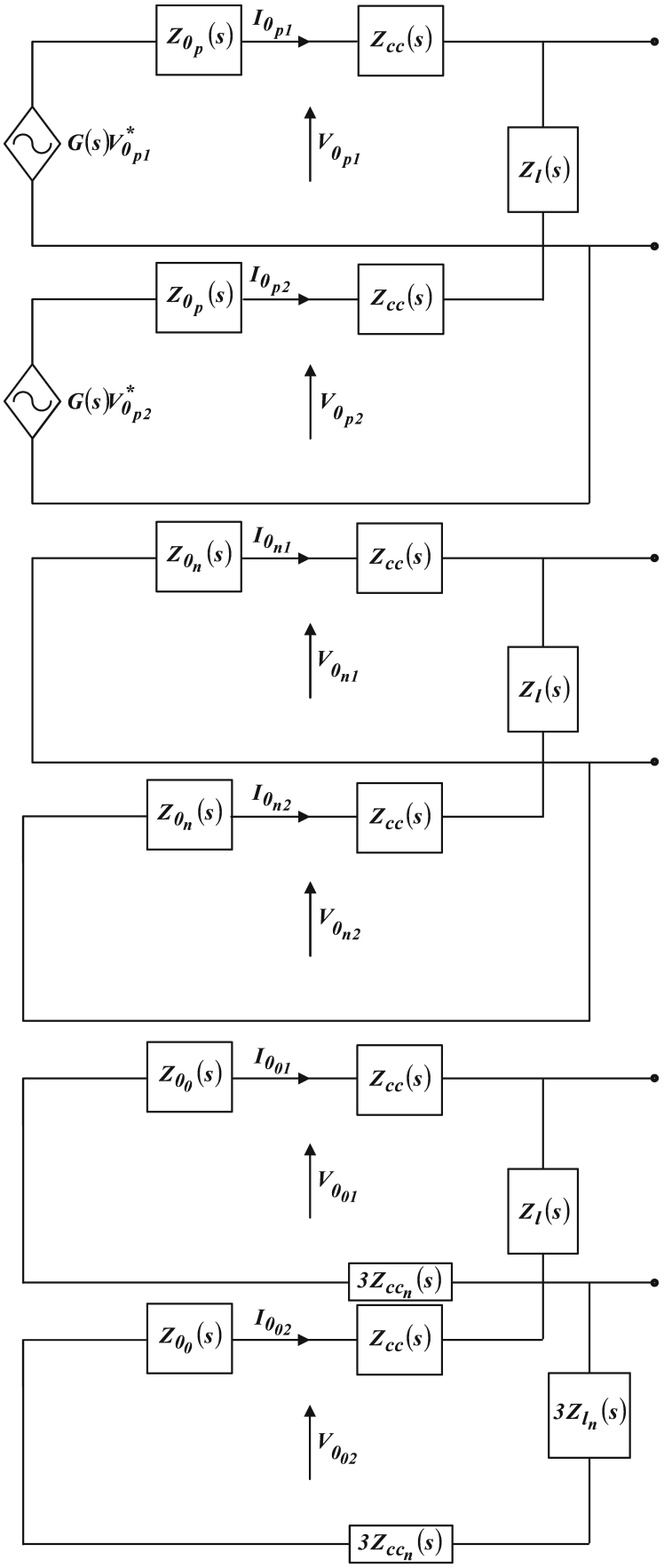


Figure 5.10: Equivalent sequence networks of two parallel-connected inverters controlled in the NatRF for a $1\phi g$ fault at F_3

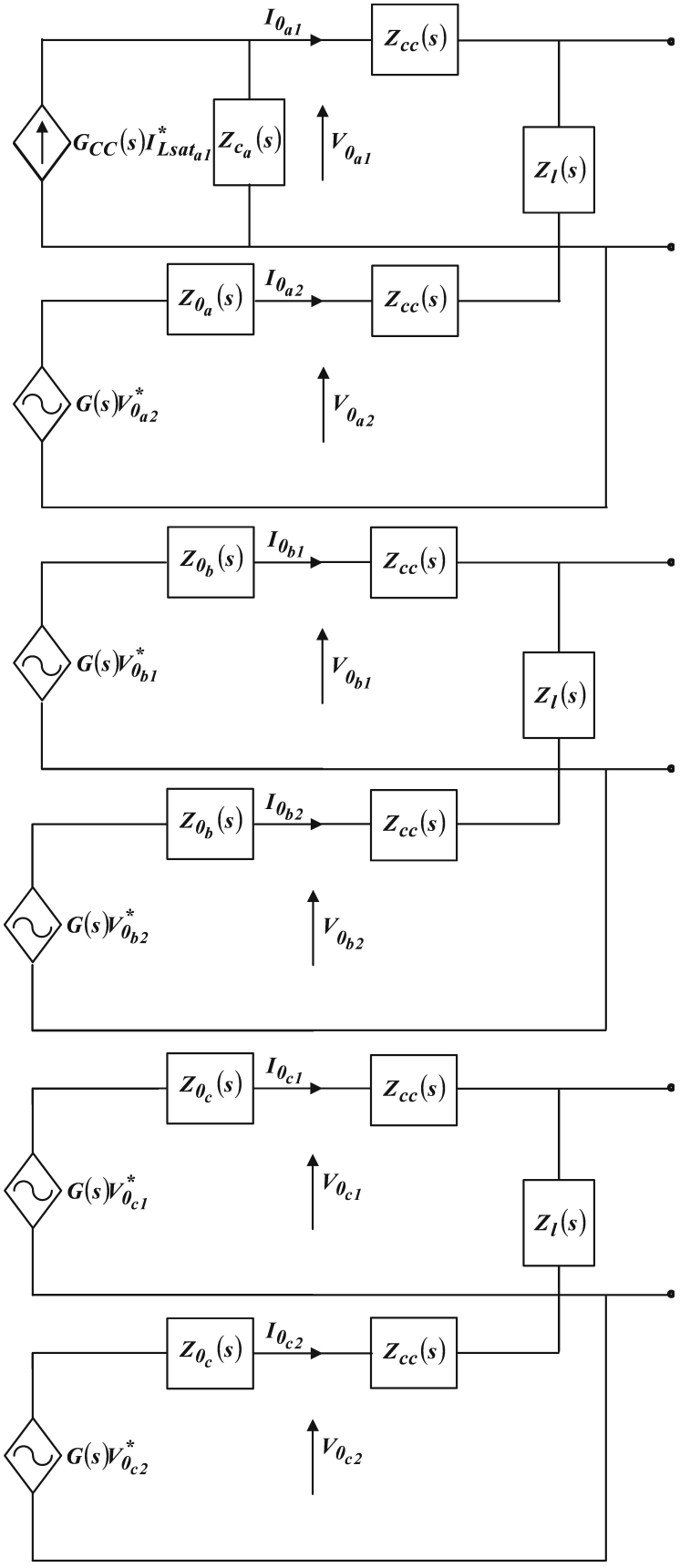


Figure 5.11: Equivalent phase networks of two parallel-connected inverters controlled in the NatRF for a $1\phi g$ fault at F_1

As not all developed fault models are symmetrical, a more general fault analysis approach which can be used with any kind of model, including the ones in Figures 5.5 and 5.11, has to be found. For this purpose, in [85] the microgrid fault behaviour is analyzed using a circuit analysis approach where an equivalent direct phase coordinate representation of the network is constructed. Figure 5.12 shows a circuit which represents all the impedances in the microgrid supplied by one inverter, see Figure 3.19, including the parallel impedances (Z_{i_a}, Z_{i_b} and Z_{i_c}) of a generic inverter model. This circuit can be represented by an equivalent bus impedance matrix Z_{BUS} based on an explicit representation of every node in the network including the neutral and the ground connections. After Z_{BUS} is determined, then the system behaviour is described by the standard relationship:

$$V = Z_{BUS} I \tag{5.13}$$

where V are the node voltages referred to the reference node and I are the currents entering the nodes from the current sources. Voltage and current are expressed in phase quantities as the bus impedance matrix is built by considering each single node in the network.

In the event of a fault, equation (5.13) gives a complete description of the system under study and can be used to calculate the voltages and currents in the microgrid. The first step in this calculation involves modifying the original Z_{BUS} to form a new matrix Z_{BUSnew} incorporating the network modifications introduced by the fault. Then the node voltages can be determined from (5.13) where the injected currents correspond to the equivalent current sources derived in the inverter models.

This general approach is directly applicable to microgrids supplied by two or more inverters. Figure 5.13 shows the equivalent circuit in per-phase quantities of the two-inverter microgrid of Figure 3.20. In this case the number of injected currents is increased compared with the stand-alone case.

Section 5.4 shows how this fault analysis approach together with the developed inverter fault models can be applied to the study of the microgrid fault behaviour. The models for the stand-alone inverter controlled in the SynRF and in the NatRF and the models for two parallel-connected inverters are considered and each of them is studied under the influence of a 3ϕ and a $1\phi g$ fault. Worked examples are given in order to show how to perform fault analysis. Numerical results are then compared with the ones obtained from the simulations in PSCAD.

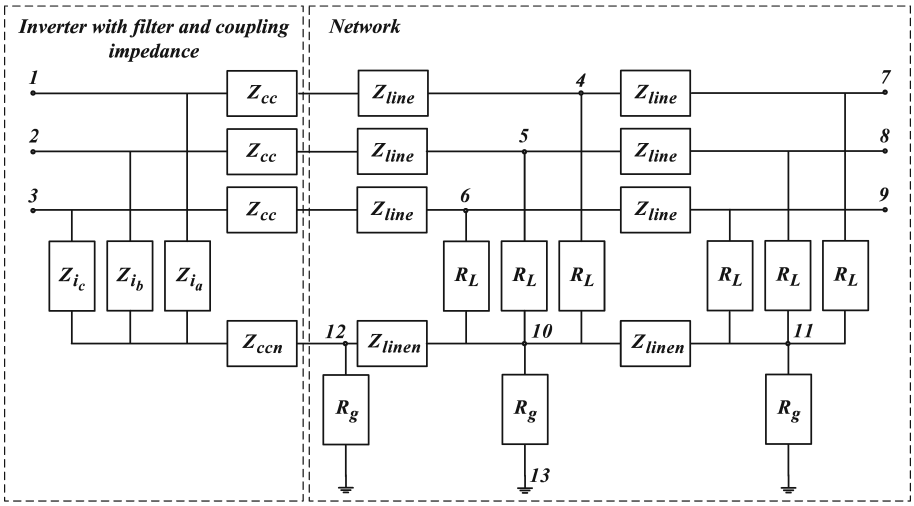


Figure 5.12: Equivalent per-phase circuit representation of the microgrid, including the parallel impedances of the inverter.

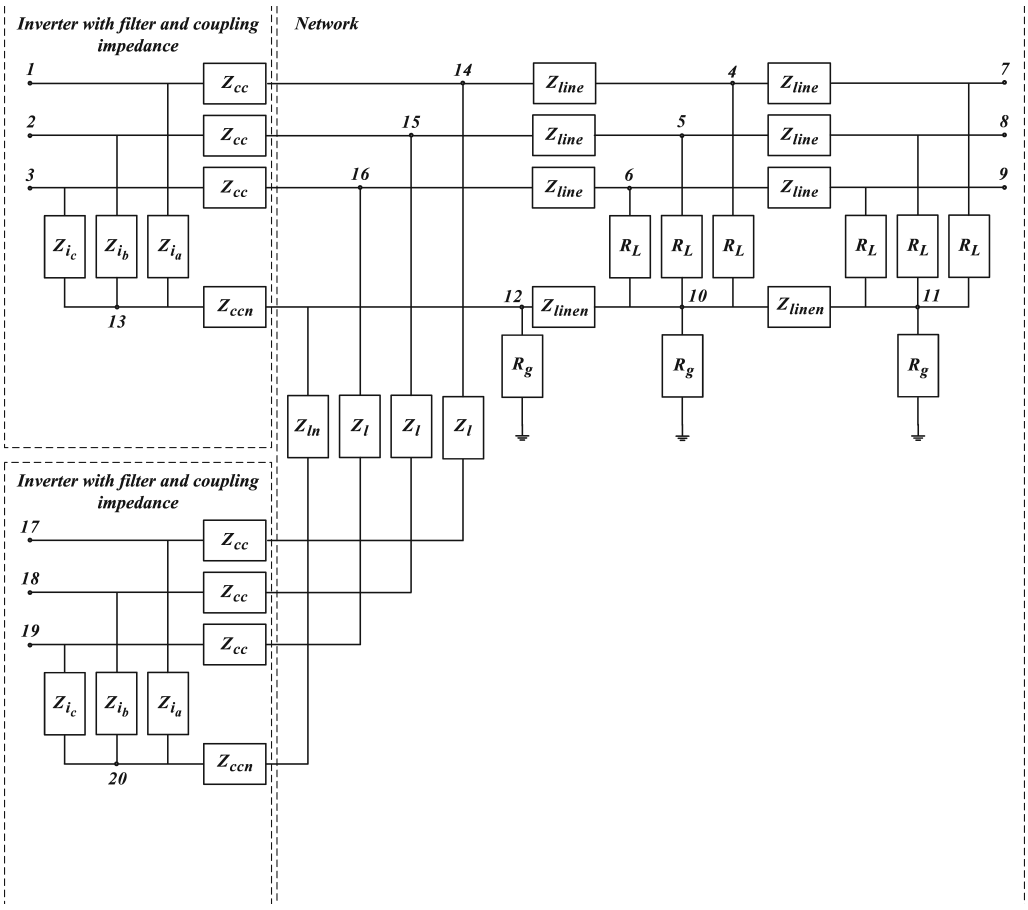


Figure 5.13: Equivalent per-phase circuit representation of the microgrid supplied by two inverters

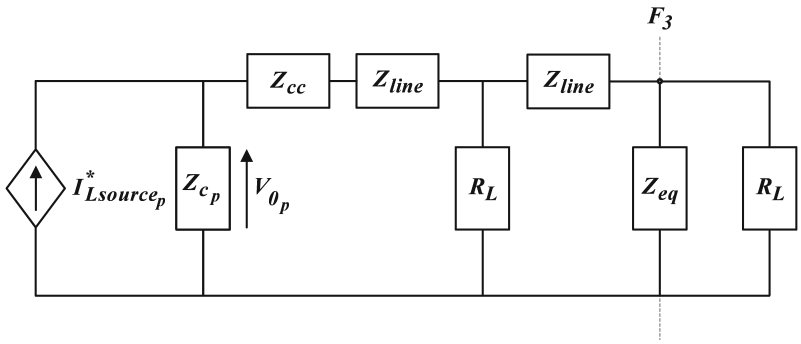


Figure 5.14: Equivalent circuit for fault analysis studies based on sequence components for a microgrid supplied by a stand-alone inverter

5.3 Fault analysis in sequence components

In fault analysis based on sequence components, the starting point is the representation of the system (in this case, the microgrid) using three equivalent circuits, one for each component. In systems where the only point of unbalance is the fault, the three circuits are de-coupled but are inter-connected at the fault point in a way which depends on the type of fault. A microgrid supplied by a stand-alone inverter controlled in the SynRF, see Figure 3.19, can be represented in sequence components as in Figure 5.14. Here the inverter is represented as a positive sequence current source $I^*_{Lsouce_p} = I^*_{Lsat_p}$ with a parallel impedance in accordance with the developed model in Figure 5.4. The circuit in Figure 5.14 contains also the microgrid network parameters and the microgrid equivalent negative and zero sequence circuits are reduced to an equivalent impedance Z_{eq} connected at the fault point. The inverter negative and zero sequence impedances Z_{c_n} and Z_{c_0} in the model of Figure 5.4 are included in the negative and zero sequence circuits and therefore taken into account when calculating Z_{eq}. It should be noted that the inverter parallel impedances $Z_{c_p}(s)$, $Z_{c_n}(s)$ and $Z_{c_0}(s)$ have now to be evaluated for $s = j\omega$ where ω is the system angular frequency.

The value of Z_{eq} depends on the type of fault and therefore on the way the sequence networks are connected. Table 5.1 summarizes the values of Z_{eq} for different faults. Z_n and Z_0 are the equivalent negative and zero sequence impedances of the microgrid seen from the fault point.

Once the injected current $I^*_{Lsource_p}$ and the equivalent fault impedance Z_{eq} are known, then the sequence components of voltages and currents can be determined and

Table 5.1: Equivalent Fault Impedances

	$3\phi Fault$	$2\phi Fault$	$2\phi gFault$	$1\phi gFault$
Z_{eq}	0	Z_n	$\frac{Z_n Z_0}{Z_n+Z_0}$	$Z_n + Z_0$

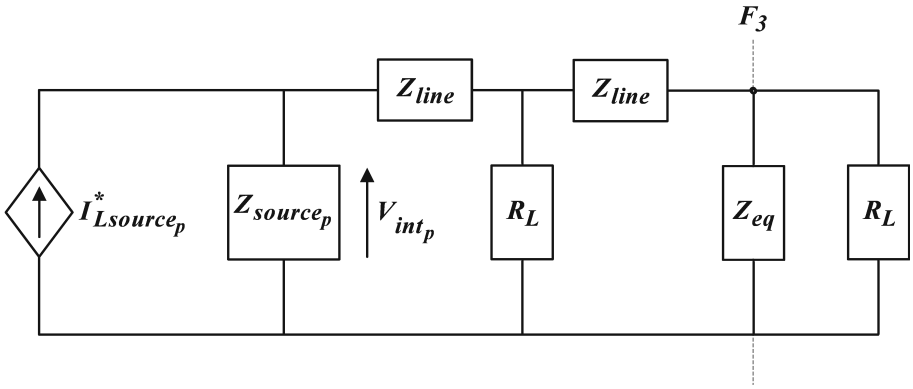


Figure 5.15: Equivalent circuit for fault analysis studies based on sequence components for a microgrid supplied by two parallel-connected inverters

from them, the resulting phase quantities can be determined as well.

This approach to fault analysis can also be used with a microgrid supplied by two inverters, see Figure 3.5, for 3ϕ faults and $1\phi g$ faults which do not cause any current limiting. Indeed the equivalent inverters' fault models are symmetrical circuits as shown in Figures 5.8 and 5.10. The equivalent circuit for this microgrid is shown in Figure 5.15 where for a 3ϕ fault

$$I^*_{Lsource_p} = \frac{G_{CC} I^*_{Lsat_{p1}} Z_{c_p}}{Z_{c_p} + Z_{cc}} + \frac{G_{CC} I^*_{Lsat_{p2}} Z_{c_p}}{Z_{c_p} + Z_{cc} + Z_l} \tag{5.14}$$

$$Z_{source_p} = (Z_{c_p} + Z_{cc}) \| (Z_{c_p} + Z_{cc} + Z_l) \tag{5.15}$$

$$Z_{eq} = 0 \tag{5.16}$$

and for a $1\phi g$ fault

$$I^*_{Lsource_p} = \frac{G V^*_{0_{p1}}}{Z_{0_p} + Z_{cc}} + \frac{G V^*_{0_{p2}}}{Z_{0_p} + Z_{cc} + Z_l} \tag{5.17}$$

$$Z_{source_p} = (Z_{0_p} + Z_{cc}) \| (Z_{0_p} + Z_{cc} + Z_l) \tag{5.18}$$

$$Z_{eq} = Z_n + Z_0 \tag{5.19}$$

It is assumed that $V^*_{0_{p1}} = V^*_{0_{p2}} = V^*_0$ as the effect of the voltage droop loop is not considered.

The four case studies that follow show how to use the inverter models in sequence-component–based fault analysis for a 3ϕ and a $1\phi g$ fault. Numerical results are then compared with the ones obtained from PSCAD simulations.

Case 1: 3ϕ fault (microgrid supplied by a single inverter controlled in the SynRF)

A bolted 3ϕ fault is considered at point F_3, see Figure 3.19. This type of fault does not introduce any unbalance in the network and therefore only positive sequence voltages and currents are present. The equivalent circuit in Figure 5.14, where Z_{eq} is equal to zero, can be reduced to a simpler network with a current source and a parallel impedance. The voltage across the impedance is the positive sequence component of the output voltage v_0. Substituting the numerical values of the microgrid impedances yields the equivalent parallel impedance for this fault

$$\mathtt{Z}_{\mathtt{p}_3} = (0.76 + \mathtt{j}0.28)\Omega \tag{5.20}$$

and the injected positive sequence current is

$$\mathtt{I}^{*}_{\mathtt{Lsource}_\mathtt{p}} = (45.86 - \mathtt{j}7.34)\mathtt{A} \tag{5.21}$$

The positive sequence component of the output voltage is given by the product:

$$\mathtt{V}_{0_\mathtt{p}} = (45.86 - \mathtt{j}7.34) * (0.76 + \mathtt{j}0.28) = (37.14 + \mathtt{j}7.61)\mathtt{V} = 37.91\angle 11.58^{\circ}\mathtt{V} \tag{5.22}$$

From here all the electrical quantities in the microgrid under fault conditions can be determined. Multiplying the voltage magnitude in (5.22) by $\sqrt{2}$, gives a value of 53.61 V which then can be compared with the peak positive sequence component of the output voltage obtained from the PSCAD simulation and shown in Figure 5.16. As it can be seen, the simplified inverter model is effective in analyzing the faulted microgrid.

Case 2: $1\phi g$ fault (microgrid supplied by a single inverter controlled in the SynRF)

A similar calculation can be performed for a $1\phi g$ fault applied at point F_3. From Table 5.1 the equivalent fault impedance Z_{eq} is given by the sum of Z_n and Z_0. The three

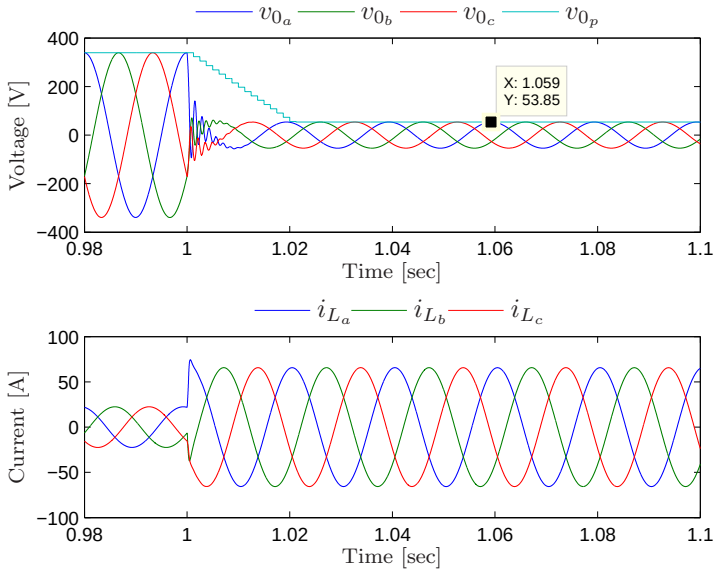


Figure 5.16: Inverter output voltage (v_0) and inductor current (i_L) during a 3ϕ fault in a microgrid supplied by a single inverter controlled in the SynRF

impedances are found to be:

$$\mathtt{Z_n} = (14.27 - \mathtt{j}3.27)\Omega \tag{5.23}$$

$$\mathtt{Z_0} = (24.33 - \mathtt{j}3.44)\Omega \tag{5.24}$$

$$\mathtt{Z_{eq}} = (38.60 - \mathtt{j}6.72)\Omega \tag{5.25}$$

From here the system becomes equivalent to a current source $I^*_{Lsource_p}$ with a parallel impedance given by:

$$\mathtt{Z_{p_{ig}}} = (10.96 - \mathtt{j}2.22)\Omega \tag{5.26}$$

The positive sequence component of v_0 is then given by:

$$\mathtt{V_{0_p}} = (45.86 - \mathtt{j}7.34) * (10.96 - \mathtt{j}2.22) = (486.49 - \mathtt{j}182.44)\mathtt{V} = 519.57\angle - 20.55^\circ\mathtt{V} \tag{5.27}$$

From (5.27) the peak value of V_{0_p} is 734.78 V. This value can be compared with the one obtained from the PSCAD simulation and shown in Figure 5.17. The mathematical model of the inverter together with the sequence-component–based fault analysis follows quite well the behaviour of the faulted microgrid simulated in PSCAD.

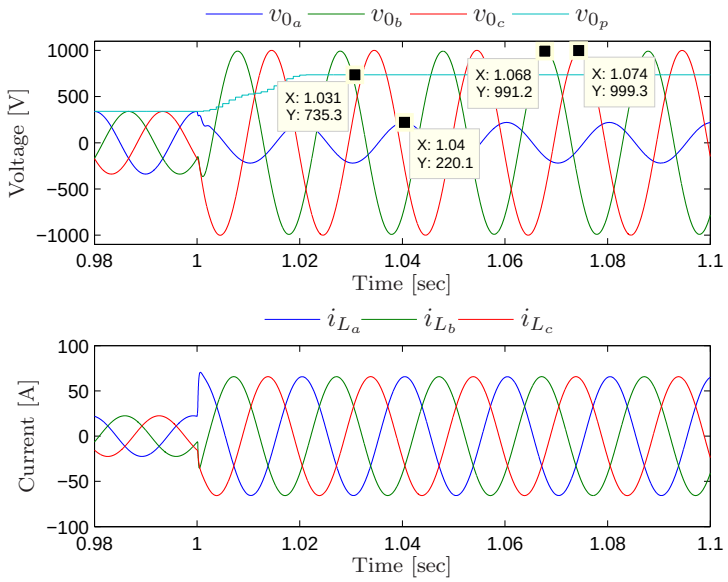


Figure 5.17: Inverter output voltage (v_0) and inductor current (i_L) during a $1\phi g$ fault in a microgrid supplied by a single inverter controlled in the SynRF

Case 3: 3ϕ fault (microgrid supplied by two parallel-connected inverters)

A 3ϕ fault is applied at the same point F_3 in a microgrid supplied by two inverters. As the fault is symmetrical there are no positive and negative sequence components to be considered and Z_{eq} is equal to zero. The inverters' fault model which has to be used is the one in Figure 5.8. Voltage and current control loops are implemented in the NatRF, therefore G_{CC} is calculated according to (5.10) and each inverter supplies a current of 47.07 A.

Equations (5.14) and (5.15) give the equivalent current source and parallel impedance of the inverter (see Figure 5.15)

$$\mathtt{I}^{*}_{\mathtt{Lsource_p}} = (\mathtt{93.57} - \mathtt{j3.11})\mathtt{A} \tag{5.28}$$

$$\mathtt{Z}_{\mathtt{source_p}} = (\mathtt{0.0976} - \mathtt{j31.76})\Omega \tag{5.29}$$

As expected, the two inverters are equivalent to a current source of twice the capacity of a single inverter and a parallel impedance half the original Z_c, except for a small difference caused by Z_l. The equivalent impedance including the network and Z_{source_p} is

$$\mathtt{Z}_{\mathtt{p_3}} = (\mathtt{0.73} + \mathtt{j0.17})\Omega \tag{5.30}$$

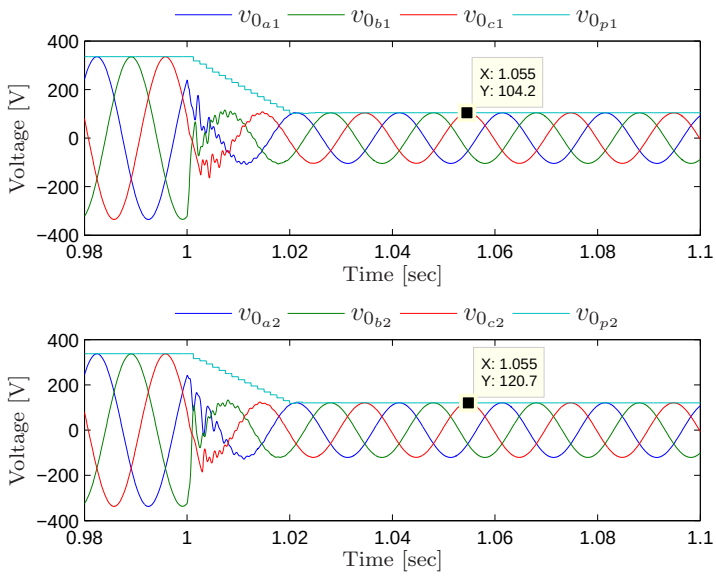


Figure 5.18: Inverter output voltages (v_{0_1}, v_{0_2}) during a 3ϕ fault in a microgrid supplied by two parallel-connected inverters

The positive sequence component of the voltage at the inverters' connection point is:

$$\mathtt{V_{int_p}} = (69.29 + \mathtt{j}13.64)\mathtt{V} = 70.62\angle 11.14^{\circ}\mathtt{V} \tag{5.31}$$

From here the positive sequence components of the inverter output voltage are derived as:

$$\mathtt{V_{0_{p1}}} = (70.98 + \mathtt{j}18.73)\mathtt{V} = 73.41\angle 14.78^{\circ}\mathtt{V} \tag{5.32}$$

$$\mathtt{V_{0_{p2}}} = (82.07 + \mathtt{j}22.53)\mathtt{V} = 85.11\angle 15.35^{\circ}\mathtt{V} \tag{5.33}$$

The peak values of $V_{0_{p1}}$ and $V_{0_{p2}}$ are 103.81 V and 120.36 V respectively. They compare well with the ones obtained from the fault simulation in PSCAD and shown in Figure 5.18.

Case 4: $1\phi g$ fault (microgrid supplied by two parallel-connected inverters)

A $1\phi g$ fault is applied at point F_3. For this type of fault the model for the inverters to be used is the one in Figure 5.10 where $G(s)$ and $Z_0(s)$ are calculated at the fundamental frequency according to (3.2) and (3.3) and equal to:

$$\mathtt{Z_0(j50)} = (0.09 + \mathtt{j}0.23)\Omega \tag{5.34}$$

$$\mathtt{G(j50)} = (0.98 - \mathtt{j}0.12). \tag{5.35}$$

From equations (5.14) and (5.18) the inverters' equivalent current source and impedance are:

$$\mathtt{I}^{*}_{\mathtt{Lsource_p}} = (351.22 - \mathtt{j}999.93) \tag{5.36}$$

$$\mathtt{Z}_{\mathtt{source_p}} = (0.10 + \mathtt{j}0.19)\Omega \tag{5.37}$$

The negative and zero sequence impedance and the resulting equivalent impedance are equal to

$$\mathtt{Z_n} = (0.80 + \mathtt{j}0.36)\Omega \tag{5.38}$$

$$\mathtt{Z_0} = (10.88 - \mathtt{j}0.79)\Omega \tag{5.39}$$

$$\mathtt{Z_{eq}} = (11.69 - \mathtt{j}0.43)\Omega \tag{5.40}$$

Once Z_{eq} is known from Figure 5.15, the total parallel impedance with $I^{*}_{Lsource_p}$ and the resulting positive sequence component of the interconnection voltage are found to be

$$\mathtt{Z}_{\mathtt{p_{1g}}} = (0.1048 + \mathtt{j}0.196)\Omega \tag{5.41}$$

$$\mathtt{V}_{\mathtt{int_p}} = (232.79 - \mathtt{j}3.59)\mathtt{V} = 235.55\angle - 8.78^{\circ}\mathtt{V} \tag{5.42}$$

Finally the positive sequence components of the inverters' output voltages are calculated as:

$$\mathtt{V}_{\mathtt{0_{p1}}} = (234.02 - \mathtt{j}3.40)\mathtt{V} = 236.48\angle - 8.27^{\circ}\mathtt{V} \tag{5.43}$$

$$\mathtt{V}_{\mathtt{0_{p2}}} = (236.1 - \mathtt{j}3.31)\mathtt{V} = 238.41\angle - 7.99^{\circ}\mathtt{V} \tag{5.44}$$

The corresponding peak values of $V_{0_{p1}}$ and $V_{0_{p2}}$ are 334.43 V and 337.16 V. They well compare with the ones in Figure 5.19. This validates the developed fault model and also the choice of neglecting the action of the voltage droop function.

5.4 Fault analysis in direct phase coordinates

The four case studies presented in the previous section give good results in accordance with the simulations, however this methodology based on sequence components cannot be applied to all inverter fault models. On the contrary, fault analysis based on direct phase coordinates can be generally applied to any inverter fault model independently of the symmetry of the models. The next seven case studies show how to perform fault analysis calculations in phase coordinates and then compare the obtained numerical results with the ones obtained from PSCAD.

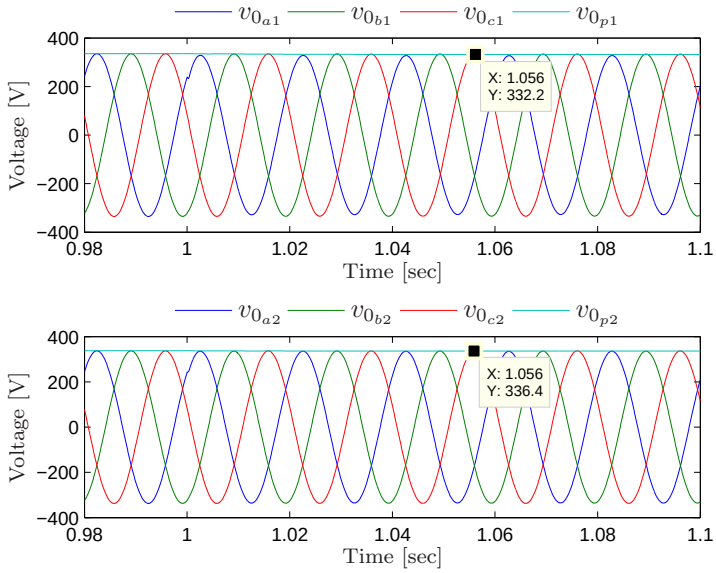


Figure 5.19: Inverter output voltages (v_{0_1}, v_{0_2}) during a $1\phi g$ fault in a microgrid supplied by two parallel-connected inverters

5.4.1 Microgrid supplied by a single inverter controlled in the SynRF

The inverter model in Figure 5.3 is made of three identical phase circuits whose injected current values and parallel impedances are

$$\mathtt{G_{CC}(j50)} = \mathtt{1} \tag{5.45}$$

$$\mathtt{Z_{c_a}(j50)} = \mathtt{Z_{c_b}(j50)} = \mathtt{Z_{c_c}(j50)} = (\mathtt{0.05} - \mathtt{j63.69})\Omega \tag{5.46}$$

$$\mathtt{G_{CC}(j50)I^*_{Lsat_a}} = \mathtt{I_1} = (\mathtt{45.86} - \mathtt{j7.34})\mathtt{A} \tag{5.47}$$

$$\mathtt{G_{CC}(j50)I^*_{Lsat_b}} = \mathtt{I_2} = (\mathtt{-29.29} - \mathtt{j36.04})\mathtt{A} \tag{5.48}$$

$$\mathtt{G_{CC}(j50)I^*_{Lsat_c}} = \mathtt{I_3} = (\mathtt{-16.57} + \mathtt{j43.39})\mathtt{A} \tag{5.49}$$

So from Figure 5.12, the parallel inverter impedances are given by

$$\mathtt{Z_{i_a}(j50)} = \mathtt{Z_{i_b}(j50)} = \mathtt{Z_{i_c}(j50)} = (\mathtt{0.05} - \mathtt{j63.69})\Omega \tag{5.50}$$

The next step is to modify the original Z_{BUS} of the network in Figure 5.12 to incorporate the effects of the different types of fault and then determine how the injected inverter currents set the voltages in the faulted network.

Case 1: 3ϕ fault (microgrid supplied by a single inverter controlled in the SynRF)

A 3ϕ fault applied at point F_3 in Figure 3.19 introduces an extra connection between nodes 7, 8, 9 and earth in Figure 5.12. After the modified matrix Z_{BUSnew} is determined, using the injected node currents, it is possible from (5.13) to determine the node voltages during the fault. For example, the inverter phase output voltages in RMS form can be determined as:

$$\mathtt{V_1} = \mathtt{Z_{11}I_1} + \mathtt{Z_{12}I_2} + \mathtt{Z_{13}I_3} = \mathtt{37.91\angle 11.59^\circ V} \tag{5.51}$$

$$\mathtt{V_2} = \mathtt{Z_{21}I_1} + \mathtt{Z_{22}I_2} + \mathtt{Z_{23}I_3} = \mathtt{37.91\angle -108.41^\circ V} \tag{5.52}$$

$$\mathtt{V_3} = \mathtt{Z_{31}I_1} + \mathtt{Z_{32}I_2} + \mathtt{Z_{33}I_3} = \mathtt{37.91\angle 131.59^\circ V} \tag{5.53}$$

where $V_{0_a} = V_1$, $V_{0_b} = V_2$ and $V_{0_c} = V_3$ are the inverter output phase voltages and Z_{ij}, with $i = 1, 2, 3$ and $j = 1, 2, 3$, are elements of Z_{BUSnew}. The corresponding peak values are equal to 53.61 V and compare well with the peak phase voltages of 53.85 V obtained from the PSCAD simulation and shown in Figure 5.16. Again, the quasi steady-state fault analysis and the inverter model are effective in describing the microgrid fault behaviour.

Case 2: $1\phi g$ fault (microgrid supplied by a single inverter controlled in the SynRF)

A $1\phi g$ fault is applied at point F_3. In this case Z_{BUS} is modified by an extra connection between node 7 and earth. By using the same inverter model, the inverter output phase voltages in RMS form are determined as:

$$\mathtt{V_1} = \mathtt{Z_{11}I_1} + \mathtt{Z_{12}I_2} + \mathtt{Z_{13}I_3} = \mathtt{155.48\angle -6.37^\circ V} \tag{5.54}$$

$$\mathtt{V_2} = \mathtt{Z_{21}I_1} + \mathtt{Z_{22}I_2} + \mathtt{Z_{23}I_3} = \mathtt{699.74\angle -142.49^\circ V} \tag{5.55}$$

$$\mathtt{V_3} = \mathtt{Z_{31}I_1} + \mathtt{Z_{32}I_2} + \mathtt{Z_{33}I_3} = \mathtt{705.75\angle 98.34^\circ V} \tag{5.56}$$

These RMS voltage values multiplied by $\sqrt{2}$ become 219.88 V, 989.58 V and 998.08 V. They compare well with the simulated peak voltages obtained from PSCAD of 220.1 V, 991.2 V and 999.3 V respectively, as shown in Figure 5.17 (the simulation assumed a high enough DC-link voltage to obtain these phase voltages). This provides confirmation of the effectiveness of the proposed model under unbalanced faults.

5.4.2 Microgrid supplied by a single inverter controlled in the NatRF

As previously discussed, the inverter model in Figure 5.6 is formed by three unbalanced elements where the values of the injected phase currents and the parallel output impedances depend on which inverter phases current limit as a result of the fault. Therefore no general inverter fault model can be considered and each fault case study requires its own inverter model. The next two sections show how to obtain the inverter fault model and how to integrate it into a quasi steady-state fault analysis of the microgrid.

Case 3: 3ϕ fault (microgrid supplied by a single inverter controlled in the NatRF)

A bolted three-phase fault is applied at point F_3 in Figure 3.19 at a time t=1 s. The control strategy of the three phases is switched to current control and for each phase the inverter supplies a fault current equal to 47.07 A. Before calculating the new bus impedance matrix Z_{BUSnew}, the equivalent fault model of the inverter has to be calculated. By using the filter parameters and the control gains, G_{CC}, Z_0 and G are expressed at the fundamental frequency as:

$$\mathtt{G_{CC}(j50)} = (\mathtt{0.99} - \mathtt{j0.03}) \tag{5.57}$$

$$\mathtt{Z_0(j50)} = (\mathtt{0.09} + \mathtt{j0.23})\Omega \tag{5.58}$$

$$\mathtt{G(j50)} = (\mathtt{0.98} - \mathtt{j0.12}) \tag{5.59}$$

So with these values, the three equivalent current sources and three parallel impedances are found to be:

$$\mathtt{Z_{c_a}(j50)} = \mathtt{Z_{c_b}(j50)} = \mathtt{Z_{c_c}(j50)} = (\mathtt{0.05} - \mathtt{j63.69})\Omega \tag{5.60}$$

$$\mathtt{G_{CC}(j50)} * \mathtt{I^*_{Lsat_a}} = \mathtt{I_1} = (\mathtt{46.67} - \mathtt{j1.44})\mathtt{A} \tag{5.61}$$

$$\mathtt{G_{CC}(j50)} * \mathtt{I^*_{Lsat_b}} = \mathtt{I_2} = (-\mathtt{24.59} - \mathtt{j39.7})\mathtt{A} \tag{5.62}$$

$$\mathtt{G_{CC}(j50)} * \mathtt{I^*_{Lsat_c}} = \mathtt{I_3} = (-\mathtt{22.08} + \mathtt{j41.14})\mathtt{A} \tag{5.63}$$

Now the original bus impedance matrix of the network in Figure 5.12 has to be modified in order to take into account the network modification introduced by the fault, which is an extra connection between nodes 7, 8, 9 and earth, see Figure 5.12. After Z_{BUSnew} is formed, the node voltages of the system can be easily determined by considering the current injection of the inverter. For example, the output voltage of the inverter for each

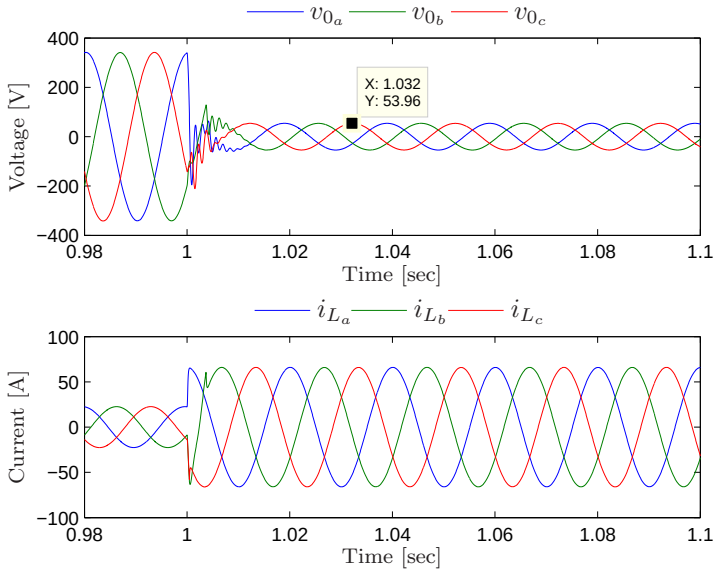


Figure 5.20: Inverter output voltage (v_0) and inductor current (i_L) during a 3ϕ fault in a microgrid supplied by a single inverter controlled in the NatRF

phase can be found as:

$$\mathtt{V}_1 = 38.11\angle 18.91^\circ \mathtt{V} \tag{5.64}$$

$$\mathtt{V}_2 = 38.11\angle -101.09^\circ \mathtt{V} \tag{5.65}$$

$$\mathtt{V}_3 = 38.11\angle 138.91^\circ \mathtt{V} \tag{5.66}$$

Their corresponding peak voltage magnitude is equal to 53.89 V. The same fault has been simulated in PSCAD and the peak values of the inverter output phase-to-neutral voltages of 53.96 V are shown in Figure 5.20. Again, the model reflects quite well the results of the simulation.

Case 4: $1\phi g$ fault (microgrid supplied by a single inverter controlled in the NatRF)

A $1\phi g$ fault is applied at point F_3. As a result of the control strategy, phase a becomes current controlled while the control of phases b and c is unchanged. By using the values of $G_{CC}(j50)$, $Z_0(j50)$ and $G(j50)$ calculated for the three-phase fault, the equivalent inverter

current sources and parallel impedances are found to be:

$$\mathtt{Z}_{\mathtt{c_a}}(\mathtt{j50}) = (\mathtt{0.05} - \mathtt{j63.69})\Omega \tag{5.67}$$

$$\mathtt{Z}_{\mathtt{0_b}}(\mathtt{j50}) = \mathtt{Z}_{\mathtt{0_c}}(\mathtt{j50}) = (\mathtt{0.09} + \mathtt{j0.23})\Omega \tag{5.68}$$

$$\mathtt{G}_{\mathtt{CC}}(\mathtt{j50}) * \mathtt{I}^{*}_{\mathtt{Lsat_a}} = \mathtt{I}_1 = (\mathtt{46.67} - \mathtt{j1.44})\mathtt{A} \tag{5.69}$$

$$\frac{\mathtt{G}(\mathtt{j50}) * \mathtt{V}^{*}_{\mathtt{0_b}}}{\mathtt{Z}_{\mathtt{0_b}}(\mathtt{j50})} = \mathtt{I}_2 = (\mathtt{-901.35} + \mathtt{j269.57})\mathtt{A} \tag{5.70}$$

$$\frac{\mathtt{G}(\mathtt{j50}) * \mathtt{V}^{*}_{\mathtt{0_c}}}{\mathtt{Z}_{\mathtt{0_c}}(\mathtt{j50})} = \mathtt{I}_3 = (\mathtt{684.13} + \mathtt{j645.8})\mathtt{A} \tag{5.71}$$

The original bus impedance matrix of the network in Figure 5.12 is modified in order to take into account the network modification introduced by the fault, which is an extra connection between node 7 and earth, see Figure 5.12. Once Z_{BUSnew} is formed, the node voltages of the system are found to be:

$$\mathtt{V}_1 = \mathtt{167.94}\angle\mathtt{1.18}^{\circ}\mathtt{V} \tag{5.72}$$

$$\mathtt{V}_2 = \mathtt{237.41}\angle - \mathtt{128.08}^{\circ}\mathtt{V} \tag{5.73}$$

$$\mathtt{V}_3 = \mathtt{237.75}\angle\mathtt{111.91}^{\circ}\mathtt{V} \tag{5.74}$$

These results and their corresponding peak values (237.5 V, 335.74 V and 336.22 V) compare well with the values in Figure 5.21.

5.4.3 Microgrid supplied by two parallel-connected inverters

The model of two parallel inverters depends on the type of fault because the current limiting strategy is on a per-phase basis. As a result, each fault case study requires its own model.

Case 5: 3ϕ fault (microgrid supplied by two parallel-connected inverters)

For a 3ϕ fault at point F_3, all three phases in each inverter switch to current control as shown in Figure 5.7. Therefore the equivalent six current sources and six parallel

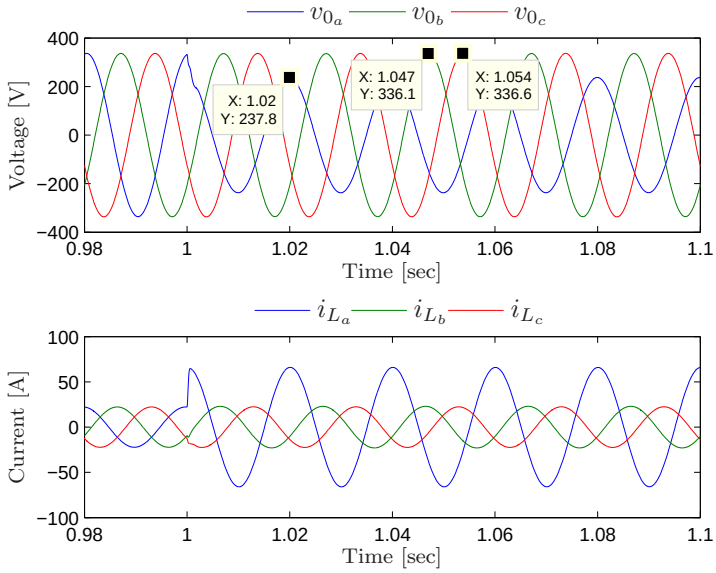


Figure 5.21: Inverter output voltage (v_0) and inductor current (i_L) during a $1\phi g$ fault in a microgrid supplied by a single inverter controlled in the NatRF

impedances are given by:

$$\mathtt{Z_{c_a}(j50) = Z_{c_b}(j50) = Z_{c_c}(j50) = (0.05 - j63.69)\Omega} \tag{5.75}$$

$$\mathtt{G_{CC}(j50) * I^*_{Lsat_{a1}} = I_1 = (46.67 - j1.44)A} \tag{5.76}$$

$$\mathtt{G_{CC}(j50) * I^*_{Lsat_{b1}} = I_2 = (-24.59 - j39.7)A} \tag{5.77}$$

$$\mathtt{G_{CC}(j50) * I^*_{Lsat_{c1}} = I_3 = (-22.08 + j41.14)A} \tag{5.78}$$

$$\mathtt{G_{CC}(j50) * I^*_{Lsat_{a2}} = I_{17} = (46.67 - j1.44)A} \tag{5.79}$$

$$\mathtt{G_{CC}(j50) * I^*_{Lsat_{b2}} = I_{18} = (-24.59 - j39.7)A} \tag{5.80}$$

$$\mathtt{G_{CC}(j50) * I^*_{Lsat_{c2}} = I_{19} = (-22.08 + j41.14)A} \tag{5.81}$$

where $G_{CC}(j50) = (0.99 - j0.03)$. This time earth is chosen as the reference node and therefore all node voltages will be referred to it. As a consequence, the injected neutral currents I_{13} and I_{20} have to be considered as well. However as the equivalent inverter current sources are balanced, I_{13} and I_{20} are equal to zero. From Figure 5.13 and considering the extra connection between nodes 7, 8, 9 and earth, the modified Z_{BUSnew} matrix is

determined and then the output phase voltages are calculated as:

$$\mathtt{V_1} = \mathtt{Z_{11}I_1} + \mathtt{Z_{12}I_2} + \mathtt{Z_{13}I_3} + \mathtt{Z_{1-17}I_{17}} + \mathtt{Z_{1-18}I_{18}} + \mathtt{Z_{1-19}I_{19}} = \mathtt{73.41\angle 14.78^{\circ}V} \quad (5.82)$$

$$\mathtt{V_2} = \mathtt{Z_{21}I_1} + \mathtt{Z_{22}I_2} + \mathtt{Z_{23}I_3} + \mathtt{Z_{2-17}I_{17}} + \mathtt{Z_{2-18}I_{18}} + \mathtt{Z_{2-19}I_{19}} = \mathtt{73.41\angle -105.21^{\circ}V} \quad (5.83)$$

$$\mathtt{V_3} = \mathtt{Z_{31}I_1} + \mathtt{Z_{32}I_2} + \mathtt{Z_{33}I_3} + \mathtt{Z_{3-17}I_{17}} + \mathtt{Z_{3-18}I_{18}} + \mathtt{Z_{3-19}I_{19}} = \mathtt{73.41\angle 134.78^{\circ}V} \quad (5.84)$$

$$\mathtt{V_{17}} = \mathtt{Z_{71}I_1} + \mathtt{Z_{72}I_2} + \mathtt{Z_{73}I_3} + \mathtt{Z_{7-17}I_{17}} + \mathtt{Z_{7-18}I_{18}} + \mathtt{Z_{7-19}I_{19}} = \mathtt{85.11\angle 15.35^{\circ}V} \quad (5.85)$$

$$\mathtt{V_{18}} = \mathtt{Z_{81}I_1} + \mathtt{Z_{82}I_2} + \mathtt{Z_{83}I_3} + \mathtt{Z_{8-17}I_{17}} + \mathtt{Z_{8-18}I_{18}} + \mathtt{Z_{8-19}I_{19}} = \mathtt{85.11\angle -104.64^{\circ}V} \quad (5.86)$$

$$\mathtt{V_{19}} = \mathtt{Z_{91}I_1} + \mathtt{Z_{92}I_2} + \mathtt{Z_{93}I_3} + \mathtt{Z_{9-17}I_{17}} + \mathtt{Z_{9-18}I_{18}} + \mathtt{Z_{9-19}I_{19}} = \mathtt{85.11\angle 135.35^{\circ}V} \quad (5.87)$$

The corresponding peak values are 103.81 V and 120.36 V. These results can be compared with the ones in Figure 5.18 and once again the inverter fault models together with the numerical fault analysis give results in accordance with the simulation.

Case 6: $1\phi g$ fault at F_3 (microgrid supplied by two parallel-connected inverters)

For a single phase-to-ground fault both inverters do not go into current limiting and keep on working as two voltage sources as described by the inverters' model in Figure 5.9. The equivalent injected current and impedances are given by:

$$\mathtt{Z_{0_a}(j50)} = \mathtt{Z_{0_b}(j50)} = \mathtt{Z_{0_c}(j50)} = \mathtt{(0.09 + j0.23)\Omega} \quad (5.88)$$

$$\frac{\mathtt{G(j50)} * \mathtt{V^*_{0_{a1}}}}{\mathtt{Z_{0_a}(j50)}} = \mathtt{I_1} = \mathtt{(217.22 - j915.38)A} \quad (5.89)$$

$$\frac{\mathtt{G(j50)} * \mathtt{V^*_{0_{b1}}}}{\mathtt{Z_{0_b}(j50)}} = \mathtt{I_2} = \mathtt{(-901.35 + j269.57)A} \quad (5.90)$$

$$\frac{\mathtt{G(j50)} * \mathtt{V^*_{0_{c1}}}}{\mathtt{Z_{0_c}(j50)}} = \mathtt{I_3} = \mathtt{(684.13 + j645.8)A} \quad (5.91)$$

$$\frac{\mathtt{G(j50)} * \mathtt{V^*_{0_{a2}}}}{\mathtt{Z_{0_a}(j50)}} = \mathtt{I_{17}} = \mathtt{(217.22 - j915.38)A} \quad (5.92)$$

$$\frac{\mathtt{G(j50)} * \mathtt{V^*_{0_{b2}}}}{\mathtt{Z_{0_b}(j50)}} = \mathtt{I_{18}} = \mathtt{(-901.35 + j269.57)A} \quad (5.93)$$

$$\frac{\mathtt{G(j50)} * \mathtt{V^*_{0_{c2}}}}{\mathtt{Z_{0_c}(j50)}} = \mathtt{I_{19}} = \mathtt{(684.13 + j645.8)A} \quad (5.94)$$

where $G(j50) = (0.98 - j0.12)$ and the voltage references are assumed identical for both inverters. The injected neutral currents I_{13} and I_{20} are again equal to zero as the equivalent inverters' current sources are balanced.

This time, after determining Z_{BUSnew}, the node voltages at the fault point are

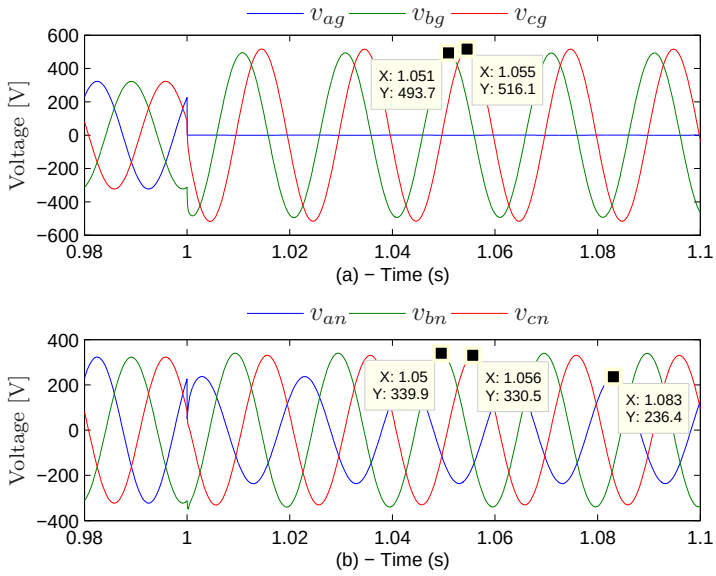


Figure 5.22: Phase-to-earth (v_{ag}, v_{bg}, v_{cg}) and phase-to-neutral (v_{an}, v_{bn}, v_{cn}) voltages at fault point during a $1\phi g$ fault at F_3 in a microgrid supplied by two parallel-connected inverters

determined as follows:

$$\mathtt{V_7} = \mathtt{Z_{71}I_1} + \mathtt{Z_{72}I_2} + \mathtt{Z_{73}I_3} + \mathtt{Z_{7-17}I_{17}} + \mathtt{Z_{7-18}I_{18}} + \mathtt{Z_{7-19}I_{19}} = \mathtt{0V} \tag{5.95}$$

$$\mathtt{V_8} = \mathtt{Z_{81}I_1} + \mathtt{Z_{82}I_2} + \mathtt{Z_{83}I_3} + \mathtt{Z_{8-17}I_{17}} + \mathtt{Z_{8-18}I_{18}} + \mathtt{Z_{8-19}I_{19}} = \mathtt{351.50\angle -156.89^{\circ}V} \tag{5.96}$$

$$\mathtt{V_9} = \mathtt{Z_{91}I_1} + \mathtt{Z_{92}I_2} + \mathtt{Z_{93}I_3} + \mathtt{Z_{9-17}I_{17}} + \mathtt{Z_{9-18}I_{18}} + \mathtt{Z_{9-19}I_{19}} = \mathtt{367.29\angle 136.11^{\circ}V} \tag{5.97}$$

These voltages are referred to earth. In order to have the corresponding phase-to-neutral voltages V_{11} is calculated as

$$\mathtt{V_{11}} = \mathtt{Z_{11-1}I_1} + \mathtt{Z_{11-2}I_2} + \mathtt{Z_{11-3}I_3} + \mathtt{Z_{11-17}I_{17}} + \mathtt{Z_{11-18}I_{18}} + \mathtt{Z_{11-19}I_{19}} = \mathtt{167.93\angle 165.20^{\circ}V} \tag{5.98}$$

and then the phase-to-neutral voltages at the fault point are given by:

$$\mathtt{V_{7-11}} = \mathtt{V_8} - \mathtt{V_{11}} = \mathtt{167.93\angle -14.79^{\circ}V} \tag{5.99}$$

$$\mathtt{V_{8-11}} = \mathtt{V_8} - \mathtt{V_{11}} = \mathtt{242.06\angle -131.67^{\circ}V} \tag{5.100}$$

$$\mathtt{V_{9-11}} = \mathtt{V_9} - \mathtt{V_{11}} = \mathtt{235.18\angle 115.80^{\circ}V} \tag{5.101}$$

The corresponding peak values are 237.48 V, 342.32 V and 332.59 V. These results compare well with the simulation ones shown in Figure 5.22.

Case 7: $1\phi g$ fault at F_1 (microgrid supplied by two parallel-connected inverters)

A $1\phi g$ fault applied at F_1 introduces and extra connection between node 14 and earth. For this particular fault, the first inverter goes into current limiting while the second one is controlled as a voltage source in all three phases. The equivalent model of the two inverters is shown in Figure 5.11. The equivalent injected current and impedances for the first inverter are:

$$\mathtt{Z}_{\mathtt{c}_\mathtt{a}}(\mathtt{j50}) = (0.05 - \mathtt{j}63.69)\Omega \tag{5.102}$$

$$\mathtt{Z}_{0_\mathtt{b}}(\mathtt{j50}) = \mathtt{Z}_{0_\mathtt{c}}(\mathtt{j50}) = (0.09 + \mathtt{j}0.23)\Omega \tag{5.103}$$

$$\mathtt{G}_{\mathtt{CC}}(\mathtt{j50}) * \mathtt{I}^*_{\mathtt{Lsat}_{\mathtt{a1}}} = \mathtt{I}_1 = (46.67 - \mathtt{j}1.44)\mathtt{A} \tag{5.104}$$

$$\frac{\mathtt{G}(\mathtt{j50}) * \mathtt{V}^*_{0_{\mathtt{b1}}}}{\mathtt{Z}_{0_\mathtt{b}}(\mathtt{j50})} = \mathtt{I}_2 = (-901.35 + \mathtt{j}269.57)\mathtt{A} \tag{5.105}$$

$$\frac{\mathtt{G}(\mathtt{j50}) * \mathtt{V}^*_{0_{\mathtt{c1}}}}{\mathtt{Z}_{0_\mathtt{c}}(\mathtt{j50})} = \mathtt{I}_3 = (684.13 + \mathtt{j}645.8)\mathtt{A} \tag{5.106}$$

while for the second inverter the equivalent model is given by:

$$\mathtt{Z}_{0_\mathtt{a}}(\mathtt{j50}) = \mathtt{Z}_{0_\mathtt{b}}(\mathtt{j50}) = \mathtt{Z}_{0_\mathtt{c}}(\mathtt{j50}) = (0.09 + \mathtt{j}0.23)\Omega \tag{5.107}$$

$$\frac{\mathtt{G}(\mathtt{j50}) * \mathtt{V}^*_{0_{\mathtt{a2}}}}{\mathtt{Z}_{0_\mathtt{a}}(\mathtt{j50})} = \mathtt{I}_{17} = (217.22 - \mathtt{j}915.38)\mathtt{A} \tag{5.108}$$

$$\frac{\mathtt{G}(\mathtt{j50}) * \mathtt{V}^*_{0_{\mathtt{b2}}}}{\mathtt{Z}_{0_\mathtt{b}}(\mathtt{j50})} = \mathtt{I}_{18} = (-901.35 + \mathtt{j}269.57)\mathtt{A} \tag{5.109}$$

$$\frac{\mathtt{G}(\mathtt{j50}) * \mathtt{V}^*_{0_{\mathtt{c2}}}}{\mathtt{Z}_{0_\mathtt{c}}(\mathtt{j50})} = \mathtt{I}_{19} = (684.13 + \mathtt{j}645.8)\mathtt{A} \tag{5.110}$$

where $G(j50) = (0.98 - j0.12)$ and the voltage references are assumed identical for both inverters. The injected neutral currents I_{13} and I_{20} are given by:

$$\mathtt{I}_{13} = -(\mathtt{I}_1 + \mathtt{I}_2 + \mathtt{I}_3) = (170.54 - \mathtt{j}913.93)\mathtt{A} \tag{5.111}$$

$$\mathtt{I}_{20} = -(\mathtt{I}_{17} + \mathtt{I}_{18} + \mathtt{I}_{19}) = 0\mathtt{A} \tag{5.112}$$

The node voltages at the fault point are determined as follows:

$$\mathtt{V}_{14} = \mathtt{Z}_{14-1}\mathtt{I}_1 + \mathtt{Z}_{14-2}\mathtt{I}_2 + \mathtt{Z}_{14-3}\mathtt{I}_3 + \mathtt{Z}_{14-13}\mathtt{I}_{13} + \tag{5.113}$$

$$+\mathtt{Z}_{14-17}\mathtt{I}_{17} + \mathtt{Z}_{14-18}\mathtt{I}_{18} + \mathtt{Z}_{14-19}\mathtt{I}_{19} + \mathtt{Z}_{14-20}\mathtt{I}_{20} = 0\mathtt{V} \tag{5.114}$$

$$\mathtt{V}_{15} = \mathtt{Z}_{15-1}\mathtt{I}_1 + \mathtt{Z}_{15-2}\mathtt{I}_2 + \mathtt{Z}_{15-3}\mathtt{I}_3 + \mathtt{Z}_{15-13}\mathtt{I}_{13} + \tag{5.115}$$

$$+\mathtt{Z}_{15-17}\mathtt{I}_{17} + \mathtt{Z}_{15-18}\mathtt{I}_{18} + \mathtt{Z}_{15-19}\mathtt{I}_{19} + \mathtt{Z}_{15-20}\mathtt{I}_{20} = 395.55\angle - 157.89^\circ\mathtt{V} \tag{5.116}$$

$$\mathtt{V}_{16} = \mathtt{Z}_{16-1}\mathtt{I}_1 + \mathtt{Z}_{16-2}\mathtt{I}_2 + \mathtt{Z}_{16-3}\mathtt{I}_3 + \mathtt{Z}_{16-13}\mathtt{I}_{13} + \tag{5.117}$$

$$+\mathtt{Z}_{16-17}\mathtt{I}_{17} + \mathtt{Z}_{16-18}\mathtt{I}_{18} + \mathtt{Z}_{16-19}\mathtt{I}_{19} + \mathtt{Z}_{16-20}\mathtt{I}_{20} = 403.30\angle 140.15^\circ\mathtt{V} \tag{5.118}$$

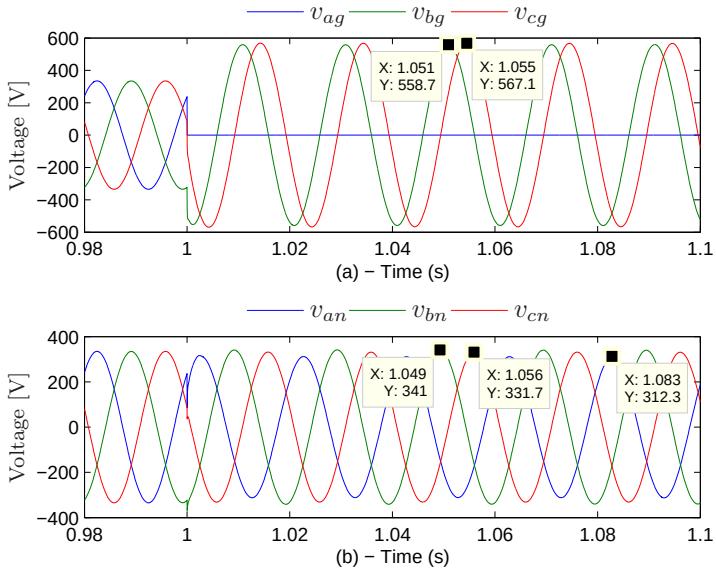


Figure 5.23: Phase-to-earth (v_{ag}, v_{bg}, v_{cg}) and phase-to-neutral (v_{an}, v_{bn}, v_{cn}) voltages at fault point during a $1\phi g$ fault at F_1 in a microgrid supplied by two parallel-connected inverters

These voltages are referred to earth. In order to have the corresponding phase-to-neutral voltages, V_{12} is calculated as

$$\begin{aligned} \mathtt{V}_{12} &= \mathtt{Z}_{12-1}\mathtt{I}_1 + \mathtt{Z}_{12-2}\mathtt{I}_2 + \mathtt{Z}_{12-3}\mathtt{I}_3 + \mathtt{Z}_{12-13}\mathtt{I}_{13} + \\ &+ \mathtt{Z}_{12-17}\mathtt{I}_{17} + \mathtt{Z}_{12-18}\mathtt{I}_{18} + \mathtt{Z}_{12-19}\mathtt{I}_{19} + \mathtt{Z}_{12-20}\mathtt{I}_{20} = 220.91\angle 169.07^{\circ}\mathtt{V} \end{aligned} \tag{5.119}$$

and then the phase-to-neutral voltages at the fault point are given by:

$$\mathtt{V}_{14-12} = \mathtt{V}_{14} - \mathtt{V}_{12} = 220.91\angle -10.92^{\circ}\mathtt{V} \tag{5.120}$$

$$\mathtt{V}_{15-12} = \mathtt{V}_{15} - \mathtt{V}_{12} = 242.37\angle -128.10^{\circ}\mathtt{V} \tag{5.121}$$

$$\mathtt{V}_{16-12} = \mathtt{V}_{16} - \mathtt{V}_{12} = 235.58\angle 113.17^{\circ}\mathtt{V} \tag{5.122}$$

The corresponding peak values are 312.41 V, 342.76 V and 333.16 V. These results compare well with the simulation ones shown in Figure 5.23.

5.5 Discussion on inverter fault models

It is clear from the results of the case studies that the developed models are capable of capturing the principle features of the fault response of inverter-only microgrids. Complex inverter control actions have been condensed into simple equivalent two-terminal circuit models which then have been validated by comparing the behaviour of PSCAD simulation

with results obtained from the use of these models in numerical fault analysis. The following points summarize important key concepts and findings which relate to the developed models.

Models structure and fault analysis

According to the developed models, in the event of a fault, an inverter can be represented as a controlled current source with a parallel impedance. Depending on the fault type and on the reference frame implementation of the control system, the equivalent inverter model can be:

- symmetrical and therefore representable in phase coordinates or sequence components
- asymmetrical and therefore representable only in phase coordinates.

For a three-phase fault, the equivalent inverter model is symmetrical regardless of the inverter control. For unbalanced faults, SynRF control generates symmetrical models while NatRF control generates asymmetrical models. Generally, the parallel-connected inverters considered in this thesis tend to have fault models similar to the ones developed for a single inverter controlled in the NatRF, because they have the two-loop control structure implemented in the NatRF.

Traditional sequence-component–based fault analysis can be used with symmetrical inverter fault models while fault analysis based on direct phase coordinates is flexible enough to be successfully used in conjunction with all the developed inverter models, both symmetrical and asymmetrical.

A novel characteristic of the developed fault models is their combination of microgrid network parameters with the inverter's control gains. For example, the model in Figure 5.5 clearly shows the dependence of the current sources and impedances on the filter parameters and on the control gains. In particular, while Z_{c_a} is a physical impedance (the capacitance of the LC filter), Z_{0_b} and Z_{0_c} are not physical impedances. This influence of the control on the models is also present in the SynRF model where G_{CC} is considered equal to unity at the system frequency because of the high current-loop bandwidth.

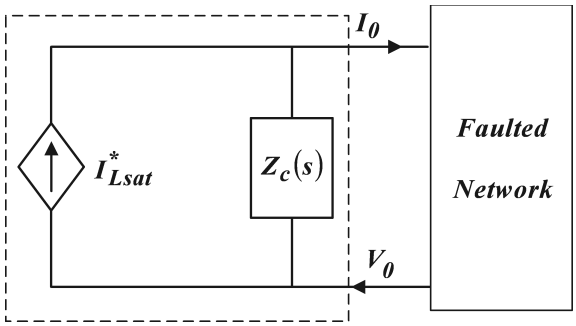


Figure 5.24: Interaction between faulted network and inverter controlled as a constant current source

Fault models and stand-alone inverters

The PSCAD simulations in Section 4.1.5, showed how a stand-alone inverter controlled in the SynRF supplies to each phase a current twice the nominal current value irrespective of the fault type. This behaviour relates perfectly to the fault model in Figure 5.3 where the inverter is equivalent to three constant ideal current sources with a parallel impedance. On the other hand, the same simulations in Section 4.1.5 showed that the behaviour of network fault voltages is highly dependent on the fault type: balanced faults lead to a uniform undervoltage (see Figure 4.17) while unbalanced faults produce a large overvoltage on the healthy phases (see Figures 4.18, 4.19 and 4.20).

This particular influence of the network on voltage can be explained by considering the overall faulted microgrid model (i.e. inverter plus network) shown in Figure 5.24. Here the inverter controls the current injected in the faulted network and the network controls the voltage through its presented impedance. This model is the opposite of the model in Figure 3.14 which shows the interactions during normal operation between the inverter (controlled as a voltage source with a series impedance) and the microgrid. During normal operation, the inverter regulates the voltage (by controlling v_0) while the network (specifically, its impedances) regulate the current. A fault can be considered as an increase in load (balanced or unbalanced) which causes an increase in current that ultimately activates the inverter current limiting. As the limit is activated, the relationship between inverter and network becomes reverse with the network now influencing the voltage magnitude.

In contrast to the control in the SynRF, the control in the NatRF limits the current in the faulty phases while keeping the control of the voltage in the healthy ones. Because of this “dual ”control, healthy phases do not experience any voltage rise in the event of

a fault. For asymmetrical inverter fault models, like the one in Figure 5.5, the resulting faulted microgrid model is a combination of the model in Figure 5.24 for faulted phases and of the model in Figure 3.14 for healthy phases. This approximation can be used to understand the fault behaviour of the system as the inverter is capable of de-coupled phase control in the NatRF. However, for fault calculation purposes, the more rigorous approach presented in Section 5.2 and applied in Section 5.4 has to be used.

Fault models and parallel inverters

Based on the PSCAD simulations in Section 4.4.5, the presence of the droop loops was neglected while developing the equivalent fault models in Figures 5.7, 5.8, 5.9, 5.10 and 5.11. Numerical fault analysis results have shown how this approximation produces very small errors compared with the simulation values.

The response of parallel inverters depends on the type of fault and on the increased fault current capability. For a 3ϕ fault both inverters inject the same amount of current into the microgrid network which then controls the voltage. The presence of Z_l results in v_{0_2} being higher than v_{0_1}, as shown from simulation in Figure 4.47. This can be explained by considering the model in Figure 5.24 where another current source should be added. The second inverter sees a bigger impedance compared with the one seen by the first inverter and, as the current injected is constant, v_{0_2} is higher than v_{0_1}.

For a $1\phi g$ fault with no current limiting, the two inverters are equivalent to two voltage sources, see Figure 5.10. As a result the fault is perceived as an increased unbalanced load and the inverters are still capable of supplying more current while controlling the voltage as shown in Figure 4.50.

Both models for 3ϕ and $1\phi g$ faults with no current limiting are symmetrical. On the other hand, the models for 2ϕ and $2\phi g$ faults and $1\phi g$ faults with current limiting are unbalanced and cannot be used in sequence-component–based fault analysis. They represent the healthy phases as voltage controlled and this is in agreement with the constant values of v_{0_1} and v_{0_2} shown in Figures 4.48, 4.49 and 4.53. On the other hand, the models' representation of phases b and c as current sources well agrees with the plots of i_{L_b} and i_{L_c} in Figure 4.48, 4.49 and 4.53.

Fault models and their applications

Overall, the development of the inverter fault models and their validation with numerical fault analysis has given a deeper insight into the different factors affecting the overall microgrid behaviour. The improved understanding and the possibility of performing fault analysis calculations, finds two immediate applications.

A first application of these models is going to be demonstrated in the next Chapter where the models are going to be used in the design process of a suitable fault detection strategy for inverter-only microgrids. The approach used in this Chapter is going to demonstrate that the models have the potential to be more generally used by utility engineers in fault protection studies.

A second application comes from the ability of these models to give a simple but complete representation of the behaviour of an inverter during faults and the factors affecting it. As a result, they can be used to modify the control of the inverter in order to have a desired fault response. The study of a desiderable fault response is not going to be considered in this thesis. However, the discussion in Chapter 4 on the various types of current limiting and on the generation of distorted waveforms by the inverter is an example of what could be involved in such study.

Chapter 6

A Fault detection technique suitable for islanded inverter-only microgrids

The microgrid models considered in this thesis are a part of a larger LV network which can be operated autonomously from the main grid supply. The existing overcurrent protection devices in the distribution network would be designed to operate for fault currents well above the values for normal load operation. However, in microgrids where the only source of power comes from inverter-interfaced DG units, like the models under study in the thesis, the detection of faults can be problematic because inverters have a reduced fault current capability. In Section 2.4.1 fault currents in a typical distribution network were compared with fault currents in islanded inverter-only microgrids and the impact of a reduced fault current on overcurrent protection was also analyzed. It is clear that alternative ways to detect the presence of a fault are needed in islanded inverter-only microgrids.

In this Chapter a fault detection technique which can be used in islanded inverter-only microgrids is proposed. First, a review is conducted of the available fault protection schemes in traditional distribution networks which might be applied to microgrids. Then, in Section 6.2, the focus is on the two microgrid models under study in this thesis (see Figure 3.19 and 3.20) and on the identification of ways to detect different types of fault through voltage. Section 6.3 gives an overview of some voltage detection techniques and finally Section 6.3.4 illustrates how the proposed voltage-based fault detection strategy can be used in the design of the protection system of the two microgrid models under study.

6.1 Protection in traditional electricity networks: a microgrid prospective

The reduced fault current environment in islanded inverter-only microgrids can be problematic when designing an overcurrent-based protection scheme. Generally, the choice of using overcurrent devices is very well suited to LV distribution networks as it represents a good compromise between performance and costs. However there are other protection methods which can be considered for microgrids even if they are not conventionally implemented in distribution networks.

One of these methods is based on unit protection where each network element (lines, transformers, etc.) is individually protected [13]. The most popular type of unit protection is the current differential protection which operates by measuring the difference between the currents at both ends of the protected element. Under normal operation or for a fault outside the zone of the protected element, the currents at the two ends are the same (i.e. the same current enters and then exits the protection zone). A fault inside the element protection zone produces a difference between these currents and if the difference exceeds a certain threshold, the protection system opens the two breakers at the terminals of the protected element. This type of protection is really selective and could definitely work for a microgrid. However it is rather costly as it requires some form of communication [13].

Another method which is quite popular in transmission networks is distance protection. Here the fault is located by measuring the current and voltage at the relay and then calculating the impedance between the relay and the fault point. The value of this impedance is a measure of the location of the fault along the protected line. Distance protection can be very selective and also has the advantage of not being dependent on system operating conditions. However, because it is affected by infeeds of power [13], it might not operate properly if additional DG units are connected to the microgrid or if the microgrid network changes its topology or if DG units are disconnected. Moreover, distance protection has some well know problems with fault arc resistance and power system oscillations [13].

Beyond these traditional and well established protection philosophies, modern numerical multifunctional relays, can calculate and process electrical quantities which previously would have required a big implementation effort. As a result, the use of sequence components to detect the presence of faults is gaining popularity [13, 86, 87] and is worth

considering in microgrid fault detection.

Finally it should be mentioned that voltage, rather than current, can be used to detect the presence of a fault even if its use is not very common in electricity networks. The problem with voltage is that its behaviour during power system fault is strongly dependent on the type of fault and on the system neutral earthing [88]. Generally a fault is associated with a drop in the system voltage however some faults like single phase-to-ground and double phase-to-ground faults may not result in a reduction in the positive sequence component of the voltage and may produce overvoltages. Nevertheless, if the fault behaviour of the system is well known, then voltage can be used in fault protection. For example, voltage sag detection techniques can be extended to general fault detection techniques by using negative and zero sequence voltage components as described in [89] and [41]. Another example of application of voltage observation in power systems protection is voltage-controlled overcurrent relays where the current threshold is reduced and the operation is inhibited until the voltage drops below a set value.

Because the available fault current is rather limited in inverter-only islanded microgrids and because the microgrid topology is intended to be flexible and costs should be minimized, it can be easily predicted that voltage could play an important role in the detection of faults in microgrids.

6.2 Fault detection in islanded inverter-only microgrids

6.2.1 Microgrid supplied by a single inverter

The microgrid in Figure 3.19, whose fault response has been simulated and modelled in Chapters 4 and 5, is considered here as well. As discussed in Section 3.1.3, there are many different microgrid network configurations but here a microgrid which can be disconnected through a 4-pole SS as shown in Figure 3.12 is selected as the example. Figure 6.1 shows the microgrid model with the SS, a possible relay configuration (R_1, R_2 and R_3) and three possible fault locations (F_1, F_2 and F_3) which will be considered in this Chapter.

When the microgrid is connected as a part of an LV distribution network, the existing protection system would detect the presence of a fault by sensing an increase in current. However, in island mode, the magnitude of the current cannot be used as an indicator of the presence of a fault as the inverter can only supply a limited amount current to the fault. An appropriate fault detection strategy needs to be designed for this type of

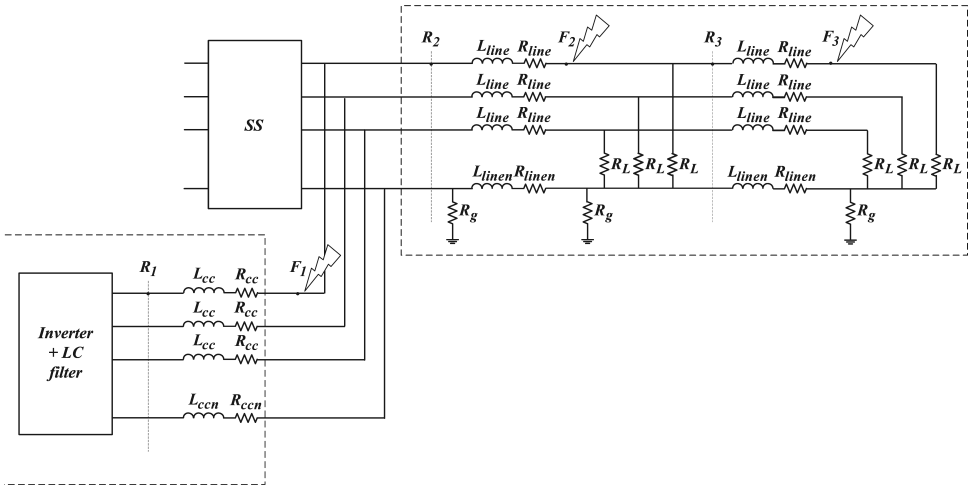


Figure 6.1: Microgrid supplied by a single inverter: relay configuration and fault locations

microgrid by considering its operation and its protection requirements.

Microgrid operation

The simulations in Chapter 4 and the modelling in Chapter 5 have shown how the control of the inverter plays a fundamental role in shaping the response of the microgrid. Here the inverter shown in Figure 3.19 is controlled in the NatRF with RMS current limiting as these choices give a better microgrid fault response as discussed in Section 4.3. The microgrid in this study supplies two resistive loads of 5.6 kW (three-phase) each. The load is assumed to be balanced and below the inverter's power ratings but unbalanced load operation and overload are also possible operating conditions of the microgrid.

Table 6.1 shows the phase-to-neutral voltages (V_a, V_b, V_c), phase currents (I_a, I_b, I_c) and their correspective sequence components at the relay locations (R_1, R_2, R_3) for two load conditions: 20% unbalance and 50% unbalance. The 20% and 50% load unbalance are referred to the inverter's rating (i.e. 17 kVA) and were determined based on the definition of load unbalance given in Section 4.1.4. The inverter's control responds well to load unbalance and the resulting voltages have very small negative and zero sequence components even for 50% load unbalance. Here, as in [13, 40], it is assumed that the microgrid can operate with a maximum 20% load unbalance. Later in this Chapter the values of V_n for 20% load unbalance in Table 6.1 will be multiplied by three and used as a threshold to detect unbalanced faults in the microgrid. These threshold values are above the corresponding values of V_n for 50% load unbalance in Table 6.1. Therefore the proposed

Table 6.1: Load unbalanced operation in a microgrid supplied by a single inverter controlled in the NatRF

20% load unbalance												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	41.35	25.42	25.49	330.11	333.08	333.23	30.75	5.59	5.01	332.13	1.41	1.27
R_2	41.35	25.42	25.49	325.75	332.72	330.81	30.75	5.59	5.01	3329.74	2.04	3.55
R_3	20.33	12.63	12.69	305.19	324.95	325.31	15.22	2.72	2.39	318.45	3.65	9.73
50% load unbalance												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	54.94	16.47	16.57	327.56	334.77	335.01	29.31	13.26	12.35	332.43	3.36	3.13
R_2	54.94	16.47	16.57	320.56	337.53	332.63	29.31	13.26	12.35	330.16	4.87	8.76
R_3	26.68	8.22	8.30	287.04	335.44	336.25	14.39	6.40	5.87	319.38	8.69	23.99

fault detection strategy does not malfunction even for 50% load unbalance. Higher load unbalance in the network is likely to cause malfunctioning in the proposed fault detection. However, this type of malfunction should be avoided as it is safe to assume that an islanded microgrid is likely to have some form of load control, as an "energy manager" [6,12], which regulates the level of load unbalance and maintains unbalance within a certain limit (i.e. 20%).

The microgrid can operate with different loading conditions which have to be considered when designing a fault detection strategy. Indeed a good fault detection strategy has to work for faults in lightly loaded as well as fully loaded (i.e. up to inverters' nominal ratings) microgrids. Overloading is also another operating condition which has to be considered when designing a fault detection strategy. The overloading capabilities of an inverter very much depend on the manufacturer and on the design specifications. Depending on the settings of the inverter own protection system, the inverter is likely to be disconnected if the power supplied is above 1.2 or 1.5 times the nominal value after a certain length of time. Or it could happen that the inverter's overloading capabilities allow the supplied current to increase to a point that it triggers the inverter current limiting. Indeed, with the low limit of 2 p.u. imposed on the maximum current which the inverter can supply, it can be very difficult to distinguish between a simple overload or a network fault. The presence of an "energy manager"in the microgrid could possibly mitigate this problem by not allowing the connection of loads beyond the inverters' ratings.

Here, the impact of different microgrid loading operations is going to be considered and discussed in Section 6.4.

Microgrid protection requirements

The example microgrid network of Figure 6.1 is fairly simple because the single power source generates power flows in one direction only. Moreover any breaker operation will not be able to form an island within the microgrid as there is only a single inverter.

At the moment there are a few rather dated standards like Engineering Recommendation G59/1 [22] and IEEE P1547 [23] which specify the response of interconnected DG units to abnormal conditions in the network (i.e. under/over voltage protection). The operation of islanded microgrids is not contemplated by any approved standard. As a result, there are no microgrid protection guidelines. In this work the main priority of the protection system is the safety of people and equipment therefore it is assumed that the inverter stays connected and supplies enough power, within its current and voltage limits, for the fault to be detected and cleared. Additional DG interconnection requirements, like the ones in [22, 23], are not considered and the inverter's own internal protection is assumed not to interfere with that of the microgrid.

Finally, it is important to recognize that in order to maintain the stability of the microgrid [44] and make sure that it is feasible to have an inverter supplying power to the microgrid during any network fault, the detection and clearing of faults should be designed to act as quickly as possible.

Fault detection in a microgrid supplied by a single inverter

The purpose of this Section is to identify the electrical quantities which can be used to detect the presence of a fault in the microgrid. Various faults at locations F_1, F_2 and F_3, shown in Figure 6.1, are considered and for each case the phase-to-neutral voltages and currents at points R_1, R_2 and R_3, expressed as maximum phase values, and the corresponding sequence components are presented and discussed. These values have been numerically determined with the inverter fault models and the direct phase fault analysis as described in Chapter 5.

Table 6.2 shows the response of the system to a 3ϕ fault applied at points F_1, F_2 and F_3 respectively (see Figure 6.1). The inverter behaves as a balanced constant current source injecting a current twice its nominal value and the resulting network impedance in parallel with the current source generates a considerable voltage drop. This type of fault can be detected by measuring the voltage drop of the positive sequence component of the

Table 6.2: 3ϕ fault in a microgrid supplied by a single inverter controlled in the NatRF (values in yellow are chosen as indicators of the presence of a fault)

Fault at F_1												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	66.15	66.15	66.15	7.53	7.53	7.53	66.15	0	0	7.53	0	0
R_2	0	0	0	0	0	0	0	0	0	0	0	0
R_3	0	0	0	0	0	0	0	0	0	0	0	0
Fault at F_2												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	66.24	66.24	66.24	29.47	29.47	29.47	66.24	0	0	29.47	0	0
R_2	66.24	66.24	66.24	24.99	24.99	24.99	66.24	0	0	24.99	0	0
R_3	0	0	0	0	0	0	0	0	0	0	0	0
Fault at F_3												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	66.34	66.34	66.34	53.90	53.90	53.90	66.34	0	0	53.90	0	0
R_2	66.34	66.34	66.34	49.76	49.76	49.76	66.34	0	0	49.76	0	0
R_3	65.54	65.54	65.54	24.73	24.73	24.73	65.53	0	0	24.73	0	0

voltage V_p which is highlighted in yellow in Table 6.2.

Table 6.3 shows the results for a 2ϕ fault at F_1, F_2 and F_3. As explained in Chapter 4, for this type of fault the inverter control triggers voltage limiting and as a result voltage and currents are distorted. For this reason their per-phase maximum value has not been included in the Table. Nevertheless, the current and voltage sequence components have been determined through simulations with the On-Line Frequency Scanner block set in PSCAD. From Table 6.3 it can be seen that V_n, which is highlighted in yellow, at R_1, R_2 and R_3 experiences a very big increase which is well above the values registered during operation with an unbalanced load. Also V_0 experiences an increase however this is increase is not as big as the one of V_n. It follows that V_n is used to detect the presence of 2ϕ faults.

It should be noted that in synchronous machine-based power systems, a 2ϕ fault will not produce any zero sequence components in the current and in the voltage in contrast to what happens in the microgrid under study. The absence of zero sequence components is caused by the fact that the synchronous machines only produce a balanced output voltage even during a fault and the corresponding zero sequence equivalent circuit network is passive. On the other hand, in a microgrid, this different behaviour for a 2ϕ fault can be explained considering the control of the inverter and its model as developed in Section 5.1.1. As the inverter is controlled in the NatRF, for a 2ϕ fault the current sources and

Table 6.3: 2ϕ fault in a microgrid supplied by a single inverter controlled in the NatRF (values in yellow are chosen as indicators of the presence of a fault)

Fault at F_1												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	49.25	16.53	10.24	255.40	253.21	173.22
R_2	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	16.42	16.41	10.24	253.84	253.68	171.78
R_3	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	8.16	8.15	5.00	247.82	247.67	157.05
Fault at F_2												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	49.07	16.48	10.05	265.71	240.11	170.03
R_2	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	49.07	16.48	10.05	264.18	240.49	168.67
R_3	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	8.11	8.11	4.91	246.62	246.26	154.24
Fault at F_3												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	48.85	16.41	9.87	275.44	227.94	167.16
R_2	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	48.85	16.41	9.87	274.2	227.93	165.71
R_3	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	40.29	24.17	4.82	256.58	233.51	151.46

Table 6.4: $2\phi g$ fault in a microgrid supplied by a single inverter controlled in the NatRF (values in yellow are chosen as indicators of the presence of a fault)

Fault at F_1												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	22.56	63.87	68.37	336.03	159.92	172.55	51.58	14.68	14.54	167.98	166.57	11.17
R_2	22.56	9.78	9.78	336.49	163.62	163.62	10.78	10.78	1.00	166.67	166.67	5.58
R_3	11.29	4.78	4.78	338.12	150.07	150.07	5.35	5.35	0.57	162.72	162.72	12.80
Fault at F_2												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	22.57	63.97	68.44	336.03	167.49	190.65	51.64	14.71	14.55	183.77	158.57	13.79
R_2	22.57	63.97	68.44	336.52	169.80	182.42	51.64	14.71	14.55	182.28	158.65	7.40
R_3	11.29	4.86	4.86	338.23	152.69	152.69	5.38	5.38	0.51	163.63	163.63	11.09
Fault at F_3												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	22.57	64.09	68.48	336.03	175.24	207.43	51.70	14.73	14.57	198.64	149.81	17.51
R_2	22.57	64.09	68.48	336.55	176.25	199.86	51.70	14.73	14.57	197.02	149.86	12.11
R_3	11.29	61.27	65.05	338.35	155.83	168.91	45.76	19.81	14.75	178.20	154.82	6.11

Table 6.5: $1\phi n$ **fault in a microgrid supplied by a single inverter controlled in the NatRF (values in yellow are chosen as indicators of the presence of a fault)**

Fault at F_1												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	66.23	21.61	21.25	12.75	336.12	335.94	36.30	14.76	15.25	224.64	111.44	111.55
R_2	0.58	21.61	21.25	0	340.27	331.03	14.47	7.21	6.68	223.76	111.55	112.27
R_3	0.35	10.70	10.54	7.14	327.31	321.26	7.19	3.58	3.26	218.46	108.90	102.65
Fault at F_2												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	66.39	22.68	21.60	48.33	335.79	336.24	36.83	15.29	14.33	237.57	98.96	99.06
R_2	66.39	22.68	21.60	40.94	339.55	331.80	36.83	15.29	14.33	236.59	98.99	99.55
R_3	0.14	11.21	10.71	0	343.90	326.56	7.35	3.42	3.79	223.31	104.12	119.40
Fault at F_3												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	66.53	23.18	21.82	90.52	335.62	336.39	37.12	15.55	13.91	251.38	85.96	86.09
R_2	66.53	23.18	21.82	83.87	339.22	332.18	37.12	15.55	13.91	250.31	85.91	86.28
R_3	65.12	11.77	10.93	43.62	342.53	327.13	29.23	18.51	17.39	236.84	90.99	105.06

Table 6.6: $1\phi g$ **fault in a microgrid supplied by a single inverter controlled in the NatRF (values in yellow are chosen as indicators of the presence of a fault)**

Fault at F_1												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	66.19	22.53	21.62	193.12	335.81	336.20	36.75	15.13	14.33	287.89	49.02	49.12
R_2	11.55	22.53	21.62	189.40	339.68	331.90	18.55	3.17	3.88	286.84	49.00	49.55
R_3	5.67	11.25	10.76	176.42	338.38	325.82	9.22	1.57	2.00	280.05	47.84	56.62
Fault at F_2												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	66.27	22.53	21.63	217.27	335.81	336.20	36.78	15.15	14.35	295.78	41.85	41.97
R_2	66.27	22.53	21.63	213.26	339.70	331.92	36.78	15.15	14.35	294.69	41.71	41.98
R_3	5.79	11.25	10.76	180.08	338.37	325.94	9.26	1.53	1.96	281.31	46.60	55.47
Fault at F_3												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	66.33	22.53	21.63	237.56	335.81	336.20	36.81	15.17	14.36	302.42	36.09	36.23
R_2	66.33	22.53	21.63	233.36	339.71	331.94	36.81	15.17	14.36	301.30	35.81	35.76
R_3	59.67	11.25	10.77	199.90	338.42	326.03	27.21	16.46	15.99	287.88	40.49	49.09

the equivalent impedances are unbalanced. It follows that the inverter injects a certain amount of zero sequence current and the equivalent zero sequence circuit network is active.

Table 6.4 shows the response of the microgrid to a $2\phi g$ fault. Here V_p experiences a drop while V_n increases and becomes almost equal to V_p depending on the position of the fault. As a result, the values of V_n, which are highlighted in yellow, can be used to detect the presence of this fault. From this Table it can also be seen that I_n and I_0 are equal at the relay points between the inverter and the fault location. This can be explained again with the inverter control and its fault model. Indeed the faulted phases are current controlled and I_b and I_c have the same magnitude and phases equal to $-\frac{2}{3}\pi$ and $\frac{2}{3}\pi$ respectively. As a result, the corresponding negative and zero sequence components are equal.

Tables 6.5 and 6.6 show the response to a $1\phi n$ and a $1\phi g$ fault respectively. Again V_p experiences a drop and V_n increases significantly. For these faults, phases b and c remain voltage controlled and as a result $V_n = V_0$ near the inverter's output. Also this time, V_n is chosen to detect these faults.

To summarize, 3ϕ faults can be detected with a drop in the positive sequence component of the phase voltage while all unbalanced faults can be detected by measuring an increase in the negative sequence component of the phase voltage. The fault detection based on V_n acts as soon as an event triggers the current limiting in one or more phases. Indeed, as the current becomes the controlled variable, control over the voltage is lost and the component V_n increases.

6.2.2 Microgrid supplied by two parallel-connected inverters

The purpose of this section is to investigate how a fault can be detected in a microgrid supplied by two inverters and what are the differences with the single-inverter case analyzed in Section 6.2.1.

Figure 6.2 shows the microgrid model under study with two parallel-connected inverters, several possible relay locations (R_1, R_2, R_3, R_4, R_5 and R_6) and three possible fault locations (F_1, F_2, F_3 and F_4).

Microgrid operation

As described in Section 4.4.1, the two parallel inverters in Figure 6.2 are controlled by an outer droop loop which generates the voltage and frequency references for the two-loop control structure which is implemented in the NatRF. The current in each inverter is RMS

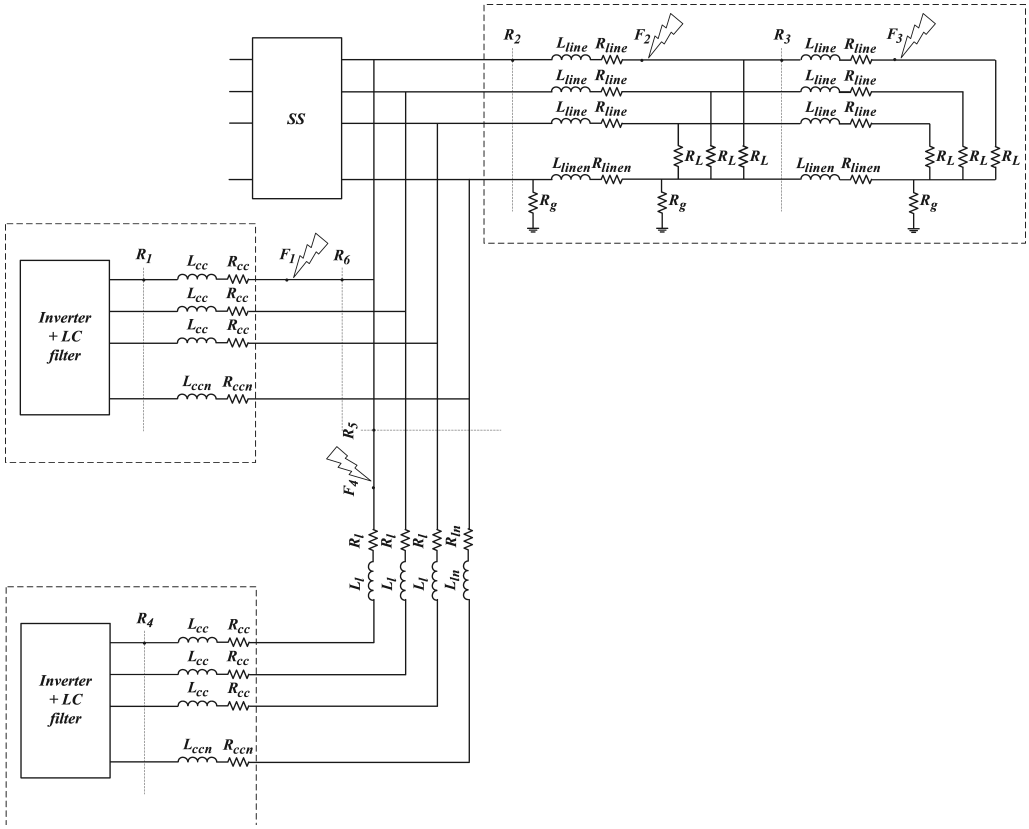


Figure 6.2: Microgrid supplied by two parallel-connected inverters: possible relay configuration

Table 6.7: Load unbalanced operation in a microgrid supplied by two parallel-connected inverters

20% load unbalance												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	42.67	25.39	25.34	320.12	323.70	323.81	31.13	5.94	5.61	322.54	1.50	1.42
R_2	74.57	48.00	48.27	315.06	323.38	321.44	56.93	9.69	7.95	319.94	2.17	3.98
R_3	36.11	23.71	23.89	279.03	308.56	309.64	27.89	4.61	3.60	299.00	5.34	14.64
R_4	32.37	22.66	23.11	327.33	328.45	328.81	26.01	3.88	2.57	328.19	0.98	0.65
R_5	32.37	22.66	23.11	315.06	323.38	321.44	26.01	3.88	2.57	319.94	2.17	3.98
R_6	42.67	25.39	25.34	315.06	323.38	321.44	31.13	5.94	5.61	319.94	2.17	3.98
50% load unbalance												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	56.42	15.43	15.02	318.59	327.19	327.24	28.93	13.70	13.81	324.32	3.47	3.51
R_2	94.94	31.96	32.36	310.30	330.40	325.34	53.03	22.34	19.57	321.94	5.03	9.79
R_3	44.93	15.93	16.20	254.06	325.94	328.49	25.64	10.44	8.84	302.39	12.32	35.05
R_4	39.36	16.59	17.46	327.61	330.31	331.00	24.28	8.94	6.34	329.63	2.26	1.61
R_5	39.36	16.59	17.46	310.30	330.40	325.34	24.28	8.94	6.34	321.94	5.03	9.79
R_6	56.42	15.43	15.02	310.30	330.40	325.34	28.93	13.70	13.81	321.94	5.03	9.79

limited in the NatRF. The inverters supply the same load as the in the microgrid model with a single inverter. Table 6.7 shows the phase-to-neutral voltages and currents at the different relay locations in the microgrid in Figure 6.2 for 20% load unbalance and 50% load unbalance. The 20% and 50% load unbalance is referred to the combined maximum power rating which is 34kVA. As it can be seen, the two inverters are quite capable of producing a balanced set of output voltages even with a 50% load unbalance. Again, it is assumed that the microgrid can operate with a maximum 20% load unbalance [13, 40]. While the 50% load unbalance has been considered to demonstrate later in the Chapter that the proposed fault detection does not malfunction for unbalances up to 50%.

In Chapter 4, the load in the two inverters-microgrid model was kept equal to the load in the single inverter-microgrid for the purpose of comparing the impact of different inverter controls on the microgrid fault response. However now, for the purpose of fault detection, different loading conditions will have to be considered.

Microgrid protection requirements

Compared with the single inverter microgrid case, the presence of two parallel inverters requires two extra relays, namely R_5 and R_6. Indeed the role of R_5 and R_6 is to detect the presence of a fault on the line connecting each inverter to the network (fault F_1 for R_6 and fault F_4 for R_5) and disconnect the affected branch and inverter from the microgrid.

Indeed, for faults at F_1 or F_4 the loads in the microgrid can still be supplied if they are within rating of the remaining inverter. In the case of a single inverter there is no such possibility and therefore a fault at F_1, see Figure 6.1, will simply cause the shut down of the whole microgrid.

The number and position of relays in Figure 6.2 is only one of the many possible configurations, nevertheless, it is felt that the presence of R_5 and R_6 is rather important in order to improve the reliability of power supply. Finally, following what has been said in Section 6.2.1 on the lack of specific protection standards for islanded microgrids, here it also assumed that the two inverters stay connected to the microgrid in order to allow the protection system to detect and clear any fault.

Fault detection in microgrids supplied by two parallel-connected inverters

This section presents the phase currents and voltages (expressed in terms of their peak values) with their corresponding sequence components at different relays locations (R_1, R_2, R_3, R_4, R_5 and R_6) for various types of fault at different locations (F_1, F_2, F_3 and F_4). These values have been determined by using the models developed in Chapter 5.

Table 6.8 shows the response of the system to a 3ϕ fault at points F_1, F_2, F_3 and F_4. As was the case for the stand-alone inverter, both inverters go into current limiting and the voltage experiences a big drop. Therefore, also this type of fault can be detected by measuring the drop in V_p. It should be noted that for faults at F_2 and F_3 the amount of current seen by R_2 and R_3 is rather high compared with the nominal load current values of 21.61A for R_2 and 10.74A for R_3, see Table 2.7. This increase is caused by the combined current capability of the two inverters. As the supplied current increases, some form of overcurrent fault detection could be used as well or instead.

Table 6.9 shows the results for a 2ϕ fault at F_1, F_2, F_3 and F_4. The high overvoltages are limited by the inverters' voltage limiting and as a result distorted waveforms are generated. Therefore the maximum phase values are not shown in this Table and the sequence components have been determined in PSCAD. The per-phase current limiting strategy results in zero sequence components in the current and voltage which are not normally presents in phase faults. As for the previous single inverter case, this fault can be detected with an increase in V_n which is well above the values during unbalanced operation.

Table 6.8: 3ϕ fault in a microgrid supplied by two parallel-connected inverters (values in yellow are chosen as indicators of the presence of a fault)

Fault at F_1												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	65.85	65.85	65.85	7.51	7.51	7.51	66.85	0	0	7.51	0	0
R_2	0	0	0	0.06	0.06	0.06	0	0	0	0.06	0	0
R_3	0	0	0	0.06	0.06	0.06	0	0	0	0.06	0	0
R_4	66.25	66.25	66.25	21.95	21.95	21.95	66.24	0	0	21.95	0	0
R_5	66.25	66.25	66.25	0.06	0.06	0.06	66.24	0	0	0.06	0	0
R_6	66.24	66.24	66.24	0.06	0.06	0.06	66.24	0	0	0.06	0	0
Fault at F_2												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	66.34	66.34	66.34	54.24	54.24	54.24	66.34	0	0	54.23	0	0
R_2	132.78	132.78	132.78	50.10	50.10	50.10	132.78	0	0	50.10	0	0
R_3	0	0	0	0	0	0	0	0	0	0	0	0
R_4	66.44	66.44	66.44	70.78	70.78	70.78	66.44	0	0	70.78	0	0
R_5	66.44	66.44	66.44	50.10	50.10	50.10	66.44	0	0	50.10	0	0
R_6	66.34	66.34	66.34	50.10	50.10	50.10	66.34	0	0	50.10	0	0
Fault at F_3												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	66.52	66.52	66.52	103.81	103.81	103.81	66.51	0	0	103.81	0	0
R_2	133.13	133.13	133.13	99.87	99.87	99.87	133.13	0	0	99.87	0	0
R_3	131.53	131.53	131.53	49.63	49.63	49.63	131.53	0	0	49.63	0	0
R_4	66.61	66.61	66.61	120.36	120.36	120.36	66.61	0	0	120.36	0	0
R_5	66.61	66.61	66.61	99.87	99.87	99.87	66.61	0	0	99.87	0	0
R_6	66.52	66.52	66.52	99.87	99.87	99.87	66.52	0	0	99.87	0	0
Fault at F_4												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	66.15	66.15	66.15	7.55	7.55	7.55	66.15	0	0	7.55	0	0
R_2	0	0	0	0.06	0.06	0.06	0	0	0	0.06	0	0
R_3	0	0	0	0.06	0.06	0.06	0	0	0	0.06	0	0
R_4	65.93	65.93	65.93	21.84	21.84	21.84	65.93	0	0	21.84	0	0
R_5	66.14	66.14	66.14	0.06	0.06	0.06	66.14	0	0	0.06	0	0
R_6	66.15	66.15	66.15	0.06	0.06	0.06	66.15	0	0	0.06	0	0

Table 6.9: 2ϕ fault in a microgrid supplied by two parallel-connected inverters (values in yellow are chosen as indicators of the presence of a fault)

Fault at F_1												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	41.90	23.76	6.79	262.59	260.32	193.81
R_2	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	16.9	16.88	11.52	261.40	261.08	193.45
R_3	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	8.41	8.40	5.62	255.18	254.86	177.38
R_4	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	39.36	23.71	4.72	269.41	257.56	199.46
R_5	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	39.41	23.79	4.72	261.30	260.98	193.71
R_6	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	22.41	40.55	6.79	261.30	260.98	193.71
Fault at F_2												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	40.81	22.81	6.85	284.62	234.40	188.08
R_2	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	78.66	45.18	11.08	282.62	235.45	186.5
R_3	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	8.31	8.30	5.4	253.15	252.84	170.48
R_4	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	38.08	22.69	4.20	293.15	228.46	190.17
R_5	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	38.04	22.74	4.24	282.78	235.54	186.48
Fault at F_3												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	39.86	22.21	6.94	304.18	208.41	178.93
R_2	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	77.03	44.03	10.62	301.7	209.54	178.72
R_3	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	67.75	51.31	5.2	272.81	226.92	163.77
R_4	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	37.05	21.88	3.71	312.28	203.61	183.3
R_5	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	37.14	21.97	3.76	301.95	209.81	178.39
Fault at F_4												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	41.96	23.86	6.81	262.80	260.36	193.90
R_2	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	16.9	16.88	11.52	261.56	261.25	193.61
R_3	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	8.41	8.40	5.62	255.44	255.13	177.30
R_4	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	39.32	23.68	4.72	269.43	257.84	199.74
R_5	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	25.07	40.74	4.73	261.30	260.98	193.71
R_6	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	41.94	23.81	6.80	261.56	261.25	193.61

Table 6.10: $2\phi g$ **fault in a microgrid supplied by two parallel-connected inverters (values in yellow are chosen as indicators of the presence of a fault)**

Fault at F_1												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	8.15	61.32	70.41	338.73	329.60	342.49	46.11	20.03	20.00	225.51	224.38	111.14
R_2	24.34	19.31	19.31	341.95	332.39	332.40	14.53	14.53	4.85	224.71	224.64	108.04
R_3	12.32	9.37	9.37	360.77	297.94	297.96	7.22	7.22	2.20	219.39	219.33	79.56
R_4	18.73	61.30	70.67	335.28	340.60	366.70	49.97	16.90	15.86	237.62	221.73	123.83
R_5	18.73	61.30	70.67	341.95	332.39	332.40	49.97	16.90	15.86	224.71	224.64	108.04
R_6	8.15	61.32	70.41	341.95	332.39	332.40	35.44	30.94	11.21	224.71	224.64	108.04
Fault at F_2												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	48.32	18.31	18.11	255.22	205.93	121.45
R_2	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	95.62	36.71	35.13	254.16	206.42	118.49
R_3	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	7.25	7.24	2.22	219.27	218.95	79.52
R_4	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	47.53	19.07	17.28	267.99	203.69	136.41
R_5	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	47.53	19.07	17.28	254.13	206.47	118.46
Fault at F_3												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	47.94	18.36	18.08	280.71	184.59	125.56
R_2	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	94.60	36.93	33.77	278.88	183.96	121.75
R_3	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	86.56	43.71	30.89	244.08	196.80	83.86
R_4	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	46.98	16.86	15.76	292.32	180.84	138.09
R_5	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	*n.a.*	46.86	16.68	15.81	270.62	185.10	122.26
Fault at F_4												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	8.15	61.32	70.41	338.73	329.63	342.55	46.11	20.03	20.00	225.59	224.33	111.17
R_2	24.34	19.31	19.31	341.95	332.39	332.40	14.53	14.53	4.85	224.71	224.64	108.04
R_3	12.32	9.37	9.37	360.77	297.94	297.96	7.22	7.22	2.20	219.39	219.33	79.56
R_4	18.73	61.30	70.67	335.29	340.56	366.64	49.97	16.90	15.86	237.54	221.78	123.80
R_5	18.73	57.01	60.64	341.95	332.39	332.40	31.72	34.49	15.17	224.71	224.64	108.04
R_6	8.15	61.32	70.41	341.95	332.39	332.40	46.11	20.03	20.00	224.71	224.64	108.04

Table 6.11: $1\phi n$ fault in a microgrid supplied by two parallel-connected inverters (values in yellow are chosen as indicators of the presence of a fault)

Fault at F_1												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	66.26	14.63	8.72	15.30	338.53	335.94	28.23	15.55	22.82	225.92	110.65	112.28
R_2	0.61	21.98	21.16	0.14	346.37	329.53	14.57	7.14	6.84	225.33	110.51	114.88
R_3	0.36	10.88	10.50	7.44	333.00	319.82	7.24	3.55	3.34	229.99	107.89	105.05
R_4	66.42	11.33	16.78	36.50	335.60	338.15	30.31	21.71	14.71	232.94	105.19	103.78
R_5	66.17	10.69	16.94	0.14	346.37	329.53	30.31	21.71	14.71	225.33	110.51	114.88
R_6	65.81	14.63	8.72	0.14	346.37	329.53	15.79	28.85	21.40	225.33	110.51	114.88
Fault at F_2												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	66.58	15.21	7.88	98.41	338.01	336.35	29.06	16.30	21.56	254.65	83.46	84.88
R_2	133.32	24.17	22.03	89.58	345.35	330.67	59.75	38.12	35.47	253.84	83.19	86.70
R_3	0.17	11.94	10.92	0.01	366.92	333.31	7.64	3.16	4.34	232.19	95.98	137.04
R_4	66.74	12.17	17.10	122.72	335.44	338.35	30.68	22.10	14.19	261.83	78.41	77.34
R_5	66.74	12.17	17.10	89.58	345.35	330.67	30.68	22.10	14.19	253.84	83.19	86.70
R_6	66.58	15.21	7.88	89.58	345.35	330.67	29.06	16.33	21.56	253.84	83.19	86.70
Fault at F_3												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	66.86	15.63	7.61	187.93	337.76	336.56	29.51	16.67	21.02	284.16	57.74	58.92
R_2	133.87	25.21	22.68	179.63	344.86	331.26	60.41	38.75	34.72	283.22	57.11	59.13
R_3	130.92	13.09	11.56	91.25	364.09	334.53	51.71	40.94	38.27	261.09	68.88	106.53
R_4	67.01	12.52	17.37	212.16	335.35	338.42	30.90	22.34	13.97	291.49	53.61	53.15
R_5	67.01	12.52	17.37	179.63	344.86	331.26	30.90	22.34	13.97	283.22	57.11	59.13
R_6	66.86	15.63	7.61	179.63	344.86	331.26	29.51	16.67	21.02	283.22	57.11	59.13
Fault at F_4												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	66.26	15.52	8.79	15.35	338.50	335.93	28.26	15.57	22.75	225.99	110.57	112.17
R_2	0.61	21.98	21.16	0.16	346.37	329.58	14.57	7.14	6.84	225.35	110.48	114.91
R_3	0.36	10.88	10.50	7.46	333.00	319.86	7.24	3.55	3.34	220.02	107.87	105.07
R_4	66.42	11.29	16.63	36.37	335.63	338.16	30.28	21.68	14.75	232.90	105.23	103.85
R_5	65.66	11.29	16.63	0.16	346.37	329.58	13.78	22.48	29.60	225.35	110.48	114.91
R_6	66.26	14.52	8.79	0.16	346.37	329.58	28.26	15.57	22.75	225.35	110.48	114.91

Table 6.12: $1\phi g$ **fault in a microgrid supplied by two parallel-connected inverters**

Fault at F_1												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	65.63	17.25	8.09	316.01	336.88	337.23	30.31	17.36	18.34	330.03	6.53	7.81
R_2	18.68	23.15	22.22	312.42	342.76	333.16	21.30	0.47	2.37	329.30	7.39	14.14
R_3	9.13	11.60	11.11	286.57	346.43	333.26	10.58	0.23	1.33	321.51	7.21	31.29
R_4	42.82	6.74	14.19	332.16	336.73	337.20	20.90	13.14	9.15	335.34	3.33	2.32
R_5	42.82	6.74	14.19	312.72	342.76	333.16	20.90	13.14	9.15	329.30	7.39	14.14
R_6	24.44	17.25	8.09	312.42	342.76	333.16	3.11	13.44	13.39	329.30	7.39	14.14
Fault at F_2												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	63.13	13.74	11.80	329.05	336.69	336.46	29.47	16.19	17.52	334.02	4.10	4.45
R_2	99.23	22.95	22.21	322.81	342.22	333.18	48.04	26.39	24.83	332.54	5.94	12.42
R_3	8.59	11.49	11.11	269.26	343.91	333.19	10.36	0.47	1.44	314.79	14.56	35.92
R_4	37.81	9.22	11.16	335.96	336.95	337.92	19.23	10.57	8.04	336.92	2.68	2.04
R_5	37.81	9.22	11.16	322.81	342.22	333.18	19.23	10.57	8.04	332.54	5.94	12.42
R_6	63.13	13.74	11.80	322.81	342.22	333.18	29.47	16.19	17.52	332.54	5.94	12.42
Fault at F_3												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	58.02	13.71	11.95	329.63	336.66	336.45	27.80	14.53	15.74	334.21	3.68	3.99
R_2	91.26	22.79	22.18	323.77	341.56	333.52	45.33	23.69	22.30	332.79	5.33	11.16
R_3	82.11	11.40	11.08	274.76	341.96	332.86	34.81	24.06	23.25	316.02	13.07	32.16
R_4	34.83	9.09	10.91	336.02	337.02	337.88	18.14	9.48	7.22	336.96	2.40	1.83
R_5	34.83	9.09	10.91	323.77	341.56	333.25	18.14	9.48	7.22	332.79	5.33	11.16
R_6	58.02	13.71	11.95	323.77	341.56	333.25	27.80	14.53	15.74	332.79	5.33	11.16
Fault at F_4												
Device	$I_a[A]$	$I_b[A]$	$I_c[A]$	$V_a[V]$	$V_b[V]$	$V_c[V]$	$I_p[A]$	$I_n[A]$	$I_0[A]$	$V_p[V]$	$V_n[V]$	$V_0[V]$
R_1	65.63	17.25	8.09	316.17	336.88	337.23	30.31	17.36	18.35	330.08	6.48	7.76
R_2	18.62	23.15	22.22	312.49	342.77	333.16	21.30	0.47	2.37	329.32	7.37	14.12
R_3	9.13	11.60	11.11	286.64	346.43	333.26	10.58	0.23	1.33	321.53	7.19	31.28
R_4	42.84	6.74	14.19	332.16	336.73	337.20	20.91	13.14	9.51	335.34	3.33	2.32
R_5	47.09	6.74	14.19	312.49	342.77	333.16	9.12	17.82	20.51	329.32	7.37	14.12
R_6	65.63	17.25	8.09	312.49	342.77	333.16	30.31	17.36	18.35	329.32	7.37	14.12

Table 6.13: Zero sequence component of the phase-to-earth voltages for unbalanced operation and $1\phi g$ faults

Device	20%*unbalance*	F_1	F_2	F_3	F_4
R_1	9.64	322.14	291.66	264.70	322.14
R_2	10.16	322.84	292.64	265.59	322.87
R_3	13.05	322.11	301.89	273.90	322.13
R_4	9.41	320.42	291.07	264.17	320.47
R_5	10.16	322.84	292.64	265.59	322.87
R_6	10.16	322.84	292.64	265.59	322.87

Table 6.10 shows the response to a $2\phi g$ fault. For faults at F_2 and F_3, the voltage limits are triggered and therefore current and voltage waveforms are distorted. This type of fault produces an increase in V_n which can be used to detect the presence of this type of fault.

The increase in the value of the negative sequence component of the voltage can be also used to detect $1\phi n$ faults as Table 6.11 shows. It is interesting to note that for faults at F_2 and F_3 the phase a current is again well above the nominal current values at R_2 and R_3. Therefore as for the corresponding case of three-phase faults at F_2 and F_3 overcurrent-based fault detection could be used.

Finally Table 6.12 shows the response of the microgrid to a $1\phi g$ fault. As expected and already illustrated, this type of fault may not trigger the inverter's current limiting as the combined current capacity is enough to supply the fault. Only faults at F_1 and F_4 triggers the current limiting of the first inverter. As a result the microgrid operates as an unbalanced system and the values of V_n and V_0 are rather well controlled. Therefore they cannot be used to indicate the presence of a fault.

An alternative to V_n and V_0 can be the zero sequence component of the phase voltage referred to earth. Table 6.13 compares the values of the zero sequence component of the phase-to-earth voltages V_{0e} for a 20% load unbalance and then for a $1\phi g$ fault at F_1, F_2, F_3 and F_4. The zero sequence component V_{0e} for $1\phi g$ faults is well above the values for unbalanced operation and therefore it can be used to detect the presence of this type of fault.

6.3 Voltage detection methods, their performance and application to fault detection in microgrids

The results shown in Sections 6.2.1 and 6.2.2 clearly point to voltage magnitude as the distinctive electrical quantity which can be used to detect the presence of a fault. Three-phase faults can be detected with the drop in the positive sequence component while unbalanced faults can be detected with the increase in the voltage negative sequence component. Single phase-to-ground faults with parallel-connected inverters, which do not cause current limiting and therefore produce no big increase in negative sequence voltage component, can still be detected by measuring the zero sequence components of the phase-to-earth voltage.

Ideally any fault should be detected and cleared as soon as possible in order not to interfere with the inverters own protection or create any stability problems. For this purpose voltage sag detection methods implemented in the microprocessor of a Solid State Transfer Switch (SSTS) seem to be rather appropriate. A SSTS is a device which is able to transfer the power supply of a sensitive load from a primary source which is experiencing some form of voltage disturbance to an alternative source. The voltage detection methods implemented in SSTS are particularly fast and are designed to be immune to false triggering caused by voltage transients and utility harmonics. As a result, these qualities make them the ideal candidate for fault detection in microgrids.

The following Sections start with a review of two voltage sag detection methods based on the dq transformation [90–92] and on the 90° phase shift operator [93, 94] and then illustrate a proposed fault detection technique suitable for islanded inverter-only microgrids.

6.3.1 Voltage sag detection method based on $dq\gamma$ transformation

The use of the SynRF transformation to calculate voltage magnitude has a significant advantage compared to processing voltage information in the StatRF or NatRF. The $dq\gamma$ transformation produces DC voltage signals which are easy to filter to eliminate any high frequency transients or harmonic components and to do so without changing the magnitude and phase of the system frequency component. Indeed, any filtering applied to sinusoidal waveforms is likely to introduce phase delay and magnitude attenuation. This is the main reason behind the popularity of this approach in SSTS where voltage sags

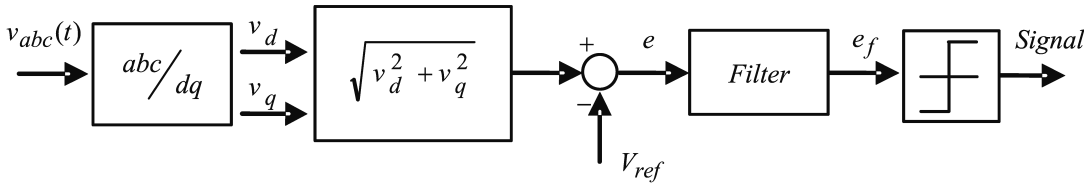


Figure 6.3: Block diagram of voltage detection method based on $dq\gamma$ transformation

have to be detected in an accurate and fast way.

A block diagram of a voltage detection method based on $dq\gamma$ transformation as proposed in [90,91] is shown in Figure 6.3. The instantaneous utility voltages $v_a(t)$, $v_b(t)$ and $v_c(t)$ are transformed into SynRF as described in Appendix A. Assuming balanced operation, the resulting components v_d and v_q are equal to:

$$\begin{aligned} v_d &= \sqrt{\frac{3}{2}} V \cos(\theta) \\ v_q &= \sqrt{\frac{3}{2}} V \sin(\theta) \end{aligned} \tag{6.1}$$

where V is the maximum voltage magnitude and θ is the phase voltage. By knowing v_d and v_q it is straight forward to determine V as follows:

$$V = \sqrt{\frac{2}{3}} \sqrt{v_d^2 + v_q^2}. \tag{6.2}$$

Once V is determined, it is possible to determine the presence of a voltage sag by simply comparing V with a reference value V_{ref} to give an error signal, e (Figure 6.3). The error is filtered to give e_f and if this is above a certain limit then a voltage sag is indicated.

A very important role is played by the filter block in Figure 6.3 as it affects the speed and the accuracy of the voltage detection method. Ideally, the method should detect a change in magnitude as quickly as possible and at the same time be immune to any voltage transient or harmonic distortion. In particular, v_d and v_q may contain 2ω ripple for unbalanced operation, where ω is the system angular frequency, and 6ω and 12ω ripples caused by harmonic components (see Appendix A for further explanation) together with some high frequency components caused by voltage transients.

A first solution to this problem is to use a low-pass filter with a cut-off frequency f_c around 50Hz. This scheme is effective and accurate but not very fast because of the delay introduced by f_c. The higher f_c, the faster the response of the filter and the shorter

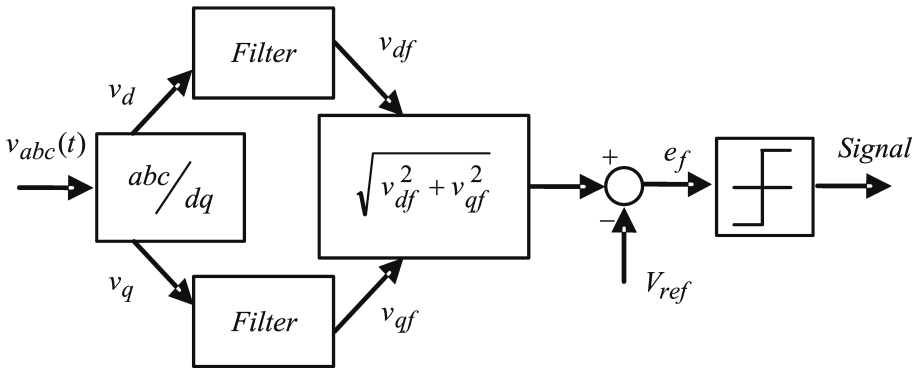


Figure 6.4: Block diagram of detection method with a notch filter

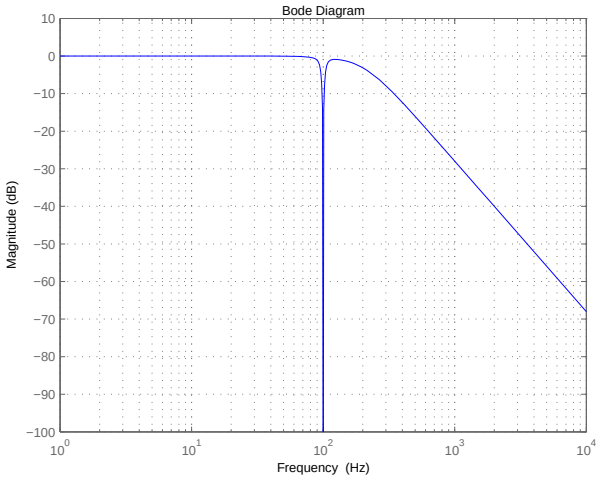


Figure 6.5: Bode diagram of the notch low-pass filter in Figure 6.4

the detection time, but, if the filter has a high f_c, then the detector is more sensitive to voltage transients and harmonic components.

Reference [92] proposes a slightly different detection method, see Figure 6.4, in order to reduce the impact of unbalanced faults on dq components and improve the speed of the detection strategy. This time the dq voltage components are first passed through a filter whose Bode magnitude diagram is shown in Figure 6.5. The filter contains a notch 2ω to eliminate any 2ω ripple for unbalanced faults and a low pass filter ($f_c = 200Hz$) to attenuate voltage transients. After the filtering, V is calculated and compared with V_{ref} in the same way as the previous method. The use of a notch enables the f_c of the filter to be set high so that the response is very fast, compared to simple low-pass filter alone, and, as a result, the fault can be detected quickly.

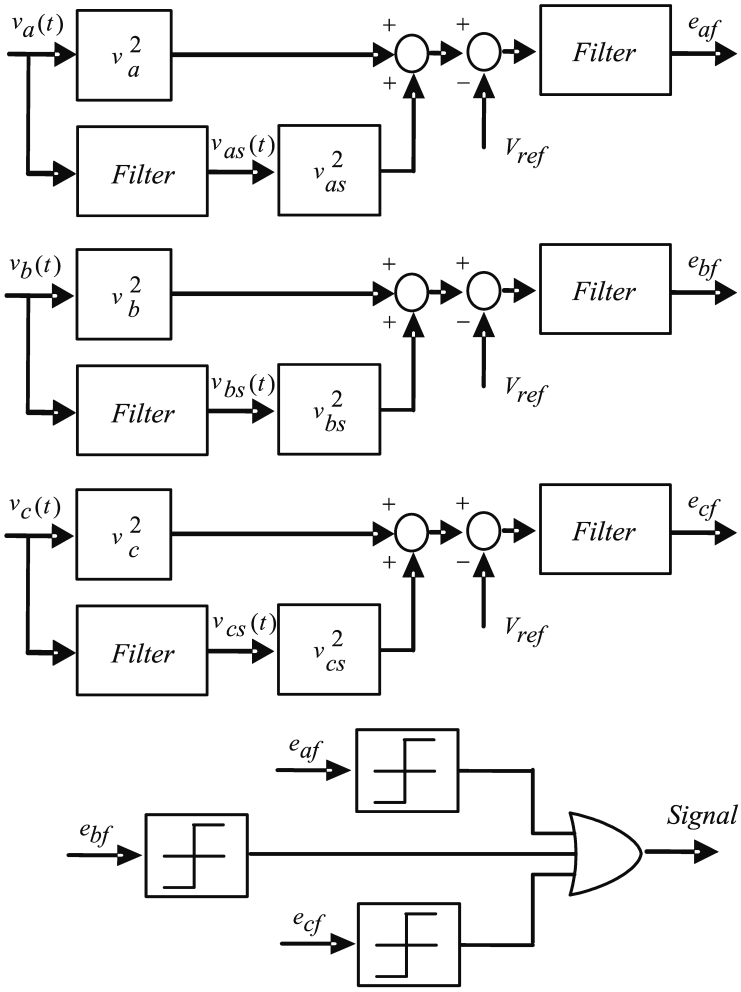


Figure 6.6: Block diagram of detection method with phase shift filter

6.3.2 Voltage sag detection method based on a 90-degree phase shift operator

The basic principle of this method [93,94], which is shown in Figure 6.6, is that the sum of two squared sinusoidal waveforms with a 90° phase shift is equal to a constant value. So, each phase voltage is passed through an all-pass filter which shifts the signal by 90°. The two signals for each phase, e.g. $v_a(t)$ and $v_{as}(t)$, are squared, summed and then compared to a reference value. The resulting error is filtered with a low-pass filter ($f_c = 50Hz$) in order to remove voltage transients. Finally the output is compared with a threshold to detect the presence of any disturbance.

6.3.3 Comparison of detection methods

In this section, the performance of the three detection methods is compared for various types of fault. In order to do so, the analytical expressions of the *dq* components of the voltage for a single phase-to-ground, double phase-to-ground and phase-to-phase faults have been derived and can be found in Appendix C. These are the input signals for the testing of the voltage sag detection methods based on the SynRF transformations and the use of a low-pass filter (see Figure 6.3) or notch filter (see Figure 6.4). The low-pass filter is designed to have a 50 Hz cut-off frequency while the notch filter is designed to have a notch at 100 Hz and a 200 Hz cut-off frequency. For both methods V_{ref} is equal to 80% of the voltage pre-fault level. For the testing of the 90° phase shift method, the input signals $v_a(t)$, $v_b(t)$ and $v_c(t)$ (see Figure 6.6) for each fault can be found in Appendix C. The transfer function of the all pass filter is

$$H(s) = \frac{1 - \frac{s}{\omega}}{1 + \frac{s}{\omega}} \tag{6.3}$$

where ω is the system frequency. The low-pass filter in Figure 6.6, which filters the error, is again designed with a 50 Hz cut-off frequency.

The three voltage sag detection methods with different input signals were coded in Matlab and their response, in terms of detection times, to various types of fault was obtained with the use of the "lsim"function in Matlab. The "lsim"function is able to simulate the time response of a continuous system to arbitrary inputs. Figures 6.7, 6.8, 6.9, 6.10 and 6.11 compare the detection times of the three methods for various types of fault.

Generally speaking the detection times are rather small, in the order of few milliseconds, and always less than half a cycle. From the response to a three-phase fault in Figures 6.7 and 6.8 it can be seen that the detection times are much smaller compared to the ones for unbalanced faults. As severity of the voltage sag increases, the corresponding detection times decrease to 1 or 2ms. The three methods do not show any major differences in the response however the method with the notch filter is generally faster than the other two.

From the responses to unbalanced faults it can be seen that the detection times are quite dependent on the type of fault and on the voltage phase angle at the time the fault happens. The longer detection times, at close to 8 ms, are for single phase-to-ground

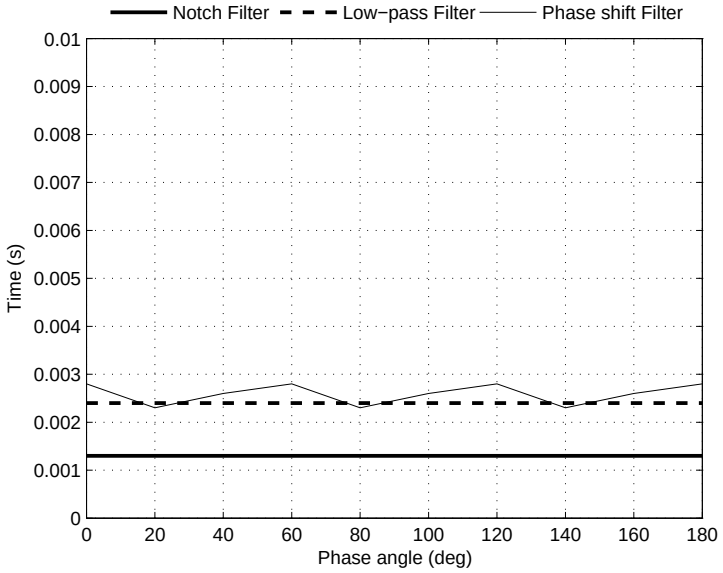


Figure 6.7: Detection times for a three-phase fault with voltage drop to 60% nominal value

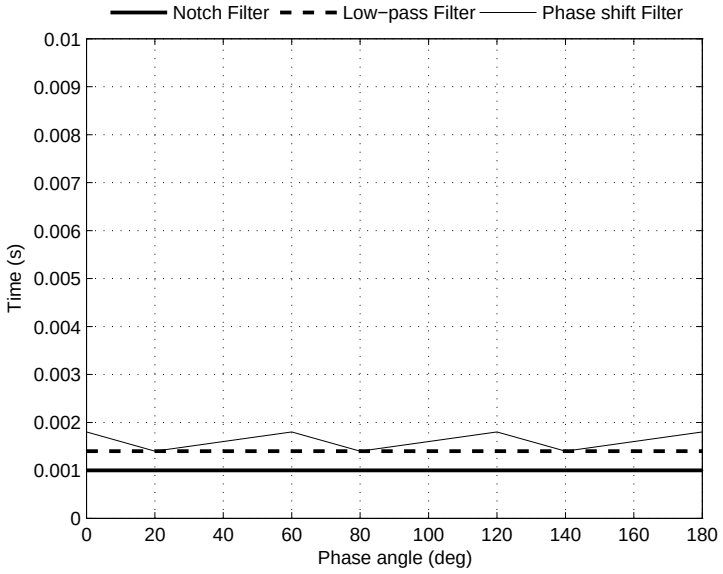


Figure 6.8: Detection times for a three-phase fault with voltage drop to 40% nominal value

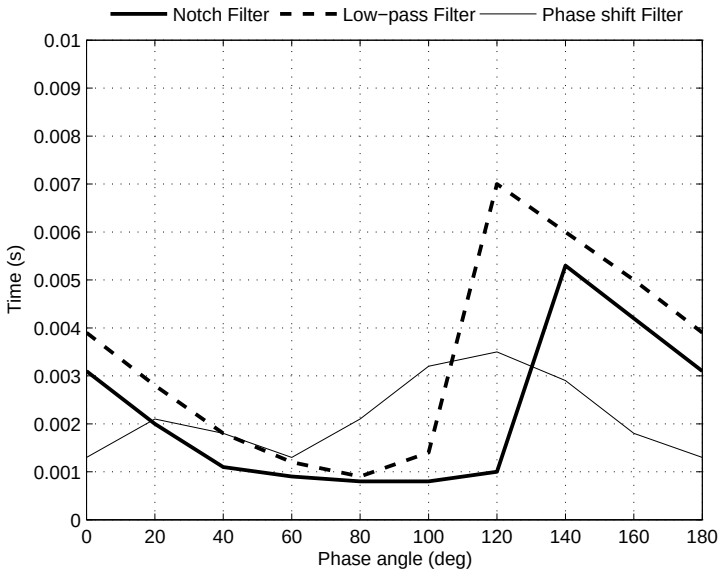


Figure 6.9: Detection times for a phase-to-phase fault (b-c)

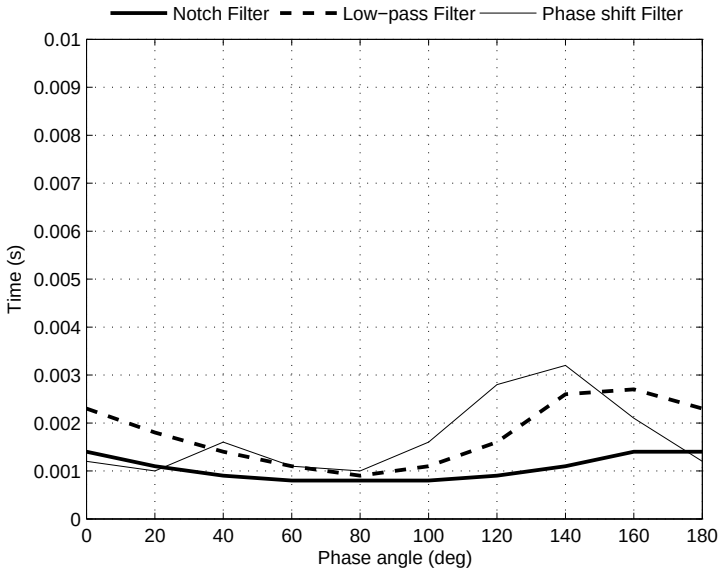


Figure 6.10: Detection times for a double phase-to-ground fault (b-c-g)

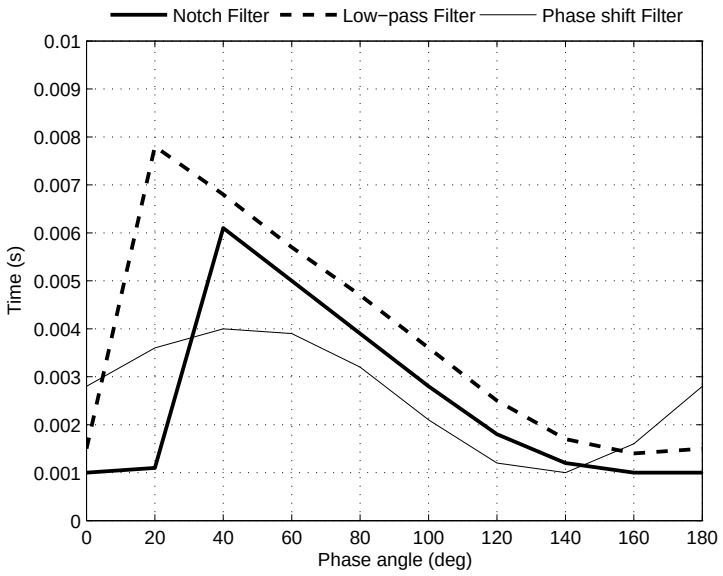


Figure 6.11: Detection times for a phase-to-ground (a-g) fault

faults with the low pass filter method. As expected, the notch filter gives a faster response compared with the low pass filter as its bandwidth is higher.

The method based on the 90° phase shift filter has a good performance for unbalanced faults, sometimes it is even faster than the notch filter method, but for three-phase faults it is slower.

The detection times shown are based on analytical expression and therefore they do not take into account other factors like the dynamics of the voltage in the event of the fault and any time associated with the online measurement and processing of voltages. Nevertheless, overall these methods are capable of detecting any drop in the voltage in few milliseconds with the notch filter method having the best performance over the other two methods.

In conclusion, the purpose of this Section and of Sections 6.3.1 and 6.3.2 has been to illustrate different methods which process voltage signals and detect the presence of voltage sags. The next Section is going to show how to adapt these methods to design a sequence-component voltage detection technique which can be then used to detect the presence of faults in islanded inverter-only microgrids.

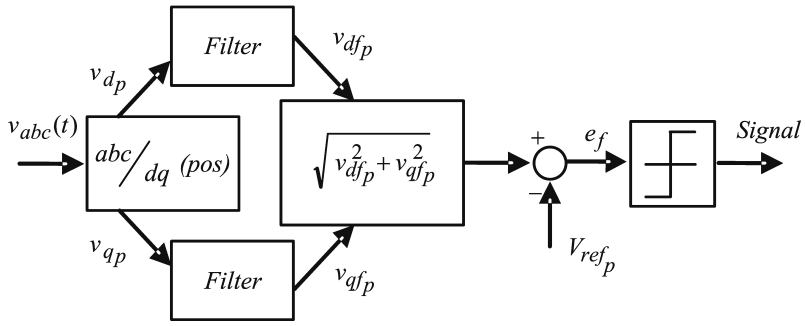


Figure 6.12: Positive sequence detector block

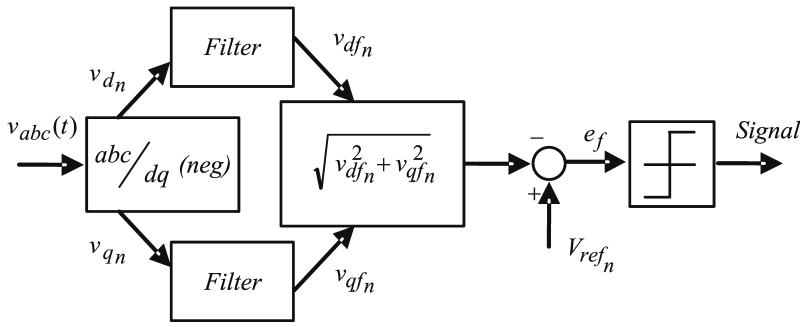


Figure 6.13: Negative sequence detector block

6.3.4 A fault detection technique based on voltage sequence components

In Section 6.2 it has been shown that the various types of fault make characteristic changes in the sequence components observed. These are: (i) large reduction of V_p for 3ϕ faults; (ii) increase of V_n for unbalanced faults; (iii) increase in V_{0e} for $1\phi g$ faults in microgrids supplied by two parallel inverters. The sequence components of the voltage can be obtained by modifying the voltage sag detection methods based on the SynRF with a notch filter and on the NatRF with a 90° phase shift filter.

In particular, Figure 6.12 shows how the positive sequence component can be obtained by using the *dq* transformation as in (A.7) and a filter with a low-pass filter with notch at 2ω. The negative sequence component can be determined by applying the modified Park transformation as in (4.12) and then filtering any 2ω component caused by the positive sequence component with a notch filter as shown in Figure 6.13. Once the positive and negative sequence components of the voltage have been determined, each of them is compared with a reference value and if V_p is below its reference value or V_n is above its reference value, then the presence of a fault in the microgrid is indicated.

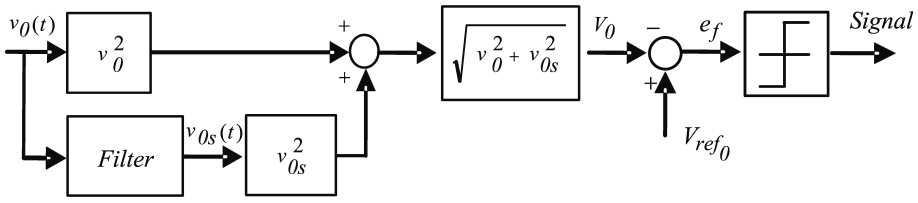


Figure 6.14: Zero sequence detector block

The zero sequence component of the phase-to-earth voltage, which is used to detect $1\phi g$ faults in microgrids with parallel inverters, can be determined by applying the extraction technique illustrated in Section 6.3.2. In particular, the zero sequence component is calculated by summing up the three phase-to-earth voltages and then by passing the obtained signal through the extractor block in Figure 6.14. Once the zero sequence component is obtained, it is compared with a reference value and if it is above it then a fault is indicated.

In conclusion, the proposed fault detection technique based on voltage sequence components is made by three voltage signal detector blocks: (i) one which extracts V_p and detects a drop in its value (see Figure 6.12); (ii) one which extracts V_n and detects an increase in its value (see Figure 6.13); (iii) one which extracts V_{0e} and detect an increase in its value (see Figure 6.14).

6.4 Voltage-based fault protection in an islanded inverter-only microgrid: two illustrative examples

The purpose of the next two Sections is to give an example for each microgrid under study of how to implement a fault protection system based on voltage detection. The three detector blocks described in Section 6.3.4 are implemented in the PSCAD models and the performance of the proposed fault detection technique is analyzed. Examples are given on how to design a selective protection strategy and extra protection requirements to complement the voltage-based protection are discussed.

6.4.1 Voltage-based fault protection in a microgrid supplied by a single inverter

Each location (R_1, R_2 and R_3) in Figure 6.1 is equipped with three blocks capable of detecting any drop in the positive sequence component of the voltage (V_p) and any increase

Table 6.14: Detection times for faults at F_1

	3ϕ	2ϕ	$2\phi g$	$1\phi g$	$1\phi n$
$t_{det_{R1}}[ms]$	3.2	2.4	3.0	2.5	0.9
$t_{det_{R2}}[ms]$	3.1	2.7	2.7	3.6	1.3
$t_{det_{R3}}[ms]$	3.2	3.4	3.8	6.4	3

Table 6.15: Detection times for faults at F_2

	3ϕ	2ϕ	$2\phi g$	$1\phi g$	$1\phi n$
$t_{det_{R1}}[ms]$	3.5	2.6	2.8	3.0	1.2
$t_{det_{R2}}[ms]$	3.4	2.9	3.0	4.1	1.5
$t_{det_{R3}}[ms]$	3.1	3.5	3.8	6.5	3.1

in the negative sequence component of voltage (V_n) as described in Section 6.3.4. The settings at each location are chosen as follows:

- a fault is indicated if V_p drops below 80% of its nominal value;
- a fault is indicated if V_n goes above three times its value at 20% load unbalanced operation (see Table 6.1).

Settings at R_1, R_2 and R_3 for V_n are 4.23V, 6.12V and 10.95V respectively. As it can be seen, these settings are well above the corresponding values of V_n for 50% load unbalance (see Table 6.1). This allows a safety margin between unbalanced operation and fault indication.

The same types of fault considered in Section 6.2 are applied again at locations F_1, F_2 and F_3 and Tables 6.14, 6.15 and 6.16 show the detection times $t_{det_{R1}}$, $t_{det_{R2}}$ and $t_{det_{R3}}$ of the extractor blocks at R_1, R_2 and R_3 for faults at F_1, F_2 and F_3 respectively. As expected, detection times are short and all in the order of few milliseconds. These detection times are relative to faults applied at t=1s, however, as shown in Section 6.3.3, detection times are strongly dependent on the voltage phase angle. So, for example, for a single phase-to-ground fault applied at t=1.0025s (around $\frac{\pi}{4}$ on phase a) at F_1, the detection time for the device at R_1 increases from 2.5 ms to 9.5 ms. Nevertheless, it can be said that faults are detected in less than 15ms.

Table 6.16: Detection times for faults at F_3

	3ϕ	2ϕ	$2\phi g$	$1\phi g$	$1\phi n$
$t_{det_{R1}}[ms]$	3.8	2.8	3.0	3.5	1.4
$t_{det_{R2}}[ms]$	3.8	3.1	3.3	4.6	1.9
$t_{det_{R3}}[ms]$	3.4	3.8	4.1	7.3	3.6

By applying the inverter fault models developed in Chapter 5, it is possible to consider various microgrid operating conditions (e.g. different loading conditions including overloading) and then to verify that the fault detection strategy operates correctly. For example, it is important to know what degree of overload would create a large enough reduction in V_p to give a false indication of a fault. Figure 6.15 shows the inverter phase output currents, the positive sequence component of the phase-to-neutral voltages at locations (R_1, R_2 and R_3) and the active power supplied by the inverter for increasing loading conditions in the microgrid. These values were obtained by representing in phase coordinates the inverter as three controlled voltage sources with a series in impedance Z_0, the microgrid network as in Figure 5.12 and the loads as varying impedances. No current limiting was considered in order to study the response of the microgrid to different loadings. The nominal load operation (two loads of 5.6kW each) is highlighted with a dashed vertical line together with the inverter nominal output active power P_n highlighted by the horizontal dashed line. From Figure 6.15 it can be seen that an increase in load produces only a small drop in V_p. It can also be seen that an overload twice P_n does not produce any current limiting and therefore no big drop in V_p is registered. It follows that there is no possibility of malfunctioning of the fault detection method for overload operation between P_n and $2 * P_n$. For sustained inverter overloading conditions above P_n, the inverter protection will act, after a pre-defined time, and disconnect the inverter.

A sudden load increase above twice P_n does cause the inverter to go into current limiting. Figure 6.16 shows what happens to the positive sequence component V_p for different overloads which do cause current limiting. Once the inverter operates as a current source, the microgrid becomes equivalent to the model in Figure 5.24 where the voltage is controlled by the network's impedances. With the overload increasing above twice P_n, the value of the value of V_p drops until it reaches the horizontal dashed line in Figure 5.24 which represents 80% of the nominal voltage value. For this condition, the fault detection

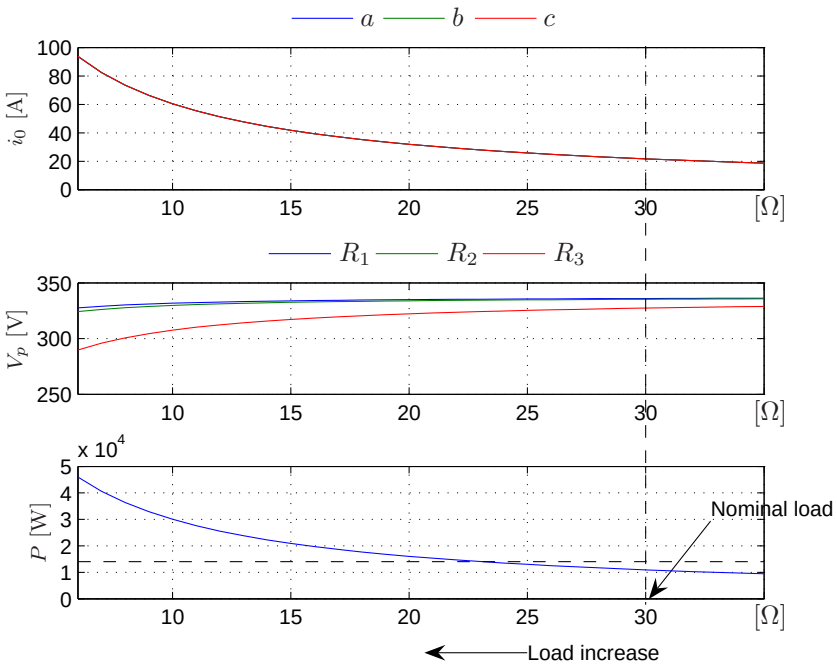


Figure 6.15: Operation of a single inverter microgrid for varying load with no current limiting

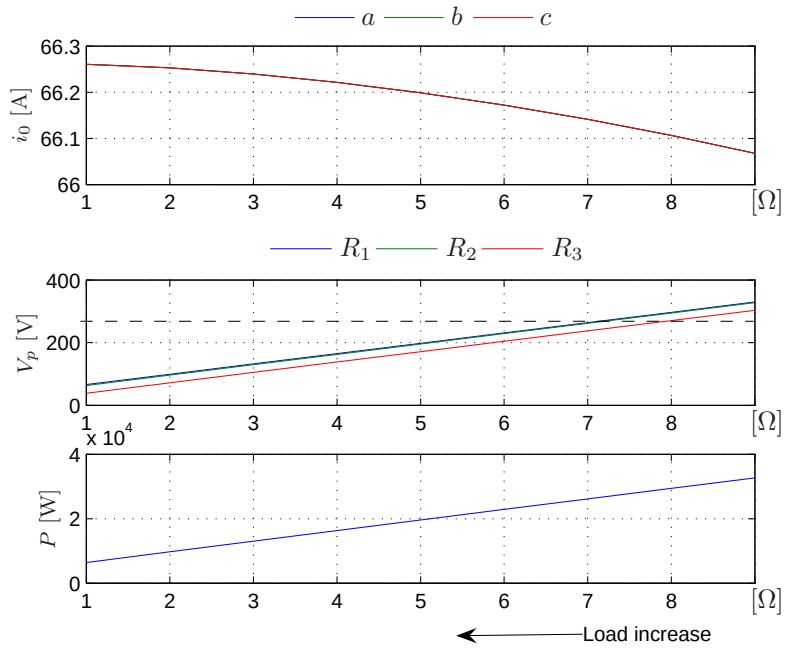


Figure 6.16: Operation of a single inverter microgrid for overloads which do cause current limiting

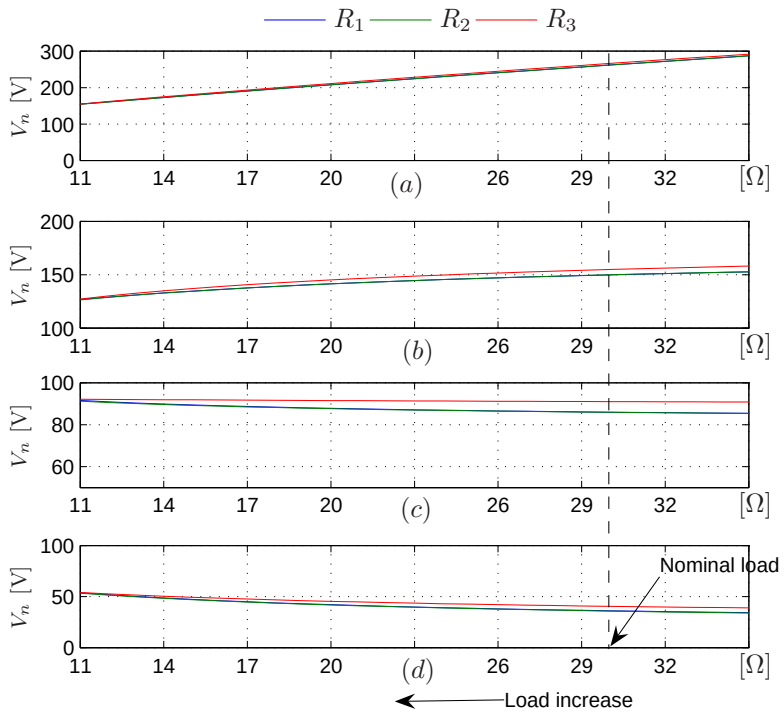


Figure 6.17: Behaviour of V_n at R_1, R_2 and R_3 for different unbalanced faults at F_3 in a single inverter microgrid for varying loads: (a) 2ϕ fault, (b) $2\phi g$ fault, (c) $1\phi n$ fault, (d) $1\phi g$ fault

strategy indicates the presence of a 3ϕ fault. However, this malfunction is unlikely to happen as the load in the microgrid should not be allowed to increase above the rating of its inverters.

The fault detection strategy for unbalanced faults has been tested in PSCAD for the microgrid nominal load however, loading affects the voltage magnitude in the event of a fault. Therefore it is important to verify V_n is sufficiently high that unbalanced faults can be detected regardless of the load present. Figure 6.17, which uses the models in Chapter 5, shows what happens to the values of V_n at R_1, R_2 and R_3 for unbalanced faults at F_3 with varying load conditions. The dashed line indicates the nominal microgrid load (i.e. two resistive loads of 5.6 kW each). As expected, the values of V_n are load dependent but they are always well above the reference values of V_n (4.23V, 6.12V and 10.95V) which cause the triggering of the voltage detection strategy. As a result, varying loads do not interfere with the detection of unbalanced faults.

So far, it has been shown that the use of voltage makes possible the detection of various faults. However the use of voltage makes it difficult to locate and selectively eliminate a fault. Protection can be made selective by assigning delays to some devices. For the specific protection of the microgrid in Figure 6.1, the fault detection at R_3 was chosen to have no delay, the one at R_2 to have a 10 cycle delay [13, 40] and then the same delay was chosen for the device at R_1. So for example, for a fault at F_3, the detection at R_3 will occur first and open the circuit while devices at R_1 and R_2 do not command any action. For a fault at F_2 or F_1, first the fault will be sensed at R_3 and a tripping signal will be sent and then after 10 cycles devices at R_1 and R_2 will open as well.

Overall this microgrid offers a rather limited example of protection studies. Indeed little selectivity is required and there are no additional DG units which could possibly form new islands as a result of the tripping of some breakers in the event of a fault. The next example will show that as soon as the number of inverters and the complexity of the microgrid network increase, protection requirements increase as well.

6.4.2 Voltage-based fault protection in a microgrid supplied by two parallel-connected inverters

Consider the microgrid in Figure 6.2. At each point R_1, R_2, R_3, R_4, R_5 and R_6, 3ϕ faults are going to be detected by a drop in V_p, unbalanced faults are going to be detected with an increase in V_n and $1\phi g$ faults are going to be detected with an increase in V_{0e}. The

Table 6.17: Detection times for faults at F_1, parallel-connected inverters

	3ϕ	2ϕ	$2\phi g$	$1\phi g$	$1\phi n$
$t_{det_{R1}}[ms]$	3.2	0.7	0.7	1.4	1.0
$t_{det_{R2}}[ms]$	3.2	1.0	1.0	1.4	1.3
$t_{det_{R3}}[ms]$	3.2	3.5	4.3	1.5	3.6
$t_{det_{R4}}[ms]$	3.4	0.7	0.7	1.4	1.0
$t_{det_{R5}}[ms]$	3.2	1.0	1.0	1.4	1.3
$t_{det_{R6}}[ms]$	3.2	1.0	1.0	1.4	1.3

Table 6.18: Detection times for faults at F_2, parallel-connected inverters

	3ϕ	2ϕ	$2\phi g$	$1\phi g$	$1\phi n$
$t_{det_{R1}}[ms]$	3.9	1.4	1.2	1.4	1.7
$t_{det_{R2}}[ms]$	3.8	1.9	1.7	1.5	2.0
$t_{det_{R3}}[ms]$	3.2	5.5	5.8	1.5	4.1
$t_{det_{R4}}[ms]$	4.2	1.3	1.1	1.5	1.5
$t_{det_{R5}}[ms]$	3.8	1.9	1.7	1.5	2.0
$t_{det_{R6}}[ms]$	3.8	1.9	1.7	1.5	2.0

settings are similar to the ones for a stand-alone inverter microgrid which are 80% voltage drop in the nominal value of V_p, three times the value of V_n for 20% load unbalance (see Table 6.7) and three times the values of V_{0e} for 20% load unbalance (see Table 6.13).

The faults simulated in Section 6.2.2 are applied again at locations F_1, F_2, F_3 and F_4 and Tables 6.17, 6.18, 6.19 and 6.20 show the corresponding detection times for the fault detection techniques implemented at R_1, R_2, R_3, R_4, R_5 and R_6. As expected, these detection times are rather small however they are relative to faults applied at t=1s and very much dependent on the voltage phase angle. Nevertheless, simulations show that it can be safely assumed that detection times are below 15 ms. Some unbalanced faults may produce a drop in the positive sequence component of the voltage as well, therefore they can be detected by measuring any drop in V_p. However not all faults produce a sharp drop and moreover simulations show that detection times are longer that the ones obtained by using V_n.

Different microgrid operating conditions can be again studied with the developed inverter fault models and the direct phase coordinates representation of the microgrid. As for the case of the microgrid supplied by a single inverter, overloads below twice the

Table 6.19: Detection times for faults at F_3, parallel-connected inverters

	3ϕ	2ϕ	$2\phi g$	$1\phi g$	$1\phi n$
$t_{det_{R1}}[ms]$	4.9	5.1	2.4	1.5	2.7
$t_{det_{R2}}[ms]$	4.7	5.2	5.3	1.5	3.4
$t_{det_{R3}}[ms]$	3.8	5.9	6.3	1.6	5.5
$t_{det_{R4}}[ms]$	5.3	5.1	2.0	1.5	2.5
$t_{det_{R5}}[ms]$	4.7	5.2	5.3	1.5	3.4
$t_{det_{R6}}[ms]$	4.7	5.2	5.3	1.5	3.4

Table 6.20: Detection times for faults at F_4, parallel-connected inverters

	3ϕ	2ϕ	$2\phi g$	$1\phi g$	$1\phi n$
$t_{det_{R1}}[ms]$	3.2	0.7	0.7	1.4	1.0
$t_{det_{R2}}[ms]$	3.2	1.0	1.0	1.4	1.3
$t_{det_{R3}}[ms]$	3.2	3.5	4.3	1.5	3.6
$t_{det_{R4}}[ms]$	3.4	0.7	0.7	1.4	1.0
$t_{det_{R5}}[ms]$	3.2	1.0	1.0	1.4	1.3
$t_{det_{R6}}[ms]$	3.2	1.0	1.0	1.4	1.3

inverters' nominal power P_n produce only a small drop in V_p and therefore the voltage detection does not indicate any fault. Because of the unequal load sharing of the two inverters during transients, a further increase in the load causes one inverter to go into current limiting before the other. Nevertheless, as the load keeps increasing (i.e. R_L diminishes), both inverters go into current limiting and V_p decreases to a point where the presence of a fault is indicated. Again, this is not to be considered as a malfunction of the detection strategy as a high increase in load in a microgrid is generally not advisable.

Similarly to what has been done in Section 6.4.1, the inverter models developed in Chapter 5 can be used to analyze the behaviour of V_n and V_{0e} for varying loads in the microgrid. Indeed, it has to be verified that unbalanced faults can be detected with an increase in V_n (2ϕ, $2\phi g$ and $1\phi n$ faults) or an increase in V_{0e} ($1\phi g$ faults) independently of the load in the network. For example, Figure 6.18, shows the influence of varying loads on the values of V_n and V_{0e} at R_1, R_2, R_3 and R_4 for various unbalanced faults applied at F_3. It can be seen that the values of V_n and V_{0e} are always above the thresholds which have been set at the beginning of this section to indicate the presence of a fault.

It has to be noted that in Figure 6.18, the values of V_n for a 2ϕ and a $2\phi g$ faults

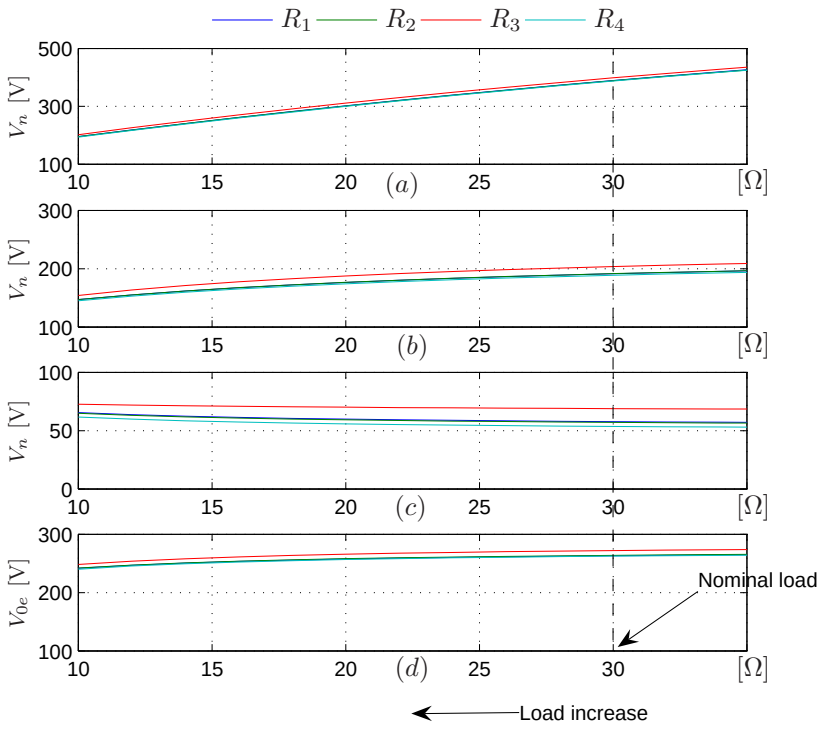


Figure 6.18: Behaviour of V_n and V_{0e} at R_1, R_2 and R_3 for different unbalanced faults at F_3 in a two-inverters microgrid for varying loads: (a) 2ϕ fault, (b) $2\phi g$ fault, (c) $1\phi n$ fault, (d) $1\phi g$ fault

at nominal load operation (see the dashed line) are above the corresponding values in Tables 6.9 and 6.10. This is because the inverter limits the overvoltages created by the fault. Nevertheless, the resulting limited values of V_n are still high enough to indicate the presence of a fault. Moreover, Figure 6.18, in particular diagrams (a) and (b), shows that an increase in load produces a decrease in the magnitude of the overvoltage on faulty phases until the voltage is well within the inverters' ratings.

An increase in load results also in the triggering of current limiting in the first inverter for a $1\phi g$ fault at F_3. Only big overloads (e.g. $R_L = 5\Omega$) cause both inverters to go into current limiting for the same fault. However, as discussed before, big overloads are unlikely to be allowed in the microgrid. It follows that V_{0e} has always to be used to detect $1\phi g$ faults in this microgrid model.

If V_p, V_n and V_{0e} can be used to detect the presence of a fault, again it is rather difficult to use them to locate the fault and selectively isolate it. Moreover as there are two inverters, there has to be some form of coordination in the protection system which allows one generator to be disconnected while the other one keeps on supplying loads. For the example of a fault at F_1, devices at R_1 and R_5 should disconnect while the second inverter should remain connected. This is the main reason behind the choice of having a disconnecting device and fault detection at R_5 and R_6. However by only using voltage sequence components, devices at R_5 and R_6 cannot distinguish between faults inside their protected area (F_1 for the device at R_6 and F_4 for the device at R_5). A possible solution to this problem is to place at R_5 and R_6 a current-based directional element which can sense if the fault is inside or outside the protected zone. Consequently, as the only function of these two devices is to sense the direction of the fault current, they do not need to have any other detection technique based on voltage sequence components.

The protection system should also be selective for faults at F_3 and F_2. In particular for a fault at F_3, only the downstream load should be disconnected thus allowing the load upstream the fault to be still supplied. A possible solution could be to assign to each device a delay. So for example R_3 can have a 10-cycle delay, followed by a 20-cycle delay for R_2, R_1 and R_4 while R_5 and R_6 do not have any delay.

For a fault at F_3, detection at R_1, R_2, R_3 and R_4 is alerted but as R_3 has the smallest delay, it is the first device to disconnect. For a fault at F_2 first R_3 will open, then R_2 followed by R_1 and R_4. By placing another delay at R_1 and R_4 it could even be

possible to keep the inverters connected while supplying no load for a fault at F_2. For a fault at F_1 (or F_4) the directional element at R_6 (or R_5) will operate first thus allowing the second inverter to stay connected. Tripping of device at R_1 (or R_4) will soon follow after a delay or could be activated by an inter-tripping signal from R_6 (or R_5)

Overall it can be said that as the system becomes bigger in size, its requirements increase and therefore the complexity of the fault detection and protection increases as well. The design of a protection system based on of voltage sequence components with the addition of directional elements at R_5 and R_6 can potentially give a good performance.

6.5 Conclusions

This Chapter has shown how it is possible to detect the presence of a fault in islanded inverter-only microgrids and how this detection strategy can be used in the design of a microgrid protection system. As inverters dominate the response of the microgrid, it has been possible to propose a suitable fault detection strategy (based on voltage only) from the analysis of the impact of the inverters' control on the microgrid fault behaviour. Indeed, the simulations in Chapter 4 and the modelling in Chapter 5 have provided the right knowledge and tools to find an answer to the problem of microgrid fault detection.

Voltage can be successfully used to detect the presence of a fault because the triggering of the current limiting breaks the inverter voltage control loop. Under normal operation, the inverter control is designed to produce a balanced output voltage with little influence from loading conditions. However, as soon as the inverter goes into current limiting, then the voltage is no longer controlled and then it exhibits abnormal behaviour (e.g. drops in positive sequence components and rises in negative sequence components). When current limiting does not happen, like for single phase-to-ground faults in parallel inverters microgrids, then an alternative way to detect the fault had to be found.

Overall this Chapter has shown that from the point of view of fault detection, parallel-connected inverters do not give a good response for $1\phi g$ faults. The bad load sharing of the two inverters causes unpredictable different responses which require the use of simulations, to determine the behaviour, and the use of an alternative fault detection. Ideally in the event of a fault, the two inverters should share the load equally and go into current limiting. This would produce a predictable behaviour and allow the use of V_n to detect any type of unbalanced fault. The flexibility provided by inverters control can

possibly achieve a better response.

The proposed voltage detection technique with its three detector blocks borrowed from the signal processing methods implemented in SSTSs give very small detection times. However the time which is needed by protective devices to clear fault is above the milliseconds range. So for example, the 10-cycle time discrimination margin proposed in Sections 6.4.1 and 6.4.2 is the minimum value which can be used [13]. However, this means that inverters may have to remain connected and supply enough current for many cycles before the fault is cleared. This requirement on inverters is not easy to meet as usually inverters are designed to supply current or power above their ratings only for few cycles. As a result, there is a strong need to design a fast acting protection system which possibly has to use solid-state breakers which would allow smaller time discrimination margins. Moreover inverters capabilities have to be chosen according to the requirements of the microgrid protection system.

Finally, it is understood that the proposed solutions to fault detection have been tailored to the two specific microgrid models, however the approach used in this Chapter and in the whole thesis can be considered as a guideline in the design of microgrid protection and can be exported to other microgrid models.

Chapter 7

Conclusion and future work

7.1 Concluding remarks

Secure and reliable power supply is one of the claimed benefits of microgrid operation. Consequently, a microgrid's own protection system should be designed to fulfil this objective (e.g. by quickly disconnecting the microgrid in the event of a grid disturbance) and the protection system should not degrade the microgrid performance through false tripping or failure to clear a fault. As the number of inverter-interfaced DG units increases and the operation of islanded inverter-only microgrids becomes possible, it is therefore of prime importance, for microgrid protection design purposes, to understand how the microgrid can respond in the event of a fault, how this response can be modelled and how faults can be detected.

At the moment, there is limited knowledge on how inverters behave during network faults and on the factors affecting this behaviour. This lack in knowledge is mainly caused by the novelty of the problem (i.e. inverter only microgrid operation) and then by the diversified and heterogeneous expertise which is required in order to address the problem. Indeed, from one side, the power systems community is not very familiar with inverters, their design and control while, on the other side, the power electronics community is not usually concerned by power systems fault analysis studies and design of protection.

It is clear that microgrids require re-examination of the established assumptions about how generators respond to faults and how faults are detected and cleared. This research work has first shown how the control of the inverter is able to shape the response of the microgrid in the event of a fault. Depending on the control choices, it is possible, for example, to choose to maintain the control over healthy phase voltages or to generate distorted waveforms by using instantaneous current limiting. The only constraints to

this shaping capability are the inverter's ratings (i.e. current and voltage limits) and the topological change in the network introduced by each fault.

While simulating faults in microgrids, it has been shown that the fault response of certain inverter control methods can be considered better than others. In particular, the popular inverter control in the SynRF with PI regulators does not give a good fault response as the global current limiting in the SynRF is not easy to implement and produces high overvoltages for asymmetric faults. In contrast, control in the NatRF, which was not popular until recent studies, gives a better controlled response by limiting the fault current and maintaining the control of voltage on healthy phases. For microgrids and in general for DG applications, the inverter control has to be designed bearing in mind not only normal steady-state operation but also faulted network operation.

The inverter's ratings, and in particular the limited overcurrent and overloading capabilities, require different fault detection approaches and faster disconnecting devices than conventional generation. On the other hand, LV distribution networks have their own requirements, which include limited overvoltages and low waveform distortion, and their specific system design characteristics, such as slow speed overcurrent protection devices. As a result, the juxtaposition of the inverter's response and ratings and the network's operation requires the development of standards which can regulate and harmonize the fault response of microgrids and the microgrid protection requirements.

This thesis has also developed inverter fault models and integrated them in fault analysis studies. The availability of these models can aid understanding and design of fault detection and protection in reduced fault current environments like inverter-only microgrids. The ability to model the inverter's behaviour can serve this purpose in two ways. First, by knowing the behaviour of the microgrid a suitable way to detect the presence of a fault can be implemented. Indeed in this thesis the inverter models have been successfully used in the design of the voltage-based fault detection. Second, the knowledge of the factors influencing fault response can be used to devise new inverter control strategies which can give a better response and aid fault detection. The conventional approach is to make the fault protection suit the system fault response. However, the flexibility of inverter control coupled with the analysis here opens up the interesting possibility of reversing the relationship and making the fault response suit a convenient means of protection.

The analytical models of the form described here may also contribute in another

way. It has to be acknowledged that the models proposed are reliant on access to data on the control characteristics of the inverter. At present such data may not be readily available from manufacturers. However, the models constitute a way in which such data could be condensed and presented by the manufacturers without disclosing the full control system. In effect, the model captures the key aspects of the fault response of inverters (i.e., current limits and equivalent impedances) in a similar manner to the widely used simplified models of synchronous machines. The development and common acceptance of such equivalent models will take time but studies such as this are a starting point for further discussion in the academic and industrial community.

Finally, the proposed fault detection strategy has demonstrated that it is possible to protect inverter-only microgrids with reduced fault current by using alternative electrical quantities like voltage sequence components. The proposed technique is supported and justified by a thorough analysis of the microgrid system and its fault response.

7.2 Author's contribution

Overall, the main novelty and originality of the work presented in this thesis is the focus on the control system of inverters in order to study the fault behaviour and fault detection of microgrids. Indeed, the very few studies on fault analysis with inverter-interfaced DG [29, 32] and microgrid protection [40, 44] do not consider the inverters' control and do not investigate the factors affecting the inverters' fault response and more generally the network's fault response.

The author's specific contribution in this thesis can be summarized in three main points as follows.

A systematic approach to the analysis of inverter-only microgrid fault behaviour

In Chapter 3 all the aspects which have to be considered when studying microgrid fault behaviour have been compiled and methodically described. This description can improve the time consuming process of analyzing and collecting the information which is required for microgrid modelling and which varies from earthing arrangements to the reference frame for implementation of the inverter control.

As the microgrid is usually formed in a LV distribution network, it is important to

represent it as a four-wire system, including earth connections, and to consider unbalanced operation. Such approach has been carried out throughout the whole thesis.

Chapter 4 has presented an analysis of the fault behaviour of three microgrid models. These three models have been chosen by following an incremental approach in which first a single inverter-supplied microgrid is considered (first two microgrid models) and then a microgrid supplied by two parallel-connected inverters is studied (third microgrid model). The difference between the first two models lies only in the different reference frame implementation of the control of the single inverter. This chosen approach has contributed to the simplification of the analysis of the impact of inverters in the fault behaviour of the microgrid.

For each model, the inverter's control, its current limiting and unbalanced operation have been described. Different faults have been simulated and for each model the results of these simulations have been analyzed and compared with the others. It is recognized that the microgrid models presented encompass only three (SynRF, NatRF and droop control) of the many mechanisms that have been proposed for control of inverters. However the framework and the approach used in this analysis can be applied to other microgrid models.

Development of inverter fault models

Inverter fault models have been developed and validated in Chapter 5. Once again, starting from the inverter's control and the different reference frame implementations, it has been possible to derive equivalent phase circuits which can model the fault response of single inverters controlled in the SynRF and NatRF and of parallel-connected droop-controlled inverters. These equivalent models, which can capture the complex inverter control actions, are made by a combination of physical network parameters and control gains.

In these fault models, the inverter is usually represented as a constant current source with a parallel impedance. In some cases, the inverter model is the Norton equivalent of what was a voltage source with a series impedance. Some models are balanced and therefore it has been possible to determine their sequence component representation and use them in sequence-component–based fault analysis. Other models are unbalanced because of the per-phase current limiting strategy. The thesis has shown how to use the unbalanced (and also the balanced) inverter fault models in numerical fault analysis based on

an equivalent direct phase coordinates representation of the network.

Development of a fault detection strategy suitable for inverter-only microgrids

In Chapter 6 a fault detection technique based on voltage has been developed and its performance tested. As current limiting is triggered, the control over the inverter output voltage is lost and therefore the voltage sequence components can be used as an alternative way to detect faults when the available fault current is too small to provide discrimination.

Again, an incremental approach has been used and therefore two basic microgrid models have been considered: one supplied by one inverter and another supplied by two parallel-connected inverters. First, for each model, the microgrid operation including unbalance and the microgrid protection requirements have been discussed. Then the inverter fault models have been used to compute the behaviour of the microgrid for various faults at various locations. Following consideration of these numerical results, voltage sequence components have been chosen to detect the presence of a fault. In particular, a drop in the positive sequence component of the voltage detects the presence of a three-phase fault while an increase in the negative sequence component of the voltage detects the presence of an unbalanced fault.

In order to implement the proposed fault detection strategy in PSCAD, various voltage detection methods presently used by transfer switches have been considered and from them three methods to extract voltage sequence components were chosen and built in PSCAD. The performance of the proposed fault detection strategy has been simulated, tested and discussed. Finally, a microgrid protection system based on voltage detection has been illustrated.

7.3 Suggestions for future work

The flexibility in the inverter control and the potential to shape the microgrid fault response need to be further investigated. The thesis has stressed the importance of having a well defined fault response for fault protection purposes. So, for example, it has been pointed out that the response of droop controlled inverters during $1\phi g$ faults and their load sharing should be improved in order to give a predictable response (i.e. both inverters in the example microgrid should enter current limiting). However, more studies are needed to understand what the desired fault response should be and how to control inverters in

order to produce it. It can be predicted that the desired fault response will be influenced by:

- the need to protect customers from undesired network disturbances while maintaining a regulated and distortion-free supply of power;
- the protection system of the host network;
- the control and design options available for inverters.

During the design of the fault detection strategy, it has been assumed that inverters remain connected to the microgrid until the fault is cleared. It has also been assumed that the inverters' own protection system does not interfere with the microgrid protection system. These assumptions require further studies, including models of prime movers and DC bus dynamics, in order to understand what are the conditions and the system requirements which can make these assumptions valid.

The microgrid models considered in Chapter 6 need to be expanded and include additional DG sources. Further studies should consider more scattered DG units with the possibility of forming new islands as a result of the tripping of breakers. Coordination between microgrid protection, DG unit protection and intertripping should be considered as well.

Finally the gap between the work based on simulations/modelling and the "real life"inverters and microgrids has to be bridged. First, the fault behaviour of inverters, which has been simulated in Chapter 4 and modelled in Chapter 5, has to be experimentally verified. Second, the proposed fault detection strategy has to be implemented and tested. The implementation in a lab of the various inverter control methods and the different microgrid network models does not only allow the verification of the results presented in this thesis but it also has the potential to demonstrate to a wider audience, including network operators and manufacturers, the feasibility of operating an islanded system supplied by inverters in the event of a fault.

Experimental implementation gives the possibility of studying even further the fault behaviour of inverters and their equivalent models for the purposes of (i) developing standard fault models and encouraging manufacturers to supply the data needed, (ii) developing some testing procedures which can give all the data needed for the inverter fault models. The comparison with the standard practice with synchronous machines is very

strong. Indeed, synchronous machines have well defined fault models whose parameters are usually supplied by manufacturers but can also be determined through standard testing procedures. Similarly, it would be very useful to have standard inverter models whose parameters can be determined if not supplied by the manufacturer.

Author's Publication

- M. Brucoli and T. C. Green , "A fault detection technique suitable for power electronic network devices," in *Proc. University Power Engineering Conference 2005 (UPEC05)*, September 2005, vol. 2, pp. 1170-4.
- R. Tumilty, M. Brucoli, G. M. Burt and T. C. Green, "Approaches to Network Protection for Inverter Dominated Electrical Distribution Systems," in *Proc. 3rd IET International Conference on Power Electronics Machines and Drives (PEMD 2006)*, April 2006, pp. 622-626.
- M. Brucoli and T. C. Green , "Fault response in inverter dominated microgrids," in *Proc. 2nd International Conference on Integration of Renewable and Distributed energy Resources*, December 2006.
- M. Brucoli and T. C. Green , "Fault response on inverter dominated microgrids," *International Journal of Distributed Energy Resources*, vol. 3, no. 2, pp. 157-175, April/June 2007.
- M. Brucoli, T. C. Green and J.D.F. McDonald, "Modelling and analysis of fault behaviour of inverter microgrids to aid future fault detection," in *Proc. IEEE International Conference on System of Systems Engineering (SoSE 2007)*, April 2007, pp. 1-6.
- M. Brucoli and T. C. Green, "Fault behaviour in islanded microgrids," in *Proc. 19th International Conference on Electricity Distribution (CIRED 2007)*, May 2007, no. 0548.
- M. Brucoli, J.D.F. McDonald and T. C. Green, "Analytical models for computation of fault behaviour of islanded inverter-only microgrids ," *IET Generation, Transmission and Distribution*, (In preparation).

Bibliography

[1] T. Ackermann, G. Andersson, and L. Soder, "Distributed generation: a definition," *Electric Power Systems Research*, vol. 57, no. 3, pp. 195–204, 2001.

[2] N. Jenkins, R. Allan, P. Crossley, D. Kitschen, and G. Strbac, *Embedded generation*, IEE Power and Energy Series, London, 2004.

[3] CIGRE C6.04.01 Taskforce, "Connection criteria at the distribution network for distributed generation," Final Report, February 2007.

[4] P. P. Barker and R. W. De Mello, "Determining the impact of distributed generation on power systems. i. radial distribution systems," in *Proc. IEEE Power Engineering Society Summer Meeting*, July 2000, vol. 3, pp. 1645–1656.

[5] N. Hatziargyriou, H. Asano, R. Iravani, and C. Marnay, "Microgrids," *IEEE Power and Energy Magazine*, vol. 5, no. 4, pp. 78–94, July/August 2007.

[6] B. Lasseter, A. Abbas, C. Marnay, J. Stevens, J. Dagle, R. Guttromsom, A. Sakis Meliopoulos, R. Yinger, and J. Eto, "Integration of distributed energy resources: The certs microgrid concept," Consortium for Electric Reliability Technology Solutions, April 2002.

[7] A. Arulampalam, M. Barnes, A. Engler, A. Goodwin, and N. Jenkins, "Control of power electronic interfaces in distributed generation microgrids," *International Journal of Electronics*, vol. 91, no. 9, pp. 503–523, September 2003.

[8] W. E. Feero, D. C. Dawson, and J. Stevens, "White paper on protection issues of the microgrid concept," Consortium for Electric Reliability Technology Solutions, March 2002.

[9] E. Lakervi and E. J. Holmes, *Electricity distribution network design*, IEE Power and Energy Series, London, 1989.

[10] F. Katiraei, M. R. Iravani, and P. W. Lehn, "Micro-grid autonomous operation during and subsequent to islanding process," *IEEE Transactions on Power Delivery*, vol. 20, no. 1, pp. 248–257, January 2005.

[11] C. A. Hernandez-Aramburo, T. C. Green, and N. Mugniot, "Fuel consumption minimization of a microgrid," *IEEE Transactions on Industry Applications*, vol. 41, no. 3, pp. 673–681, May/June 2005.

[12] A. L. Dimeas and N. D. Hatziargyriou, "Operation of a multiagent system for microgrid control," *IEEE Transactions on Power Systems*, vol. 20, no. 3, pp. 1447–1455, August 2005.

[13] J. M. Gers and E. J. Holmes, *Protection of Electricity distribution networks*, IEE Power and Energy Series, London, 2004.

[14] S. R. Wall, "Performance of inverter interfaced distributed generation," in *Proc. IEEE/PES Transmission and Distribution Conference Exposition*, 28 Oct.-2 Nov. 2001, vol. 2, pp. 945–950.

[15] IEEE Std 929-2000, "Recommended practice for utility interface of photovoltaic systems," IEEE, 2000.

[16] S. M. Brahma and A. A. Girgis, "Effect of distributed generation on protective device coordination in distribution system," in *Proc. Large Engineering Systems Conference on Power Engineering*, July 2001, pp. 115–119.

[17] R. C. Dugan and T. E. McDermott, "Operating conflicts for distributed generation on distribution systems," in *Proc. Rural Electric Power Conference*, April/May 2001, vol. 1, pp. A3/1–A3/6.

[18] T. Ackermann and V. Knyazkin, "Interaction between distributed generation and the distribution network: operation aspects," in *Proc. IEEE PES Transmission and Distribution Conference and Exhibition*, October 2002, vol. 2, pp. 1357–1362.

[19] K. Kauhaniemi and L. Kumpulainen, "Impact of distributed generation on the protection of distribution networks," in *Proc. Eighth IEE International Conference on Developments in Power System Protection*, April 2004, vol. 1, pp. 315–318.

[20] K. Maki, S. Repo, and P. Jarventausta, "Effect of wind power based distributed generation on protection of distribution network," in *Proc. Eighth IEE International Conference on Developments in Power System Protection*, April 2004, vol. 1, pp. 327–330.

[21] S. M. Brahma and A. A. Girgis, "Microprocessor-based reclosing to coordinate fuse and recloser in a system with high penetration of distributed generation," in *Proc. IEEE Power Engineering Society Winter Meeting*, January 2002, vol. 1, pp. 27–31.

[22] Engineering recommendation G.59/1, "Recommendations for the connection of embedded generating plants to the public electricity suppliers' distribution systems," 1991.

[23] IEEE P1547, "Standard for interconnecting distributed resources with electric power systems," IEEE, 2003.

[24] R. A. Walling and N. W. Miller, "Distributed generation islanding - implications on power system dynamic performance," in *Proc. IEEE Power Engineering Society Summer Meeting*, 2002, vol. 1, pp. 92–96.

[25] M. Fontela, C. Andrieu, S. Bacha, N. Hadjsaid, and Y. Besanger, "On the use of distributed generation to increase eps robustness," in *Proc. 2005 IEEE Power Engineering Society Summer Meeting*, June 2005, vol. 3, pp. 2991–2998.

[26] C. Jauch, J. Matevosyan, T. Ackermann, and S. Bolik, "International comparison of requirements for connection of wind turbines to power systems," *Wind Energy*, vol. 8, pp. 295–306, July 2005.

[27] N. R. Ullah, T. Thiringer, and D. Karlsson, "Voltage and transient stability support by wind farms complying with e.on netz grid code," *IEEE Transactions on Power Systems*, vol. 22, no. 4, pp. 1647–1656, November 2007.

[28] IEEE Std P1547.4/Draft 1.3, "Draft guide for design, operation, and integration of distributed resource island systems with electric power systems," IEEE, 2006.

[29] M. E. Baran and I. El-Markaby, "Fault analysis on distribution feeders with distributed generators," *IEEE Transactions on Power Systems*, vol. 20, no. 4, pp. 1757–1764, November 2005.

[30] J. J. Grainger and W.D. Stevenson, *Power system analysis*, McGraw-Hill, 1994.

[31] W. Freitas, J.C.M. Vieira, A. Morelato, L.C.P. da Silva, V.F. da Costa, and F.A.B. Lemos, "Comparative analysis between synchronous and induction machines for distributed generation applications," *IEEE Transactions on Power Systems*, vol. 21, no. 1, pp. 301–311, February 2006.

[32] R. A. N. Nimpitiwan, G. T. Heydt, and S. Suryanarayanan, "Fault current contribution from synchronous machine and inverter based distributed generators," *IEEE Transactions on Power Delivery*, vol. 22, no. 1, pp. 634–641, January 2007.

[33] D. Iioka, H. Shimizu, Y. Yokomizu, M. Goto, and T. Matsumura, "Effects of fault current limiter installed in ccustomer system on suppression of fault current and voltage sag," in *Proc. IEEE 2003 Power Tech Conference*, June 2003, vol. 12.

[34] G. Tang and M. R. Iravani, "Application of a fault current limiter to minimize distributed generation impact on coordinated relay protection," in *Proc. International Conference on Power Systems Transients, Montreal, QC, Canada*, 19-23 June 2005.

[35] W. El-Khattam and T. S. Sidhu, "Restoration of directional overcurrent relays coordination in distributed generation systems utilizing fault current limiter," *IEEE Transactions on Power Delivery*, vol. 23, no. 2, pp. 576–585, April 2008.

[36] M. E. Baran and I. El-Markaby, "Adaptive over current protection for distribution feeders with distributed generation," in *Proc. IEEE PES Power Systems Conference and Exposition*, October 2004, vol. 2, pp. 715–719.

[37] I. Chilvers, N. Jenkins, and P. Crossley, "Distance relaying of 11 kv circuits to increase the installed capacity of distributed generation," *IEE Proceedings Generation, Transmission and Distribution*, vol. 152, no. 1, pp. 40–46, January 2005.

[38] H. Y. Li, P. A. Crossley, and N. Jenkins, "Transient directional protection for distribution feeders with embedded generations," in *Proc. 14th Power Systems Computation Conference*, June 2002, vol. 03, Paper 05.

[39] Zeng Xiangjun, K.K. Li, W. L. Chan, and Su Sheng, "Multi-agents based protection for distributed generation systems," in *Proc. IEEE International Conference on Electric Utility Deregulation, Restructuring and Power Technologies*, April 2004, vol. 1, pp. 393–397.

[40] H. Nikkhajoei and R. H. Lasseter, "Microgrid protection," in *Proc. IEEE Power Engineering Society General Meeting*, June 2007, pp. 1–6.

[41] R. M. Tumilty, M. Brucoli, G. M. Burt, and T. C. Green, "Approaches to network protection for inverter dominated electrical distribution systems," in *Proc. 3rd IET International Conference on Power Electronics, Machines and Drives*, April 2006, pp. 622–626.

[42] "www.inverter.co.uk," Accessed on 04/08/08.

[43] "www.inveter.co.jp," Accessed on 04/08/08.

[44] W. Xueguang, N. Jayawarna, Y. Zhang, N. Jenkins, J. Peças Lopes, C. Moreira, A. Madureira, and J. Pereira da Silva, "Protection guidelines for a microgrid," Deliverable DE2 for EU Microgrids project, June 2005.

[45] N. Jayawarna, C. Jones, M. Barnes, and N. Jenkins, "Operating microgrid energy storage control during network faults," in *Proc. IEEE 2nd System of Systems Engineering Conference*, April 2007, pp. 1–7.

[46] H. Al-Nasseri, M. A. Redfern, and R. O'Gordman, "A voltage based protection for micro-grids containing power electronic converters," in *Proc. IEEE Power Engineering Society General Meeting*, June 2006, pp. 1–7.

[47] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*, John Wiley and Sons Inc, 1989.

[48] B. Lasseter and P. Piagi, "Control and design of microgrid components," Consortium for Electric Reliability Technology Solutions, January 2006.

[49] D. M. Divan, "Inverter topologies and control techniques for sinusoidal output power supplies," in *Proc. 6th Annual Applied Power Electronics Conference and Exposition*, March 1991, pp. 81–87.

[50] R. Zhang, D. Boroyevich, V. H. Prasad, H. Mao, F. C. Lee, and S. Dubovsky, "A three-phase inverter with a neutral leg with space vector modulation," in *Proc. 12th Annual Applied Power Electronics Conference and Exposition*, February 1997, vol. 2, pp. 857–863.

[51] G. Venkataramanan and M. Illindala, "Microgrids and sensitive loads," in *Proc. IEEE Power Engineering Society Winter Meeting*, January 2002, vol. 1, pp. 315–322.

[52] M. Prodanović and T. C. Green, "A survey of control methods for parallel three-phase inverters connection," in *Proc. IEE PEVD Conference Publication*, September 2000, pp. 472–477.

[53] IEEE 142-1991, "Recommended practice for grounding of industrial and commercial power systems," IEEE, 1991.

[54] IEEE 446-1995, "Recommended practice for emergency and standby power systems for industrial and commercial applications," IEEE, 1995.

[55] N. Jayawarna, N. Jenkins, M. Barnes, M. Lorentzou, S. Papathanassiou, and N. Hatziagyriou, "Safety analysis of a microgrid," *International Journal of Distributed energy Resources*, vol. 2, no. 4, pp. 261–278, October - December 2006.

[56] M. J. Ryan and R. D. Lorenz, "A high performance sine wave inverter controller with capacitor current feedback and back-emf decoupling," in *Proc. IEEE 26th Annual Power Electronics Specialists Conference*, June 1995, pp. 507–513.

[57] P.C. Loh, M.J. Newman, D. N. Zmood, and D. G. Holmes, "Improved transient and steady state voltage regulation for single and three phase uninterruptible power supplies," in *Proc. IEEE 32nd Annual Power Electronics Specialists Conference*, June 2001, vol. 2, pp. 498–503.

[58] Y. Li, D. M. Vilathgamuwa, and P. C. Loh, "Microgrid power quality enhancement using a three-phase four-wire grid-interfacing compensator," *IEEE Transactions on Industrial Applications*, vol. 41, no. 6, pp. 1707–1719, November/December 2005.

[59] M. Prodanović and T. C. Green, "High-quality power generation through distributed control of a power park microgrid," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 5, pp. 1471–1482, October 2006.

[60] M.C. Chandokar, D.M. Divan, and A. Rambabu, "Control of parallel connected inverters in stand-alone ac supply systems," *IEEE Transactions on Industrial Applications*, vol. 29, no. 1, pp. 136–143, Jan./Feb. 1993.

[61] T. Kawabata, T. Miyashita, and Y. Yamamoto, "Dead beat control of three phase pwm inverter," *IEEE Transactions on Power Electronics*, vol. 5, no. 1, pp. 21–28, January 1990.

[62] N. Abdel-Rahim and J.E. Quaicoe, "Three-phase voltage-source ups inverter with voltage-controlled current-regulated feedback control scheme," in *Proc. 20th International Conference on Industrial Electronics, Control and Instrumentation, IECON 1994*, September 1994, vol. 1, pp. 497–502.

[63] N. Pogaku, M. Prodanović, and T. C. Green, "Modeling, analysis and testing of autonomous operation of inverter-based microgrids," *IEEE Transactions on Power Electronics*, vol. 22, no. 2, pp. 613–625, March 2007.

[64] A. Tuladhar, H. Jin, T. Unger, and K. Mauch, "Parallel operation of single phase inverter modules with no control interconnections," in *Proc.Twelfth AnnualApplied Power Electronics Conference and Exposition, APEC '97*, February 1997, vol. 1, pp. 94–100.

[65] F. Katiraei and M. R. Iravani, "Power management strategies for a microgrid with multiple generation units," *IEEE Transactions on Power Systems*, vol. 21, no. 4, pp. 1821–1831, November 2006.

[66] E.Barklund, N. Pogaku, M.Prodanović, C. A. Hernandez-Aramburo, and T. C. Green, "Energy management system with stability constraints for stand-alone autonomous microgrid," in *Proc. IEEE International Conference on System of Systems Engineering (SoSE '07)*, April 2007, pp. 1–6.

[67] P. Mattavelli, "Synchronous-frame harmonic control for high-performance ac power supplies," *IEEE Transactions on Industry Applications*, vol. 37, no. 3, pp. 864–872, May/June 2001.

[68] F. Blaabjerg, Chen Ze, and S.B. Kjaer, "Power electronics as efficient interface in dispersed power generation systems," *IEEE Transactions on Power Electronics*, vol. 19, no. 5, pp. 1184–1194, September 2004.

[69] M. Brucoli and T.C. Green, "Fault response of inverter dominated microgrids," *International Journal of Distributed Energy Resources*, vol. 3, no. 2, pp. 157–175, April/June 2007.

[70] M. Brucoli and T.C. Green, "Fault behaviour in islanded microgrids," in *19th International Conference on Electricity Distribution CIRED 2007*, May 2007, number 0548.

[71] X. Yuan, W. Merk, H. Stemmler, and J. Allmeling, "Stationary-frame generalized integrators for current control of active power filters with zero steady-state error for current harmonics of concern under unbalanced and distorted operating conditions," *IEEE Transactions on Industry Applications*, vol. 38, no. 2, pp. 523–532, March/April 2002.

[72] D. N. Zmood and D. G. Holmes, "Stationary frame current regulation of pwm inverters with zero steady-state error," *IEEE Transactions on Power Electronics*, vol. 18, no. 3, pp. 814–822, May 2003.

[73] C. Bohn and D.P. Atherton, "An analysis package comparing pid anti-windup strategies," *IEEE Control Systems Magazine*, vol. 15, no. 2, pp. 34–40, April 1995.

[74] EN 50160:2007, "Voltage characteristics of electricity supplied by public distribution networks," 2007.

[75] Math H.J. Bollen, *Understanding power quality problems*, IEEE Press, 2000.

[76] N. Kroutikova, C.A. Hernandez-Aramburo, and T.C. Green, "State-space model of grid-connected inverters under current control mode," *IET Electric Power Applications*, vol. 1, no. 3, pp. 329–338, May 2007.

[77] M. J. Newman, D. N. Zmood, and D. G. Holmes, "Stationary frame harmonic reference generation for active filter systems," *IEEE Transactions on Industry Applications*, vol. 38, no. 6, pp. 1591–1599, November/December 2002.

[78] D. N. Zmood, D. G. Holmes, and G. H. Bode, "Frequency-domain analysis of three-phase linear current regulators," *IEEE Transactions on Industry Applications*, vol. 37, no. 2, pp. 601–610, March/April 2001.

[79] Y. Li, D. M. Vilathgamuwa, and P. C. Loh, "Design, analysis, and real-time testing of a controller for multibus microgrid system," *IEEE Transactions on Power Electronics*, vol. 19, no. 5, pp. 1195–1204, September 2004.

[80] R. Teodorescu, F. Blaabjerg, M. Liserre, and P.C. Loh, "Proportional+resonant controllers and filters for grid-connected voltage-source converters," *IEE Proceedings Electric Power Applications*, vol. 153, no. 5, pp. 750–762, September 2006.

[81] E. Twining and D. G. Holmes, "Grid current regulation of a three-phase voltage source inverter with an lcl input filter," *IEEE Transactions on Power Electronics*, vol. 18, no. 3, pp. 888–895, May 2003.

[82] A. V. Timus, R. Teodorescu, F. Blaabjerg, M. Liserre, and A. Dell' Aquila, "Independent synchronization and control of three phase grid converters," in *Proc. Proc. SPEEDAM 2006 International Symposium and Power Electronics, Electrical Drives, automation and Motion*, March 2006, pp. 1246 – 1251.

[83] J. M. Guerrero, L. Garcí de Vicuña, J. Matas, M. Castilla, and J. Miret, "A wireless controller to enhance dynamic performance of parallel inverters in distributed generation systems," *IEEE Transactions on Power Electronics*, vol. 19, no. 5, pp. 1205–1213, September 2004.

[84] M. Brucoli, T.C. Green, and J.D.F. McDonald, "Modelling and analysis of fault behaviour of inverter microgrids to aid future fault detection," in *Proc. IEEE International Conference on System of Systems Engineering (SoSE '07)*, April 2007, pp. 1–6.

[85] M. Brucoli, J.D.F. McDonald, and T.C. Green, "Analytical models for computation of fault behaviour of islanded inverter-only microgrids," *IET Generation, Transmission and Distribution*, (In Preparation).

[86] F. Calero, "Rebirth of negative-sequence quantities in protective relaying with microprocessor-based relays," in *Proc. of the 30th Annual Western Protective Relay Conference*, October 2003, pp. 1–30.

[87] A.F. Elneweihi, E.O. Schweitzer, and M.W. Feltis, "Negative-sequence overcurrent element application and coordination in distribution protection," *IEEE Transactions on Power Delivery*, vol. 8, no. 3, pp. 915–924, July 1993.

[88] R. Roeper, *Short-circuit currents in three-phase systems*, John Wiley, 1985.

[89] M. Brucoli and T. C. Green, "A fault detection technique suitable for power electronic network devices," in *Proc. University Power Engineering Conference 2005 (UPEC05)*, September 2005, vol. 2, pp. 1170–4.

[90] A. Sannino, "Static transfer switch: analysis of switching conditions and actual transfer time," in *Proc. IEEE Poweer Society Winter Meeting*, 28 2001, vol. 1, pp. 120–125.

[91] IEEE PES, "Benchmark systems for digital computer simulation of a staic transfer switch," *IEEE Transactions on Power Delivery*, vol. 16, no. 4, pp. 724–731, 2001.

[92] Po-Tai Cheng and Yu-Hsing Chen, "Design and implementation of solid-state transfer switches for power quality enhanchement," in *Proc. IEEE 35th Annual Power Electronics Specialists Conference PESC04*, 2004, vol. 2, pp. 1108–1114.

[93] H. Mokhtari and H. Yasaman, "Performance evaluation of hybrid transfer switches in grounded and ungrounded medium-voltage electrical systems," in *Proc. CIGRE/IEEE PES International Symposium on Quality and Security of Electric Power Delivery Systems*, 2003, pp. 91–96.

[94] M. Takeda, H. Yamamoto, Y. Hosokawa, and I. Kamiyama, "A low loss solid-state transfer switch using hybrid switch devices," in *Proc. of The Third Power Electronics and Motion Control Conference PIEMC 2000*, 2000, vol. 1, pp. 235–240.

Appendix A

Three-phase transformations

A.1 Symmetrical Components

According to the method of symmetrical components proposed by C.L. Fortescue in 1918, in a three-phase system, any asymmetrical set of vectors (for example a set of three-phase voltage vectors $\bar{V}_a$, $\bar{V}_b$ and $\bar{V}_c$) can be expressed as the sum of three symmetrical sets of vectors defined as follows:

- a three-phase vector set, $\bar{V}_{a_p}$, $\bar{V}_{b_p}$ and $\bar{V}_{c_p}$, with vectors of equal size and 120° clockwise displacement, called positive sequence components;
- a three-phase vector system, $\bar{V}_{a_n}$, $\bar{V}_{b_n}$ and $\bar{V}_{c_n}$, with vectors of equal size and 120° anticlockwise displacement, called negative sequence components;
- a three-phase vector system, $\bar{V}_{a_0}$, $\bar{V}_{b_0}$ and $\bar{V}_{c_0}$, with vectors of equal size and 0° displacement, called zero sequence components.

Figure A.1 shows the decomposition of asymmetrical voltage vectors as the sum of positive, negative and zero sequence components.

Now from Figure A.1 the following relations can be written:

$$\begin{aligned} \bar{V}_a &= \bar{V}_{a_p} + \bar{V}_{a_n} + \bar{V}_{a_0} = \bar{V}_p + \bar{V}_n + \bar{V}_0 \\ \bar{V}_b &= \bar{V}_{b_p} + \bar{V}_{b_n} + \bar{V}_{b_0} = \alpha^2\bar{V}_p + \alpha\bar{V}_n + \bar{V}_0 \\ \bar{V}_c &= \bar{V}_{c_p} + \bar{V}_{c_n} + \bar{V}_{c_0} = \alpha\bar{V}_p + \alpha^2\bar{V}_n + \bar{V}_0 \end{aligned} \tag{A.1}$$

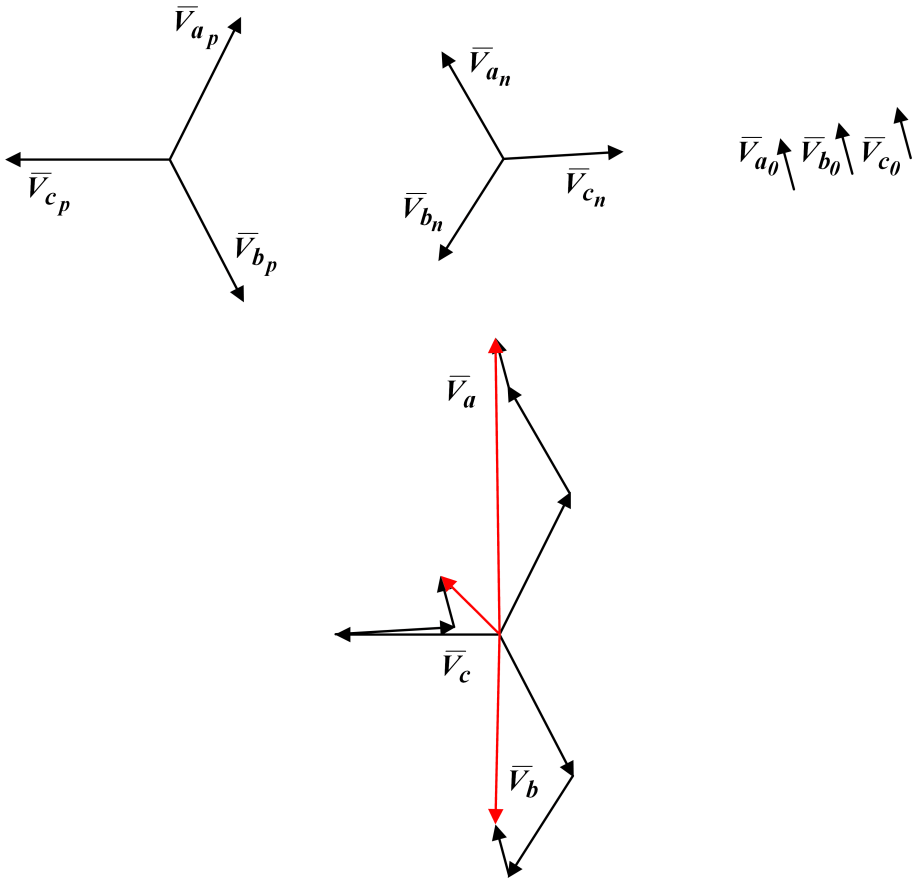


Figure A.1: Symmetrical components and decomposition of an unbalanced three-phase set of voltage vectors

where, $\alpha = -0.5 + j0.5\sqrt{3}$, $\alpha^2 = -0.5 - j0.5\sqrt{3}$, $\bar{V}_{a_p} = \bar{V}_p$, $\bar{V}_{a_n} = \bar{V}_n$ and $\bar{V}_{a_0} = \bar{V}_0$. The relation in (A.1) can be re-arranged in the matrix form as:

$$\begin{bmatrix} \bar{V}_a \\ \bar{V}_b \\ \bar{V}_c \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ \alpha^2 & \alpha & 1 \\ \alpha & \alpha^2 & 1 \end{bmatrix} \begin{bmatrix} \bar{V}_p \\ \bar{V}_n \\ \bar{V}_0 \end{bmatrix} = A \begin{bmatrix} \bar{V}_p \\ \bar{V}_n \\ \bar{V}_0 \end{bmatrix} \tag{A.2}$$

where A is the Fortescue's matrix. Conversely for a given asymmetrical three-phase system, it is possible to determine its symmetrical components as:

$$\begin{bmatrix} \bar{V}_p \\ \bar{V}_n \\ \bar{V}_0 \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} \bar{V}_a \\ \bar{V}_b \\ \bar{V}_c \end{bmatrix} \tag{A.3}$$

A.2 Clarke and Park transformations

Consider the instantaneous three phase utility voltages of an ideal (balanced and undistorted) supply:

$$\begin{aligned} v_a(t) &= V\cos(\omega t + \theta) \\ v_b(t) &= V\cos(\omega t + \theta - \frac{2}{3}\pi) \\ v_c(t) &= V\cos(\omega t + \theta + \frac{2}{3}\pi). \end{aligned} \tag{A.4}$$

This set of voltages is transformed into a two axes coordinate system with the Clarke transformation as follows:

$$\begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \\ v_\gamma(t) \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} \tag{A.5}$$

which gives

$$\begin{aligned} v_\alpha(t) &= \sqrt{\frac{3}{2}} V\cos(\omega t + \theta) \\ v_\beta(t) &= \sqrt{\frac{3}{2}} V\sin(\omega t + \theta) \\ v_\gamma(t) &= 0. \end{aligned} \tag{A.6}$$

Effectively the Clarke transformation converts a three-phase stationary coordinate system (the NatRF) into a two-phase stationary system (the StatRF) as shown in Figure A.2.

The StatRF defined by the Clarke transformation can be further transformed into a rotating $dq\gamma$ coordinate system with the Park transformation as follows:

$$\begin{bmatrix} v_d \\ v_q \\ v_\gamma \end{bmatrix} = \begin{bmatrix} cos(\omega t) & sin(\omega t) & 0 \\ -sin(\omega t) & cos(\omega t) & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \\ v_\gamma(t) \end{bmatrix} \tag{A.7}$$

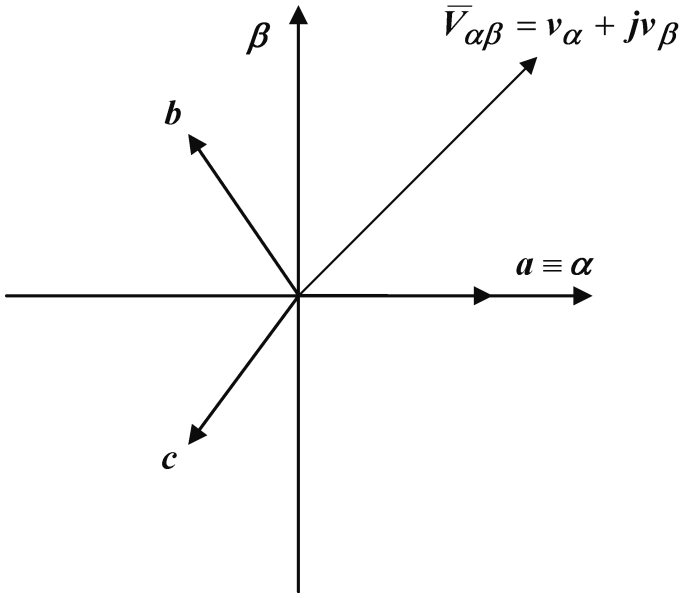


Figure A.2: Clarke transformation from three-phase abc to two phase $\alpha\beta$ stationary system

which results in

$$\begin{aligned} v_d &= \sqrt{\frac{3}{2}} V \cos(\theta) \\ v_q &= \sqrt{\frac{3}{2}} V \sin(\theta) \\ v_\gamma &= 0. \end{aligned} \tag{A.8}$$

By applying the Clarke and Park transformations, the original set of three phase utility voltages which varies in time is now represented by another set of components which are constant in a rotating reference frame as shown in Figure A.3.

A.3 System unbalance in the StatRF and in the SynRF

In the NatRF an asymmetrical set of three-phase voltages can be expressed in terms of symmetrical components as follows:

$$\begin{aligned} v_a(t) &= V_p \cos(\omega t + \theta_p) + V_n \cos(\omega t + \theta_n) + V_0 \cos(\omega t + \theta_0) \\ v_b(t) &= V_p \cos(\omega t + \theta_p - \frac{2}{3}\pi) + V_n \cos(\omega t + \theta_n + \frac{2}{3}\pi) + V_0 \cos(\omega t + \theta_0) \\ v_c(t) &= V_p \cos(\omega t + \theta_p + \frac{2}{3}\pi) + V_n \cos(\omega t + \theta_n - \frac{2}{3}\pi) + V_0 \cos(\omega t + \theta_0) \end{aligned} \tag{A.9}$$

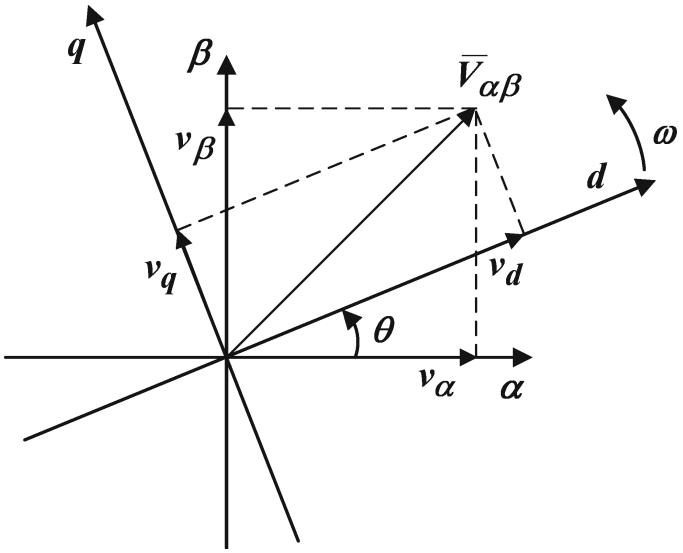


Figure A.3: Park transformation from the StatRF to the SynRF

By applying the Clarke transformation to (A.9), the following voltages are obtained:

$$\begin{aligned} v_\alpha(t) &= \sqrt{\frac{3}{2}}V_p cos(\omega t + \theta_p) + \sqrt{\frac{3}{2}}V_n cos(\omega t + \theta_n) \\ v_\beta(t) &= \sqrt{\frac{3}{2}}V_p sin(\omega t + \theta_p) - \sqrt{\frac{3}{2}}V_n sin(\omega t + \theta_n) \\ v_\gamma(t) &= \sqrt{3}V_0 cos(\omega t + \theta_0) \end{aligned} \tag{A.10}$$

The positive sequence component of the voltage becomes a vector $\bar{V}_{\alpha\beta_p}$ which rotates anti-clockwise with an angular speed ω describing a circle and the negative sequence component becomes a vector $\bar{V}_{\alpha\beta_n}$ which rotates clockwise in a circle with an angular speed of ω as shown in Figure A.4. The zero sequence component of the voltage becomes a vector moving back and forth along the γ axis. The resultant rotating vector $\bar{V}_{\alpha\beta}$ given by the sum of $\bar{V}_{\alpha\beta_p}$ and $\bar{V}_{\alpha\beta_n}$ describes in the $\alpha\beta$ plane an ellipse with a major radius equal to $|\bar{V}_{\alpha\beta_p}| + |\bar{V}_{\alpha\beta_n}|$ and a minor radius equal to $|\bar{V}_{\alpha\beta_p}| - |\bar{V}_{\alpha\beta_n}|$ where $|\bar{V}_{\alpha\beta_p}| = \sqrt{\frac{3}{2}}V_p$ and $|\bar{V}_{\alpha\beta_n}| = \sqrt{\frac{3}{2}}V_n$. Figure A.5 shows the trajectory of $\bar{V}_{\alpha\beta}$ for a balanced three-phase set of voltages (circle) and for an unbalanced one (ellipse).

If then the Park transformation is applied to (A.10), the equivalent components in

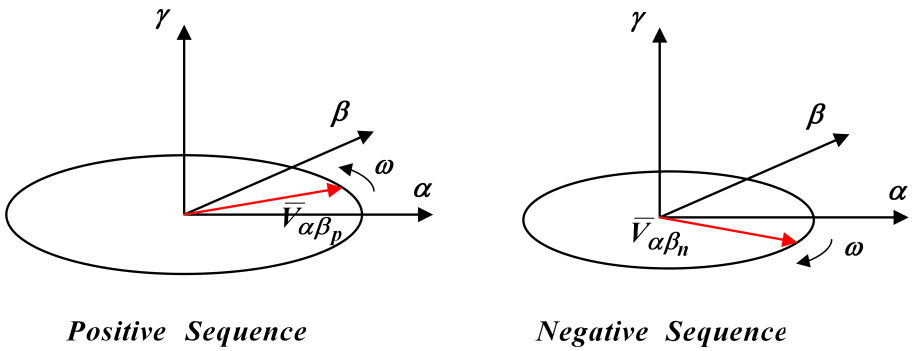


Figure A.4: Positive and negative sequence components in the StatRF

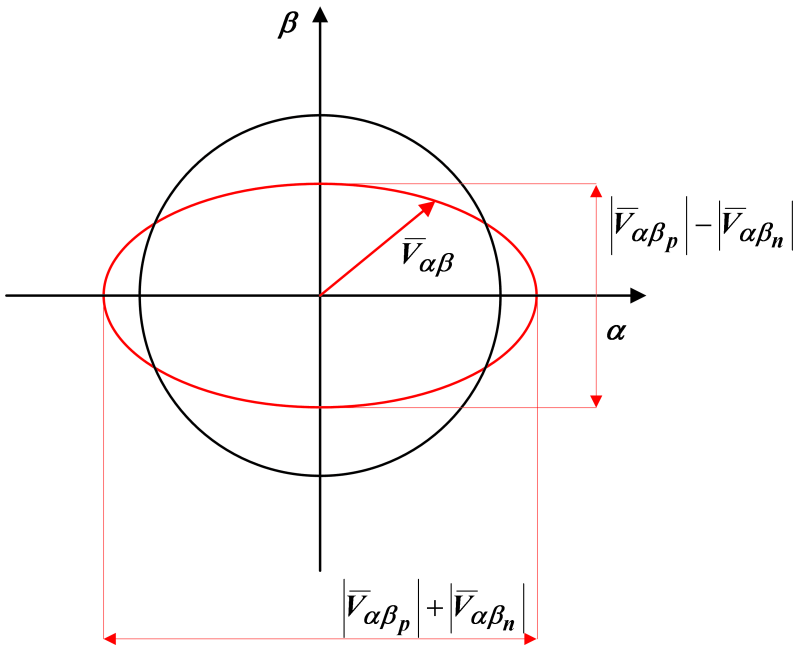


Figure A.5: Voltage vector trajectory for balanced and unbalanced operation in the $\alpha\beta$ plane

the SynRF are:

$$\begin{aligned} v_d &= \sqrt{\frac{3}{2}}V_p cos(\theta_p) + \sqrt{\frac{3}{2}}V_n cos(2\omega t + \theta_n) \\ v_q &= \sqrt{\frac{3}{2}}V_p sin(\theta_p) - \sqrt{\frac{3}{2}}V_n sin(2\omega t + \theta_n) \\ v_\gamma &= \sqrt{3}V_0 cos(\omega t + \theta_0) \end{aligned} \tag{A.11}$$

As a result of the unbalance, the dq components of the voltage have a DC component and a 2ω ripple.

A.4 Harmonic components in the SynRF

The utility voltage is often distorted by the presence of harmonics produced by the non-linearities of loads. So, the three phase utility voltages with harmonic components can be then written as:

$$\begin{aligned} v_a(t) &= V_1 \cos(\omega t + \theta_1) + V_5 \cos(5\omega t + \theta_5) + V_7 \cos(7\omega t + \theta_7) + ... \\ v_b(t) &= V_1 \cos(\omega t + \theta_1 - \frac{2}{3}\pi) + V_5 \cos(5\omega t + \theta_5 - 5\frac{2}{3}\pi) + V_7 \cos(7\omega t + \theta_7 - 7\frac{2}{3}\pi) + ... \\ v_c(t) &= V_1 \cos(\omega t + \theta_1 + \frac{2}{3}\pi) + V_5 \cos(5\omega t + \theta_5 + 5\frac{2}{3}\pi) + V_7 \cos(7\omega t + \theta_7 + 7\frac{2}{3}\pi) + ... \end{aligned} \tag{A.12}$$

By applying the Clarke and Park transformations to this set of voltages, the dq components are:

$$\begin{aligned} v_d &= \sqrt{\frac{3}{2}}V_1 \cos(\theta_1) + \sqrt{\frac{3}{2}}V_5 \cos(6\omega t + \theta_5) + \sqrt{\frac{3}{2}}V_7 \cos(6\omega t + \theta_7) + ... \\ v_q &= \sqrt{\frac{3}{2}}V_1 \sin(\theta_1) - \sqrt{\frac{3}{2}}V_5 \sin(6\omega t + \theta_5) + \sqrt{\frac{3}{2}}V_7 \sin(6\omega t + \theta_7) + ... \end{aligned} \tag{A.13}$$

As a result of the harmonics, v_d and v_q have a DC component and then a 6ω ripple if 5^{th} or 7^{th} harmonics are present in the signal. It can be shown that 11^{th} and 13^{th} harmonics determine a 12ω in the dq components.

Appendix B

Frequency-domain transformations

The frequency-domain transformations developed and applied in [72,77,78] make possible to shift controllers form one reference frame to the other thus allowing comparison and performance evaluations. The first step is to consider a SynRF control system where the input variables x_{ab} in the NatRF are transformed with the Clarke and Park transformations into a SynRF and then passed through a regulator $h_{dq}(t)$. The output from the regulator is then transformed by applying the inverse of the Park and Clarke transformations, thus giving the output controlled variables y_{ab}. This process is expressed by the following equation [77]:

$$\begin{aligned}\begin{bmatrix} y_a(t) \\ y_b(t) \end{bmatrix} = \sqrt{\frac{3}{2}} \begin{bmatrix} 1 & \frac{1}{\sqrt{3}} \\ 0 & \frac{2}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} cos(\omega_o t) & -sin(\omega_o t) \\ sin(\omega_o t) & cos(\omega_o t) \end{bmatrix} \\ \left\{ [h_{dq}(t)] * \left\{ \begin{bmatrix} cos(\omega_o t) & sin(\omega_o t) \\ -sin(\omega_o t) & cos(\omega_o t) \end{bmatrix} \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} x_a(t) \\ x_b(t) \end{bmatrix} \right\} \right\}\end{aligned} \tag{B.1}$$

where ω_o is the fundamental angular frequency. From (B.1), the equivalent representation of the system in the StatRF in the frequency-domain is given by:

$$\begin{bmatrix} Y_\alpha(s) \\ Y_\beta(s) \end{bmatrix} = H_{\alpha\beta 0}(s) \begin{bmatrix} X_\alpha(s) \\ X_\beta(s) \end{bmatrix} \tag{B.2}$$

where

$$H_{\alpha\beta}(s) = \frac{1}{2} \begin{bmatrix} H_{dq}(s+j\omega_o) & -jH_{dq}(s+j\omega_o) \\ +H_{dq}(s-j\omega_o) & jH_{dq}(s-j\omega_o) \\ jH_{dq}(s+j\omega_o) & (H_{dq}(s+j\omega_o) \\ -jH_{dq}(s-j\omega_o) & +H_{dq}(s-j\omega_o) \end{bmatrix} \tag{B.3}$$

Using the above transformation, the frequency-domain transfer fuction of synchronous frame PI regulators can be expressed in the StatRF as:

$$H_{\alpha\beta}(s) = \begin{bmatrix} K_p + \frac{K_i s}{s^2+\omega_o^2} & -\frac{K_i \omega_o}{s^2+\omega_o^2} \\ \frac{K_i \omega_o}{s^2+\omega_o^2} & K_p + \frac{K_i s}{s^2+\omega_o^2} \end{bmatrix} \tag{B.4}$$

As a result of the frequency domain-transformation, it can be seen that the two PI regulators in the SynRF are equivalent to two P+Resonant controllers and some coupling terms. An alternative to the transformation in (B.3) is the "bandpass transformation", which is defined as follows:

$$H(s) = H_{dq}(\frac{s^2+\omega_o^2}{2s}) \tag{B.5}$$

By applying this transformation to $H_{dq} = K_p + \frac{K_i}{s}$, the StatRF regulator becomes:

$$H(s) = K_p + \frac{2K_i s}{s^2+\omega_o^2}. \tag{B.6}$$

By applying the bandpass transformation, the cross-coupling terms in (B.4) disappear and the StatRF controllers are symmetrical around 0 Hz. As a result they are able to remove negative sequence components from the input signals. On the other hand the system in (B.4) does not remove negative sequence components.

The work presented in [72,77,78] refers to three-phase three-wire systems therefore the γ sequence component is not considered. However the procedure can be easily extended to a three-phase four-wire system. So if a third regulator $h_0(t)$ is included, the following equation can be written:

$$\begin{bmatrix} y_a(t) \\ y_b(t) \\ y_c(t) \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} cos(\omega_o t) & -sin(\omega_o t) & 0 \\ sin(\omega_o t) & cos(\omega_o t) & 0 \\ 0 & 0 & 1 \end{bmatrix}$$
$$\left\{ [h_{dq0}(t)] * \left\{ \begin{bmatrix} cos(\omega_o t) & sin(\omega_o t) & 0 \\ -sin(\omega_o t) & cos(\omega_o t) & 0 \\ 0 & 0 & 1 \end{bmatrix} \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} x_a(t) \\ x_b(t) \\ x_c(t) \end{bmatrix} \right\} \right\} \tag{B.7}$$

From (B.7), the equivalent representation of the system in the StatRF in the frequency domain is given by:

$$\begin{bmatrix} Y_\alpha(s) \\ Y_\beta(s) \\ Y_0(s) \end{bmatrix} = H_{\alpha\beta 0}(s) \begin{bmatrix} X_\alpha(s) \\ X_\beta(s) \\ X_0(s) \end{bmatrix} \tag{B.8}$$

where

$$H_{\alpha\beta 0}(s) = \frac{1}{2} \begin{bmatrix} H_{dq}(s+j\omega_o) & -jH_{dq}(s+j\omega_o) & 0 \\ +H_{dq}(s-j\omega_o) & jH_{dq}(s-j\omega_o) & \\ jH_{dq}(s+j\omega_o) & (H_{dq}(s+j\omega_o) & 0 \\ -jH_{dq}(s-j\omega_o) & +H_{dq}(s-j\omega_o) & \\ 0 & 0 & H_0(s) \end{bmatrix} \tag{B.9}$$

It is interesting to note that the presence of the third zero sequence component does not introduce any additional coupling with the other phases in the StatRF. Now if it is

assumed that in the *dq* loops a PI controller is used while a P+Resonant is used in the zero sequence loop, the equivalent matrix $H_{\alpha\beta 0}(s)$ in the StatRF is given by:

$$H_{\alpha\beta 0}(s) = \begin{bmatrix} K_p + \frac{K_i s}{s^2+\omega_o^2} & -\frac{K_i \omega_o}{s^2+\omega_o^2} & 0 \\ \frac{K_i \omega_o}{s^2+\omega_o^2} & K_p + \frac{K_i s}{s^2+\omega_o^2} & 0 \\ 0 & 0 & K_p + \frac{K_i s}{s^2+\omega_o^2} \end{bmatrix} \tag{B.10}$$

Now the equivalent matrix $H_{abc}(s)$ in the NatRF can be found as:

$$\begin{aligned} H_{abc}(s) &= \frac{2}{3} \begin{bmatrix} 1 & 0 & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \end{bmatrix} H_{\alpha\beta 0}(s) \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \\ &= \begin{bmatrix} K_p + \frac{K_i s}{s^2+\omega_o^2} & -\frac{1}{\sqrt{3}} \frac{K_i \omega_o}{s^2+\omega_o^2} & \frac{1}{\sqrt{3}} \frac{K_i \omega_o}{s^2+\omega_o^2} \\ \frac{1}{\sqrt{3}} \frac{K_i \omega_o}{s^2+\omega_o^2} & K_p + \frac{K_i s}{s^2+\omega_o^2} & -\frac{1}{\sqrt{3}} \frac{K_i \omega_o}{s^2+\omega_o^2} \\ -\frac{1}{\sqrt{3}} \frac{K_i \omega_o}{s^2+\omega_o^2} & \frac{1}{\sqrt{3}} \frac{K_i \omega_o}{s^2+\omega_o^2} & K_p + \frac{K_i s}{s^2+\omega_o^2} \end{bmatrix} \end{aligned} \tag{B.11}$$

If the control system is implemented in the StatRF with three P+Resonant regulators, the equivalent control system in the NatRF is obtained as follows:

$$\begin{aligned} H_{abc}(s) &= \frac{2}{3} \begin{bmatrix} 1 & 0 & -\frac{1}{\sqrt{2}} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & -\frac{1}{\sqrt{2}} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & -\frac{1}{\sqrt{2}} \end{bmatrix} H_{\alpha\beta 0}(s) \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \\ &= \begin{bmatrix} K_p + \frac{K_i s}{s^2+\omega_o^2} & 0 & 0 \\ 0 & K_p + \frac{K_i s}{s^2+\omega_o^2} & 0 \\ 0 & 0 & K_p + \frac{K_i s}{s^2+\omega_o^2} \end{bmatrix} \end{aligned} \tag{B.12}$$

Overall the frequency-domain transformations are a powerful tool in the design and comparison of control systems.

Appendix C

Derivation of the voltage dq components for unbalanced faults for comparison of different voltage detection methods

In the event of an unbalanced fault, the resulting voltage contains both positive, negative and zero sequence components. The following paragraphs show the derivation of the dq components of the voltage for different types of faults. Once v_d and v_q are obtained, the magnitude of the utility voltage can be calculated and be used to compare the detection times of different voltage detection techniques illustrated in Chapter 6.

C.1 Single phase-to-ground fault ($1\phi g$)

In the case of a $1\phi g$ fault involving phase a, the utility voltages are given by:

$$\begin{aligned} v_a(t) &= 0 \\ v_b(t) &= V\cos(\omega t + \theta - \frac{2}{3}\pi) \\ v_c(t) &= V\cos(\omega t + \theta + \frac{2}{3}\pi). \end{aligned} \tag{C.1}$$

The symmetrical components of the faulted utility voltages expressed as phasors are found as follows:

$$\begin{aligned} \bar{V}_p &= \frac{2}{3}Ve^{j(\omega t+\theta)} \\ \bar{V}_n &= -\frac{1}{3}Ve^{j(\omega t+\theta)} \\ \bar{V}_0 &= -\frac{1}{3}Ve^{j(\omega t+\theta)}. \end{aligned} \tag{C.2}$$

The sequence components of the voltage can be also expressed in time domain as:

$$\begin{aligned} v_p(t) &= \frac{2}{3}V\cos(\omega t+\theta) \\ v_n(t) &= -\frac{1}{3}V\cos(\omega t+\theta) \\ v_0(t) &= -\frac{1}{3}V\cos(\omega t+\theta) \end{aligned} \tag{C.3}$$

and the utility voltages can be then expressed as a sum of positive, negative and zero sequence components of the voltage:

$$\begin{aligned} v_a(t) &= \frac{2}{3}V\cos(\omega t+\theta) - \frac{1}{3}V\cos(\omega t+\theta) - \frac{1}{3}V\cos(\omega t+\theta) \\ v_b(t) &= \frac{2}{3}V\cos(\omega t+\theta-\frac{2}{3}\pi) - \frac{1}{3}V\cos(\omega t+\theta+\frac{2}{3}\pi) - \frac{1}{3}V\cos(\omega t+\theta) \\ v_c(t) &= \frac{2}{3}V\cos(\omega t+\theta+\frac{2}{3}\pi) - \frac{1}{3}V\cos(\omega t+\theta-\frac{2}{3}\pi) - \frac{1}{3}V\cos(\omega t+\theta). \end{aligned} \tag{C.4}$$

Now the dq components of the voltage are be found by applying the Clarke and Park transformations to (C.4) as follows:

$$\begin{aligned} v_d &= \frac{2}{3}V\cos(\theta) - \frac{1}{3}V\cos(2\omega t+\theta) \\ v_q &= \frac{2}{3}V\sin(\theta) + \frac{1}{3}V\sin(2\omega t+\theta). \end{aligned} \tag{C.5}$$

C.2 Phase-to-phase fault (2ϕ)

In the case of a 2ϕ fault involving phases b and c, the utility voltages are:

$$\begin{aligned} v_a(t) &= V\cos(\omega t+\theta) \\ v_b(t) &= v_c(t) = -\frac{V}{2}\cos(\omega t+\theta). \end{aligned} \tag{C.6}$$

The symmetrical components of the faulted utility voltages are:

$$\begin{aligned} \bar{V}_p &= \frac{1}{2}Ve^{j(\omega t+\theta)} \\ \bar{V}_n &= \frac{1}{2}Ve^{j(\omega t+\theta)} \\ \bar{V}_0 &= 0 \end{aligned} \tag{C.7}$$

which can be expressed in the time domain as:

$$\begin{aligned} v_p(t) &= \frac{1}{2}V\cos(\omega t+\theta) \\ v_n(t) &= \frac{1}{2}V\cos(\omega t+\theta) \\ v_0(t) &= 0. \end{aligned} \tag{C.8}$$

The utility voltages expressed as a sum of positive, negative and zero sequence components of the voltage are:

$$\begin{aligned} v_a(t) &= \frac{1}{2}V\cos(\omega t+\theta)+\frac{1}{2}V\cos(\omega t+\theta) \\ v_b(t) &= \frac{1}{2}V\cos(\omega t+\theta-\frac{2}{3}\pi)+\frac{1}{2}V\cos(\omega t+\theta) \\ v_c(t) &= \frac{1}{2}V\cos(\omega t+\theta+\frac{2}{3}\pi)+\frac{1}{2}V\cos(\omega t+\theta). \end{aligned} \tag{C.9}$$

By applying the Clarke and Park transformations to (C.9), the dq components are:

$$\begin{aligned} v_d &= \frac{1}{2}V\cos(\theta)+\frac{1}{2}V\cos(2\omega t+\theta) \\ v_q &= \frac{1}{2}V\sin(\theta)-\frac{1}{2}V\sin(2\omega t+\theta). \end{aligned} \tag{C.10}$$

C.3 Double phase-to-ground fault ($2\phi g$)

For a $2\phi g$ fault involving phases b and c, the utility voltage at the fault point become:

$$\begin{aligned} v_a(t) &= V\cos(\omega t+\theta) \\ v_b(t) &= v_c(t)=0. \end{aligned} \tag{C.11}$$

The symmetrical components of the faulted utility voltages are:

$$\begin{aligned} \bar{V}_p &= \frac{1}{3}Ve^{j(\omega t+\theta)} \\ \bar{V}_n &= \frac{1}{3}Ve^{j(\omega t+\theta)} \\ \bar{V}_0 &= \frac{1}{3}Ve^{j(\omega t+\theta)} \end{aligned} \tag{C.12}$$

and the utility voltages can be expressed as a sum of positive, negative and zero sequence components of the voltage as:

$$\begin{aligned} v_a(t) &= \frac{1}{3}V\cos(\omega t+\theta)+\frac{1}{3}V\cos(\omega t+\theta)+\frac{1}{3}V\cos(\omega t+\theta) \\ v_b(t) &= \frac{1}{3}V\cos(\omega t+\theta-\frac{2}{3}\pi)+\frac{1}{3}V\cos(\omega t+\theta+\frac{2}{3}\pi)+\frac{1}{3}V\cos(\omega t+\theta) \\ v_c(t) &= \frac{1}{3}V\cos(\omega t+\theta+\frac{2}{3}\pi)+\frac{1}{3}V\cos(\omega t+\theta-\frac{2}{3}\pi)+\frac{1}{3}V\cos(\omega t+\theta). \end{aligned} \quad \text{(C.13)}$$

By applying the Clarke and Park transformations, the dq components of the voltage are:

$$\begin{aligned} v_d &= \frac{1}{3}V\cos(\theta)+\frac{1}{3}V\cos(2\omega t+\theta) \\ v_q &= \frac{1}{3}V\sin(\theta)-\frac{1}{3}V\sin(2\omega t+\theta). \end{aligned} \quad \text{(C.14)}$$