Comprehensive Study of Large-Area CVD Graphene Field Effect Structures at DC and Microwave Frequencies

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MEng ARSM

A DISSERTATION FOR THE DEGREE OF

DOCTORATE OF PHILOSOPHY



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Declaration of Originality

I hereby declare that the content of this thesis is entirely is result of my independent research except where otherwise cited and acknowledged. Any contribution from third-party research including other collaborations has been given full acknowledgment.

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September 2016

Acknowledgements

At the very outset, I would like to thank my supervisors Prof Norbert Klein and Dr Sandrine Heutz whom constant support and encouragement made my research experience very joyful. My sincere gratitude goes to Norbert who provided me with the opportunity to join his research group after completion of my Master's degree and gave me the freedom to explore my curiosities and new ideas in the field and never tired of having long discussions and sharing his incredible scientific knowledge with me. I have also learnt a tremendous amount from Norbert and his exemplary attitude that has helped me on taking a much better and broader approach to my life, for which I am very thankful.

I would like to acknowledge the support that I received from Dr Peter Petrov who not only granted me with access to the facilities at Imperial College Thin Film Technology laboratory, but also, he was always happy to provide me with his expert opinions on various subjects such as safety matters, vacuum technology as well as fabrication of various advanced thin film materials.

I would also like to express my gratitude to my good friend and colleague Dr Stefan Goniszewski with whom I have had endless dialogues and debates from fundamentals of electrodynamics and band structure of graphene to origin of matter and quantum physics, which were often followed by an intense *frisbee* competition. My collaboration with Stefan also turned fruitful by publishing our joint work in Nature Scientific Reports journal.

A special thanks to Dr Stephen Hanham for his thoughtful advice over the years as well as his assistance and support by sharing his expertise in the Microwave-

Terahertz field and also in the theoretical simulations and script developments that would have not been possible without him.

I extend my appreciation to Dr Johannes Lischner whose in-depth knowledge and expertise in the theory and simulation of materials greatly facilitated the understanding of the experimental results presented in Chapter 5.

I gratefully acknowledge and appreciate the contribution of Dr Olena Shaforost, Mr Wei Liu, Dr Andrei P. Mihai, Mr Ling Cheng-Sheng, Mrs Rui Wang, Mrs Becky Kilmurray, Mrs Viktoryia Shautsova, Dr Evgeniy Donchev, Dr Bin Zou, and Dr Toby Basey-Fisher from Imperial College and Dr Ling Hao from the National Physics Laboratory where some of the AFM measurements in this thesis were conducted.

Last but certainly not least, I would like to thank my parents who paved the path for me to study, learn, and grow at a very high standard both personally and professionally. They gave me encouragement and support every step of the way, for which I shall forever be grateful.

Abstract

Following the successful isolation of graphene in 2004 by Novoselov and Geim, a significant amount of time and energy have been invested in studying the properties of this 2D material. Many researchers and companies from all around the world have established the vision of incorporating graphene into industrial scale applications where full utilisation of this material can be achieved outside the laboratories. One of the major technical challenges facing electrical characterisation of graphene is the different processes such as lithography and plasma etching that this material has to be exposed to before an electrical measurement can be conducted on it. These processes are known to partially deteriorate the inherent properties of graphene. A potential solution is to employ a contact-free electrical measurement technique where transport properties of large-area graphene films can be extracted without the need for realization of contacts to the surface of graphene.

This thesis explores a microwave resonance technique to study the field effect properties of graphene based field effect structures. Field effect devices with a variety of dielectric films are fabricated and performance of each of them is analysed separately. This microwave method will prove to be consistent with the DC measurements and also in perfect agreement with the theoretical results from the Boltzmann equation.

Further to successful demonstration of the microwave cavity technique, a novel stacked heterostructure of graphene-aluminum nitride-graphene is designed and developed. It will be shown that the sheet resistance of one graphene layer in such structure can be modulated by the application of a gate voltage to another graphene layer. This system resembles a parallel circuit of the two graphene films where each layer has a distinct doping level. The Boltzmann's framework is used and the

obtained microwave field effect conductivity result are accompanied by a fitting model. Switching ratio of as high as 4.5 is achieved at room temperature by controlling the doping level in each graphene sheet. This heterostructure system presents a promising new device structure that can potentially be used as a dual-biosensing device for biomedical applications. Such device could utilise the piezoelectric properties of aluminium nitride in combination with the strength, conductivity, transparency, and bio-compatibility of graphene to detect and measure the mass as well as the charge of various cells including the cancer cells. The dual-sensing mode is expected to significantly improve the false negatives that are currently obtained via other cell capturing methods.

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1. M. Adabi, J. Lischner, S. Hanham, A. P. Mihai, O. Shaforost, R. Wang, L. Hao, P. Petrov, N. Klein, Microwave Study of Field-Effect Devices Based on Graphene/Aluminum Nitride/Graphene Structures. Accepted for Publication in Nature Scientific Reports.

2. M. Adabi, W. Liu, O. Shaforost, S. Goniszewski, S. Hanham, L. Hao, J. Gallop, P. Petrov, N. Klein, Simultaneous DC and microwave measurements of large-area graphene FET structures, 2nd International Scientific Symposium, St Petersburg, Russia, 2015

3. S. Goniszewski, M. Adabi, O. Shaforost, SM. Hanham, L. Hao, and N. Klein. "Correlation of P-Doping in CVD Graphene with Substrate Surface Charges." *Scientific Reports.* 6 (2016). Print.

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11. C. Watts, S. M. Hanham, M. M. Ahmad, M. Adabi and N. Klein, "Coupled dielectric-split ring microwave resonator for liquid measurements in microfluidic channels at nanoliter volumes", European Microwave Week 2016, EuMC14-01, EuMW 2016

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List of Constants and Variables

a_i	Lattice vector
b_i	Reciprocal lattice vector
δ	Skin depth
ϵ	Energy
ε	Permittivity
ε_0	Free-space permittivity
f_r	Resonant frequency
Γ	Scattering rate
h	Planck constant
$\hbar$	Reduced Planck constant
k_B	Boltzmann constant
k	Wave-vector
μ	Permeability, Mobility
μ_0	Free-space permeability
μ_C	Chemical potential
μ_H	Hall mobility
n	Charge carrier concentration
ω	Angular frequency
p	Momentum
q	Electric charge
ρ	Resistivity
σ	Conductivity
τ	Scattering time
v_F	Fermi velocity
t, x	Thickness
t_b	Tight-binding model constant
$tan\delta$	Loss-tangent
A	Area
C	Capacitance
D	Magnetic flux density
$D(\epsilon)$	Density of states
E	Energy, Electric field
G	Conductance

H	Magnetic field strength
I	Current
K	Brillouin-zone corners
L	Inductance
P	Pressure
Q	Charge per unit area
$Q(V)$	Voltage-dependant Q-factor
R	Resistance
R_S	Sheet resistance
S_{ij}	Scattering parameter
T	Temperature
W	Stored electrical energy
Z	Impedance
Z_C	Characteristic impedance

List of Abbreviations

ALD	Atomic Layer Deposition
APC	Automatic Pressure Control
AFM	Atomic Force Microscopy
BSE	Back-Scattered Electrons
CNP	Charge Neutrality Point
CMOS	Complementary Metal Oxide Semiconductor
CRT	Cathode Ray Tube
CVD	Chemical Vapor Deposition
DC	Direct Current
EBSD	Electron Back-Scatter Diffraction
EDX	Energy Dispersive X-ray Spectroscopy
G-FET	Graphene based Field Effect Transistor
HEM	Hybrid Electromagnetic
HOPG	Highly Ordered Pyrolytic Graphite
HRS	Highly Resistive Silicon
LEED	Low Energy Electron Diffraction
$nSiO_2$	Native Silicon Dioxide
PLD	Pulsed Laser Deposition
PVD	Physical Vapor Deposition
Q-factor	Quality Factor
RF	Radio Frequency
RIE	Reactive Ion Etching
RT	Room Temperature
SEM	Scanning Electron Microscopy
TE	Transverse-Electric
TEM	Transmission Electron Microscopy
TM	Transverse Magnetic
VNA	Vector Network Analyser
XRD	X-ray Diffraction Analysis

List of Instruments

Technique	**Instrument, Location**
Atomic Force Microscopy	BRUKER Icon, NPL
Chemical Vapour Deposition	VACGEN Vertical Cluster Deposition System, Imperial College
Electron Backscattered Diffraction	Zeiss Auriga Cross Beam, Imperial College
I-V characterisation	Dual Channel 2636B Keithley Sourcemeter, Imperial College
Magnetron Sputtering	Mantis QPrep Thin Film Deposition System, Imperial College
Microwave Measurements	Rohde & Schwarz Vector Network Analyser, Imperial College
Optical Microscopy	
Photolithography	KarlSuss MJB3, Imperial College
Pulsed Laser Deposition	LAMDA PHYSIK COMPeX, Imperial College
Reactive Ion Etching	SENTECH Etchlab 200, Imperial College
Scanning Electron Microscopy	LEO Gemini 1525 FEGSEM, Imperial College
Surface Profiling	BRUKER Dektak 150, Imperial College
Raman	WITec Alpha300 R, Imperial College
X-ray Diffraction	PANalytical's X-ray Diffractometer, Imperial College

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1. Motivation and Thesis Overview

Discovery of new materials, innovative techniques, and reducing dimensions of electrical devices have formed the core constituents of the technological advances in the 21st century. From electrical vehicles and carbon fibre jet engine fan blades to 3D printing instruments, small video cameras, and high frequency data communication links, they all share a common future goal; That is reducing the dimensions and mass of the individual components while maintaining/improving previous performance merits as well as added functionalities to the existing ones. Discovery of graphene has not only opened the door to the possibility of having electronic devices made entirely from 2D materials, but also it has expanded the horizons for flexible wearable electronics. Some of the potential products that incorporate graphene in different industrial sectors and are highlighted in the Graphene Roadmap predicted by Ferrari et al. [1] are displayed in Figure 1.1.

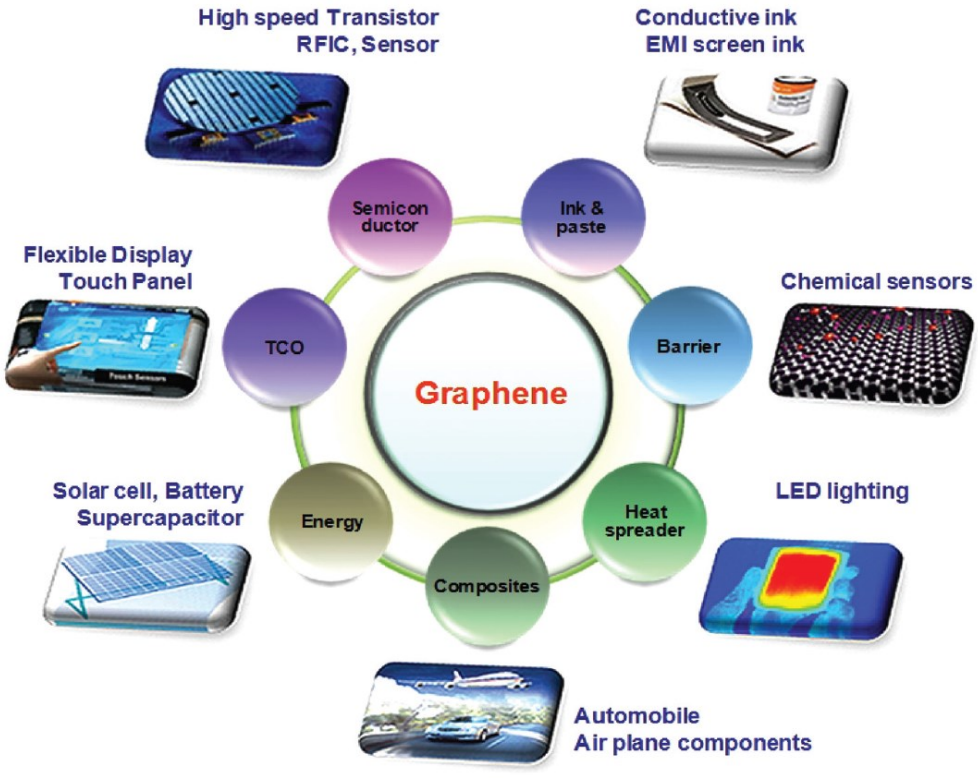


Figure 1.1. Potential industrial applications of graphene in various industries. [1]

It is therefore important to make all the necessary research and investigation into ensuring that the industrially compatible characterisation methods are established en route to mass production of the potential products where graphene would theoretically present a considerable advantage over the existing materials.

In chapters two and three of this thesis, I'll be introducing some of the basic and fundamental properties of graphene and will describe its behaviour and response at DC as well as at high frequencies. I'll then explore growth of graphene on copper substrates using two different chemical vapor deposition techniques in chapter four. Further in the same chapter, I'll present a step-by-step fabrication procedure optimisation of graphene based field effect structures. This will be followed by system development for field effect characterisation of the various field effect devices at DC (Direct Current) as well as at Microwave frequencies (High frequency Alternating Current) via an innovatively developed wafer-scale compatible microwave cavity technique. Chapter five will involve data extraction and performance analysis of the fabricated devices. Figures of merit are then drawn from the transport properties of each device and a comparative analysis will be made. The importance of graphene-dielectric interface will also be investigated and discussed in this chapter and the thesis will conclude by presenting the first results for a graphene-gated aluminium nitride based field effect device along with the accompanied theoretical fit model. The demonstration of the working principles of such a device is an important milestone as both the field-effect properties of graphene and piezoelectricity of AlN can be utilised in a single integrated device. As such, it is expected to enable fascinating opportunities in the field of biosensing, where both charge and mass of various cells including cancer cells can be identified.

2. Introduction to Graphene

Graphene had been studied theoretically since 1947 but was discovered experimentally after 57 years in 2004 by Andre Geim and Konstantin Novoselov.

Graphene is a two dimensional crystalline sheet of carbon atoms arranged hexagonally in a honeycomb like lattice structure. [2, 3, 4, 5] Since the 18th century, scientists demonstrated curiosity in studying the properties of graphene. In fact, Sir Benjamin Collins Brodie from the University of Oxford investigated the atomic weight of graphite in 1859. [6] Upon examining the oxidised state of graphite, he observed transparent and extremely thin crystals of reduced graphite oxide under the optical microscope. In 1947, Philip Russell explained some of the physical properties of graphite via addressing the structure as well as the conductivity of a single hexagonal layer of carbon atoms. [7] More than a century after Brodie's work, in 1962, Boehm et al. [8] successfully isolated extremely thin carbon foils by reducing graphite oxide in a solution. Despite their efforts, it was not enough to earn them the Noble Prize. It was not until 2004, when Andrei Geim and Konstantin Novoselov discovered this 2D material by accidentally exfoliating highly pyrolytic graphite with a scotch tape and isolating single/few layer graphene films during a fun Friday night experiment. [9] They were awarded with the Noble Prize in Physics in 2010 for their ground-breaking discovery.

Graphene (Figure 2.1d) is also known as mother of the carbon allotropes where it can be stacked to give rise to graphite (Figure 2.1a), or be wrapped to form fullerene (Figure 2.1c), as well as be rolled to produce carbon nanotube (Figure 2.1b). [10] In graphene, each carbon atom is separated by covalent bonds of length 0.142 nm [11]

from its three adjacent carbon atoms, leaving a single electron from each carbon available for formation of weak pi bonds which arises from the orbital sp^2 hybridization throughout the lattice. [5,12,13,14] Graphene has attracted enormous attention worldwide in many different research areas. The electronic band structure of graphene is out of the ordinary [15,16] which transforms it into a potential candidate in many applications such as in complementary metal oxide semiconductors (CMOS) [17], field effect transistors [17], gas sensors [18], ultracapacitors [19], transparent conductors [20], cancer cell detection [21], nanometre scale coplanar waveguides, and many other electronic applications where transparency, high mobility, and modulation of charge carriers density can play critical roles. [22] The remarkable properties of graphene include high elasticity [23], ballistic transport conduction [28,24], good chemical stability [25] and outstanding carrier mobility of about 200000 $\frac{cm^2}{V.s}$ [2,20,26-27] at room temperature due to the relatively low effective mass of the charge carriers. [28] Despite having incredible properties, scalable and high quality production of graphene film has remained yet a very challenging and ongoing task. [28,19]

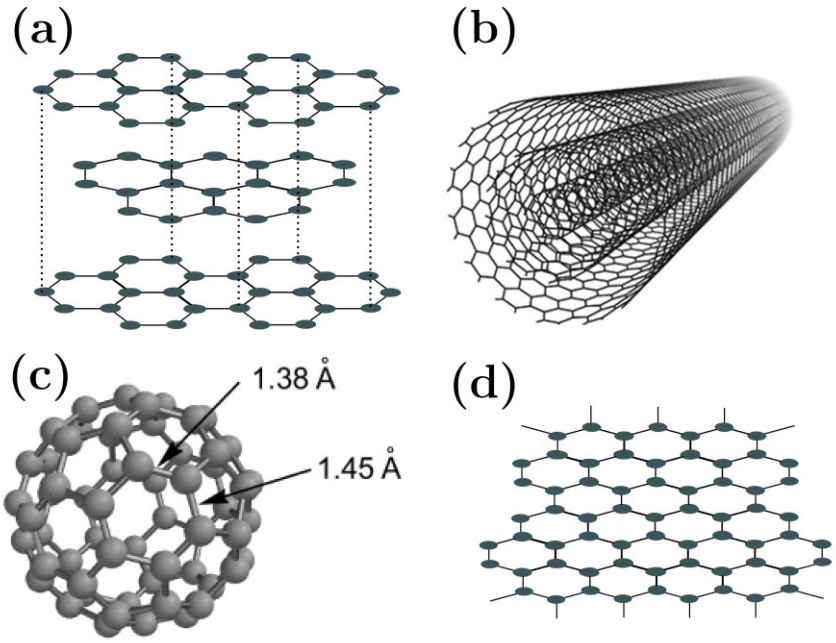


Figure 2.1. Schematics of the four main carbon allotropes; (a) Graphite, (b) Carbon nanotubes [29], (c) Fullerene [30], and (d) Graphene.

2.1 Band Structure of Graphene

The lattice structure of graphene is made up of a sheet of carbon atoms each sitting on the corners of inter-connected hexagons giving rise to a two dimensional honeycomb configuration with a lattice constant of 1.42 Å and thickness of 0.34 nm, which is equivalent to the extension of the pi-bonds. Hexagonal crystal structure of graphene is effectively a build-up of the translation of two carbon atoms. In real space these two carbon atoms result in two sublattices, A and B, as shown in Figure 2.2.

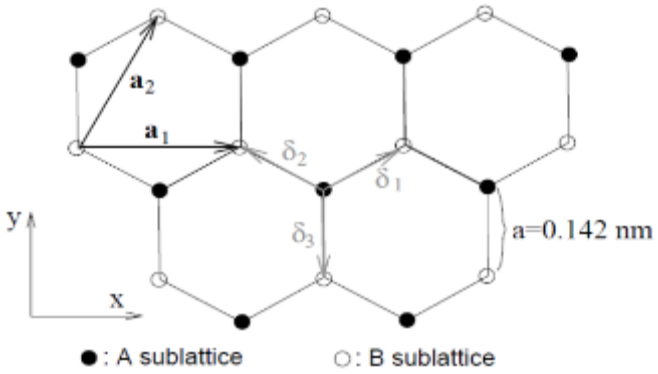


Figure 2.2. The triangular Bravais lattice of graphene with a two-carbon atom basis and bond length of 0.142 nm. [31]

The sigma bond between one carbon atom and its three in-plane neighbours results in a bond length of 0.142 nm. It is apparent that the formed hexagonal lattice structure is not a Bravais lattice (where all the points are equivalent). This can be seen by looking at neighbours of the individual sublattices A and B. Therefore, lattice structure of graphene is called a triangular Bravais that consists of a two-carbon atom basis and its translation via the lattice vectors a_1 and a_2. Sites A and B are related by the three vectors $\overrightarrow{\delta_1}$, $\overrightarrow{\delta_2}$, and $\overrightarrow{\delta_3}$;

$$\overrightarrow{\delta_1} = \frac{a}{2}(\sqrt{3}\ \vec{x} + \vec{y}),\ \overrightarrow{\delta_2} = \frac{a}{2}(-\sqrt{3}\ \vec{x} + \vec{y}),\ \overrightarrow{\delta_3} = -a\,\overrightarrow{y} \tag{2.1}$$

$$\overrightarrow{a_1} = \sqrt{3}\,a\,\vec{x}\ ,\ \overrightarrow{a_2} = \frac{\sqrt{3}}{2}a\,(\vec{x} + \sqrt{3}\,\vec{y}) \tag{2.2}$$

The electronic configuration of a carbon atom consists of 4 valence electrons that occupy the $2s$ and $2p$ orbitals. Although the electronic configuration suggests to have a filled $2s$ orbital with the remaining two electrons in the $2p$ orbitals, but in the stable state, formation of covalent bonds becomes favourable due to the presence of other carbon atoms. The result is a gain of energy of greater than 4 eV (4 eV is how much the $2s$ orbital is lower in energy than $2p$ orbital). Therefore, in the presence of other carbon atoms, one of the electrons in $2s$ orbital is excited to the $2p$ orbital as shown in Figure 2.3.

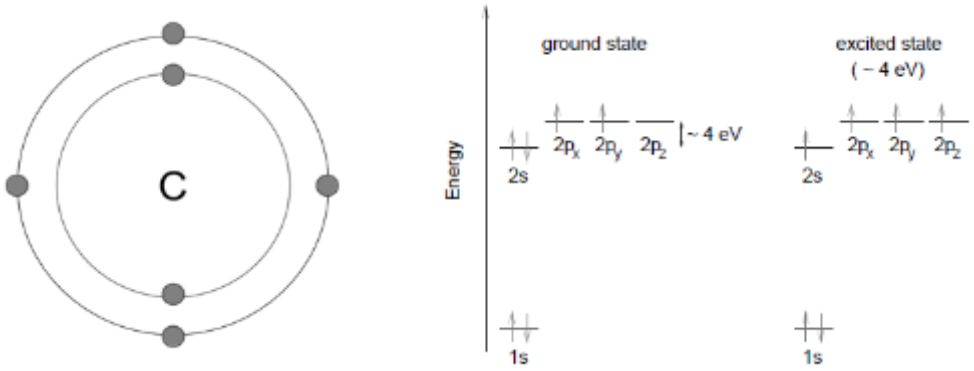


Figure 2.3. Carbon atom with four valence electrons (left), its ground state (middle), and its stable state next to other carbon atoms (right). [31]

As the carbon atoms merge on the x-y plane to form the honeycomb structure, electrons in the $2s$, $2p_x$, and $2p_y$ orbitals hybridise and give rise to three sp^2 hybridised orbitals in plane that results in strong in-plane sigma bonds. This results in a remaining electron in the p_z orbital (out of plane) for each carbon atom. The p_z orbitals of all carbon atoms then overlaps with one another to form weak π bonds across the graphene plane. [32] The extension of theses pi-bonds is responsible for the thickness of graphene (0.34 nm).

In order to investigate the interaction between the crystal structure of graphene and the electromagnetic waves, it is simpler to consider the reciprocal lattice structure of graphene. If a real space lattice vector $\vec{x}$ is considered in x-y-z space, then the reciprocal lattice vector of $\vec{x}$ is perpendicular to both $\vec{y}$ and $\vec{z}$. As defined

earlier, the real lattice basis vectors of graphene can be presented by $\overrightarrow{a_1}$ and $\overrightarrow{a_2}$. The reciprocal lattice vectors, $\overrightarrow{b_i}$, can then be related to the real ones by the Kronecker delta: [31]

$$\overrightarrow{b_i}.\overrightarrow{a_j} = 2\pi\delta_{ij} \tag{2.3}$$

The reciprocal lattice points are constructed by knowing the relationship between the reciprocal space and the real space lattice vectors. Using Eq. 2.3, the real space unit vectors $\overrightarrow{a_1}$ and $\overrightarrow{a_2}$ can be used to find reciprocal space unit vectors $\overrightarrow{b_1}$ and $\overrightarrow{b_2}$ in the plane of graphene:

$$\overrightarrow{b_1} = \frac{2\sqrt{3}\pi}{3a}\left(\vec{x} - \frac{\sqrt{3}}{3}\vec{y}\right) \tag{2.4}$$

$$\overrightarrow{b_2} = \frac{4\pi}{3a}\vec{y} \tag{2.5}$$

The first Brillouin zone is defined as the zone that is associated with k-values (crystal momentum/wavenumber) of the lowest energy band. [33] It is constructed by taking a reciprocal lattice point as the origin and connecting it to the closest equivalent neighbours. For graphene, this results in six vectors. The first Brillouin zone can then be constructed by finding the set of planes that are perpendicular bisectors to the so drawn vectors. The point K and K' are not equivalent since they cannot be connected via a reciprocal lattice vector. [33]

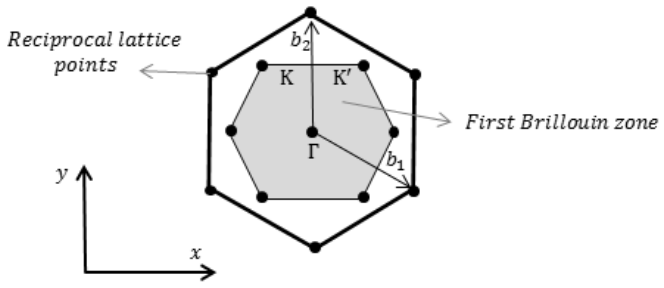


Figure 2.4. The first Brillouin zone of graphene with regards to the reciprocal lattice points.

As mentioned earlier, the *s*-orbital and two p-orbitals combine to form three hybridised orbitals known as sp^2 hybrid orbitals. The last p orbital (p_z) contains the

fourth electron and hence it is half filled. This orbital overlaps with those of the adjacent carbon atoms to form π bonds across the plane. [34] This essentially results in the extraordinary electrical properties of graphene. Using the linear combination of atomic orbitals model, [35] it can be shown that there exist no gaps between the valence and conduction band at each corner of the Brillouin zone where they merge (*K* and *K'* in Figure 2.5). These corners are better known as Dirac points merely because the behaviour of electrons at these states deviates from that in the conventional condensed matter system. Instead, the velocity of an electron in graphene takes a constant value of $V_F = 9.5 \times 10^5$ m.s^{-1} where V_F denotes the velocity at the Fermi level. [35]

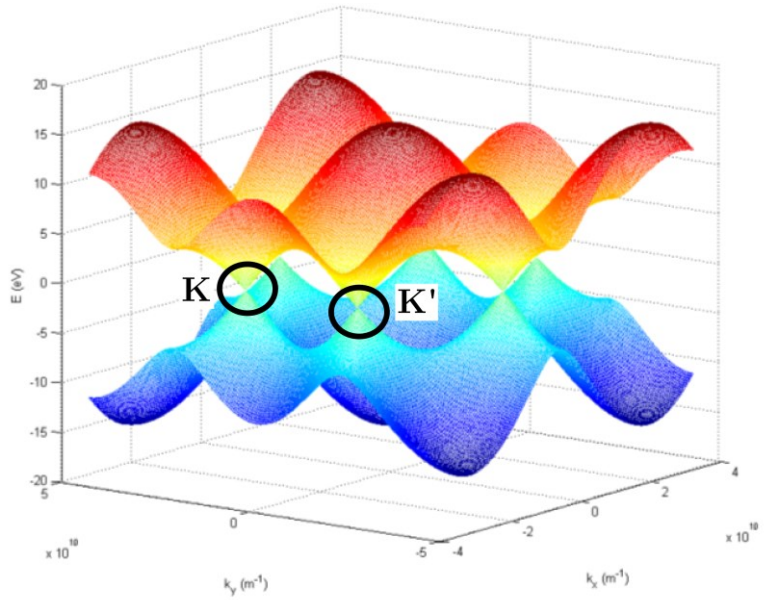


Figure 2.5. Energy dispersion of π-band in graphene, indicating the valence and the conduction bands where they only come into contact at the corners of the Brillouin zone. [10]

In graphene, the energy dispersion for the π-electrons can be derived from tight binding model and it can be shown to take the following form: [36]

$$E(k) = \pm t_b \sqrt{1 + 4cos\frac{\sqrt{3}k_x a}{2} cos\frac{k_y a}{2} + 4cos^2\frac{k_y a}{2}} \tag{2.6}$$

where, t_b denotes the tight binding model constant with a value of 3 eV. Negative and positive sign in the energy dispersion equation express the bonding and

antibonding, π and π* bands respectively. For a typical direct band gap semiconductor, the band dispersion shows quadratic type characteristics where the velocity of the electron changes upon any change in the binding energy. However, in the case of graphene, at low energies this behaviour has linear nature with electrons having a constant velocity. Eq. 2.6 can be approximated for sufficiently low energies, which would effectively correspond to the energy around the Dirac point:

$$E(k) \approx \pm \hbar k v_F \tag{2.7}$$

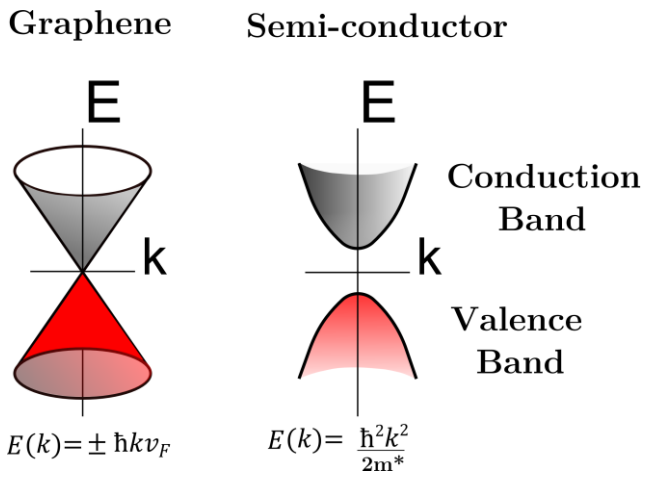


Figure 2.6. Band structure near the Dirac point for (a) graphene and (b) for a typical direct-bandgap semiconductor.

On the other hand, energy, momentum and mass of the electron are correlated by the dispersion relationship formulated from Einstein's relativity theory: [35]

$$E = \pm\sqrt{m^2c^4 + p^2c^2} \tag{2.8}$$

The momentum is related to the wavevector via $p = \hbar k$, therefore it is apparent that Eq. 2.7 is indeed analogous to Eq. 2.8. The difference comes from the fact that in Eq. 2.7, the low energy electrons are effectively behaving as if they are massless with a constant velocity value that is estimated to be 9.5×10^5 m.s^{-1}. [37]

2.2 Field Effect in Graphene and its Applications in Nano-Electronics

The first ever field effect transistor was fabricated by deposition of an aluminium film on top of a copper sulphide semiconductor (Cu_2S), where the semiconductor had metallic electrical contacts on both sides. Application of voltage to the aluminium, over the top of the semiconductor (with electric field normal to the surface of the semiconductor), resulted in change in conductance of the semiconductor. Devices built on this concept therefore have the name field effect associated them. [38]

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is often used as a switch or an amplifier for a given electronic signal. A typical MOSFET has a structure shown in Figure 2.7. In an off-state, no current can flow between source and drain terminals merely because one of the p-n junctions is reverse biased. Therefore, a third terminal called the gate is introduced to create a local channel within the semiconductor via the minority carriers' accumulation. At a certain value of gate voltage, the minority carriers locally overcome the population of majority carriers, resulting in a conducting channel between source and drain. This is better known as the population inversion. Here the minority carrier is pre-defined according to the dopant. This means that application of the external field can essentially act as a switch. By definition current flows into the drain and out of the source. [39]

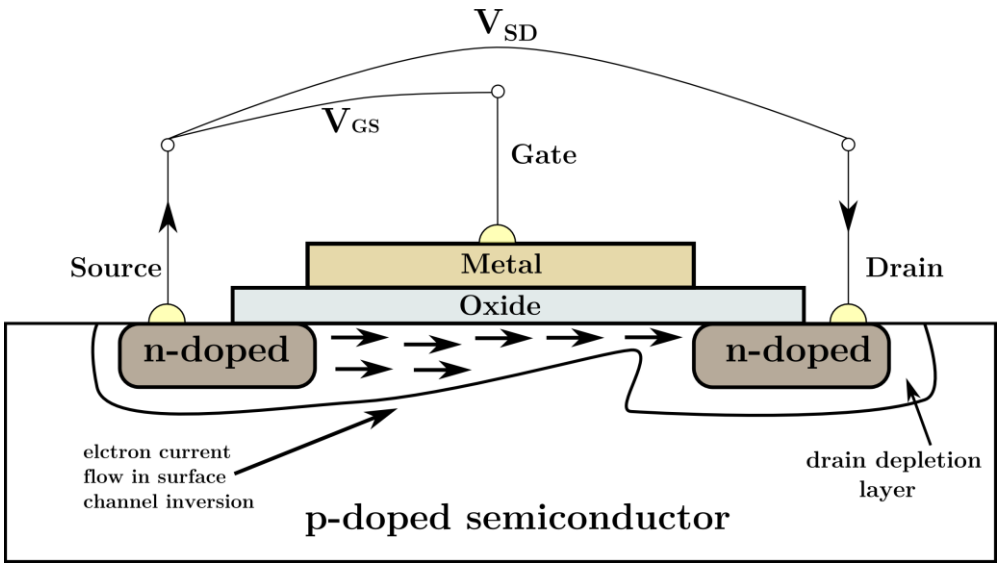


Figure 2.7. Structure of a typical MOSFET. (Motivated by [40])

Graphene based field effect structures (G-FET) follow a very similar concept. Illustrated in Figure 2.8a is structure of a typical back-gated G-FET, where an insulating layer is sandwiched between graphene and a conducting substrate. Two low contact resistance electrical contacts are made to the graphene layer in order to realize the source and drain terminals. The gate terminal is established on a conductive substrate (silicon in this case). Similar to a MOSFET, application of a voltage between the gate and source, V_{GS}, results in polarisation in the dielectric film and subsequent formation of electric field between the silicon and graphene layers. This effectively translates into accumulation of a certain concentration of surface charges at the Si/SiO_2 interface. Depending on the strength of the field, which is determined by the thickness of the dielectric material as well as the voltage value ($E_{GS} = V_{GS}/t$), the carrier concentration in the graphene film and hence the resistance of the graphene channel can be controlled. The external bias essentially gives rise to a shift in the Fermi level of graphene. For an undoped graphene and in case of a positive gate voltage, the surface charges will have a negative sign and the channel is consequently called n-doped, whereas for a negative gate voltage, a p-type channel is formed. This is extremely important, as it allows for the resistance of the channel to be controlled via the externally applied electric field.

Figure 2.8b illustrates how such a structure can be implemented in construction of a radio frequency receiver. The fabricated bottom gated G-FET by the IBM in this example employs a 10 nm atomic layer deposited (ALD) aluminium oxide (Al_2O_3) film that takes a T-shape structure. Recent achievements by IBM in fabrication of the graphene based devices have significantly contributed to the advances in graphene technology. Figure 2.9 demonstrates schematics and SEM micrographs of top-gated G-FET structure with a channel length of 550 nm, incorporated in a radio frequency mixer that can operate at frequencies up to 10 GHz. This was a part of the demonstration of the first fabricated wafer-scale graphene integrated circuit.

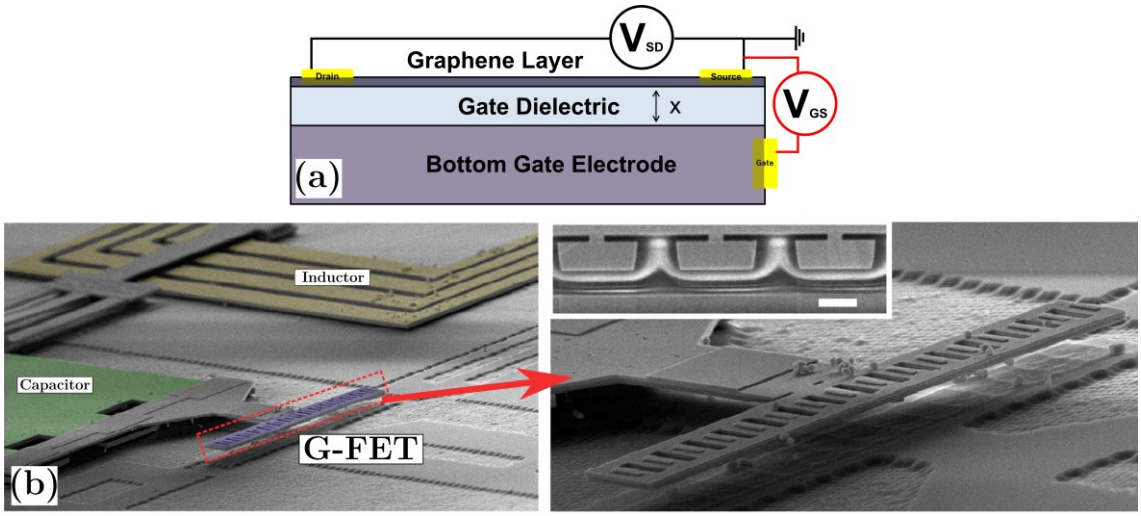


Figure 2.8. (a) Typical structure of a back-gated G-FET and (b) incorporation of such G-FET in an integrated circuit of a radio frequency receiver developed by IBM (scale bar on the cross-section view is 500 nm). [41]

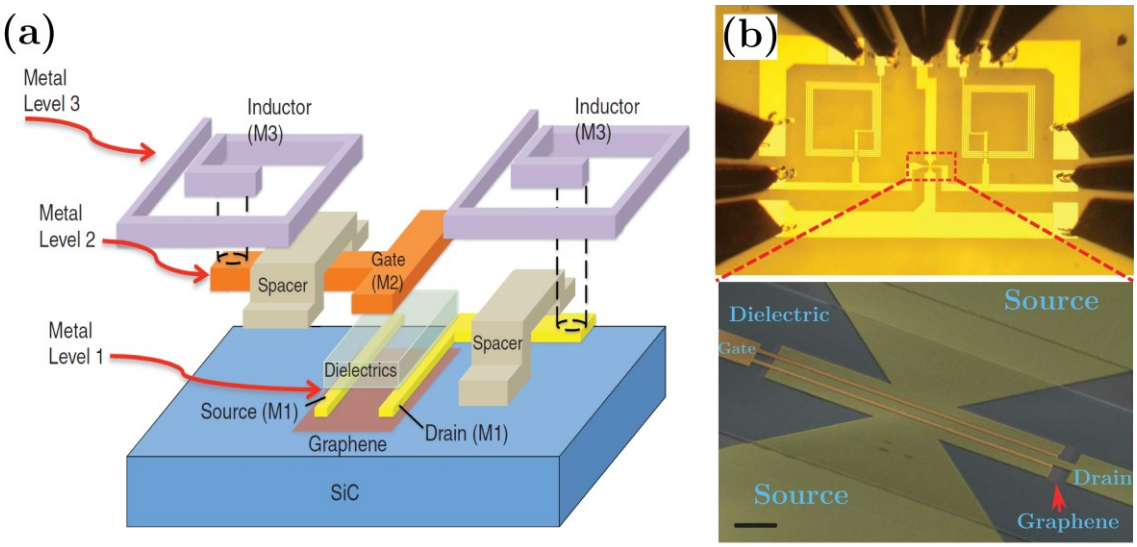


Figure 2.9. (a) Schematics of a radio frequency mixer incorporating top gated G-FET and (b) SEM micrograph of the fabricated G-FET (scale bar is 2 µm) by IBM. [42]

The consequence of the externally applied electric field can be observed experimentally upon varying the gate voltage and monitoring and the change in the current that occurs between the source and drain (I_{SD}), while a constant voltage is applied between the two terminals (V_{SD}). An ideal graphene is known to have its minimum conduction point (Dirac point, V_D) when no gate voltage is applied (V_{GS}=0 V). In such case, gate-dependant channel resistance takes a form which is represented by the plot in Figure 2.10. Although the curve shown below is highly symmetrical, experimental results have proved the possibility of an asymmetry that may exist due to the variation of scattering time between the charge carriers. [43] This will be visited and further discussed later in chapter 5.

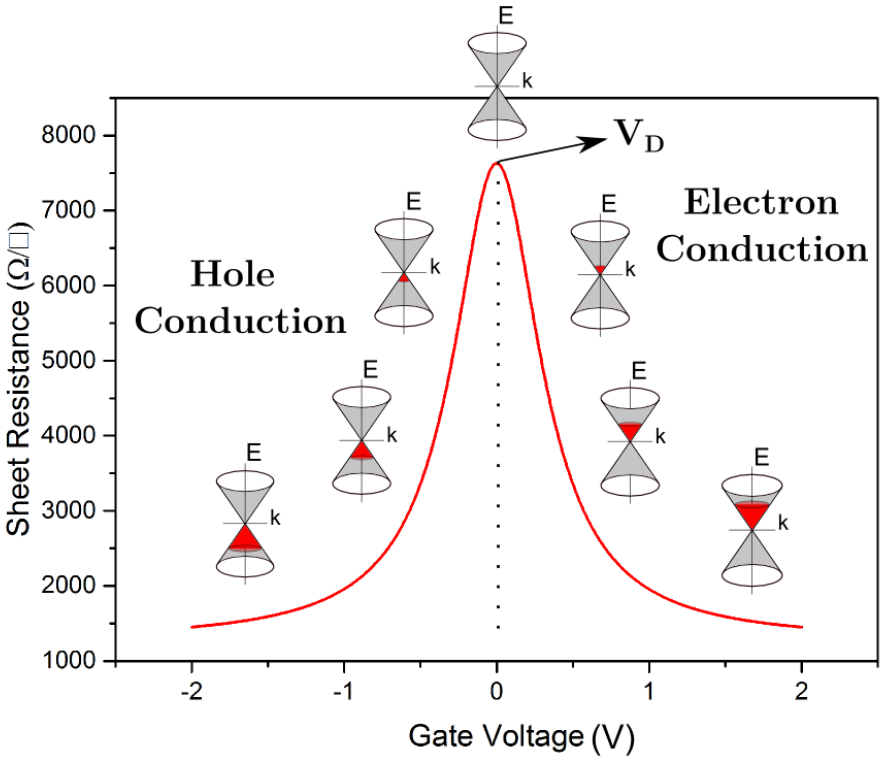


Figure 2.10. Transport curve of a back-gated G-FET for a pure un-doped graphene.

As mentioned previously, for an ideal un-doped graphene, V_D will be expected to occur at V_{GS}=0 V, however, due to unintentional doping that may arise from the atmospheric contaminations, treatment of the substrate and also during the graphene transfer process, G-FETs are often p-doped. The doping effect due to the substrate is often referred to as the electron-hole puddles that are distributed inhomogeneously across the sample. [44] This effectively translates into a relative shift of the Fermi level to the valence/conduction band for a p-doped/n-doped sample. This Fermi level shift to valence band will reflect itself in the FET measurements by observing a V_D>0 V. Similarly, if graphene is treated to be n-doped and have its Fermi level in the conduction band, it will be expected to have a V_D<0 V. Novoselov et al. believe that the p-doping (reflected in sheet resistivity peak taking place at a positive gate voltage) is merely due to the trapped water molecules induced during the transfer step. [9] In order to verify this theory, an annealing process was carried out, which resulted in shifting of the resistivity peak closer to the zero gate voltage. Higher mobility values were also observed. [45]

In order to perform a quantitative analysis on the G-FETs, the dielectric properties, the thickness of the gate insulator, dimensions of the channel as well as the applied bias values will need to be taken into account. These parameters will be used to calculate the DC conductivity of a given graphene sample in the fabricated G-FET structures.

Considering a back gated graphene field effect structure such as the one shown in Figure 2.8, it can be seen that effectively, the structure is comprised of a parallel plate capacitor that is created by having silicon dioxide of thickness, x, between two conductors; silicon and graphene. The capacitance of such structure can simply be presented by C:

$$C = \frac{q}{V_{GS}} \tag{2.9}$$

where q is the amount of charge on each plate as a result of the electric field at a given applied gate voltage. This is correlated with the carrier concentration n via:

$$q = ne \tag{2.10}$$

The capacitance can further be expanded as a function of dielectric's relative permittivity ε_r:

$$C = \frac{\varepsilon_0 \varepsilon_r A}{x} \tag{2.11}$$

where ε_0 is free space permittivity (8.854×10^{-12} F/m), A is the surface area and x is thickness of the insulator. Combining Eq. 2.9 and 2.11 results in total areal charge, Q, of:

$$Q = \frac{\varepsilon_0 \varepsilon_r}{x} V_{GS} \tag{2.12}$$

The areal density of the charge carriers (cm^{-2}) can therefore be related to the applied voltage via:

$$n = \frac{\varepsilon_0 \varepsilon_r}{xe} V_{GS} \tag{2.13}$$

Conductivity of the graphene sheet can be written in terms of its carrier concentration (n), carrier mobility (μ) and their charge (q):

$$\sigma = \sum nq\mu \tag{2.14}$$

It's apparent that conductivity of the sheet can be controlled by controlling the carrier concentration, which itself can be adjusted via an applied external voltage.

The areal density of the charge carriers is determined according to Eq. 2.13 and conductivity versus carrier concentration plot will be constructed (see Figure 2.12). Eq. 2.15 can be derived by combining Eq. 2.14 and 2.11, which can be used to determine the carrier mobility at a given gate voltage:

$$\mu = \frac{\sigma}{nq} = \frac{1}{\rho nq} = \frac{1}{R_S C V_{GS}} \tag{2.15}$$

In the next section, I will be looking at the Boltzmann's framework regarding the frequency dependence of conductivity of graphene and how interband and intraband transitions contribute to conductivity of graphene at different frequencies.

2.3 Complex Conductivity of Graphene

The unique band structure of graphene is known to result in a frequency dependant conductivity that is different to that of typical metals expressed by the Drude formula in Eq. 2.15. Conductivity of graphene has been subject to theoretical and experimental studies by a number of groups. [46, 47, 48, 49] It can be best described by the Kubo formula represented in Eq. 2.16. According to Kubo, conductivity of graphene takes a complex form and is directly correlated with the operation frequency (ω), the chemical potential (μ_C), the scattering rate of charge carriers ($\Gamma = 1/\tau$), and the temperature (T).

$$\sigma_{Metals}(\omega) = \frac{ne^2\Gamma}{m(1-i\omega\Gamma)} = \frac{\sigma_{DC}}{1-i\omega\Gamma} \tag{2.16}$$

$$\sigma_{Graphene}(\omega, \mu_C, \Gamma, T) =$$

$$\frac{ie^2(\omega-i2\Gamma)}{\pi\hbar^2}\left[\frac{1}{(\omega-i2\Gamma)^2}\int_0^\infty \epsilon\left(\frac{\partial f_d(\epsilon)}{\partial\epsilon} - \frac{\partial f_d(-\epsilon)}{\partial\epsilon}\right)\partial\epsilon - \int_0^\infty \frac{f_d(-\epsilon)-f_d(\epsilon)}{(\omega-i2\Gamma)^2-4(\epsilon/\hbar)^2}\partial\epsilon\right] \tag{2.17}$$

where ϵ denotes energy ($\epsilon = \hbar\omega$), $\hbar$ denotes the reduced Planck constant. f_d is represses the Fermi-Dirac distribution, defined by Eq. 2.18:

$$f_d(\epsilon) = [(exp\,(\epsilon - \mu_C)/k_BT) + 1)]^{-1} \tag{2.18}$$

where k_B denotes the Boltzmann's constant. Kubo is essentially comprised of two parts; contribution from (1) the intra-band (σ_{intra}) and (2) the inter-band (σ_{inter}) transitions to the total conductivity of graphene. As shown in Figure 2.11, the intra-band transitions are responsible for conductivity of graphene at lower frequencies, $\hbar\omega < \mu_C$, which is measured to be independent of the frequency up to about 100 GHz.[50] In such a transition, the carriers are excited to a higher energy level within the same band. As soon as $\hbar\omega > \mu_C$, inter-band transitions will begin to have a greater contribution to the total conductivity and they will be the dominating factor in the optical range. Interband transition are associate with excitation of carriers to a higher energy level in another band.

$$\sigma_{intra} = \frac{ie^2}{\pi\hbar^2(\omega-i2\Gamma)}\int_0^\infty \epsilon\left(\frac{\partial f_d(\epsilon)}{\partial\epsilon} - \frac{\partial f_d(-\epsilon)}{\partial\epsilon}\right)\partial\epsilon \tag{2.19}$$

$$\sigma_{inter} = \frac{ie^2(\omega-i2\Gamma)}{\pi\hbar^2}\int_0^\infty \epsilon\frac{f_d(-\epsilon)-f_d(\epsilon)}{(\omega-i2\Gamma)^2-4(\epsilon/\hbar)^2}\partial\epsilon \tag{2.20}$$

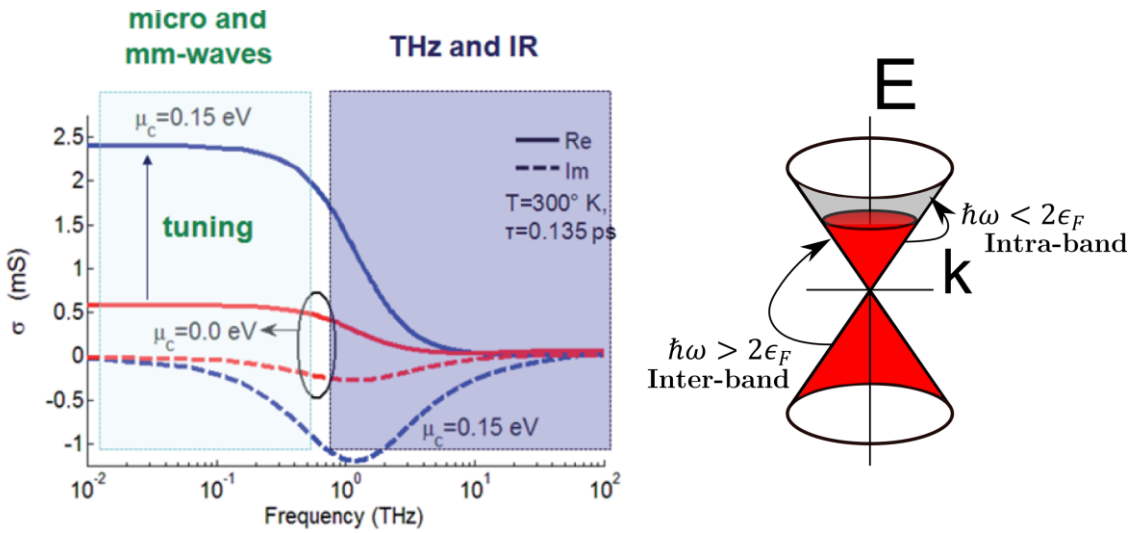


Figure 2.11. Complex conductivity of graphene at room across the electromagnetic spectrum at room temperature. [50]

It is apparent that at very high frequencies when $\hbar\omega > \mu_C$, conductivity of graphene becomes mostly real and independent of frequency. It therefore can be further simplified to Eq. 2.21, which is equivalent to about 2.3% optical absorption per graphene layer. [51]

$$\sigma(\omega) = \frac{\pi e^2}{2h} \tag{2.21}$$

The chemical potential of graphene can be determined from the density of carrier concentration n. In order to understand the relation between the effective carrier density and the chemical potential of graphene, one needs to define the carrier concentration density of both the electrons (n_ϵ) and holes (n_h) for a graphene sheet.

$$n_e = \int_0^\infty D_c(\epsilon) f(\epsilon, \mu_C) d\epsilon = \frac{1}{\pi\hbar^2 {v_F}^2} \int_0^\infty \frac{1}{1+\exp\left[\frac{\epsilon-\mu_C}{kT}\right]} \epsilon d\epsilon \tag{2.22}$$

$$n_h = \int_{-\infty}^0 D_v(\epsilon)(1 - f(\epsilon, \mu_C)) d\epsilon = \frac{-1}{\pi\hbar^2 {v_F}^2} \int_{-\infty}^0 \left[1 - \frac{1}{1+\exp\left[\frac{\epsilon-\mu_C}{kT}\right]}\right] \epsilon d\epsilon \tag{2.23}$$

where D_c and D_v denote the graphene density of states (DOS) for conduction and valence bands respectively.

$$D_c = \frac{\epsilon}{\pi\hbar^2 {v_F}^2} \tag{2.24}$$

$$D_v = -\frac{\epsilon}{\pi\hbar^2 {v_F}^2} \tag{2.25}$$

The chemical potential can then be related to the effective carrier concentration ($n_{eff} = n_e - n_h$) by Eq. 2.26 upon analytically solving the resulting integral.

$$n_{eff} = \frac{1}{\pi\hbar^2 {v_F}^2}\int_0^\infty \epsilon f(\epsilon - \mu_C)d\epsilon \tag{2.26}$$

In this work, the behaviour of various G-FETs is investigated in the DC and microwave regimes, where intra-band transition dominate the total conductivity of graphene. Assuming $\hbar\omega < \mu_C$ which is a valid assumption for both the DC and microwave frequencies, Eq. 2.19 can be approximated to:

$$\sigma_{intra} = \frac{\mu_C\, e^2}{2\pi\hbar^2\Gamma} + \frac{kTe^2}{\pi\hbar^2\Gamma} ln(e^{-\frac{\mu_C}{kT}} + 1) \tag{2.27}$$

At room temperature, $kT \ll \mu_C$, therefore Eq. 2.27 can be further simplified to:

$$\sigma_{intra} = \frac{\mu_C\, e^2}{2\pi\hbar^2\Gamma} \tag{2.28}$$

It is important to add that in the mentioned equations, all the energies are referenced to the Dirac point energy. It is also worth to note that from the G-FET device perspective, RC time constant plays an important part as it determines how quickly charge carriers will react to change in the applied electric field. Therefore, smaller channels combined with a graphene with a higher scattering time is preferred. Such device is expected to have a lower time constant and hence a faster switching capability associated with it.

As can be seen from Eq. 2.28, conductivity of graphene can be modulated by varying the chemical potential that is dependent on the density of carrier concentration. This is an extremely important feature of graphene as the density of carrier concentration itself can be controlled by both doping the graphene film as well as applying a gate voltage to it.

Often the mobility of graphene is extracted from gradient of the sheet conductivity (conductance), σ_s=$1/R_s$ versus carrier concentration plot. This approach takes the linear regime close to the Dirac point on both hole and electron conduction sides and assumes a constant mobility over the chosen range as shown in Figure 2.12. Areal density of charge carriers is deduced from the applied electric field. The charge neutrality point is then shifted to zero by deducting intrinsic charge density due to unintentional doping of graphene films (n_0).

$$n = n_0 + \frac{CV_{GS}}{e} \tag{2.29}$$

$$\mu = \frac{1}{e}\frac{\partial \sigma_s}{\partial n} \tag{2.30}$$

The intrinsic doping (n_0) can therefore be deduced by calculating the carrier concentration at the shifted Dirac voltage.

$$n_0 = \frac{\varepsilon_0 \varepsilon_r}{xe} V_{Dirac} \tag{2.31}$$

In the calculations, energy-independent scattering time is assumed whose value is different in each side of Dirac point, denoted τ_+ and τ_- for electrons and holes respectively. Also, the charge carrier density values were obtained using the applied gate voltage and capacitance via Eq. 2.13 which is then used to evaluate the chemical potential, μ_C.

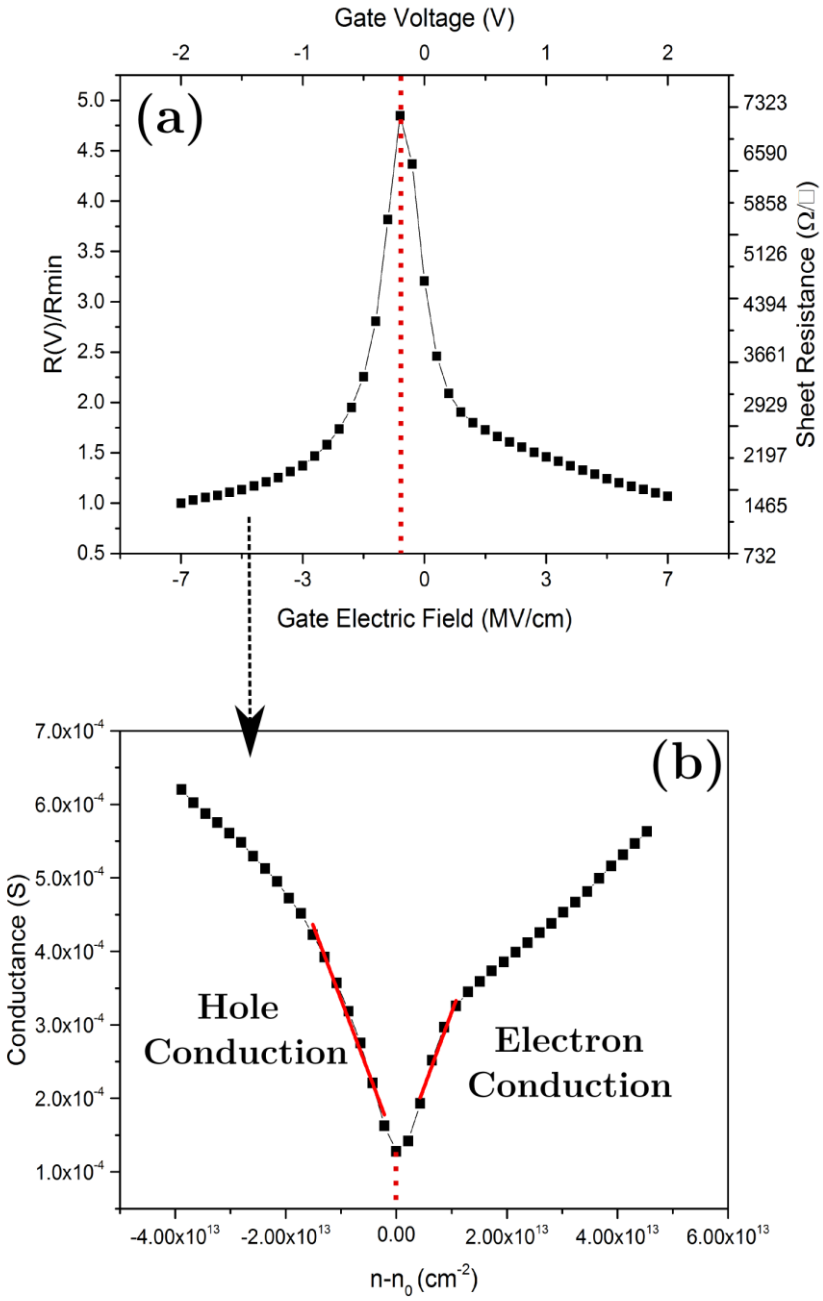


Figure 2.12. Extracting mobility of charge carriers by converting (a) resistance measurements to (b) areal density of carrier concentration versus conductance and considering the linear regime next to Dirac point for each of the Dirac sides.

One of the disadvantages of using this method of mobility extraction is that the chosen area can affect the calculated mobility and therefore a certain degree of error and uncertainty will be involved. Hall-effect measurements will be carried out to investigate the agreement between the estimated microwave mobility figures and the measured Hall mobility values. Despite the existing uncertainty, it is a robust

way of estimating the approximate value of charge carriers' mobility in the right order of magnitude.

The ability to modulate the carrier concentration by an external electric field, coupled with the thickness, flexibility, transparency, strength, and conductive nature of graphene transforms this 2D material to an ideal choice for a variety of applications. They include but not limited to Microwave-THz modulators, and detectors with fast response rates. [52] In fact, graphene based devices for flexible electronics, tunable antennae, optical modulators and waveguides, amplifiers and broadband terahertz modulators have already been experimentally demonstrated. [53, 54 , 55, 56, 57, 58, 59, 60]

2.4 Graphene Growth

There has been a numerous amount of research carried out on growing single and multilayer graphene films. Major methods of growing single-layer graphene include micromechanical cleavage of highly oriented pyrolytic graphite (HOPG)[13], chemical exfoliation of graphene oxide[4,5,28,61], thermal decomposition of Silicon Carbide (SiC)[62,63], and chemical vapour deposition (CVD) on various transition metal substrates [25,28,64,65] as well as on dielectric substrates such as Magnesium Oxide (MgO)[17]. Each of the mentioned methods will be discussed and the advantages and disadvantages associated with each will be outlined.

2.4.1 Chemical Vapor Deposition (CVD)

Chemical vapor deposition is a technique where a desired material can be deposited on a given substrate upon chemical reactions. For graphene, a hydrocarbon precursor such as methane is often used in combination with hydrogen (and argon) at an elevated temperature. The precursor is transported from one end of the reaction chamber to the other end and depending on the processing conditions,

methane molecules dissociate into carbon atoms and diffuse on the surface. The resulting carbon atoms would migrate on the surface and bond with the surface of the substrate where energetically favourable. As represented in Figure 2.13, a number of surface mechanisms can be observed. Precursor-substrate reaction strongly relies on the processing condition, surface treatments, and nature of the substrate over which graphene is intended to be grown. The Thermodynamics and Kinetics mechanisms essentially govern the deposition process. [66] This means that a large number of parameters, from temperature to roughness of the substrate will play vital roles and will therefore need consideration.

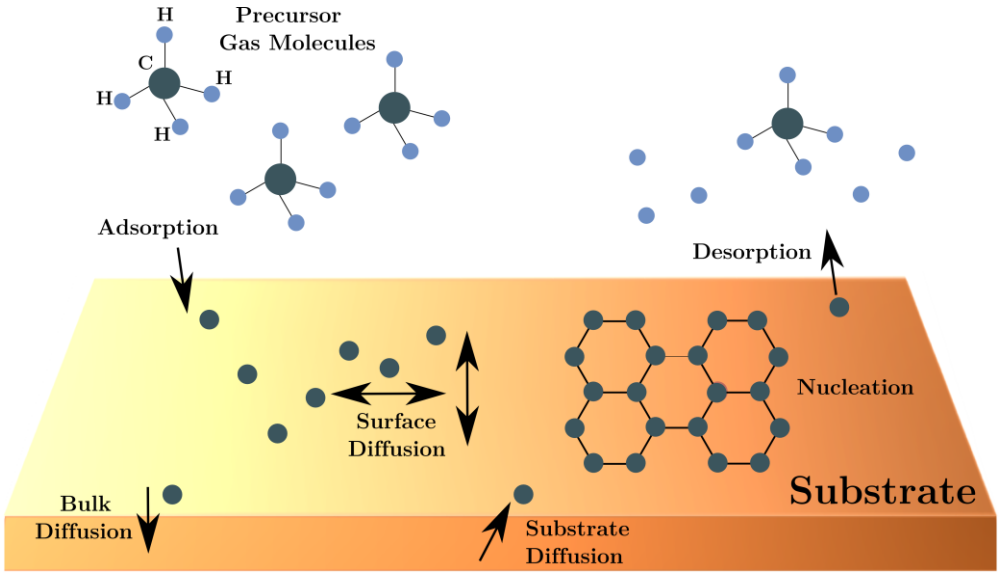


Figure 2.13. Potential mechanisms that can take place during nucleation of carbon atoms on the substrate.

Amongst the available graphene fabrication methods, CVD processes that utilise transition metals have received a significant amount of attention compared to the other techniques. This is due to the capability of CVD in producing large-scale graphene sheets coupled with the easier transfer process that is associated with it. [67] Current CVD graphene growth research is largely devoted to enhancement of the wafer scale compatibility while matching the electrical properties observed in exfoliated graphene films. Metal substrates such as Nickel (foil and thin film), Copper (foil and thin film), Cobalt, hexagonal boron nitride, magnesium oxide as

well as germanium have already been subjected to monolayer graphene growth. [10, 22, 25, 64, 65]

Formation of graphene and the mechanisms involved in its growth are strongly affected by the chosen substrate. [20] Carbon solubility of the substrate and formation of carbide phases at various temperatures, effectively determine the mechanism upon which the grain development of graphene will be dependent on. [20] Carbon atoms will tend to migrate inside the heated metal and precipitate out on cooling when a substrate with a relatively high carbon solubility such as Ni, Co or Ru is used. A typical growth sequence for such a substrate is shown in Figure 2.14.

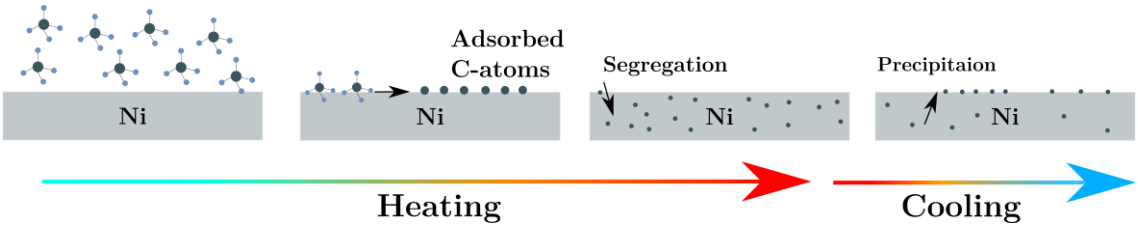


Figure 2.14. Graphene formation sequence over nickel substrate.

It is suggested [3,25-27] that when nickel is used, formation of the metastable nickel carbide phase encourages and smoothens the path for carbon precipitation out of the carbide on cooling. This is in stark contrast to the mechanism of graphene growth on a copper foil. For metal substrates with low carbon solubility such as copper (with 0.03% carbon solubility at 1000°C), [68] graphene formation is tailored mainly by surface mechanisms. As shown in Figure 2.15, the growth step is proceeded by carbon adsorption on the surface after dehydrogenation of methane. It is then followed by a successive connection of carbon atoms to form the hexagonal sp^2 carbon structure. [20,76]

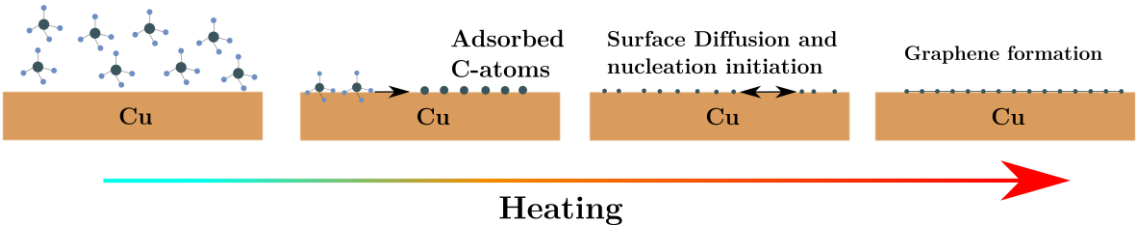


Figure 2.15. Graphene formation sequence over copper substrate.

Domination of the surface mechanism in graphene growth over copper has been reported to hold true by an isotopic labelling technique where carbon atoms were tracked during the growth process. [65,67] The stable electronic configuration of copper as can be seen in Figure 2.16a results in a single electron in its outer shell (4s) orbital that weakly that enables a delocalised bonding condition with graphene.

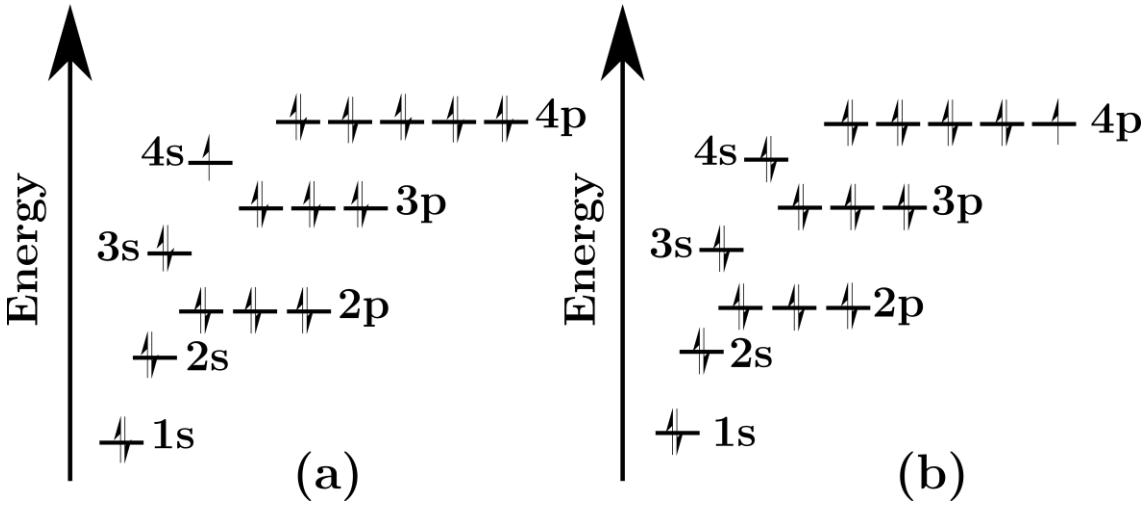


Figure 2.16. The (a) stable and (b) expected electronic configuration of copper. (motivated by [31][)

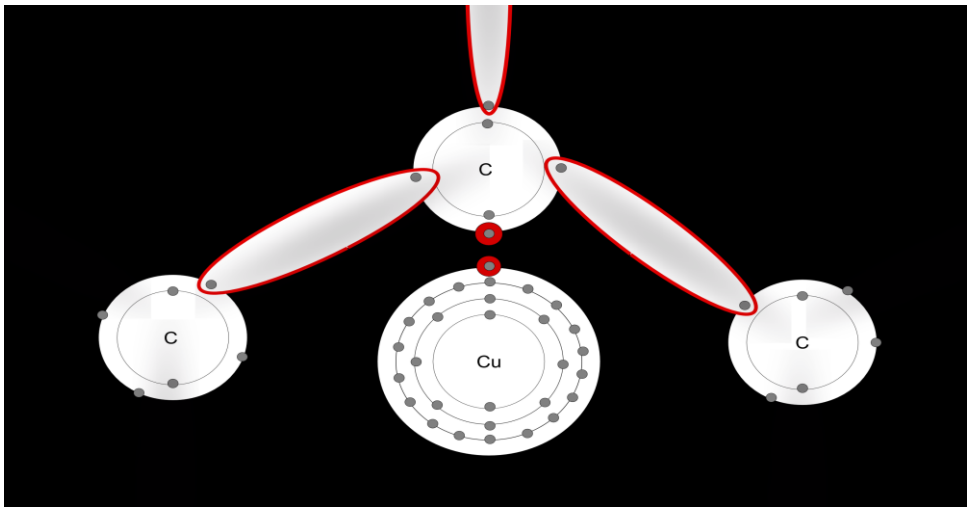


Figure 2.17. Three electrons per carbon atom form three hybridised in-plane sigma bonds, whereas the delocalised fourth electrons bond weakly to outer-shell electron of copper atoms.

The adhesion energy measurements have shown that the bonding between copper and a carbon atom is weaker than that of nickel. [69] The Nanoscratch technique was used to measure the adhesion energy of carbon atoms to metallic surfaces. By debonding graphene from copper and nickel surface in independent measurements, the interfacial energy for each material was found. The covalent bonding between graphene and nickel was found to be stronger than that on copper (70 J/m^2 for nickel compared to 10 J/m^2 for copper). This is attributed to the density of covalent bonds which appears to be higher between nickel and graphene compared to that of copper and graphene interface. The fact that the adhesion energy between graphene and metals is much higher than that and silicon dioxide which explains the impossibility of transferring graphene directly from copper to a silicon substrate by simply pressing it down.

A recent development in the CVD graphene growth involved utilisation of germanium substrates. [70,71] Lee et al. [70] used single crystal hydrogen terminated germanium substrate to grow single-crystal graphene film (as opposed to polycrystalline graphene conventionally grown on polycrystalline copper substrates). Germanium has a very low carbon solubility and catalytic activity on its surface as well as a similar coefficient of thermal expansion to graphene. During the CVD process (similar to that on copper), a gas flow of methane and hydrogen (CH_4:H_2 0.01) at a total pressure of 130 mbar at 900°C was employed. Mobility of about 7000 $cm^2V^{-1}s^{-1}$ were reported for the single crystal graphene films that were grown using this method.

One of the core questions that can arise from production perspective is the reason for not utilising Silicon itself as the growth substrate, which can greatly facilitate integration of graphene with the existing silicon technology. This is simply due to the fact that silicon's high carbon solubility and low carbon surface diffusivity transforms it into an unfavourable graphene growth platform.

One of the main purposes of choosing CVD technique over the other available methods is to achieve a continuous scalable single-layer graphene compatible with industrially matured processes. Among the mentioned metallic substrates, it is believed that Cobalt has an excess of carbon precipitation on cooling, which results in undesirable thickness variation across the graphene film. [72] Ruthenium has a high carbon solubility, but large area single-layer graphene growth is achievable owing to the absence of carbide phase under growth conditions, [20] however, this metal is very expensive. Difficulties in achieving single layer graphene over the entire surface of nickel substrates, effectively due to lack of precise control over the precipitation process at the grain boundaries, presents great challenges in pursuing growth of defect free graphene films on this metal. [20,72] There have also been efforts on growing graphene on nickel [73] and copper [26] thin films of 1μm and 500nm respectively. Multilayers of graphene were obtained on the nickel thin film [73] but copper thin film was reported to be unstable under growth conditions due to diffusion of silica nanoparticles onto copper surface and therefore it was not found to be a suitable choice for graphene growth. [26] Among all the noted metal substrates, copper foil possesses the most promising properties. It has low carbon solubility, offers more facile and controllable transfer mechanism, and is readily available at a comparatively cheap price. [20]

Attaining high quality graphene films of carrier mobility relatively closer to that achievable by the mechanical exfoliation technique (>50000 $cm^2.V^{-1}.s^{-1}$ at RT) requires thorough investigation of all the potential factors and parameters in every stage of synthesis. Both preparation of the substrate and surface treatments are known to be crucial prior to deposition in obtaining highly homogeneous films with no thickness variations. [20,82] Essential treatments include surface cleaning, flattening, and pre-annealing to remove contaminations, where annealing also contributes in copper grain enlargement. [26] It is believed that lowering the

nucleation densities and having larger domain sizes lead to enhancement of transport properties of graphene. This is because domains boundaries essentially act as scattering regions and result in lower carriers' mobility. [20,26,67,74] However, electrical measurements carried out by Kim and his colleagues [75] suggest possibility of having high carrier conductivity by having smaller domains, which is contrary to the observation of the previously mentioned groups. The choice of growth temperature and also methane to hydrogen gas flow ratio have been found to play critical role in achieving large domains and low nucleation densities. [65,67,74,76,77] Detailed experimental conditions for graphene synthesis process on copper foil reported by various groups are summarised in Table 2.1. It is noticeable that larger domains of single-layer graphene with fewer nucleation densities tend to be achieved by keeping the methane to hydrogen partial pressure low and a relatively low growth pressure (0.5-4 mbar). It is also apparent the gas flow conditions are preserved during the cooling in majority of the recipes.

Table 2.1. Summary of the widely used graphene growth steps and experimental conditions at each stage of the growth on polycrystalline copper foils.

Stages / Cu Samples	Heating		Pre-growth annealing			Growth			Cooling		Highlights
	Rate (°C/m)	Ar:H_2 (sccm)	*T (°C), t (min)*	Ar:H_2 (sccm)	*P(total) mbar*	*T (°C), t (min)*	Ar:H_2:CH_4 (sccm)	*P(total) mbar*	Rate (°C/m)	Ar:H_2:CH_4 (sccm)	
Copper foil (25 µm) [32]	33.3	100:5	1000, 30	100:5	-	1000, 30	100:5:0.5	4.10	~4	100:5:0.5	Observation of Nucleation density
Copper foil (25 µm) [34]	36	0:10	1000, 35	0:10	0.43	1000, 30	0:7:15	0.83	-	0:7:15	Monolayer Graphene
Copper foil (25 µm) [29]	22.2	0:2	1000, 15	0:2	0.05	1000, 30	0:2:35	0.67	~45	0:2:35	Monolayer Graphene
Copper foil (25 µm) [30]	22.2	0:2	1035, 20	0:2	0.05	1035, 2.5 1035, 1	0:2:7 0:2:X	0.16 2.00	~45	0:7:15	Large Domain Monolayer Graphene
Copper foil (25 µm) [33]	-	0:7	1000, 20	0:7	0.05	1000, 30	0:30:7	0.67	-	0:30:7 until 600°C and 0:30:0 below 600°C	Monolayer Graphene
Copper foil (25 µm) [78]	-	0:500	1035, 420	0:500	1500	1035, 120	0:70:0.15	142	-	-	Large Domain Monolayer Graphene

2.4.1.1 Chemical Treatments and Annealing of Copper

Often electropolishing is employed to clean surface of copper prior to graphene growth. The advantage of electropolishing over other chemical method is that it completely removes the natural oxide on the surface of copper while resulting in a highly smooth surface. In this work, the oxide is removed via acetic acid treatment as will be discussed in details in 4.1. In order to reduce the roughness of the copper surface and avoid post-growth wrinkles, high temperature annealing will be required. Preforming the annealing step at a high pressure is also recommended as copper evaporation can be retained to a lower degree.

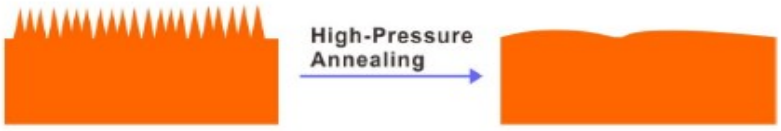


Figure 2.18. Schematics showing the creation of a smooth copper surface via high-pressure annealing. [78]

2.4.1.2 Role of Methane and Hydrogen Molecules

A high growth pressure combined with a very low methane flow rate are known to be effective in restricting formation of high density double layers and increasing the chances of enlarging the single layer domains. It has been reported that increasing the growth pressure from 8 Torr to 108 Torr resulted in a change of domain shape from squares to hexagons. This suggests that the growth pressure can effectively determine the shape of the domains. [78]

On the other hand, it is known that a high methane flow rate highly encourages the formation of bilayer and multilayers by encouraging the diffusion of carbon atoms towards the active sites where the first layer of graphene had already nucleated. [79] Nie *et al.* [80] reported that at a high growth concentration of methane, an underlay mechanism will take place. According to this mechanism, after formation of the first graphene layer, the following carbon atoms will diffuse underneath the first layer, migrating towards the centre of the active area. This is

attributed to the higher kinetic energy on the activation site compared to the energy associated with the bonding of the carbon atoms to the sides of the already formed domains. Increasing the carbon source flow rate speeds this process up before the full coverage is obtained, leading to a higher density of double-layer and potentially multi-layer films. Results from the low energy electron diffraction from graphene LEED technique, which was used to detect the order of graphene layers also implies that the second layer does indeed form next to substrate and not on top of the first layer. This is in good agreement with the mentioned theory. [80] It can therefore be concluded that the second layer grows next to copper, below the initially formed single layer.

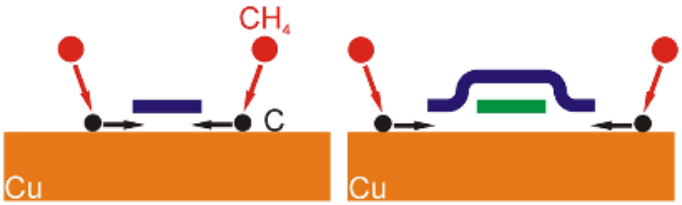


Figure 2.19. A possible mechanism for formation of graphene double/multi-layer films (green) underneath the initially formed (blue) graphene island. [80]

Moreover, active sites such as wrinkles, point defects (missing atoms), and grain boundaries have a lower activation energy associated with them and therefore graphene is expected to initiate nucleating at these sites via a heterogeneous nucleation process. In such nucleation, the Gibbs energy is largely reduced due to presence of the defects.

2.4.1.3 Role of Oxygen Molecules

The dendritic shapes of the domains and also the lower numbers of domain density are both correlated with oxygen content at the surface of copper. As mentioned previously, graphene has a tendency to grow at active sites of the surface such as impurities and defects. These sites are also attractive to oxygen atoms, where their presence on these locations would result in passivation of the available sites for graphene nucleation. This has shown to give rise to dendritic shapes of graphene

domains as apparent from the SEM micrographs in Figure 2.20. It is also believed that oxygen, through a different kinetic route compared to its passivation behaviour, can result in a facilitated graphene growth via enhancing the dissociation of CH_x components into carbon atoms. This is attributed to the OH groups that result from interaction of CH_x and oxygen atoms. [81]

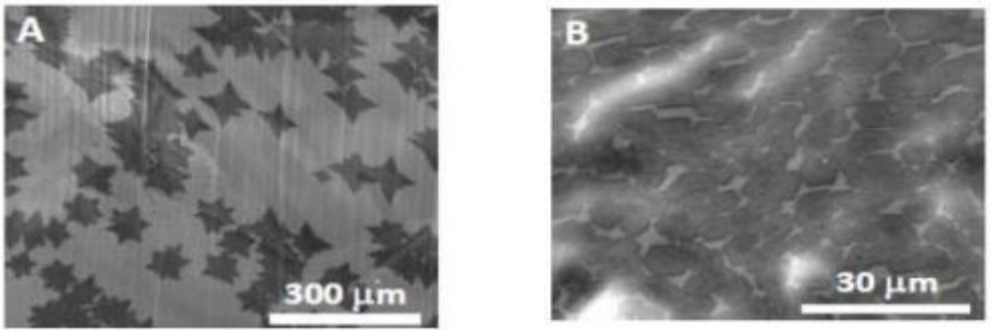


Figure 2.20. SEM micrographs of the graphene domains grown under low CVD pressure of 0.1torr H_2 on a A) oxygen rich and a B) oxygen free copper substrate. [81]

2.4.2 Other Growth Techniques

There are three other well established graphene growth techniques that are widely being used by various groups. Although they do not offer the scalability that the CVD method does, they do have other advantages associated with them. A brief introduction to each of these methods is presented below.

2.4.2.1 Mechanical Exfoliation

The first isolated single layer graphene was obtained by the mechanical exfoliation of highly oriented pyrolytic graphite (HOPG). [9] In this technique, a scotch tape was used and repeated precise peeling of the graphite flakes was carried. This was done simply by pressing the tape against the substrate and lifting it away. The substrate was treated via an ultrasound cleaning technique to remove the thicker flakes until single-layer/few-layer graphene film was remained on the surface. The peeling is a consequence of breaking the weak Van der Waals bonds between the graphene sheets, which are much weaker than the in-plane σ bonds. This method

is known to yield monolayer graphene films with the best structural integrity [20] and the highest carrier mobility [82] at room temperature. There are however a number of drawbacks associated with this technique. The inability to produce wafer-scale graphene [82] as well as its lack of capability to produce films with thickness uniformity limits industrial use of this graphene fabrication method and therefore restricts it to lab-based research use. [3]

2.4.2.2 Chemical Reduction of Graphite Oxide

Single layer graphene can be derived from graphite oxide through chemical reduction of the oxide sheets via using potassium hydroxide (KOH) solution to produce reduced graphene oxide, which is then dispersed in the solution. [61] Addition of hydrazine monohydrate compound to the solution along with a constant stirring for 6 hours is typically carried out while retaining the process temperature at 35°C. The produced films can then be deposited on various substrates. It is believed that although the associated cost with this chemically assisted technique is low, but the graphene films suffer from a large degree of structural defects, which limits this fabrication method from device applications perspectives. [3]

2.4.2.3 Epitaxial Growth on Silicon Carbide

Monolayer graphene film can also be grown epitaxially on a silicon carbide substrate (6H-SiC (0001)). [62] N-doped 6H-SiC (0001) wafer is usually annealed at the temperature of 1275°C under the flow of argon gas while retaining the pressure to a very low value (about 10^{-13} atm) for a few minutes. This allows for silicon atoms to be sublimated. The subsequent desorption then results in a homogeneous monolayer graphene film to be formed. Despite the success with obtaining high quality graphene films, this method is not an ideal choice of growth merely due the high cost of silicon carbide substrates. [3,28]

2.5 Graphene Transfer

Successful growth of graphene on copper is only one part of making graphene based devices. The other important constituent is the separating graphene from copper and transferring it onto a target surface. Wet and dry transfer techniques are known to be the two major methods of graphene transfer.

2.5.1 Wet Transfer

In order to transfer a graphene film on to the target substrate via the wet transfer method, copper is first coated with a polymeric film such as Poly(methyl methacrylate) (PMMA). The polymer acts as a support layer, protecting graphene from the subsequent transfer steps. As can be seen in Figure 2.21, the coating is then followed by immersing the stack in an etchant solution such as Ferric Chloride (FeCl3) or ammonium persulfate $(NH_4)_2S_2O_8$) to fully remove the underlying copper substrate. [3,28,65,83] The floating PMMA/graphene stack will be then transferred to a water bath and then onto the desired substrate. Next, substrate is heat treated and placed in a solvent solution to remove the polymer coating. This would leave the graphene layer on the surface of the substrate.

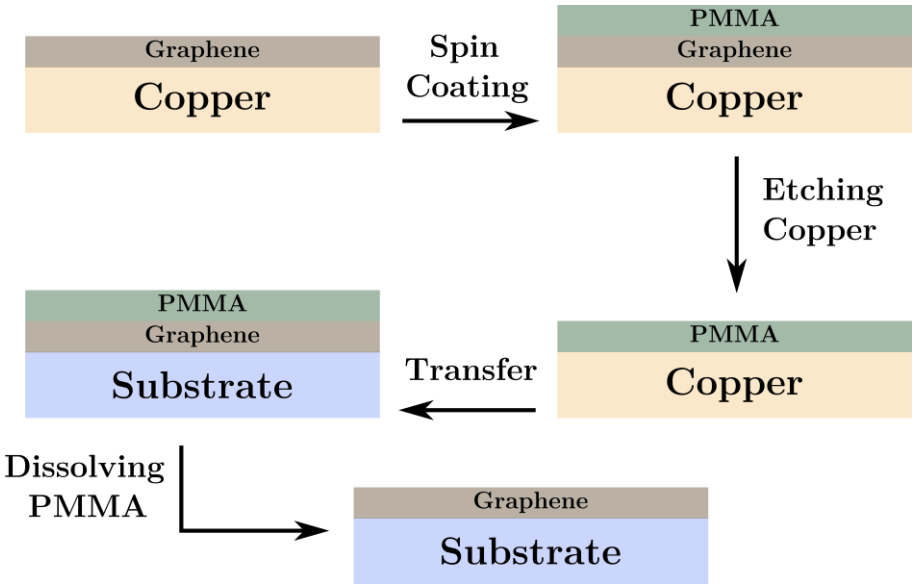


Figure 2.21. Schematic representation of the CVD graphene wet transfer process onto a target substrate.

It is worth noting that a recent research [22] suggests that the mechanical properties of the films are strongly affected by the wet transfer. It was reported that films are damaged as structural defects are introduced during the transfer process. It was recommended to use thermal release tapes in a roll-to-roll transferring technique as an alternative approach (see Figure 2.22). [22] This process is currently being used by Graphene Square for a large scale transfer of graphene onto various substrates. [84]

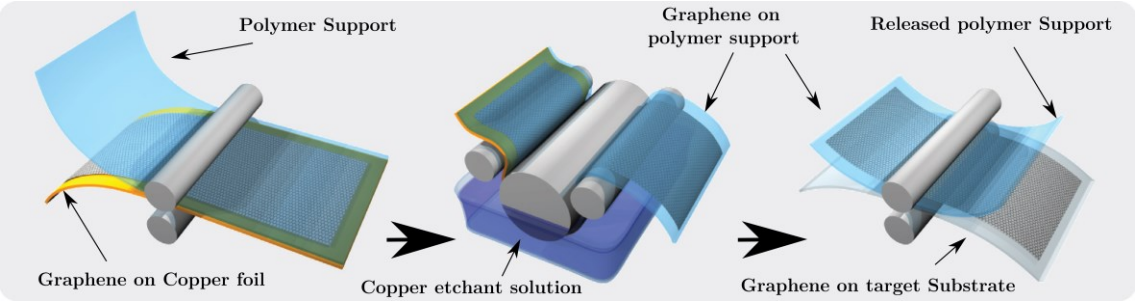


Figure 2.22: The roll-to-roll transfer of graphene film to a target substrate. [22]

Wet transfer can also be completed by taking advantage of the water hydrolysis. As shown in Figure 2.23, in such method, a potential is applied between cathode (typically platinum) and anode (copper substrate) in an electrolyte and the produced hydrogen bubbles help detach copper from pmma/graphene stack.

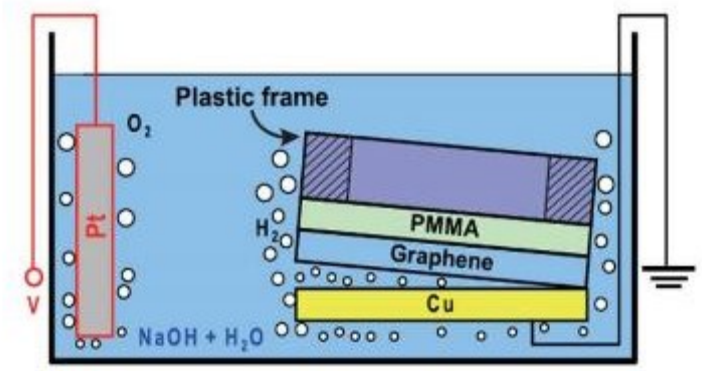


Figure 2.23. The process of water electrolysis that is used to remove copper from PMMA/graphene stack. [85]

2.5.2 Dry Transfer

The dry transfer technique has recently begun to become a popular transfer method due to the flexibility and the freedom that it offers. [86] This technique utilises an

elastomer stamp that adheres to a supporting polymer layer (such as PMMA). Similar to wet transfer, the stack is then placed in an etchant solution for removal of the underlying copper. This is then followed by stamping of graphene/PMMA on the target substrate and subsequent removal of the stamp together with the supporting polymer. This method has been investigated and assessed in this work, however, it was not found to be a consistently successful method in delivering defect-free graphene films. The results will be presented later on in 4.5.3.

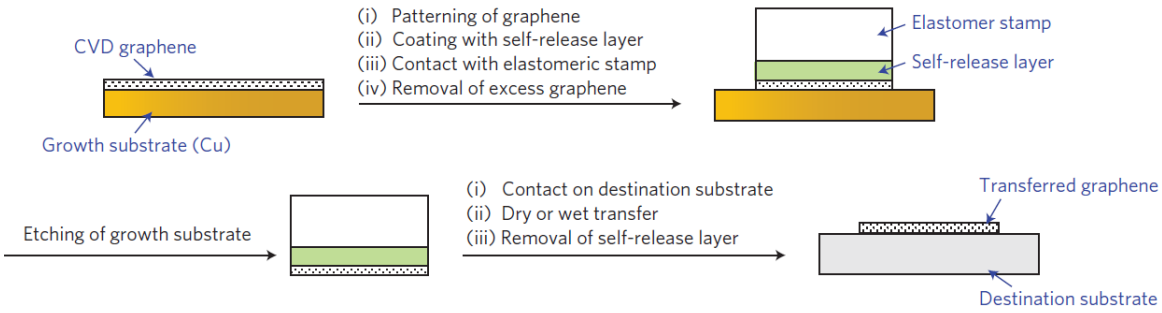


Figure 2.24. Schematics illustrating the step-by-step stages of the graphene dry-transfer method. [86]

2.6 Post-Transfer PMMA Removal

2.6.1 Solvents

Most researchers working with graphene utilise acetone for removal of pmma. There have been reports of employing solvents such as chloroform/methanol mixture, [87] acetic acid [88] and dichloromethane. [89] Other solvents such as, tetrahydrofuran (THF), and anisole can also be used to dissolve the PMMA film. Due to the existing uncertainty about the ideal choice of solvent to remove PMMA, variety of solvents are investigated in this work. (Section 4.5.1)

2.6.2 Annealing

Although many groups use solvent-based methods to remove PMMA, Lin et al. [90] investigated how clean CVD graphene sheets really are when PMMA is removed via annealing. It was found that a two-step annealing process yields a cleaner

graphene compared to other annealing procedures; the first step involved annealing the sample in the air at the temperature of 250°C followed by a second annealing under H_2/Ar flow at the same temperature. More than 2 hours of annealing was believed to cause no difference in cleanness of the surface and in the contrary, various structural damages were observed in some cases.

Furthermore, TEM analysis revealed that two distinct layers of PMMA with different decomposition temperatures are present over the graphene layer; the top -PMMA with a lower degradation temperature (~160°C) and the bottom-PMMA film, which is in uninterrupted contact with graphene (~200°C).

It is worth noting that some of the PMMA macromolecules during the decomposition process may form a covalent bond to the graphene layer at the sites of defects such as cracks or pin holes. It may subsequently result in a local switching from the sp^2 carbon hybridization to sp^3. This is reflected in the Raman spectrum of these areas as well as a reduced Fermi velocity.

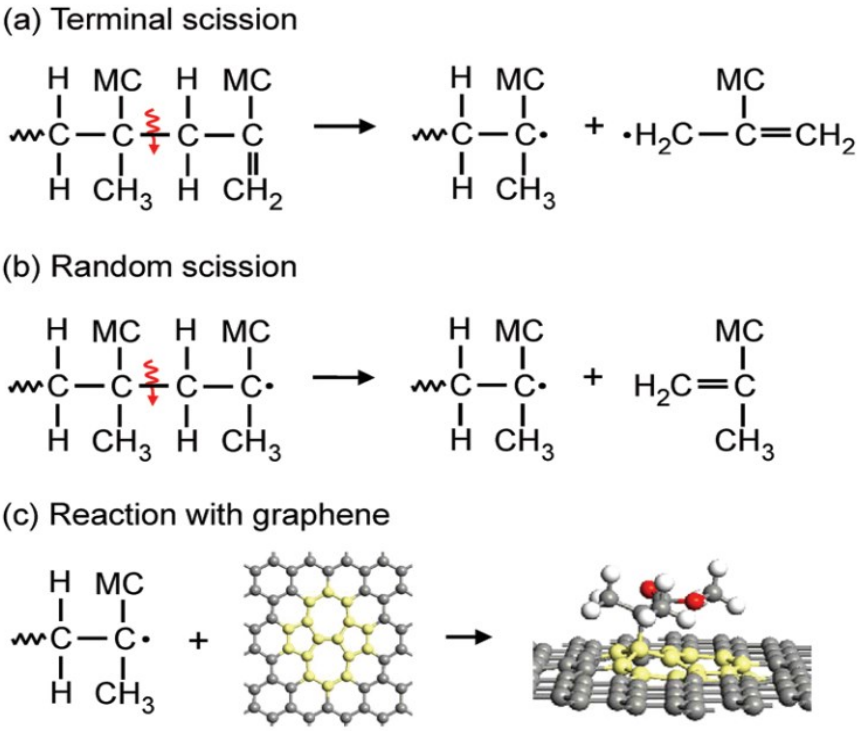


Figure 2.25. Shows (a) and (b) the two possible types of pmma on graphene due two different scission procedures and (c) potential covalent bond formation at sites of imperfection. [90]

2.7 Summary and Conclusion

This introductory chapter started by introducing graphene and its unique electronic band structure. The asymmetric field effect shape of the transport curve of graphene as one of its key characteristics was discussed in details and it was shown that graphene based field effect transistors behave differently when compared to the typical metal oxide semiconductor based field effect transistors. Complex conductivity of graphene was presented and discussed via the Kubo formula and the processes dominating the conductivity of graphene at DC, Microwave and higher frequencies were presented and discussed. Furthermore, the potential applications of graphene where transparency, unique field effect response, and flexibility of this 2D material can/has already been be exploited were reviewed. The main graphene fabrication methods were described in details, where advantages and disadvantages if each technique were discussed and the CVD technique on copper was proposed as the most ideal method. The chapter concluded with description of a step-by-step graphene transfer procedure that is widely being used for transferring CVD graphene films on various substrates. In short, chapter presented the previous state-of-art work performed on understanding of graphene as well as the methodology of producing this film and the devices based on this material. They were described to justify the use of graphene in addressing/solving the current semi-transparent graphene based FETs.

3. Characterisation Methods

Never is method something outside of the material.

"John Dewey"

Characterising the fabricated materials and devices is certainly a vital step in understanding how different materials and combinations best work together. It is an important stage that is essential to be carried in order to build up on the existing technologies.

The employed copper foils for the graphene growth, the synthesised graphene films as well as the fabricated field effect devices are characterised via a variety of methods to assess and improve their quality, morphology, and electrical properties. In this chapter, the characterisation methods that were employed in the present work along with the fundamental working concepts of each technique will be presented.

3.1 Morphology and Structural Analysis

3.1.1 Scanning Electron Microscopy (SEM) and Energy-Dispersive X-Ray Spectroscopy (EDX)

The scanning electron microscopy technique uses an electron gun to irradiate a given specimen with a beam of electrons. It is capable of revealing morphological and compositional information about the sample under test. Upon interaction of the incident electron beam with the sample, radiation such as X-rays will result that contain important information as shown in Figure 3.2. The radiation can be detected separately, which provides the necessary signal for modulation of a Cathode Ray Tube (CRT). The signals are displayed as a varying brightness on the CRT. [91] As a result, it gives rise to various contrasts that can reveal different

information about the material that is under investigation. There are two main types of scattered electrons that are separately detected and result in different contrasts; (1) Backscattered electrons (BSE) that are scattered in an elastic manner, where the scattered electrons are very close in energy to the primary electrons (incident beam) and their scattering is strongly dependant on the atomic number of the scattering atom. [92] This essentially means that the image obtained using BSE shows strong compositional contrast. On the other hand, are the (2) secondary electrons that are the result of interaction of primary electrons with the specimen, where most of the energy is lost as heat and only a small portion of it gives rise to scattering of secondary electrons (as well as X-Rays). [93] These secondary electrons therefore, have low energies and the image obtained using these electrons will have weak compositional, but strong topographical contrast. Detection of the secondary electrons is usually done using a photomultiplier system better known as the Everhart-Thornley detector [93] shown in Figure 3.1.

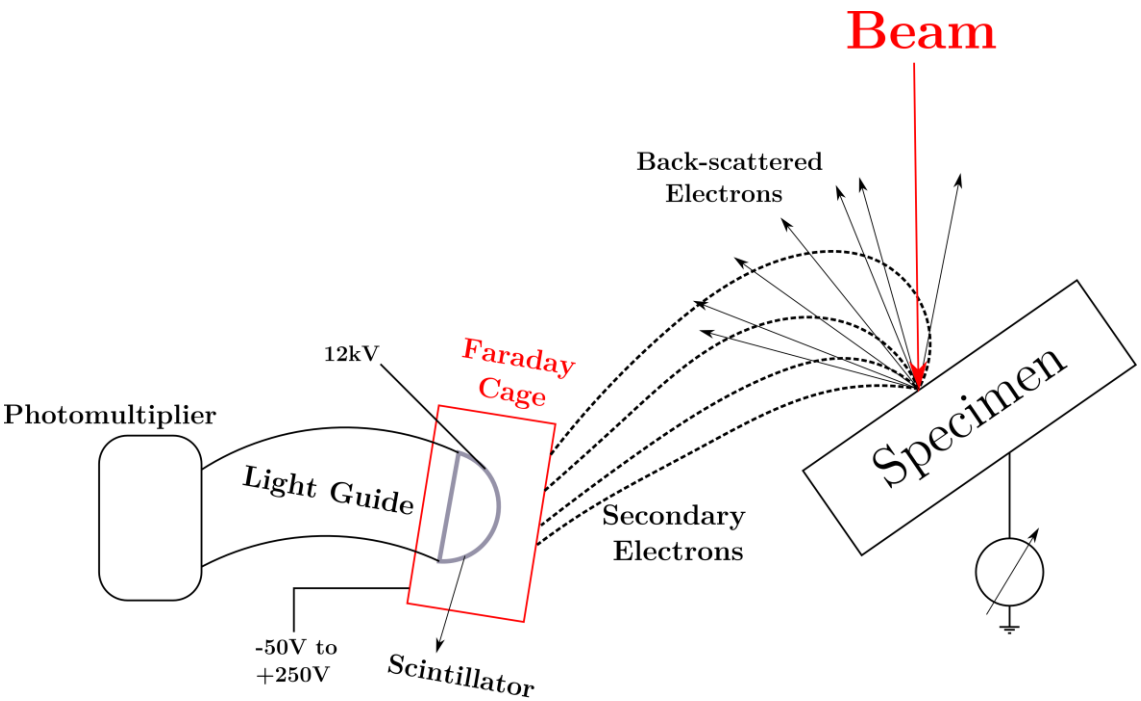


Figure 3.1. Schematic of an Everhart-Thornley detector used to detect secondary electrons.

SEM is often employed to observe the morphology of graphene on copper substrates. It is very important to be able to distinguish between the different

features in an SEM image. This would allow reaching more clear and comprehensive conclusions regarding the preliminary defects, domain sizes, and coverage area. To do so, one needs to know the expected contrast between graphene and copper substrate. Here, SEM images are obtained by detecting the backscattered electrons (BSE).

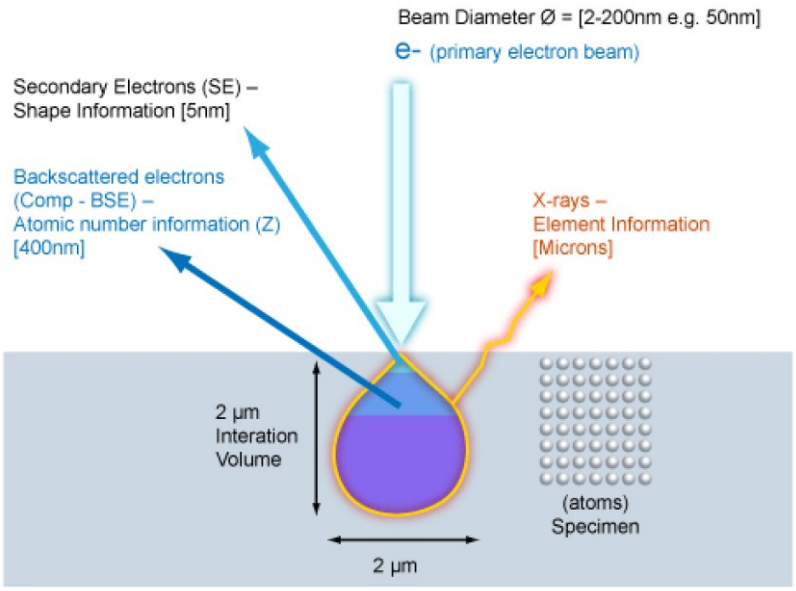


Figure 3.2. Schematic showing the different signals that are produced upon beam-specimen interaction in a SEM analysis. [94]

The number of generated backscattered electrons strongly depends on the atomic number of the sample. Considering graphene on copper, atomic number of copper (29) is much higher than that of a Carbon atom (6). Coupling this with the fact that graphene is only one layer thick, a significantly higher degree of backscattered electrons would be released from copper than graphene. It is therefore expected for graphene to look darker if placed next to copper at the same thickness. The contrast between graphene and the underlying copper however can be attributed to the losses that arise due to the graphene layer. Here the electrons are scattered from the underlying substrate, they get attenuated by graphene and result in the observed darker contrast.

Figure 3.3 displays a SEM micrograph of graphene on a polycrystalline copper substrate. Different copper grains are distinguishable owing to the apparent contrast between the different grains of the polycrystalline copper. Moreover, graphene wrinkles are noticeable as they reveal themselves by appearing darker while running against the copper step edges.

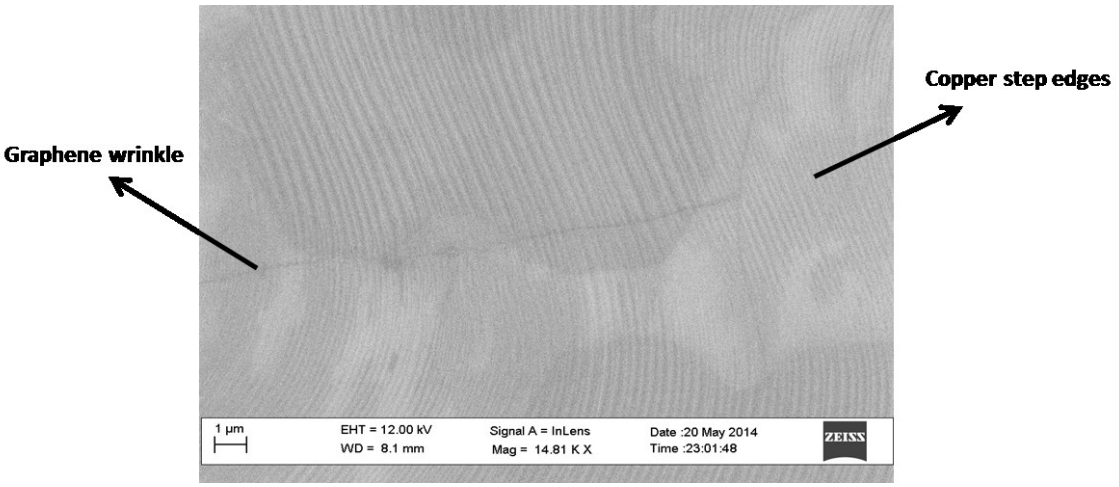


Figure 3.3. A SEM micrograph of graphene on copper. Detected wrinkle that has possibly arisen from the difference in coefficient of thermal expansion between copper and graphene or due to the polycrystallinity nature of copper.

In addition to SEM, electron backscattered diffraction (EBSD) analysis can be carried out to allows for micro-texture mapping of copper substrates. It can be used to detect different grains and estimate grain size evolution upon annealing. [95] Furthermore, energy-dispersive X-ray spectroscopy (EDX) can be used in conjunction with SEM. It also employs electrons but for the purpose of detecting various elements of the periodic table at the desired sites. However, it suffers from detecting light elements. EDX works by bombarding surface of the target material with energetic electrons that subsequently excites an electron in an inner shell, which creates a vacancy. The vacancy will then be filled by de-excitation of another electron from a further shell in order to establish a stable state. This transfer of vacancy from one shell/sub-shell to another has an X-ray emission associated it,

which is different for various atoms. In a typical EDX spectrum, the energy of the emitted X-ray photons mostly lies in the range of 1-10 keV. [96]

3.1.2 X-Ray Diffraction (XRD) and Pole Figures

X-ray diffraction technique is an eminent tool that is used to identify different phases and degree of crystallinity of various structures. In this work, X-ray analysis is used as a non-destructive technique to determine the structural properties of the copper film before and after the annealing stage as well as to identify the structural properties of different dielectric materials that will be utilised as gate insulators in the fabricated G-FET devices. The X-Ray (wavelength of 0.154 nm) beam is applied to the sample and a diffractometer is used to measure the "intensity versus diffraction angle (2θ)" of a given sample. The obtained XRD patterns can then be used along with the Bragg's equation ($n\lambda = 2dSin\theta$) to find the interplanar spacing and the diffraction planes in the samples. The key components of such a system are represented in Figure 3.4.

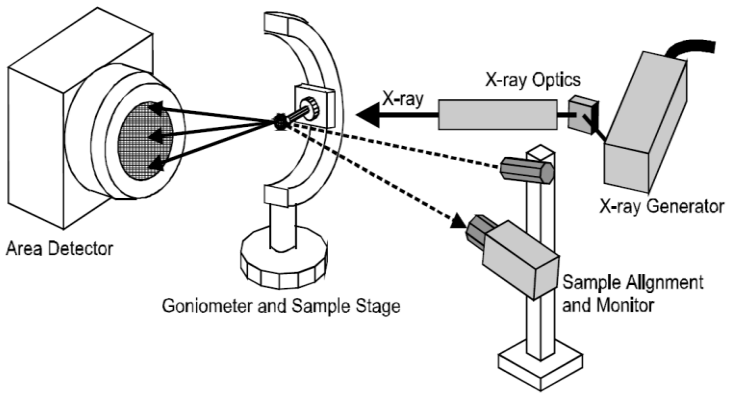


Figure 3.4. Schematic of the key elements of a typical XRD system. [97]

In the case of a copper substrate, an annealed copper foil is expected to exhibit a preferred crystallographic facets due to the recrystallization that takes place during annealing. Therefore, X-ray pole figure analysis can also be carried out in addition to XRD analysis to investigate the texture of copper before and after annealing. This method essentially delivers a map of variation in the diffracted intensities

which represents density of crystallographic planes in the sample. [98] Setting the angle of the goniometer to a specific plane, the orientation distribution in the sample with respect to the set angle can be found. Pole figures can provide a complete picture of the orientation of the crystals in the polycrystalline copper substrates.

3.1.3 Raman Spectroscopy

Raman spectroscopy is an extremely powerful tool when it comes to characterisation of graphene. It works by scattering of the incident photons (laser with a specific wavelength) upon their interaction with material's molecules. [99] In this work, the laser beam with the wavelength of 532 nm and intensity of about 1 mW is employed to characterise graphene samples. The laser scattering can take both elastic (Rayleigh) and inelastic (Raman) forms upon scattering. When elastic, scattered photons will have a similar energy to the incident ones. In the case of an inelastic scattering, photon's energy will differ from the incident beam. The intensity of the scattered photons is dependent on the structure of the material under test and can be used to characterise/identify a given material. For graphene, these characteristics Raman peaks can be used to detect the number of graphene layers, estimate the doping level (not the type of doping), form defect density mapping, and also to measure strain. [100] There are three main characteristics peaks that are typically associated with a graphene film; Graphite mode (known as G-peak), double resonance D mode (also known as diamond mode), and double-resonance 2D mode (also known as G'). Typical positions of these peaks are represented in Figure 3.5, where x-axis is essentially an indication of the shift in energy compared to the incident line, denoted as Raman shift.

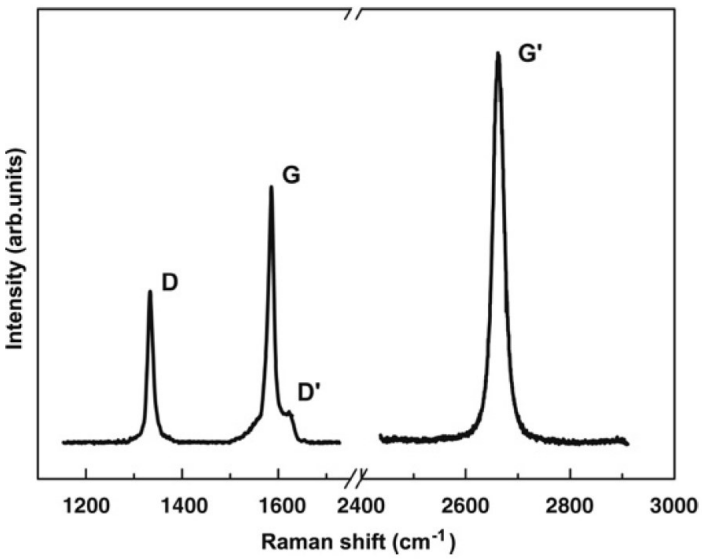


Figure 3.5. Characteristic graphene peaks under Raman spectroscopy with laser wavelength of 532nm. [101]

The processes that lead to G, D, and 2D peaks are represented in Figure 3.6. G-peak is a result of a scattering via longitudinal vibrations and is usually liberated from the incident beam energy. This mode occurs at roughly 1580 cm^{-1}. Any blue-shift in G-peak is known to be an indication of presence of certain amount of doping. [102-103] The double resonance modes are due to electron-phonon scattering. The D-mode at 1330 cm^{-1} involves an inelastic scattering of the beam with phonons and an elastic one with defects; hence it is used as a measure of defect concentration in graphene. The D-peak reflects not only defect density in graphene samples obtained by exfoliation method, but also it can be an indication of inhomogeneity of crystal domains for the graphene grown via CVD. [102-103] Therefore, the D-peak is expected to be intensified when a higher degree of disorder is present in lattice of graphene. The 2D peak (at about 2700 cm^{-1}) occurs upon two inelastic scatterings. It takes place when two phonons of reverse momentum are scattered next to high symmetry points of graphene, K and K' of the primary BZ. [90] If there is a second layer of graphene involved, interaction of the layers will result in re-configuration of the conduction bands. The FWHM of the peak in such structure will then be expected to be broader and blue-shifted (by about 20 cm^{-1}) compared to when there is only one layer of graphene present. FWHM of the 2D peak, 30 cm^{-1}, and its ratio with

the G-peak of more than 2 for undoped samples are generally used as reference values for monolayer graphene. [101] Defect-free graphene is also expected to have a D/G ratio of less than 0.3.

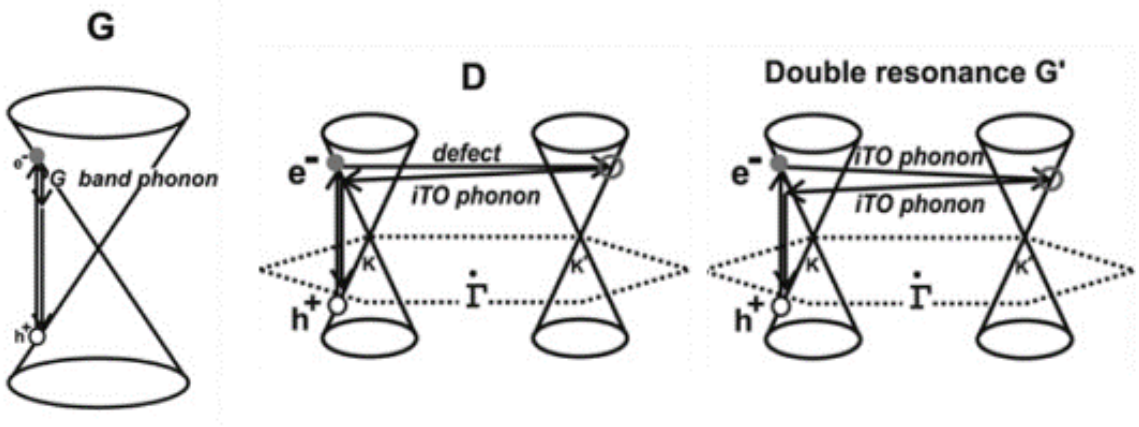


Figure 3.6. The schematics representation of the different processes that lead to the G, D, and 2D peaks. [101]

Ferrari et al. [104] report that the drop in the I(2D)/I(G) is observed due to an increase in the carrier concentration (doping) of the graphene sheet also supported by the experimental data obtained by Lin et al. [105] As mentioned before, this doping can occur upon application of an external gate voltage or/and can come from trapped interface charges and the various treatments done on the substrate. The doping is also known to reflect itself in the spectrum by a blue shift in the position of the G-peak. This shift is believed to be more significant than that of the 2D peak. [103] Figure 3.7 illustrates the expected the 2D and the G peaks for different layers of pure graphene transferred on quartz and SiO2/Si substrates. The expected Raman peak positions of graphene on SiO_2/Si as well as quartz substrates are also presented in Table 3.1.

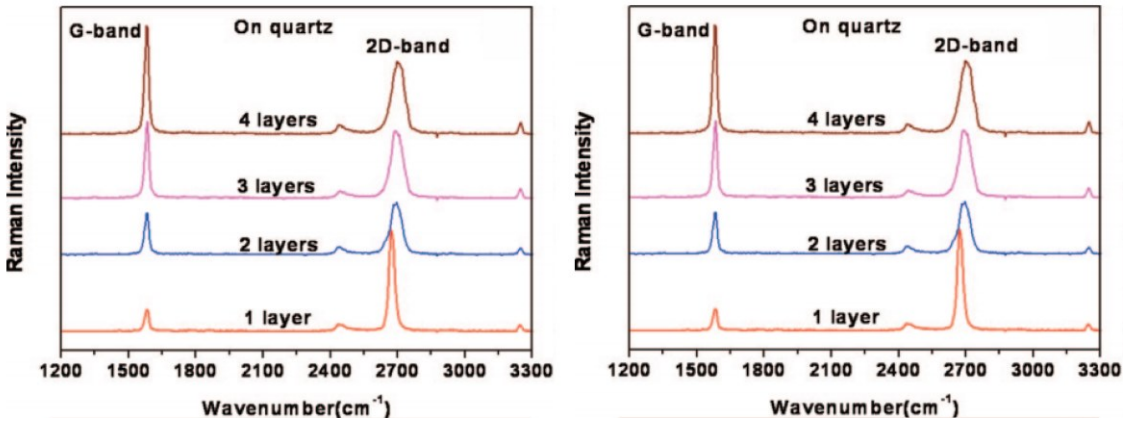


Figure 3.7. The typical G and 2D peaks for different graphene number of layers on quartz (left) and SiO2/Si (right) substrates. [103]

Table 3.1. The expected position and the full width at half maximum of the 2D and the G peaks of graphene on SiO_2/Si and quartz substrates. [103]

Substrate	G-Band Position (cm^{-1})	G-Band FWHM (cm^{-1})	2D-Band Position (cm^{-1})	2D-Band FWHM (cm^{-1})
SiO_2/Si	1580-1588	6-16	2676	24-32
Quartz	1582	15.6	2675	29

3.1.4 Atomic Force Microscopy (AFM)

Atomic force microscopy is generally used to map out the topography of a given sample with an extremely high out of plane resolution (down to atomic levels). It can be used to get an accurate measure of the surface roughness and to measure thickness of atomically thick samples. [99] As shown in Figure 3.8, it employs a cantilever with an extremely sharp tip (below ten nanometre), which approaches the surface of the sample. It is then deflected as it comes to close proximity of a given surface. The deflection is measured by a laser beam, which is focused on the top surface of the cantilever. By keeping the position of the tip vertically constant and performing a scan over the desired area, the variation in z-direction can be easily mapped out. Table 3.2 summarises some of the measured thickness values in the literature for Raman-confirmed single-layer graphene films that were grown via both CVD and mechanical exfoliation methods.

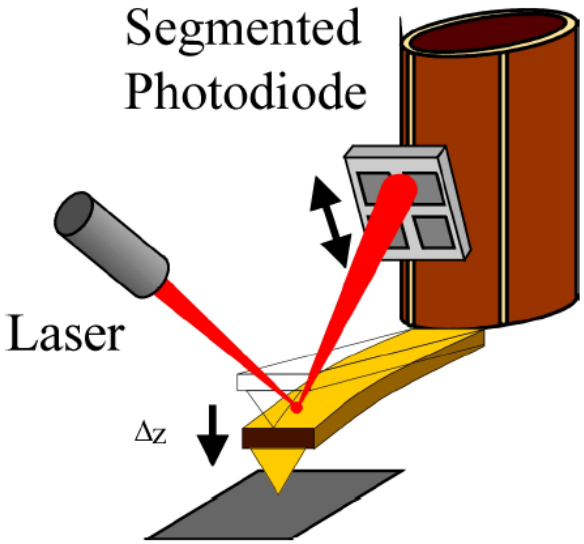


Figure 3.8.Schematics presentation of the basic working principles of an Atomic Force Microscopy system. [99]

Table 3.2 The measured thickness of both CVD and mechanically exfoliated prepared single-layer graphene transferred on SiO_2/Si substrates.

Graphene Type	AFM Mode	Recorded Thickness (nm)
CVD [106]	Tapping mode	1.8
Mechanical Exfoliation [107]	Tapping mode	0.4-1.7
Mechanical Exfoliation [108,109]	Contact Mode	0.4-1

3.1.5 Optical Microscopy

Optical microscopy is usually used to observe contrast (if any) between graphene (Single and multilayer) and the underlying substrate. Presence of an optical contrast is beneficial when it comes to performing different processes on graphene such as photolithography. For quartz substrates, both materials have a high optical transparency which makes it very difficult to observe any contrast. A typical optical microscopy equipment is illustrated in Figure 3.9. Resolution for a typical optical microscope takes the value of one wavelength.

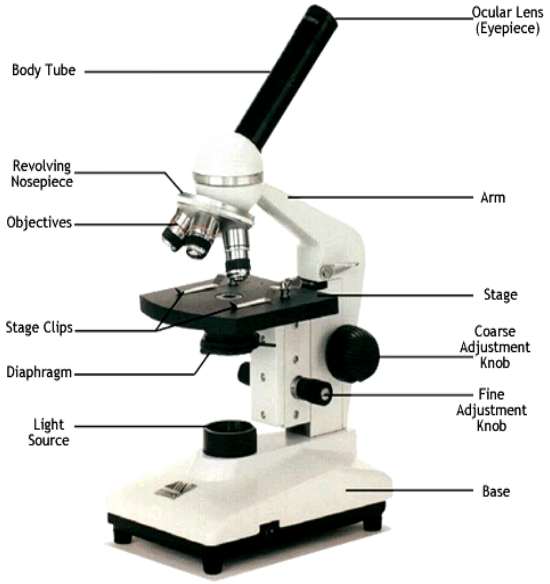


Figure 3.9. The major components of a typical optical microscopy system. [110]

By employing the relationship between the complex refractive indices of graphene, silicon dioxide, and silicon to their complex relative permittivity, Blake et al. [111] were able to find the oxide thickness that is necessary to observe a clear interference on the substrate. Fresnel law was employed to investigate how the thickness of SiO_2 as well as the light wavelength are correlated with the observed contrast. Intensity of the reflected light was measured with ($I_{Graphene}$) and without graphene ($I_{Substrate}$) for various oxide thicknesses while taking the refractive indices of both SiO_2 and graphene into account. The contrast was simply calculated via $C = (I_{Substrate} - I_{Graphene})/(I_{Substrate})$. It was shown that an oxide layer of thickness 90 nm and 280 nm would have the best contrast under white light while using no filters. [111]

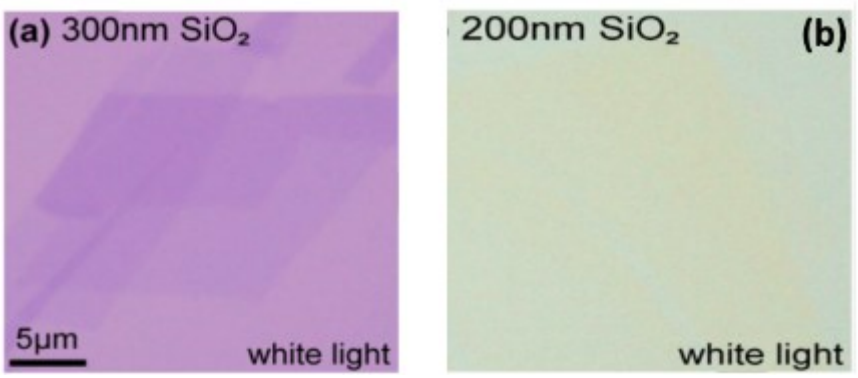


Figure 3.10. Optical contrast of graphene under white light when deposited on silicon oxide of different thicknesses. [111]

As shown in Figure 3.10, the transparency of graphene significantly improves by replacing a substrate with 200 nm of oxide by one with 300 nm thick SiO_2. Otherwise, appropriate optical filters will need to be used in to achieve a good contrast for different oxide thicknesses. This is summarised in the following graph, where the scale represents the anticipated contrast.

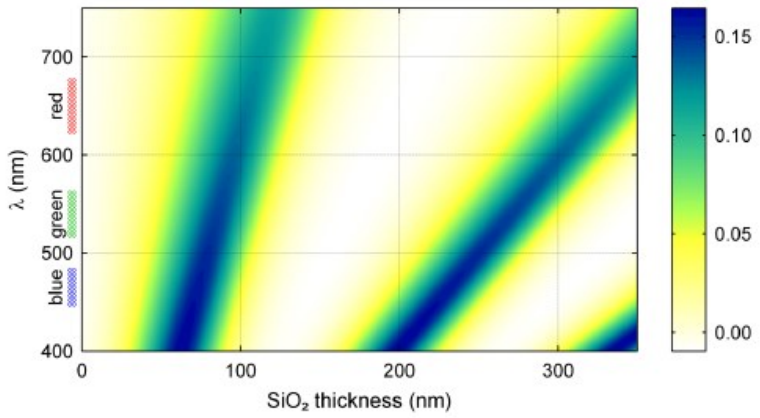


Figure 3.11. The achievable contrast of graphene on silicon dioxide of different thickness values with the appropriate filters included. [111]

3.2 Electrical Characterisation

In this section, I'll be looking at the techniques that were used in the present work to characterise the electrical properties of the fabricate graphene and graphene based field effect structures at the DC and microwave frequencies.

3.2.1 Two-Point Vs Four-Point DC Measurements

In measuring the DC electrical properties of graphene and the field effect devices that employ graphene, electrical contacts are made to both the conducting channel and the gate electrode. [112] The measurements can be performed in two conventional ways of two-point or four-point contacts techniques.

Often measuring a small current is easier than measuring a small voltage, hence voltage is applied between source and drain (two-points), and current is measured. In case of graphene, a low voltage is applied in order to have a low current flowing

(μA scale), limiting dissipation of power. It is important to note that in this way, the resistance of leads as well as contacts are included in the measurements. For sub-Ohm measurements, the two-point method can result in a large degree of inaccuracy.

Alternatively, four-wire method can be employed. Here, four contacts are made in an array, separated from each other by a known distance. A known current is applied between two contact points and the resulting voltage is measured between the other two distinct points. This way the lead/contact resistances can be avoided. However, it is important to note that for large scale industrial integrated circuits, two point contacts are preferred. This effectively means that obtaining low resistance Ohmic contacts is crucial. [112] Figure 3.12 shows the difference between two-point and 4-point measurement techniques.

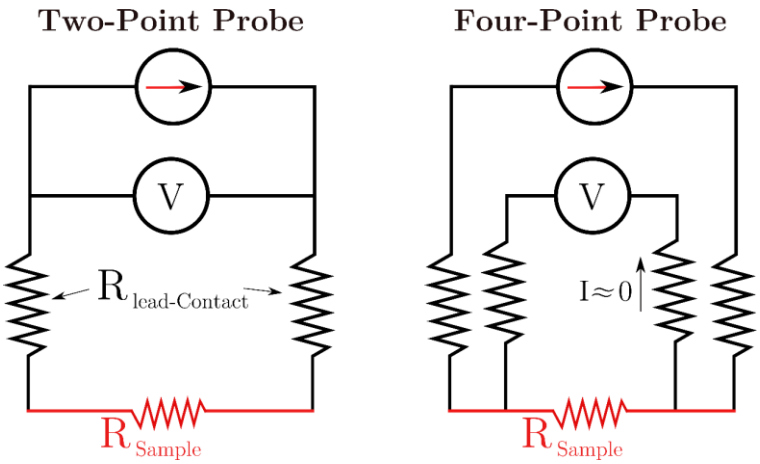


Figure 3.12. Two-point and four-point methods of measuring resistance of a given sample.

Currently amongst the available methods, Van der Pauw is a widely used method of measuring conductivity of thin films. It's a contact-mode low resistance measurement technique, where thickness of the structure under test is typically insignificant compared to its area. Contacts are made very small and are situated close to the boundaries of the surface. [113] It works according to the four-point probe principles, where a certain amount of current is applied and the subsequent voltage change across any two points is measured. This gives rise to a number of resistances

across the sheet, which are used find the overall sheet resistance and hence the conductivity of the thin film under investigation. The typical configuration of a Van der Pauw measurement and the equations that are used for sheet resistance calculations are shown in Figure 3.13, Eq. 3.1 and Eq. 3.2 respectively. The resistance of any material is in fact a function of its resistivity and volume (volume resistance). However, for a material such as graphene with a negligible thickness compared to its surface area, sheet resistance (ohms per square) is used to avoid confusion with the volume resistance (ohms).

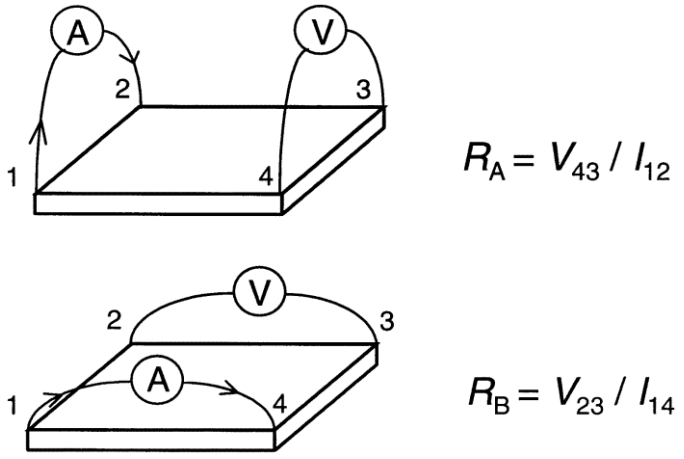


Figure 3.13.Sheet resistance measurements using square van der pauw configuration. [114]

$$e^{-\pi R_A/R_S} + e^{-\pi R_B/R_S} = 1 \tag{3.1}$$

$$R_S = \frac{\rho}{t} = \frac{\pi(R_A+R_B)}{2\ln(2)}\, c \tag{3.2}$$

This work utilises a state-of-art dual channel Keithley Sourcemeter with voltage source capacity of 200 V on each channel to generate, measure and monitor DC voltage and current in characterisation of the devices.

3.2.1.1 Field Effect Measurements at DC

The field effect measurements in DC is carried out following the same procedures that were explained in chapter 2.5. Constant current of 200 mV is applied between the source and drain terminals and the current in the graphene channel is measured

as a function of gate voltage (V_{GS}). Sheet resistance value at every point is then used to calculate both the resistivity and conductivity of the graphene channel. The areal density of the charge carriers is determined according to Eq. 2.30 and conductivity versus carrier concentration plot is constructed. The mobility of the graphene is then calculated via three different methods; (1) by using the gradient of the plot (close to the Dirac point) as discussed in 2.3, (2) by obtaining a fit to the obtained curves via the Boltzmann's equation and (3) by performing the Hall-effect measurements.

3.2.2 Hall-Effect Measurements

The Hall-effect technique is a more reliable and accurate method of computing mobility of graphene when compared to extraction of mobility from transport curves. Hall-method can be employed to find the mobility of the carriers and their concentration in the graphene sheet at both very low and room temperatures. A magnetic field, of the order of 1.6 T perpendicular to the sample is applied while a DC current is sourced between two ends of the sample. This results in a Lorentz force and a resulting voltage to be generated in a perpendicular direction to both the supplied current and the applied magnetic field. This voltage is then measured and used to calculate carrier mobility according to Eq. 3.3. A typical Hall-bar structure is shown in Figure 3.14 below. Hall voltages are usually within the range of millivolts. Graphene samples are typically patterned via photolithography and Oxygen plasma etching to have the Hall bar structure. In this work due to the large dimensions of the samples combined with the relatively high sheet resistance of graphene that typically lies in the range of few kΩ, silver paste is used to realize the Hall-contacts on the surface of graphene.

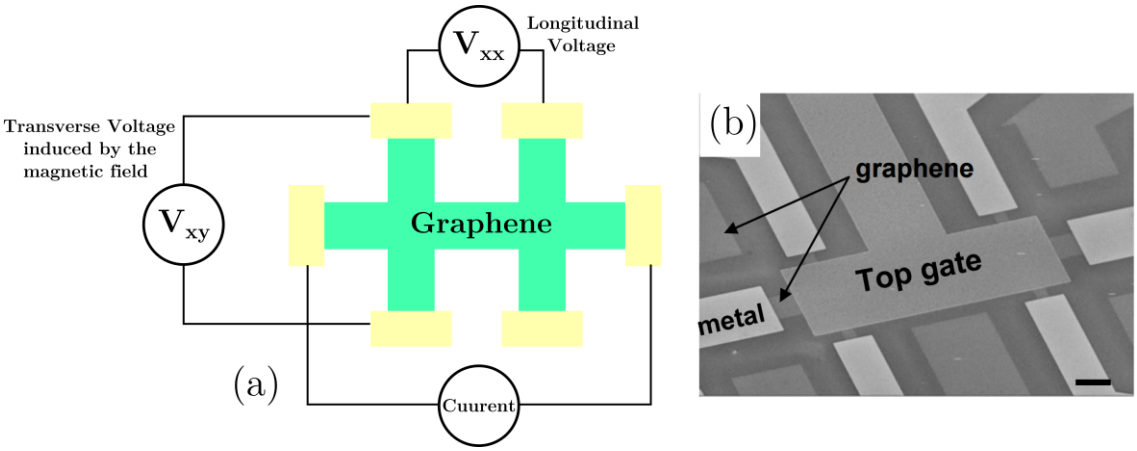


Figure 3.14. (a) The typical sample geometry that is used for Hall-effect measurements. (b) An SEM micrograph of a fabricated graphene Hall bar structure. [115,116]

$$\mu_{Hall} = \frac{|V_H t|}{BI\rho} \tag{3.3}$$

In the above equation, B is magnetic field, V_H is Hall-voltage, I is the longitudinal current, t is sample's thickness, and ρ is its resistivity. [117] The calculated mobility can then be coupled with the measured resistivity data to find the concentration of carriers in a sample. In this work, a Lake Shore Hall measurements system is used which applies magnetic field of 1.6 T and is also capable of performing measurements while gating FET structures. For convenience, the same Van der Pauw geometry shown in Figure 3.13 is adopted for the Hall-effect measurements in this work.

3.2.3 Non-Invasive Microwave Measurements

The electrical properties of graphene at microwave frequencies can also be exploited in a contact-free approach by employing a dielectric resonator in a metallic cavity. [118] It is worth noting that this technique also enables field-effect characterisation of wafer-scale graphene FET structures. The first results of such a measurement will also be presented and its efficiency and accuracy with other available methods will be compared. This will be the subject of discussion later in 4.6.

3.2.3.1 Resonant Circuits and Dielectric Resonators

Metallic cavities have the capability to store electric and magnetic energies. However, insertion of a dielectric resonator with a relatively high dielectric constant inside a metallic cavity will allow concentration of the field inside the ceramic, enabling a very sensitive tool for detection of disturbances close to its fields. The combination also allows for smaller cavities can be used at the same operating frequencies, very convenient for testing and monitoring small samples. Therefore, in this work, a metallic cavity is designed (via SolidWorks CAD software) that encloses a dielectric resonator with an incorporated aperture to allow for coupling of the field between the resonator and a given sample. The dielectric resonator is essentially a low-loss ceramic dielectric material of high permittivity, therefore the speed at which electromagnetic wave travels through material is relatively low, resulting in its immense capability of storing energy. The wavelength, impedance, and the velocity of a given electromagnetic wave is proportional to the inverse of the square root of the permittivity. [119] Therefore, by entering a high permittivity ceramic in a microwave assembly, the wave would slow down and consequently bounces forth and back in the ceramic. This results in a standing wave pattern that causes the fields to be concentrated inside the ceramic.

A general circuit that is used at both high and low frequencies is the resonant circuit (RLC), where AC source, capacitor (C), inductor (L) and resistor (R) represent an analogy to a microwave signal generator, lumped capacitor (the stored electrical energy), inductor (the stored magnetic energy) and resistors (the losses) in the system.

Figure 3.15 shows a simple resonant RLC series circuit. Resistor, inductor, and capacitor are suitable terms when the wavelength is larger than the dimensions of the circuit parts. As the wavelength becomes shorter and comparable to the physical dimensions of the circuit elements, one must take into account the effects

of wave propagation, radiation, as well as consequences of raised impedance of wirings. [120] For a microwave circuit (usually operating between 1-100 GHz), terms R, L, and C shall be used as symbols to demonstrate the electric energy losses, the magnetic energy stored, and the electric energy stored respectively, for elements at a given operation frequency. [120]

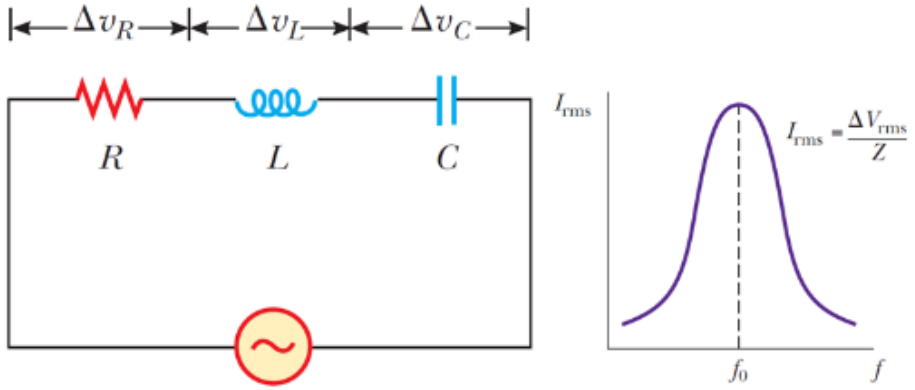


Figure 3.15. Circuit model of a typical series resonant circuit model connected to an alternating current source. [121]

The impedance of the circuit (Z) can be shown to be purely resistive at a specific frequency, better known as the resonant frequency, f_r. This is the frequency at which the maximum current (I_{rms}) is achieved assuming that $R \ll \omega L$. [121]

$$f_r = \frac{1}{2\pi\sqrt{LC}} \tag{3.4}$$

The microwave measurement configuration in the present work is comprised of a 7 mm in diameter and 3 mm thick cylindrical dielectric puck made of a barium zinc tantalate (BZT) ceramic with a very low loss tangent a high relative permittivity at microwave frequencies (10^{-4} and 29 respectively at 10 GHz) is arranged inside a copper cavity as represented by the schematics in Figure 3.16. It is important to note that the resonator is supported by a low-loss quartz stand. A circular aperture of 5mm in diameter is also designed at the centre of the top wall of the cavity. This is combined with placing the ceramic puck (fixed on top of a quartz holder) approximately 1 mm below the aperture to allow for the evanescent field to leak

through the aperture and interact with a given sample. The structure is connected to a state-of-art Rohde-Schwarz *ZVA* vector network analyser (*VNA*), where the fields are essentially coupled/excited by loop coupling technique. The *VNA* is used as the signal source, receiver, and display. It is important to note that the lid is covered by kapton tape in order to protect the *VNA* from electrical damages by preventing any potential leakage current from cavity through to the coaxial cables.

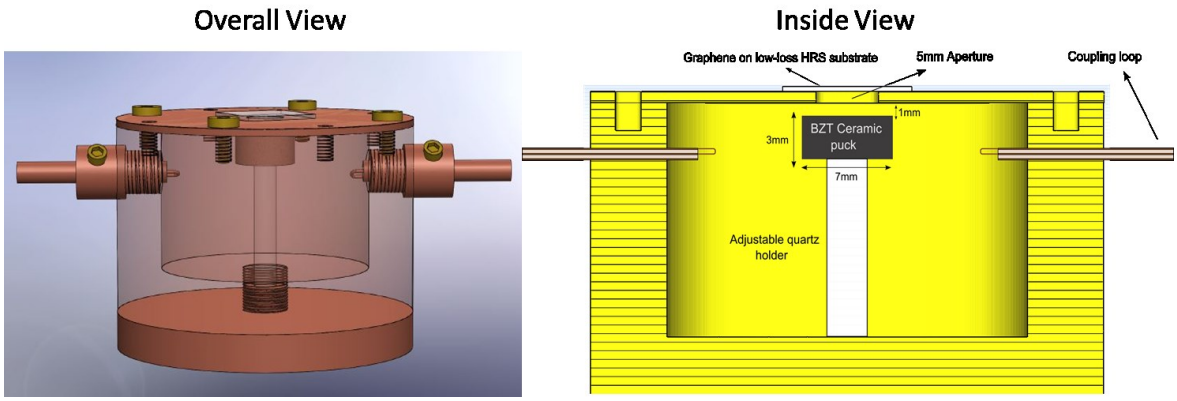


Figure 3.16. The designed microwave resonator configuration.

At the resonant frequency, the stored electric and magnetic energies inside the resonator are equal, hence the reactance is essentially zero and the impedance is purely real. Although most of the energy is stored inside the resonator but a small amount of the resonant field would be stored in air at close proximity of surface of the resonator and decays in an exponential rate as it gets further from it. A *VNA* is used and the frequency is measured over a specified range. It is then plotted against the transmitted power (in logarithm scale, decibels dB). The frequency is varied in a given bandwidth and the transmitted power is plotted against the frequency. A simple sketch of such a plot is shown in Figure 3.17.

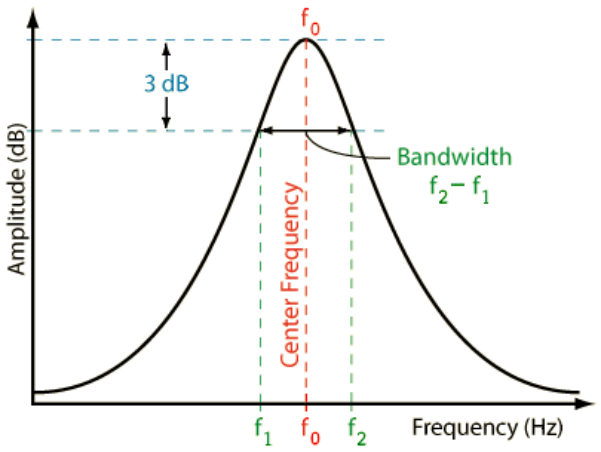


Figure 3.17. A typical Bell-shaped curve of the resonance with the resonant frequency at f_0. [122]

The frequencies f_1 and f_2 are the frequencies at which the power is half of the maximum at the resonant frequency (better known as 3-dB drop). The difference between the two, Δf, is called the half-power bandwidth. Quality factor (Q-factor) is one of the most important figures of merit when it comes to microwave resonators. It quantifies the energy storing capability of a given resonator and is defined as the ratio of maximum energy stored per cycle to the average energy dissipated in that cycle. [132]

$$Q = 2\pi \frac{maximum\ energy\ stored\ per\ cycle}{average\ energy\ dissipated\ per\ cycle} = \frac{\omega L}{R} = \frac{2\pi W}{PT} = \frac{\omega W}{P} \tag{3.5}$$

In Eq. 3.5, W is the stored electrical energy (at resonant frequency this is equal to the stored magnetic energy), P is the power dissipated in the resonator/cavity (V^2/R) and ω is the resonant angular frequency. It can be further shown that Q-factor is related to inverse of 3dB-bandwidth. [132] The centre frequency f_0 will be simply referred to as f from now on. In dielectric resonator system, the total loaded Q-factor (Q_L) is made up of four other Q-factors; conduction of metals (Q_π), radiation losses (Q_{rad}), and external losses due to the coupling antennas (Q_{ext}) where these terms are related via Eq. 3.6: [123,124,125]

$$\frac{1}{Q_L} = K\ tan\delta + \frac{1}{Q_{ext}} + \frac{1}{Q_{rad}} + \frac{1}{Q_\pi} \tag{3.6}$$

where K denotes the filling factor for a given geometry and $tan\delta$ is the inverse of Q-factor, better known as the loss tangent. It is used to quantify the energy dissipation in a given material. Both the quartz stand and the ceramic resonator are low-loss materials with $tan\delta$ of $6x10^{-5}$ and $2x10^{-5}$ at 10 GHz respectively. [126, 127]

$$tan\delta = \frac{1}{Q} \tag{3.7}$$

Similar to metallic cavities, ceramic resonators will have infinite number of resonant frequencies, arising from the constructive interference of the waves. In metallic cavities these modes are generally categorised according to their mode of operation. TE_{mnp}, TM_{mnp}, and HEM modes (transverse electric, transverse magnetic, and hybrid electromagnetic respectively) are the common widely used resonant modes. [128] Subscripts m, n, and p are used to present number of periodic halfwaves in the three directions of x, y, and z respectively. [129] In dielectric resonators however, the only available modes are the hybrid transverse modes of $T_{0,n+\gamma,p+\delta}$. Here the non-integer values of γ and δ are not zero at the radial and longitudinal dielectric-air interfaces respectively. In the transverse electric TE mode, there is no electric field in the direction of wave's propagation. This means that it only contains the azimuthal electric field component, hence the field is expected to remain continuous on interfaces of the resonator. [130] The $TE_{01\delta}$ mode is the lowest fundamental mode, that is well separated from its adjacent modes and any distortion of the field can be easily detected. This mode also has a high Q-factor associated with it and can also excite circular current in graphene. Here, the employed *VNA* essentially enables excitation of the $TE_{01\delta}$ mode in the puck. The microwave measurements in the present work employ the $TE_{01\delta}$ mode as the operation mode. Moreover, the metallic cavity enclosure minimises the radiative field from the resonator, hence it improves the Q-factor of the resonator. [131] The electric and magnetic fields' distributions for a $TE_{01\delta}$ resonant mode is shown in Figure 3.18.

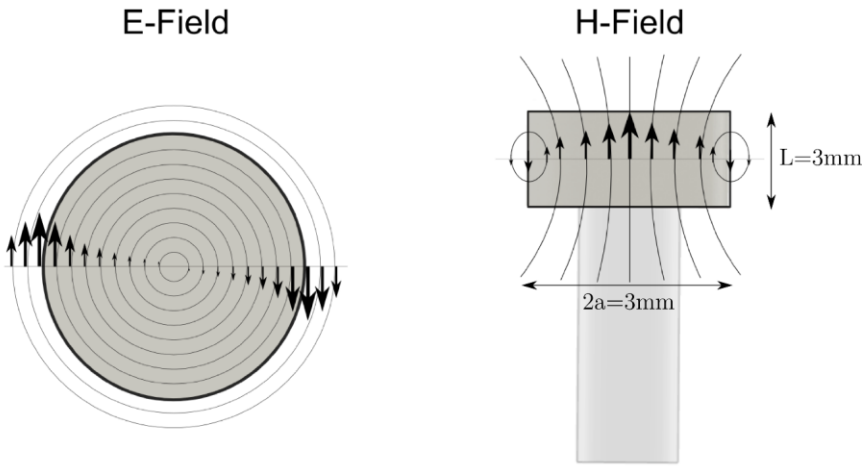


Figure 3.18. Distribution of *E*-field and *H*-field in a $TE_{01\delta}$ mode.

The dimensions of the isolated cylindrical ceramic resonator can be used according to Eq. 3.8 to roughly estimate the resonant frequency of its fundamental mode, $TE_{01\delta}$ in free space. [132] As shown in Figure 3.18 and mentioned previously, the puck used in this work has diameter of 7 mm and thickness of 3mm, which translates into $TE_{01\delta}$ resonant frequency of about 8.328 GHz. However, the measured f_r of the puck inside the copper cavity is observed to be slightly higher at 8.72 GHz. This is attributed to the difference between the true and the reported permittivity as well as the contribution from the metallic walls that lead to an increase in the observed resonant frequency and is not accounted for in the equation.

$$f_r = \frac{34(\frac{a}{L}+3.45)}{a\sqrt{\varepsilon_r}} \tag{3.8}$$

In order to measure the conductivity of a given material using this technique, the sample is first brought inside the evanescent field (non-radiative) of the resonator by being placed over the 5mm aperture. The disturbance of the field upon introduction of a given sample results in distortion of the resonant frequency as well as the *Q*-factor of the ceramic resonator. Perturbation theory is then used to calibrate readings and to subsequently calculate the sheet resistance of the sample.

3.2.3.2 Perturbation Theory

Perturbation theory is often used in conjunction with cavity resonators to investigate the electric as well as magnetic properties of a given dielectric material. [133] In this work, the perturbers are graphene coated samples. The placement of the samples over the aperture would result in perturbation of the evanescent field that is leaking through the aperture. The field is a non-radiative reactive field, therefore; variation in the dielectric constant gives rise to a perturbed field. This would result in shifting of both the resonant frequency and the Q-factor of the resonator depending on the nature of perturber. Figure 3.19 illustrates the shift in frequency due to the substrate (black to red). The substrate in this example is a bare high resistivity silicon (>1000 Ω.cm) with a thin layer (approximately 1 nm) of native silicon dioxide over the top. This shift of frequency will be further exploited for calibration of measurements.

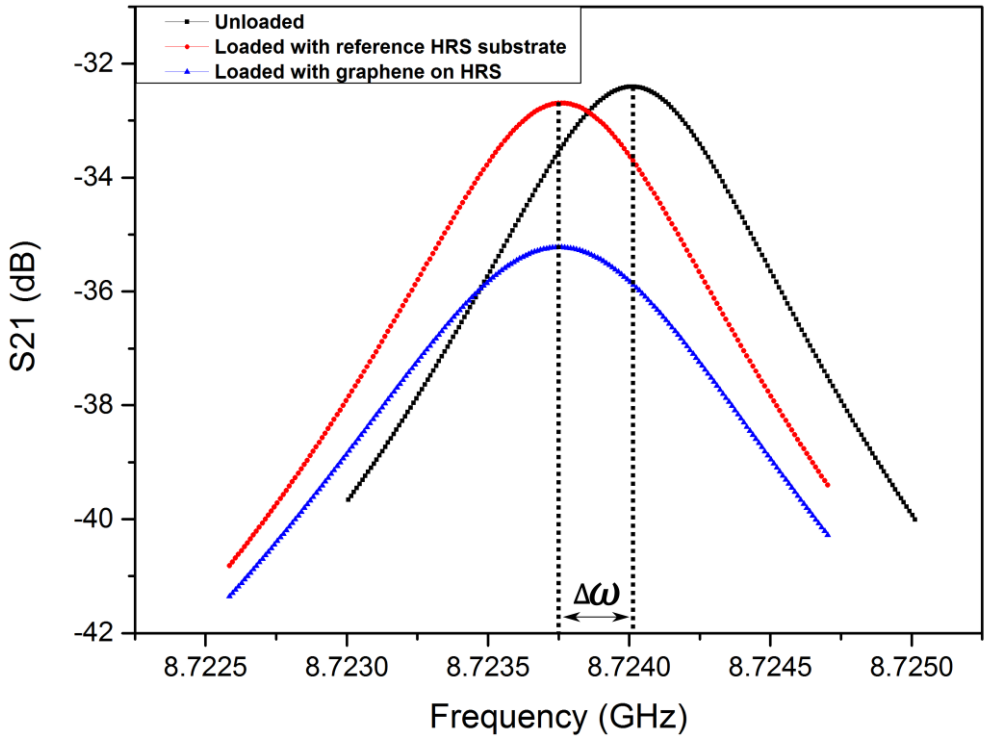


Figure 3.19. Perturbation of the field resulting in frequency shift and Q-factor reduction.

If the resonant frequency changes by $\Delta\omega$ upon introduction of the substrate, the electric and magnetic fields before and after perturbation can be taken into account

(E_1, E_2 and B_1, B_2 respectively) and by using the Maxwell's equations, this change can be related to the fields as well as the properties of the material under test: [133]

$$\frac{\Delta\omega}{\omega} = \frac{\iiint_{V_{perturber}}[(D_1E_2-E_1D_2)-(B_1H_2-H_1B_2)]dv}{\iiint_{V_{resonator}}(E_1D_2-H_1B_2)dv} \tag{3.9}$$

For a non-magnetic material, Eq. 3.9 becomes:

$$\frac{\Delta\omega}{\omega} = \frac{\iiint_{V_{perturber}}(D_1E_2-E_1D_2)dv}{\iiint_{V_{resonator}}(E_1D_2-H_1B_2)dv} \tag{3.10}$$

In both Eq. 3.9 and Eq. 3.10, D denotes the electric flux density (defined as the amount of charge per surface area (q/A)) and H denotes the magnetic field strength. These two parameters are governed by the permittivity and permeability of the medium respectively:

$$\vec{D} = \varepsilon\vec{E} \tag{3.11}$$

$$\vec{B} = \mu\vec{H} \tag{3.12}$$

Assuming the fields are constant within the thickness of the perturber, E and B will essentially be unchanged and Eq. 3.10 can then be simplified to: [133]

$$\frac{\Delta\omega}{\omega} = \frac{\varepsilon_0(1-\varepsilon'_r)\int_V {E_1}^2 dV}{4W} \tag{3.13}$$

Here ε_r' denotes the real part of sample's permittivity and W is the energy stored in the ceramic resonator. On the other hand, it is noticeable that replacing the bare substrate with one that is covered by graphene results in an apparent Q-factor drop but a negligible frequency drift. The imaginary part of the permittivity can be shown to be directly related to the change in Q-factor when the bare substrate (with Q_S) is replaced by a graphene covered substrate (with $Q_{Graphene}$):

$$\Delta(Q^{-1}) = \frac{1}{Q_{Graphene}} - \frac{1}{Q_S} = \frac{P_{graphene}}{\omega W}\frac{\varepsilon_0\varepsilon''_r\int_V {E_1}^2 dV}{2W} \tag{3.14}$$

In order to calculate the sheet resistance of graphene, the volume integral can be re-written in terms of areal integrals and thickness of graphene can be taken out. [134] It is assumed that the field is unchanged as the thickness of graphene (0.34 nm) is much smaller than its skin depth at microwave frequencies which is about 1.26 µm at the frequency of 10 GHz, assuming a realistic sheet resistance of 2000 Ω/□. Moreover, as the imaginary part of permittivity is related to the sheet conductivity by $\varepsilon''_r = \frac{\sigma}{\omega\varepsilon_0}$, Eq. 3.14 can be further simplified Eq. 3.15 taking into account that sheet resistance can be re-written in terms of conductivity and thickness ($R_s = \frac{1}{\sigma t}$):

$$\Delta(Q^{-1}) = \frac{P_{graphene}}{\omega W} = \frac{\sigma t \int_A {E_1}^2 dA}{(2\pi f)2W} = \frac{\int_A {E_1}^2 dA}{R_s(2\pi f)2W} = \frac{Z_C}{R_S} \tag{3.15}$$

where $P_{graphene}$ denotes the power dissipated in the graphene layer:

$$P_{graphene} = \frac{V^2}{R_S} = \frac{\int_A {E_1}^2 dA}{R_S} \tag{3.16}$$

The expression $\frac{\int_A E_1 dA}{2\omega W}$ is a constant and will be expressed as Z_C, better known as the characteristic impedance of the substrate. [135[The frequency shift due to graphene is negligible but the shift due to substrates is very important and will be taken into account in order to calculate the value of Z_C. Permittivity of the substrate will be used in combination with its thickness to obtain a numerical value for Z_C according to Eq. 3.17 and Eq. 3.18:

$$\frac{\Delta f_s}{f} = -\varepsilon_0(\varepsilon_s - 1)t_s Z_C \pi f \tag{3.17}$$

$$Z_C = -\frac{(\frac{\Delta f_s}{f})}{\varepsilon_0(\varepsilon_s - 1)t_s \pi f} \tag{3.18}$$

Simplifying Eq. 3.15 and rearranging the variables will result in Eq. 3.19 which will be employed to extract the sheet resistance of graphene:

$$R_S = \frac{Z_C}{\Delta(Q^{-1})} = \frac{Z_C}{\frac{1}{Q_{Graphene}} - \frac{1}{Q_S}} \tag{3.19}$$

Once the numerical value of Z_C is found, the substrates with graphene can be interested and the change in Q-factor will be monitored. Sheet resistance of graphene is then calculated according to Eq. 3.19.

As will be presented in 4.2, the values that are obtained from the microwave measurements in this work are in perfect agreement with those gathered from the DC measurements. This non-invasive method will not only be used to measure the sheet resistance of graphene samples, but also it will be employed to characterise the designed graphene based field effect transistors at microwave frequencies and to extract important transport parameters such as mobility, carrier concentration, scattering time, and modulation depth.

3.3 Summary and Conclusion

The main focus of this chapter was on describing the techniques that were utilised in order to characterise the fabricated graphene films and graphene based devices from morphology assessment of the films to the Hall-effect and electrical characterisation of the devices at both DC and microwave frequencies. It presented the development stages, as well as the working principles of the microwave resonance technique that incorporates a low-loss high Q-factor ceramic resonator. Theoretical concept of the method was explained and derivations of the important figures were demonstrated. The following two chapters will present the results of the optimised graphene growth and transfer procedures as well as the characterisation of various fabricated graphene based field effect devices.

4. Results and Discussion 1: Preparations and System Development

If you cannot measure it, you cannot improve it.

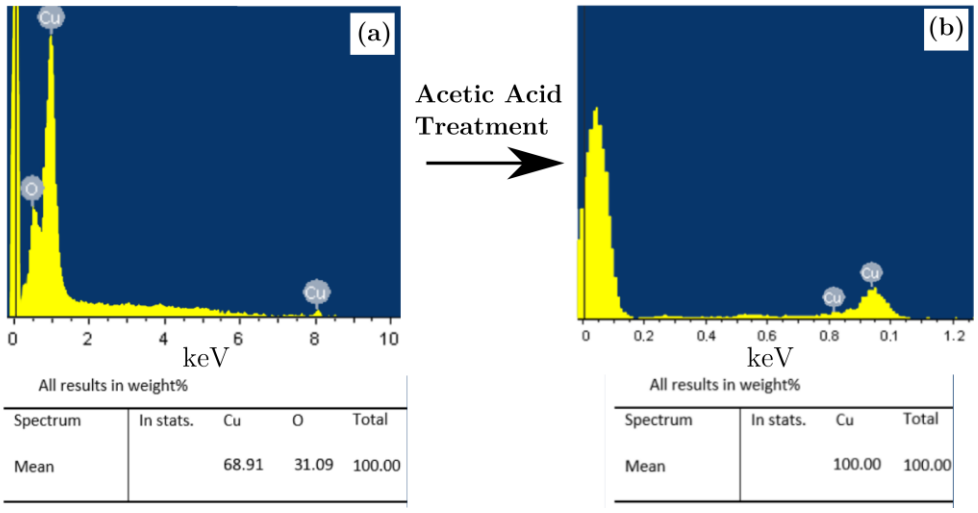
"Lord Kelvin"

The optimisation procedures of both the horizontal and the vertical CVD graphene production systems are presented in this chapter. The outcomes of the first attempts on growing graphene over thin films of copper by using a plasma enhanced vertical CVD system is discussed. Material selection for the gate dielectric of the fabrication of G-FET devices is considered and the step-by-step graphene transfer optimisation process is conferred. The chapter will conclude with demonstration of the system development for both the DC and the microwave field effect characterisation of the G-FET devices.

4.1 Copper Substrate Preparation

Chemical vapour deposition of a graphene layer on copper requires a highly clean growth atmosphere coupled with a uniform uncontaminated copper surface. All the growth attempts in this thesis utilised copper substrates. The surface of copper was only cleaned by acetic acid in order to remove the natural oxide on the surface (2.4.1.1). Acetic acid was chosen as an alternative to electropolishing which was not available. Water rinsing post acetic acid treatment was avoided as water exposure is known to result in formation of cupric hydroxide layer which can lead to a rougher surface profile. [136] It is important to avoid having a rough copper surface as it can promote heterogeneous nucleation, which would result in a higher density of nucleation sites and a raised amount of multilayer graphene coverage. [78] Therefore, samples are only nitrogen blow-dried after the acetic acid treatment. In

order to ensure full removal of the natural oxide layer on copper, EDX analysis was carried out prior to and after exposure of copper to acetic acid. The EDX profiles of copper substrate shown in Figure 4.1 reveal successful removal of the natural oxide.



All results in weight%

Spectrum	In stats.	Cu	O	Total
Mean		68.91	31.09	100.00

All results in weight%

Spectrum	In stats.	Cu	Total
Mean		100.00	100.00

Figure 4.1. The EDX spectra of the copper surface (a) prior to and (b) after acetic acid treatment.[1]

As discussed in 2.4.1.1, copper annealing is an essential part of reducing the surface roughness of copper. The AFM analysis shown in Figure 4.2 compares surface profile of copper foils with various treatments. Copper foil that has not been treated in anyways has a surface morphology that is shown in Figure 4.2a with a measured surface roughness of 62 nm (±1 nm). It is found that acetic acid treatment results in a slightly rougher surface with roughness value of 76 nm (Figure 4.2b). However, it is apparent that 60 minutes annealing under hydrogen atmosphere at 1050°C reduces the roughness value by more than 50% to about 20 nm as shown in Figure 4.2c. It is therefore significantly important to carry out the annealing step prior to the growth in order to ensure a smoother copper surface. The summary of the roughness values is presented in Table 4.1.

[1] In collaboration with Dr Stefan Goniszewski

Table 4.1. Surface roughness data for differently treated copper foils.

Copper Sample	As-received copper with no treatment	Treated in Acetic Acid for 45minutes	60min annealed at 1050°C
Roughness Ra (nm)	62.3	76.5	20.4

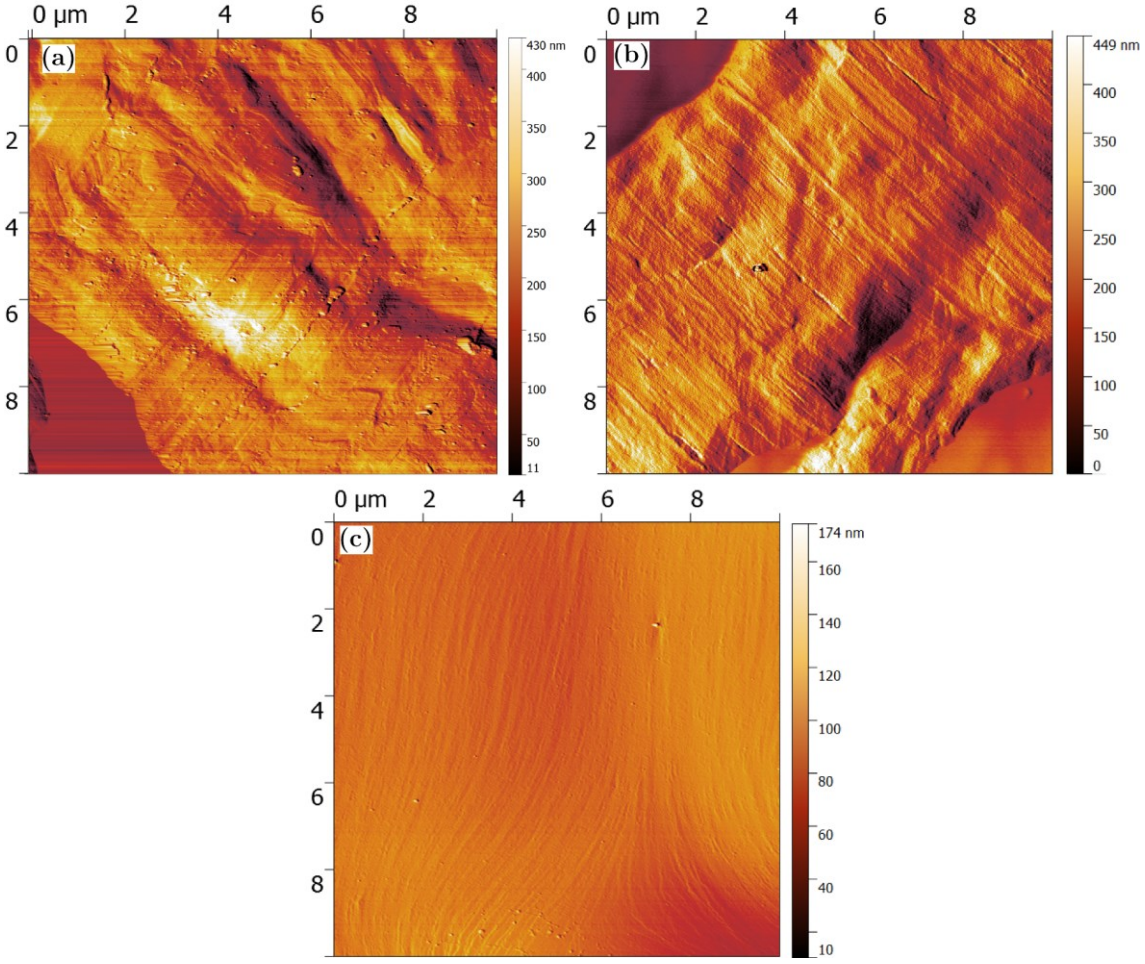


Figure 4.2. Surface roughness maps of copper foils upon different treatments carried out via the Atomic Force Microscopy. (a) Untreated as-received plain copper, (b) Acetic Acid treated copper and (c) annealed copper for 60 minutes under hydrogen atmosphere.

Furthermore, EBSD analysis was performed to investigate the effect of annealing on copper grain size. The untreated copper foil was found to be very difficult for this type of analysis due to its high surface roughness. As a result, the measured data points are found to be very scattered as presented in Figure 4.3. However, EBSD data for the 60 minutes annealed copper foil revealed an average grain diameter of 5 µm. As it can be seen from the pole-figures in Figure 4.4, the annealed copper exhibits a highly oriented microstructure with planes aligning along the

(100) facets with a slight misorrientation. The coloured map coupled with the pole figures are indicative of a very small misorrientation between the grains as most of the points are very localised as opposed to the previous analysis on untreated copper foil.

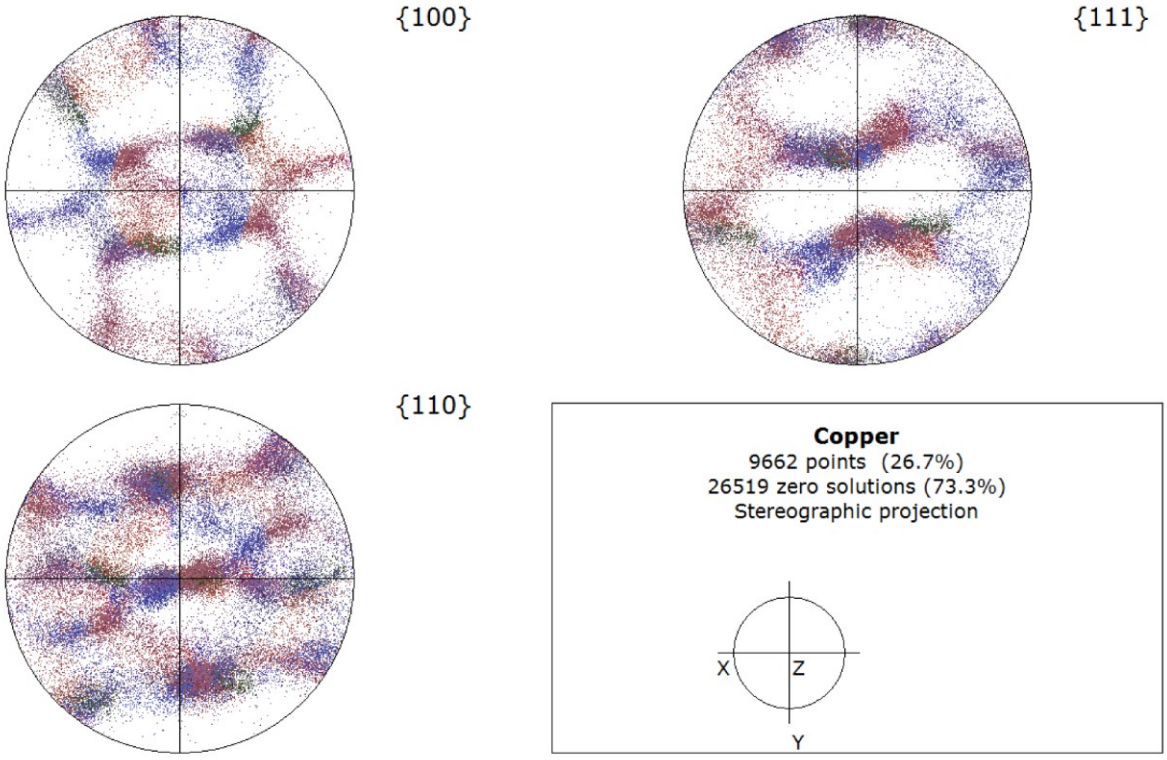


Figure 4.3. Stereographic projection of the untreated copper foil obtained by the EBSD analysis. It is only representing 26.7% of the scanned area as the rest was found to yield no solutions due to the high roughness of the surface.

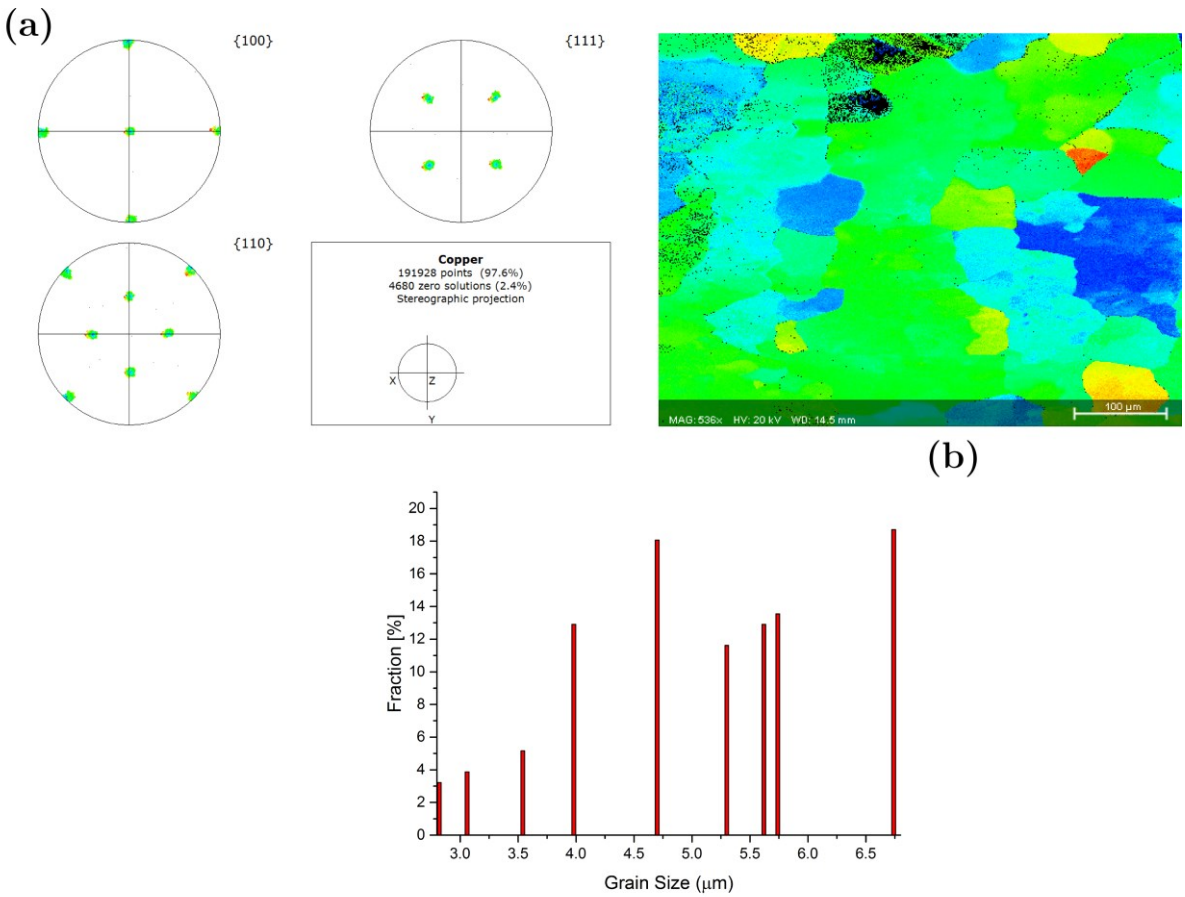


Figure 4.4. (a) The Pole figures and the grain distribution of copper after 60 min annealing performed via the EBSD analysis with a slight misorrientation present. (b) The calculated grain size fractions across the scanned area.

In order to finalise the comparison between the copper foils, X-ray diffraction patterns of the sample were obtained. As demonstrated in Figure 4.5, and as anticipated, the results are in perfect agreement with the previously performed EBSD analysis. The grains in copper have evolved from both (111) and (220) facets to (200) facets upon annealing. This is apparent from the much sharper peak at 2θ of 50.4° after annealing (black spectrum). It is important to note that copper foil annealing plays a crucial role in reducing the nucleation sites and areas that have a low activation energy associated with them. This is important as it allows for mitigation of growing multi-layer graphene films.

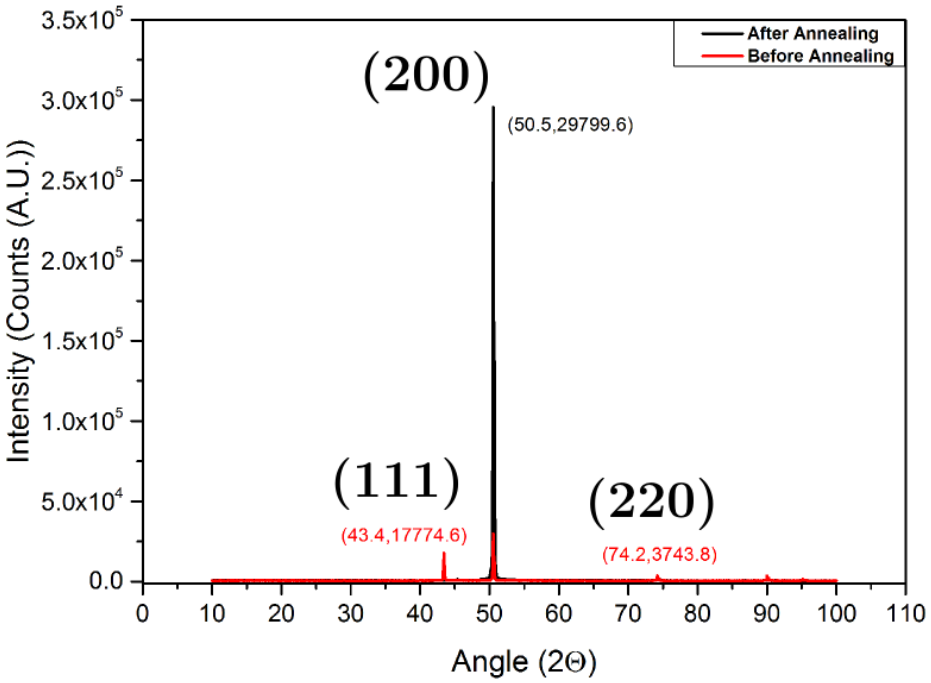


Figure 4.5. XRD spectrum of the used copper foil for graphene growth before and after annealing.

4.2 Horizontal CVD Graphene Fabrication

Figure 4.6 demonstrates the schematics of the horizontal CVD equipment that was initially used to grow single layer graphene films on copper foils. Precursor gases are fed from one end of the horizontally arranged quartz tube, where copper foil is located at the centre. The other end of the tube is connected to a primary rotary pump that takes the assembly to a base pressure of 2×10^{-2} mbar. A high temperature single-zone furnace covers 70% of the quartz tube and leaves the two ends uncovered. In order to optimise the growth procedure for obtaining monolayer graphene films, more than 80 samples with 35 different recipes were prepared. Parameters such as growth temperature, pressure, annealing conditions, gas flow ratios, cooling rate, and copper purity were tuned. (Recipe details are available in appendix 7.1)

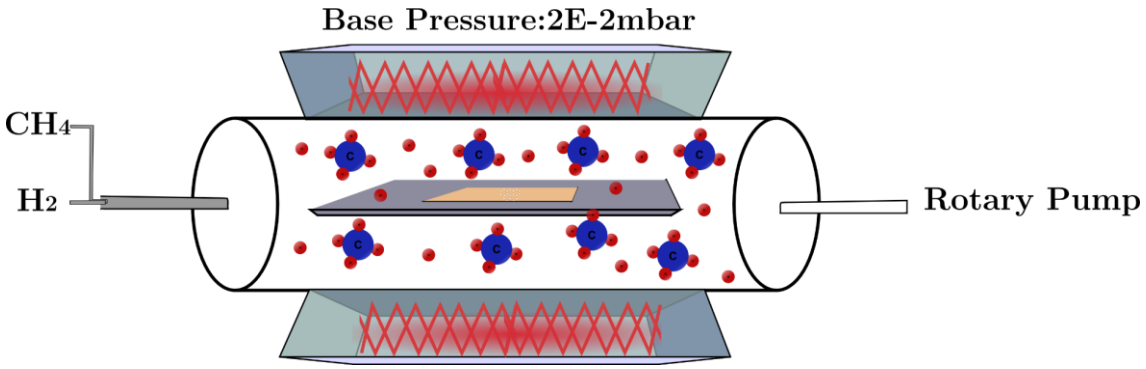


Figure 4.6. Schematics of the horizontal CVD system that was initially used to fabricate single-layer graphene films.

It is important to note that there are two sources of hydrogen present during the growth process; hydrogen that comes from a hydrogen generator and is used as the main hydrogen source while the second source stems from the hydrogen released when methane molecules dissociate above the copper surface. Excess of hydrogen present in the chamber can potentially lead to a reverse reaction, where carbon atoms from methane dehydrogenation would react with hydrogen and result in methane molecules. This effectively means that the as-grown graphene islands would be etched from the surface of copper. Figure 4.7 indicates that in the absence of the carbon precursor gas, a high portion of a graphene film can be etched away in the temperature regime of 700-1000°C. The CH_4 flow is therefore essential to be retained during the cooling step in order to prevent any potential oxidation at such high temperatures. Therefore, fast-cooling of the chamber to around 300°C was carried out to avoid hydrogen etching issues. The rate of fast cooling versus that of slow cooling is presented in Figure 4.8. It is noticeable that reaching 700°C by fast cooling is about 24 times quicker compared to slow cooling.

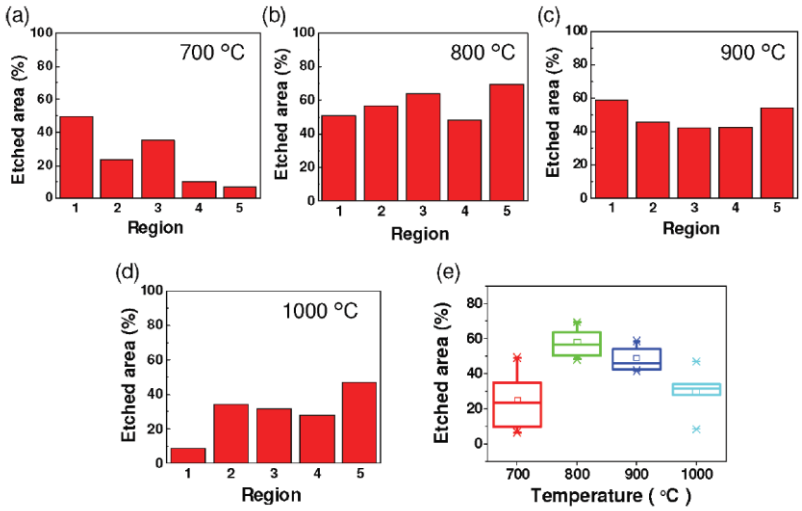


Figure 4.7. The proportion of the total etched area of graphene from 700°C to 1000°C (a-d) and under 30 sccm of H_2 flow. [137]

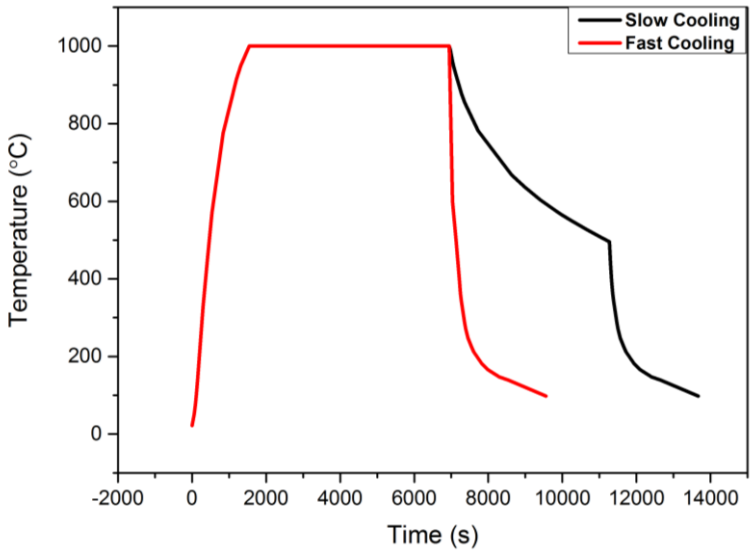


Figure 4.8. Comparison between the fast and the slow cooling rates of samples after heating to 1000°C, and the subsequent annealing and growth at 1000°C.

A number of existing recipes (recipes 1-10) were attempted until continuous graphene layer was successfully grown. The existing knowledge in the literature (described in 2.4.1) was utilised in order to reduce the number of multilayer islands and to eventually achieve a graphene film of a high single-layer coverage. The pattern of attaining a continuous monolayer film is presented in Figure 4.9 below. The covered areas in Figure 4.9a-b are highlighted in green.

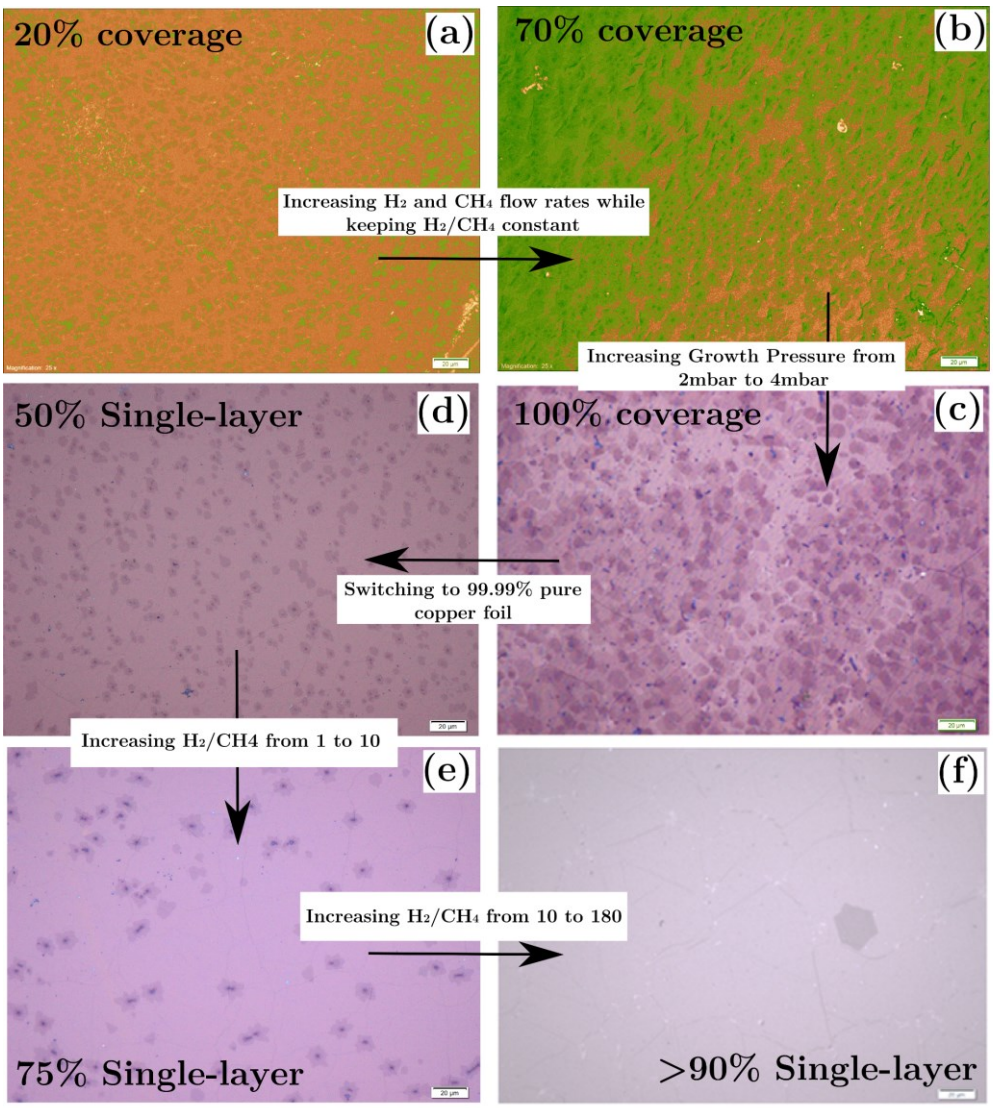


Figure 4.9. The optical micrographs presenting the evolvement of single layer CVD graphene growth optimisation procedure; (a) only a 20% coverage achieved by the initial recipe (recipe 1). (b) 70% coverage is achieved upon increasing flow rate of hydrogen and methane gas (recipe 6). (c). 100% coverage with many multilayer graphene as a result of increasing growth pressure (recipe 10). (d) Reduction of multilayer graphene by switching to a purer copper foil and repeating the recipe in (c) (recipe 25). (e) Reducing the number of double layers by increasing the H_2/CH_4 ratio (recipe 28). (f) Achieving more than 90% single-layer graphene coverage by increasing the H_2/CH_4 to 180 (recipe 35). (All scale bars are 20 µm).

As shown in Figure 4.9, the first chosen recipe did not result in a full graphene coverage. In fact, recipe 1 only yielded 20% graphene coverage. This value improved to about 70% by increasing the flow rate of methane and hydrogen from 8 sccm and 6 sccm to 40 sccm and 30 sccm respectively during the growth stage (recipe 6). A coverage of 100% was eventually achieved (recipe 10) at an increased pressure of

4 mbar and 40 sccm to 30 sccm of hydrogen to methane gas flow rates. As shown in both the optical image and the Raman spectrum in Figure 4.10, graphene that was grown over the used copper substrate incorporates a large number of multilayer areas. It is reflected in the blue-shift of the G-peak from 1589 cm^{-1} as well as a mean average value of 2D/G ratio of below 1 (as described in 3.1.3). The SEM micrograph where there is a clear contrast in the colour between the different layers further validates the mentioned results.

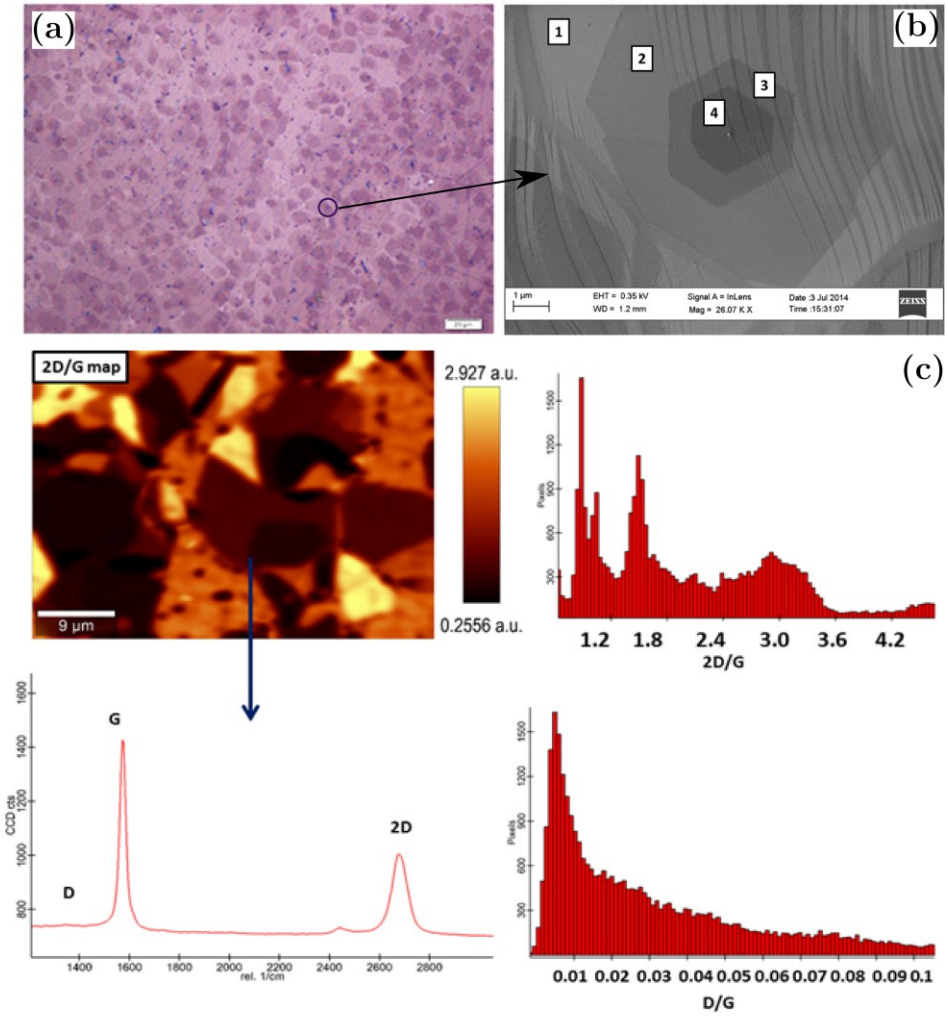


Figure 4.10. Characterisation of the graphene film that was grown via recipe 10, using a 95% pure copper foil. (a) The optical image showing a number of different contrasts arising from having different number of layers (scale bar 20 µm). It agrees well with (b) the SEM micrograph of a small region of the sample clearly displaying one of the nucleation sites and the different number of graphene layers adjacent to it. (c) Raman map, spectrum, distribution of the 2D/G as well as the D/G peak over the large scanned area (40x40 $µm^2$) indicating the multilayer nature of the grown graphene.

The other crucial factors such as growth pressure, annealing time, and gas ratios were later tuned but no success was seen in reducing the density of multilayer graphene, until recipe 25. In recipe 25 the 95% pure copper foil was changed to one with 99.95% purity. Upon this change, the subsequent grown graphene films were significantly different. Figure 4.11a illustrates the optical image of the sample grown under the same condition as recipe 10 (Figure 4.9b).

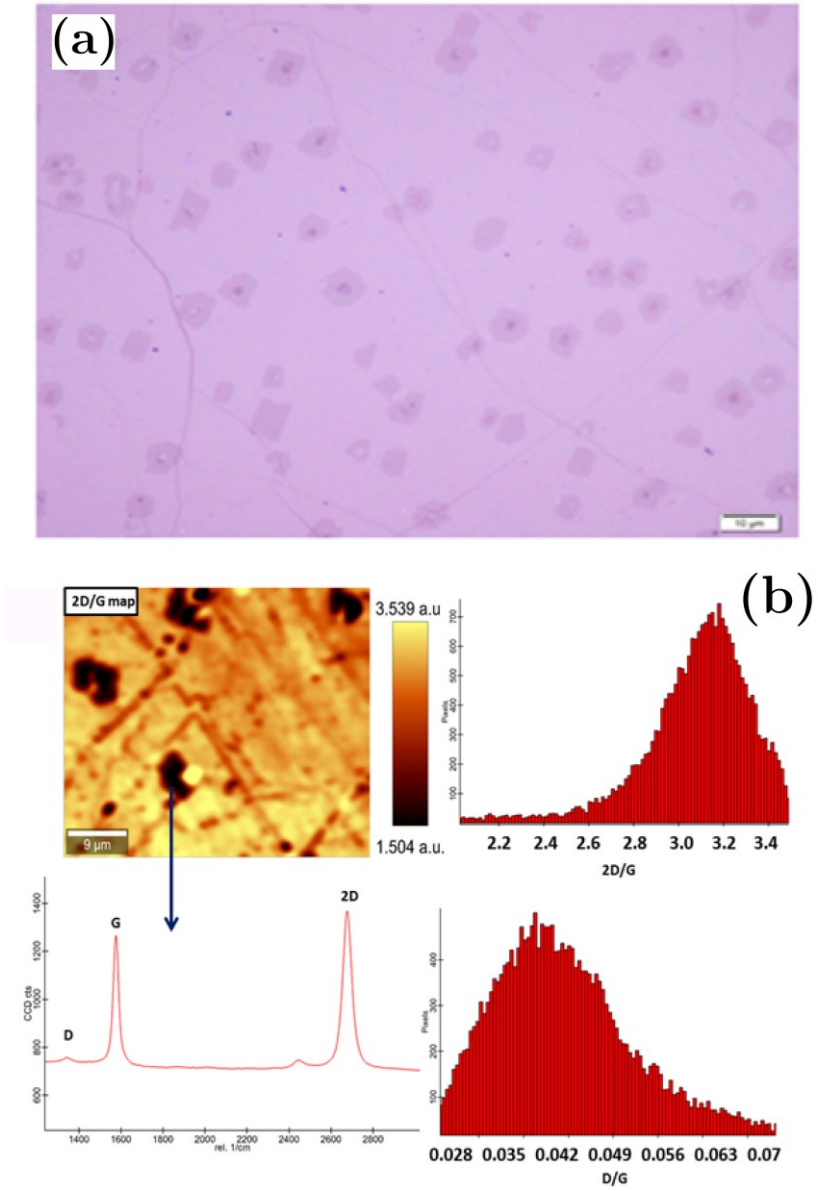


Figure 4.11. (a) The optical image and (b) Raman analysis of the graphene grown via recipe 10, using 99.99% pure copper foil.

It is apparent that the degree of multilayer coverage is dramatically reduced. This observation is further confirmed by the Raman analysis that was performed on the sample as shown in Figure 4.11b. It is noticeable that the 2D/G ratio now has an increased mean value of above 2 over the entire scanned area. However, the islands of double-layer/multilayer nature still exist in great numbers (the darker spots in both optical and Raman map). The fact that a lower purity copper foil had a large number of multilayer graphene areas associated with it can be attributed to the quantity of available heterogeneous nucleation sites during the growth step. The copper foil with a higher amount of impurities exhibits a higher density of areas/points with a lower activation energy, which can act as favourable sites for nucleation of graphene islands.

By considering the vast amount of work that had been done to enhance quality of single-layer CVD grown graphene films (section 2.2.1), optimization of this horizontal system then followed the work of Yan et al. who suggested that increasing the growth pressure in combination with a higher H_2/CH_4 ratio would yield larger domains of single layer graphene. [78] As the recipes evolved, the growth pressure of 130 mbar coupled with a high H_2/CH_4 ratio (180) at 1035°C growth temperature followed by fast-cooling of the sample resulted in graphene films with over 90% single-layer coverage. Annealing conditions were kept constant at 200 mbar, 30 min, and 100 sccm of H_2 flow at 1035°C. The optical image of the sample under the explained condition is presented in Figure 4.12a. The Raman spectrum, the 2D/G (mean value of 2.35) as well as the D/G ratio distribution (mean value of 0.03) presented in Figure 4.12b all confirm the monolayer nature of the obtained graphene film with minimal amount of structural disorder.

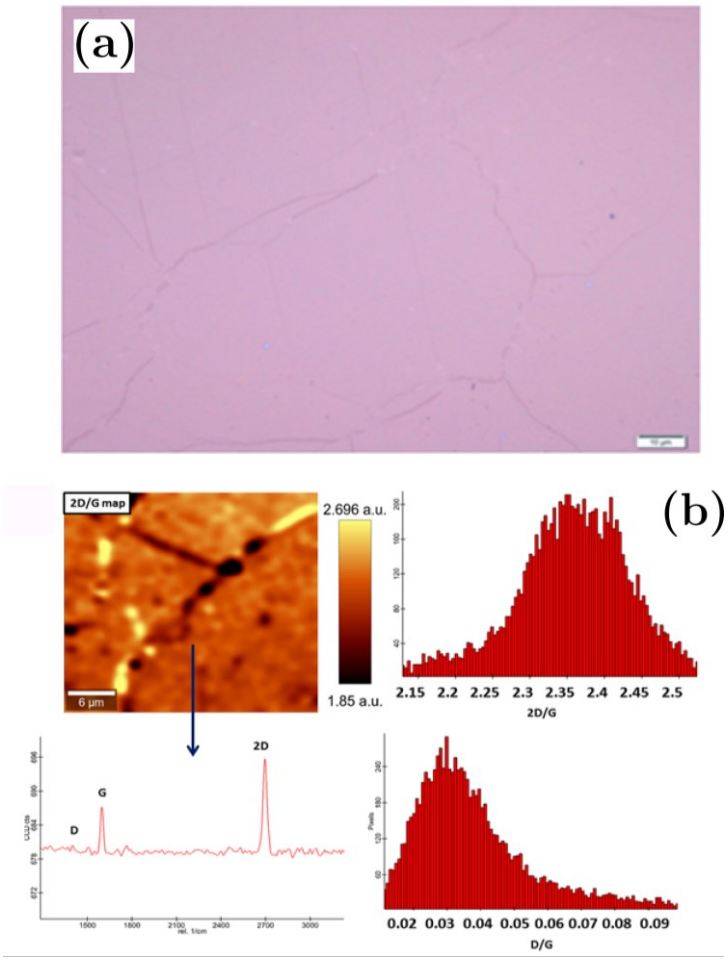


Figure 4.12. (a) The optical image and (b) Raman analysis of graphene grown under the optimised growth condition at high pressure and H_2/CH_4 ratio of 180.

4.3 PVD-CVD Cluster Deposition System

Advances in wafer-scale graphene synthesis and the high demand for CVD grown graphene in the Materials Department of Imperial College London, resulted in a collaboration between the university and the manufacturing industry to deliver a 4-inch wafer-scale single/Multi-layer graphene production system. In collaboration with VG-Scienta (UK) [138] and planarTECH (US) [139], a cluster Physical Vapour Deposition (PVD) module for thermal evaporation of copper coupled with a vertical CVD graphene synthesis module interconnected via a load-lock was designed, tested and then installed in the Materials Department in January 2015. Each module is controlled by a separate computer while the two computers work together to control

interlocks for avoiding inter-chamber accidents. A photograph and a schematics view of the entire cluster deposition system are presented in Figure 4.13.

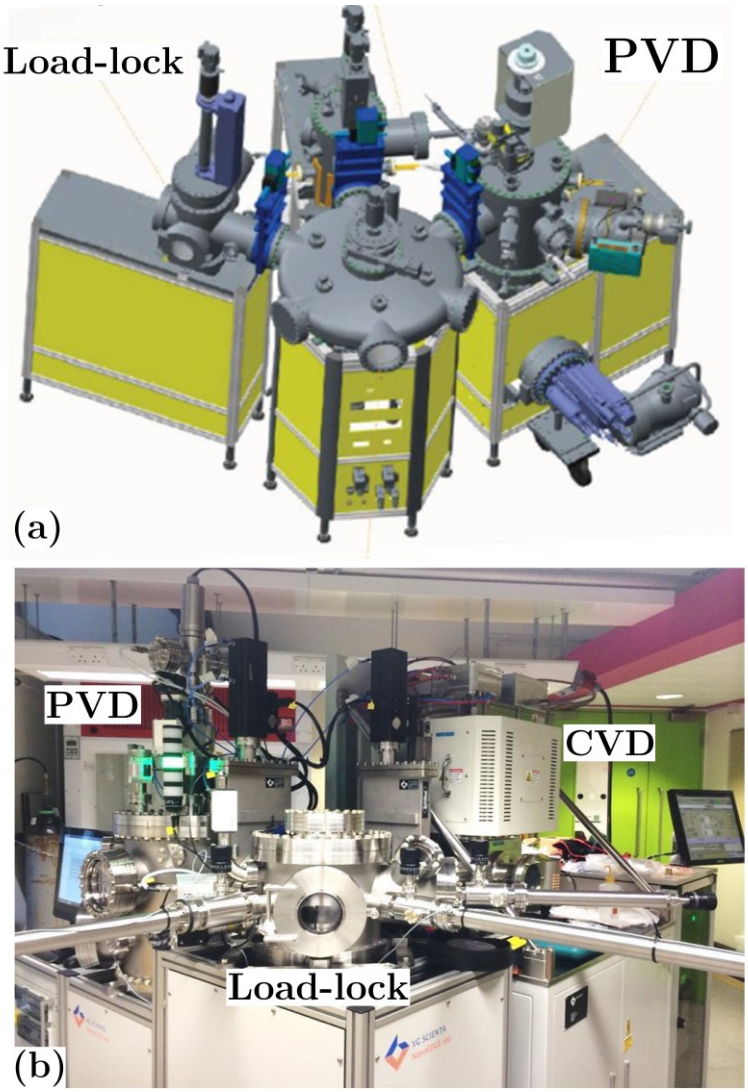


Figure 4.13. (a) The schematics and (b) a photograph of the cluster PVD-CVD graphene deposition system.

The PVD module that is apparent on the left hand side of Figure 4.13b has a base pressure of 8×10^{-9} mbar and can be heated to 1000°C. It is equipped with two thermal evaporation sources that are employed to produce copper thin films on a given substrate. The purpose of having a PVD module attached to a graphene CVD production unit is pursuing a wafer scale uniform single-layer graphene growth over epitaxially grown single crystal copper thin films without the need to break the vacuum or require to clean backside of copper in between the processes. The high vacuum level of the chambers is required to have a clean working atmosphere and

to avoid potential copper oxide formation. A load-lock is present in-between the PVD and the CVD chambers with the purpose of keeping both mentioned chambers at a high vacuum level at all times. Therefore, samples are first placed in the load-lock before entering any of the other two chambers. It is important to note that the CVD system has a designated *RF* plasma generating unit incorporated at its top that is capable of generating plasma with up to 600 W of power. It is located next to the gas shower head and is designed and implemented to assist and enable graphene growth over thin films of copper at a lowered growth temperature.

4.3.1 Vertical Chamber CVD Graphene Fabrication

The vertical CVD module is one of the core elements of the cluster PVD-CVD deposition equipment. This CVD system possesses many advantages over the previously used horizontal assembly. It has a base pressure of 4×10^{-8} mbar resulting in a highly clean atmosphere. The growth process is fully automated to achieve consistent and reproducible graphene films. The internal pressure is also automatically controlled and adjusted via a very accurate ($\pm$0.01 Pa) APC (automatic pressure control) system that regulates movement of a throttle valve to attain the desired working pressure in the chamber. Furthermore, stage over which the sample lies on can be rotated to mimic physical vapor deposition systems where more homogeneous films can be achieved simply due to the rotation of the stage. The gases are also mixed before entering the chamber through a shower head as shown in Figure 4.14. The adjustable parameters, their maximum range, as well as the control unit setup of the CVD module are presented in Figure 4.15.

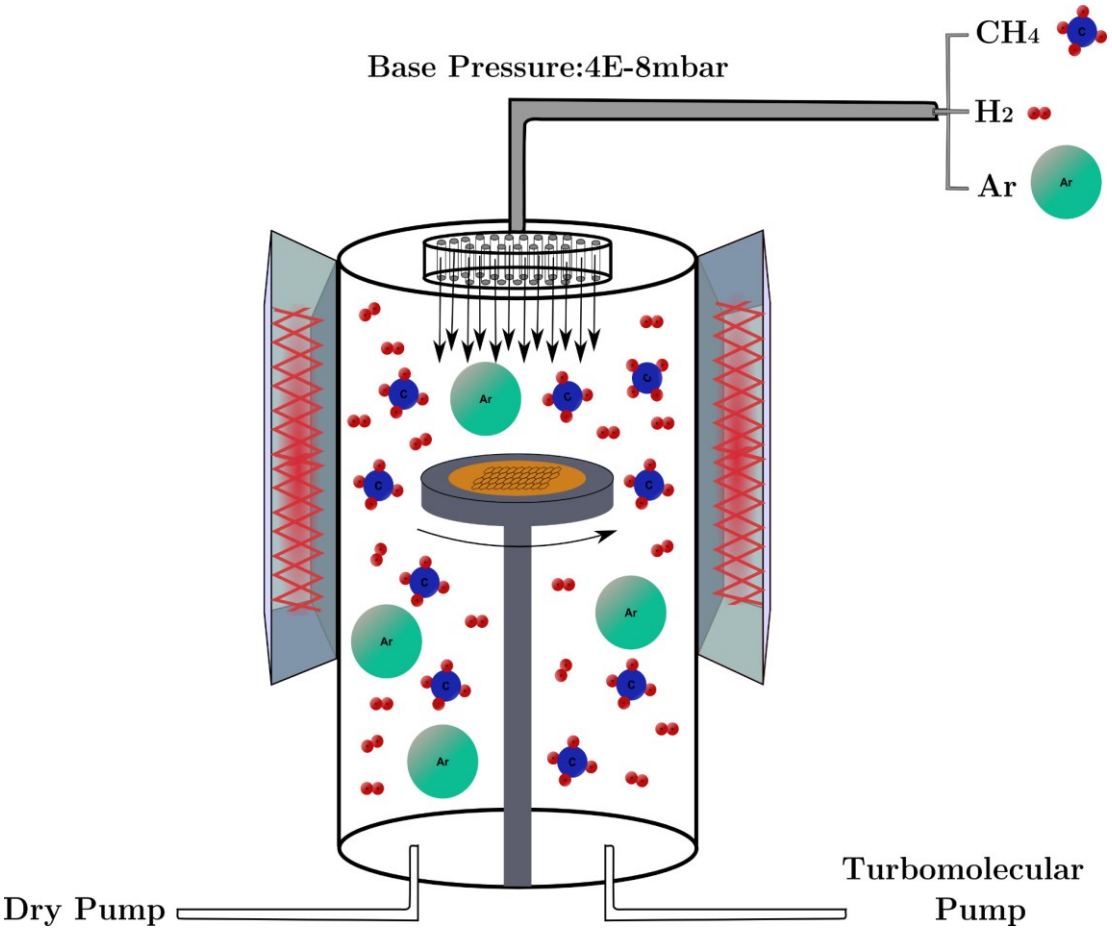
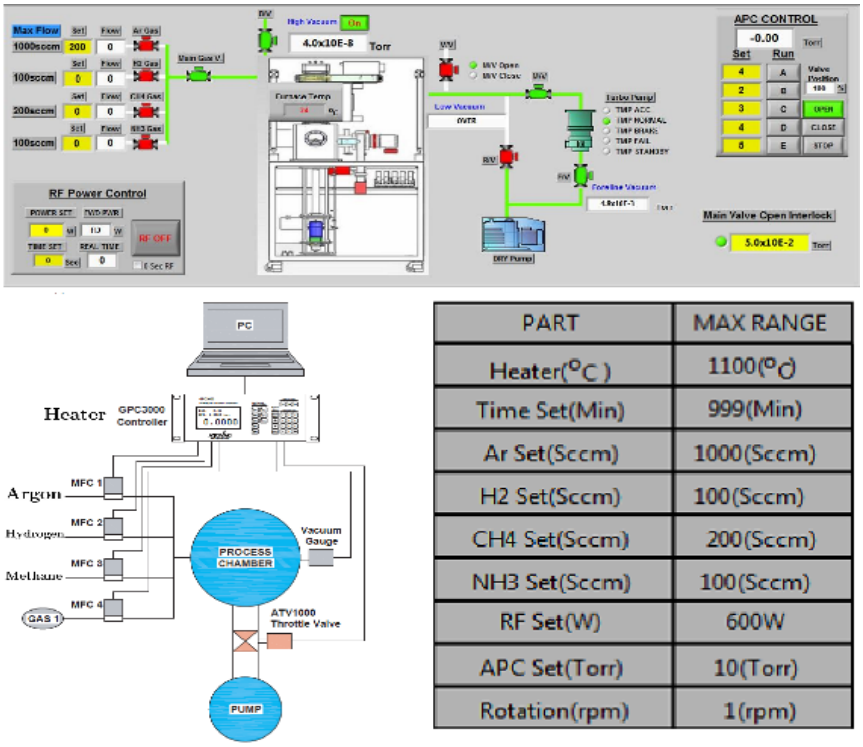


Figure 4.14. Vertical CVD graphene growth system, as part of the PVD-CVD cluster deposition equipment. [189]



PART	MAX RANGE
Heater(°C)	1100(°C)
Time Set(Min)	999(Min)
Ar Set(Sccm)	1000(Sccm)
H2 Set(Sccm)	100(Sccm)
CH4 Set(Sccm)	200(Sccm)
NH3 Set(Sccm)	100(Sccm)
RF Set(W)	600W
APC Set(Torr)	10(Torr)
Rotation(rpm)	1(rpm)

Figure 4.15. Vertical CVD control unit showing full automatization of the process.

The optimisation of the horizontal CVD single layer graphene growth system resulted in a more straightforward optimisation procedure for the vertical growth unit. Figure 4.16 shows the optical image of the first graphene sample produced by this system. It was grown via the recommended recipe of the cluster deposition system manufacturers, performed at a pressure of 5 Torr and a H_2/CH_4 ratio of 0.11 for 30 minutes. [138]

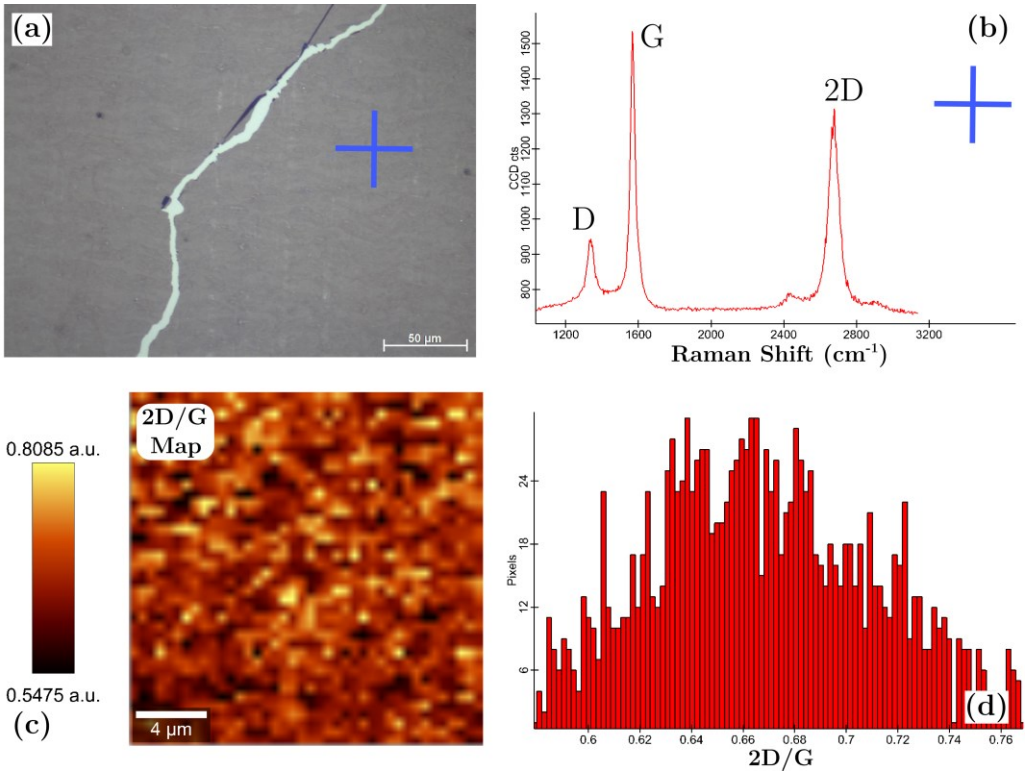


Figure 4.16. (a) An optical image and (b) the Raman spectrum, (c) the 2D/G map, and (d) the distribution of 2D/G over the scanned area of the grown graphene layer via recipe 1.[2]

What initially was suspected to be a full coverage of single-layer graphene from the optical images, was then shown to be a multilayer graphene film via Raman spectroscopy. This is apparent from the sharp G-peak in the Raman spectrum and the 2D/G map over the scanned area with a mean value of less than 1, presented in Figure 4.16b-d respectively. Moreover, AFM measurement was carried out as shown in Figure 4.17 and the thickness of the film was measured. It was found to

[2] In collaboration with Dr P. Sherrell at Imperial College

be approximately 40 nm. Combining the obtained results to the AFM work done on CVD graphene by Jung et al. [106], the measured AFM thickness of 40 nm would translate to about 20 layers of graphene.

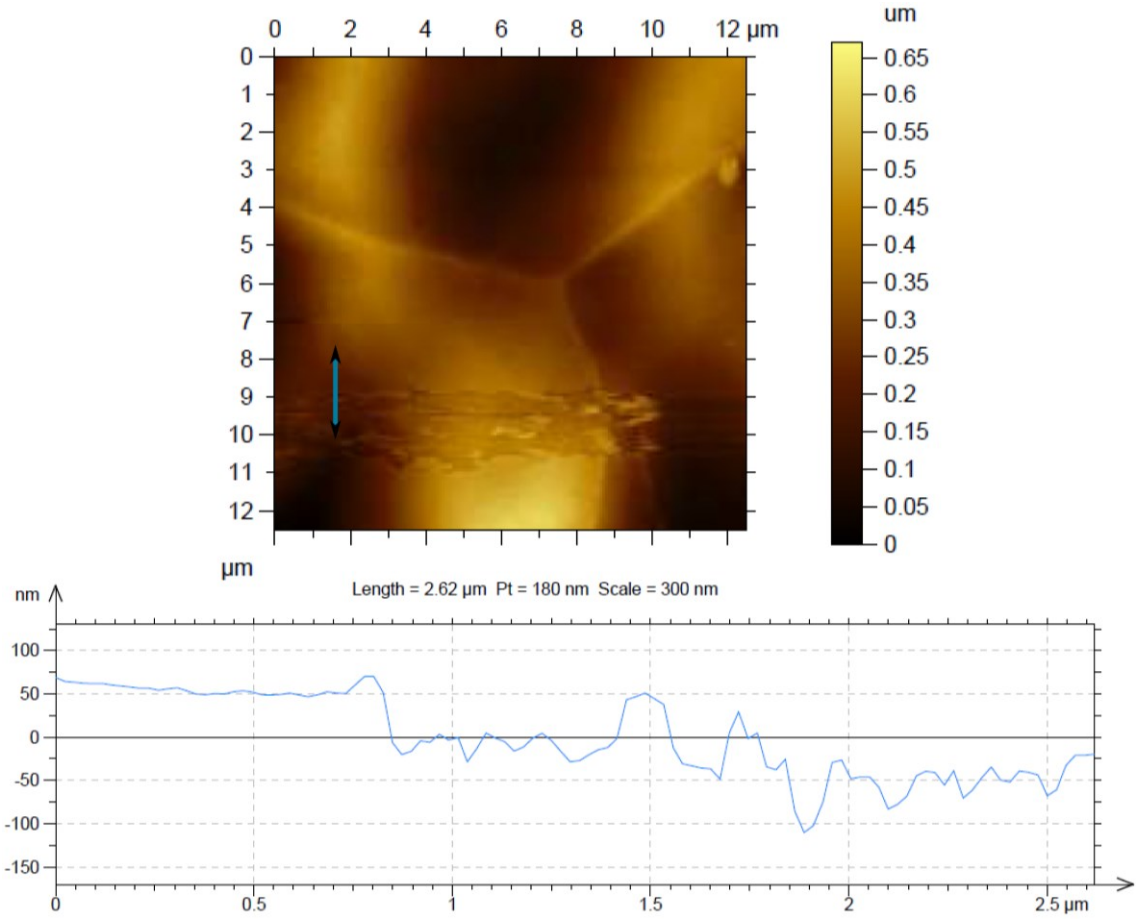


Figure 4.17. The AFM analysis on the graphene grown via recipe 1, indicating thickness of about 40 nm. [3]

Using this recipe as the benchmark and utilising the previous optimisation experience from the horizontal CVD system, full coverage of single-layer graphene with minimised multilayer islands was achieved upon only 15 recipes, all grown at a set temperature of 1050°C. The optimisation process progressed by maintaining the growth pressure at 5 Torr and gradually increasing H_2/CH_4 ratio. As can be seen in the Raman analysis of the grown and transferred graphene samples in Figure 4.18, increasing H_2/CH_4 ratio from 0.11 in the first sample gradually up to

[3] In collaboration with Dr P. Sherrell at Imperial College

16 resulted in a more prominent 2D peak as well as weakening of the D peak signal, indicating presence of a more crystalline graphene layer with lowered multilayer regions. Double and triple layer nucleation sites are apparent in both the optical and the Raman spectrum of the sample grown under H_2/CH_4 ratio shown in Figure 4.18c.

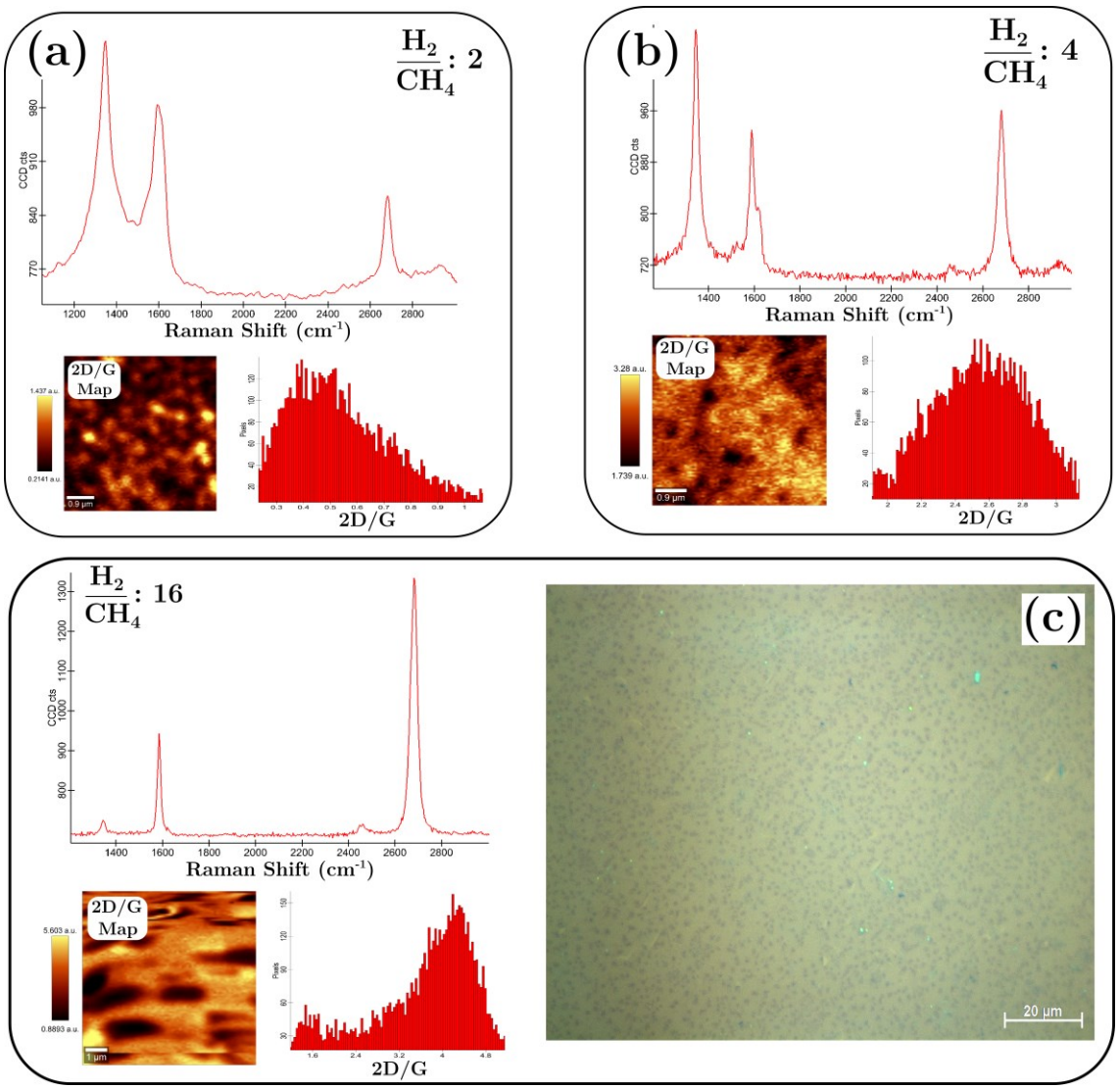


Figure 4.18. Raman analysis of the graphene sample that were grown by increasing hydrogen to methane gas ratio of (a) 2, (b) 4, and (c) 16 with the associated optical image where small black regions represent the multilayer graphene regions.

However, further increase of the ratio to 32 did not result in single layer graphene and as shown in Figure 4.19 by the Raman analysis in had an amorphous carbon

structure associated with it with a relatively large D peak indicating a large degree of disorder present in the structure.

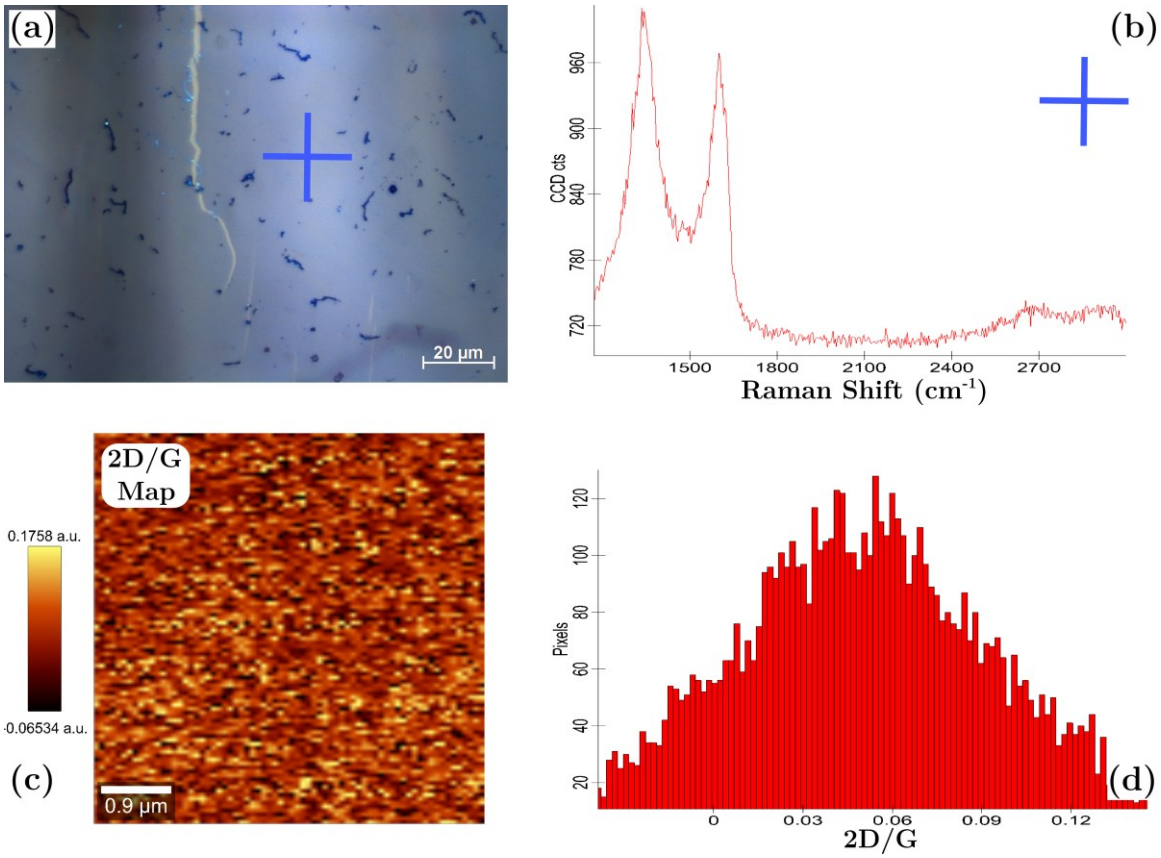


Figure 4.19. Characterisation of the graphene sample grown at a pressure of 5 Torr under hydrogen to methane gas ratio of 32. (a) The optical image, (b) the characteristic Raman spectrum of the sample, (c) the 2D/G mapping of the scanned area and (d) the 2D/G distribution over the scanned area all indicating towards the amorphous nature of the grown film.

Upon carrying out further experiments and different growth recipes, predominantly single-layer graphene film with full coverage over the copper substrate was obtained at a lowered growth pressure of 2 Torr and a H_2/CH_4 ratio of 32. It can be seen from the optical image, the 2D/G Raman map, as well as the relatively weak D peak of the sample presented in Figure 4.20 that the obtained profile is in perfect agreement with that of single-layer CVD graphene shown by other research groups. [103]

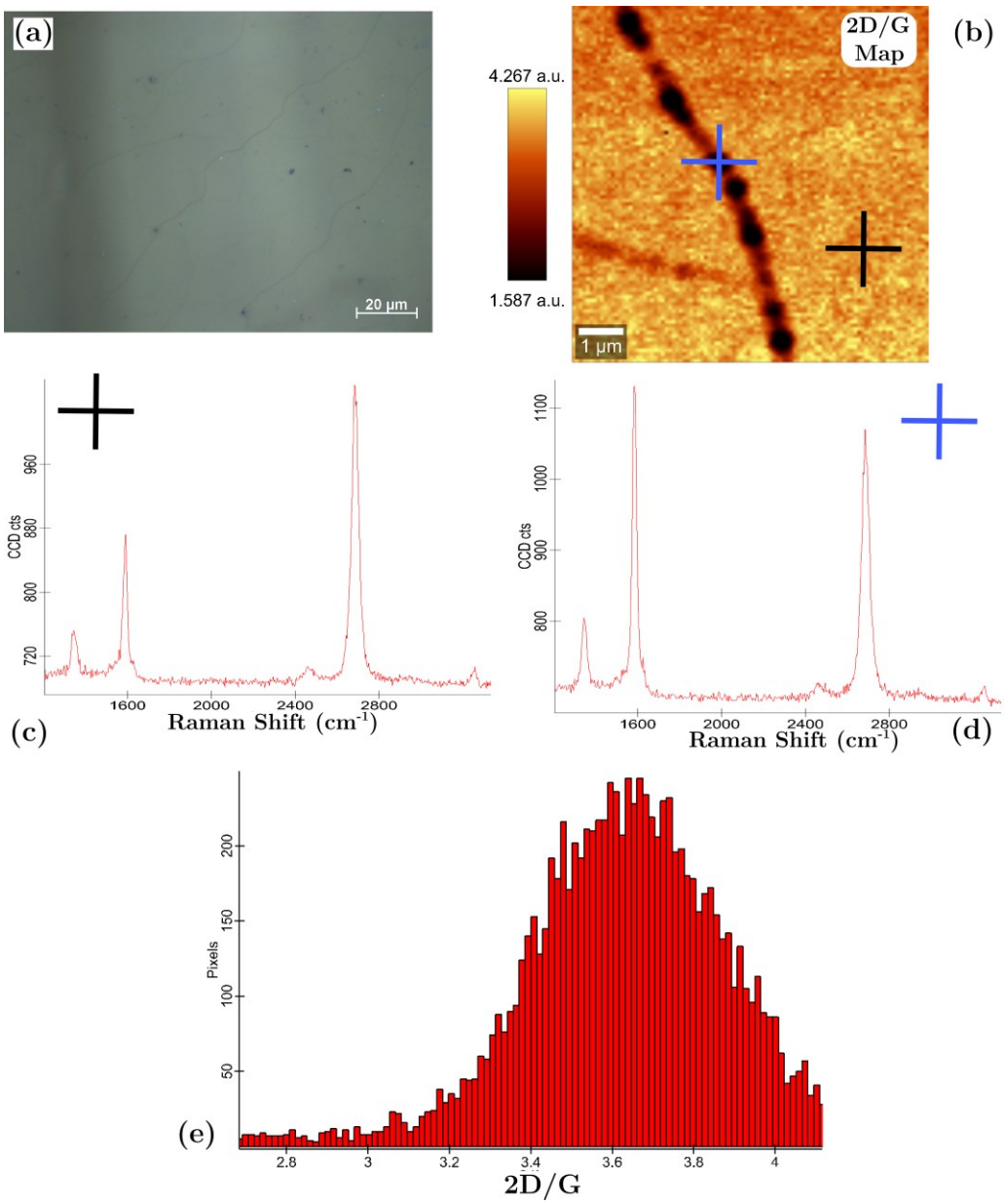


Figure 4.20. (a) Optical image and (b-e) Raman characterisation of the dominantly single-layer graphene sample grown under the optimised condition of 2 Torr growth pressure and hydrogen to methane gas ratio of 32.

The Raman spectrum in Figure 4.20d points towards presence of more than one layer of graphene. This can be attributed to the folding of the transferred graphene that had occurred post-transfer process as a result of evaporation of the trapped water between graphene and substrate. Growth of the graphene film under the optimised condition have shown to be reproducible as shown by the optical and Raman characterisation in Figure 4.21 for another transferred graphene sample grown at a repeated growth condition.

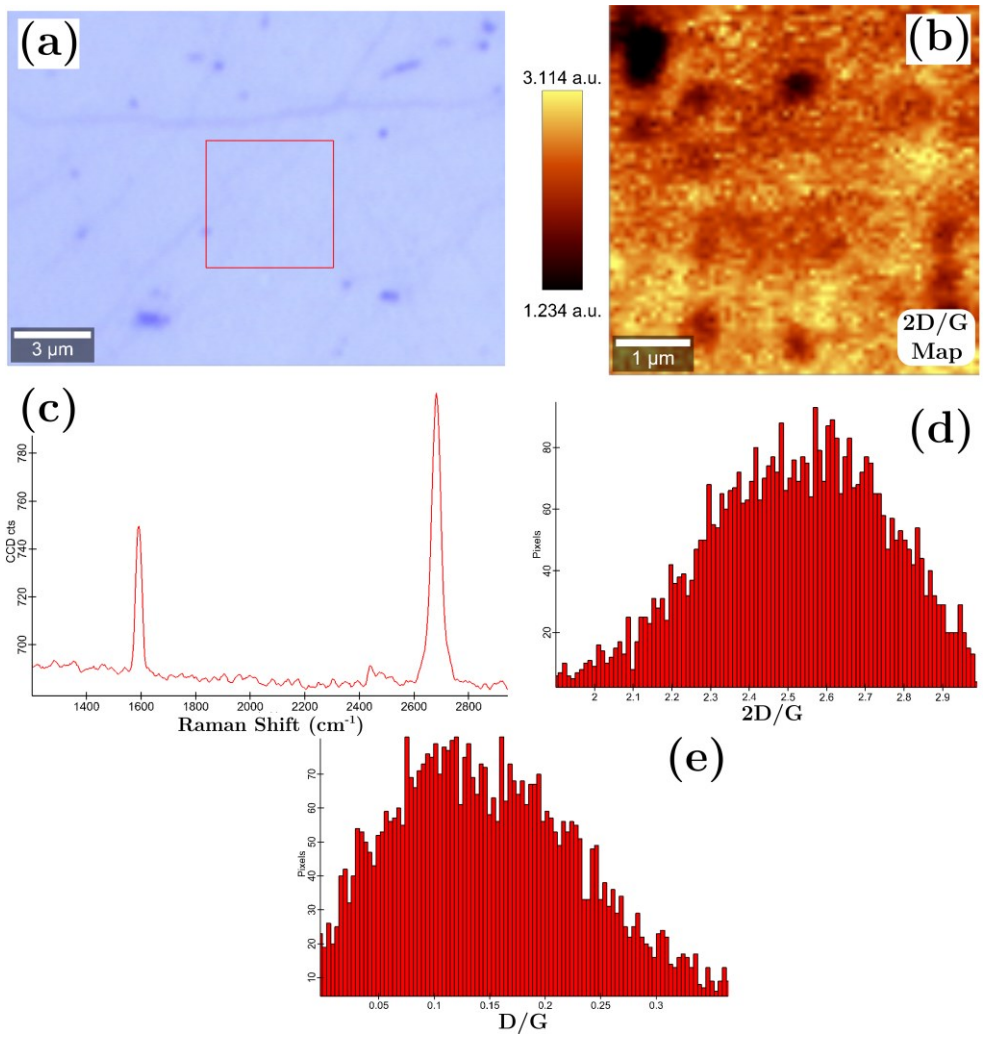


Figure 4.21. (a) Optical image, (b)-(e) Raman characterisation of another batch of graphene grown under the optimised condition of 2 Torr growth pressure and hydrogen to methane gas ratio of 32.

Lastly, it is important to make a comparison between the optimised graphene that was grown via the horizontal CVD system, the vertical CVD system and the one that can be obtained commercially from the Graphenea and Graphene Supermarket companies [140]. The optical images in Figure 4.22 compare the transferred graphene samples from the mentioned four different sources. Although the single layer regions of all four graphene films shared similar feature in their Raman profiles (such as 2D/G mean distribution of greater than 2 and D/G mean distribution of less than 0.3), it is apparent that the density of double/multilayer graphene as well as the doping levels varied between the samples. This was reflected in the FET characteristics of the samples as presented below in Figure 4.23.

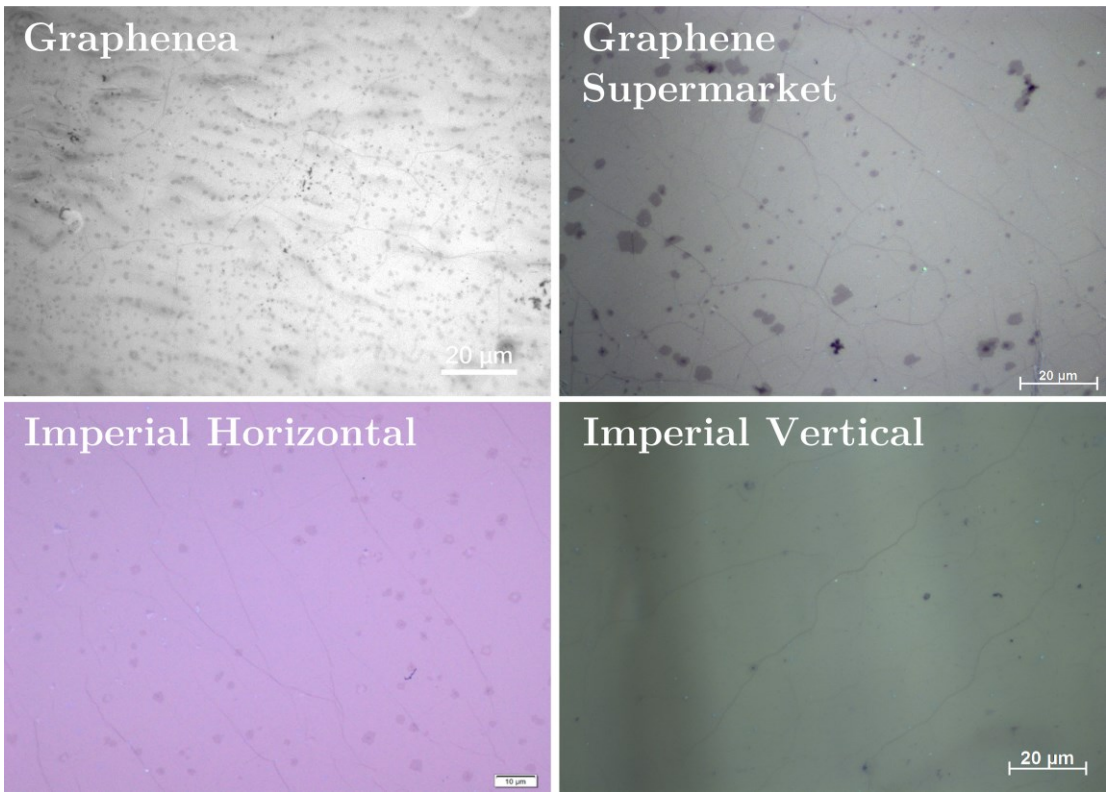


Figure 4.22. Optical micrographs of graphene samples from four different sources that were wet transferred on 300 nm SiO_2/Si substrates.[4]

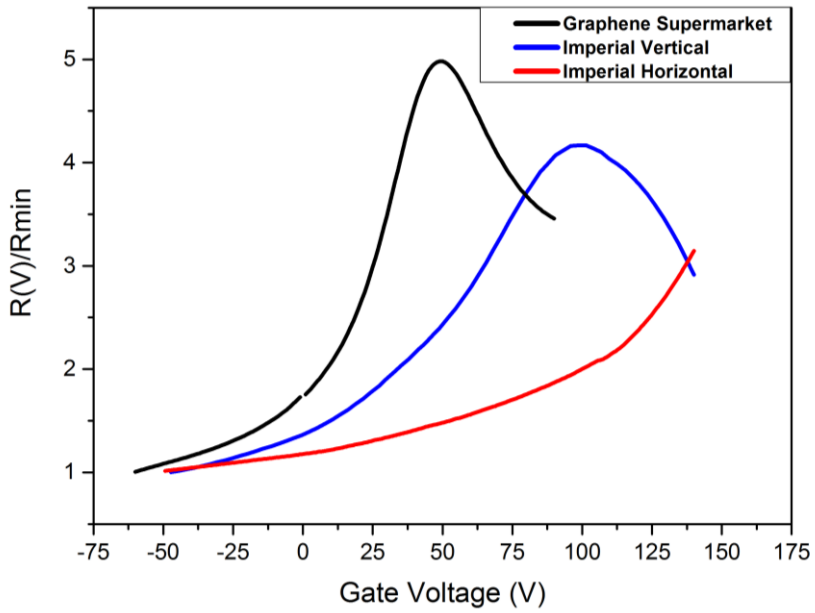


Figure 4.23. The obtained DC field effect characterisation of the three different CVD graphene samples that were grown under three different conditions. An identical wet-transfer procedure on 300 nm SiO_2/Si substrates was performed for every sample.

[4] In collaboration with Viktoryia Shautsova at Physics Department of Imperial College London

An identical wet transfer procedure was followed for fabrication of each device where untreated high resistivity silicon substrate (with 300 nm SiO_2) was used as the back gate electrode material. The obtained field effect data suggest that the graphene film which was supplied by Graphene supermarket has the best switching ratio as well as the least p-doping level associated with it. It must be noted that the reduction in steepness of the transport curves from left to right (Graphene Supermarket to Horizontal CVD sample) is indicative of reduction in carrier mobility that can potentially stem from an increased number of graphene layers. This suggests that although Raman analysis points towards single layer nature of samples grown in-house via both the Horizontal and Vertical CVD system, there is a possibility that these samples contain more than one layer of graphene film across the covered area.

4.3.2 Attempts of Graphene Synthesis on Evaporated Copper Thin Film [5]

It is known that growth of graphene with very large domains is directly correlated with the crystallinity of the underlying copper substrate. Wood et al. [141] showed that using single-crystal copper with planes aligned along (111) facet results in larger domains and a faster growth rate compared to other planes, merely due to the minimised lattice mismatch. In order to utilise the feature of the cluster CVD-PVD system, investigation into growth of graphene over copper thin films at lower growth temperatures via assistance of plasma was carried out. Sapphire and quartz substrates were chosen to serve as the copper growth platforms as both are known to facilitate epitaxially growth of (111) copper films. Copper thermal evaporation deposition is carried out at a rate of 0.3 Å/s and at 250°C utilising a copper source

[5] In collaboration with Dr Olena Shaforost at Imperial College

of 99.999% purity. As shown in Figure 4.24, the XRD spectrum of the films reveal the highly (111) orientated of the grown samples.

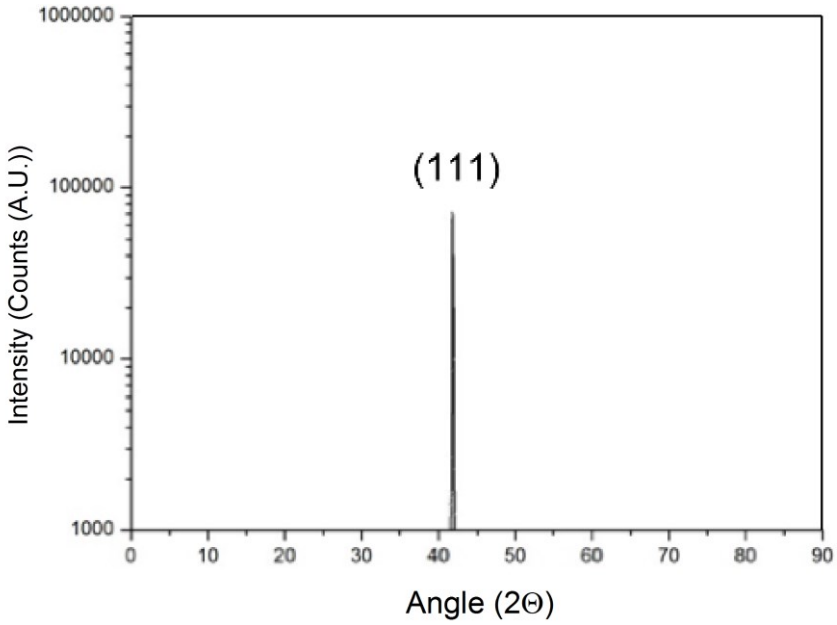


Figure 4.24. XRD spectrum of copper thin film grown via thermal evaporation on sapphire at 250°C at a rate of 0.3Å/s.

In order to make an attempt and grow graphene on copper thin films via a RF plasma enhanced CVD technique, the process was first carried out on a 35 µm thick copper foil. Temperature in recipe 1 was reduced to 500°C and plasma during growth was set to 170 W (referring to it as recipe PA1). Gas flow rates and pressure were set to identical values as to that of recipe 1. The optical image of the transferred graphene on a 90 nm SiO_2/Si substrate as well as the Raman spectrum associated with it are presented in Figure 4.25.

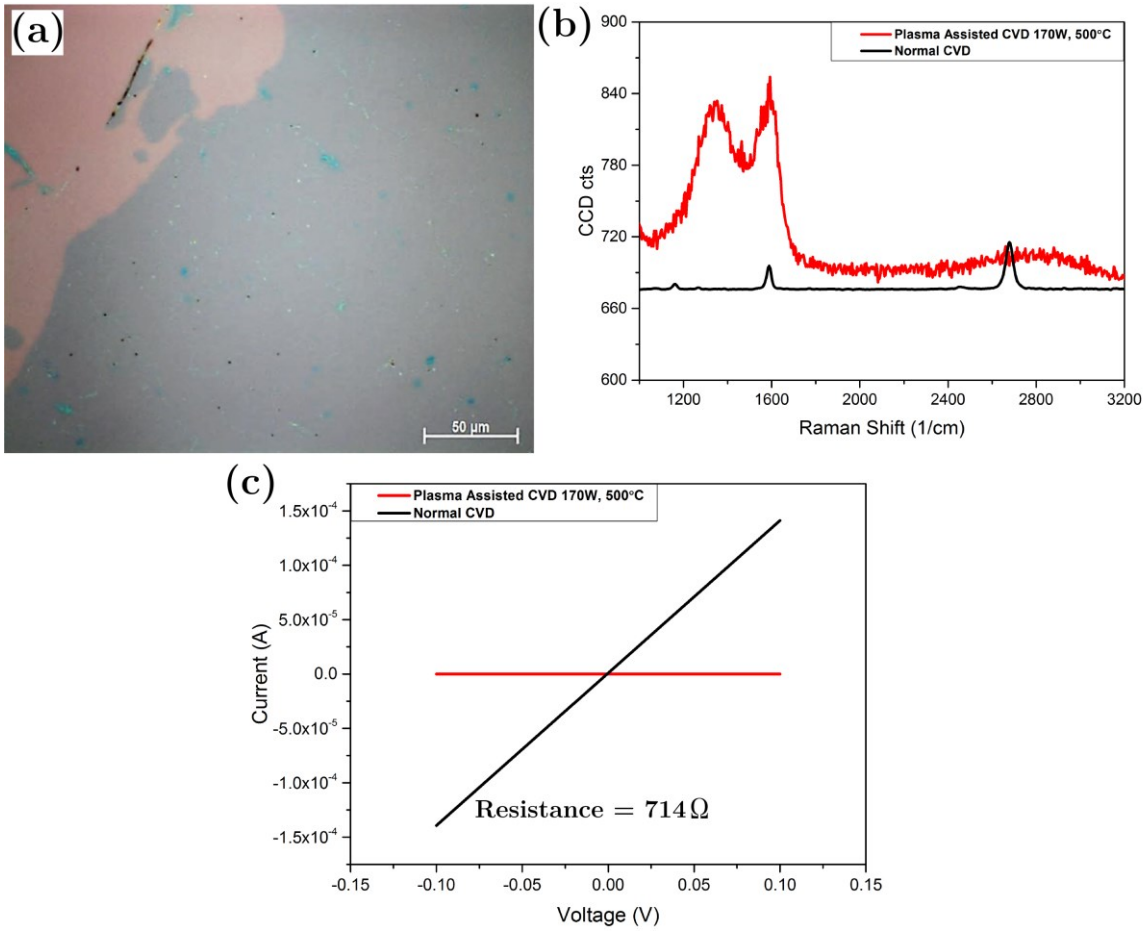


Figure 4.25. (a) Optical image, (b) Raman spectrum, and (c) the I-V electrical characteristics of the plasma assisted grown graphene film transferred onto silicon substrate with 90 nm thermal oxide.

It is clear that the Raman spectrum of the plasma assisted grown graphene is very different to that of a normal single layer graphene (red and black profiles in Figure 4.25b-c respectively). It is apparent that the plasma assisted sample has an amorphous nature where the 2D peak is missing and both the D and the G peaks are more intense compared to those in a single-layer graphene film. The electrical characterisation of the samples (Figure 4.25c) is also evident of the disordered nature of the grown sample, where no electrical conduction could be detected.

No further success was achieved by tuning a variety of different conditions including varying the plasma power between 150 W to 400 W and temperature from 500°C to 850°C. Furthermore, recipe PA1 was also tested on the copper thin films grown on sapphire. The obtained results were similar to that observed on copper foil. The

SEM micrograph in Figure 4.26 resembles graphitic patches with similar Raman profile to the one shown in Figure 4.25b.

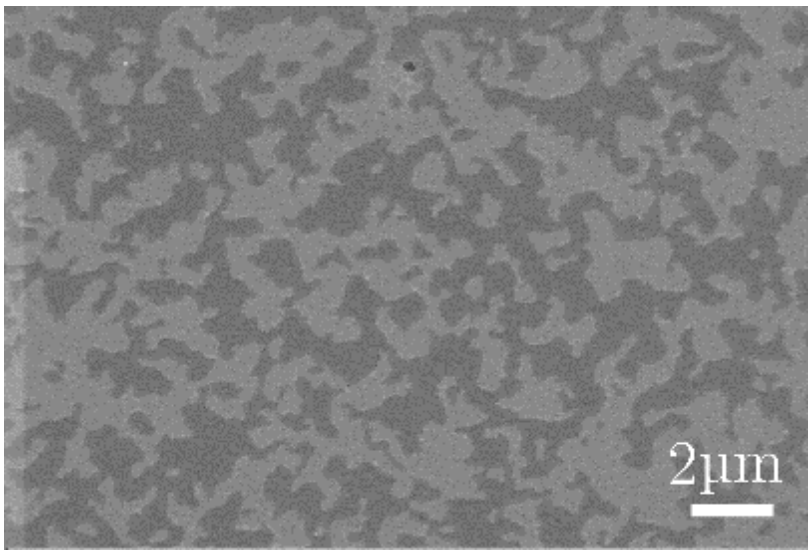


Figure 4.26. SEM micrograph of the graphene sample on copper thin film, exhibiting lumped batches of graphite-like nature.

Shortly after all the unsuccessful attempts, it was realized that the plasma generating unit could be the root cause of the problem. The RF generator in the system is placed on the top end of the vertical quartz tube surrounding the shower head, whereas the wafer holder during the growth process sits in the middle of the quartz tube, where the furnace heating zone is at its highest mean temperature. This means that the plasma generation and copper platform are about 9 cm away from each other. This is believed to result in only partially dissociated methane radical molecules that reach the copper surface. Therefore, batches of radical CH_2/CH_3 molecules would bond to form graphitic films over surface of copper as opposed to the expected agglomeration of carbon atoms in a typical CVD growth. Further optimisations were outside of the scope of this thesis. However, future works will include adjustment of the height of the sample holder close to the plasma unit and measurement of the exact temperature difference between the new position and the previous position by introducing an extra thermocouple into the system.

4.4 Gate Insulator Material Selection and Transistor Preparation

Typical field-effect structures that are based on a graphene channel, (Figure 2.8 in 2.2), are comprised of three distinct layers; (1) the electrically conductive graphene channel, (2) the gate insulating layer, and (3) a gate electrode material with electrical conduction capabilities. Often top-gating is preferred over back-gating because devices with top-gate terminals would not suffer from large parasitic capacitances and avoidance of thick insulators improves the ease of their integration with other components. [142] A large part of this work involves a methodology proof of concept and therefore G-FET devices will incorporate back-gated silicon with a measured resistivity value of 3500 Ω.cm. There are a number of insulating materials that can be used including oxides, nitrides and polymers that have already been subject to research for this purpose. A summary of potential gate materials along with their dielectric properties are shown in Figure 4.27 below.

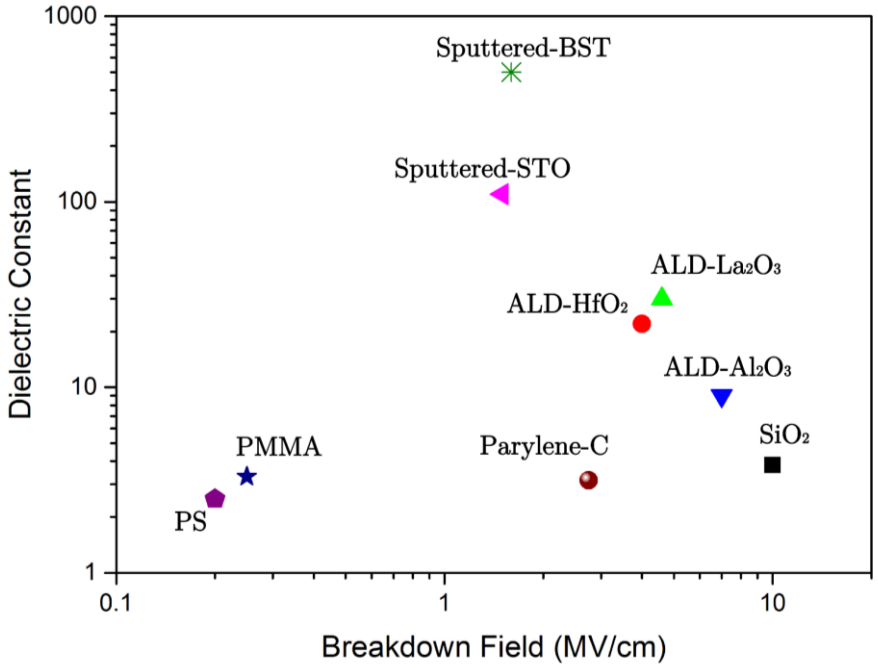


Figure 4.27. Potential gate insulating materials and their dielectric properties. [143, 144,145, 146,147,148,149]

It's important to note that the dielectric properties of these materials are directly correlated with their crystal structure, which itself is highly dependent on the method and condition of growth. Upon considering factors such as the dielectric strength of the insulating material, ease of fabrication procedure, as well as the synthesis feasibility of the gate materials, G-FET devices with gate dielectric of SiO_2, STO, YSZ, AlN, multilayer h-BN, and PMMA were fabricated and tested. To assess the quality of each material, XRD, AFM, and Raman spectroscopy were used and crystal structure as well as thickness of the grown dielectric layers were studied.

4.4.1 Silicon Dioxide

Two different types of silicon dioxide films were employed in this work; (1) native SiO_2 ($nSiO_2$) with a widely accepted thickness of 1 nm (Figure 4.28b) [150] and (2) 300 nm thermally grown SiO_2 on 500 µm thick high resistivity silicon (3500 Ω.cm), both purchased from Crys-Tech. [151] As shown in Figure 4.28a, SiO_2 has an amorphous structure, where single silicon atoms are tetrahedrally bonded to four oxygen atoms. It is a desirable choice as a gate insulator material because it readily forms on silicon substrates with no fabrication difficulties associated with it, it has a relatively good dielectric constant, and it is also compatible with the industrial silicon technologies. However, $nSiO_2$ suffers from current leakage at comparatively small gate voltage values. The working voltage range is measured to be limited to -5 to 5 V before breakdown of the material occurs.

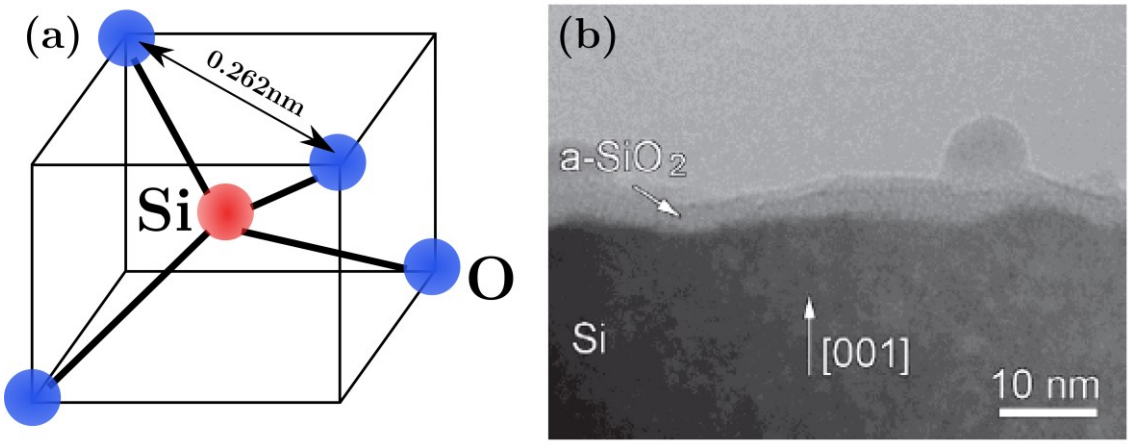


Figure 4.28. (a) SiO_2 lattice structure unit cell and (b) cross-section TEM image of a 1nm $nSiO_2$ layer on Si. [152]

4.4.2 Yttrium Stabilised Zirconia (YSZ) and Strontium Titanate (STO)

Both Yttrium Stabilised Zirconia (YSZ) and Strontium Titanate ($SrTiO_3$ denoted as STO) films in this study were grown via Pulsed Laser Deposition (PLD) technique. PLD is a physical vapour deposition method that is used for deposition of a variety of materials ranging from superconductors to dielectrics. [153] Variable growth rate, epitaxially growth at relatively low temperatures, and good control over growth parameters has transformed it into a flexible and attractive deposition technique. Here, the employed PLD system works by using a 248 nm wavelength Excimer laser. The laser is aimed at a given target material which is rotating. Each laser pulse superheats the surface and results in ablation. Ablation is a process where the incident laser interacts with the target material, heats the surface beyond melting temperature and produces plasma as a result of ionisation of the ejected species. The resulted laser plume will contain atoms, molecules, ionised species, and particle clusters. [154] The working principles and a photograph of the PLD system that was used in the present work are represented in Figure 4.29. It is worth noting that in order to achieve epitaxial deposited films with better crystallinity and smoother surfaces, substrates are usually heated to above 400°C.

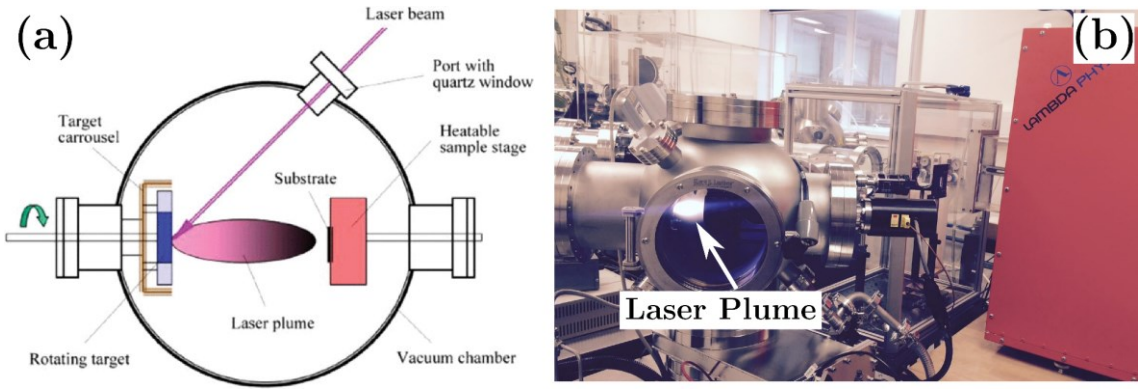


Figure 4.29. (a) Schematic presentation of the working principles and (b) a photograph of the PLD system. [155]

Three distinct G-FET structures were built based on YSZ and STO dielectric layers: (1) 80nm YSZ, (2) 80nm of STO, and (3) stack of 50 nm STO on 10 nm YSZ. The performance of the devices was investigated individually. The PLD growth conditions for both YSZ and STO are shown in Table 4.2. Upon completion of STO film growth, the chamber is filled with O_2 at pressure of 600 mTorr for 20 minutes to ensure full oxidation of STO thin film.

Table 4.2. PLD growth conditions of the YSZ and STO thin films.

Gate Material	Film Thickness (nm)	Laser Energy (mJ)	Growth rate (Å/pulse)	Growth Pressure (mbar)	Growth Temperature (°C)
YSZ	80	520	1 (10Hz)	10^{-5}	800
STO	80	520	1 (10Hz)	10^{-3}	740
YSZ/STO	10/50	520	1/1 (10Hz)	$10^{-5}/10^{-3}$	800/740

It is important to note that growth of both thin films had previously been matured by Materials department's thin film technology lab experts led by Dr Petrov. This greatly facilitated achieving high quality films. [156] As shown in Figure 4.30, both STO and YSZ take a cubic lattice structure where the lattice constant of YSZ is slightly larger than that of STO (0.51 nm compared to 0.39 nm). The cubic lattice structure of both materials means that the interplanar spacing between the (100) planes would ideally be equal to the lattice parameter of the structure. However,

the Poisson ratio need be taken into account for a more precise lattice parameter calculation.

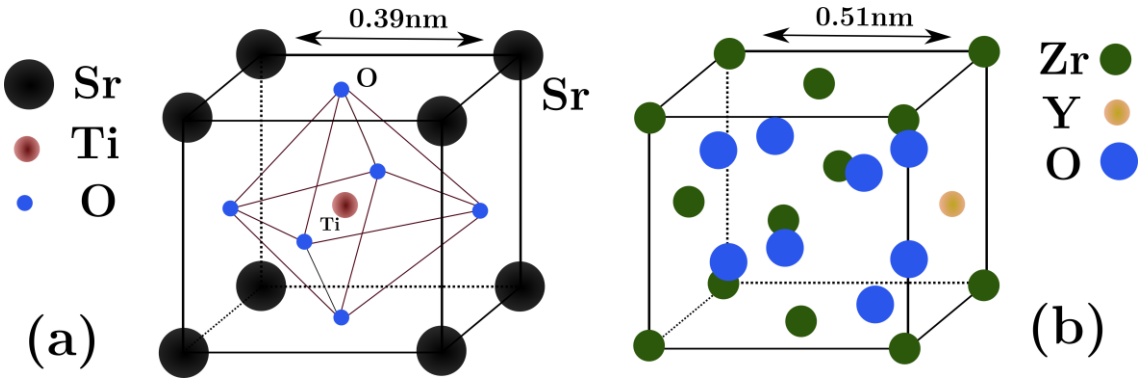


Figure 4.30. The cubic lattice cell structure of bulk (a) STO and (b) YSZ.

The thickness of the grown films and their crystallinity were investigated via AFM and XRD analysis respectively. As shown in Figure 4.31, the thickness of the YSZ film was found to be 80 nm, confirming the accuracy of the input PLD growth parameters. The roughness of the surface was also measured to be about 0.7 nm, indicative of a smooth surface morphology. Furthermore, the films were found to be oriented along family of (200) planes as shown by the XRD spectrum of the YSZ film in Figure 4.31 (c). The PLD grown STO thin films on nSiO_2 as will be shown later in 5.1 appear to have current leakage associated with them. This is due to the large mismatch between thermal coefficient of expansion, α, of STO and SiO_2 ($6.8*10^{-5}$ K^{-1} and $5.6*10^{-7}$ K^{-1} respectively). Therefore, 10 nm YSZ (α=$9.2*10^{-6}$ K^{-1}) was grown as the buffer layer at STO/SiO_2 interface to improve structural integrity of STO and to consequently reduce current leakage, enabling utilisation of STO's high dielectric performance in G-FET devices. [157]

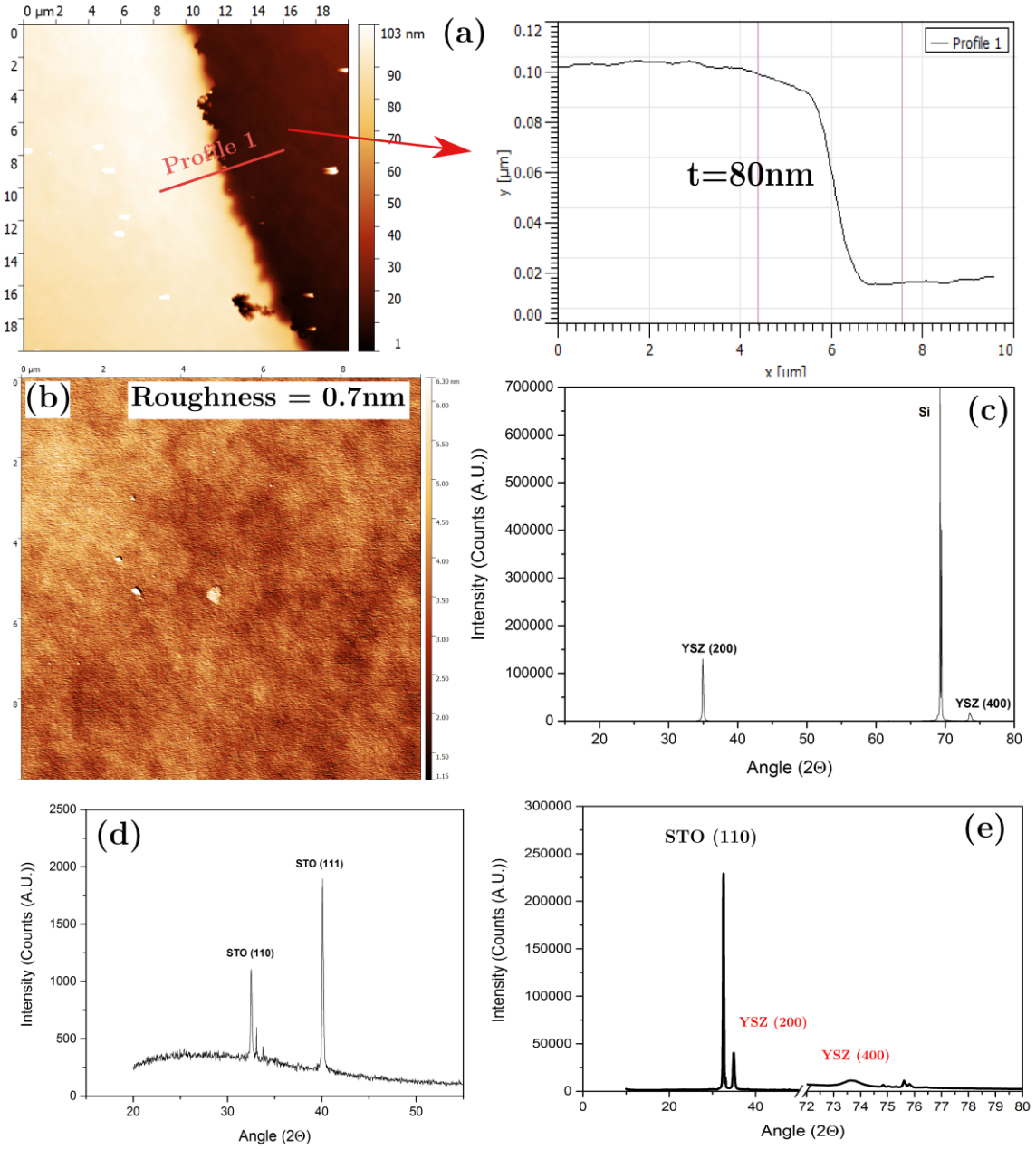


Figure 4.31. (a) Thickness measurement via AFM showing thickness of 80 nm in agreement with the input values of PLD growth parameters. (b) The 0.7 nm roughness value is indicative of a smooth surface for the grown YSZ film, and (c) The XRD results confirming the crystallinity of PLD grown YSZ samples. (d) XRD spectrum of the STO film grown on $nSiO_2$ and (e) STO on 10 nm YSZ on $nSiO_2$.

Using Bragg's diffraction law ($\lambda = 2dSin(\theta)$), the interplanar spacing, d, of each of the films can be calculated from combining the obtained diffraction angle and the wavelength of the X-ray beam, λ, which is known to be 0.154 nm.[97] A summary of the extracted data is presented in Table 4.3 below.

Table 4.3. Interplanar spacing of the fabricated thin films extracted from XRD data.

Gate Material	Prominent 2θ (°)	Corresponding interplanar spacing (Å)	Corresponding diffraction plane
YSZ	35	2.5	(200)
STO	32	2.8	(110)

These extracted numbers will further be used in the next chapter in order to explain the observed difference in the performance of the fabricated G-FETs that utilised YSZ and STO gate dielectric layers.

4.4.3 Aluminium Nitride

Aluminium nitride thin films are grown using a radio frequency (RF) magnetron sputtering system. The RF sputtering technique was chosen merely because the DC sputtering method is not capable of depositing insulating materials. The schematics of a typical RF sputtering process is displayed in Figure 4.32. It illustrates how the energised ionised Argon molecules bombard the surface of the target material and result in ejection of the target atoms. This subsequently results in deposition of a thin film of the material on the substrate.

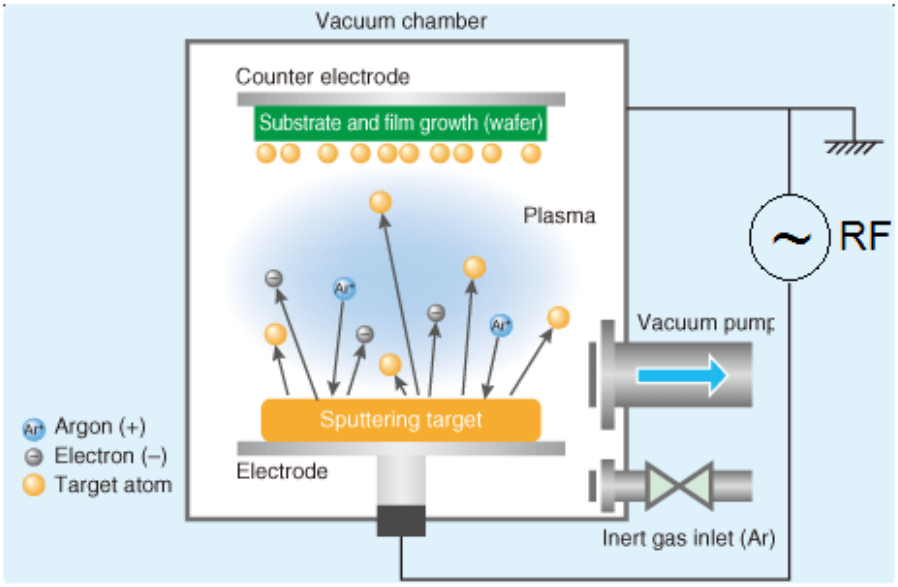


Figure 4.32. Schematic of a typical RF sputtering system. [156]

The sputtering process in this work was conducted in a Mantis combined sputtering/thermal evaporation system with a base pressure of 5×10^{-8} mbar. In order to grow thin films of AlN, 40% N_2/Ar partial pressure at growth pressure of 4×10^{-3} mbar and RF power of 200 W were used. The temperature of the target and the growth rate were set to 400°C and 0.3 Å/s respectively. A typical crystal structure of Aluminum nitride is shown in Figure 4.33. AlN is known to have a direct band gap of 6 eV which transforms it into an ideal dielectric material.

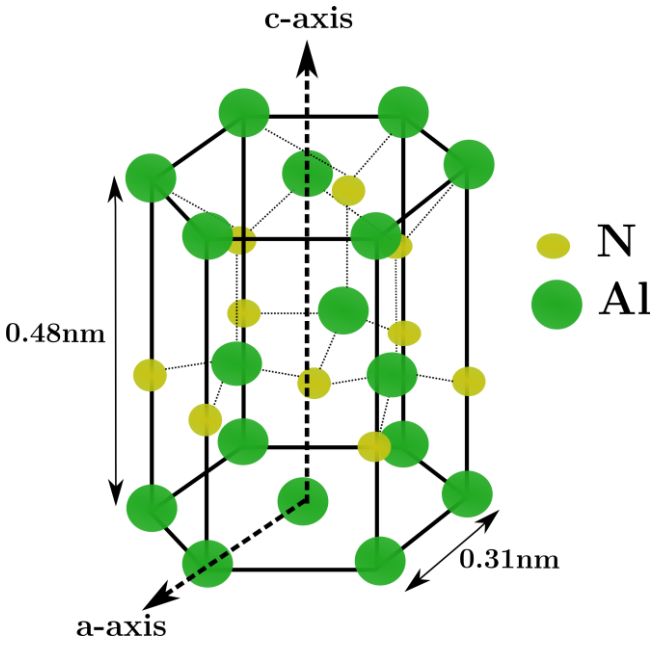


Figure 4.33. A typical hexagonal crystal structure of AlN with lattice parameters of a=0.31 nm and c=0.48 nm. (Motivated by [158])

The thickness and roughness of the films were confirmed via AFM and the crystal structure of the grown AlN films was investigated by the XRD analysis. As shown in Figure 4.34, the sputtering process has been done to a good accuracy as the obtained 5 nm film thickness is in good agreement with the input parameters. Moreover, the roughness value of 0.4 nm is a strong indication of the low surface roughness of the sputtered thin films under the used growth conditions. The XRD spectrum shown in Figure 4.34c illustrates the c-axis orientation ((0002) plane) of the AlN films. [159] Weak relative intensity of the peak is merely the consequence of the extremely small thickness of the grown film.

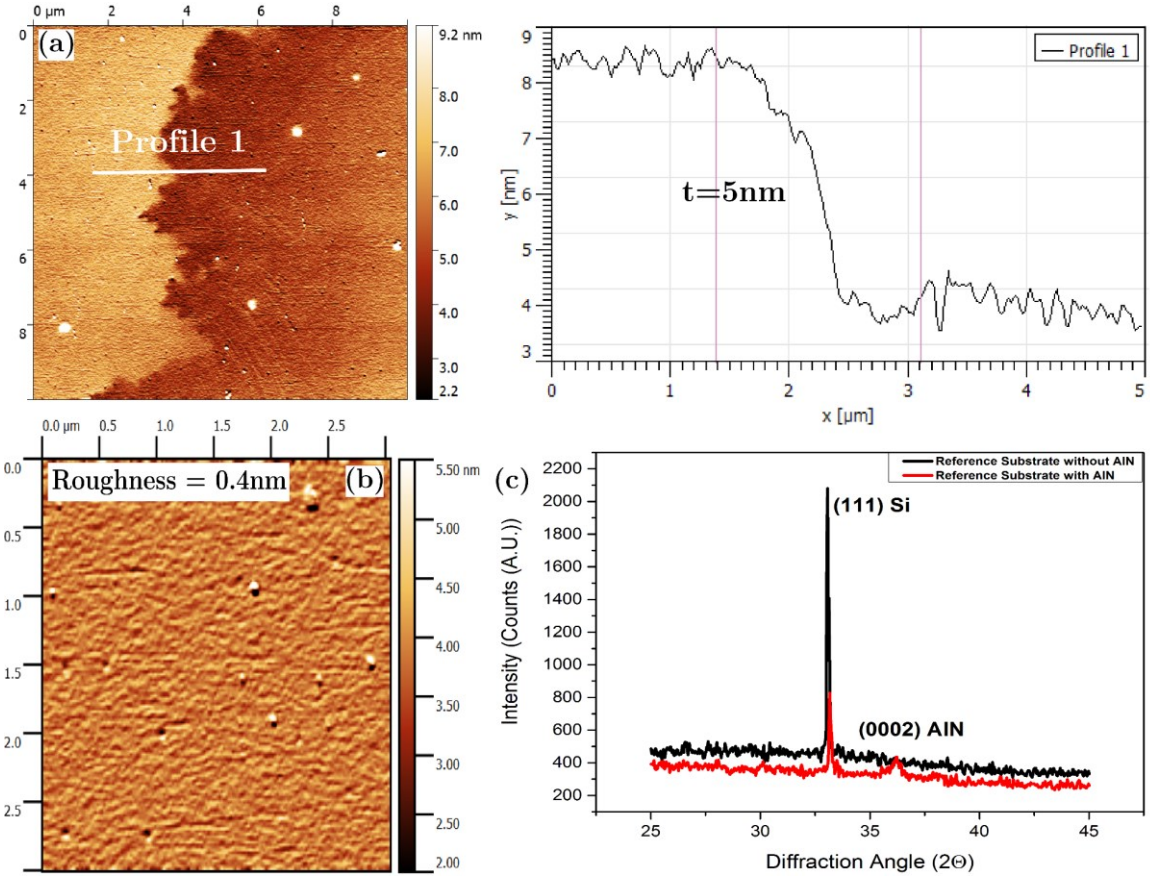


Figure 4.34. (a) Thickness of AlN and its (b) roughness measured by AFM analysis. (c) XRD results confirming the presence of the sputtered film.

To further probe the characteristics of the grown AlN films, capacitance-voltage measurement was carried out on the structure shown in Figure 4.35a with graphene and GaN acting as parallel plates of the structure. This was carried out to investigate the piezoelectric properties of AlN which would allow this material to potentially have a dual functionality when incorporated in a G-FET device. [160]

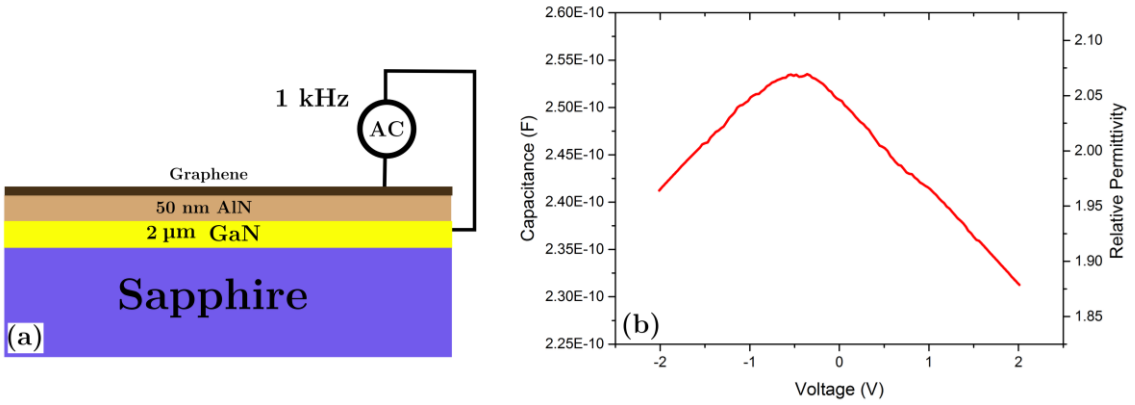


Figure 4.35. (a) Graphene-AlN-GaN capacitance structure that was used to obtain the (b) C-V characteristics of the AlN thin film.[6]

The area of the plates was measured to be 694257 µm^2 which combined with the dielectric thickness of 50 nm resulted in a relative permittivity of 1.9-2.05. The piezoelectric characteristics of AlN can potentially present a dual sensing functionality when coupled with graphene. This will be further discussed in 5.4.

4.4.4 Multilayer Hexagonal Boron Nitride (h-BN)

Commercial CVD grown single-layer and multilayer h-BN (13 nm thick) on copper were purchased from Graphene Supermarket on the target substrates via a wet transfer technique identical to the one used for graphene transfers (refer to 4.5.1). A thin film of h-BN is known to neutralise graphene by providing a platform on which graphene remains un-doped. [161] Multilayer h-BN was chosen over single-layer h-BN in order to increase the probability of obtaining pin-hole-free insulating layer as well as to have a broader measurement range for characterisation of the G-FET devices. The transferred multilayer films were characterised via both the XRD and the Raman analysis. The optical image in Figure 4.36a illustrates the presence of a large number of wrinkles in the transferred films. Despite the full coverage of the transferred h-BN films, the samples were found to contain residues and contaminations which were difficult to remove. The XRD spectrum combined with

[6] In collaboration with Lin Chen-Sheng

the performed Raman analysis (Figure 4.36b-d) were both in agreement with the previous works in the literature and both confirmed presence of the multilayer film. [162]

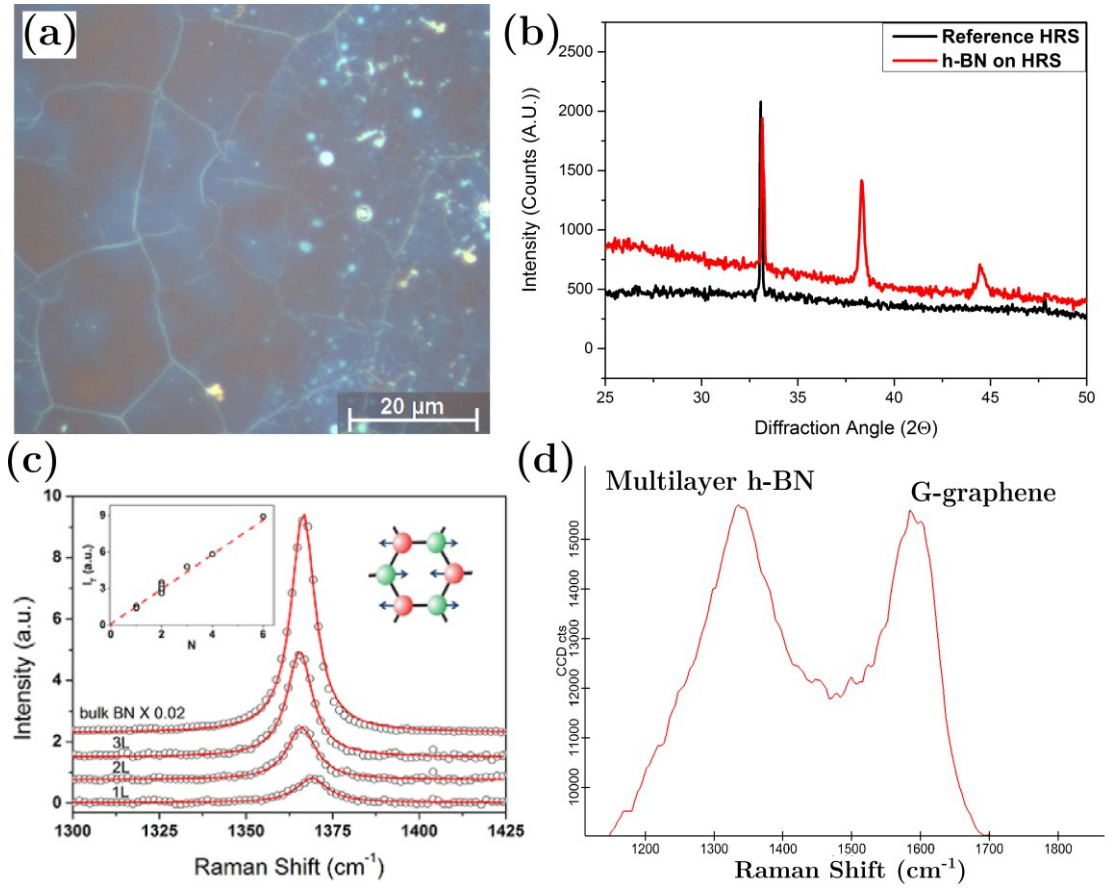


Figure 4.36. (a) The optical micrograph of a wet transferred multilayer h-BN film on a 90 nm SiO_2/Si substrate. (b) The XRD spectrum, (c) reference h-BN Raman spectrum and (d) the obtained Raman spectrum of the G-FET device fabricated with the transferred h-BN film on nSiO_2 on HRS. [162]

4.5 Graphene Transfer to Target Substrates

As discussed in 2.5, there exists two well-established ways of transferring graphene from copper on to a given substrate; dry and wet. Both methods were investigated by following the already established procedures. [28] It was found that the dry transfer leads to a large number of wrinkles as well as a greater number of defects and cracks especially when the dimension of the sample becomes large (>0.25 cm^2).

Based on the achieved results, wet transfer was chosen as the main method of transfer for delivery of clean, defect-free and consistent graphene films.

4.5.1 Wet Transfer

Transferring graphene from copper onto a given substrate via the matured wet transfer technique, although might seem straightforward and trouble-free, but it is a process where even slight carelessness can result in introduction of large number of structural defects.

Soon after completion of the graphene CVD growth, PMMA is deposited on graphene/copper via the spin coating technique. Few drops of PMMA solution are dispensed over the stack and it is spun at a fast rate of 8000 rpm for 60 seconds to form a homogenous thin layer of PMMA. The film is measured to be about 423 nm thick (see Figure 4.42a). The coated PMMA provides the required support and rigidity for the next stages of transfer. The next step involves removal of the unintentionally grown graphene on the back-side of copper. Removing the backside graphene is done via chemical treatment by using diluted 10% nitric acid water solution. The sample is placed on a flat transparent polypropylene film with PMMA facing down and all four sides taped as shown in Figure 4.37.



Figure 4.37. Photograph showing back-side of copper taped and ready to be cleaned using nitric acid contained cotton bud.

A nitric acid dipped cotton bud is then used to rub back-side of copper (the exposed middle part). Taping is done merely to avoid leakage of acidic solution from the sides on to the top side, which can deteriorate PMMA and subsequently graphene on the top-side. The back-side is then cleaned with a water dipped cotton bud and is then cut into a desirable dimension. The removal of the back-side graphene is an eminent part of the transfer process. Leaving this step out can result in aggregated and rolled up graphene pieces at the graphene-substrate interface. This can reduce the coverage of graphene after the transfer is completed. An example of such a case where the back-side graphene has not been removed is shown in Figure 4.38.

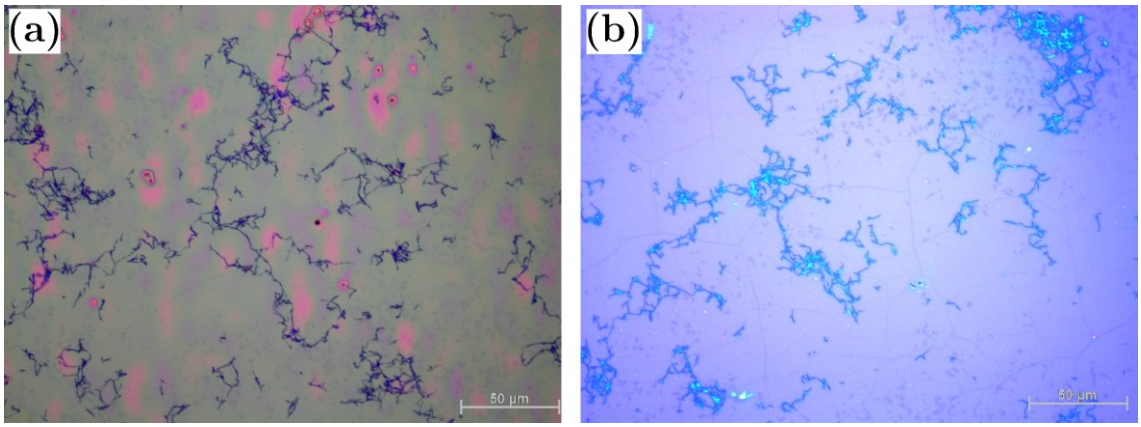
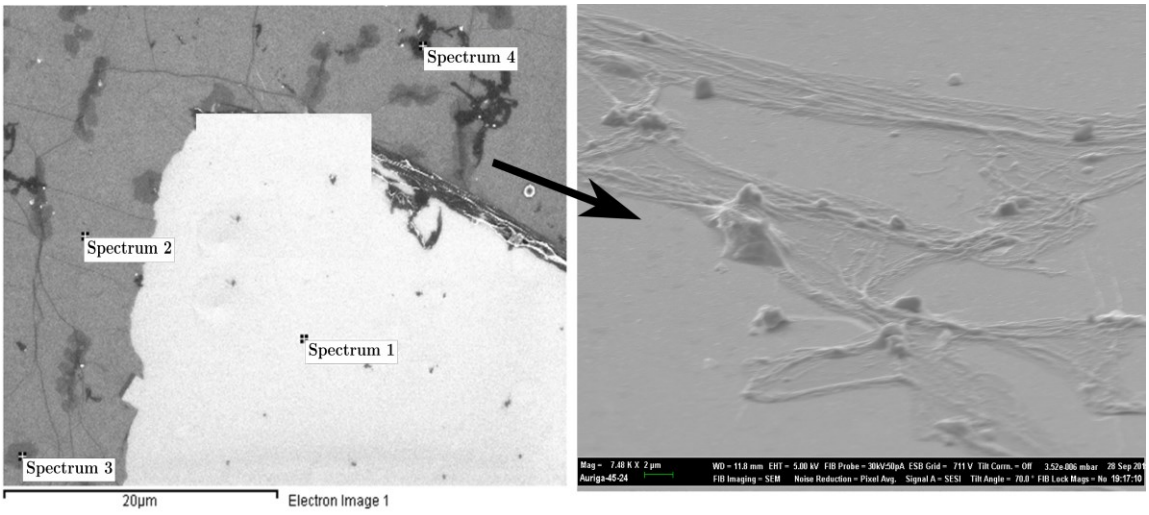


Figure 4.38. Transferred graphene on Silicon with 90 nm SiO_2 (a) after transfer and before removing PMMA (pink areas contrast arises from optical reflection of PMMA) and (b) after PMMA removal.

After completion of the transfer process, the EDX analysis, as presented in Figure 4.39, was carried out on different areas of the sample to investigate the nature of the contamination on the surface. It was found that the carbon content of the suspected contamination species is relatively higher compared to the rest of the surface. Although it points towards the fact that these species are potentially rolled-up state of the remainder of back-side graphene, but it does not remove that they could arise from residual PMMA. Therefore, to avoid using PMMA, a PMMA free transfer process was invented and carried out. As will be shown later in 4.5.2, the contamination species were found to be present even when the transfer process

was carried out without using a polymeric support layer. It proves that these contaminations are indeed the rolled-up form of the unremoved back-side graphene.



Spectrum	In stats.	C	O	Si	Total	Conclusion
Spectrum 1	Yes	7.30	26.61	66.09	100.00	SiO_2 Surface
Spectrum 2	Yes	17.62	25.13	57.25	100.00	Graphene
Spectrum 3	Yes	16.65	25.56	57.79	100.00	Graphene
Spectrum 4	Yes	33.46	24.76	41.78	100.00	PMMA or rolled up back-side graphene

Figure 4.39. EDX analysis of different spots post-graphene transfer. (Image on the right has a scale bar of 2 µm) [7]

In the next step of transfer, the spin-coated samples are placed in an ammonium persulfate (APS) solution that consists of 1.1 gr in 100 ml water (0.1M molarity). This is carried out twice to remove the underneath copper and it takes about 8 hours each time (Figure 4.41a). It is important to carry out the copper etching two times in order to ensure full removal of the copper residues. As shown in Figure 4.40, the optical microscopy images confirm the presence of copper residues on the samples that have only been APS treated once.

[7] **In collaboration with Dr Stefan Goniszewski**

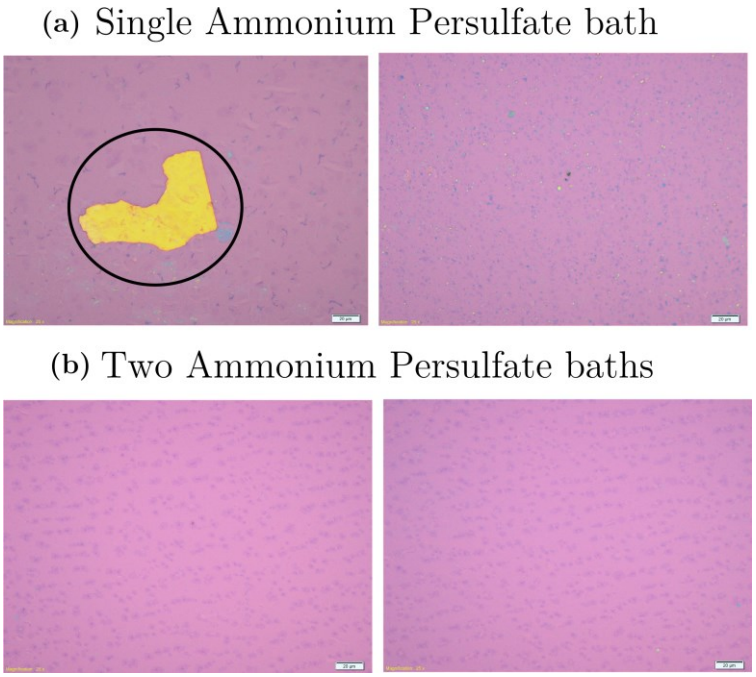


Figure 4.40. Bright field optical images indicating (a) the presence of copper residues after single bath of APS compared to (b) when etching is carried out twice (Scale bars are 20 µm).

The sample is then cleaned in DI water solution three times to dispose of any remainder of the etching solution on the sample. It's important to note that the samples are transferred from one water container to another without ever being touched. This is done via a polyethylene made mini-spoon. The target substrate is then placed on the head section of a dental mirror, loosely attached to it via a small piece of double-sided tape (Figure 4.41b). The head provides a flat platform for substrate while the handle offers a great control on movements.

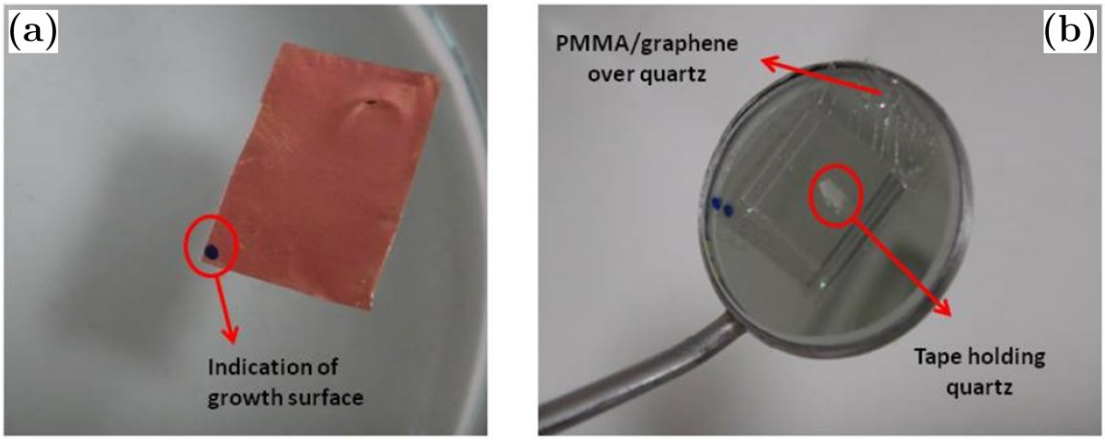


Figure 4.41. The as-grown graphene film on copper in (a) a 0.1M ammonium persulfate solution. (b) The transferred PMMA/graphene stack on a quartz substrate using the dental mirror assisted approach.

This assembly is used to transfer PMMA/graphene stacks from DI water onto a given substrate. The sample is then left under the fume cupboard to dry overnight. Once the trapped water is fully cleared, the substrate is heat treated on a hot plate at 180°C for the duration of one hour. It not only results in a thinner PMMA, but also it ensures enough adhesion between graphene and the substrate. Dektak 150 profiler was used and the approximate thickness of the PMMA film before and after reflow was measured. As presented in Figure 4.42, there is a 194 nm thickness reduction associated with heat treating PMMA at the mentioned conditions.

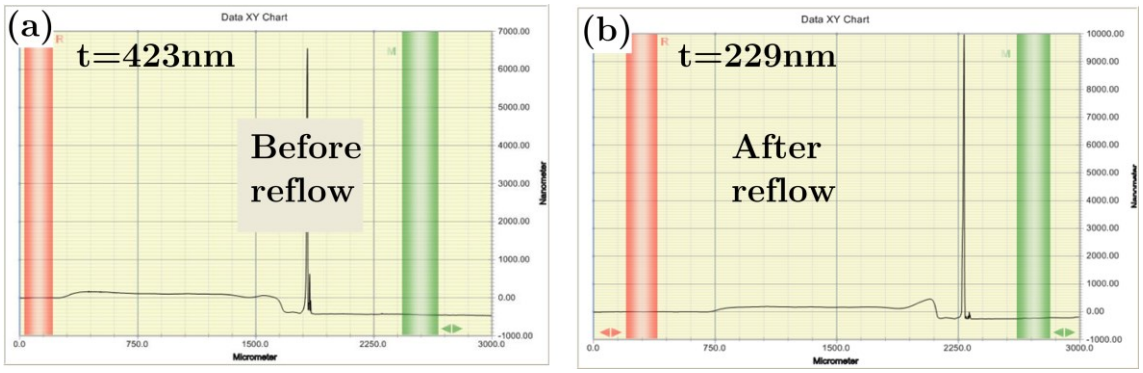


Figure 4.42. Thickness of PMMA after transfer and (a) before heat treatment at 180°C for one hour and (b) after the treatment.

Figure 4.43, highlights the importance of this heat treatment step as skipping it may result in poor adhesion and consequent removal of graphene once PMMA removed via the solvent solution.

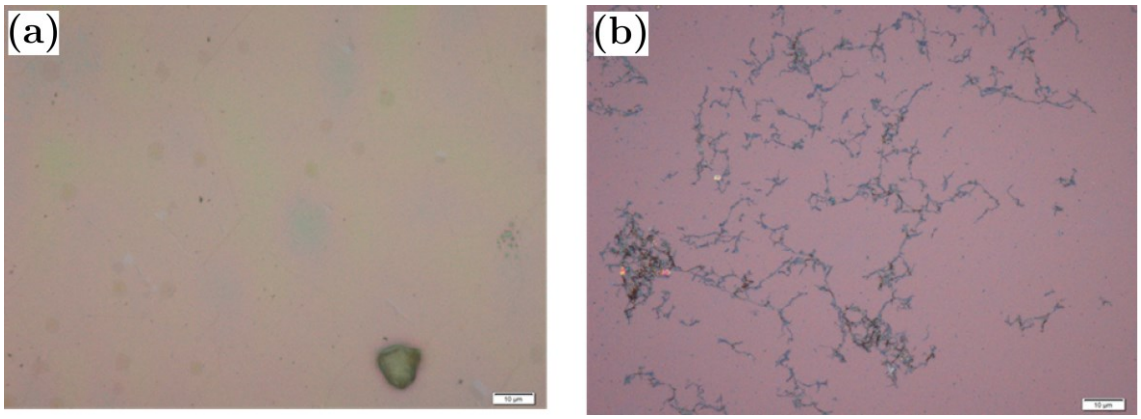


Figure 4.43. The Un-heat-treated transferred graphene film (a) before pmma removal and (b) after pmma removal (right). The poor level of adhesion between graphene and the substrate has resulted in removal of the graphene film together with PMMA. (Scale bar is 20 µm)

However, it is important to note that deterioration of the sample has also been observed when heat treatment is carried out too early. As can be seen in Figure 4.44, when heating is carried out within 4h of transfer, graphene/PMMA stack breaks into pieces as result of sudden evaporation of the remaining trapped water at the oxide-graphene interface.

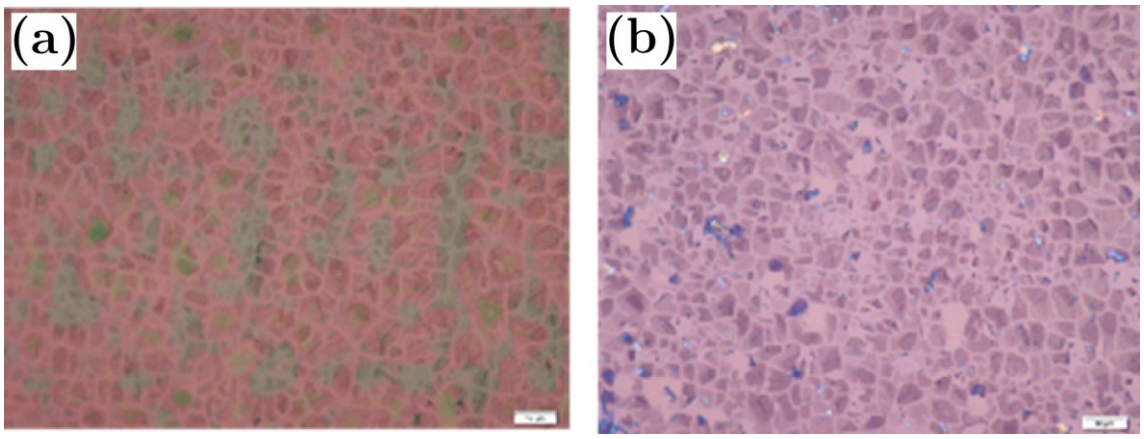


Figure 4.44. (a) Before and (b) after removal of pmma (left and right respectively) for sample with significant water trapped between graphene and substrate (Scale bar is 20 µm).

The final step of the transfer process involves removing the PMMA support layer. Effectiveness of different solvents as well as annealing in H_2 atmosphere were investigated. As can be seen in Figure 4.45, various solvents were used to remove PMMA from graphene. It is apparent that dichloromethane followed by warm acetone are the most effective solvents, whereas chloroform, MIBK, and Anisole have all damaged graphene and have resulted in partial graphene peeling from the underlying substrate. On the other hand, annealing under H_2 flow at 350°C has also resulted in a clean removal of PMMA, although very small (sub-micron size) residues have remained. Based on the achieved results and the fact that the solvent based PMMA removal process does not require physical transfer of the samples to other laboratories, Dichloromethane was chosen as the primary choice of PMMA removal for all the graphene based FET structure throughout this work.

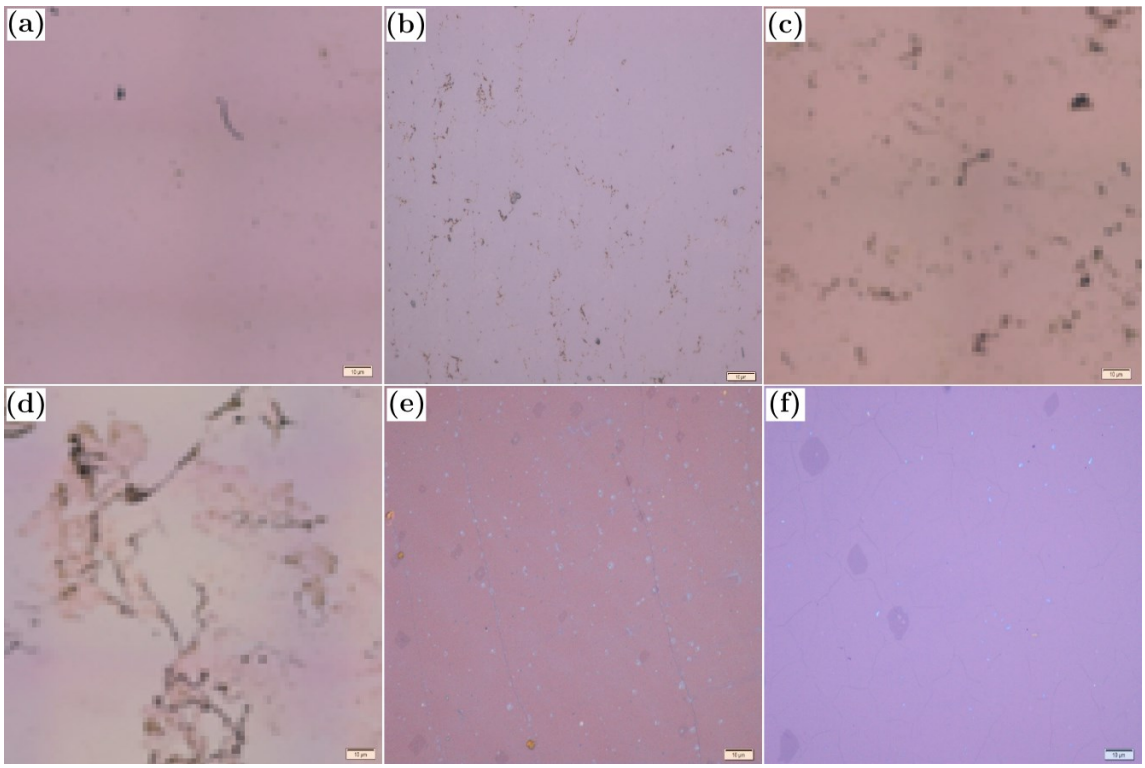


Figure 4.45. Similar graphene films transferred on silicon substrates with 90 nm SiO_2 where PMMA is removed by (a) Dichloromethane (b) Chloroform (c) MIBK (d) Anisole (e) warm Acetone and (f) annealing under H_2 atmosphere at 350°C for 12h. It is apparent that in images (b)-(e) graphene has been fully deteriorated (All scale bars 10 µm).

It is concluded, from the obtained results, that the contamination can either be the left over PMMA or the rolled up back-side graphene. Therefore; the question on whether or not the contamination arises from the back-side graphene remains. To solve this, a similar sample was transferred via a PMMA-free transfer technique. This technique was developed by combining ideas from two different works in the literature. [163-164]

4.5.2 PMMA-Free Pen-Tape-Frame Transfer

As briefly mentioned in the previous part, in order to verify the nature of the regularly observed contamination after the transfer process, a PMMA-free transfer technique was developed. It involves using a water-proof pen in combination with a 100 µm kapton tape frame. Pen is used to create a uniform frame with a good level of adhesion to graphene and the tape is used to keep the pen frame intact.

Both frames are constructed on the top-side of the graphene film and before removal of the copper substrate. Photographs in Figure 4.46 are examples of a copper etched graphene sample while utilising the described frame. Figure 4.46a demonstrates a single layer graphene sample whereas in Figure 4.46b, multilayer graphene sample is intentionally damaged by a sharp needle to clarify presence of the sample upon creating an apparent contrast.

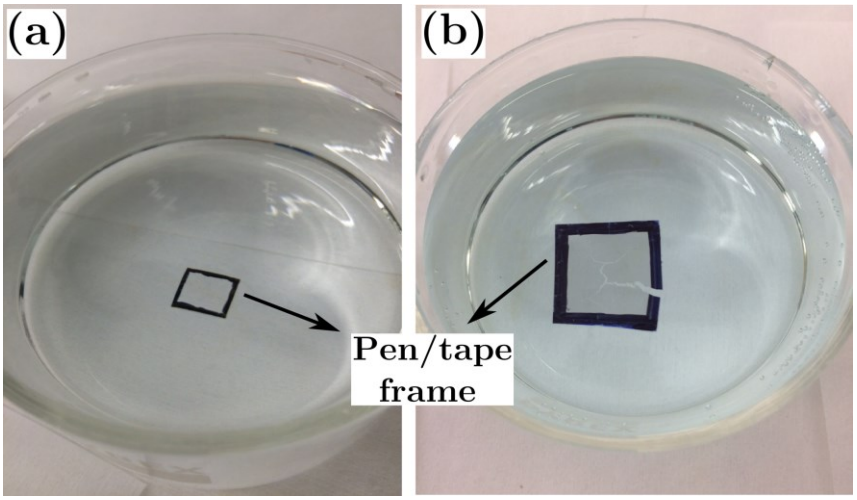


Figure 4.46. Photographs illustrating a (a) single layer and (b) multilayer graphene film in an ammonium persulfate solution using a pen-tape-frame assisted transfer technique.

As apparent from the optical image in Figure 4.47a, the very same bulky features (identified by red circles) are still observed although no PMMA was used to carry out this graphene transfer. It proves that the regularly observed contamination does indeed originate from the un-etched back-side graphene. It rolls into a denser graphitic type structure and adheres to the top-side graphene upon removal of copper. This is in agreement with the Raman analysis that is shown in Figure 4.47b-c. It is clear that this method is not suitable for transfer of single-layer graphene as it results in great number of cracks and structural disorders. The increased intensity of the D/G ratio in the Raman spectrum as well as the large amount of wrinkles observable in both 2D/G Raman map and the optical image of the sample are indicative of incapability of this method in delivering defect-free large area graphene films. However, it must be noted that this technique shows to

be a suitable approach for transferring thicker films such as multilayer graphene as well as the multilayer h-BN films. It can be concluded that it is important to ensure a strong enough Nitric acid solution is used and the back-side graphene is completely removed.

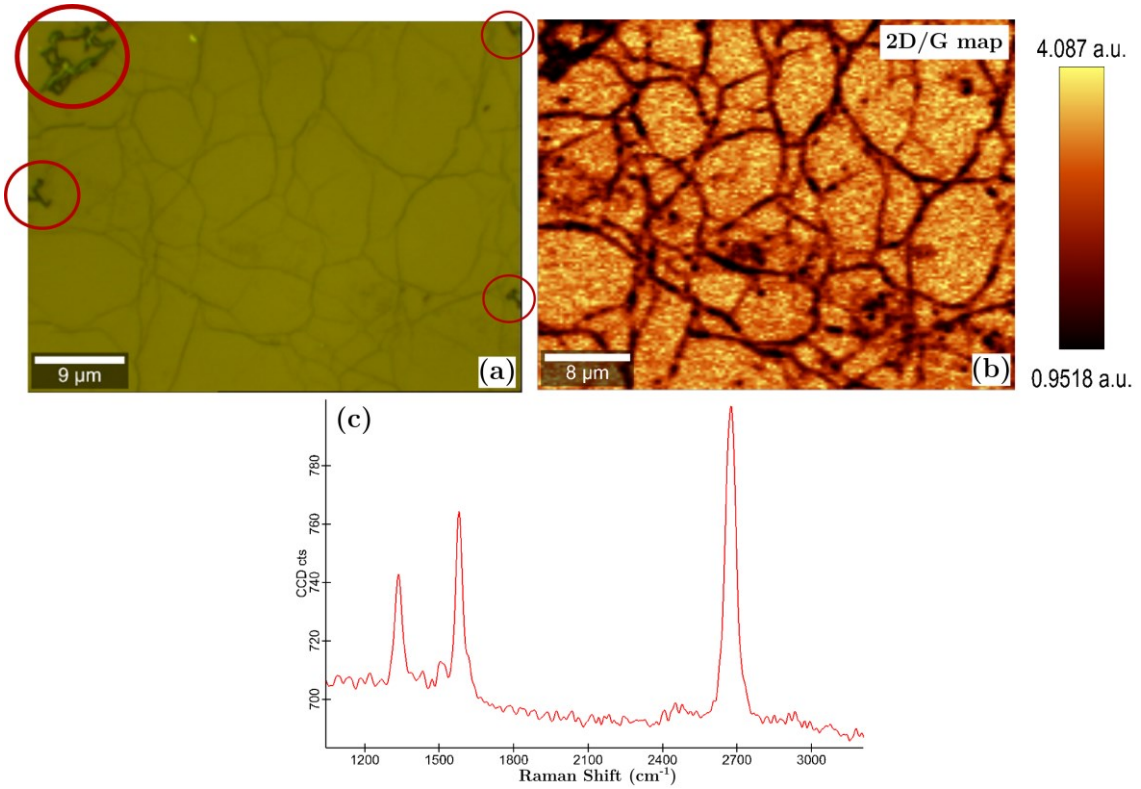


Figure 4.47. (a) The optical image, (b) the 2D/G Raman map and (c) the Raman spectrum of a single layer graphene film transferred on silicon substrate with 90 nm SiO_2 via PMMA-free pen-tape-frame transfer method.

4.5.3 Dry Transfer

The dry transfer technique as discussed in 2.5.2 was first introduced by Song et al. [86]. This method was followed step by step in order to transfer graphene films from copper foil onto target substrates. This dry transfer procedure involves construction of a polymeric stamp made from Poly-dimethylsiloxane, better known as PDMS. A glass petri dish was taken and it was made hydrophobic by leaving Hexamethyldisilazane solution in it for 6hours. A silicon elastomer and its curing agent are then added to the dish in a mixture ratio of 9:1 (9 grams of elastomer and 1 gram of curing agent). The resulting stamp has a thickness of 3 mm. The

mixture is then put inside a vacuum oven set at 75°C for 4 hours to ensure that the final stamp will have enough hardness and rigidity for handling purposes. The stamp is then placed over the PMMA coated graphene/copper. Backside graphene is removed via floating on 30% Nitric acid solution for 30 seconds. Copper was then etched away via ammonium persulfate in an identical process to that being done for a wet transfer method. After the bottom-face of the stamp was rinsed in water, it was dried via a nitrogen gun and then placed on the target substrate with graphene facing downward. The whole assembly was then placed on a hot-plate of 180°C for 45 minutes. The stamp was then gently peeled off, leaving graphene/PMMA on the substrate. Removal of the PMMA was then followed in a similar process to that explained earlier in 4.5.1. The optical images in Figure 4.48 demonstrate examples of the transferred graphene film on a target silicon substrate. It is apparent that the transferred graphene films in both cases are comprised of a large amount of wrinkles that is known to deteriorate electrical properties of graphene such as carrier mobility. These defects including wrinkles act as charge carrier scattering sites. Furthermore, deterioration of the graphene film into small segments was often observed as shown in Figure 4.48 (b). The inset is the optical image of the sample before PMMA removal, pointing towards the fact that the damage was not initiated in the PMMA-removal stage.

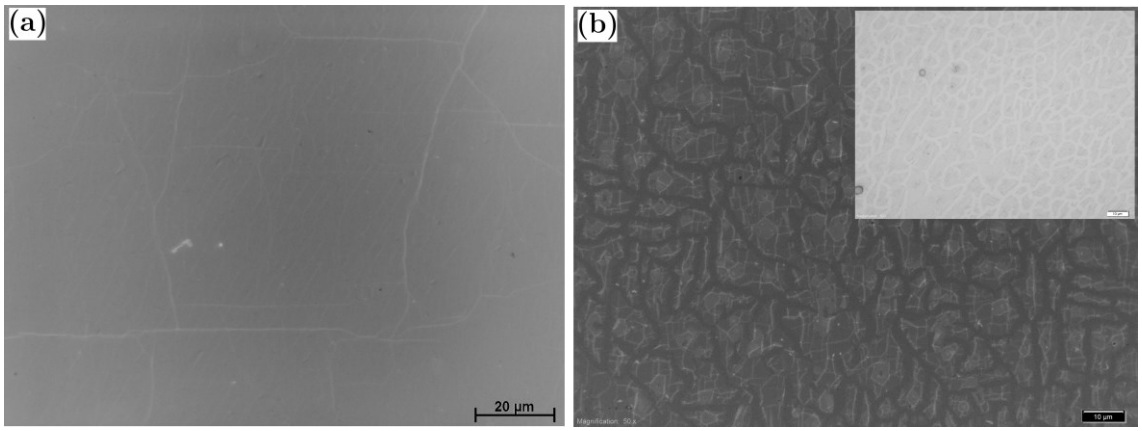


Figure 4.48. Graphene transferred via the dry transfer technique onto silicon substrates with (a) 300nm SiO_2 and (b) 90nm SiO_2. The inset showing the sample before removal of PMMA. (Scale bar 20 µm)

4.6 DC and Microwave Characterisation of FET Structures

After successful optimisation of the graphene transfer process, graphene field effect devices are fabricated. Construction of such devices require extreme level of precision. Care must be taken in order to ensure that the large-area graphene layer does not come into contact with sides of the substrate and that it does not become contaminated during the measurements.

4.6.1 Fabricating Electrical Contacts

In order to characterise the fabricated G-FET devices at both the DC and the Microwave frequencies, electrical contacts are needed to be made to the samples. It is known that in order to achieve a low contact resistance (contact resistance$< 10^{-5}$ $\Omega.cm^2$) [165], as well as a good contact adhesion with surface of graphene, few nanometres of titanium accompanied with a thin layer of gold is essential. In fact, it has been shown that 50 nm gold/10 nm titanium stack on graphene followed by annealing at about 450°C can result in a resistivity value of as low as 10^{-7} $\Omega.cm$. [165] An example of a Van der Pauw geometry with 50 nm gold on 10 nm titanium contact sputtered through a shadow mask is shown in Figure 4.49. As discussed in 3.2.1, four-point resistance measurement is known to be more accurate when compared to the two-point I-V analysis.

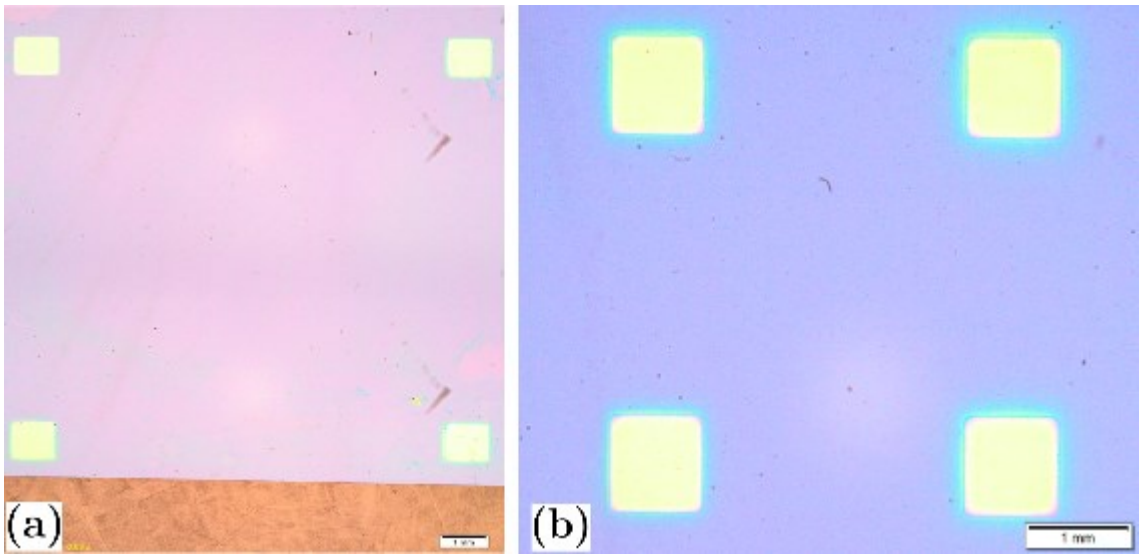


Figure 4.49. Optical micrograph of the 50 nm Au/10 nm Ti contacts sputtered on graphene that was transferred on (a) silicon with 90 nm SiO_2 and (b) silicon with native oxide. (Scale bars are 1 mm)

This method of realizing electrical contacts to graphene has been shown to be very reliable. However, for the large-area samples in this thesis with sheet resistance values ranging from 1 kΩ to 15 kΩ, simple silver paste drops are employed to achieve electrical contacts with surface of graphene. The difference in resistance measured via the two methods typically lies within 40 Ω.

4.6.2 Trials of Patterning the Bottom-Gate Electrode

It is a common practice to use a cut side of the silicon substrate for obtaining an Ohmic contact with silicon. However, patterning and etching the silicon oxide on the surface of the silicon substrates and then fabricating the electrical contact on the top would provide a more reliable method of accessing silicon as the gate electrode. Otherwise the side of the silicon substrate is needed to be scratched before making electrical contact to it, which has the risk of breaking the substrate.

Early on in this work, it was decided to fabricate bottom-gate electrode contact of the G-FET devices on the top surface. It was done by pattering the top surface via photolithography. Ultraviolet (UV) photolithography technique was employed to create rectangular patterns of the gate electrodes on the surface of silicon. To do

so, Hexamethyldisilazane (HDMS) was dispensed on the substrates to provide a better adhesion for the positive photoresist (A2 5214E). Standard photolithography procedures as shown in Figure 4.50 were followed and the desired rectangular pattern was achieved.

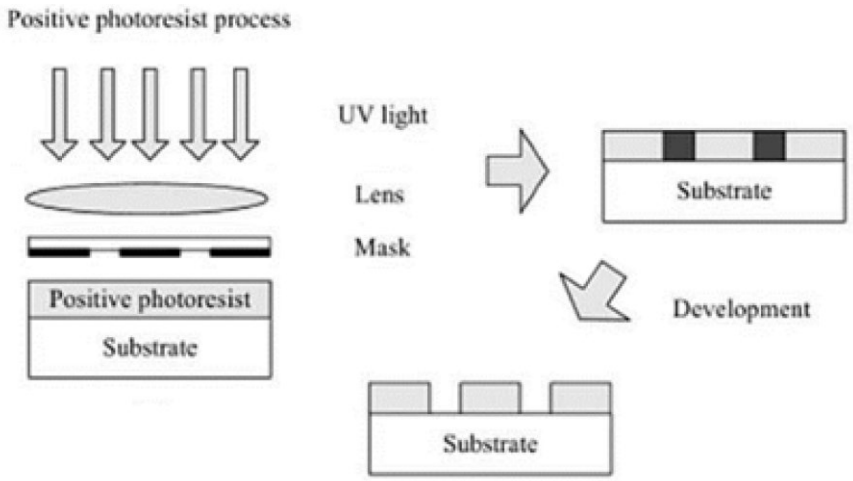


Figure 4.50. Schematics that is illustrating a step by step procedures of a typical UV-lithography method that utilises a positive phortoresist. [166]

Reactive ion etching (RIE) was subsequently used to etch the silicon dioxide from silicon. CF_4 gas was employed as an etchant gas where 40 sccm of CF_4 was supplied at the pressure of 100 Pa and RF bias of -50 V to result in a measured etch rate of 14 nm/min. It was carried out for 8 minutes and 2 minutes aiming for complete removal of 90 nm SiO_2 and the native oxide respectively. Samples were then immediately placed in the vacuum chamber of the sputtering system for deposition of the 50 nm Au/10 nm Ti electrical contacts. Upon completion of the contact deposition, photoresist was simply removed by acetone. After successful realization of the gate-electrode contact and in the final stage of device preparation, graphene was transferred on the substrates and the source and drain electrical contacts were made to graphene via sputtering as explained in 4.6.1. Figure 4.51 illustrates the optical images of the typically achieved source, drain, and gate contacts for the fabricated G-FET devices.

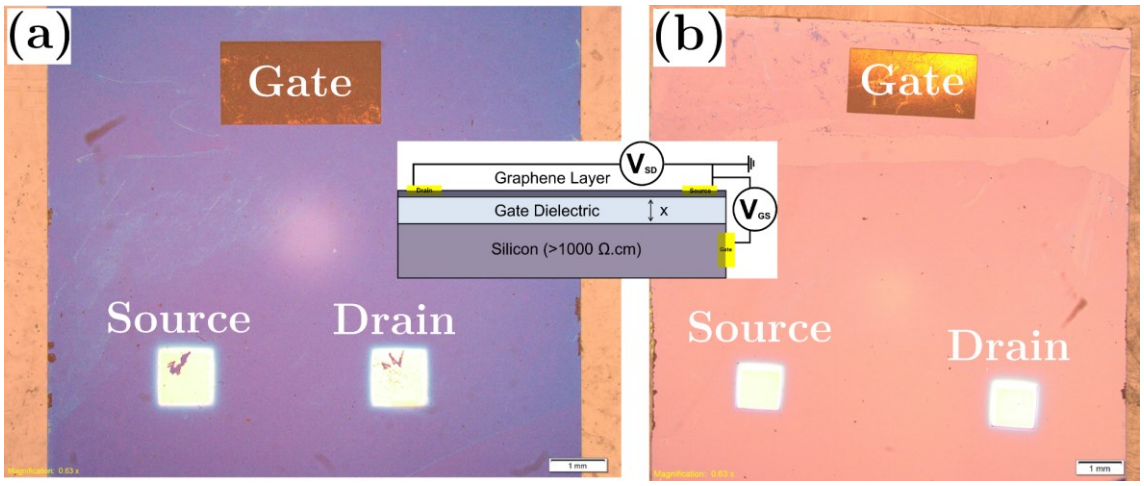


Figure 4.51. The electrical contacts of the fabricated G-FET devices made by employing UV-lithography, reactive ion etching, and sputtering processes. (Scale bar is 1mm)

The source-gate resistance was monitored after fabrication of each device to ensure that the insulating layer has remained leakage-free. It was however found that all 34 fabricated samples were damaged and there was a short circuit that was detected between graphene and the silicon substrate. The obtained I-V characteristics between source and gate electrode that is presented in Figure 4.52 compares an example of a FET device with a defective gate insulator to a leakage-free G-FET. As can be seen, the current between source and gate (I_{GS}) rapidly increases in the defective sample as the voltage between the electrodes (V_{GS}) is increased. It then becomes comparable to the current in the graphene channel that results in a lack of control over resistance switching of the device.

Therefore, due to the inconsistency of the lithography prepared contacts to silicon, it was decided to make contacts to silicon by scratching the side of the substrate and placing the electrical contact over the scratched area to avoid breaking of the gate insulator (red line in Figure 4.52). The source and the drain contacts are also made to the surface of graphene via silver paste drops. Samples are then annealed under 200 sccm argon flow at the temperature of 200°C for 60 minutes. This is done to reduce the amount of trapped charge carriers at graphene-insulator interface and to subsequently shift Dirac voltage of the graphene towards the zero.

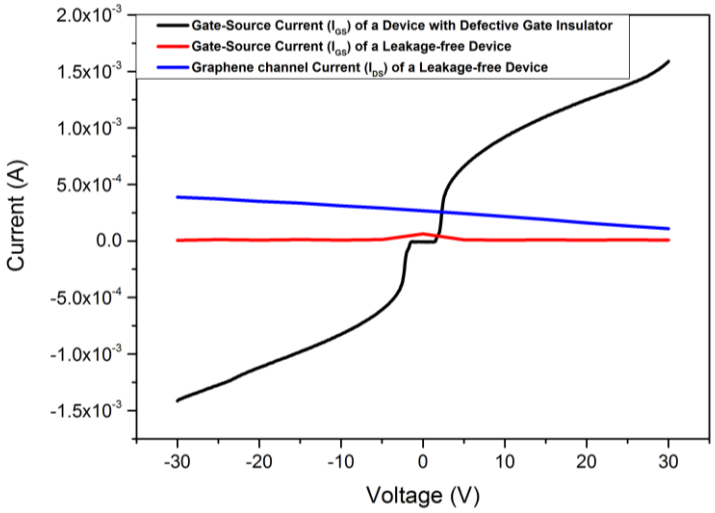


Figure 4.52. The I-V electrical characteristics of a leakage free G-FET device compared to a defective one.

4.6.3 Measurement Configurations

The DC and microwave characterisation of the built G-FET devices can be done separately and then compared to one another. However, in order to improve the accuracy of the comparison between the two measurements and avoid hysteresis at a given cycle, a robust measurement setup was developed, where both DC and microwave field effect measurements could be performed simultaneously and. This was then followed by an instant data analysis that was coded in the developed script. As can be seen in Figure 4.53, the device under test is placed on the copper cavity over the 5mm aperture. The previously made electrical contacts are connected to the test leads via a very small quantity (a single drop) of silver paste. Test leads effectively connect the source, drain, and gate terminals on the device to the dual channel Sourcemeter unit. The microwave setup is connected to the *VNA* via thick microwave coaxial cables. Both the *VNA* and the Sourcemeter are connected to a single computer to allow for simultaneous control of both systems. In collaboration with Dr Hanham and using the Q-factor extraction code developed at NPL [167], a Matlab script was developed in which both the Sourcemeter and the *VNA* could be controlled and measurements could be performed simultaneously.

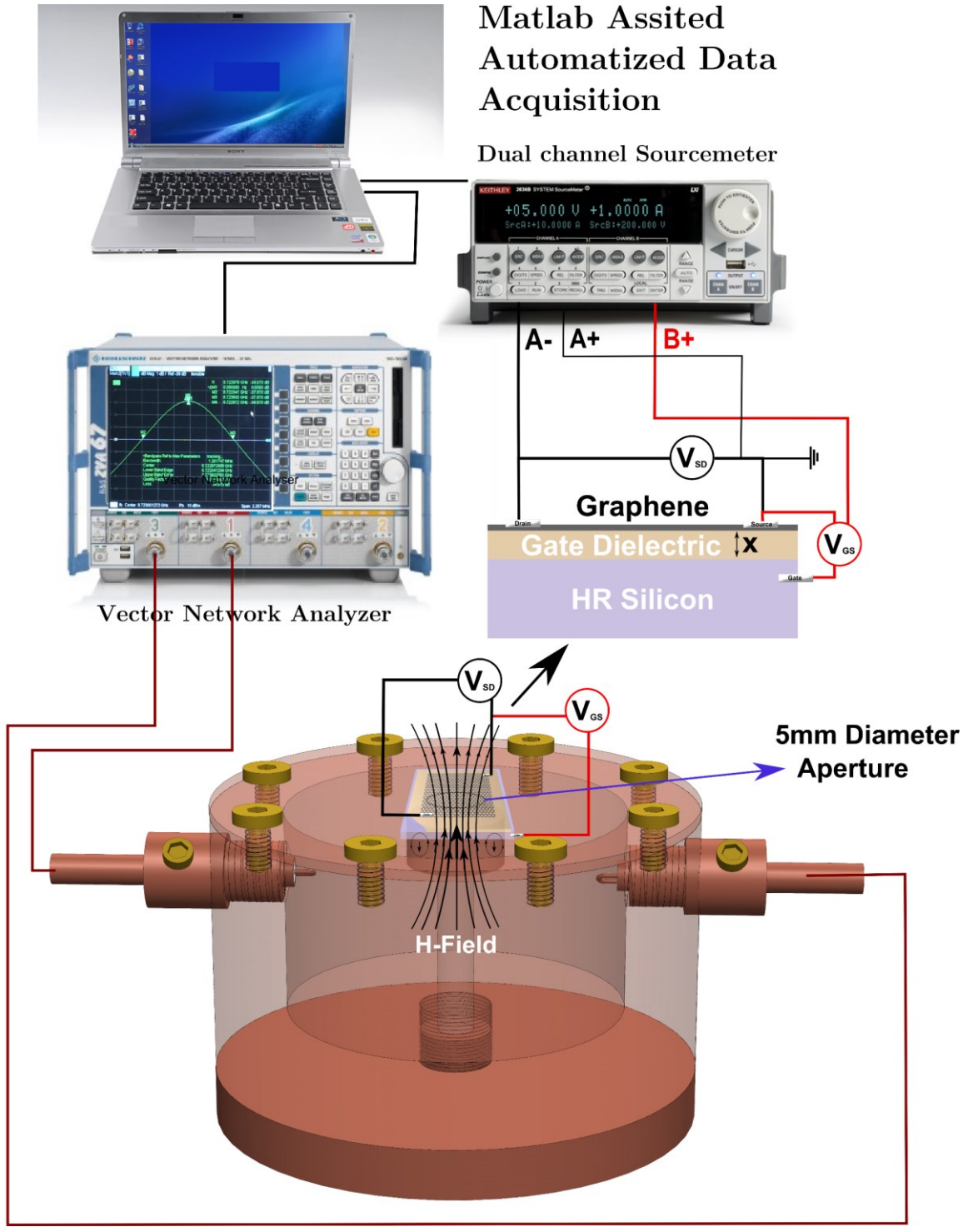


Figure 4.53. The developed experimental setup of the dual DC-Microwave field effect measurements.

4.6.4 DC and Microwave Transport Curves Extraction

As briefly mentioned in 3.2.1.1, the field effect measurements at DC is carried out following the same procedures explained in chapter 2.3. Sheet resistance in the graphene is measured as a function of gate voltage (V_{GS}), where a fixed voltage of

200 mV is applied between source and drain electrodes (V_{SD}) and current in the channel (I_{SD}) is measured at every gate voltage point. Application of voltage between the source and the gate (V_{GS}) results in an electric field between graphene and silicon which leads to a subsequent alteration of the current in the graphene channel (I_{SD}). The potential gate leakage current is also taken into account via the Kirchhoff's law. For simplicity, only the measured current between the source and the two electrodes on graphene are considered. Resistance of the channel at every gate voltage point is calculated via Eq. 4.1 and it is then used to calculate resistivity and then the conductivity of the graphene channel as a function of the gate voltage via Eq. 2.14 and Eq. 4.2 respectively.

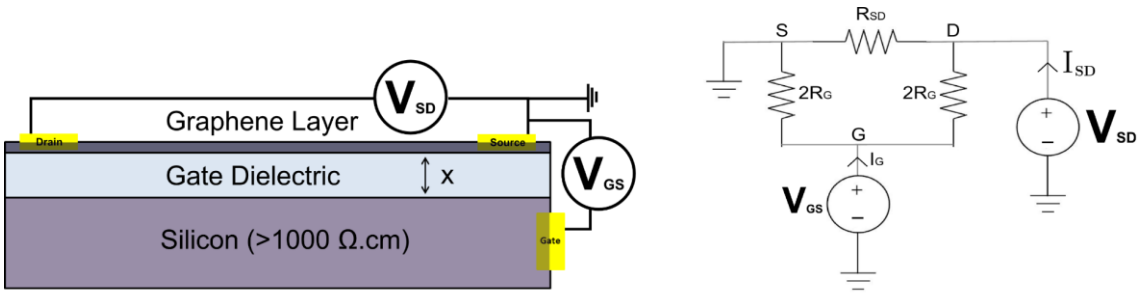


Figure 4.54. Wiring scheme and equivalent electrical circuit associated with a typical G-FET structure.

$$R_{SD} = \frac{V_{SD}}{I_{SD} + \left(\frac{V_{GS} - V_{SD}}{2R_G}\right)} \tag{4.1}$$

$$\rho = \frac{R_{SD}.w.t}{l} \tag{4.2}$$

where w, l, and t denote width, length, and thickness of graphene. On the other hand, the microwave field effect measurement is carried out by inducing current in the graphene film by exposing it to the evanescent field that leaks through the designated 5 mm diameter aperture, as explained in 3.2.3. The field in the microwave resonator is excited via the coupling loops that are situated inside the cavity where the coaxial cables are connected to the *VNA* (Figure 4.53). The CST Microwave Studio simulations were performed to estimate the resonant frequency of the dielectric resonator and to optimise the distance of the loops from dialectic

puck for achieving a reasonable coupling along with a sensitive Q-factor. They were also used to confirm that the chosen operation mode is $TE_{01\delta}$ mode. The input dimensions and materials properties were set to be identical to the real physical parameters of the system. Frequency domain solver was chosen for these simulations to achieve more accurate results. It is important to note that the peak power input in the simulations is set to 1 W, whereas in the actual measurement, VNA's peak power is set to 10 dB which is equivalent to 0.01 W. Linear nature of the measurements coupled with the mentioned peak power of 0.01 W means that the scales shown in the simulations are 100 times smaller in the actual measurements (i.e. current density of 1 A/m translates to 10 mA/m). The plot in Figure 4.55 compares the resonant frequency of the resonator at different coupling loop-cavity wall distances. It is apparent that a strong coupling is achieved when the loops are in close proximity of the resonator. Reducing the coupling strength by moving the loops further away from the resonator, not only results in a higher Q-factor, but also resolves the double-peaks into a single resonance. The simulations reveal that coupling loops ideally need to be placed 20 mm into the cavity measuring from the wall of the cavity.

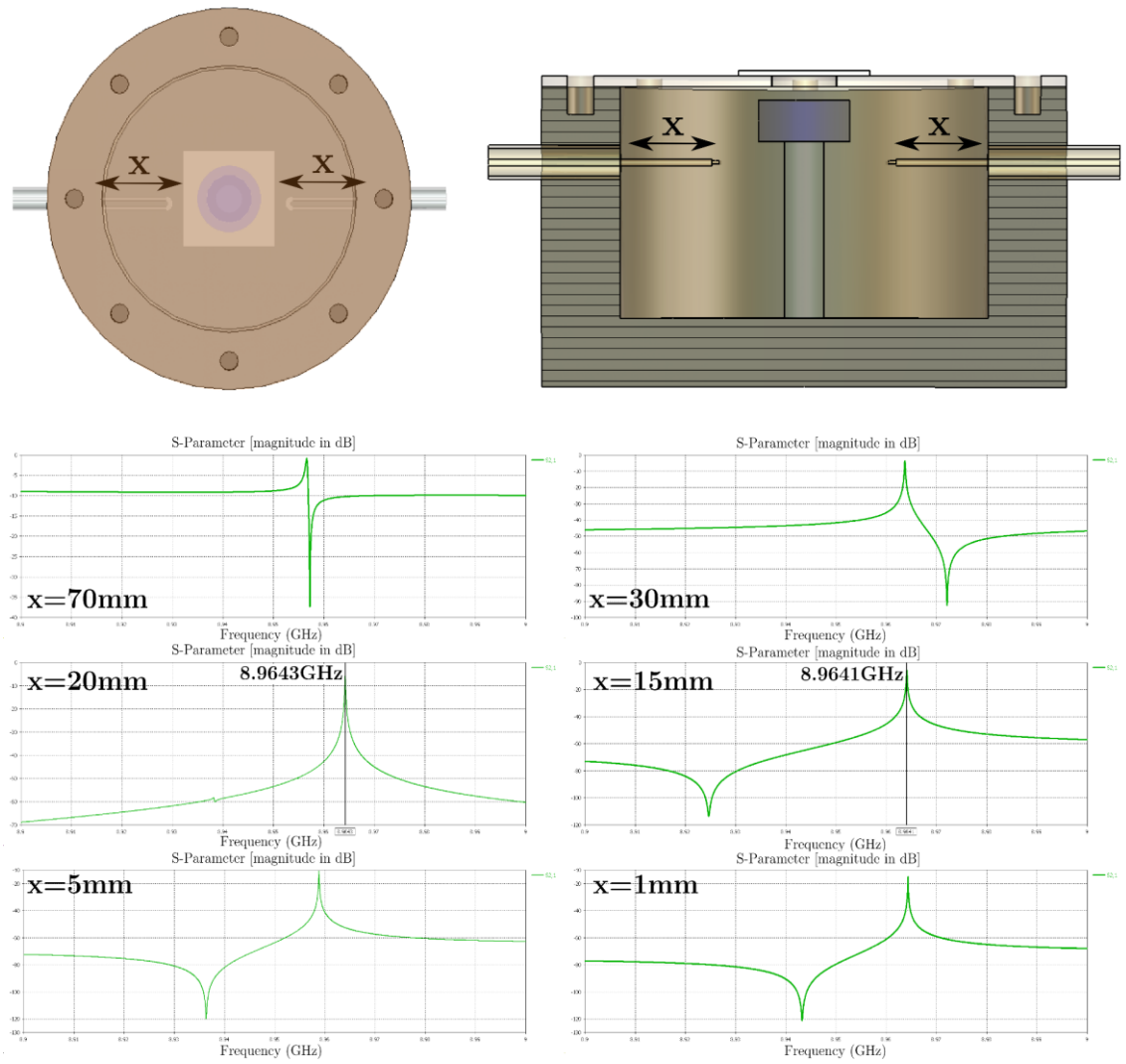


Figure 4.55. Frequency domain solver simulation results for the resonant frequency change upon changing coupling loops distance, x, from cavity's wall.

Upon finding the resonant frequency of the resonator, the simulation was repeated and both the electric and the magnetic fields as well the current density distribution in the cavity were monitored, this time at the ideal resonant frequency of 8.9643 GHz. In-plane electric field lines with no vertical components as presented in Figure 4.56a confirm that the chosen resonant mode does correspond to the transverse electric $TE_{01\delta}$ mode of the dielectric resonator as described in 3.2.3. The field lines decay exponentially through the aperture as they move away from the resonator. As apparent in Figure 4.56c-d, the field lines penetrate through the high resistivity silicon substrate. They will then interact with the graphene sample and

result in excitation of a high frequency circular current parallel to x-y plane in the graphene film. Figure 4.56e reveals the generated current density in graphene upon its interaction with the evanescent field.

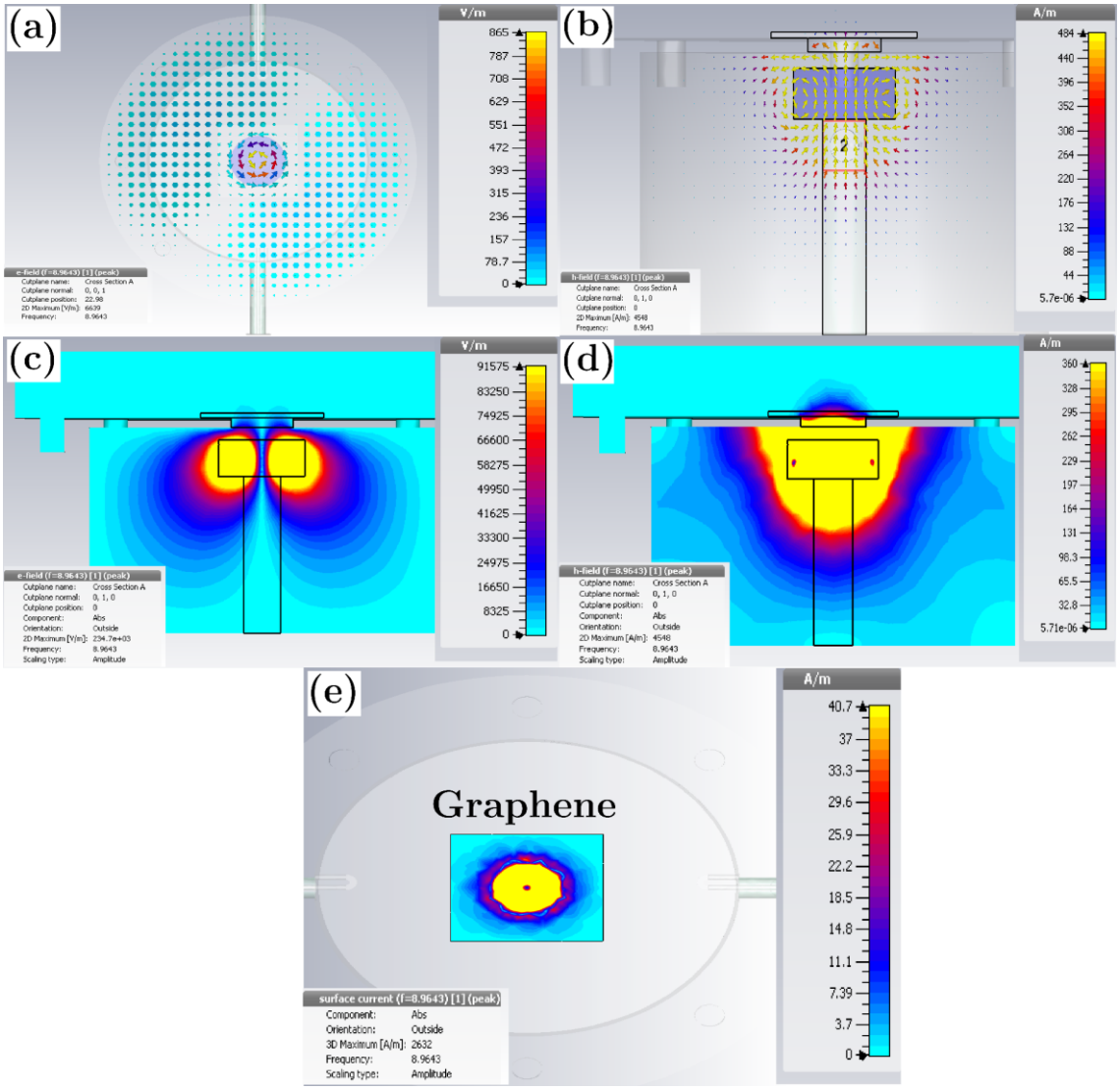


Figure 4.56. The frequency domain microwave simulation at resonant frequency of 8.9643 GHz that revealed the distribution of (a) & (c) electric field, (b) & (d) magnetic field in the cavity and (e) surface current density in the graphene layer.

Furthermore, variation in resonant frequency of the resonator was investigated while varying distance of the puck from the aperture as shown in Figure 4.57b. Experimental observations showed that resonant frequency and Q-factor of the resonator occur at about 8.72 GHz and 9250 respectively (Figure 4.57a).

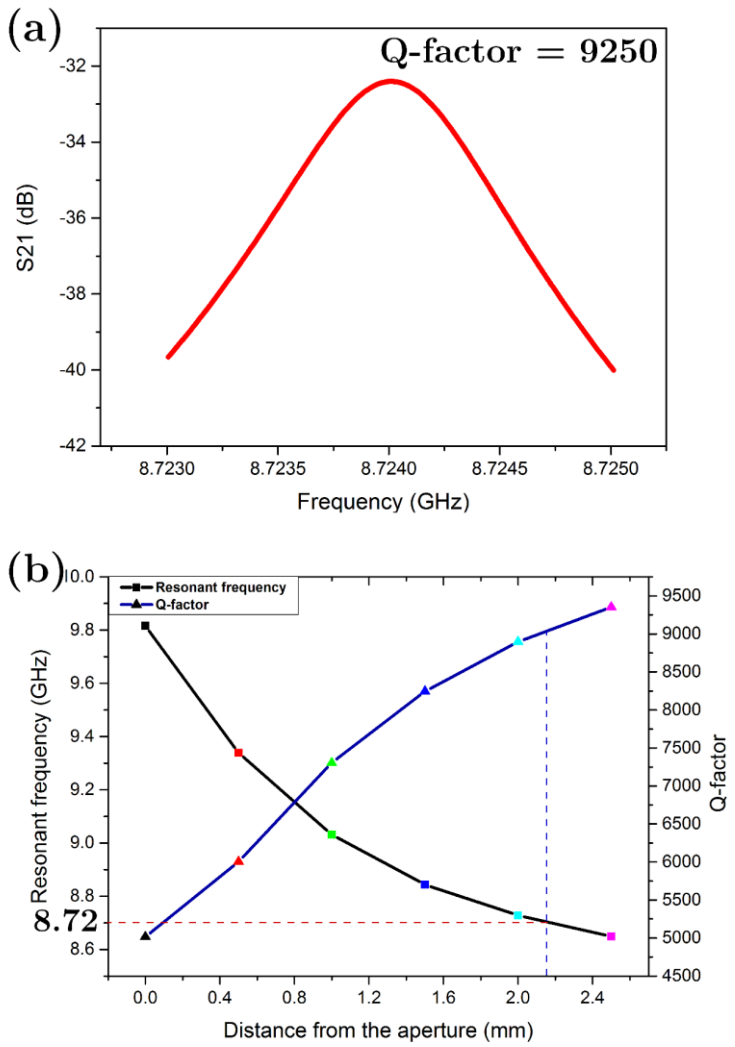


Figure 4.57. (a) The experimentally observed resonant frequency and Q-factor of the resonator compared to (b) CST Microwave Studio simulations results showing the variation of resonance frequency depending on the vertical position of the puck.

The increasing trend of the Q-factor when moving away from the aperture is directly correlated with the fact that losses to the cavity walls as well those through the aperture drop and result in a higher amount of energy concentrated in the puck, hence the resonator will have a higher Q-factor associated with it.

The microwave field effect measurements are carried out by placing the G-FET structure over the 5mm aperture as previously shown in Figure 4.53 and also presented below in Figure 4.58 below. Application of V_{GS} results in alteration of the Q-factor of the resonator as a result of the carrier concentration modulation in graphene. The Q-factor at each gate voltage ($Q(V)$) is then translated into sheet

resistance as a function of the gate voltage ($R(V)$) via Eq. 4.3 that is derived from Eq. 3.19. The minimum sheet resistance occurs at the minimum Q-factor and can be deduced from Eq. 4.4.

$$R(V) = \frac{Z_C}{\frac{1}{Q(V)} - \frac{1}{Q_S}} \tag{4.3}$$

$$R_{min} = \frac{Z_C}{\frac{1}{Qmin} - \frac{1}{Q_S}} \tag{4.4}$$

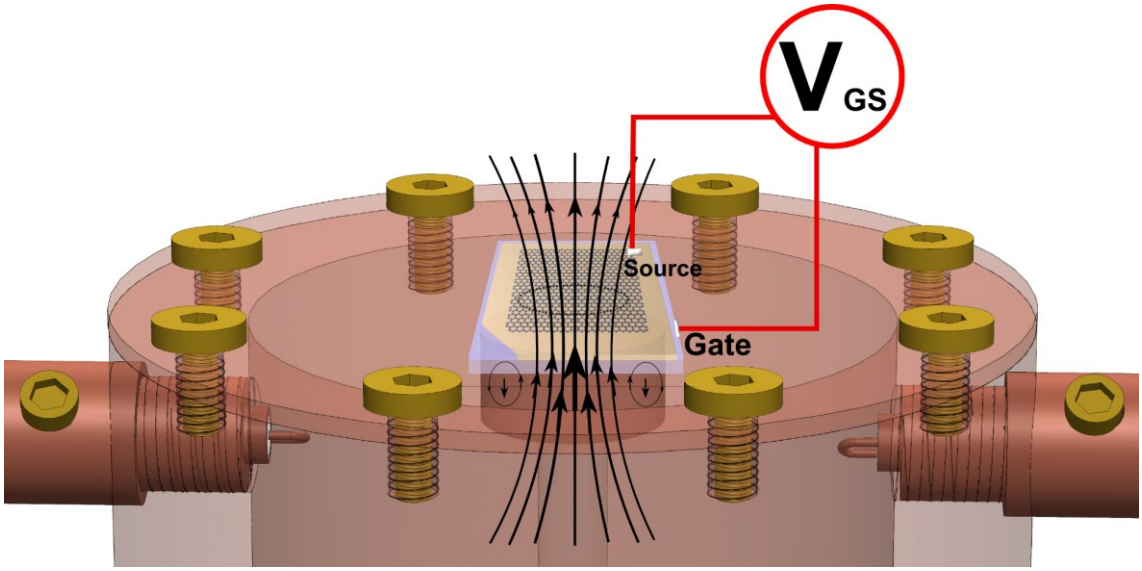


Figure 4.58. Microwave field effect measurement setup.

Further, based on Eq. 4.3 and Eq. 4.4, the ratio of sheet resistance at a given voltage to the minimum sheet resistance ($R(V)/R_{min}$) can be represented via Eq. 4.5, where the calibration factor Z_C no longer plays a part.

$$\frac{R(V)}{R_{min}} = \frac{Q(V)(Q_S - Q_{min})}{Q_{min}(Q_S - Q(V))} \tag{4.5}$$

The maximum value of this ratio essentially represents the highest switching ratio of a given G-FET device. Similar to the DC method that was described in 3.2.1.1, the mobility of the charge carriers for each device at microwave frequencies can also be calculated from the transport curves (R_S *vs* V_{GS}). Step by step sheet resistance extraction procedure from the microwave transmission data is presented

in Figure 4.59 where one of the graphene/nSiO$_2$/HRS FET structures is chosen as an example.

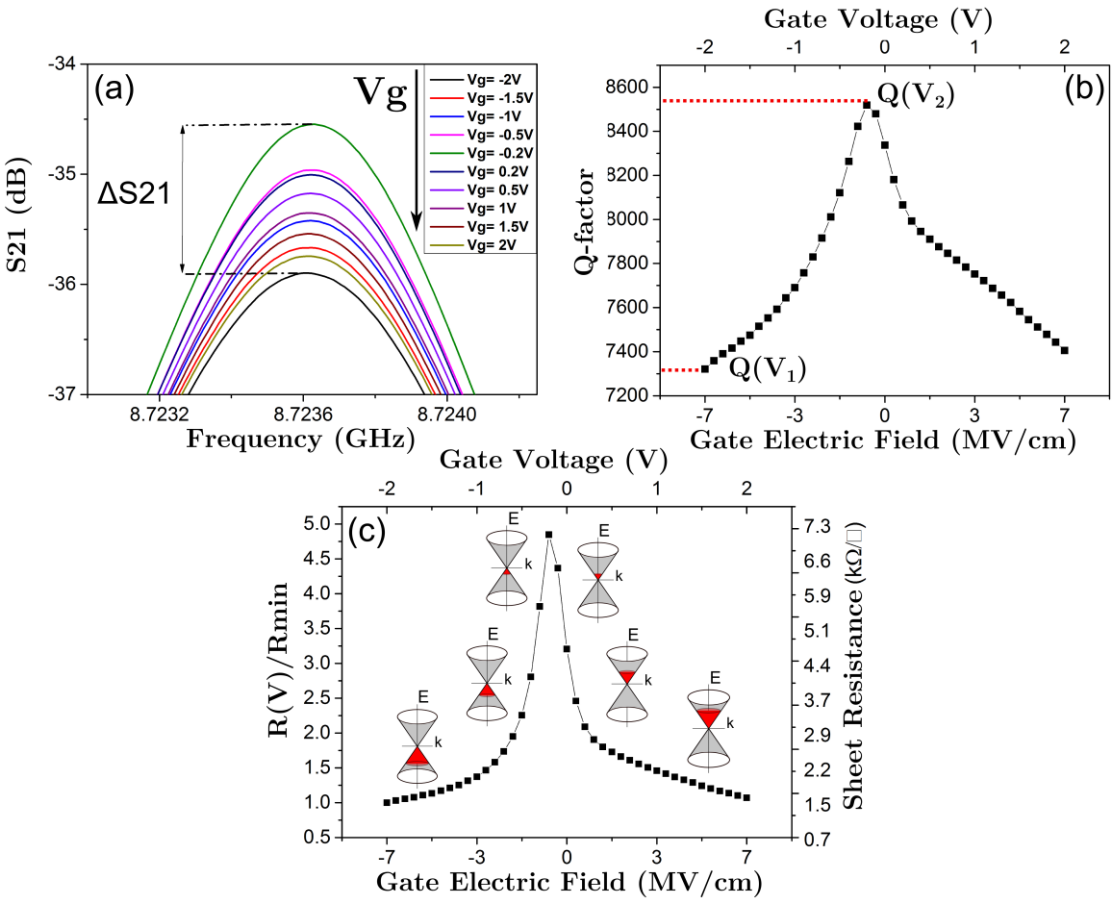


Figure 4.59. The step by step procedure of extracting the transport data from the microwave transmission curves. (a) The transmission measurements at each gate voltage and (b) the Q-factor from the measured gate-voltage dependant resonant curves and subsequently calculate (c) sheet resistance of graphene at a given gate voltage. [189]

It is important to note that the typically achieved modulation depth of 2.1 dB (Figure 4.59a) with HRS substrates is not representative of the maximum achievable modulation depth for a graphene-modulated device. This is merely because the silicon substrate still significantly contributes to the resonator losses. Denoting the switching ratio β in Eq. 4.6 which is derived from Eq. 4.5, a measured β of 5 would result in a modulation depth (ΔS_{21}) of 14 dB for an optimized structure where graphene entirely dominates the losses, i.e. where substrate and other cavity losses are negligible so that $Qs \rightarrow \infty$ and $A(Q,V) \rightarrow 1$ in Eq. 4.6.

$$\beta = \frac{R(V_1)}{R(V_2)} = \frac{Q(V_2)}{Q(V_1)}\left(\frac{1-\frac{Q(V_1)}{Qs}}{1-\frac{Q(V_2)}{Qs}}\right) = 10^{\frac{\Delta S21}{20}} A(Q,V),$$

$$A(Q,V) = \frac{1-\frac{Q(V_1)}{Qs}}{1-\frac{Q(V_2)}{Qs}} \tag{4.6}$$

In the next chapter the extracted data from the microwave cavity method will be compared to those obtained from the DC technique and the characteristics of the fabricated G-FET devices will be discussed.

4.7 Summary and Conclusion

This chapter focused on presenting the systematic procedure of fabricating graphene layers by using both horizontal and vertical CVD systems. Detailed analysis of the grown graphene layers was presented and they were compared to the graphene sheets that were purchased from commercial sources. The vertical CVD system yielded wafer scale graphene films on copper which significantly reduced the need for purchasing graphene from external sources. However, there are still slight improvements needed to enhance the roughness of the used copper films such as exploiting electropolishing. Optimisation of the transfer process of graphene on a given substrate was also demonstrated. Transfer of graphene proved to be one of the most challenging steps of the FET device fabrication process. Factors such as cleanness of the transfer environment, the type of solvent, pre-transfer treatment of the substrate, and thickness of PMMA were found to play important roles. The step by step fabrication procedure of the graphene based field effect devices was presented. It was found that making large area contacts to silicon substrate via photolithography and REI processes did not result in consistent leak-free samples. The use of silver paste on the side of the substrate was found to be a more effective approach. Lastly, the measurement system development for

characterizing the fabricated G-FET devices at both the DC and the microwave frequencies was represented and discussed. The main challenge of this stage was found to be connecting and controlling both the VNA and the Sourcemeter simultaneously via a single script on Matlab.

5. Results and Discussion 2: DC and Electromagnetic Data

Quality is never an accident; it is always the result
of high intention, sincere effort, intelligent direction
and skilful execution. "William A. Foster"

This chapter will expand on chapter 4 and will present the achieved electromagnetic data for the various fabricated FET devices. The validity of the microwave cavity characterisation technique will be discussed and comparison will be made to the measurements performed at DC. Effects of the gate dielectric-graphene interface on the field effect characteristics of the devices will be investigated. Moreover, performance of the FET devices with various dielectric materials will be presented. This chapter will conclude by presenting the first results for a self-gated graphene heterostructure based on sandwiching 50 nm Aluminium Nitride film between two single layer graphene films.

5.1 DC and Microwave Transport Data for Graphene-Insulator-HRS FETs

Graphene-insulator-HRS FET structures with seven different insulating materials were fabricated as described in 4.4. In this section, first the validity of the characteristic impedance that plays an important part in calculation of the microwave sheet resistance of graphene will be investigated. It will be followed by presenting the obtained DC and the microwave field effect data will be presented and analysed.

5.1.1 Validity of Z_C

In order to verify the accuracy of the extracted characteristic impedance that is obtained from the shift in frequency upon introduction of a substrate over cavity's aperture, the sheet resistance measurements at DC (using Van der Pauw geometry 3.2.1) were compared to $1/\Delta Q^{-1}$ data from the microwave measurements. This was carried out for 16 graphene samples transferred on quartz substrates. Introduction of the quartz substrate over the aperture results in f_r shift of about 460 kHz. Using Eq. 3.18 that was described by the perturbation theory (see 3.2.3.2), this frequency-shift results in Z_C of 0.107 Ω. On the other hand, the plot of DC sheet resistance versus "$1/\Delta Q^{-1}$" of all 16 samples is represented in Figure 5.1. The gradient of this plot, according to Eq. 3.19, is also equivalent to the characteristic impedance. As apparent from the plot, Z_C from the gradient calculation is extracted to be 0.102 Ω. This value is in good agreement with the extracted estimate by the perturbation theory. It therefore validates the characteristic impedance calculations in the microwave cavity technique.

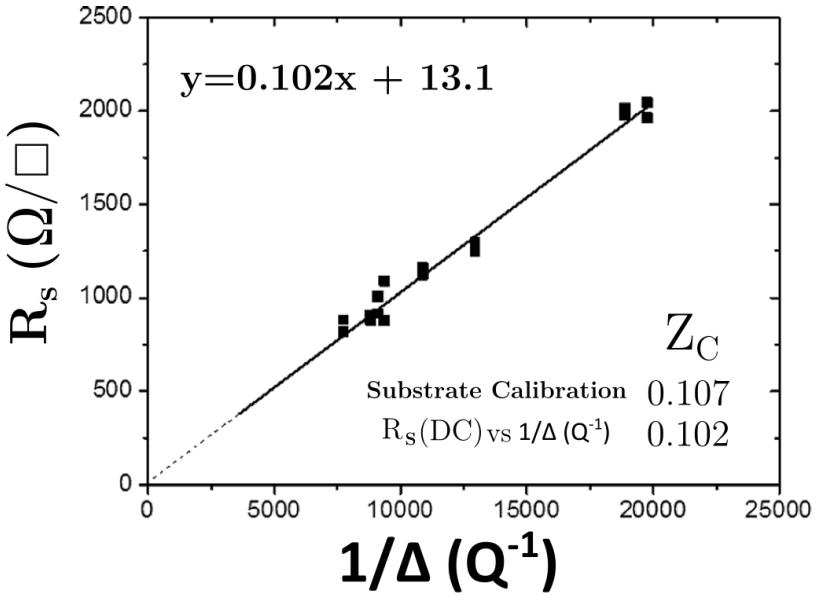


Figure 5.1. The sheet resistance values extracted from the performed four-point measurements plotted against the inverse Q-factor data obtained microwave cavity technique verifying the calculated substrate calibration factor Z_C. [135]

5.1.2 Sheet Resistance VS Gate Voltage, DC VS Microwave

As mentioned previously, the following insulating gate materials were chosen and employed: (1) Native SiO_2, (2) 300 nm SiO_2, (3) 80 nm YSZ, (4) 80 nm STO, (5) 50 nm STO/10 nm YSZ (6) 5 nm AlN and (7) 13 nm multilayer h-BN. The procedure of obtaining leak-free G-FET devices was established after unsuccessful fabrication of more than 50 devices that had high amount of gate leakage associated with them (gate-source current comparable to source-drain current). Although the fabrication procedure was optimised sample after sample, but the graphene film and the bottom silicon gate were consistently found to be short circuited in the first trails. Similar effect as to the sample shown in Figure 4.52 was observed. Factors such as graphene coming into contact with one of substrate's sides, adverse effects of substrate cleaning by strong oxygen plasma, mishandling of the substrates during slicing of the wafer as well as inadvertent scratch of the surface during the graphene transfer process were found to play major parts in damaging the $nSiO_2$ dielectric layer and causing a short circuit between the graphene and the bottom gate. After careful avoidance of the mentioned factors, a routine for fabrication of working FET structure was established. The DC and microwave sheet resistance of each device were found and plotted against the varying gate voltage as described in 4.6.4. More than 21 large-area (8 mm by 8 mm active area) devices with at least three devices for each of the seven described dielectric layers were fabricated and tested. Single layer graphene films from the same graphene growth batch was employed and identical transfer process as well as an identical post-transfer annealing was carried out for all samples to ensure subsequent unbiased comparative analysis of the results. The DC and microwave field effect measurements for all seven dielectric materials are presented in Figure 5.2.

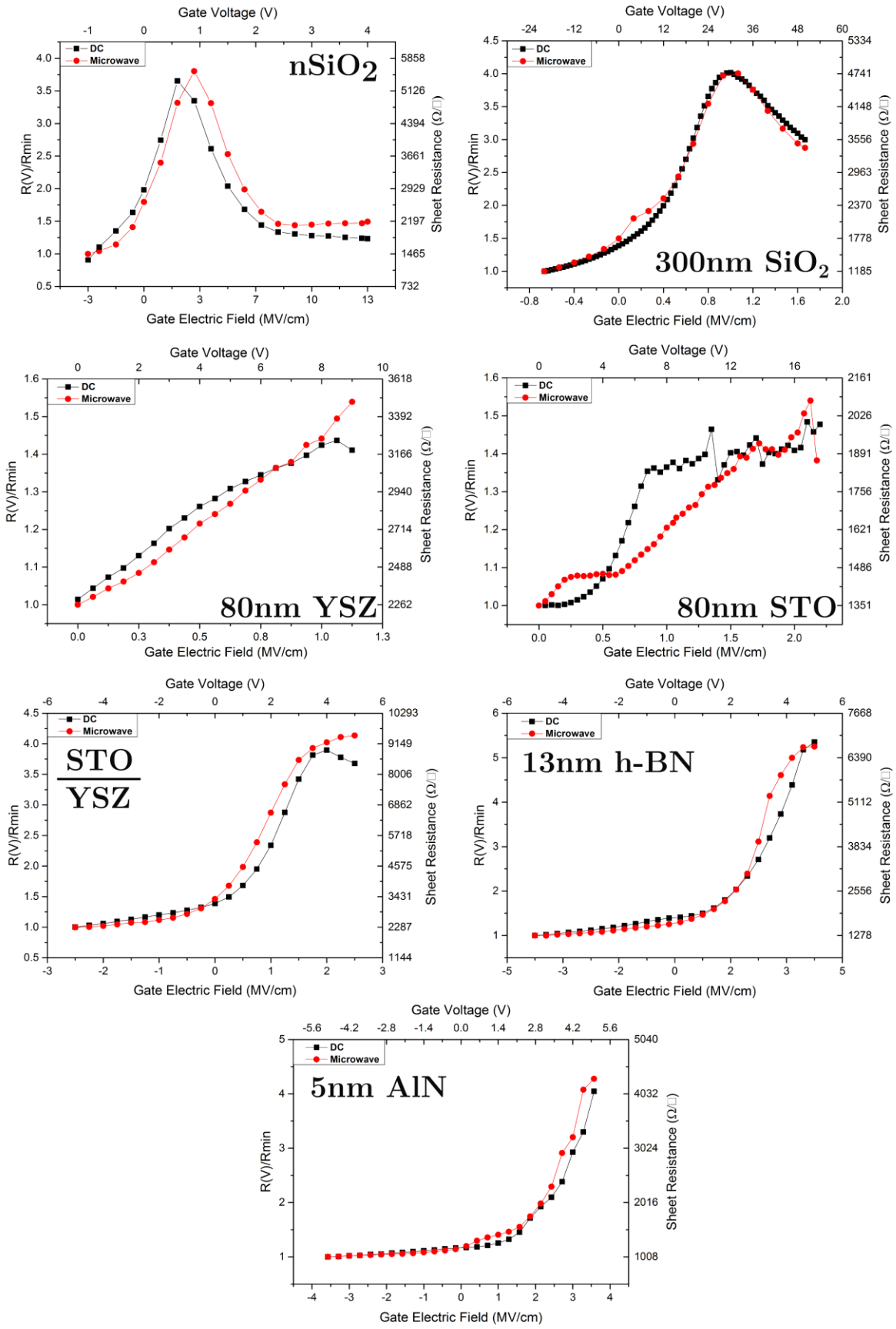


Figure 5.2. Comparison between the *DC* and the microwave field effect transport curves of the fabricated G-FET devices before annealing. [189]

The comparison between the DC and microwave data is indicative of a strong agreement between the two measurements for all the samples except for the device that incorporates 80 nm of STO as its dielectric gate material. It is noticeable, that the obtained microwave results for G-FETs with STO dielectric layer (Figure 5.2d) do not follow the one that is measured at DC. I reason that this difference is attributed to the properties of STO thin film when grown on $nSiO_2$. The coefficient of thermal expansion of STO is almost two orders of magnitude larger compared to that of $nSiO_2$, resulting in a significantly larger expansion during heating and greater contraction on cooling. This leads to a large number of defect sites upon disruption to the epitaxial growth when STO is grown over $nSiO_2$. A defective interface results in a significant amount of current leakage which can strongly affect both the DC and the microwave measurements. This is reflected in the DC measurements by the leakage current that affects the DC current in the graphene channel. The leakage is less influential in the microwave measurements, merely because leakage current would not interact with the high frequency current of the evanescent field. Instead, it results in a voltage drop between source and gate that is effectively equivalent to screening of the field. Therefore, presence of a buffer layer such as YSZ whose thermal expansion coefficient is closer to both SiO_2 and STO [168] is imperative in obtaining a defect-free STO film. This is achieved by minimising cracks and defects that arise from the difference in lattice constant and have significant leakage current associated with them. Moreover, drawing upon the XRD analysis on the grown STO films, the interplanar spacing of STO and YSZ were found to be 0.28 nm and 0.25 nm respectively (see 4.4.2). Assuming both films have a perfect cubic structure, this interplanar spacing translates into lattice parameters for each of the films. Figure 5.3 illustrates a (001) view of the lattice structure for $nSiO_2$, STO and YSZ structures. Lattice parameter values can then be used to calculate the degree of lattice mismatch between all three films. [169] The degree of mismatch (δ) between the lattices can be calculated via Eq. 5.1. [170]

$$\delta = 2(a_{STO} - a_{SiO2})/(a_{STO} + a_{SiO2}) \quad (5.1)$$

a_i denotes the lattice parameter of a given material.

The lattice mismatch is found to be 6% for STO on SiO_2 and 5% for YSZ on $nSiO_2$. The mismatch can also manifest itself as potential sites of defects where there is a missing atom at the growth interface. It is important to note the growth process can have more complexities associated with it as for instance a plane of atoms may also rotate diagonally and be strained to adapt to the growth and subsequently secure the most stable state with the underlying material's geometry.

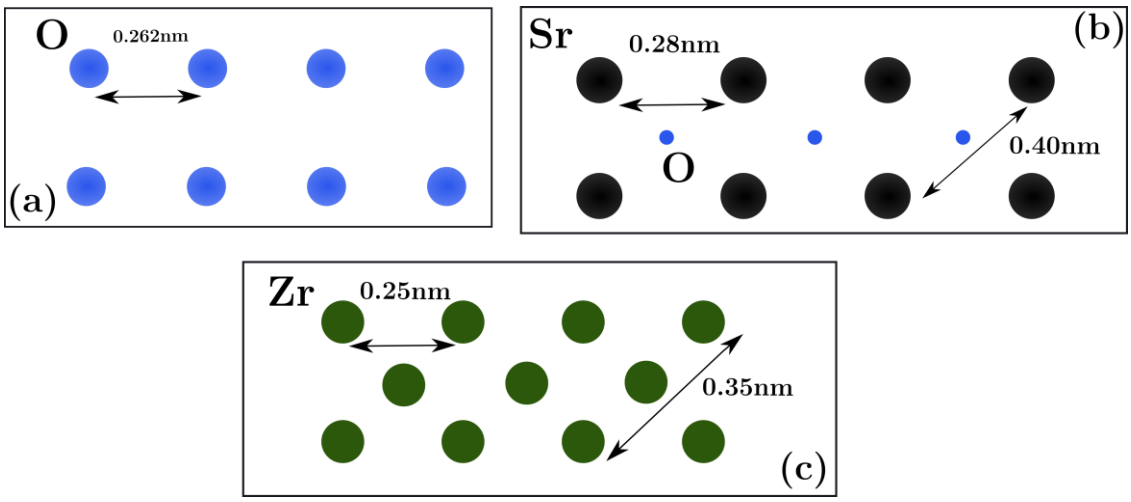


Figure 5.3. The (001) plane view of lattice structure of (a) SiO_2, (b) $SrTiO_3$ and (c) YSZ.

One of the other key outcomes of the measurements is the fact that the charge neutrality point of the devices is either not reached for most of the devices or when reached, it occurs at a relatively high applied electric field. As demonstrated in Figure 5.2, the annealing process under argon atmosphere at 250°C for 2h has helped with removal of the trapped interfacial charges and carrier puddles, resulting in shifting of the CNP towards zero gate voltage. This is in agreement with the similar works done by Stolyarova et al. [171] and Schedin et al.. [172]

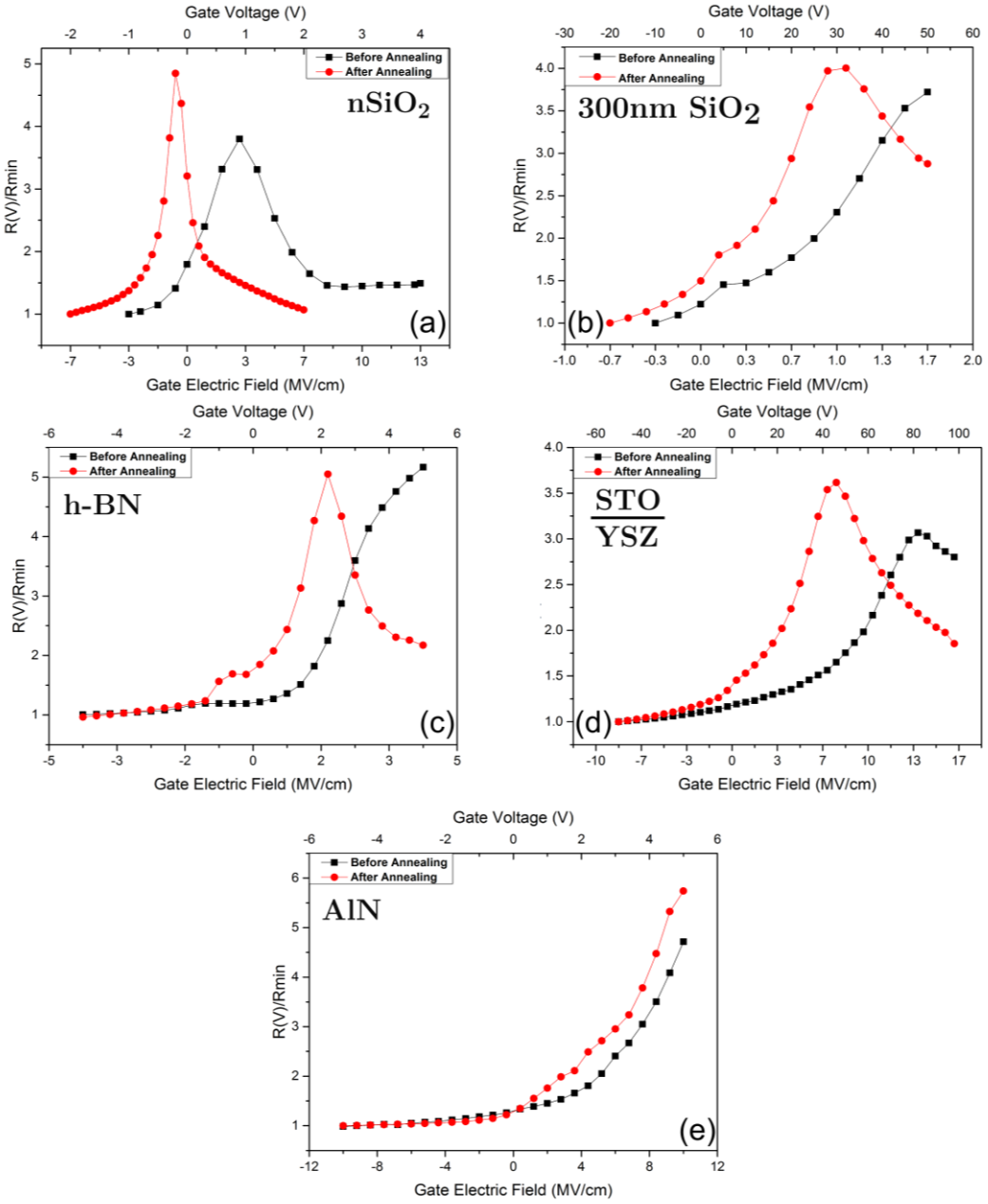


Figure 5.4. Impact of annealing at 250°C for 2h under 200 sccm argon flow on switching ratio of each of the G-FET samples.

Although identical fabrication procedure was followed for every sample, but it was found that the charge neutrality point for samples varied. On the other hand, mobility and on-off ratio of the samples with same dielectric gate material remained unaffected. Figure 5.5 compares three different G-FET samples on the same dielectric layer of $nSiO_2$. It is apparent that a consistent on-off ratio of approximately 4.9 is achieved, however Dirac points vary by ±2 V. This is

correlated with the external unintentional doping of the graphene film via the substrate over which it lies. Although annealing has helped with desorption of the charge adsorbents, there still exists a certain amount of trapped charges at the interface that leads to CNP variation between the samples.

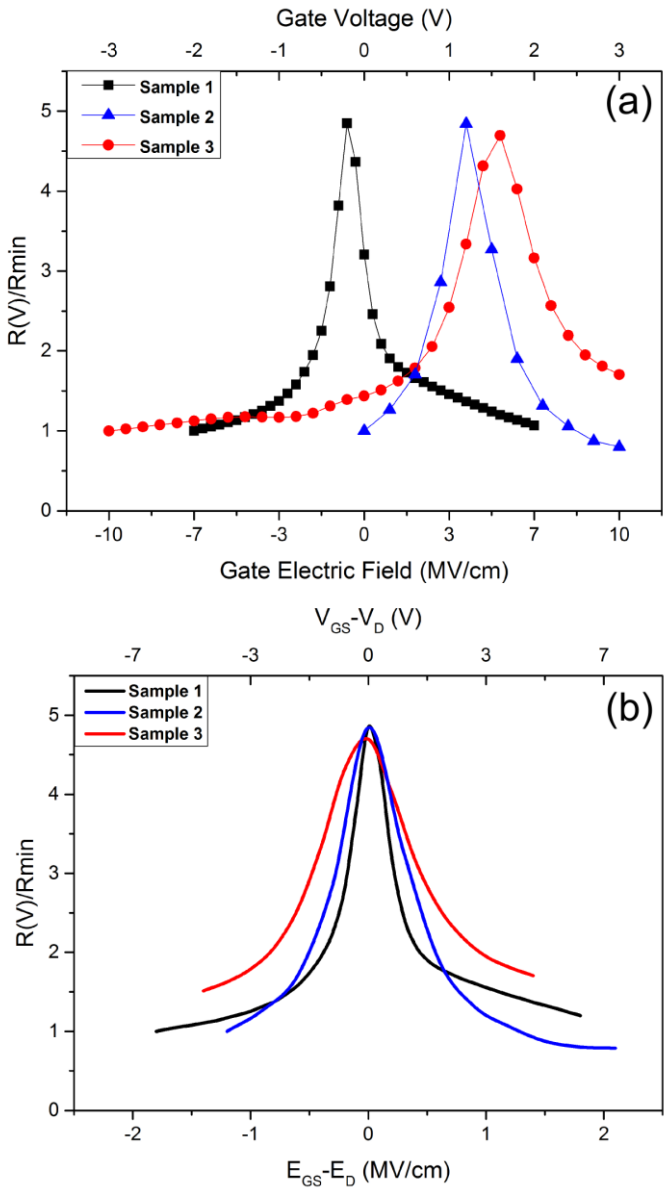


Figure 5.5. (a) Comparison of CNP of three G-FET samples on $nSiO_2$ on HRS. (b) Identical plots upon shifting Dirac points to zero electric field indicative of a consistent achievable switching ratio of about 5.

5.1.3 Hysteresis of Transport Curves

A high degree of hysteresis was initially observed in the measured field effect data (both DC and microwave) of the fabricated G-FETs. Figure 5.6 demonstrates how

the hysteresis in the measurement disappears as the sweep time per gate voltage point is decreased from 200 ms to 50 ms to execute measurements at a more rapid pace. It is apparent that both the electrostatic and the chemical environment affect the field-effect response of G-FET devices similar to FET devices based on carbon nanotubes. [173] If a single gate voltage point is considered, 2 V for instance, it is apparent that resistance at this point increases with increasing the sweep time. This effect can be explained by considering the trapped states, which will have time to reach their quasi-equilibrium state at a given gate voltage and result in less current instability in the channel. Sweep time for the measurements is therefore set to 200 ms to avoid hysteresis.

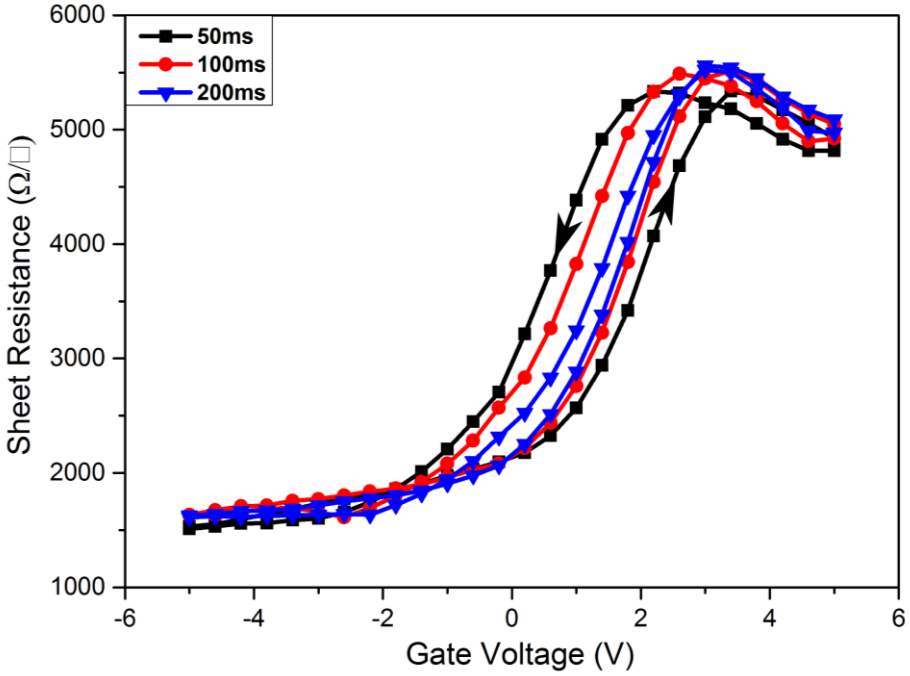


Figure 5.6. Gate voltage response a G-FET at different sweep time per gate voltage point values.

5.1.4 Experiment vs Theory

In order to gain more insight into the obtained experimental results, field effect data are compared to the theoretical fit model that is developed in Boltzmann's framework (described earlier in 2.3). Comparison between the transport curve obtained experimentally for G-FET with nSiO2 dielectric and the theoretical fit

can be seen in Figure 5.7a. The conductivity values are presented as a function of the widely accepted minimum conductivity of graphene ($4e^2/\pi h$). [174] The fitted plot is used and the mobility, on-off ratio, scattering time for both electrons and holes, as well as the intrinsic carrier concentration values were extracted.

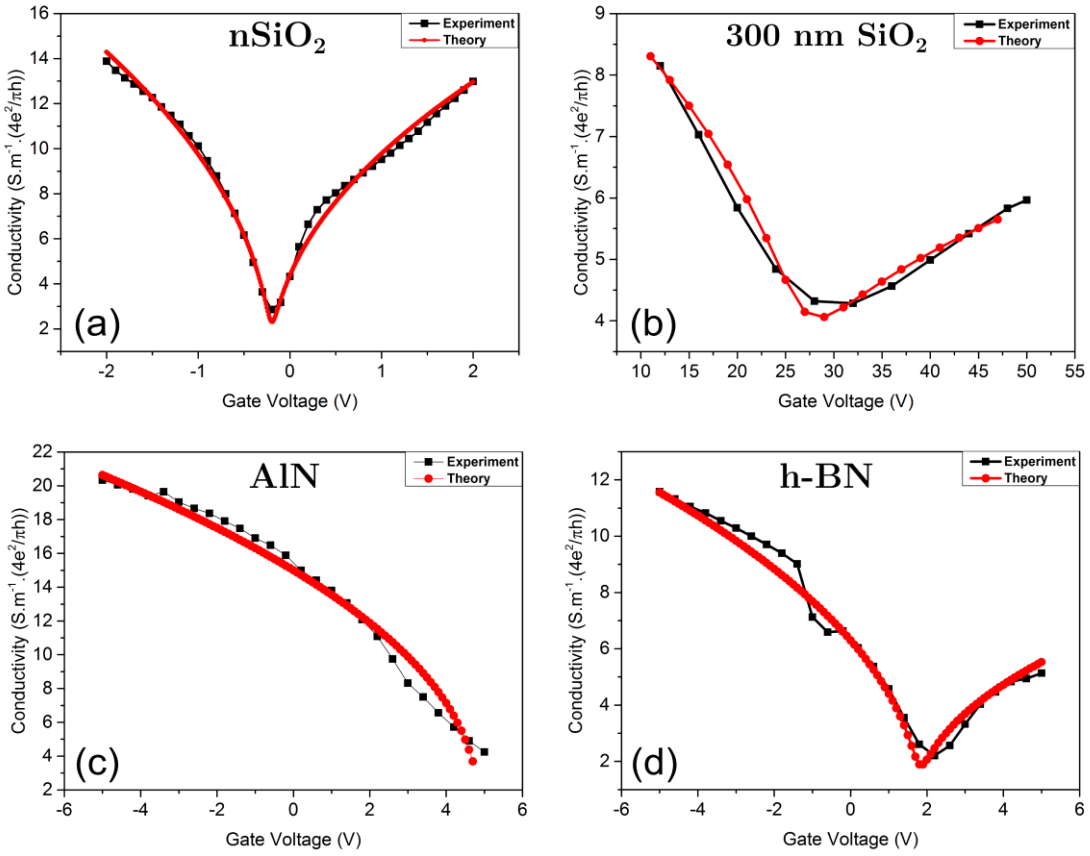


Figure 5.7. Comparison of the experimentally observed conductivity data with the theoretical fit from the Boltzmann's equation results for G-FET with (a) $nSiO_2$ (b) 300 nm SiO_2, (c) 5 nm AlN, and (d)13 nm multilayer h-BN. {189}

In order to obtain the fit, areal capacitance (using Eq. 2.11), intrinsic carrier density (via Eq. 2.31) and the electron and hole scattering times were used. These values are extracted and presented for each device in Table 5.1. It is important to note that these values are in strong agreement with previously reported figures in the literature. [175, 176, 177, 178, 179]

Table 5.1. Parameters used to obtain fit between theoretical and the experimental data for the fabricated G-FET devices.

Gate Material	Capacitance (mF/m^2)	Intrinsic carrier density (10^{12} cm^{-2})	Electron scattering time (fs)	Hole scattering time (fs)
$nSiO_2$	34.5	4.30	17	14
300nm SiO_2	0.11	2.15	19.1	8.22
YSZ/STO	0.44	11.06	5.81	2.90
5nm AlN	3.54	11.06	-	14.51
Multilayer h-BN	2.04	2.55	13.06	8.22

Furthermore, Hall Effect measurements (described in 3.2.2) were performed and the mobility as well as the carrier concentration of each sample were found. Prior to the measurements, Ohmic checks are carried out to ensure good electrical contacts have been established. An example if this check is shown in Figure 5.8. Correlation of 0.99999 and 1.00 are indicative of good Ohmic contacts.

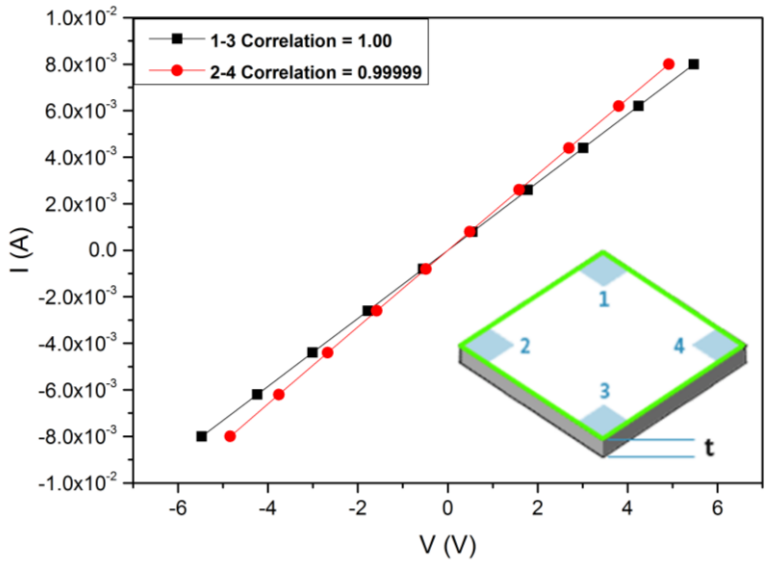


Figure 5.8. The I-V electrical characteristics of the Ohmic contact checks prior to the Hall-effect measurements.

Ohmic checks are then followed by the Van der Pauw resistivity measurements as discussed earlier in 5.1.1. The mobility of the sample is then calculated using Eq. 3.3. Hall Effect data revealed that charge carriers for the earlier described G-FET sample on $nSiO_2$ are holes with an associated Hall mobility of 872 $cm^2.V^{-1}.s^{-1}$. It is apparent that the obtained mobility is significantly higher than the estimated

values from gradient of the transport curves. I believe this is purely attributed to the inaccuracy involved with estimating carrier mobility from gradient of the transport plot as the gradient is chosen in an arbitrary manner close to Dirac point. Summary of the obtained figures are presented in Table 5.2.

Table 5.2. Hall Effect parameters obtained for a G-FET sample on $nSiO_2$.

Hall mobility [cm²/V·s]	**μ_H**	872
Carrier type	-	P (100%)
Carrier concentration [1/cm³]	n	1.15E20
Sheet carrier concentration [1/cm²]	**n(sheet)**	3.92E12
Hall coefficient [cm³/C]	**R_H**	5.42E-2
Resistivity [Ω·cm]	**ρ**	6.21E-5
Hall voltage [V]	**V_H**	5.0975E-1

Moreover, the sample was gated above its CNP to ensure switching of the carrier type from holes to electrons. A gate voltage of 2 V was applied to the sample and an identical Hall measurement was performed. As can be seen in Table 5.3, the results confirmed that the charge carriers at a V_{GS}=2 V are indeed electrons with a Hall mobility of 2030 $cm^2.V^{-1}.s^{-1}$. This value is more than twice the mobility at no V_{GS}=0 V which is correlated to the different scattering time of the carriers.

Table 5.3. Hall Effect parameters obtained for a G-FET sample on $nSiO_2$ at V_{GS}=2 V.

Hall mobility [cm²/V·s]	**μ_H**	2030
Carrier type	-	N (100%)
Carrier concentration [1/cm³]	n	6.87E19
Sheet carrier concentration [1/cm²]	**n(sheet)**	2.33E12
Hall coefficient [cm³/C]	**R_H**	9.09E-2
Resistivity [Ω·cm]	**ρ**	4.48E-5
Hall voltage [V]	**V_H**	-8.55E-1

Table 5.4 compares the obtained Hall mobility data to those estimated from the linear part of the G-FET's transport curves of the same device via the method described in 4.6.4. It is apparent that the values do not coincide well. I strongly believe that the reason for such difference is partly due to the inaccuracy of the estimated mobility and the uncertainty that arises from the capacitance term C. It is also partly because the transport curves are obtained over an averaged area of graphene whereas the Hall data are acquired over a smaller area. In the calculation of the capacitance term, permittivity of the dielectric film is taken from the bulk values that were introduced earlier in Figure 4.27. Moreover, the active area of graphene is estimated. The thickness of the dielectric film in case of $nSiO_2$ is another contributing factor as its value is widely accepted to be 1nm but there are signs of discrepancy in the literature with the values varying from 0.5 nm to 2 nm. [180]

Table 5.4. Comparison between the measured Hall mobility data and those estimated from the linear segment of the G-FETs' transport curves.

Sample\Method	Hall-effect [cm²/V·s]	Estimation from the Gradient [cm²/V·s]
$nSiO_2$	872	125
300nm SiO_2	247	1128
AlN	200	100
STO/YSZ	155	85
h-BN	85	200

5.1.4.1 Performance Assessment of Devices

The DC and microwave field effect characteristics of all seven different G-FET devices were investigated and the fit explained in 5.1.4 was used to extract the important figure of merits. Mobility of the charge carriers (at V_{GS}=0 V), switching ratio as well as the scattering times were obtained. Figure 5.9 presents a comprehensive comparison between the different fabricated G-FET devices.

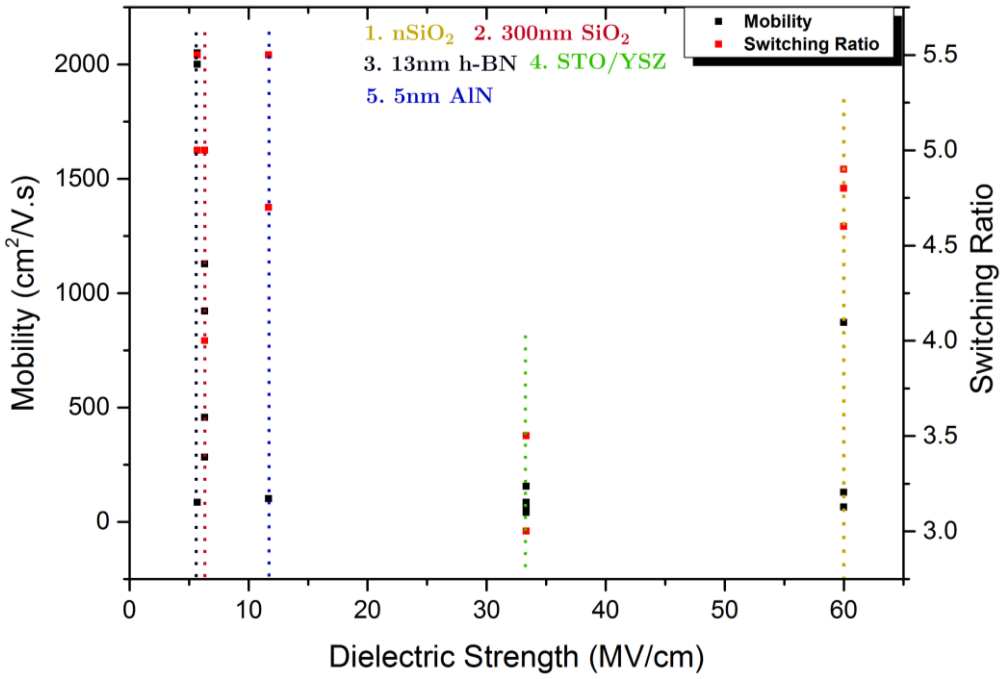


Figure 5.9. Summary of the figure of merit of the fabricated G-FET devices with various dielectric layers.

Establishment of an agreement between the employed theory and the experimental data was an eminent part of the study as it allowed expansion of the G-FET device concept towards graphene-insulator-graphene to validate possibility of gating one graphene with another to achieve a fully graphene integrated transparent field effect device that can be exploited in various fields from transmission modulators in data rate communication devices to biosensing at microwave frequencies. This will be further discussed in 5.4. Based on the achieved results and taking the structural integrity as well as the functionality of the dielectric gate materials into account, it is apparent that $nSiO_2$ and AlN offer a significant advantage over the rest of the investigated materials. The thin layer of $nSiO_2$ not only offers a reduced dimension for future devices, but also it is compatible with the current silicon technologies. On the other hand, the AlN thin film can be grown to have a dielectric constant of 9.2 (Compared to $\varepsilon_r = 2$ in this work) if grown at a higher temperature. [181] The combination of the good dielectric properties of AlN, the additional piezoelectric functionality that it offers, the switching ratio of more than 5, its compatibility with high frequency applications due to its low loss tangent, and the ease of

fabrication associated with it (sputtering disposition) transform aluminum nitride to an ideal choice of gate dielectric material for G-FET devices. As will be shown later in 5.4, AlN can also be grown on top graphene without causing a significant destruction. As a result, fully transparent all-graphene field effect devices can be fabricated and exploited for sensing applications. This will be discussed in details later in 5.4.

5.2 Role of Dielectric-Graphene Interface

It is known that properties of the graphene-insulator interface greatly contribute to the intrinsic doping that is observed as a shift in the Dirac voltage from CNP of 0 V. [182] In order to investigate the substrate effect analytically, G-FET devices were fabricated on identical silicon substrates with 90 nm SiO_2 layer from the same wafer. They were treated under 5 different conditions; (1) as received and untreated, (2) 5 minutes of water-sonication, (3) 5 minutes of acetone/IPA-sonication, (4) 5 minutes Oxygen plasma treatment, and (5) 5 minutes UV-Ozone treatment. As can be seen by the contact angle measurement in Figure 5.10, the surface of samples has become more hydrophilic, going from treatment (1) to (5). This is reflected in the contact angle drop from θ of about 92° in (1) to 44° in (5).

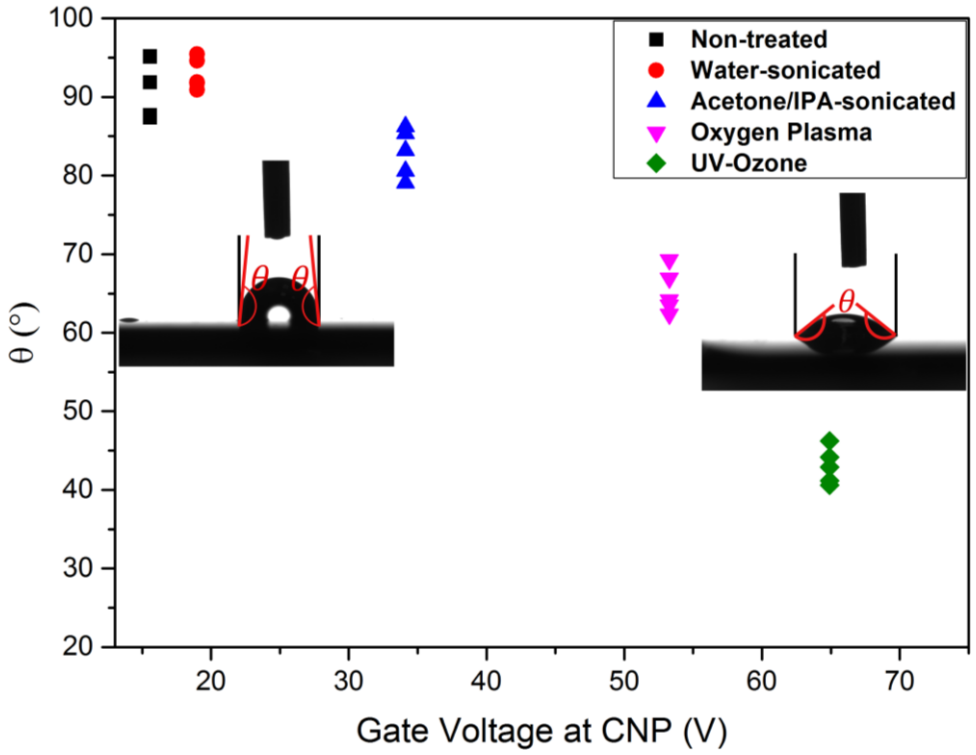


Figure 5.10. Contact angle on the graphene surface at the charge neutrality point (CNP) when transferred on 90nmSiO_2/Si substrates of different surface charge densities upon different surface treatments. [182]

The obtained figures indicate that the graphene-insulator interface play a critical role in dictating the level of doping in graphene, where less hydrophilic surfaces show a CNP that is closer to 0 V. Therefore, in order to achieve G-FET samples with Dirac point closest to 0 V, surface of the substrates need to remain untreated. This is a direct result of avoiding introduction of trapped charges and dangling bonds at the graphene-dielectric interface which is more pronounced at rougher surfaces.

5.3 Pulsed Gate Voltage Dynamics Analysis

In order to gain insight into the dynamics of the fabricated G-FET devices, pulsed gate voltage measurements were carried out. A waveform generator was used and square shaped pulses with amplitude of 300 mV at various mean gate voltages

above and below the CNP were applied. A low frequency of 3 Hz with a sweep time of 1 s was chosen and the measurements utilised 2000 data points as shown in Figure 5.11a.

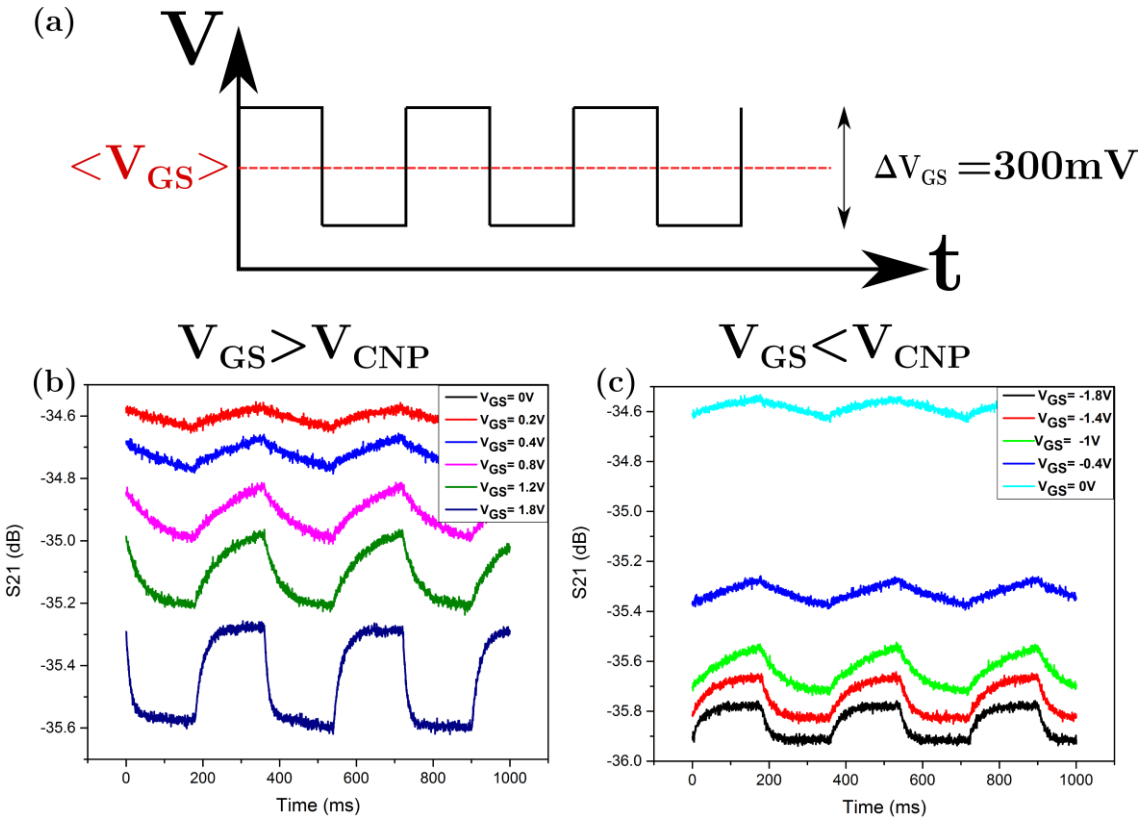


Figure 5.11. (a) Pulsed voltage of 300 mV amplitude and 3 Hz frequency applied between source and gate. Response of graphene to the pulsed gate voltage recorded at the resonant frequency for mean gate voltages (b) above and (c) below the Dirac point.

The gate voltage response of the G-FET device on $nSiO_2$ for both sides of the Dirac cone is shown in Figure 5.11b-c. In order to extract the time constant value from the obtained plots, the S21 transmission data are converted from dB into percentage using the following relation:

$$T = 10^{(dB/20)} \tag{5.2}$$

An exponential fit $(y = y_0 + A \times \exp(R_0 x))$ is then used to calculate the constant R_0, which is the exponential constant term and is directly related to the RC time

constant via $\tau = 1/R_0$. An example of such fit to the normalised time data of the sample is presented below in Figure 5.12.

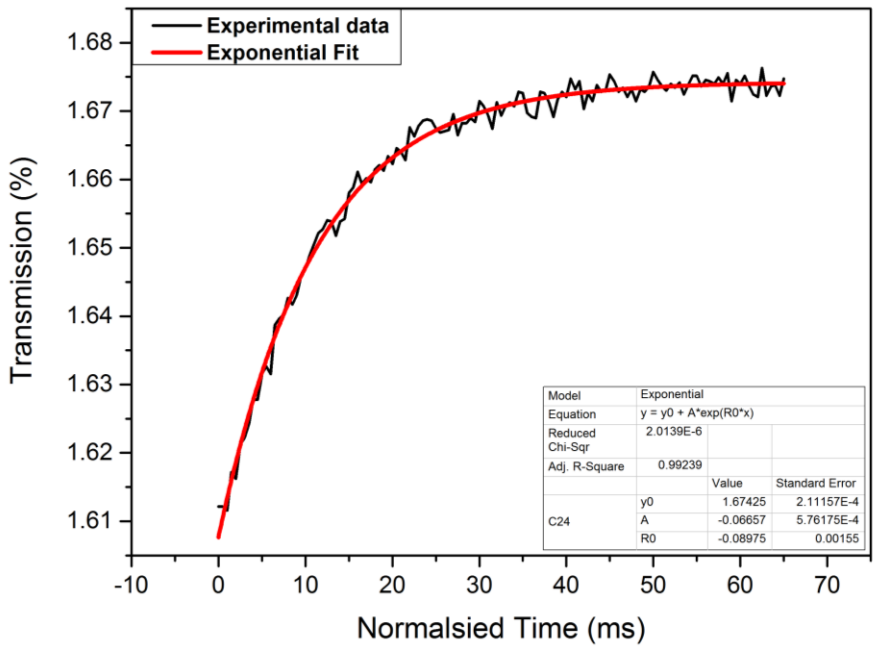


Figure 5.12. Exponential fit to the pulsed-gate voltage response of G-FET device at mean gate voltage of 2V.

Upon extraction of the time constant values at every applied $<V_{GS}>$, a double y-axis plot of gate voltage versus switching ratio and time constant is plotted in order to make a comparative analysis. This is shown in Figure 5.13.

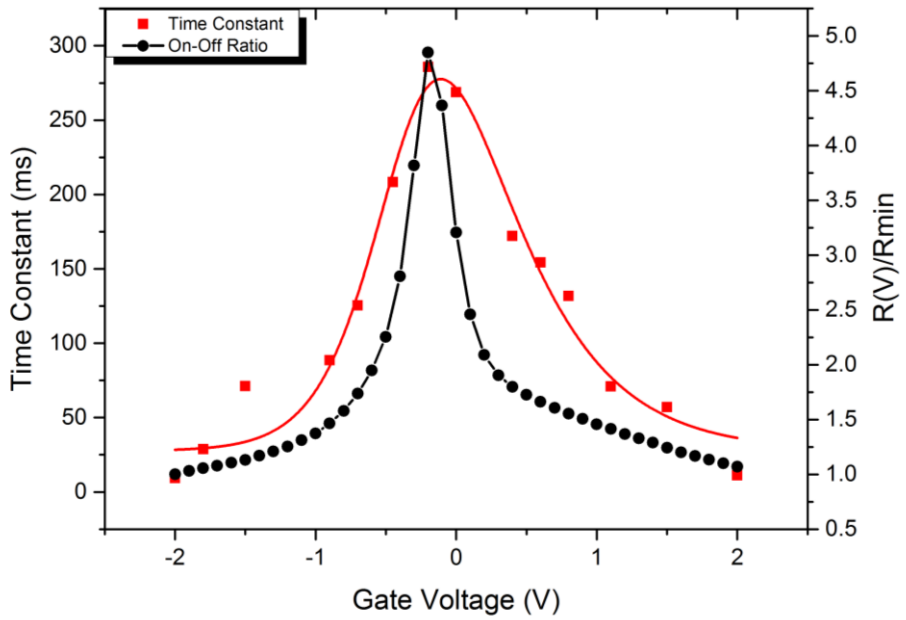


Figure 5.13. Comparison of on-off ratio and time constant for G-FET on $nSiO_2$ obtained from exponential fit to the pulsed-gate voltage response of the device shown in Figure 5.11b and c.

The relatively high time constant value of about 280 ms at Dirac point is directly related to the high RC constant of the device due to the large areal dimension of the sample (area of 1 cm^2). From the device and application perspectives, such high time constant would not be acceptable for the high speed communication purposes where switching and signal modulation speed play vital roles. Current silicon based technologies have time constant values in the order of nanoseconds that enables Gb/s communication capability. [183] However it must be noted that scaling of the investigated graphene device from $1cm^2$ down to $1\mu m^2$ can result in a significant improvement of the time constant. This stems from the fact that both R ($\propto d$) and C ($\propto d^2$) are proportional to dimensions of the graphene sample. Assuming a square geometry for convenience, with a side length of d, the time constant of the devices is effectively proportional to d^3. This means that a 250 ms time constant can be reduced by a factor of 10^{12} to about 0.25 ps by fabricating devices of the area of 1 μm^2.

Moreover, it is apparent that the resistance switching ratio of 5 is not repeated for the time constant. The time constant rather changes by a calculated factor of 11. This effectively means that capacitance is playing a significant role and is changing by a factor of 2.2 with gate voltage (11/Maximum on-off ratio). Xia et al.[184] correlate this phenomenon to quantum capacitance of graphene, where they were able to measure the quantum capacitance of graphene in an ionic liquid based G-FET. Quantum capacitance of graphene was first introduced in order to account for the missing capacitance in the graphene based capacitors and it is taken to be in series with the geometrical capacitance. It can be shown that the quantum capacitance is correlated with the square root of the carrier concentration in graphene, which means that it has its minimum value at CNP. [184] Therefore the missing factor of 2.2 in the present work cannot be attributed to the quantum capacitance. Future works will need to involve measuring and developing a

comprehensive script to accurately fit and extract the time constant value from the square wave response of the devices. The results will need to be compared with the capacitance measurements (C-V) of the same device to reveal a more conclusive picture.

5.4 Graphene-Gated G-FET Structure

One of the existing issues in the area of high frequency modulators and transmission devices is the fact that the currently employed contacts become lossy and result in lack of functionality of the device. To tackle this problem, one can utilize the full potential of graphene as a modulator or a transmission device, by replacing the lossy HRS substrate with a transparent gate electrode material. To do so, it needs to be demonstrated, experimentally, that a similar switching ratio to typical back-gated devices is achievable. Therefore, I realized a proof of concept experiment, investigating performance of a self-gating graphene structure composed of an ultrathin dielectric layer sandwiched between the two graphene layers. Such structure would replace the lossy silicon substrate by another graphene layer. Two other attempts to build a self-gated graphene structure have been reported by Gomez-Diaz *et al.* [185] who used PMMA layer as the dielectric gate material, and Kakenov *et al.* who utilized an electrolyte. [186] Although the fabrication of graphene-PMMA stack is relatively straightforward, PMMA is prone to deterioration by post-transfer procedures and also suffers from a low breakdown field (experimentally found to be 0.37 MV/cm as shown in Figure 5.14). Therefore, there exists a demand for a stable and reproducible wafer-scale fabrication technique compatible with the industrially matured methods, such as sputtering, pulsed laser deposition (PLD) or atomic layer deposition (ALD).

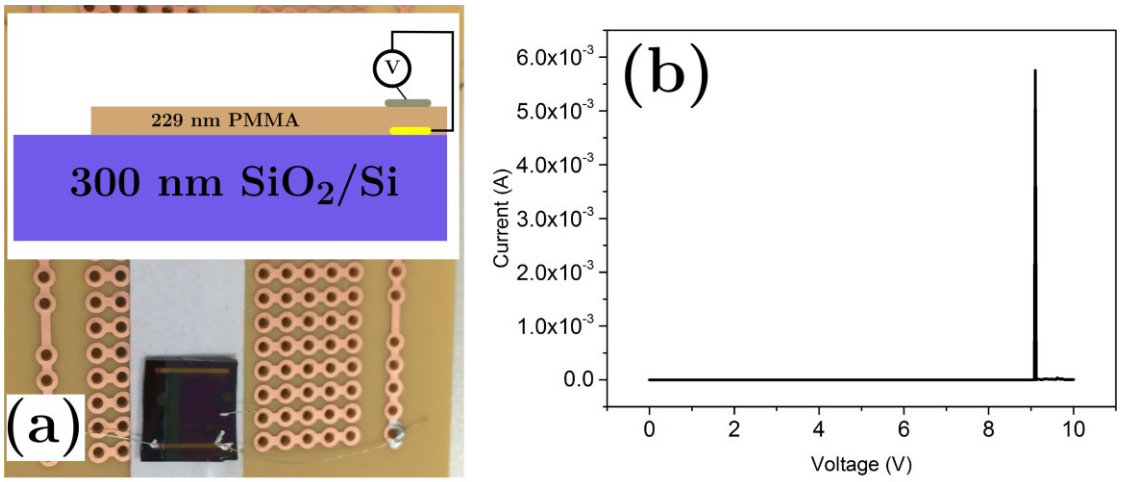


Figure 5.14. (a) Breakdown test configuration of 229 nm spin-coated PMMA on a 300 nm SiO_2/Si substrate and (b) the I-V characteristics when measured across the thickness of the PMMA.

Amongst the potential choices of gate dielectric materials which were discussed in 4.4, a thin film of AlN was chosen. It has a simple fabrication process via sputtering at moderate temperatures (400°C) on top of graphene without destruction of the underlying material associated with it as well as a low leakage current. It also offers a high achievable switching ratio, when used in combination with silicon as a back-gate structure (see Figure 5.4e). The structure is designed to be fabricated by (1) covering HRS/nSiO_2 substrate by a 0.6 cm by 0.8 cm graphene film followed by (2) sputtering of 50nm AlN via identical procedure explained in 4.4.3 and finally (3) transferring the second graphene layer with same geometry as the first graphene but 90° rotated. This results in construction of a squared shaped active area of 0.6 cm*0.6 cm. It is important to note that the electrical contact to the lower graphene layer was made before deposition of AlN thin film over the top. Both the schematics and the optical images of the fabricated graphene-AlN-graphene structure on nSiO_2/Si are presented in Figure 5.15. The optical contrast between different layers of the structure can be clearly observed in the obtained optical images.

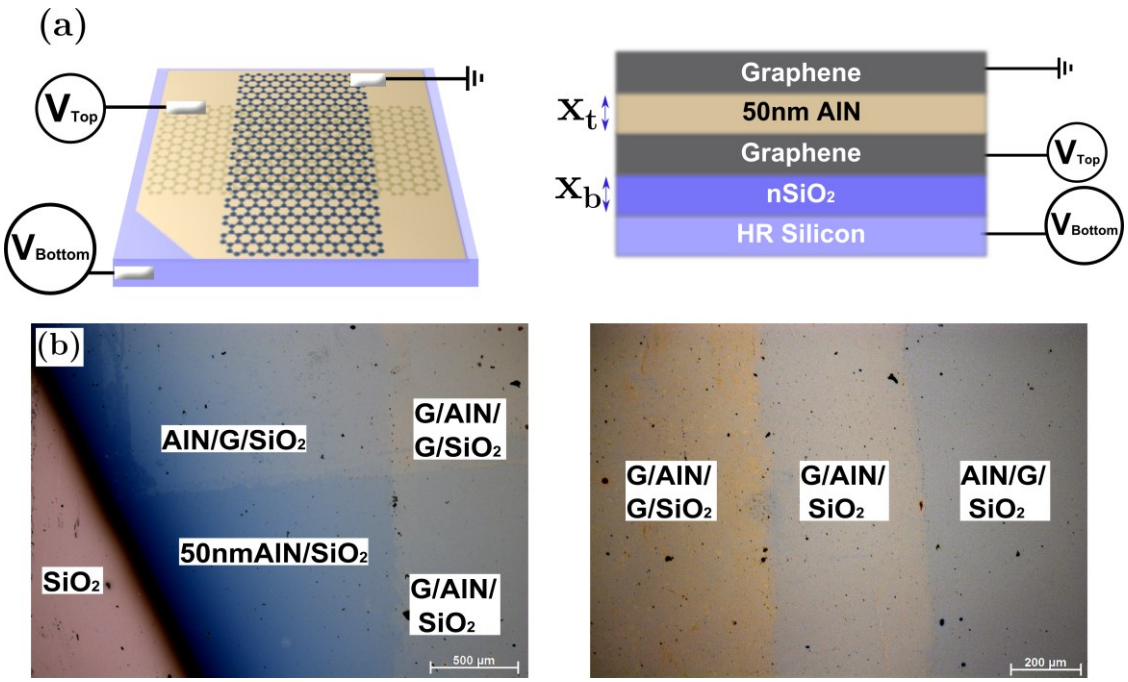


Figure 5.15. (a) Schematics and (b) the optical images of the fabricated graphene-gated G-FET heterostructure with 50 nm AlN insulating layer. [189]

To further investigate the quality graphene and confirm presence of each layer, thickness measurement, XRD and Raman spectroscopy analysis were performed which are presented in Figure 5.16. As apparent in Figure 5.16a, the grown AlN thin film is measured to be 50 nm thick and both the XRD and the Raman spectra of the film are indicative of its c-axis orientation. [187] Raman spectrum on the graphene also reveals that the film has retained its integrity upon AlN deposition as seen by the intensity of the D-band that has remained well below that of the G peak. The 2D/G distribution with a mean value of about 2.4 further proves the single layer nature of the graphene layer. The growth mechanism on graphene can be explained by the theory recently developed by Zou et al. [188], where pillar like growth from the sites of defects was proposed for fabrication of STO on graphene. In the case of AlN, such growth is believed to be initiated with bonding of the incoming sputtered atoms to the oxygen terminated SiO_2, over which graphene is transferred on. The growth of the film is then believed to proceed horizontally and in-plane until a continuous layer is achieved.

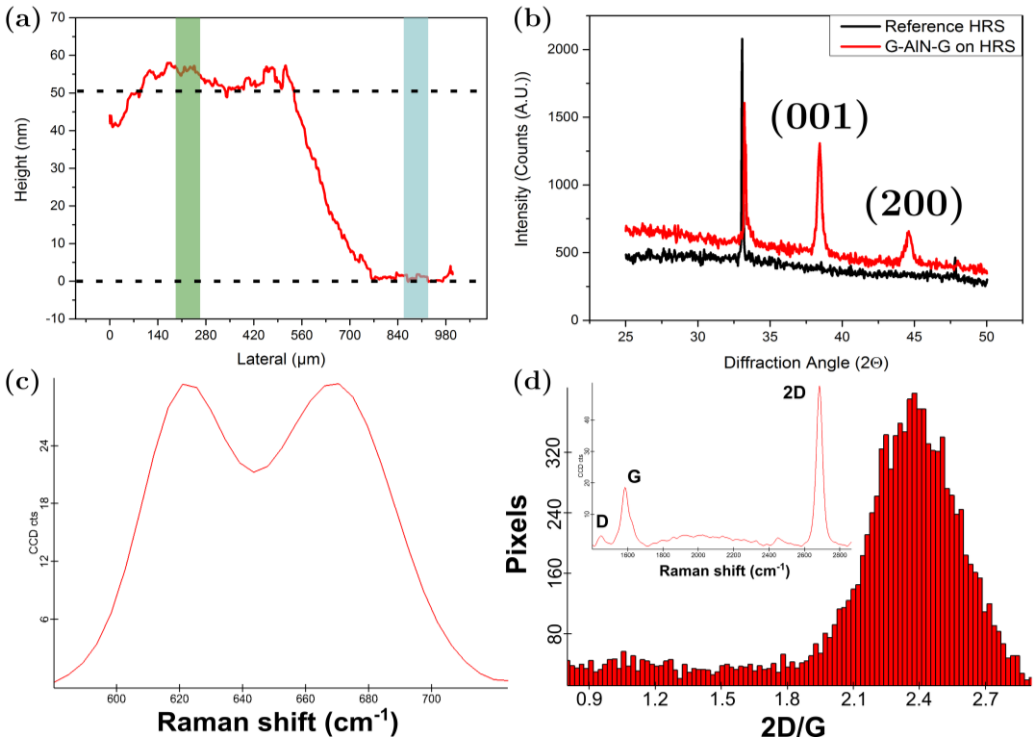


Figure 5.16. (a) 50nm thickness confirmation of the sputtered AlN thin film on graphene by 150 Dektak profiler. (b) The XRD spectrum coupled with (c) the Raman spectrum of the G-AlN-G confirming the c-axis orientation of AlN thin film. (d) Raman spectrum of graphene indicative of its monolayer nature with minimal defects. [189]

In order to perform the microwave field effect measurements on the fabricated heterostructure, the sample is placed on the cavity while its active area is fully covering the aperture. This is represented in the schematics shown in Figure 5.17. The microwave measurements are carried out identical to 4.6.4 with an added second gate terminal as shown in Figure 5.15a. V_{Top} is designed to adjust the Fermi level of the top graphene and realization of V_{Bottom} is intended for modulation of initially the bottom graphene and subsequently the top graphene layer. Figure 6a shows the results of the microwave sheet resistance for a large area (25 mm^2) self-gated and back-gated graphene with 50 nm of AlN in between as a function of the applied voltage between the two graphene layers. The different curves correspond to the different voltages that are applied to the HRS back-gate. Note that the partial transparency of graphene and AlN to the electromagnetic cavity fields enables the measurements of the parallel resistance of the two graphene layers.

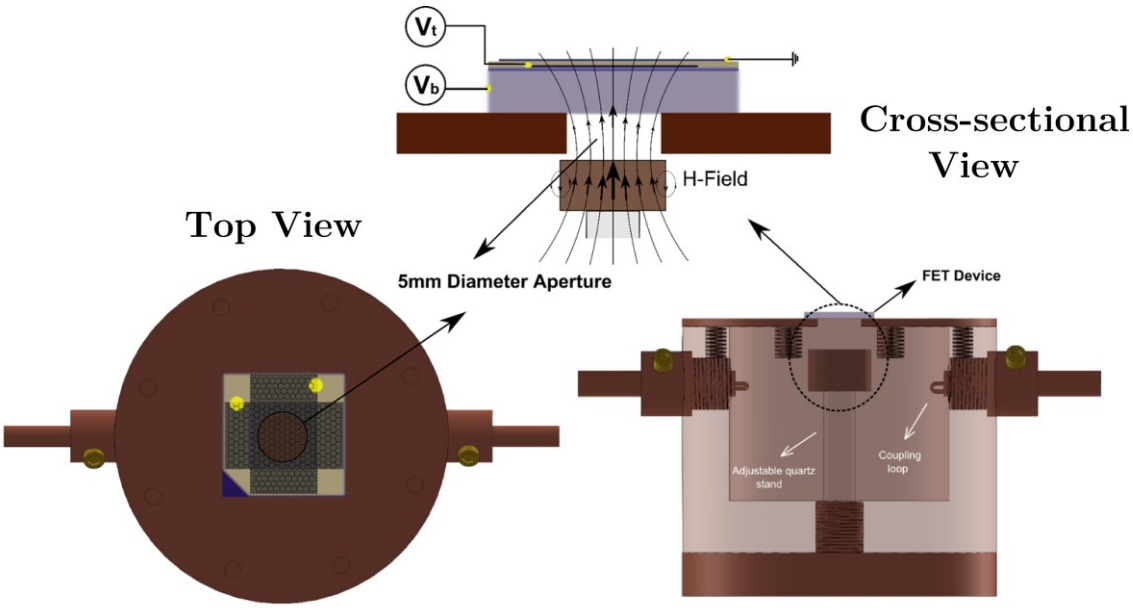


Figure 5.17. Schematics of the microwave measurement assembly demonstrating the arrangement of the double-graphene G-FET structure over the cavity.

Considering the double-layer stack configuration shown in Figure 5.15a, the areal carrier concentration of each graphene layer can be determined via the capacitance of each stack coupled with the intrinsic carrier concentration of the top and bottom graphene sheets ($n_{0\ (Top)}$ and $n_{0\ (Bottom)}$ respectively). The positive and negative signs of the capacitance term correspond to n-doping and p-doping respectively:

$$n_{Top} = n_{0\ (Top)} + \frac{C_{Top}V_{Top}}{e} \tag{5.3}$$

$$n_{Bottom} = n_{0\ (Bottom)} - \frac{C_{Top}V_{Top}}{e} + \frac{C_{Bottom}V_{Bottom}}{e} \tag{5.4}$$

Similar to Eq 2.11, the areal capacitance of both the top (graphene-graphene) and bottom (Graphene-Si) parallel-plates can be calculated:

$$C_{Top} = \frac{\varepsilon_0\varepsilon_{r(AlN)}}{X_t} \tag{5.5}$$

$$C_{Bottom} = \frac{\varepsilon_0\varepsilon_{r(SiO2)}}{X_b} \tag{5.6}$$

The presented plots in Figure 5.18 show the conversion of the obtained voltage dependant Q-factor to sum of the sheet resistance for the two graphene layers.

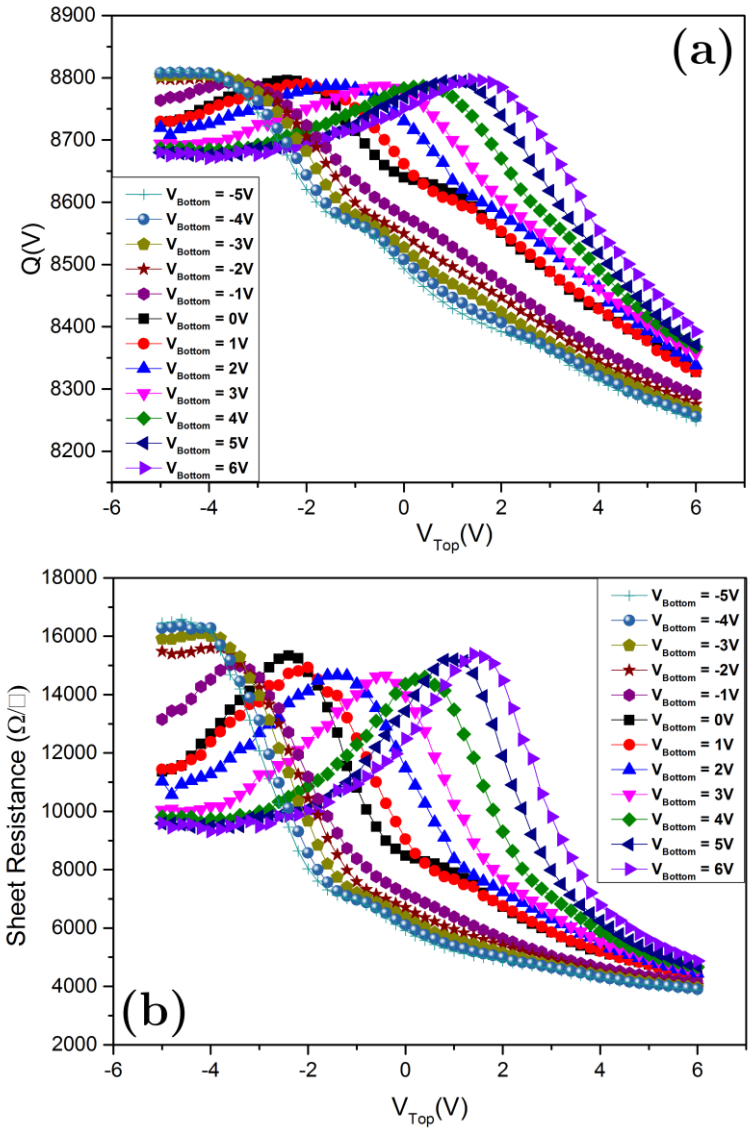


Figure 5.18. Microwave field effect characterisation of the G-AlN-G heterostructure showing (a) Q-factor dependence on both top and bottom gate voltages that were used to calculate sheet resistance of both graphene layers as function of V_{Top} at various V_{Bottom} values. [189]

The obtained resistance values are then converted into conductivity. The Boltzmann equation that was described earlier in 2.3 can then be employed once again to obtain a fit to the conductivity plots at different interlayer gate voltages (different V_{Top} and V_{Bottom}). The resulting conductivity curves and the numerical fit associated with each curve is then acquired. The fit can then be used to extract scattering time and mobility of each of the graphene layers. The plotted curves in Figure 5.19a-b compare the theoretical conductivity simulations with the experimental conductivity results for the graphene stack.

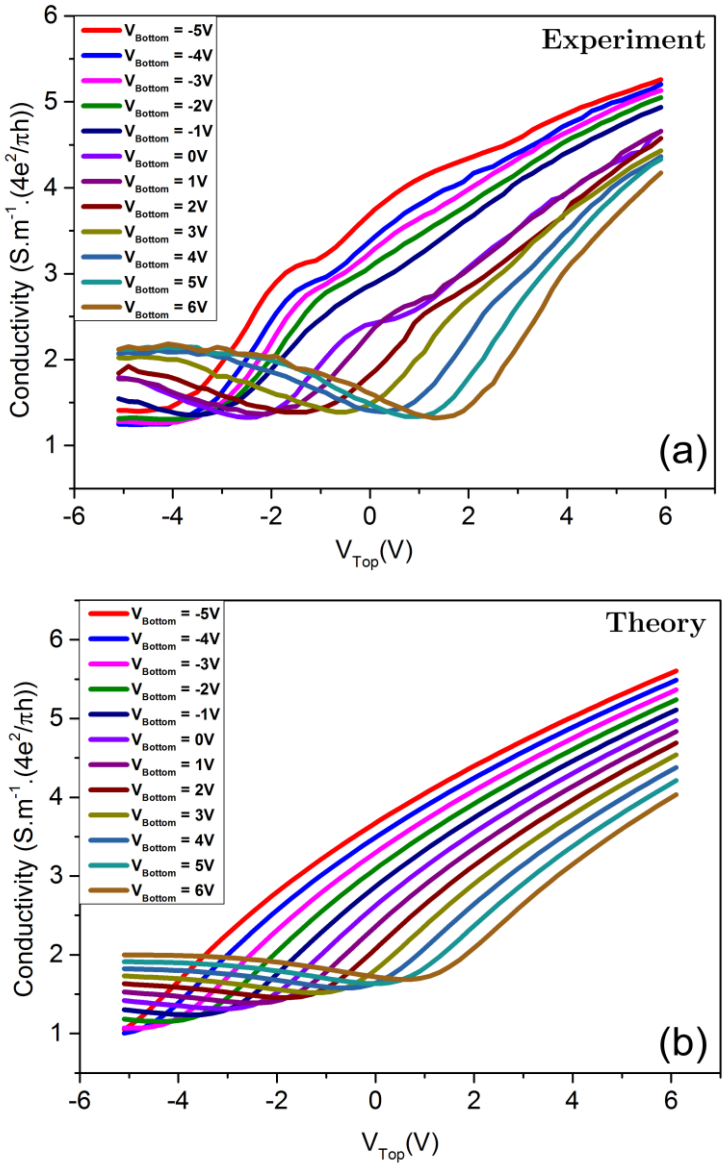


Figure 5.19. (a) Theoretical model and (b) experimentally obtained field effect data on the G-AlN-G heterostructure, where the charge carrier density of graphene layers were controlled via two gate terminals of V_{Top} *(graphene)* and V_{Bottom} *(Silicon).* [189]

In order to obtain the fit, identical electron and hole scattering time of $\tau_+ = \tau_- = 3.6\,\text{fs}$ and intrinsic carrier concentration of $n_{0\,(Top)} = 10.8 \times 10^{11}\,\text{cm}^{-2}$ for the top graphene sheet and $\tau_+ = 10.9\,\text{fs}$, $\tau_- = 5.8\,\text{fs}$ and $n_{0\,(Bottom)} = -4.0 \times 10^{11}\,\text{cm}^{-2}$ for the bottom graphene sheet are used. Areal capacitances of $0.3\,\text{mF/m}^2$ and $0.17\,\text{mF/m}^2$ were used for the top capacitor (50 nm AlN) and the bottom capacitor (nSiO_2) respectively.

The achieved results demonstrate a switching ratio of as high as 4.5 for the parallel resistance due to alteration of the gate voltage between the two graphene layers, i.e. without any change of the back-gate voltage and without any metallic top gate. As can be seen in Figure 5.20, when considering the curve where only the top gate voltage is varied, the resistance of the layers can be modified by varying the V_{Top} while the bottom gate voltage is set to zero.

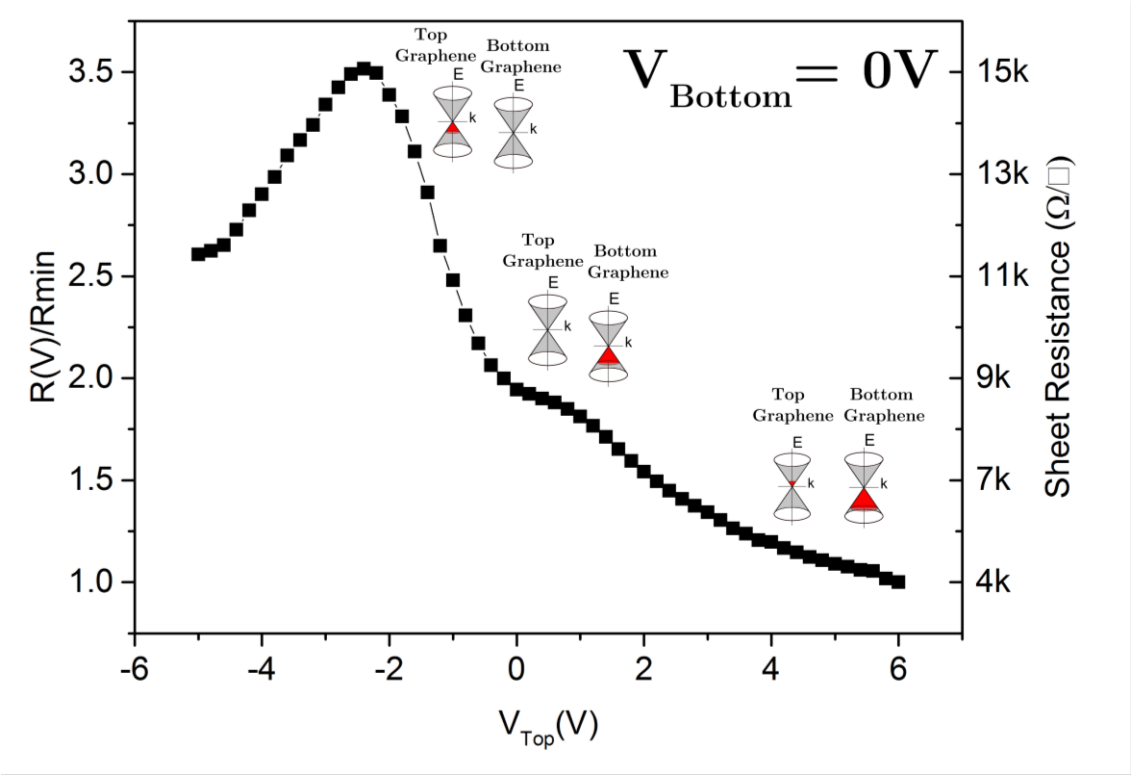


Figure 5.20. The switching ratio and resistance dependence of the double-layer graphene FET device on the top gate voltage when the bottom gate voltage is set to zero.

At the positive end of the applied top gate voltage, the bottom graphene is significantly p-doped while the top graphene is lightly n-doped. As V_{Top} is reduced, the Fermi level of the top graphene reaches zero while the bottom graphene is being injected with electrons. Further decrease of the top gate voltage results in Fermi level of the bottom graphene to reach the Dirac point which has manifested itself as a maximum in the sheet resistance value in the obtained curve. The results are in agreement with the fact that the induced current in the bottom graphene layer

is slightly higher than the current in the top graphene layer due to partial reflection of the magnetic field from the bottom graphene layer.

The presented simulations reproduce some of the key features of the experimental result, including the shift of the Dirac point of the bottom graphene layer for changes of the back gate voltage and the strong asymmetry of the conductivity curves, which arises from the presence of the top graphene layer whose Dirac point is at a large negative bias voltage which lies outside the range of leakage-free voltages between the two graphene layers.

Furthermore, as interfacial properties dictate the charge neutrality point of graphene and since the two graphene films are deposited over two different surfaces, the Dirac voltage is expected to different for each of the layers. It is found that the minimum conductivity in the theoretical results increases upon increasing the back gate voltage, while this value is almost constant in the experimental measurement. I attribute this discrepancy to the assumption of a constant scattering time in the computed conductivity, which cannot reproduce the experimentally observed saturation of the conductivity at large gate voltages (see AlN example in Figure 5.2,). Moreover, the spacing between the resistance curves in Figure 5.19 is even in contrary to the estimation by the theory. This can be described by considering the piezoelectricity of AlN, which results in a voltage-dependent capacitance. This was not taken into account due to the additional complexity of introducing an extra variable into the equations. However, it is important to take the change in permittivity of the AlN layer into consideration for future works as it was found that the permittivity of the AlN film changes by about 10% upon varying the gate voltage (see Figure 4.35).

In conclusion, this novel heterostructure represents an all-graphene voltage-controlled attenuator for microwave frequencies. Such structure also resembles a promising platform for the highly scaled CMOS devices where two gate electrodes

need to be used. Future work is highly encouraged to investigate such structure with a comparatively more complex electrical contact geometry to enable characterisation of individual graphene sheet upon device fabrication completion, which will also allow for development of a more accurate fitting model.

5.5 Summary and Conclusion

The microwave field effect characterisation of graphene based FET structures with gate dielectric materials of SiO_2, AlN, multilayer h-BN, and STO/YSZ stack were conducted via the microwave cavity technique at an operation frequency of about 9 GHz. The obtained transport plots were in strong agreement with the ones attained via the DC measurements, which verified the robustness of the employed microwave technique. Importantly, it was shown that the microwave behaviour of graphene follows closely to that of DC. This is due to the domination of the intra-band transitions that result in lack of dispersion up to around 100 GHz, according to the Kubo formula for the frequency dependant conductivity of graphene. The switching ratio and mobility of the devices were investigated. Based on the performance of the devices and the complexities associated with fabrication of each device, native SiO_2 as well as AlN thin film were found as ideal choices for graphene based field effect devices. Based on the archived results on single layer graphene FET devices, a graphene-AlN-graphene structure was fabricated on top of an $nSiO_2$/Si substrate. This was carried out with the aim of replacing the metallic gate electrodes that have a significant contribution to the losses in various optical applications, with another graphene layer. The microwave measurements provided a clear indication of the possibility of adjusting the carrier concentration in one graphene sheet by the application of bias between the two graphene layers. Maximum switching ratio of 4.5 was achieved by varying the potential between the two graphene layers. The Boltzmann equation was used and the carrier

concentration as well as the scattering time of the individual graphene sheets were calculated after obtaining a fit to the measured microwave transport curves. The novel combination of two graphene layers and a thin film of AlN in single structure presents motivates new opportunities for optical and sensing applications. The ability of modulating the sheet resistance of one graphene layer via another graphene sheet, detecting charge variations, and the piezoelectricity of the AlN films for mass detection can all be utilised in a single integrated device. To conclude, this study revealed the possibility of replacing the metallic thin films with graphene in order to achieve an all transparent graphene based field effect device. This plays an eminent role in the biosensing area where chemical sensitivity of graphene coupled with the transparency of the device transforms the all graphene field effect system into a versatile and powerful diagnostic tool.

6. Concluding Remarks

In the first two chapters, an introduction to graphene and overview of the current developments with regards to fabrication and applications of graphene was presented. The fundamental structural as well as the electrical and field effect properties of this material were described. It was eminent to do so as it allowed for a firm foundation upon which the rest of the research could be built on. It was explained how the transparency, the lack of band gap, the ability to modulate sheet resistance of graphene via an external gate voltage and the compatibility of this two dimensional material with the current wafer-scale processes have transformed it to an ideal choice for many of the microwave-THz applications.

In chapter 3, the focus was placed on describing the tools and techniques that were employed in order to assess the quality of fabricated materials and devices. Meeting the set standards in the field was vital in ensuring a high performance of the devices. This chapter ended by introducing the novel microwave cavity technique as a contact-free method of characterising electrical properties of graphene. The microwave cavity was carefully designed via the computer assisted design (CAD) software of SolidWorks.

Chapter 4 explored the optimisation of growing the single-layer graphene films on copper substrates via two different methods of vertical and horizontal CVD. The fabricated graphene layers were fully characterised via the Raman analysis as well as AFM measurements. The copper substrates were characterised via the XRD, AFM, and EBSD analysis. It was shown that the choice of copper substrate is as important as finding the optimum growth conditions in order to establish a consistent single-layer graphene growth mechanism. The chapter continued with optimisation of transfer of a graphene film on a given substrate. It was demonstrated that the graphene/substrate interface play a key role in ensuring

adequate adhesion between the two materials. The morphology and crystallinity of the various used dielectric thin films were also investigated via a variety of characterisation techniques. The obtained results were in strong agreement with the existing guidelines in the literature. Chapter 4 concluded by describing the system development procedures for performing the DC and the microwave measurements via a single setup. The microwave cavity technique and the DC measurements (via the Sourcemeter) were coupled by using a developed Matlab script connecting the two systems together.

The obtained DC and electromagnetic data for the fabricated field effect structures were presented in chapter 5. The validity of the microwave cavity technique was evaluated by a comparative analysis to the measured DC field effect characteristic of the device. It was shown that the microwave transport curves were in strong agreement with the DC ones, where this was illustrated for all the fabricated G-FET devices. To further assess the performance of the devices, the Boltzmann framework was employed and theoretical fit was obtained to the measured transport plots. Parameters such as mobility, scattering time and intrinsic carrier concentration were extracted. The obtained mobility data were then compared to the values that were attained via the Hall-effect measurements. It was found that there existed a discrepancy between the mobility values that were obtained by the two methods. It was attributed to the area of the graphene that each method uses to realize a mobility value. In the microwave technique the attained mobility is an average value over an active area of 16 mm^2 that is exposed to the microwave evanescent field whereas in the Hall-effect geometry, the current and voltage would follow a preferential path that is different to that of the microwave analysis.

Dynamic measurements on the graphene/nSiO_2 G-FET samples revealed that the very high RC constant of the large-area devices significantly slows down the response time of the charge carriers.

Further the influence of the dielectric layer interface on positioning of the Dirac point of graphene was investigated. The contact angle measurements were used and it was shown that various treatment such as Oxygen plasma or Acetone sonication can result in an increased trapped charge density at the graphene-dielectric interface, which subsequently gives rise to p-doping of the graphene film.

Based on the achieved results and the performance of the investigated dielectric gate materials, aluminum nitride was chosen to be deposited in between two graphene layers in order to examine the possibility of modulating the sheet resistance of one graphene layer via the application of gate voltage to another graphene film. For the first time it was shown that such structure resembles an all-graphene field effect device, where the combination of AlN and graphene yielded a maximum switching ratio of about 4.5 at the operation frequency of about 9 GHz. Boltzmann equation was employed once again and the obtained fit was used to extract scattering time and intrinsic carrier concentration in the individual graphene layers. This novel concept of combining AlN with two graphene layers can take advantage of transparency, modulation of carrier concentration, and conductivity of graphene in conjunction with the piezoelectricity of AlN in many optics and sensing applications where currently lossy metallic gate electrodes are being used. The work included a number of major original contributions; The very first was with regards to production of graphene (via a vertical CVD) and transfer of this 2D material via a novel tape-pen method. However, the major outcome of the work comes at successful fabrication of AlN/graphene FET and demonstration of the working concept of an all-graphene FET system to address the transparency issue that limits the versatility of the current FETs. This was an eminent part of me and my colleagues at the Terahertz Technology Centre at Imperial College to enable us using graphene FETs in a multi-purpose device. This is further explained in the Future Works below.

6.1 Future Works

Despite the very ambitious road map set by the graphene pioneers, this field still lacks a clear vision where graphene would outwit, outlast and outperform the existing materials and technologies. The present work demonstrated the potential for combining graphene and aluminum nitride in a double-graphene field effect structure where mass and charge detection capability can be incorporated in a single integrated biosensing device. Knowing that different cells have different charge and mass values, a dual sensing device where both the charge and the mass of the cell under test can be measured simultaneously can significantly boost the efficiency of the biosensor while reducing the number of false alarms. Utilization of aluminum nitride for reading an electrical signal (due to its piezoelectricity) and a graphene film for its biocompatibility and charge detection capability would allow for fabrication of such device.

A graphene-AlN-graphene structure fabricated on a low loss substrate such as quartz can be employed where the ambipolar characteristic in resistance change by the application of a voltage between the graphene layers can be observed. The assembly of such structure is presented in Figure 6.1. As apparent from the represented schematics, a thin film of AlN is sandwiched between two graphene films. The high Young's modulus of graphene coupled with the two dimensional nature of this material suggests that graphene would not compromise the mechanical properties of AlN which transforms it to an ideal choice of electrode for AlN.

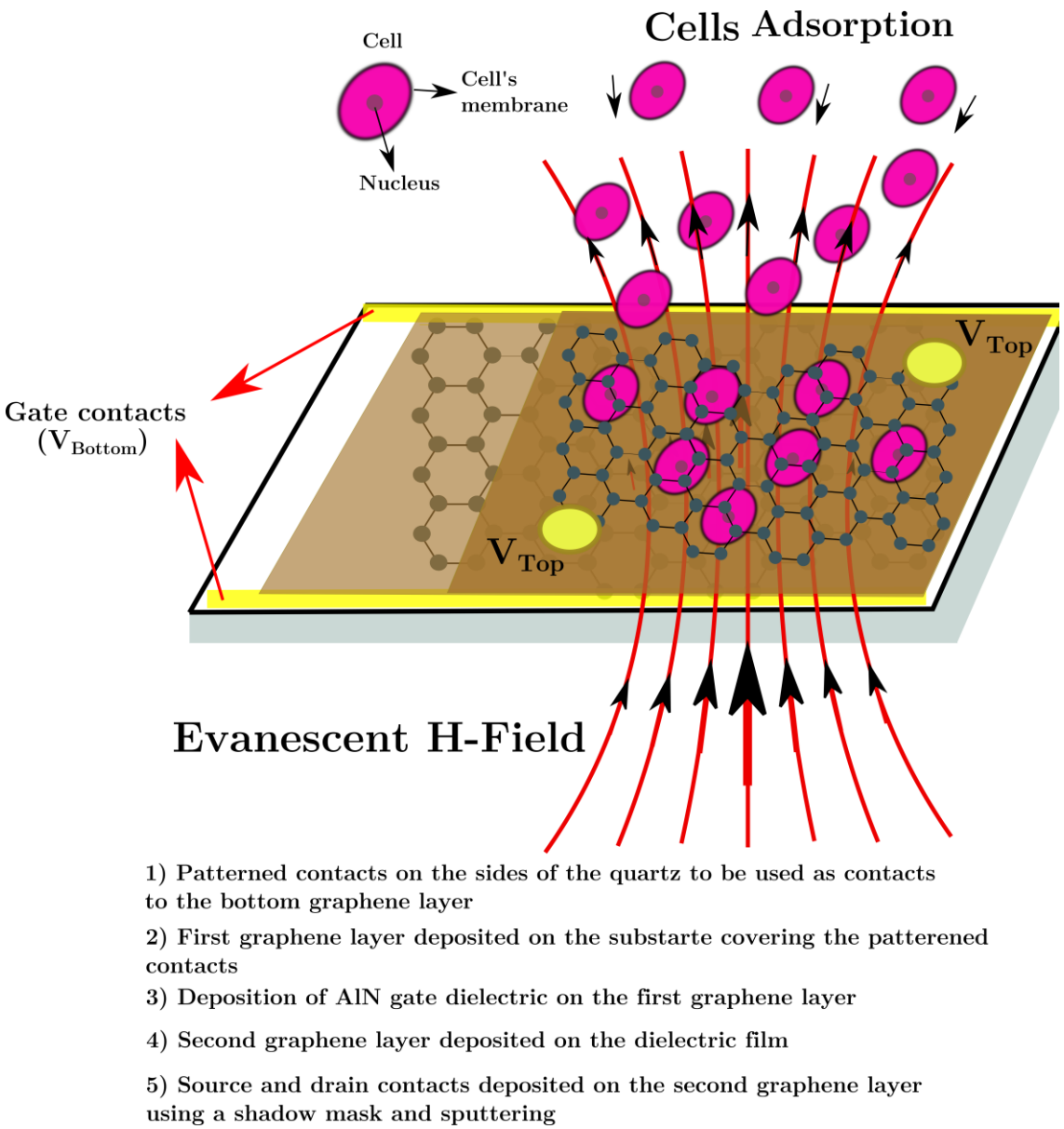


Figure 6.1. Schematics of the proposed biosensing double graphene FET structure containing the step by step fabrication procedures.

As shown in Figure 6.2, the gate voltage between the two graphene layers can be utilised to shift the working range towards the maximum resistance point near which the gradient is the steepest, hence the sensitivity is maximised. Furthermore, the amount of introduced charges due to adsorption of a given cell can be estimated from the shift in the Dirac point. On the other hand, the mechanical resonance in the thin film of AlN and the subsequent shift in the resonant frequency associated with it that can be used for the mass detection. Coupling the charge detection

capability with ability of this device to detect mass of the introduced cells results in a novel dual-biosensing application of this structure. Therefore, the present work provided the foundation for the testing of this dual-biosensing concept with different cells including cancer cells which are subject to future works.

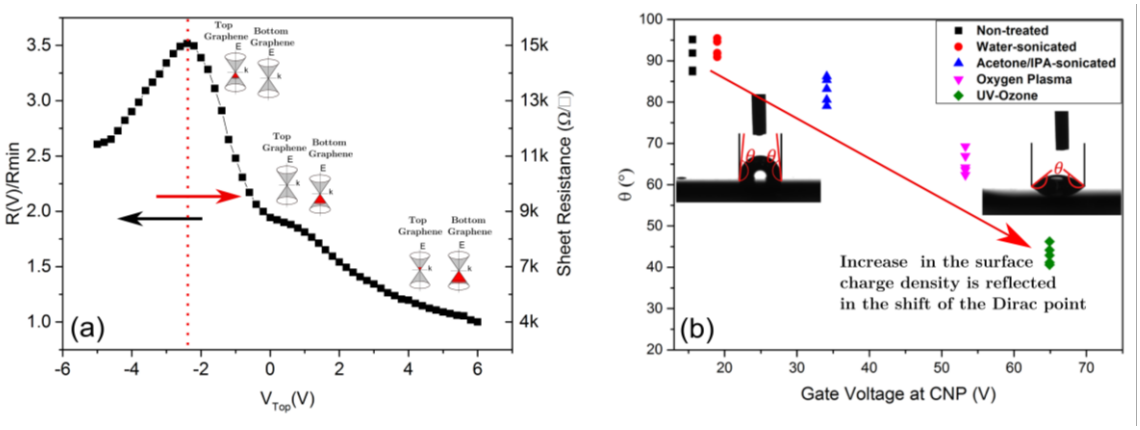


Figure 6.2. (a) The microwave sheet resistance as a function of a gate voltage applied between two graphene layers in a graphene-AlN-graphene structure where two graphene films are separated by a 60 nm thin film aluminium nitride. (b) The shift in the position of the Dirac point which can be used to detect the amount of the introduced charge and subsequently appoint it to a given cell.

7. Appendix

7.1 Horizontal CVD Graphene Growth Recipes

Sample	Annealing				Growth				Cooling		
	H_2:Ar (sccm)	P (mbar)	T (°C)	t (m)	CH_4:H_2:Ar (sccm)	P (mbar)	T (°C)	t (m)	CH_4:H_2:Ar (sccm)	P (mbar)	Type
1	30:20	1	1000	50	5:15:20	1.2	1000	30	5:15:20	1.2	Slow
2	30:15	1	1000	50	30:15:10	1.1	1000	30	30:15:10	1.1	Slow
3	45:15	1.8	1000	50	15:45:10	1.3	1000	30	15:45:10	1.3	Slow
4	40:100	6.6	1000	60	5:15:100	5.9	1000	30	5:15:100	5.9	Slow
5	40:100	6.2	1000	60	10:30:100	6.2	1000	30	10:30:100	6.1	Slow
6	40:100	6.2	1000	60	15:45:100	6.5	1000	30	15:45:100	6.5	Slow
7	40:100	6.2	1000	60	20:45:100	6.5	1000	30	20:45:100	6.5	Slow
8	40:100	6.2	1000	60	40:45:100	6.5	1000	30	40:45:100	6.5	Slow
9	80:0	1	1000	60	40:40:0	1	1000	30	40:40:0	1	Slow
10	80:0	1	1000	60	40:40:0	1	1000	30	0:40:0	0.5	Slow
11	80:0	1	1000	40	40:40:0	1	1000	20	0:40:0	0.5	Fast
12	80:0	2	1000	90	40:40:0	2	1000	30	0:40:0	2	Fast
13	80:0	2	1000	90	40:40:0	2	1000	30	40:40:0	2	Slow
14	80:0	2	1000	90	40:40:0	2	1000	20	0:40:0	1	Fast
15	80:0	2	1000	30	40:40:0	2	1000	30	0:40:0	1	Fast
16	80:0	2	1000	40	40:40:0	2	1000	30	40:40:0	2	Slow
17	80:0	2	1000	40	40:40:0	2	1000	20	0:40:0	1	Fast
18	80:0	2	1000	40	40:40:0	2	1000	10	0:40:0	1	Fast
19	80:0	4	1000	60	40:80:0	5	1000	30	0:80:0	2	Fast
20	80:0	4	1000	60	40:80:0	5	1000	30	40:80:0	5	Fast
21	80:80	6	1000	60	30:80:10	6	1000	30	0:80:80	6	Fast
22	80:0	4	1000	60	40:80:0	4	1000	7	0:80:0	2	Fast

23	80:0	4	1000	60	40:80:0	4	1000	5	0:80:0	2	Fast
24	80:0	4	1000	60	40:80:0	4	1000	50	0:80:0	4	Fast
25	80:0	4	1000	60	40:40:0	5	1000	30	0:40:0	4	Fast
26	80:0	4	1000	60	40:40:0	5	1000	5	0:40:0	4	Fast
27	80:0	4	1000	60	40:40:0	4	1000	30	0:40:0	4	Fast
28	80:0	4	1000	60	40:40:0	4	1000	5	0:40:0	4	Fast
29	80:0	4	1000	60	40:80:0	9.1	1000	10	40:80:0	8.9	Fast
30	80:0	2	1000	90	40:40:0	2	1000	30	0:30:0	2	Slow
31	80:0	2	1000	60	40:80:0	2	1000	30	0:40:0	2	Fast
32	80:0	4	1000	60	40:80:0	9.7	1000	20	40:80:0	9.5	Fast
33	80:0	4	1000	60	40:80:0	9.7	1000	20	40:80:0	9.5	Fast
34	80:0	4	1000	60	30:40:0	4	1000	30	0:40:0	4	Fast
35	80:0	4	1000	60	40:40:0	4	1000	30	0:40:0	4	Fast

7.2 Vertical CVD Graphene Growth Recipes

Sample	Annealing				Growth				Cooling		
	H_2:Ar (sccm)	**P (mbar)**	**T (°C)**	**t (m)**	**CH_4:H_2:Ar (sccm)**	**P (mbar)**	**T (°C)**	**t (m)**	**CH_4:H_2:Ar (sccm)**	**P (mbar)**	**Type**
1	5:0	5	1050	15	45:5:0	5	1050	30	45:5:200	5	Slow
2	5:0	5	1050	15	6:3:0	5	1050	30	6:3:200	5	Slow
3	5:0	5	1050	15	8:2:0	5	1050	30	8:2:200	5	Slow
4	5:0	4	1050	15	8:2:0	4	1050	30	8:2:200	4	Slow
5	5:0	2	1050	15	8:2:0	2	1050	30	8:2:200	2	Slow
6	5:0	5	1050	15	8:8:0	5	1050	30	8:8:200	5	Slow
7	5:0	2	1050	15	32:8:0	2	1050	30	32:8:200	2	Slow
8	64:0	5	1050	15	64:8:0	5	1050	30	64:8:200	5	Slow
9	64:0	2	1050	15	64:8:0	2	1050	30	64:8:200	2	Slow
10	5:0	4	1050	60	32:8:0	4	1050	30	32:8:0	4	Slow

11	64:0	5	1050	15	64:4:0	5	1050	30	64:4:200	5	Slow
12	64:0	2	1050	15	64:4:0	2	1050	30	64:4:200	2	Slow
13	64:0	2	1050	15	64:2:0	2	1050	30	0:0:200	2	Slow
14	64:0	5	1050	15	64:2:0	5	1050	30	64:2:200	5	Slow
15	5:0	4	1050	60	32:8:0	4	1050	30	32:8:0	4	Slow

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