Available online at www.sciencedirect.com

ScienceDirect

Procedia Engineering 00 (2012) 000–000

Procedia Engineering

www.elsevier.com/locate/procedia

Proc. Eurosensors XXVI, September 9-12, 2012, Kraków, Poland

Implementation of a single supply pre-biasing circuit for piezoelectric energy harvesters

Alwyn D. T. Elliott[a*], Paul D. Mitcheson[a]

[a]*Department of Electrical and Electronic Engineering, Imperial College, London, SW7 2AZ, UK*

Abstract

Increased output power can be obtained from piezoelectric energy harvesters by using switching circuits that modify the charge on the material at the extremes of cantilever travel. Here we present an implementation of the most efficient of these charge modification techniques, single-supply piezoelectric pre-biasing. We describe practical results from this scheme and circuit details, including power processing components and control circuits. The power circuit current paths are synchronously commutated with MOSFETs, removing inefficient diode voltage drops. The control circuit is implemented using low power discretes. A useful output power of 2.6 mW was achieved after a 400 μW reduction required for the control circuitry. This is a factor of 4.3 greater than when the harvester was connected to a passive diode bridge and is greater than can be achieved by other piezoelectric interface circuits using an inductor with the same Q-factor.

© 2012 Published by Elsevier Ltd.

*Key*words: bidirectional switches; energy harvesting; piezoelectric, pre-biasing

1. Introduction

Mechanically excited piezoelectric energy harvesters produce a sinusoidal output voltage which must be rectified in order to power a load circuit. The simplest method of achieving this is to connect a diode bridge to the output to charge a battery or capacitor, but the electrical damping achieved with this arrangement is poor and this in turn limits the electrical power generated. In order to maximise the power generated by an energy harvester, the electrical damping should be set to limit the mass motion to just within the end-stop limits, or set equal to any parasitic damping in the system, whichever is greater [1]. Several circuits have been presented which increase the electrical damping and the implementation of one of those, the single supply pre-biasing technique, is the subject of this paper.

The power generated with a piezo and diode bridge can be maximised by setting the output voltage, Vout, to an optimised value derived in [2]. The theoretical maximum power is then equal to $f_0 C_p (V_{po}-2V_D)^2$ where f_0 is the mechanical excitation frequency, C_p is the piezo capacitance, V_{po} is the piezo open circuit voltage, and V_D is the forward voltage drop across a diode. The circuit is self-commutated and so only control of V_{out} is required to maximise power generation.

A more advanced technique, Synchronised Switch Harvesting on Inductor (SSHI) flips the charge on the piezoelectric material at the extremes of the cantilever travel by closing a switch, causing the piezoelectric force to always act in the opposite direction that the cantilever tip is travelling in, effectively increasing the electrical damping. The SSHI topology has demonstrated a gain of 4.5 times that of the bridge rectifier including its control overhead [3]. The theoretical maximum power extraction for SSHI was derived in [4] and is given here in equation (1) where Q is the Q-factor of the switch-capacitor-inductor current path for the charge inversion process.

$$P_{SSHI} = V_{po}^{\ 2} f_0 C_p (4Q/\pi) \qquad (1)$$

* Corresponding author. Tel.: +44-781-728-3034.
E-mail address: alwyn.elliott07@imperial.ac.uk.

A technique known as piezoelectric pre-biasing (PPB) was shown in [5] to yield an even greater improvement in output power than the SSHI technique and is detailed in the next section. This work builds on earlier PPB implementations described in [5, 6].

2. Single Supply Pre-biasing circuit operation

The piezoelectric pre-biasing technique, whilst similar in principles to SSHI, performs all energy exchange between the piezo and energy storage element (battery or capacitor) synchronously through switches [5]. The implementation discussed here, called Single Supply Pre-Biasing (SSPB) is an efficient implementation of the concept as it requires a minimal number of circuit components compared to the originally proposed circuit [5]. The circuit consists of an H-bridge with the piezoelectric material connected in series with an inductor across the bridge legs as shown in Fig. 1(a). The switches are operated in pairs (S_1-S_4 and S_2-S_3) to control current flow between the pre-bias V_{cc} rail and the piezoelectric material. The open circuit sinusoidal voltage across the piezoelectric material increases above the supply rail voltage and so the switches must be capable of bidirectional voltage blocking.



Fig 1: (a) Single supply pre-biasing circuit; (b) Charge and discharge waveform.

When the piezo cantilever is in its maximum position, a charge is placed on C_p, by closing one pair of switches for half a cycle of resonance of the LC_p circuit, causing a resonant pulse of current to flow from V_{cc} into the piezoelectric capacitance, pre-biasing the piezoelectric material to a voltage of V_{PB} (Fig. 1(b)). The piezoelectric element then moves, and the change in stress on the piezoelectric material causes the voltage on C_p to increase approximately sinusoidally, reaching a maximum when the cantilever reaches the opposite extreme of motion. At this point, the same set of switches briefly closes, discharging the capacitor into V_{cc}. The second pair of switches then close to pre-charge the piezoelectric material with the opposite polarity and the cycle repeats. In all cases the switch pairs are closed for exactly a half resonant cycle of the LC_p components and so the switches open at a zero current crossing. The theoretical maximum SSPB power extraction has been derived in [4] and is given equation (2). It can be seen that this circuit has the ability to generate twice as much power as the SSHI technique.

$$P_{SSPB} = V_{po}{}^2 f_0 C_p (8Q/\pi) \qquad (2)$$

3. Circuit Realisation

3.1. Peak Detection

For maximum power extraction it is crucial that the switches are fired at either the piezoelectric voltage waveform maxima or minima. A secondary piezo, mechanically connected to but electrically isolated from the generator piezo provided a sinusoidal in-phase sense voltage for determining when the switches should fire.

A very high input impedance op-amp was used to measure the sense piezo voltage, however a DC offset voltage was required to level shift the signal eliminating the need to generate a negative voltage rail (Fig. 2(a)). By comparing the sense signal instantaneous value to a lossy peak-hold copy held on a capacitor, a peak can be detected by the comparator's negative going edge. The outputs are pulled high when the input signal exceeds the reference voltage and low when the input signal falls below the reference voltage.

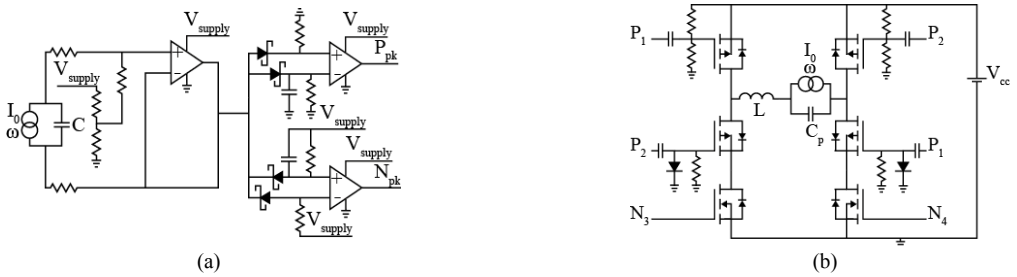


Fig. 2: (a) Peak detection circuit schematic; (b): SSPB switch arrangement schematic.

3.2. Timing

The switches in the power circuit need to be held on for one electrical resonance half cycle in order to ensure that the switches are opened under zero current conditions. Gate drive pulses can be implemented at the required times for a specific on-time through the use of monostables. Either the maximum or minima peak detector output will trigger the first switch pair through a monostable to discharge the piezoelectric capacitance into V_{cc}. Then, the monostable falling edge can be used to trigger the second switch pair to pre-charge the piezoelectric using a second monostable. The order is then reversed upon triggering of the opposite peak detector output.

3.3. Switch Implementation

The switches S_1-S_4 must be able to both conduct and block in both directions. TRIACs provide this functionality, however their operation is too slow. An n-type BJT series connected with a diode then parallel connected to p-type BJT with a series connected diode as suggested by [7] would work, however it suffers from voltage drop across the diodes and the BJTs in the on-state reducing efficiency.

An improved solution is to use series connected n-type and p-type MOSFETs for the low-side switches and a single p-type MOSFET for the high-side switches, as shown in Fig. 2(b). Only a single device is required on the high-side as the low-side switch prevents a conduction path from forming. This arrangement has very fast switching speeds, and low on-state voltage drops. There is a requirement for both a positive and negative gate-source voltage to be generated on the low-side. However, this is possible with a suitable gate drive circuit.

3.4. Gate Drive Circuit

Three types of signals need to be generated to control the MOSFETs (high-side p-type, low-side n and p-type), where the command signals are generated from the output of monostables and simple low-power logic. The command signals therefore need to be referenced to the correct levels for driving the gates in as low power way as possible. The simplest to control are the low-side n-type MOSFETs, as these can be driven directly from the output of the timing circuitry since their source terminal is connected to ground.

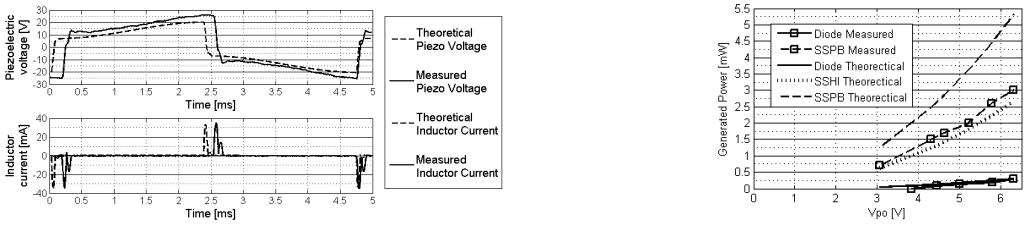
The low-side p-type MOSFET's gate signal needs to be level shifted so that it switches between $-V_{supply}$ and ground and this can be accomplished with a simple capacitor and diode arrangement (Fig. 2(b)). The high-side p-type MOSFET's source was connected to the V_{supply} rail and a potential divider was DC-decoupled from the timing circuitry and connected to the gate terminal. When the signal from the timing circuitry was high, the gate voltage floats towards V_{cc}. When it was pulled low, the gate voltage falls and a negative voltage between the gate and source terminals turning on the MOSFET. Consequently, all of the MOSFETs can be controlled by simple monopolar signals without the need to use isolated gate-drive circuits, hence maintaining low power operation.

4. Results

The circuit was simulated using Orcad Capture v16.5 and implemented using the same parts chosen to minimize power consumption. The switches were constructed from BSH201 for the p-type MOSFETS and BSS138 for the n-type as they were able to block the required 60 V and conduct 300 mA of continuous current. For the peak detection circuit, Analog's AD8500 amplifier was chosen for the differential amplifier and Microchip's push-pull MCP6542 comparator was used to generate the peak-detect signals. A deglitching circuit was also included comprised of an AND gate and a D-type flip flop to prevent spurious switching signals.

The gate signal generation circuit was constructed from two falling edge triggered CD74HC221 monostables and some low power CMOS logic. The ICs are non-retriggerable ensuring switch pulses are not extended due to glitching. Sense and generation piezos were constructed from two Kingstate KPSG-100 piezoelectric loudspeakers, connected together in the centre and glued around the edge. The edge was connected to a shaker driven by a signal generator so that both devices could freely oscillate in phase when mechanically excited. The Q-factor of the circuit was measured by applying a step voltage and observing the ring-down envelope. The harvester piezoelectric was found to have a capacitance of 52.9 nF with a resonant circuit Q-factor of 5.8. A 7.5 mH inductor was used.

Fig. 3(a) shows the piezoelectric voltage and the current through the inductor as simulated and measured in the prototype circuit. The two peaks in the inductor current are due to the discharge and pre-charge of the piezoelectric material at the point of switching. It can be clearly seen that the first curve is greater than the second hence there is a net power gain (as both currents flow into and out of the same voltage source).



(a) (b)

Fig. 3 (a): Measured versus simulated waveforms for piezoelectric voltage and inductor current; (b): Measured bridge rectifier and SSPB power output versus theoretical bridge rectifier, SSHI and SSPB limit

A Yokogawa WT210 Digital Power Meter measured the power generated into the V_{cc} rail and was used to characterise the 400 µW power consumption during operation of the control and gate drive circuits. Powers of 3 mW were readily generated at excitation frequencies of around 200 Hz, giving a useful power output of 2.6 mW.

Fig. 3(b) shows the power generated for both the SSPB (without the control overhead deducted) and bridge rectifier circuits as a function of V_{po} at 200 Hz excitation with the same piezo under optimal conditions. The vibration amplitude was increased in order to increase V_{po}. A power gain of around 6 was obtained through the use of the SSPB circuit. Equation (3) suggests that the maximum power gain possible using the SSPB circuit with the Q-factor achieved in the experiment is 15, suggesting that further improvements in switch fire timing, as well as control power overhead would allow further significant improvements to the useful generated power.

5. Conclusions

In this paper we have presented details of the implementation of a single supply pre-biasing circuit for piezoelectric energy harvesters, including the power processing circuit and control circuit. The H-bridge configuration requires the switches to be capable of blocking voltage in both directions, and so a double MOSFET arrangement of one n-channel and one p-channel FETs were used on the low-side. Control circuitry was implemented using low power discretes and was found to consume 400 µW when the circuit was operating.

Thus the SSPB circuit was shown to improve the power extracted from a piezoelectric harvester by 6 times over what can be achieved with a diode rectifier (4.3 times when the control overhead is subtracted). Contrastingly, the maximum power gain achieved in a recent paper using the SSHI technique at power levels in the mW range was 4.5 [3], however the inductor Q-factor was higher. Further improvement to the gain factor will require improved switch timing and lower power consumption of the control circuit.

Acknowledgements

This work was supported by EPSRC under grant number EP/G070180/1, "Next Generation Energy-Harvesting Electronics: Holistic Approach".

References

[1] P. D. Mitcheson, E. K. Reilly, T. Toh, P. K. Wright and E. M. Yeatman, “Performance limits of the three MEMS inertial energy generator transduction types,” *Journal of Micromechanics and Microengineering,* vol. 17, no. 9, pp. 211-216, September 2007.

[2] G. Ottman, H. Hofmann, A. Bhatt and G. Lesieutre, “Adaptive piezoelectric energy harvesting circuit for wireless remote power supply,” *IEEE Transactions on Power Electronics,* vol. 17, no. 5, pp. 669-676, September 2002.

[3] M. Lallart, C. Richard, L. Garbuio, L. Petit and D. Guyomar, “High efficiency, wide load bandwidth piezoelectric energy scavenging by a hybrid nonlinear approach,” *Sensors and Actuators,* vol. 165, no. 2, pp. 294-302, February 2011.

[4] J. Dicken, P. D. Mitcheson, I. Stoianov and E. M. Yeatman, “Power-Extraction Circuits for Piezoelectric Energy Harvesters in Miniature and Low-Power Applications,” *IEEE Transactions on Power Electronics,* in press 2012.

[5] J. Dicken, P. D. Mitcheson, I. Stoianov and E. M. Yeatman, “Increased Power Output from Piezoelectric Energy Harvesters by Pre-Biasing,” in *PowerMEMS 2009*, Washington DC, USA, pp. 75-78, 2009.

[6] J. Dicken, P. D. Mitcheson, A. Elliott and E. M. Yeatman, “Single-Supply Pre-biasing Circuit for low-amplitude energy harvesting applications,” in *PowerMEMS*, Seoul, South Korea, pp. 46-49, 2011.

[7] M. Lallart and D. Guyomar, “An optimized self-powered switching circuit for non-linear energy harvesting with low voltage output,” *Smart Materials and Structures,* vol. 17, no. 3, pp. 1-8, June 2008.