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Device fabrication for investigating Maxwell's Demon at room-temperature using double quantum dot transistors in silicon

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ABSTRACT

Maxwell's Demon and its development by Szilard to a single particle engine, probe the limits of the 2nd law of thermodynamics and demonstrate a link between entropy and information. With advances in nanofabrication techniques, these thought experiments are becoming feasible. Room temperature (RT) dual-gate double quantum dot (DQD) transistors have been fabricated using electron beam lithography and geometric oxidation. Measurements at RT have shown device operation, where hexagonal patterns have been extracted from the charge stability diagram. These patterns imply ideal underlying characteristics and have been simulated in the form of a series DQD transistor. The boundaries of hexagonal regions correspond to a one-electron exchange between the coupled QDs. Carefully defined gate voltage trajectories crossing these boundaries show the behaviour of Szilard's engine and an identical minimum entropy of $-k_B \ln 2$. These results suggest that DQD devices, even those that operate at RT, can be used to investigate the limits of the 2nd law of thermodynamics.

1. Introduction

In 1867 James Clerk Maxwell [1–3] proposed a thought experiment in which the 2nd law of thermodynamics could potentially break down. He envisaged a chamber filled with identical gas particles at temperature T, that was divided into two equal parts by a 'massless' trap door, controlled by an intelligent being, Maxwell's Demon [1,3]. The demon would open the door to allow only fast-moving particles in one direction and only slow-moving particles in the other. This results in a non-uniform energy distribution and temperature difference across the chamber, where one side is hotter than the other. Because entropy can be considered as a measure of disorder, the actions of the demon appear to result in a decrease in the total entropy of the system, without any work being done, thus violating the 2nd law of thermodynamics. This conundrum was refuted by Szilard [4] who realised that to fulfil its role, entropy changes must be occurring within the demon's 'memory' as it had to both identify and erase information concerning the properties of the gas particles. Szilard proposed a single-particle gas engine surrounded by a thermal bath, Fig. 1. Initially, a single particle occupies a container with volume, V, Fig. 1(I). A frictionless partition connected to a piston is then inserted to trap the particle on one side of container, Fig. 1(II). The particle exerts a pressure on the piston forcing it to move, isothermally expanding the volume, Fig. 1(III).

During this isothermal expansion process, work is done by raising a weight connected to the piston. As this process is isothermal, heat is taken from the bath to do work, $W = k_B T \int_{V/2}^{V} dV/V = -k_B T \ln 2$, where k_B is Boltzmann's constant and T, is the temperature of the bath. At the end of the expansion, the piston is removed, and the system is reset, Fig. 1(IV). In the expansion process, energy is converted from the heat bath without any transfer to a heat sink, contradicting Kelvin-Plancks' form of the 2nd law. However, measurement and storage of the particle's location is necessary for the engine's operation and is accompanied by a change in entropy, thereby restoring the 2nd law.

The Szilard engine was recast in a quantum mechanical interpretation by Zurek [5]. In this picture, the single particle could exist as a superposition of energy states in a coupled, double quantum well (DQW), which was formed by the insertion of a barrier into a single potential well. The implication of superposition is that the particle may be on both sides of the barrier and only upon measurement, collapses into one of the wells. Calculation of the change in free energy following measurement gives a result equal to the work done, $W = -k_B T \ln 2$, if the barrier is moved to restore the original, single potential well. The entropy changes in the measurement process are inherent to the restoration of the 2nd law. A Maxwell Demon must gain information regarding the particle location at the start of an engine, thus 'information is physical' [6].

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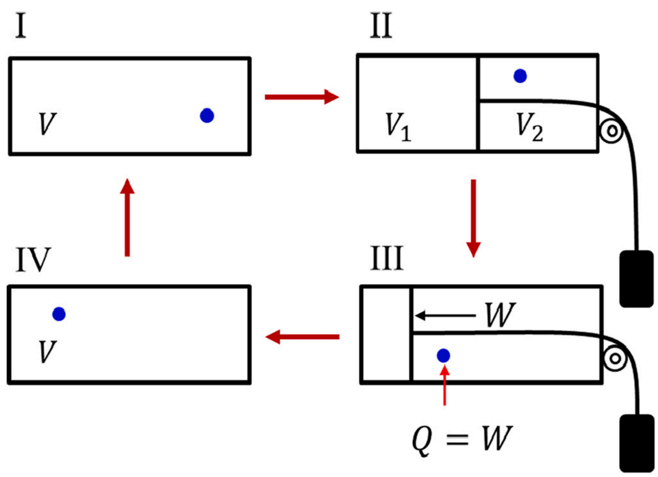

Fig. 1. Szilard's engine. (I) A single particle occupies the entire volume (V) of a container surrounded by a thermal bath. (II) A demon inserts a partition to trap the particle on the RHS. (III) The particle remains at the same temperature, and via isothermal expansion does work. (IV) The system is back to its original state but has done work, $W = k_B T \int_{V/2}^{V} dV/V = -k_B T ln2$.

Advances in nanofabrication and in the understanding of quantum-effect nano-electronic devices have enabled the realisation of the Szilard/Zurek engine by way of semiconductor double quantum dots (DQDs) [7–9]. In this, the single-particle gas is replaced by one electron that is transferred between coupled QDs in a single-electron box and a single-electron transistor (SET) that acts as the Maxwell Demon [7,8]. Furthermore, developments of DQDs based on oxidised silicon – highly doped with phosphorus (P) – has facilitated deep quantum wells and room temperature (RT) operation of SETs [10] and DQD transistors [11]. Electrical measurements of these devices have produced charge stability diagrams that indicate single-electron effects. These charge stability regions may be used to investigate Maxwell's demon at RT.

In this work, RT DQD transistors have been fabricated, where electrical measurements at RT have shown successful device operation. Simulation of the ideal characteristics and emulation of a Szilard engine pave way for understanding the nanoscale thermodynamics of such devices and probe the limits of the 2nd law of thermodynamics.

2. Device fabrication

The devices used in this study have been fabricated in ⟨100⟩ oriented silicon-on-insulator (SOI) wafers having an ultra-thin 12–14 nm thick top Si layer and 25 ± 1.5 nm buried oxide (BOx). The silicon layer was heavily doped using ion-implantation with P at a concentration of ~5 × 10^{20} cm^{-3}. This is shown schematically in Fig. 2a.

The SET patterns, i.e. the devices, access conductors and bond pads, had been designed using AutoCAD software. Prior to electron beam exposure the pattern data was prepared using the GenISys BEAMER software. As part of this process the patterns were divided into 'coarse' and 'fine' regions, with the central areas around each SET (~ 200 μm × 200 μm) being the 'fine' regions. The data was fractured, and proximity corrected with appropriate doses ascribed. A Raith-Vistec VB6-UHR machine operating at 100 kV was used for electron beam exposure. The pattern was defined using a bilayer resist lift-off structure, consisting of ~40–50 nm thick PMMA (MW 100 k) beneath a second layer ~40–50 nm thick 950 k MW PMMA, with both layers sequentially post-baked at 180^o C for 180 s. The central device area (200 μm × 200 μm) was written with a 7.8 nA beam (estimated diameter 2–3 nm) and the outer area (interconnect and bond pad regions) with a 184 nA beam (estimated diameter 70 nm). The areal dose was ~600 μC/cm^2 for the large areas and with the fine features increased by a factor (~1.4–1.7). The exposed resist was developed in MEK:MIBK:IPA in the ratio 1:5:15 for 10 s followed by 100% IPA rinse and then blown dry (see Fig. 2b). A thin layer of Al (~ 30 nm) was deposited by thermal evaporation at a pressure ≈ 10^{-7}–10^{-6} mbar and a resist lift-off undertaken in acetone.

The Al pattern acted as a mask to etch the doped Si layer to give a trench isolated pattern, being transferred into the underlying oxide by reactive ion etching to a depth of 200 nm using SF_6 (30 sccm), O_2 (10 sccm), with power 100 W at a potential of 200 V, pressure 100 mTorr, temperature 20 °C and time 1 min (Fig. 2c). The Al mask was removed by wet etching in ~3% HCl (Fig. 2d).

Samples were oxidised in a tube furnace at 900 °C for 15 mins in oxygen with a ramp time of 1 h to maximum temperature, followed by

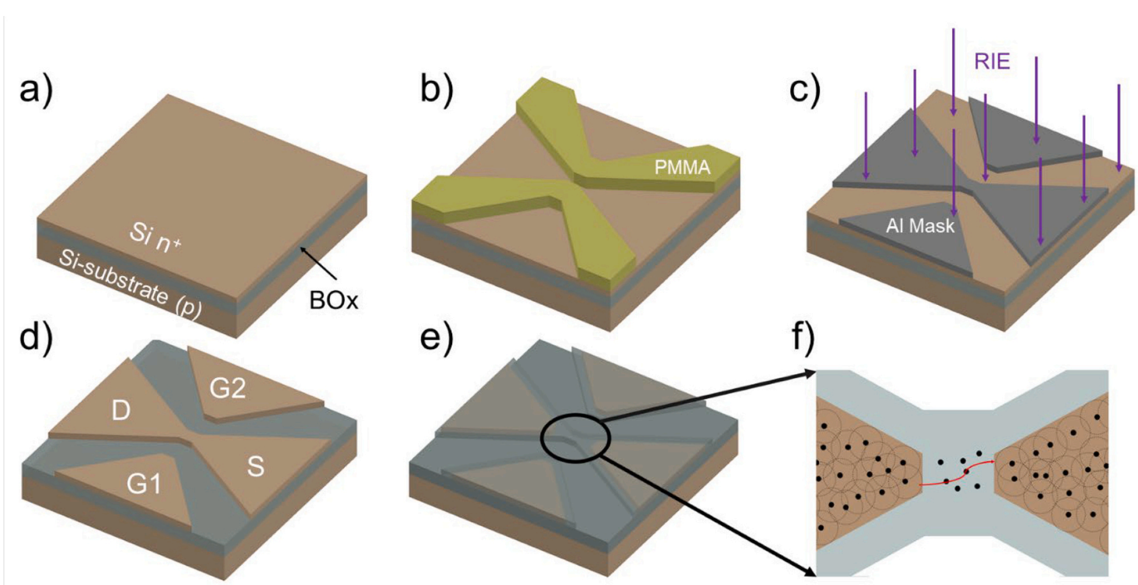

Fig. 2. Schematic representation of the key process steps used to create room temperature devices for room temperature double quantum dots. (a) Silicon-on-insulator wafer with buried oxide layer (BOx) and thin heavily n-doped top silicon (~10^{20} cm^{-3}). (b) Bilayer poly(methyl methacrylate) (PMMA) after patterning by electron beam exposure for aluminium lift-off. (c) Deposited Al is used as a mask for reactive-ion etching (RIE) of the top silicon layer. (d) Silicon structure on BOx after RIE. (e) Structure following geometric oxidation to form the source (S), drain (D), and gate electrodes (G1, G2), together with QDs. (f) High resolution schematic of the gap between source and drain showing the phosphorus dopant atoms.

natural cooling to room temperature. This formed a SiO_2 layer ~15 nm thick on the surface of the device and also served as a geometric oxidation process resulting in a complete oxidation of the point-contact region in the silicon pattern, thereby forming the source and drain electrodes, while at the same time creating quantum dots, (Fig. 2e). These dots were not islands of silicon, because in the gap the Si had been fully oxidised to SiO_2, but as earlier studies had shown [10], these were the phosphorus dopant atoms, (Fig. 2f). Thus, using standard processing tools and techniques, this process had facilitated the formation of quantum dots, smaller than the lithographic limits. This method has similarities to the doping of Si nanocrystal in SiO_2 layers formed by annealing of Si rich layers, of great current interest for solar cell applications [12,13]. Here, P or B dopant atoms may be incorporated in the SiO_x or SiO_2 matrix which encapsulates the nanocrystals. Furthermore, our results suggest that the encapsulation of QDs in a grown or deposited insulating matrix is a promising technique to obtain RT operation of ~1–10 nm QDs synthesised even by other methods, e.g. well-controlled Ge or InAs QD formation from Ge or InAs epitaxial wetting layers on Si or GaAs substrates [12,14].

Contact windows were opened in this oxide to the silicon conductors and with bond pads formed using photolithography. Photoresist S1828 was spin-coated at 500 rpm for 10 s, and then at 4500 rpm with an accelerating rate of 1000 for 50 s, to form a resist layer ≈ 3.5 μm thick. This was baked, first on a hotplate at 65 °C for 1 min then at 85 °C for 1 min, finally an oven bake at 115 °C was used for 1 min. A dark field mask was exposed using a power density of 5.3 mW/cm^2 for 160 s and developed in MF319 for ~2 min, followed by a descum for 3 min and a HF dip for 1 min. The same mask was used again to form a lift-off structure, but with a slight under-exposure to ensure that contact was only made to the doped silicon below. A metal layer consisting of ~20 nm Cr and ~ 200 nm Al was deposited by evaporation. Optical and SEM micrographs of the final device are shown in Fig. 3. The chips were covered with a protective layer of PMMA ~400 nm thick and were diced as required using a Spectra Physics Talon UV laser micromachining system (wavelength 355 nm, max. Power 40 watts). To cut-through the substrate 60 repeat passes at 75% maximum power were used. The PMMA was removed in acetone.

3. Electrical characteristics

The RT electrical characteristics of the DQD transistor were measured using an Agilent 4155B parameter analyser. The source – drain current (I_{ds}) was measured as a function of two gate voltages, V_{gs1} and V_{gs2}, shown in Fig. 4. Ideally, for a DQD transistor, the $I_{ds} - V_{gs1}$, V_{gs2} characteristics appear as sharp current peaks [15,16], commonly referred to as triple-points, that form hexagonal regions of charge stability, where each hexagon corresponds to the average additional number of electrons on the associated QD [15,16]. However, in Fig. 4, non-ideal current features appear due to the random distribution of P dopants in the point-contact region, yet underlying ideal characteristics remain. Here, the current peaks are broadened and smeared due to RT operation, in contrast to sharp, well-defined current peaks at cryogenic temperatures.

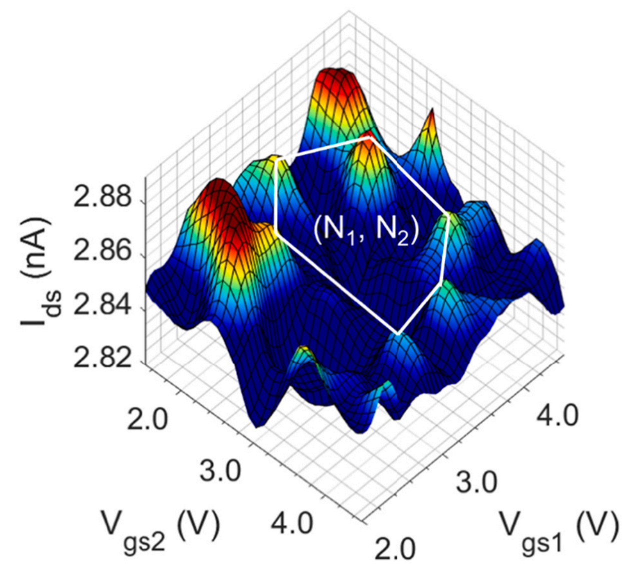

Fig. 4. Charge stability diagram ($I_{ds} - V_{gs1}$, V_{gs2}) of the DQD transistor device at RT = 290 K. A hexagon is superimposed to identify underlying ideal series DQD features.

The extracted hexagon in Fig. 4 is irregular and distorted because the effective capacitances and resistances vary with respect to the gate voltages [11]. $N_{1(2)}$ indicate the average additional number of electrons on $QD_{1(2)}$. Other hexagonal regions may also form and can be attributed to neighbouring DQD complexes [11]. Underlying hexagonal patterns in the electrical characteristics further suggest that there is a dominant DQD complex contributing to the device current. The extracted hexagon pattern allows for the emulation of Szilard's engine in these types of devices. Hexagon regions and boundaries dictate voltage values that may be used to define a trajectory for observing Szilard's engine and calculating entropy changes in this system.

4. Monte Carlo simulation and Szilard engine emulation

A dominant DQD complex is the main path of current flow in the device, however, given the fabrication methodology, multiple QDs may also contribute to the current magnitude and charge stability characteristics. A possible representative circuit can be seen in Fig. 5a, where QD_1 and QD_2 form the main DQD complex, but QD_3 and QD_4 may also be tunnel coupled or capacitively coupled to other parts of the circuit. As underlying hexagons are present in the experimental measurements, for simplicity when emulating the Szilard engine, only the series DQD circuit (solid lines in Fig. 5a) is considered.

Typically, DQD simulations calculate QD energies and electron tunnelling rates for tunnel barriers coupling the QDs and other parts of the circuit. These calculations are essential for investigations into the

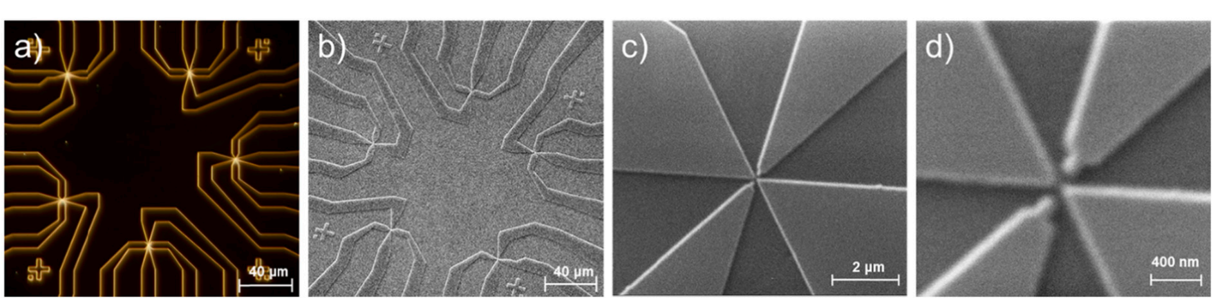

Fig. 3. Optical and SEM micrographs of the device. a) A darkfield image of the device. b) A scanning-electron micrograph (SEM) of the device. c) and d) Magnified SEMs of a single device showing two gates (reduced at the tip to enable a closer approach to the QD and the point-contact region).

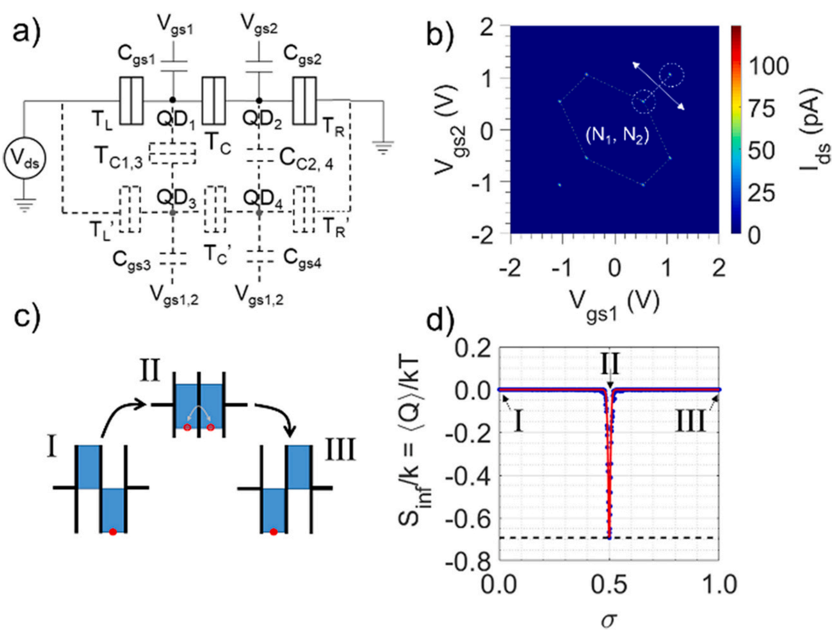

Fig. 5. a) Device circuit showing possible configurations (dotted lines) owing to random distribution of P atom QDs within the point-contact region. Solid lines represent the DQD series circuit used for simulation. b) Monte Carlo simulation of the series DQD from a) at 4.2 K. A hexagon region is outlined, and the Szilard engine trajectory is defined (forward-backward arrow). Degeneracy is indicated by the line connecting the two triple-points encircled. c) Energy band diagram for the trajectory defined in b). I and II are at the centre of each hexagon region, while III is at degeneracy. d) Entropy changes along the trajectory, with regions I – III labelled.

underlying device physics of, e.g., QD transistors [10] and recent, third generation QD based solar cells [12,13].

Here, we use a single-electron Monte Carlo circuit simulator to calculate electron tunnelling rates and the current vs dual gate voltage charge stability diagram for a series DQD transistor (Fig. 5a). In Fig. 5b, the $I_{ds} - V_{gs1}$, V_{gs2} plot is shown for a constant value of $V_{ds} = 100$ μV at a temperature of 4.2 K. The selected capacitance values ($C_L = C_R = C_C = \sim$ 1aF, $C_{gs1} = C_{gs2} = \sim 0.1$ aF) used in the DQD simulation are similar to those found in our previous works on RT QD and DQD devices [12,13], which can be calculated from the dimensions charge stability diagram shows sharp current the extracted hexagon [8]. In addition, the peaks that may be inter-connected to form of hexagonal regions (grey dotted hexagon), where the average additional number of electrons on each QD is defined by (N_1, N_2).

To emulate the Szilard engine in the DQD system, a gate voltage dependent trajectory that crosses degeneracy between the centres of adjacent hexagonal regions is defined (forward-backward arrow in Fig. 5b). Following this trajectory, a single electron is transferred between QD_1 and QD_2 and crosses the (0,1) – (1,0) boundary, therefore a single electron moves from QD_2 to QD_1, similar to a particle moving from the right side of the container to the left side in Szilard's engine. At degeneracy, the Fermi energies for both QDs align and the electron is delocalised between them, analogous to a particle occupying the entire volume of the container in Szilard's engine (Fig. 1(I)).

Fig. 5c illustrates the energy levels for both QDs at different points along the trajectory. Fig. 5d shows the reduced entropy, S_{inf}/k, vs the voltage parameter σ, where $\sigma = C_{gs1}V_{gs1}/\mid e \mid$, for the entire trajectory, with each point from 5c referenced. The trajectory corresponds to different stages of the Szilard engine. At (I), in both Fig. 5c and d, the particle is precisely on the right QD (QD_2). Here, V_{gs2} pulls the ladder of states in QD_2 below source and drain Fermi energy levels, trapping an electron on QD_2. The information entropy, S_{inf}, is defined using Gibb's entropy for a two state system. Here, $S_{inf} = p_1 \ln p_1 + p_2 \ln p_2$, where $p_{1(2)}$ are the occupational probabilities for $QD_{1(2)}$. Since the electron is on QD_2 with a probability of unity, $S_{inf} = 0$. As the voltage levels change, the system reaches degeneracy, (II). Here, the QD energy levels align, allowing for the electron to occupy both states through superposition. The occupation probability for QD1 and QD2 are equal, $p_1 = p_2 = 1/2$, hence, $S_{inf} = -k \ln 2$, similar to the limit defined by Szilard (*sec.* 1, Fig. 1). Further changes along the trajectory bring the system's entropy back to 0, however, this time the electron is trapped on QD_1 (III).

5. Summary

Double-QD transistors have been fabricated using electron beam lithography, followed by geometric oxidation to create tunnel junctions, where a random distribution of P dopant atom QDs are embedded within a SiO_2 point-contact region. This fabrication process facilitates RT DQD transistor operation. Electrical characteristics show broadened current peaks that form distorted hexagonal patterns, implying QD interactions at RT. Distortions to the hexagon are caused by changes in effective device parameters with respect to the gate voltages, and nearby DQD complexes [10]. Simulations at cryogenic temperatures showed ideal hexagon patterns, which appear as underlying features in the charge stability diagram of our device. These simulations have been used to understand the entropy limits in a DQD system, by emulating Szilard's engine, which is examined by defining a voltage trajectory that passes through degeneracy. It is found that the minimum entropy extracted in a DQD transistor device is the exact minimum found in Szilard's engine. This implies that DQD devices, even those that operate at RT, may be used to probe the limits of the 2nd law of thermodynamics.

Declaration of Competing Interest

The authors confirm that there is no conflict of interest, either between themselves or with the agencies funding this work.

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