

Some Key Aspects of Near-Field Wireless Power Transfer Technologies for High Frequency, High Power, and High Efficiency

Shu-Yuen Ron Hui¹, Fellow, IEEE, Cheng Zhang², Member, IEEE, Kerui Li³, Member, IEEE, Alex M. H. Wong⁴, Senior Member, IEEE, and Siew Chong Tan⁵, Fellow, IEEE

Abstract—Existing wireless power transfer (WPT) applications and standards mainly rely on sub-Mega-Hertz operations and their power level generally decreases with operating frequency. Many emerging WPT applications have limited charging areas and prefer higher frequency operation for fast charging with improved energy efficiency. With the new recommendations by the International Telecommunication Union on the use of Mega-Hertz frequency bands for nonbeam WPT applications, it is imperative to explore new high-frequency WPT technologies. This article presents the hurdles and possible solutions to the uncharted area of high-frequency (MHz), high-power (kW), and high-efficiency (>95%) WPT technologies. For 1–13.56 MHz operation, the technical hurdles include 1) resonator designs suitable for mass production, 2) ultrafast gate drive designs, 3) power inverters with soft switching, and 4) electromagnetic shielding methods for Mega-Hertz WPT applications. Existing solutions and emerging technologies for overcoming the hurdles in these four key aspects of WPT are addressed.

Index Terms—Electromagnetic (EM) shielding, gate drive circuit, magnetic resonance, soft switching, wireless power transfer (WPT).

I. INTRODUCTION

SINCE the launch of the world's first wireless charging standard “Qi” in 2010, wireless power transfer (WPT) has become a fast growing market covering a wide range of applications including portable consumer electronics such as mobile phones and smart watches. According to Fortune

Business Insights [1], the global wireless charging market size was valued at USD 30.75 billion in 2024 and is expected to grow from USD 37.3 billion in 2025 to USD 172.2 billion by 2032.

Formed in 2008 and comprising over 300 company members worldwide, the Wireless Power Consortium (WPC) upgraded the Qi standard from Qi 1.0 to Qi 2.2 with charging power increased up to 50 W for portable consumer electronics with improved energy efficiency. In this upgrade, the switching frequency is changed from the range of 110–205 kHz to 360 kHz. In addition, the WPC is launching a new standard called “Ki” for the wireless charging of kitchen electrical appliances at a frequency around 20–60 kHz for charging power of up to 2.2 kW. Meanwhile, the Society for Automobile Engineers (SAE) has launched the SAE J2954 standard for the stationary charging of light-duty electric vehicles with charging power of up to about 11 kW for WPT3 class and an operating frequency of about 85 kHz. Another industrial group, the Airfuel Alliance, promotes high-frequency (6.78 MHz) WPT applications for charging power of up to 50 W.

With a charging power of 5 W, the first generation of Qi standard contains a wide range of transmitter and receiver designs with the aim of maximizing compatibility to attract many manufacturers to share the same standard. Energy efficiency and charging time were not the prime concerns at that time. With the charging power increasing with new WPT applications to the kilo-Watt level, it was pointed out in [2] that there is a need for a paradigm shift from compatibility to optimal performance in terms of maximizing energy efficiency and minimizing charging time for WPT of the next generation. This paradigm shift is now reflected in the upgrade of the Qi standard in which both energy efficiency and charging time are improved in the Qi2 standard by the WPC.

Fig. 1 shows the power frequency profile of major standards adopted in industry by 2025. There is an uncharted territory for WPT research and development in the high-frequency and high-power region. Operating the WPT system at a higher frequency has certain benefits.

- 1) Consumer electronics with small form factors (such as smartwatches, fitness bands and wireless earbuds) can retain slim and light-weight designs without compromising the charging speed.
- 2) For implantable medical devices such as cochlear implants, neurostimulators and pacemakers, electromagnetic

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Shu-Yuen Ron Hui is with the Department of Electrical Engineering, City University of Hong Kong, Hong Kong, and also with the Department of Electrical and Electronic Engineering, Imperial College London, South Kensington, SW7 2AZ London, U.K. (e-mail: eeronhui@cityu.edu.hk).

Cheng Zhang is with the School of Electrical and Electronic Engineering, The University of Manchester, M13 9PL Manchester, U.K. (e-mail: cheng.zhang@manchester.ac.uk).

Kerui Li and Siew Chong Tan are with the Department of Electrical Engineering, City University of Hong Kong, Hong Kong (e-mail: kerui.li@cityu.edu.hk; siewctan@cityu.edu.hk).

Alex M. H. Wong is with the Department of Electrical Engineering and the State Key Laboratory of Terahertz and Millimeter Waves, City University of Hong Kong, Hong Kong (e-mail: alex.mh.wong@cityu.edu.hk).

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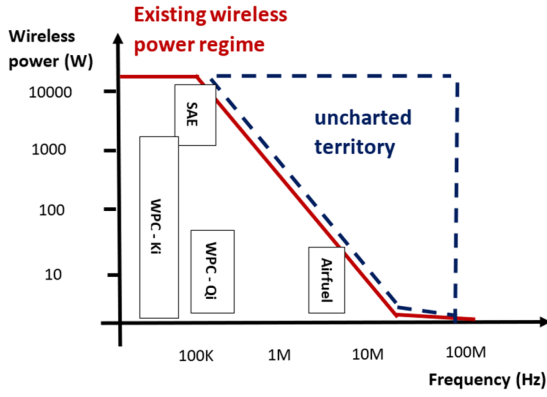


Fig. 1. Power–frequency profile of major WPT standards.

TABLE I
SIX FREQUENCY RANGES RECOMMENDED BY THE ITU FOR NONBEAM
INDUCTIVE OR MAGNETIC RESONANCE WPT TECHNOLOGIES [3]

Band	Frequency range for Non-beam (Inductive or magnetic resonance) WPT technologies	Authors' remarks
A	100-148.5 kHz	Qi1
B	315-405 kHz	Qi2
C	1.700-1.800 MHz	Used by Apple watches
D	2.005-2.170 MHz	
E	6.765-6.795 MHz	ISM
F	13.553-13.567 MHz	ISM

(EM) waves at high frequencies can allow for minimizing device sizes while ensuring safe and controlled charging inside the body.

- 3) For fast charging of relatively high-power applications (such as mobile robots, drones and e-bikes), high frequency (HF) operation can increase the quality factor of the resonators and transmission energy efficiency; and reduces the transmitter and receiver coil areas and charging time.

In September 2024, the International Telecommunication Union (ITU) published the Recommendation ITU-R SM.2191-1: “Guidance on frequency ranges for the operation of nonbeam wireless power transmission for mobile and portable devices” [3]. Table I tabulates the six frequency ranges recommended by the ITU for nonbeam inductive or magnetic resonance WPT technologies.

While the frequency bands of the Qi1 and Qi2 standards fall within the first two frequency bands (A and B) in the kilo-Hertz region, it is important to note that four out of the six frequency bands (C, D, E, and F) are in the Mega-Hertz range. Also, unlike bands A and B with a wide frequency range, these four MHz bands have narrow frequency range. In fact, E and F are of the Industrial, Scientific and Medical (ISM) frequency bands [4]. Therefore, it is imperative to explore the technical challenges in these MHz frequency bands for emerging and future WPT applications.

This article focuses on the technical hurdles and possible solutions in this uncharted territory. It aims at exploring existing and new ideas to form a comprehensive set of WPT solutions

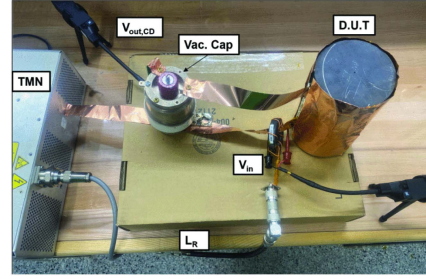


Fig. 2. Prototype and the test setup for the high- Q inductor [6]. (IEEE Copyright).

to achieve HF, high power (HP), and high efficiency (HE). In this context, the HF range refers to 1–13.56 MHz, the HP range refers to 50 W–1 kW and HE refers to 95% or above. Major hurdles for entering this HF, HP, and HE region include at least the lack of the following.

- 1) High-quality resonator design suitable for mass production with precise parameters.
- 2) Gate drive circuits with low latency of 10 ns or less.
- 3) Power inverters with soft switching capability at MHz operation
- 4) Suitable EM shielding materials with low core losses for MHz operation.

The remaining sections of this article will review existing technologies and their limitations and then explore potential solutions to overcome these hurdles.

II. EMERGING TECHNOLOGIES FOR HIGH-QUALITY RESONATORS FOR MEGA-HERTZ OPERATION

Transmission efficiency of the WPT system shows a positive relationship with the quality factor of the resonators and the coupling coefficient between them. For a given coupling coefficient, high-quality resonators naturally lead to higher transmission efficiency. In this section, we will first review existing resonator designs and then introduce some emerging technologies that have the potential to advance the state-of-the-art.

A. Brief Review of Existing Resonator Works for MHz WPT Applications

As the skin effect becomes prominent at MHz frequencies, the corresponding skin depth in conductors decreases significantly. For instance, the skin depth of copper at 1 MHz is only $65.20 \mu\text{m}$. Consequently, the ac resistance of a conductor becomes effectively independent of its total cross-sectional area, provided its dimensions exceed the skin depth at these frequencies [4]. By fully leveraging this phenomenon, high- Q resonators can be constructed using extremely thin conductor layers—closely matching the skin depth—and eliminating the need for Litz wire [5]. Next, we will discuss some new and emerging approaches to realizing these resonators.

1) *Copper Foil-Wound Inductors/Coils*: A high- Q inductor design utilizing copper foil was recently reported in [6]. Fig. 2 shows the prototype and test setup used for large-signal quality factor characterization. This design exhibits an exceptionally

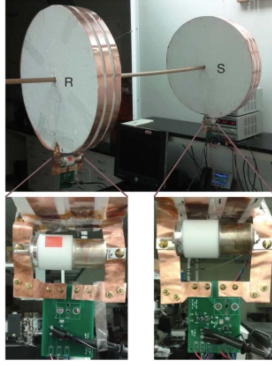


Fig. 3. Copper foil-wound coil for short- to mid-range WPT system [9]. (IEEE Copyright).

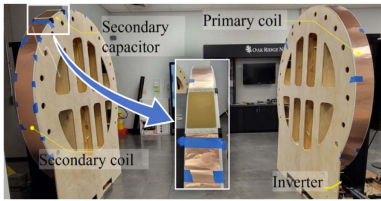


Fig. 4. Copper foil-wound coil for long-distance WPT system [11]. (IEEE Copyright).



Fig. 5. Prototype of the single-turn high-Q coil. (a) Three-dimensional printed coil frame. (b) Copper-plated coil with compensation capacitors and connector [12]. (IEEE Copyright).

high Q factor of 1150 at 13.56 MHz. In addition, the outer copper foil layer serves as EM shielding. The impressive quality factor is attributed to the implementation of a quasi-distributed gap within the magnetic core, which balances the magnetic field distribution and thereby mitigates skin effect loss [7], [8]. Copper foil-wound coils have also been employed for short- to mid-range [9] and long-distance WPT [10], [11], as shown in Figs. 3 and 4, respectively. However, the structural approach demands more intricate manufacturing procedures and higher production costs to ensure consistent performance parameters, making it less favorable for mass production.

2) *Three-Dimensional-Printed Inductors/Coils*: Three-dimensional printing is particularly suitable for customized inductors/coils with complex geometries. A prototype of a single-turn high-Q coil [12], fabricated through a combination of 3-D printing and copper electroplating, is shown in Fig. 5. Specifically, a thin copper layer is electroplated onto a precisely designed 3-D-printed plastic frame [see Fig. 5(a)]. Given the skin depth of $25\ \mu\text{m}$ at 6.78 MHz, the electroplated copper layer is $50\ \mu\text{m}$ thick and is sufficient, ensuring the design will not

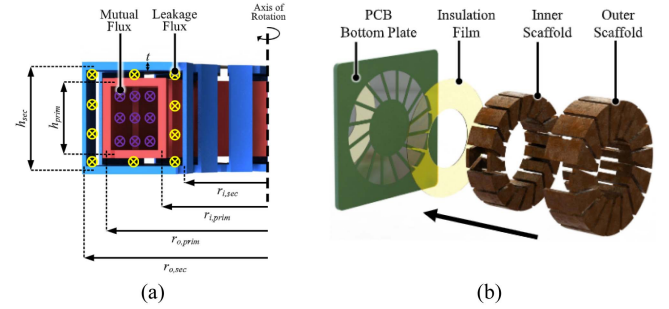


Fig. 6. Three-dimensional printed air-core transformers [13]. (a) Cross section of the 3-D printed air-core transformer. (b) Assembly of 3-D printed air-core transformer. (IEEE Copyright).

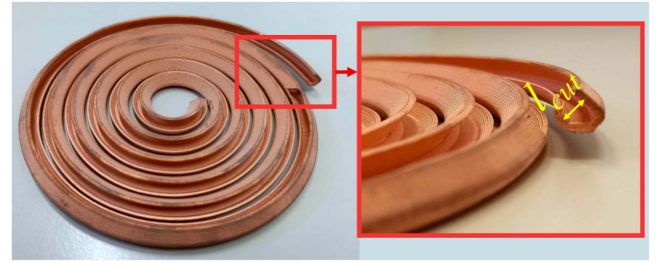


Fig. 7. Metal 3-D Printing for irregular cross-sections [15]. (IEEE Copyright).

be compromised by the skin effect. The single-turn structure effectively minimizes the proximity effect. Furthermore, 3-D printing enables irregular cross-section. Optimization is then performed on this cross-sectional design to minimize eddy current loss and enhance mutual coupling [12].

In addition, 3-D printing can be employed for the fabrication of a toroidal air-core transformer. The toroidal structure effectively confines the magnetic field, thereby enhancing both self-inductance and mutual coupling [13], as shown in Fig. 6. Given that only a thin copper layer ($70\ \mu\text{m}$, as detailed in [13]) is necessary for the inductive components, the overall weight of the reactive component can be substantially reduced. The feature is favorable in some emerging applications such as ion thruster [14].

An alternative to electroplating the plastic frame surface involves using Metal 3-D Printing for the direct fabrication of coil structures with irregular cross-sections. An example of this optimized geometry is shown in Fig. 7, where the low current density region is removed [15]. Conventional practice involves manufacturing a solid structure and then performing subtractive cutting to remove redundant material. In contrast, with 3-D printing, the optimized coil structure is printed directly in its final form. This additive manufacturing method is a more resource-efficient process that leads to material saving.

Similarly, the additive manufacturing and topology optimization method are also applied to the design and optimization of magnetic structures [16], [17].

3) *PCB Inductors/Coils*: The printed technology ensures high consistency in manufacturing, in addition to maintaining low production costs. It also enables the possibility of fully integrated solutions for WPT systems. To maximize space and

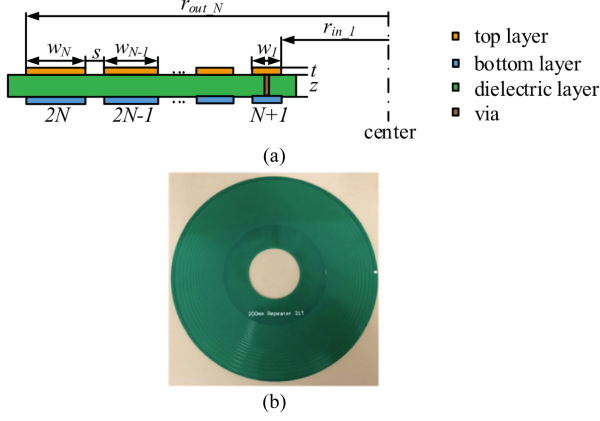


Fig. 8. Existing PCB inductor/coil design, of which copper layers are printed on both sides of the PCB [18]. (a) Cross-sectional view of the PCB coil. (b) Front view of the PCB coil. (IEEE Copyright).

generate sufficient inductance, spiral windings are printed on both sides of the printed circuit board (PCB), as shown in [18] and [19]. Fig. 8 illustrates the cross-section and front views of the PCB coil. A hollow area exists at the center of the PCB coils. This design choice is based on the understanding that the spiral windings in the center do not generate significant inductance, but instead contribute to considerable conduction resistance. Filling the hollow area with spiral windings will adversely affect the overall quality factor, as pointed out in [20].

In addition, this two-layer structure also introduces dielectric loss in the PCB coils. As shown in Fig. 8, the spiral windings on both sides of the PCB create inter-capacitance. The resulting displacement current flows through the dielectric layer of the PCB (i.e., FR4), generating dielectric loss that adversely affects the quality factor [18]. An alternative solution to mitigate dielectric loss is to use high-frequency PCB materials (such as Rogers PCB materials) [19], [21]. While these materials can slightly reduce dielectric loss, they increase the production costs of these PCB resonators several times [22], [23]. Consequently, the benefits of PCB resonators are reduced when compared to competing technologies.

B. Emerging Approaches With Promising Features

1) *Dual-Single-Layer PCB Resonator*: To address dielectric loss issues, a dual-single-layer PCB resonator structure has been proposed [22], [23]. Fig. 9(a)–(c) shows the physical structure and PCB spiral windings of this dual-single-layer PCB resonator. It comprises two single-layer PCBs with air trenches between adjacent turns. The middle layer uses air as the dielectric material, which exhibits nearly zero loss tangent. The spiral patterns of spiral windings can be optimized through a computer-aid approach [24]. The third-order circuit model presented in Fig. 9(d) is used to characterize the resonator. The inductor L accounts for the magnetic field generated by the spiral windings when electrically excited. The capacitor C_p represents the intracapacitance caused by adjacent turns of the spiral windings, and the capacitor C_s is introduced to model the intercapacitance of the middle layer. The two primary

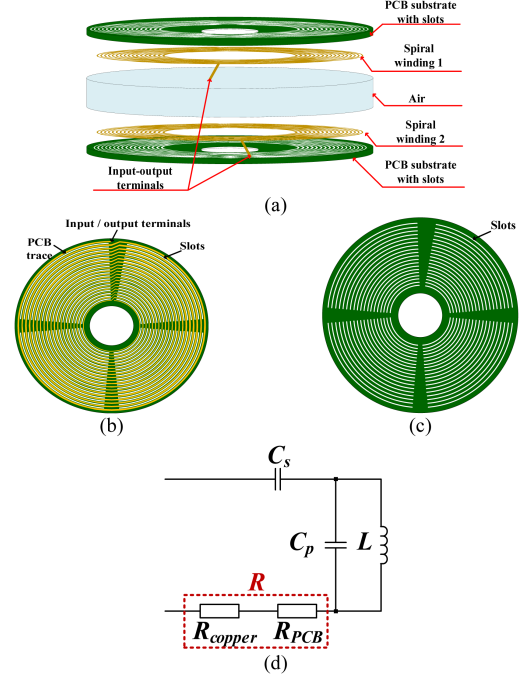


Fig. 9. (a) Physical structure of the dual-single-layer PCB resonator. (b) Front view of the PCB, showing spiral winding and air slots between adjacent turns. (c) Back view of the PCB without printed winding. (d) Equivalent circuit model for the dual-single-layer PCB resonator [22], [23]. (IEEE Copyright).

loss mechanisms in the resonator, copper loss and dielectric loss, are modeled as series-connected resistors, R_{copper} and R_{PCB} , respectively. Compared to conventional designs, where the dielectric loss (R_{PCB}) constitutes 57% of the overall loss resistance, the dual-single-layer PCB resonator exhibits a significantly lower dielectric loss, accounting only for 7.8% of the total loss resistance. This substantial reduction in dielectric loss results in an improvement of over 435% in quality factor and 41% in transmission efficiency relative to conventional design [23].

In addition to the conventional magnetic field coupling mechanism, the dual-single-layer PCB resonator also enables hybrid capacitive and magnetic coupling to enhance transmission capacity [25]. By utilizing asymmetric spiral winding patterns [see Fig. 10(a) and (b)], mutual capacitance C_m between two resonators is generated, leading to capacitive coupling [see Fig. 10(c) and (d)]. To evaluate the WPT system with hybrid coupling, the mixed coupling coefficient is employed [26]. As reported in [25], the mixed coupling coefficient k_{mix} is generally higher than that of pure inductive or capacitive coupling as

$$|k_{mix}| = \frac{|k_{IPT}| + |k_{CPT}|}{1 + |k_{CPT}| |k_{IPT}|} > |k_{IPT}|$$

and

$$|k_{mix}| = \frac{|k_{IPT}| + |k_{CPT}|}{1 + |k_{CPT}| |k_{IPT}|} > |k_{CPT}| \quad (1)$$

where k_{IPT} and k_{CPT} represent the coupling coefficient of the inductive coupling and capacitive coupling path. Complementing theoretical analysis, the experimental results from [27] and [28]

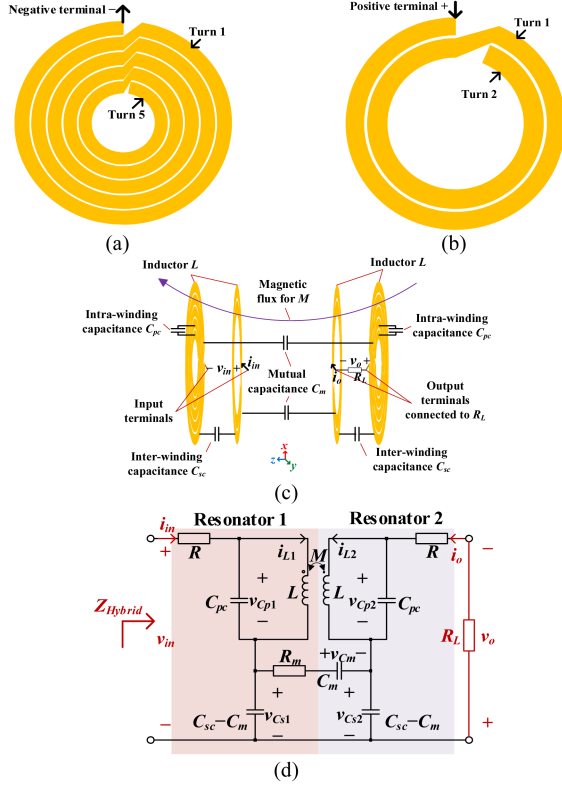


Fig. 10. (a) Spiral winding 1 and (b) Spiral winding 2 of the dual-single-layer PCB resonator with hybrid coupling. (c) WPT system based on dual-single-layer PCB resonators and (d) equivalent circuit model [25]. (IEEE Copyright).

verify the effectiveness of the dual-single-layer PCB resonator [22] over 250 W in the MHz frequency range in a preliminary study. As demonstrated in [12], the single-turn resonator structure effectively minimizes the proximity effect. When the single-turn design is implemented in the dual single-layer PCB resonator structure, the prototype also exhibits an exceptionally high Q-factor of over 1000 [29].

This dual single-layer PCB resonator structure has high potential for high-power applications in the MHz range for several reasons.

- 1) The replacement of the PCB material with air in the airgap between the two printed coils drastically reduces the dielectric power loss arising from high-frequency operation in the PCB.
- 2) With an airgap between the two printed coils, the self-capacitance of the resonator becomes small, enabling the self-resonance reaching the 1 MHz to 13.56 MHz range.
- 3) The reduction of the equivalent resistance R_{PCB} in the equivalent circuit model [see Fig. 9(d)] enables the design of a low-loss and high-Q resonator.
- 4) The possibility of utilizing both inductive and capacitive WPT can improve the effective coupling coefficient.
- 5) This dual single-layer PCB-based resonator structure can be manufactured in mass production.

2) *Multilayer PCB Resonator*: Planar PCB resonators with multiple turns suffer from the proximity effect generated by adjacent turns [20]. An increased number of turns on a single PCB escalates this effect, consequently degrading the quality

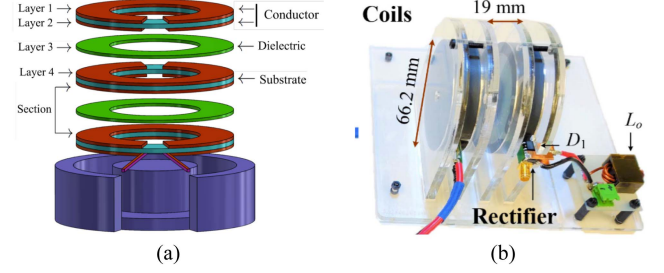


Fig. 11. (a) Multilayer PCB resonator [30] and (b) WPT system formed by two resonators [31]. (IEEE Copyright).

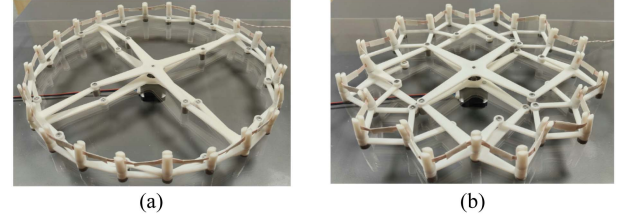


Fig. 12. Motorized flexible inductor [32]. (a) Inductor with a folding ratio of 8.2 grad. (b) Inductor with a folding ratio of 46.7 grad. (IEEE Copyright).

factor. As an effective alternative, the multilayer PCB resonator structure has been proposed [30], [31]. Fig. 11 shows the multilayer PCB resonator and the corresponding WPT system. This design utilizes single-turn windings on each PCB layer, and stacking these layers increases inductance while minimizing losses caused by proximity effects. Furthermore, the incorporation of HF NiZn ferrite further improves the quality factor, reaching 1183 at 7.09 MHz as reported in [30]. Based on this design, the overall transmission efficiency of the WPT system can reach 95% at kilowatts power range [31].

3) *Motorized Flexible Inductor and Switched Capacitor*: To avoid interfering with wireless communication devices, MHz WPT systems commonly utilize ISM bands. However, the ISM bands exhibit narrow bandwidth (less than 0.5% of the center frequency); for example, the bandwidth of the 6.78 MHz ISM band is restricted to 30 kHz, and that of the 13.56 MHz ISM band is restricted to 14 kHz.

Due to factors such as aging or manufacturing tolerances, the nominal values of inductors and capacitors can drift by up to 20%, causing the resonant frequency to fall outside the bandwidth of the ISM bands. In addition, the self-resonance frequency of a WPT system may change with the load resistance. These challenges have motivated research efforts into tunable inductors [32] and capacitors [33] to maintain a consistent resonant frequency. For example, a novel motorized flexible inductor structure (see Fig. 12) in which a mechanical motor precisely adjusts the inductance by altering its folding ratio is presented in [32]. This motorized coil can be used as part of the transmitter resonator in a platform for wireless charging of drones and mobile robots in the 1–13.56 MHz range.

C. Manufacturing Precision and Design Example

1) *Manufacturing Precision Comparison*: Both 3-D printing and PCB manufacturing exhibit high manufacturing precision,

TABLE II
MANUFACTURING PRECISION COMPARISON

	PCB [34]	Plastic 3D printing [35] and copper electroplating [13]	Metal 3D printing [36]
Process	Subtractive (Etching and drilling)	Additive (Layer-by-layer deposition)	
Precision	Minimum copper thickness: 35 μm Minimum clearance between copper tracks: 0.1 mm Minimum copper track width: 0.1 mm Track width tolerance: $\pm 20\%$	Accuracy: $\pm 0.3\%$ lower limit of ± 0.2 mm Minimum wall thickness: 1 mm Copper electroplating thickness: 50–70 μm	Accuracy: $\pm 5\%$ lower limit of ± 0.13 mm Minimum wall thickness: 2 mm
Design Flexibility	Low. Planar structure.	High. Irregular geometry	
Mass Production Cost	Low	High. Only cost-effective for low volume or prototyping	

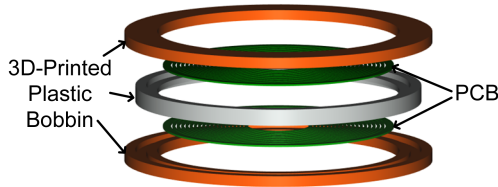


Fig. 13. New design example of the dual-single-layer PCB resonator using 3-D printing to fabricate the bobbin.

but they present tradeoffs in their capabilities for constructing resonators. A comparison is detailed in Table II, where data are collected from mature commercial service providers [34], [35], [36]. PCB fabrication generally offers higher precision. However, this high precision is limited to planar structures, whereas 3-D printing provides a high degree of freedom to realize irregular, nonplanar geometries. PCB manufacturing is suitable for mass production, as its process allows for the simultaneous fabrication of multiple units, leading to a substantial reduction in per-unit cost. Conversely, the cost of 3-D printing increases proportionally with the number of products.

2) *Design Example*: Fig. 13 shows a new design example, where 3-D printing is used to fabricate the bobbin for the dual-single-layer PCB resonator. Due to the precision limits inherent in 3-D printing (i.e., $\pm 0.3\%$ accuracy with a lower limit of ± 0.2 mm), the spacing between the two PCBs may deviate from its nominal value. We evaluate this effect using the resonator design (Design 2) from [23]. Finite element simulations are performed to quantify the influence of the maximum and minimum distance variations on the equivalent circuit parameters [see Fig. 9(d)].

TABLE III
CIRCUIT PARAMETERS OF DUAL-SINGLE-LAYER PCB RESONATOR

	Nominal spacing (5.95 mm)	Maximum spacing (5.95 + 0.2 mm)	Minimum spacing (5.95 - 0.2 mm)
L	37.66 μH	37.62 μH (-0.1062%)	37.66 μH
C_s	49.46 pF	47.99 pF (-2.972%)	51.08 pF ($+3.275\%$)
C_p	25.76 pF	25.06 pF (-2.717%)	26.55 pF ($+2.873\%$)
R	8.429 Ω	8.492 Ω ($+0.7474\%$)	8.504 Ω ($+0.8898\%$)

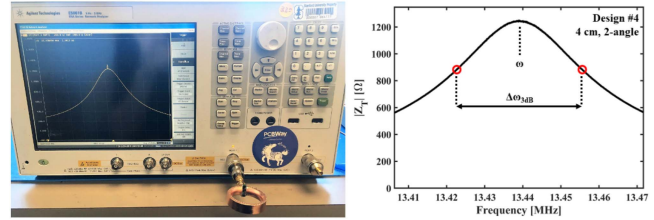


Fig. 14. Direct measurement of high-Q resonator using network analyzer [12]. (IEEE Copyright).

The data outlined in Table III suggest that the effect on circuit parameters is relatively small.

D. Measurement Techniques for Q Factor

1) *Direct Measurement*: The Q factor is determined using the 3-dB bandwidth of the impedance curves obtained from the network analyzer [12] or impedance analyzer [30]. The Q factor is derived as

$$Q = \frac{f_r}{\Delta f} \quad (2)$$

where f_r is the resonant frequency and Δf is the 3-dB bandwidth.

Fig. 14 shows an example of direct measurement [12]. The single-turn coil is connected to the vector network analyzer for measurement. The resonant frequency and 3-dB bandwidth are obtained from the impedance curve and thus derive Q factor.

The result of direct measurement may be affected by the coaxial connector (e.g., BNC connector), which could introduce stray capacitance to the resonator under measurement. Moreover, some resonators may exhibit extremely high or extremely low impedance at their resonant frequency (depending on series resonance or parallel resonance). This impedance could exceed the effective measurement range of the network analyzer or impedance analyzer, thereby compromising the measurement accuracy.

2) *Indirect Measurement*: Alternatively, the Q factor can be determined using noncontact measurement approaches [37], [38], [39], [40]. These techniques involve using small auxiliary coils to inductively couple with the resonator under test. The procedure outlined in [40] is used as an example, and the measurement steps are shown in Fig. 15. First, the input impedance of the auxiliary coil, $Z_{\text{aux}}(f)$, is measured. Second, the resonator under test is placed near the auxiliary coil. Then, the input

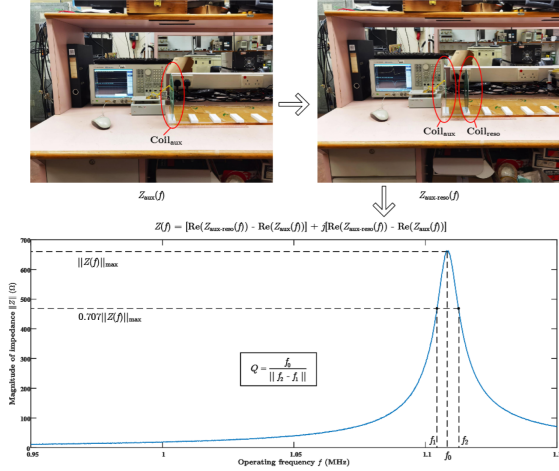


Fig. 15. Noncontact measurement for high- Q resonator [40]. (IEEE Copy-right).

impedance of the auxiliary coil, $Z_{\text{aux-reso}}(f)$, is measured. Third, the resonant frequency and 3-dB bandwidth are obtained from the impedance curve, $Z_{\text{aux-reso}}(f) - Z_{\text{aux}}(f)$, and subsequently derive Q factor.

This noncontact measurement could minimize the adverse effects introduced by the coaxial connector. Moreover, adjusting the distance between the auxiliary coil and the resonator under test allows the impedance curve to be adjusted, ensuring the input impedance remains within the effective measurement range of the network analyzer or impedance analyzer. This method is only applicable to the resonators operating with parallel resonance. The resonators operating with series resonance need to be reconfigured into parallel resonance [23].

E. Summary and Classification of Resonators for WPT

The summary and classification of the selected resonators are provided in Table IV. Based on the manufacturing techniques, the resonators are categorized into four groups: copper foil-wound coils, 3-D-printed structures, PCB-based designs, and variable mechanical structure windings. This categorization highlights the impact of construction on performance; for example, the copper foil-wound coil in [6] and the multilayer PCB resonator [30] achieve extremely high Q factors ($Q > 1000$).

F. Emerging Hybrid Couplers for Mixed Inductive-Capacitive WPT Operations

High-frequency operation in the megahertz range favors the additional use of WPT channel via the electric field. This prompts recent interest in studying hybrid couplers in WPT systems with both inductive and capacitive power flow paths. A hybrid WPT system typically comprises a transmitter coil and receiver coil for inductive power transfer (IPT) and four metallic plates for capacitive power transfer (CPT). A 6.78-MHz hybrid WPT system is reported for notebook computers in [85] Fig. 16, in which a systematic analysis of the inductive and capacitive power flow paths is included. This application is a good demonstration of hybrid WPT because the interface area

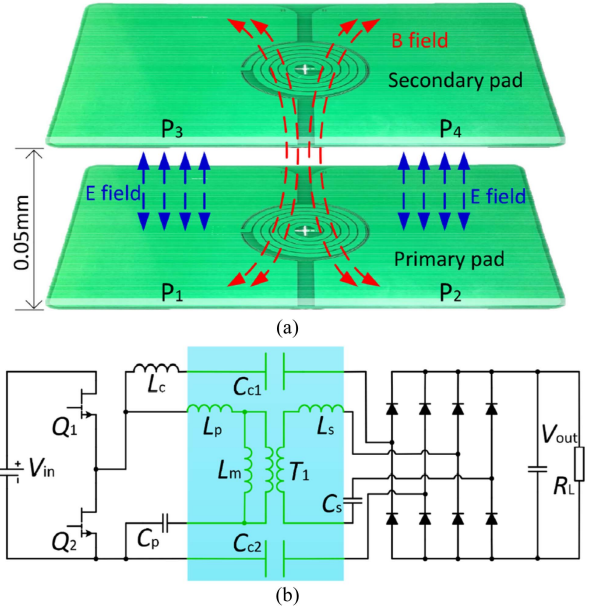


Fig. 16. (a) Structure of a hybrid WPT system for notebook computer and (b) equivalent circuit of the hybrid coupler [85] (Courtesy of Dr. River Li).

between the transmitter pad and receiver pad is sufficiently large to provide substantial mutual capacitive coupling. A comprehensive review on hybrid couplers for WPT is reported in [86]. Hybrid coupling structures have either series or parallel configuration. Their compensated circuit can be separated or shared. The power flow can be designed according to

$$P_{\text{HWPT}} = \alpha_1 P_{\text{IPT}} + \alpha_2 P_{\text{CPT}} \quad (3)$$

where P_{HWPT} , P_{IPT} , and P_{CPT} are hybrid power flow, inductive power flow, and capacitive power flow, respectively; $\alpha_1 + \alpha_2 = 1$. Hybrid couplers are suitable for wireless charging of mobile robots [25] and can be used in multiple forms to achieve HP density and misalignment tolerance [87] and voltage gain [88].

III. EMERGING TECHNOLOGIES FOR HIGH-FREQUENCY GATE DRIVES

A. Brief Review on MHz Gate Drive Integrated Circuits

Gate drive integrated circuits (ICs) are critical components in power inverter circuits for WPT systems. With few exceptions, high-frequency inverters typically require dedicated gate drives. Notable exceptions include the Mazzilli oscillator [41] and the spark-gap triggered oscillator [42], which are uncontrolled switching circuits beyond the scope of this article.

The primary functions of a gate drive circuit include: 1) Switching the power device on and off in response to control signals as quickly as possible, while suppressing voltage overshoots and oscillations; 2) Level-shifting the drive signals relative to the source terminal of a floating MOSFET. In practice, gate drive circuits have limitations that can impact overall system performance. When selecting gate drive ICs, several factors must be considered. Rising and falling times are determined by the IC's source and sink current capabilities, the total gate charge $Q_{g(\text{tot})}$ of the driven MOSFET, and the parasitic impedance present

TABLE IV
SUMMARY AND CLASSIFICATION OF SELECTED RESONATORS

Resonator	Manufacturing technique	Compensation	Coupling mechanism	Dimension	Resonant/operating frequency	Q factor
Fig. 2 [6]	Copper foil-wound	N.A.	Inductive coupling	Height = 192 mm Shield radius = 51.92 mm Diameter = 103.84mm	13.56 MHz	1150 (w/o shielding) 1050 (w/ shielding)
Fig. 3 [9]	Copper foil-wound	External circuits Parallel compensation	Inductive coupling	Copper ribbon width = 2.54 cm Copper ribbon thickness = 0.25 mm Coil diameter = 58 cm	2.50 MHz	300
Fig. 5 [12]	3D printing and electroplating	External circuits Parallel compensation	Inductive coupling	Diameter = 6 cm	6.78MHz	440
Fig. 6 [13]	3D printing, electroplating, and PCB	N.A.	Inductive coupling	Diameter = 38 mm Height = 12.5 mm	30 MHz	74
Fig. 7 [15]	Metal 3D printing	External circuits	Inductive coupling	Diameter = 10 cm	6.78 MHz	317 (Calculated using data of Table IV in [15])
Fig. 8 [18]	Double-layer PCB	Self-resonance Parallel compensation	Inductive coupling	Diameter = 200 mm	460 kHz	64
Fig. 9 [22][23]	Dual single-layer PCB	Self-resonance Series or parallel compensation	Inductive coupling	Diameter = 200 mm	2.961 MHz	198.574
Fig. 10 [25]	Dual single-layer PCB	Self-resonance Series compensation	Inductive and capacitive coupling	Diameter = 200 mm	11.64 MHz	210.6
Fig. 11 [30]	Multi-layer PCB	Self-resonance Parallel compensation	Inductive coupling	Diameter = 6.6 cm	7.09 MHz	1183
Fig. 12 [32]	Variable mechanical structure, wound with Litz wire	External circuits	Inductive coupling	Diameter = 40 cm (Variable, depending on folding ratio)	700 kHz	319 (Variable, depending on folding ratio)

in the gate-driver-to-G-S loop. For fast-switching devices such as GaN HEMTs, typical rise and fall times are below 10 ns. By contrast, propagation delay time—an inherent characteristic of the gate drive IC's internal architecture—is often significantly longer, especially for ICs with level-shifting capabilities, ranging from tens to hundreds of nanoseconds. Accurately understanding and synchronizing these timing parameters is essential for the successful operation of multi-MHz inverter circuits.

The gate drive circuits can be configured in several ways. Some commonly seen configurations are depicted in Fig. 17. The simplest configuration is a nonisolated low-side driver [see Fig. 17(a)], which is only suitable for single switch circuits such as class-E [51] and class- Φ_2 inverters [43]. A high-low side gate drive IC [see Fig. 17(b)] integrates two isolated drivers (some only have the top-side isolated) and can conveniently drive a half-bridge inverter.

A bootstrap circuit utilizes the bottom switch's ON time to charge the flying capacitor, harvesting the energy needed to turn on the high-side gate in the following interval. In WPT applications, a bootstrap circuit is sufficient to provide high-side source currents because the duty ratio of the top and bottom switches is normally 50%. The propagation delays of the two drivers sometimes do not match, with the high side experiencing a longer delay. This must be compensated with extra dead time, impacting the maximum switching frequency. Therefore,

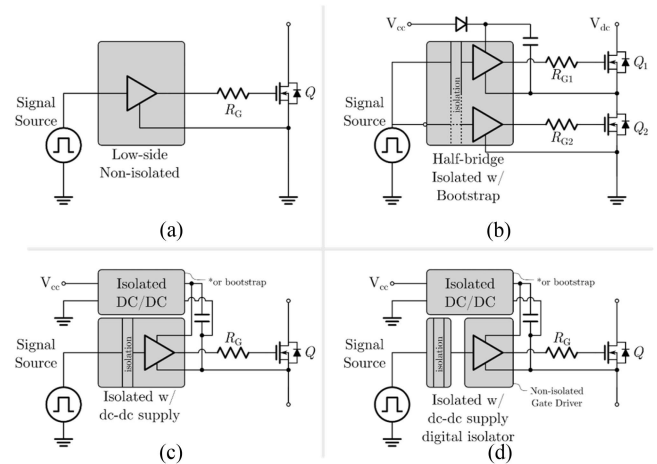


Fig. 17. Common gate drive configurations. (a) Nonisolated, lowside only. (b) Isolated, high-low-side, powered by a bootstrap circuit. (c) Isolated, using an isolated DC–DC converter. (d) Isolated, using an isolated DC–DC converter and a digital isolator.

homogeneous isolated gate drives [see Fig. 17(c) and (d)] are used in applications requiring precise synchronous switching. The driving voltage can be sourced from an isolated dc–dc converter to ensure good power quality. In terms of the driving voltages, isolated type drivers can be configured with either

TABLE V
SELECTED GATE DRIVE ICs AND THEIR MAIN CHARACTERISTICS

Vendor	Model	Type	Drive Voltage	Source/Sink Current	Isolated and CMTI	Package size	Propagation Delay	Max Frequency in Datasheet
AD	LTC7068	Half-bridge	6–14 V	2.6/3.6	150 V	MSOP10 3 x 3 mm	24 ns	N/A
Renesas	ISL71441M	Half-bridge	4.5–5.5 V	2/4(H), 4/8(L)	No	QFN 5 x 5 mm	29 ns	1.6 MHz
ST	STDRIIVE611	Half-bridge	6 V (internal LDO)	1/2.4	600V, 200 V/ns	QFN 4 x 5 mm	45 ns	2 MHz
TI	LMG1210	Half-bridge	5 V (internal LDO)	1.5/3	300 V/ns	WQFN19 3 x 4 mm	10 ns	50 MHz
TI	TPS7H60x5	Half-bridge	5 V (internal LDO)	1.3/2.5	No	HTSSOP56 14 x 6 mm	~40 ns	5 MHz
TI	UCC21231	Half-bridge	6.5–25 V	4/6	1600Vrms, 125 V/ns	WSON13 4 x 4 mm	33 ns	5 MHz
TI	UCC21225	Half-bridge	6.5–25 V	4/6	2500Vrms, 100 V/ns	LGA13 5 x 5 mm	19 ns	5 MHz
TI	UCC21521	Half-bridge	6.5–25 V	4/6	5700Vrms, 100 V/ns	SOIC16 10 x 7.5 mm	19 ns	5 MHz
TI	UCC2154x	Half-bridge	6–18 V	4/6	5700Vrms, 125 V/ns	SOIC14/16 10 x 7.5 mm	33 ns	5 MHz
Skyworks	Si8271	Isolated	4.2–30 V	1.8/4	2500Vrms, 200 V/ns	SOIC8 7.5 x 5.8 mm	60 ns	500 kHz
TI	UCC5304	Isolated	6–18 V	4/6	1060Vrms, 100 V/ns	SOIC8 7.5 x 5.8 mm	40 ns	2.36 MHz
Renesas	ISL71040M	Low-side	4.5 V (internal LDO)	1.5/2.8	No	DFN8 4 x 4 mm	40 ns	500 kHz
Rohm	BD2312G	Low-side	4.5–18 V	4/4	No	SSOP5 2.9 x 2.8 mm	15 ns	N/A
Rohm	BD2311NVX	Low-side	4.5–5.5 V	5.4/2.7	No	SSON6 2 x 2 mm	<4 ns	30 MHz
TI	UCC44273	Low-side	4.5–18 V	4/4	No	SOT23 2.9 x 1.6 mm	13 ns	700 kHz
TI	LMG1025	Low-side	5 V	7/5	No	QFN 2 x 2 mm	<3 ns	60 MHz
TI	LMG1020	Low-side	5 V	7/5	No	WCSP6 0.8 x 1.2 mm	2.5 ns	60 MHz
TI	UCC27624	Low-side	4.5–26 V	5/5	No	WSON8 3 x 3 mm	17 ns	1 MHz

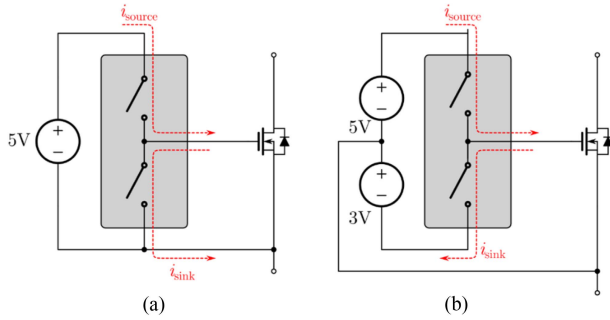


Fig. 18. Single- versus dual-voltage-rail drive configurations. (a) Single-voltage-rail gate drive. (b) Dual-voltage-rail gate drive.

single- or dual-voltage-rail [45] (see Fig. 18). The latter one offers faster turn-OFF speed at a cost of circuit complexity.

A survey on representative commercial gate drive ICs are listed in Table V. For isolated gate drives, the common mode transient immunity (CMTI) is the limit where the level-shifter can operate without propagating a wrong signal level when the secondary-side reference is rapidly rising or falling. The package size has impact on the total loop inductance—compact packages are preferred and expected to have less ringing and EMI issues. Some latest nonisolated gate drive ICs exhibit ultra-low propagation delays, such as Rohm BD2311NVX and TI LMG1020, as well as the smallest dimensions. When configuring them with discrete digital isolator [see Fig. 17(d)] such as TI ISO7720 which has a propagation delay of 11 ns, the combined total propagation delay is still less than using an isolated gate drive. In the last column, the maximum testing frequency mentioned in the datasheet is listed; though they do not necessarily assert the actual maximum frequency, they are good indicators of what frequency the manufacturers intend these devices to be operated at in the first place.

Among recent high-power multi-MHz implementations, the dc–dc converter + digital isolator + low-side gate driver approach [see Fig. 17(d)] is the most popular due to its consistent

low delay times. In [44], a 10.4-kW 6.78 MHz stacked inverter system is demonstrated, requiring precise synchronization of 12 GS66516T devices. In [46], the authors achieved accurate independent amplitude and phase control of two half-bridges in a 1-kW 13.56 MHz inverter, optimized for ZVS across a wide variable load range.

In [47], the authors proposed an ultra-fast gate driver using LVDS digital isolators, achieving a latency of less than 6.8 ns and rise/fall times below 0.5 ns. In the same paper, they also presented a current-fed gate driver implemented with an additional transformer, which achieved an even shorter propagation delay of 2.7 ns but relatively slower rise/fall times of 2.2 ns.

Apart from dedicated gate-driver ICs, logic-gate ICs have also been employed to drive GaN HEMTs, owing to their suitable voltage range, fast rise and fall times, and low propagation delays. However, their output current capability is limited—typically to only tens of milliamperes. One approach to mitigate this limitation is to parallel multiple logic-gate ICs. For instance, in [48], the authors paralleled six dual logic gates (SN74LVC2G series) to form a gate driver, enabling the operation of a current-mode Class-D inverter at 27.12 MHz. Similarly, in [49], parallel CMOS inverters were employed in a resonant gate-drive configuration, achieving operation at 20 MHz. Furthermore, these methods can be combined; in [50], logic gates were integrated with a transformer to establish a positive-feedback mechanism, enabling switching frequencies beyond 100 MHz.

B. Emerging MHz Gate Drive ICs With ZVS Controller

For 1–13.56 MHz operation, the power switches have to be soft-switched in order to avoid unacceptable switching losses. Some commercial gate drive ICs are integrated with ZVS PWM controllers, such as Renesas ISL6753, ON Semiconductor MC34067, and TI UCC28951. They help reduce the cost and complexity of the circuits and are preferred in product designs. They utilize external RC circuits for setting timing parameters achieving ZVS. Their datasheets highlight that the propagation

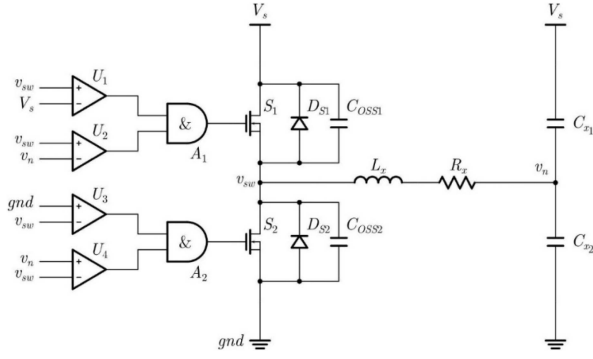
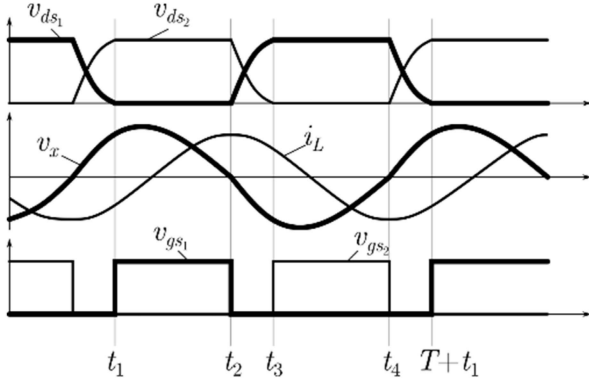


Fig. 19. Self-triggering nonisolated half-bridge ZVS driver circuit.

Fig. 20. Typical waveforms in the self-triggering ZVS circuit, where t_1 is the time of S_1 ZVS turn-ON; t_2 is where i_L is peaked due to LC resonance and S_1 is turned OFF; t_3 is the time of S_2 ZVS turn-ON; t_4 is the other peaking point of i_L .

delay needs to be taken into account when calculating the oscillator's timing parameters. If the propagation delay times for the high-side and low-side gate drives mismatch, longer deadtime will be needed which therefore limits the maximum operating frequency and effective maximum duty cycle. The maximum operating frequencies of these controllers are up to 2 MHz.

In [52], a nonisolated gate drive circuit utilizing differential comparators and generating the high-side PWM signals referenced to the switching node voltage is reported (see Fig. 19). Its typical waveforms are shown in Fig. 20. The inverter automatically drives the resonant load tank to the maximum amplitude and achieves ZVS by hardware feedback. Due to the elimination of the level-shifter/isolator, the propagation delay essentially comprises the comparator and the logic gate, which can be achieved below 10 ns—therefore, it will be suitable for driving future multi-MHz HP inverters.

IV. POWER INVERTERS FOR MEGA-HERTZ OPERATION

A. Types of Circuit Topologies for MHz WPT Operations

Two families of converter topologies are mostly used for operating at MHz range—the class-D and class-E inverters (see Fig. 21). The class-D family has the advantages of easy to design, convenient to control, and their breakdown voltage limit can be fully utilized. The disadvantage of class-D inverters are the difficulties in synchronizing their switch operations, which is

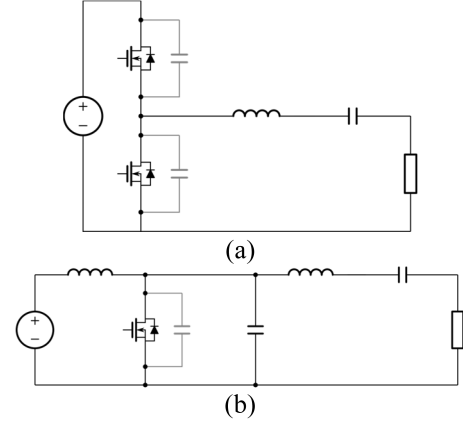


Fig. 21. (a) Class-D. (b) Class-E inverters.

limited by the rising and falling times, propagation delays, and minimum turn-ON time. Moreover, it is difficult for the class-D inverters to achieve ZVS operation at very high frequencies in the presence of load variation. In [53], a multistage discrete power amplifier structure with a lossless merging mechanism is proposed to achieve 5 W to 5 kW dynamics at 13.56 MHz. The class-E inverters have the benefits of single switch (grounded) operation, which is easier to run into tens of MHz even GHz range. The drawback is the extra voltage stress on the switch when it is turned OFF. This voltage stress is more than 2x the effective voltage delivered to the load, and the high stress also contributes to additional C_{oss} losses, which appears in GaN HEMTs [54], [55]. Both types of converters can be implemented in either single-ended or push-pull configurations. Push-pull converters offer the advantage of doubling the effective voltage applied to the load for the same supply rail, thereby facilitating higher power density [51].

B. Emerging Multimega-Hertz and Multikilo-Watt Power Inverters

For HP applications, class-D half-bridge and full-bridge power inverters are preferred. A comprehensive study on multimega-Hertz and multikilo-Watt full-bridge power inverters for WPT applications is reported in a recent publication [56]. It is based on the practical comparison of full-bridge power inverters based on the SiC MOSFETs and GaN power switches. With the same three-layer stacked inverter structures (see Fig. 22), tests were performed with SiC power inverter (at 4 MHz and 3.87 kW with an energy efficiency of 95.22%), and GaN power inverter (at 6.78 MHz and 2.28 kW with an energy efficiency of 97.22%).

HP inverters for mega-hertz operation are also reported in other publications. Several important design factors for arising from [56], [57], [58] are highlighted here.

1) *Selection of Power Switches:* For SiC MOSFETs, the proposed figure of merit (FOM) is the product of gate charge Q_g and internal gate resistance $R_{G(int)}$. That is,

$$\text{FOM} = Q_g R_{G(int)}. \quad (4)$$

A small $Q_g R_{G(int)}$ product implies fast switching speed, small dynamic conduction loss, and low driving power. The gate

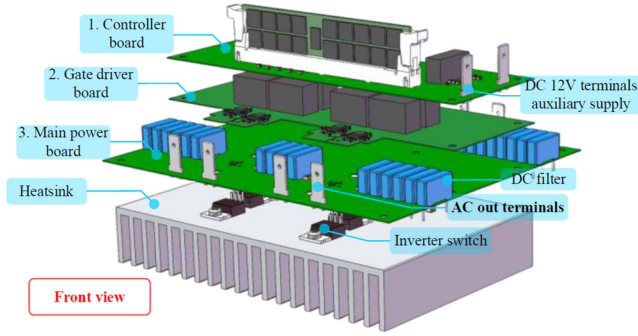


Fig. 22. Three-layer power inverter structure for multimega-Hertz and multikilo-Watt applications [56]. (IEEE Copyright).

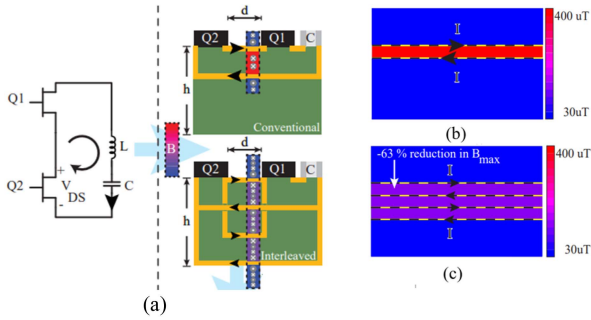


Fig. 23. (a) Use of interleaved multilayer PCB tracks to reduce loop inductance with simulated magnetic fields in (b) conventional design and (c) interleaved design [57]. (IEEE Copyright).

charge of a GaN switch is exceptionally low and is typically ten times less than that of a SiC power switch. In principle, this FOM applies to a GaN switch although its gate charge is typically one-tenth of that of a SiC switch.

2) *Auxiliary Power Consumption and Thermal Design of Gate Drive Circuits:* The control board normally consumes about 1 W while the majority of the auxiliary power is consumed by the gate drive circuit. Wang et al. [56] compare an SiC (C3M0060065K) inverter and a GaN (GS66506T) inverter from 1 to 6.78 MHz. The auxiliary power consumption of the SiC inverter varies from 7.3 W at 1 MHz to 22.0 W at 6.78 MHz, while that of the GaN inverter increases from 3.1 W at 1 MHz to 4.6 W at 6.78 MHz. These results give designers the typical order of magnitude of the auxiliary power for the thermal design of the gate drive circuits. In general, GaN inverters require less auxiliary power and are more suitable for HF operation. SiC inverters may require forced cooling for the gate drive when the frequency exceeds about 3 MHz.

3) *Power Inverter Layout to Reduce Loop Inductance:* For MHz operation, the loop inductance in the gate drive circuit is critical because a large loop inductance increases the switching power losses and the transients (adversely affecting the EM radiation). A method is proposed in [57] to reduce the parasitic inductance of the commutation loop in a half-bridge topology with surface-mount power devices. In Fig. 23(a), two switches Q1 and Q2 are connected in a totem pole manner across a dc voltage provided by a capacitor C. To minimize the loop inductance L, this method utilizes multiple PCB layers for enhanced

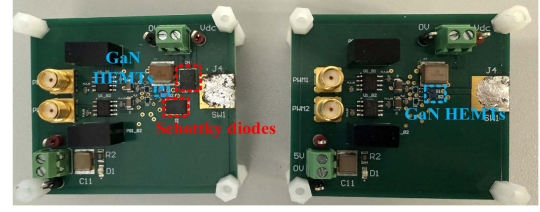


Fig. 24. Prototypes of totem-pole inverters with and without Schottky free-wheeling diodes [92]. (IEEE Copyright).

TABLE VI
EXPERIMENTAL PARAMETER SETTINGS

Parameters		Values
DC input voltage V_{dc}		60 V
DC bus capacitor C_{dc}		3 μ F
Gate-source voltage V_{gs}		5 V
1 MHz	Dead-time intervals	0.2 μ s
	Circuit parameters for the inductive load	4.29 Ω , 3.8 μ H, 9 nF
6.78 MHz	Dead-time intervals	0.0369 μ s
	Circuit parameters for the inductive load	4.31 Ω , 0.81 μ H, 0.82 nF
13.56 MHz	Dead-time intervals	0.026 μ s
	Circuit parameters the inductive load	4.27 Ω , 0.24 μ H, 0.8 nF

current distribution and magnetic cancellation, which results in low inductance designs with less sensitivity to the geometric parameters of the PCB design. Fig. 23(b) and (c) shows the comparison of the conventional PCB layout and the interleaved PCB layout reported in [57], with the resulting effect of reducing the magnetic field (and hence the loop inductance) by 63%.

4) *Inclusion of Freewheeling Diodes to GaN Inverters:* The arrival of GaN high-electron-mobility transistors (HEMTs) opens a door for MHz operations. The reverse-conducting property of such device enables it to work in four quadrants without using additional free-wheeling diodes, as recommended in manufacturers' data sheets [59], [60], [61]. Contrary to the datasheets of GaN HEMTs manufacturers that highlight the reverse-conducting characteristics of the devices, recent studies in [58] and [92] find that the performance of GaN HEMTs degrades significantly at MHz operations due to elevated reverse conduction losses, high-frequency oscillations, and thermal instability from self-heating. Two prototypes of totem-pole inverters with and without Schottky diodes, as shown in Fig. 24, were tested for comparison at 1, 6.78, and 13.56 MHz. The parameters and test conditions are listed in Table VI. The practical measurements are recorded in Table VII. It can be seen that the inverters with the free-wheeling diodes are consistently more efficient than their counterparts without the free-wheeling diodes at 1, 6.78, and 13.56 MHz.

5) *Energy Efficiency and Soft-Switching:* The comparative study of two multi-MHz and multi-kW power inverters based on SiC and GaN power switches (see Fig. 25) provides a useful reference in terms of their dc-dc efficiency at 6.78 MHz and up to about 2.5 kW, as shown in Fig. 26. Two important observations can be made. First, the GaN inverter is slightly more efficient than the SiC inverter. Second, hard switching occurs at the

TABLE VII
EFFICIENCY COMPARISON OF THE TWO CIRCUIT CONFIGURATIONS

Frequency	Configuration	Output current	Input power	Output power	Efficiency
1 MHz	Without diodes	2.53 A	29.02 W	27.45 W	94.60%
	With diodes	2.53 A	27.97 W	27.24 W	97.39%
6.78 MHz	Without diodes	2.35 A	26.77 W	24.10 W	90.02%
	With diodes	2.36A	24.85 W	24.17 W	97.28%
13.56 MHz	Without diodes	2.39 A	27.43 W	24.09 W	87.85%
	With diodes	2.37A	24.57 W	23.29 W	94.81%

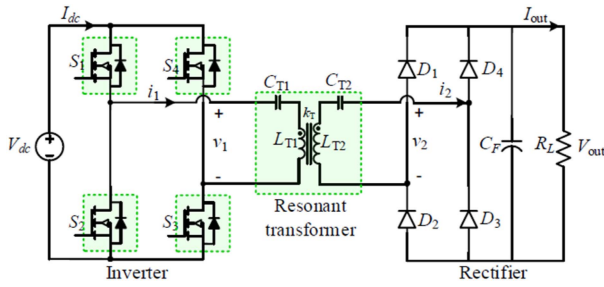


Fig. 25. Power circuits for SiC and GaN power inverter [56]. (IEEE Copyright).

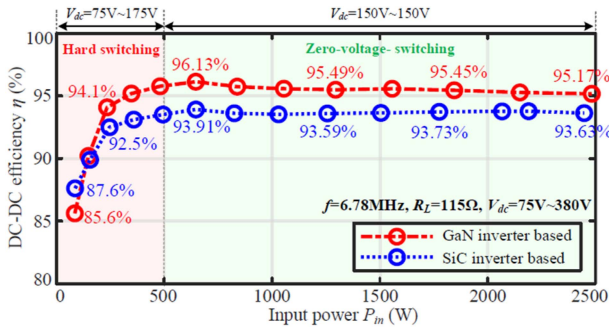


Fig. 26. Comparison of SiC and GaN inverters at 6.78 MHz [56]. (IEEE Copyright).

relative low power region when the load current is relatively small.

In order to ensure soft switching for the entire load range, including no-load condition, an auxiliary LC resonant tank can be added across the ac output of the inverter as explained in [62] and [63]. This extra resonant tank can be designed to draw the minimum current for soft switching of the power inverter, even when the current in the transmitter resonator of the WPT system is zero. Such a resonant tank can ensure soft switching of the power inverter without significantly compromising the energy efficiency.

6) *Accurate Frequency Generation on Microcontrollers:* When generating PWM signals from a microcontroller, the frequency accuracy is determined by the timer's reload register. Since the register can only take integer values, the exact target frequency is not always achievable. For instance, with a 100-MHz clock, it is impossible to generate exactly 6.78 MHz:

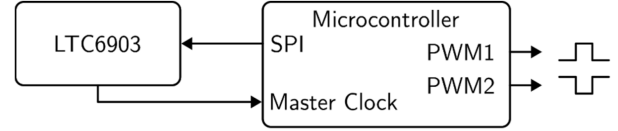


Fig. 27. Generating accurate frequency from a microcontroller.

a reload value of 15 yields 6.66 MHz, while 14 gives 7.14 MHz. This limitation can be addressed by using a programmable oscillator with a synchronous interface, such as the LTC6903 (see Fig. 27). The oscillator can be configured via SPI to provide a master clock close to the microcontroller's maximum frequency—for example, generating 23.73 MHz, applying a $\times 4$ multiplier to obtain 94.92 MHz, and then setting the reload register to 14 to achieve an accurate 6.78 MHz PWM. The tradeoff is that communications with external devices must either use a synchronous bus or operate from an independent clock source (e.g., a separate 48 MHz clock for USB).

V. EM SHIELDING MATERIALS AND METHODS

A. Existing EM Shielding Materials and Methods

While EM shields for WPT systems have become mature at lower frequency bands, the search remains for a suitable shield at the newly opened high-frequency WPT bands. Crucially, ferrite plates, which feature high permeability and high permittivity, also attain increasing loss with frequency [64]. This makes them increasingly absorptive, causing significant decrease in the power transfer efficiency (PTE) of WPT systems operating at 10 MHz and above. In the following, we review several techniques which have been proposed to perform shielding for WPT systems at this HF regime.

Firstly, an EM shield consisting of a thin ferrite layer backed by a metallic ground plane originally proposed in [65] was applied to a WPT system in [66], in which strong magnetic shielding exceeding—a magnetic field suppression of over 30 dB—was achieved at 6.78 MHz as the entire WPT system, including both the transmit and receive coils, was enclosed by the magnetic shield. Only a slight degradation in the PTE was observed. While a remarkable achievement, the system faces practicality issues, as the entire WPT system needs to be shielded, making the charging environment resemble a case into which the entire charging device must be enclosed. Further, the proliferation of loss for the ferrite material will lead to an increased PTE degradation for WPT bands at higher frequencies.

Shi et al. [67] and Radha et al. [68] propose the usage of artificial magnetic conductors (AMCs) as the WPT shield. The AMC uses printed metallic patterns, metallic vias, and/or chip components to generate LC resonances, effectively forming an EM dual to the conventional perfect conductor. While the ideal magnetic conductor can “short out” magnetic fields and prevent field penetration without reducing the PTE, practical implementations are limited by material and lumped component losses. Both works have reported strong shielding and an increased $|S_{21}|$ between the transmit and receive ports. However, the original systems (without the shield) achieved relatively low efficiency. For example, the $|S_{11}|$ in [64] is above 0.95,

meaning the power ratio between the transmitted and incident waves is below 10% without the shield. This raises question as to whether the improvement in S_{21} has resulted from better impedance matching, and consequently, whether similar PTE improvements can be applied to highly efficient WPT systems whose impedances are already well-matched without the shield.

Nanocrystalline materials have emerged as promising options for magnetic shielding in WPT systems. Compared with ferrites, they have advantages of high permeability, high saturation flux density, and mechanical strength [89]. They are effective in suppressing magnetic field from kHz to MHz. However, they have limitations of having higher conductivity than ferrite, leading to pronounced eddy current losses and heat generation under high-frequency and high-power operation. [90]. The high eddy current loss issue was tackled with a hybrid multipermeability nanocrystalline laminated ribbon magnetic structure in a 3-kW WPT system operating at 85 kHz [91]. The lamination structure is like that in a laminated core for traditional transformers. Such laminated structure offers good shielding effectiveness with reduced core losses but may be costly for mass production.

Finally, Rong et al. [69] and Lu et al. [70], [71] propose the use of mu-near-zero (MNZ) metamaterials as magnetic shields. Again, using circuit boards with carefully designed metallic patterns, LC resonances can be generated such that the board behaves as a material possessing near-zero permeability, setting up a magnetic boundary that prevents magnetic field penetration. In [69], a strong magnetic field suppression of -17.5 dB is demonstrated when such a shield is placed behind the transmit coil. However, the presence of the shield has led to a 24% decrease in the PTE. In [70] and [71], the authors show that the PTE degradation can be remedied by adding a mu-negative (MNG) metamaterial between the transmit and receive coils. However, the adding of the MNG layer complicates the WPT system and reduces the separation distance between the device and charger. Furthermore, as MNZ and MNG materials are strongly dispersive, the desirable material properties are attained over a narrow bandwidth. Thus, precision control is likely needed for fabrication and alignment, and the concept is likely limited to wider band WPT applications. Finally, as with the AMC structures introduced above, the researchers have used $|S_{21}|^2$ to represent the PTE, leaving open the possibility that some of the observed PTE improvements were obtained from improved impedance matching in the presence of the MNG layer.

In an earlier work, we have also proposed a frequency selective surface (FSS)-based magnetic shield for WPT systems at the GSM wireless bands surrounding 1 GHz [72]. The shield acts as a bandstop filter (BSF), preventing the GHz waves generated by the charging pad from causing RF interference and degrading the wireless communication sensitivity of the cellular phone. Moderate magnetic shielding (at the GHz frequency) is achieved with negligible performance degradation to the PTE (at a much lower frequency). A recent work has built on this approach and showcased the capability of the FSS to perform shielding for 13.56 MHz WPT systems [73]. In this work, two types of double-layered FSSs are shown to provide a moderate level of magnetic field shielding, without significantly affecting the quality factor of the resonator, which should bode well

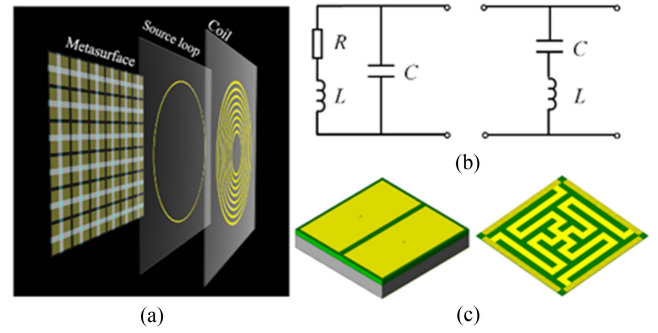


Fig. 28. (a) Conceptual diagram of the proposed metasurface EM shield. (b) Equivalent circuit diagrams of the artificial magnetic conductor topology and the bandstop filter topology. (c) Example unit cells for the artificial magnetic conductor (with Ferrite) and the bandstop filter prototypes. Metallic, dielectric and ferrite regions are denoted in yellow, green, and gray, respectively. [81].

for maintaining the PTE. However, the shielding level does not attain to that of the ferrite or metallic plate, and the PTE is not explicitly characterized. In addition, it remains unclear whether the quality factor for a high-Q resonator, such as the one proposed in Section II, will remain preserved when placed in close proximity to an FSS. Moving forward, the achievement of a stronger shielding will help provide the necessary protection for HP WPT, and the characterization of the shield's effect on the PTE will help determine the suitability of this shield for the MHz WPT system.

B. Metasurface as EM Shields

To address the aforementioned issues, novel EM metasurface shields for high-frequency WPT systems must be developed. Metasurfaces—2-D counterparts of metamaterials—are electromagnetically modified surfaces, featuring a combination of metallic patterns, dielectric structures, and lumped circuit components, which allow the surface to exhibit a user-defined response to an incident EM field [74], [75]. Metasurfaces have been demonstrated which redirect waves with near-perfect efficiency, focus and collimate EM waves, serve as polarization filters, form holographic displays, perform imaging, cloaking, and improve wireless communication channels [76], [77], [78], [79]. The multitude of applications showcase the adaptability of the metasurface and the varied impact it has achieved. However, most proposals to date utilize the metasurface to perform wavefront engineering in the far-field and the radiative near-field, where the incident wave is often characterized as a plane wave or a superposition of multiple plane waves. There is great potential in adapting the metasurface for shielding operations which happen in the reactive near-field of the WPT coils.

C. Design and Simulation Methodology

As an illustration [80], Fig. 28(a) shows a metasurface developed using filter theory and implemented using shunt reactive components. This metasurface is designed by first considering the microwave equivalent circuit. Different circuitries are compared, including an AMC topology and a BSF topology, whose circuit diagrams are shown in Fig. 28(b). After desirable circuits

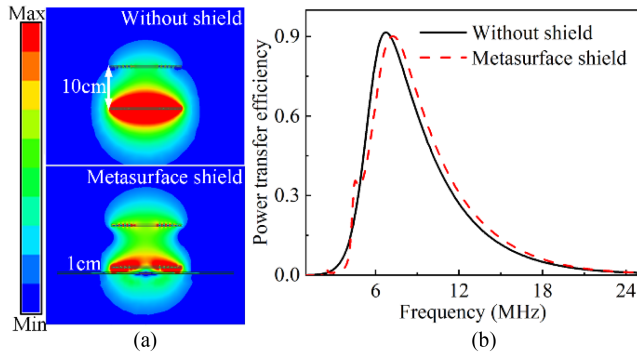


Fig. 29. (a) Simulated magnetic field profile for a metasurface designed at the 6.78 MHz WPT frequency. The top (bottom) panel shows the magnetic fields when the shield is absent (present). Metallic, dielectric and ferrite regions are denoted in yellow, green and gray respectively. (b) Corresponding power transfer efficiency as a function of frequency.

are obtained, the series and shunt inductors and capacitors are implemented using metallic patterns on the metasurface unit cell. Fig. 28(c) shows example metasurface unit cells for the AMC and BSF prototypes [80]. Finetuning may be required when the reactive elements are placed in close proximity to one another in the same unit cell. Salient properties of the unit cell, such as input impedances, are obtained through a periodic full-wave simulation featuring Floquet (periodic) wave ports. The geometrical parameters and/or component reactances can be swept and/or optimized through iterative algorithms and machine learning methods to arrive at the desired unit cell performance, which in this case entails strong reflection with suitable phase control at the WPT frequency. Upon successful unit cell design, a series of $N \times N$ unit cells (where N is an integer) is placed together to form a complete metasurface. The metasurface's shielding performance and its effect on the PTE can be evaluated in another full-wave simulation including the transmit and receive coils. Fig. 29(a) shows an example field magnetic field profile for a metasurface designed at the 6.78 MHz WPT frequency, compared alongside the field profile when the shield is absent. Fig. 29(b) shows the corresponding PTE as a function of frequency, when the coils are placed at a separation distance of 100 mm. The PTE changes from 91.6% to 90.5% after adding the metasurface EM shield. For a separation distance of 10 mm, the PTE changes from 97.5% to 97.4% with the use of metasurface. Clearly, magnetic field suppression is achieved without negatively affecting the PTE [81].

D. Comments on the Requirements of EM Shielding and Safety

The scope of discussion in this paper focuses on short-range WPT applications in the MHz range with the expectation that the coupling magnetic field is enclosed by EM shields to minimize human exposure to EM field. Unless the WPT systems are operated in an uncrewed environment, EM shielding is envisaged to be essential for MHz WPT systems because of uncertainty about human exposure to the EM field. While existing standards such as the IEC/IEEE 63184:2025 and ICNIRP guidelines set limits on the energy absorption by the human body and its thermal effects, research reports from quantum biologists and biologists

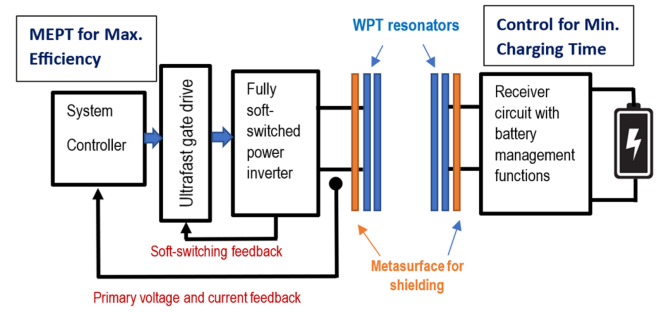


Fig. 30. Overall WPT system structure for high-frequency, high-power, and HE applications.

[82], [83], [84] have raised the concerns of nonthermal effects, such as cell proliferation under human exposure to EM field in the MHz range. More research is therefore needed to study the effects of high-frequency EM field on human cells.

VI. CONCLUSION

This article addresses several major hurdles to the high-frequency (1–13.56 MHz), high-power (kW), and HE ($\geq 95\%$) regime of WPT applications. Recent advances in

- 1) dual-single-layer PCB resonators with a high quality factor and suitable for mass production;
- 2) ultra-fast gate drives with low latency of 10 ns or less for fast SiC and GaN power switches;
- 3) multi-MHz and multi-kW power inverters with auxiliary soft-switching circuits; and
- 4) metasurfaces for EM shielding have provided the technologies required for entering this uncharted WPT territory in the near future.

The four aspects of advancements highlighted in this Visionary Paper enable the overall structure of a WPT system to be formed as shown in Fig. 30. With the paradigm shift of WPT from compatibility to optimal performance [2], maximum energy point tracking, and minimum charging time can also be incorporated to the primary-side control and secondary-side control, respectively.

As WPT systems with small airgap between the transmitter and receiver resonators can be adopted and the wireless power path can be effectively shielded in many emerging WPT applications (similar to the short transmission distance in the Qi standard for portable consumer electronics in the sub-kW and sub-MHz regime), the human safety concerns arising from human exposure to EM radiation in the emerging MHz and kW WPT applications should not be an issue. For WPT applications that require compact design such as smartwatches and medical implants, MHz WPT allows the use of small PCB resonators for fast charging or energy transfer. For relatively high-power WPT applications such as mobile robots, drones and e-bikes, MHz PCB resonators with high Q factors enable fast charging and HE. Together with ultra-fast gate drives and MHz half-bridge and full-bridge power inverters with soft-switching, WPT technologies for high-frequency, high-power and high-efficiency can become a reality.

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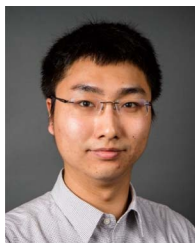


Shu-Yuen Ron Hui (Fellow, IEEE) received the B.Sc. (Eng.) (Hons.) in electrical and electronic engineering from the University of Birmingham, Birmingham, U.K., in 1984, and the D.I.C. and Ph.D. degree in electrical engineering from Imperial College London, London, U.K., in 1987.

He is currently a Chair Professor of Power Electronics with the City University of Hong Kong, and Imperial College London. Previously, he held academic positions with the University of Nottingham, and University of Sydney, and endowed professorship

with the University of Hong Kong. He has authored or coauthored more than 500 research papers including 330 refereed journal publications. His IEEE Xplore patent citations exceed 1280. More than 150 of his patents have been adopted by industry worldwide. His inventions on wireless charging platform technology underpin key dimensions of Qi, the world's first wireless power standard, with freedom of positioning and localized charging features for wireless charging of consumer electronics. He also developed the Photo-Electro-Thermal Theory for LED Systems and Electric Spring technology for smart grid. His research interests include power electronics, wireless power, sustainable lighting, and smart grid.

Dr. Hui was the recipient of the IEEE Rudolf Chope R&D Award and the IET Achievement Medal (The Crompton Medal) in 2010, IEEE William E. Newell Power Electronics Award in 2015 and the IET JJ Thomson Medal in 2024. He is a Fellow of the Australian Academy of Technology & Engineering, US National Academy of Inventors, and Royal Academy of Engineering, U.K.



Cheng Zhang (Member, IEEE) was born in China, in 1990. He received the B.Eng. degree (first class Hons.) in electronic and communication engineering from the City University of Hong Kong, Hong Kong, in 2012, and the Ph.D. degree in electronic and electrical engineering from The University of Hong Kong, Hong Kong, in 2016.

From 2016 to 2017, he was a Senior Research Assistant with the Department of Electrical and Electronic Engineering, The University of Hong Kong.

He was a Postdoctoral Research Associate with the

Research Laboratory of Electronics, Massachusetts Institute of Technology, Cambridge, MA, USA from 2017 to 2018. He is currently a Senior Lecturer in power electronics with the University of Manchester. His research interests include high-frequency ac–dc power conversions and designs and optimizations for wireless power transfer applications.



Kerui Li (Member, IEEE) received the B.Eng. degree in integrated design and integrated systems from the South China University of Technology, Guangzhou, China, in 2013, the M.Eng. degree in information and communication engineering from the Sun Yat-sen University, Guangzhou, China, in 2016, and the Ph.D. degree in electrical and electronic engineering from The University of Hong Kong, Hong Kong, in 2021.

Since 2025, he has been with City University of Hong Kong, Hong Kong, where he is currently an Assistant Professor with the Department of Electrical Engineering. Prior to that, he was a Research Fellow with Nanyang Technological University, Singapore, and a Research Assistant Professor with The Hong Kong Polytechnic University and The University of Hong Kong.

Dr. Li's professional services and research have been recognized with several prestigious awards, including the IEEE Transactions on Power Electronics Outstanding Reviewer Award (2025), two IEEE Transactions on Power Electronics Prize Paper Awards (second place for the year 2023 and first place for the year 2022), the IEEE Power Electronics Society Ph.D. Thesis Talk Award (2022), and the University of Hong Kong Power Engineering Prize (2020).



Alex M. H. Wong (Senior Member, IEEE) received the B.A.Sc. degree in engineering science (electrical option) and the M.A.Sc. and Ph.D. degrees in electrical and computer engineering from the University of Toronto, Toronto, ON, Canada, in 2006, 2009, and 2014, respectively.

He was a Postdoctoral Fellow with the University of Toronto. He is currently an Associate Professor with the Department of Electrical Engineering, City University of Hong Kong, Hong Kong, where he is also a member of the State Key Laboratory of

Terahertz and Millimeter Waves. He has advanced multiple projects in applied electromagnetics on next-generation RF, infrared, and optical metasurfaces, super-resolution imaging and radar systems. Particularly, he has made academic contributions to research on wave shaping using discrete Huygens' metasurfaces and far-field imaging based on super-oscillation waves. His current research interests include metasurfaces, metamaterials, super-resolution systems, bio-electromagnetics, and wireless power transfer.

Dr. Wong is a Member of IEEE Antennas and Propagation Society, Microwave Theory and Technology Society, and Photonics Society. He received accolades include an IEEE RWP King Award (for the best annual publication by a young author in IEEE TRANSACTIONS ON ANTENNAS AND PROPAGATION), the URSI Young Scientist Award, the Raj Mittra Grant, the IEEE Doctoral Research Awards from the AP and MTT societies, and the Canada Graduate Scholarship (doctoral level). He has served as the General Co-Chair for the 2025 International Workshop in Electromagnetics: Applications and Student Innovation Competition (iWEM 2025), the General Co-Chair for the 2022 IEEE HK AP-MTT Postgraduate Student Conference, and the TPC Vice-Chair for the 2020 Asia-Pacific Microwave Conference (APMC 2020). He has taken on various program committee, Session Chair, Technical Judge, and Reviewer duties for IEEE conferences and journal publications in the AP and MTT societies, as well as relevant venues in applied physics.



Siew Chong Tan (Fellow, IEEE) received the B.Eng. (Hons.) and M.Eng. degrees in electrical and computer engineering from the National University of Singapore, Singapore, in 2000 and 2002, respectively, and the Ph.D. degree in electronic and information engineering from the Hong Kong Polytechnic University, Hong Kong, in 2005.

From September to October 2009, he was a Visiting Scholar with Grainger Center for Electric Machinery and Electromechanics, University of Illinois at Urbana-Champaign, Champaign, and an Invited

Academic Visitor of Huazhong University of Science and Technology, Wuhan, China, in 2011. He is currently a Chair Professor with the Department of Electrical Engineering, City University of Hong Kong, Hong Kong. His research interests include the areas of power electronics and control, LED lightings, smart grids, and clean energy technologies.