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Analysis, Design & Fabrication of Low-Power Brain Tissue Oxygenation Pulse Oximetry.

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Abstract

Pulse oximetry is widely used for brain tissue oxygenation measurement, where optical fibres crossing the patient's skull through a cranial bolt carry pulsed light from LEDs to the brain tissue while transferring the light reflected from the brain tissue to a current measuring photodiode. Pulse oximetry light detectors have evolved from a standalone, relatively small photodiode to an array of photodiodes that are spatially distributed around the pulsed LEDs. While novel photodiode arrays can provide a larger photocurrent by collecting a larger number of photons compared with the stand-alone version, and thereby provide better contrast, their relatively large output capacitance can significantly degrade the noise performance and the speed of the analogue front-end. This Thesis is dedicated to the design and fabrication of a novel front-end that can be used in conjunction with a modern photodiode to provide high-resolution brain tissue oxygenation measurement.

A novel low-power, ultra low noise pulse oximetry front-end is designed, fabricated, and tested in this study. This front-end encompasses a low noise novel transimpedance amplifier, which can handle modern photodiode arrays with large output capacitance. The front end is designed in a fashion that its input-referred RMS noise power always remains much weaker than that of the photodiode shot noise for all photocurrent DC levels within a range of interest, which, in turn, provides the maximum possible signal-to-noise ratio. The front-end also utilises a novel thermometric calibrator capable of adjusting the LED light intensity with respect to the photocurrent DC level. Therefore, if the signal DC level drops below a certain level, the LED light is increased to enhance the signal's strength; for signals with a high DC level, the LED light is decreased to save power. Finally, the front-end uses a correlated dual

sampling technique to eliminate the dark current and offset errors.

In addition, this work analyses conventional pulse oximetry front-end topologies to specify the trade-offs and limitations posed by these architectures. All the theoretical and system level analyses are supported by transistor-level simulation data collected by means of Cadence Design Framework (CDF). These simulated results highlight the superiority of the proposed front-end design regarding power dissipation, silicon area usage, and noise performance in comparison with existing architectures.

Dedication

This Thesis is dedicated to my beloved family.

Acknowledgements

Firstly, I would like to express my sincere gratitude to my supervisor Prof. Drakakis for the continuous support of my PhD study and related research, for his patience, motivation, and immense knowledge. His guidance helped me in all the time of research and writing of this thesis.

I thank my fellow labmate, Mr. Graham Peyton for his valuable support, contribution and collaboration in shaping up this thesis in its present form. I do not imagine any better collaboration than what I had with him.

Last but not least, I would like to thank my parents and my brother for their unconditional love and support throughout my life. I am the luckiest man to have you.

Declaration of Originality

I declare that this project was entirely my own original work and that any additional sources of information have been duly cited.

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Chapter 1

Introduction

Monitoring of cerebral oxygenation is a crucial clinical procedure applied to patients suffering from traumatic brain injury (TBI). Secondary damage, associated with cerebral hypoxia and ischemia [10], occurs in most of these patients as a consequence of cerebral perfusion pressure drop (CPP), caused by either intracranial hypertension or arterial hypotension. CCP can be calculated using Equation 1.1, where ABP and ICP stand for arterial blood pressure and intracranial pressure, respectively [11].

$$CPP = APB - ICP \tag{1.1}$$

Such a drop in the level of perfusion can cause cerebral blood flow reduction, which limits the oxygen delivery to the injured brain [12, 13]. Thus, by mon-

itoring the cerebral oxygenation along with intracranial pressure (ICP) in a real-time fashion, secondary damage might be prevented [14]. Clinical studies have illustrated that oxygen monitoring in patients with severe TBI leads to significant mortality reduction [15–18].

A number of measurement techniques have been proposed in state-of-the-art studies on brain tissue oxygenation monitoring including near-infrared spectroscopy (NIRS) [19–23], invasive oxygen partial pressure ($PbtO_2$) monitoring using LICOX catheter oxygen probe [24–26] and pulse oximetry (PO) [2, 3, 27]. These techniques require massive bedside stand-alone signal recording devices that are only suitable for the clinical environment. As mentioned earlier, since the lack of oxygenation can profoundly damage the brain, it is crucial to measure the cerebral oxygen level immediately after the brain injury, preferably at the scene of the injury.

The aim of this study is to develop a battery-operated portable device capable of monitoring the brain tissue oxygenation in a real-time fashion. Therefore, it is important to assess the feasibility of the implementation of these clinically approved techniques in the form of a portable device.

A wireless battery-operated brain tissue oxygenation monitoring device is desirable for use in the Intensive Care Unit (ICU). The absence of any wire connected to the patient's bed from the outside world would allow medical staff to move freely around the patient's bed. Ideally, one battery should be enough to support the monitoring device throughout the time that the TBI patient is in the ICU. This would ensure reliable continuous-in-time monitor-

ing of the brain tissue oxygenation during the treatment. The design of an appropriate low-power sensor front-end is obviously essential to achieve such extended battery life.

Measurement of the partial pressure of oxygen in brain tissue ($PbtO_2$) is one of the most common techniques used to monitor the oxygenation of both human and animal brains [14, 28, 29]. More than 200 medical studies are listed in [28] where $PbtO_2$ was measured either separately or along with other cerebral measurements. Most of these studies are clinical, where $PbtO_2$ is monitored for various medical applications such as brain tumour surgery and cardiopulmonary resuscitation. $PbtO_2$ measurement can be conducted by introducing an invasive Clark-type electrochemical sensor, such as LICOX, into the Perfused brain tissue; the sensor can be inserted via a cranial bolt screwed into the skull [2, 26]. This sensor generates an electrical current proportional to the amount of oxygen diffused into its electrolyte chamber from the adjacent tissue, namely 17 to 27 mm below the dura [25]. This technique for measuring local oxygenation requires up to two hours to be settled before providing a stable measurement [2]. $PbtO_2$ measurement is also regarded as one of the most reliable technique to monitor focal cerebral oxygenation in order to prevent episodes of desatuartion [29].

$PbtO_2$-based therapy is commonly used in patients suffering from TBI [30, 31]. Nangunoori et al. have conducted a systematic literature review of a number of clinical studies published between 1993 and 2010 that employed $PbtO_2$-based therapy for TBI patients. Interestingly, more than 60 % of the patients who received this therapy had favorable outcomes [32].

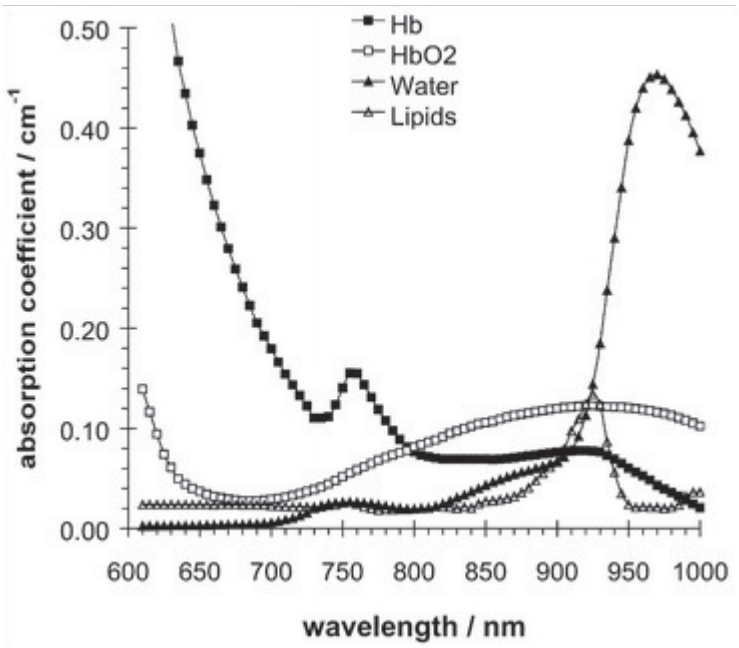


Figure 1.1: Main tissue constituents absorbing in the 600-1000 nm spectral range[1].

Non-invasive optical techniques have been employed to measure tissue oxygenation since 1980. Near infrared spectroscopy is one such method. It assesses the tissue oxygen level by continuously monitoring the regional hemoglobin saturation, using the difference between the absorption spectra of oxygenated (HbO_2) and deoxygenated hemoglobin (Hb) to achieve this[33–35] (See Figure 1.1).

Near infrared radiation of wavelength 700-1000nm generated by light-emitting diodes (LED) placed on the patient's skull is used in NIRS. As biological tissues are relatively transparent in this frequency range, NIRS optical detectors can be placed on the skull and measure radiation that has penetrated as deep as 8cm [4].

The NIRS device signal processing unit employs the Beer-Lambert law, formulated in Equation 1.2, to calculate the concentration of the HbO_2 in the biological tissue.

$$A = log(\frac{I}{I_0}) = \alpha \times c \times d \tag{1.2}$$

where I and I_0 denote the intensity of the incident and transmitted light, respectively; A is the attenuation coefficient; α is the specific extinction coefficient of the compound ($mmol^{-}1cm^{-}1$); c, the concentration of the absorbing compound; and d, the optical path-length or distance travelled by the light beam in tissue (cm) [4].

In practice, there are many other IR-absorbing compounds also present within biological tissue, including water and lipid (See Figure 1.1). Therefore, Equation 1.2 can be re-written as:

$$A = (\alpha_1 \times c_1 + \alpha_2 \times c_2 + \alpha_3 \times c_3 + ...) \times d \tag{1.3}$$

The concentration of the HbO_2 varies with cardiac pulsation whilst that of the other compounds remains relatively constant, the tissue oxygenation, therefore, can be monitored by monitoring the changes in the concentration of the HbO_2 using Equation 1.4.

$$\Delta(A_1 - A_2) = \alpha \times d \times \Delta(C_1 - C_2) \tag{1.4}$$

Equation 1.4 can also be used to monitor the change in the concentration of more than one light absorbing compound. This can be realized by using more than one wavelength of the light. This technique is employed in modern pulse oximetry systems where two wavelengths of lights are used to record the change in concentration of the Hb and HbO_2, simultaneously.

Absorption due to intervening structures, such as bone or skin, can be bypassed by delivering the light directly onto the cerebral tissue using fibre optics [2, 36]. The optical fibres can be placed in the cranial bolt that is already situated in the TBI patient's skull to measure the ICP, which minimises the invasiveness of the technique. This technique is also known as brain tissue pulse oximetry.

Figure 1.2b shows, in cross-section, a pair of such optical fibres passing through the skull via a cranial bolt. The mechanical device, shown in Figure 1.2a., is proposed by a study [2] to hold the fibres firmly while keeping them separate.

As illustrated in Figure 1.2a., two optical fibres are used for the brain tissue pulse oximetry. One, labelled as source fibre, shines light into the cerebral cortex, and the other returns the reflected light to the photodiode. The source and detector fibres are connected to an LED and a photodiode, respectively, on the other end to enable brain tissue oxygen measurement using a reflectance pulse oximetry technique [37].

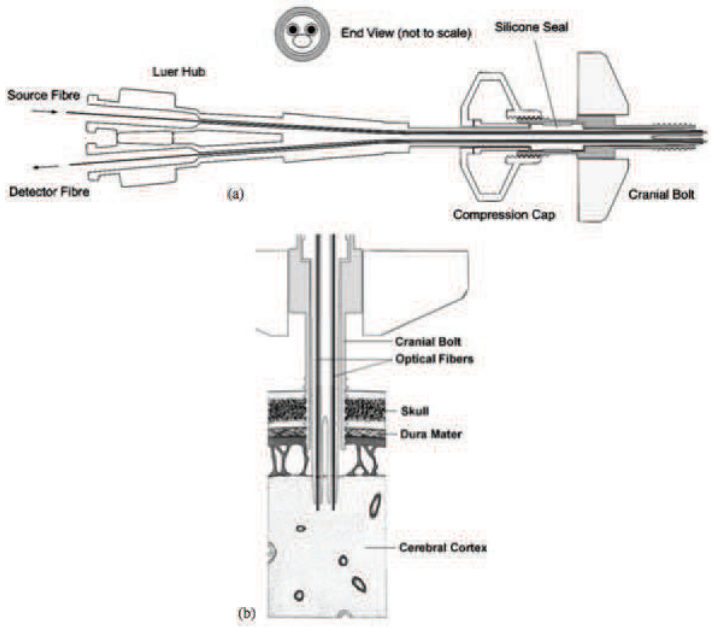


Figure 1.2: (a) a mechanical device to hold the fibres into the cranial bolt (b) the cross-sectional view of a cranial bolt inserted into the skull, which provides a pathway for the embedded Fibre-optics to reach the cerebral cortex [2, 3].

1.1 Pulse oximetry principles and prior art

Pulse oximeters (PO) measure the level of oxygen in an organic fluid by employing the Beer-Lambert model, as formulated in Equations 1.2-1.4. In conventional PO devices, two wavelengths of radiation are used: 660nm ("red") and 950nm ("infrared"). As shown in Fig 1.3, the absorption coefficients of Hb and HbO_2 are significantly different at these wavelengths, which means their relative concentrations can be simultaneously measured with a high degree of selectivity. When the concentration of Hb is larger than that of HbO_2, the "red" absorption will be higher than the "IR". Conversely, the IR absorption

will be greater at high oxygen saturation levels [38].

As explained later in this section, the PO device post-processing unit translates this recorded information to the peripheral oxygen saturation level (SpO_2) using a calibration curve generated empirically by measuring the SpO_2 of healthy individuals [38].

The red and infrared light is delivered to the tissue under examination sequentially and the reflected light collected by one or more photodiodes, which generate a current proportional to the its intensity, also known as photoplethysmography (PPG).

The recorded PPG photocurrent is comprised of a non-pulsatile (DC) and a pulsatile (AC) component [see Figure 1.4] [5, 39]. The light reflected from venous blood, non-pulsation arterial blood and other intermediate tissues generate the DC component of the PPG signal while the pulsating arterial blood generates the AC component.

The transmitted light amplitude profile during a PO measurement is depicted in Figure 1.4. The amplitude reaches its maximum, marked as I_{max} in Figure 1.4, immediately after the Systole phase in the cardiac cycle. At this phase, the heart ventricles contract and oxygenated blood is pumped through arteries, which increases the level of HbO_2 in the blood. This leads to minimum absorption of the light in the perfused tissue. As the cycle proceeds to the diastole phase, the level of HbO_2 diminishes continuously while the Hb levels increases, which leads to maximum absorption of the light within the tissue and a minimum transmitted light amplitude. The patient's heartbeat can thus

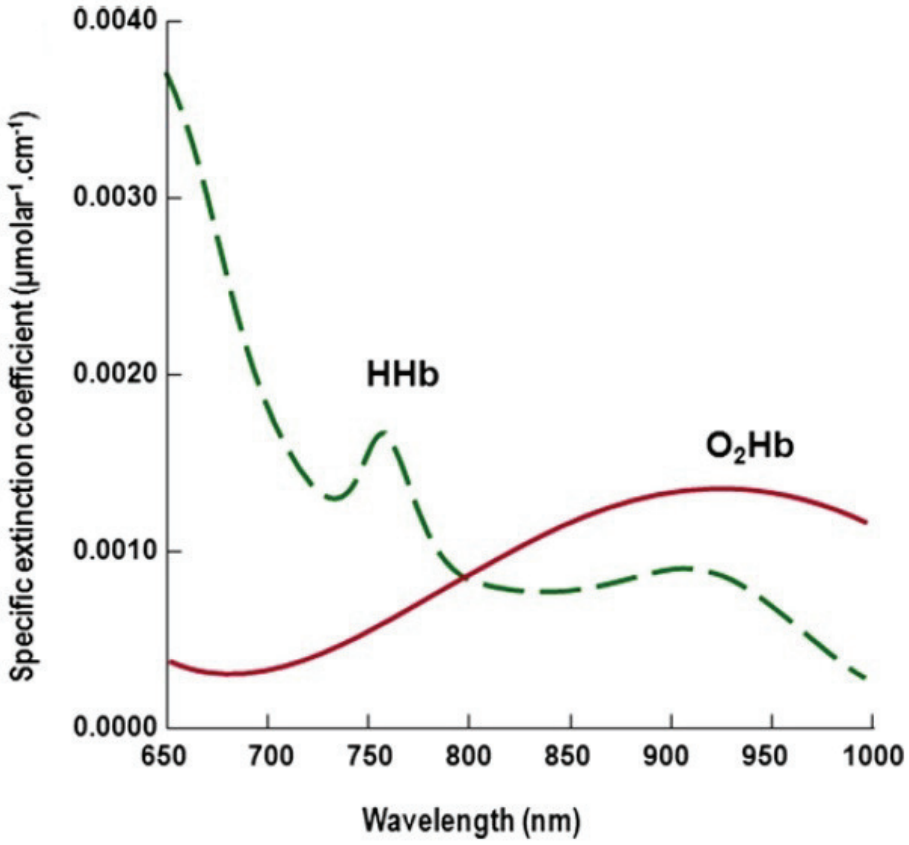


Figure 1.3: Light absorption spectra of Hb versus HbO_2. At 800nm, known as isobestic point, the absorption spectra of Hb and HbO_2 is equivalent. This wavelength, therefore, can be employed to calculate the hemoglobin concentration independent of oxygen saturation. Source [4].

be monitored by tracking the PPG signal.

Λ can be defined as the ratio of the peak-to-peak amplitude of the AC component of the PPG signals acquired using red and infrared light (See Equation 1.5). The peripheral capillary oxygen saturation (S_pO_2), which is a measure of oxygen level in the perfused tissue, can then be estimated by an empirical

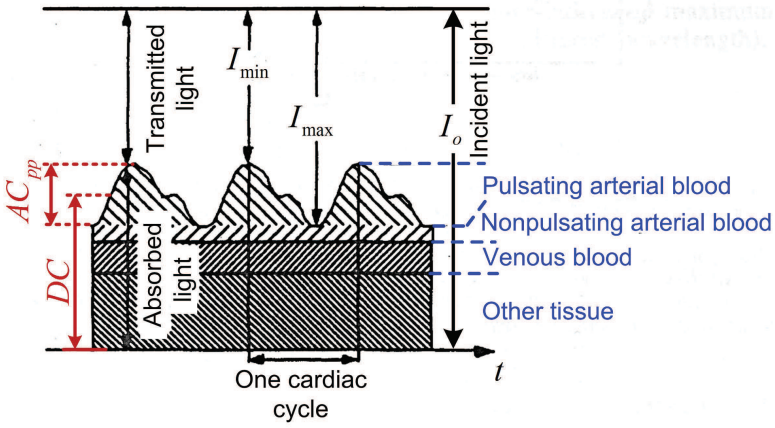


Figure 1.4: Transmitted light amplitude profile during PO measurement. Source [5].

formula (see Equation 1.6) [3, 7].

$$\Lambda = \frac{\frac{AC_{pp}}{DC}|\lambda_1}{\frac{AC_{pp}}{DC}|\lambda_2} \tag{1.5}$$

$$S_pO_2 = 110 - 25 \times \Lambda \tag{1.6}$$

The pulse oximetry technique can be used to measure oxygenation directly, without using fibre optics, at various body locations such as: fingertip ([7, 40]), esophagus [41], wrist [42] and with fibre optics at the cerebral cortex [2] and retina [43].

1.2 Pulse oximetry sensor design

The distance between LEDs and the photodiode (PD) determines the PPG signal AC/DC ratio, also known as the signal contrast. 3 to 5 mm, LED-PD separation is sufficient to have a relatively strong AC component [3, 42]. Such distance between LEDs and the photodiode(s) leads to the collection of the photons that have travelled deeper in the tissue. Collection of these photons leads to the generation of a large AC component, which eventually increases the resolution of the measurement.

A modern approach toward recording a high-resolution PPG signal is to utilise a number of photodiodes placed radially around LEDs (see Figure 1.5). The positive effects of such a distribution of the photodiodes on the contrast of the PPG signal are discussed in other studies [6, 42]. It has been reported that the amplitude of the PPG AC component is determined by the size and relative position of photodiodes with respect to the LEDs. A much stronger PPG signal was recorded by utilising 12 photodiodes with a 12-15 mm^2 active area in [6] than was obtained with the conventional opto-pairs with a single photodiode.

The circular placement of photodiodes around LEDs used in [6], called an "outer-ring configuration", is depicted in Figure 1.5. Furthermore, it has been reported that the location on the patient's body where the measurement is conducted also affects the strength of the acquired signal [6].

The latest generation of opto-probes utilises a "ring-shaped" photodiode sur-

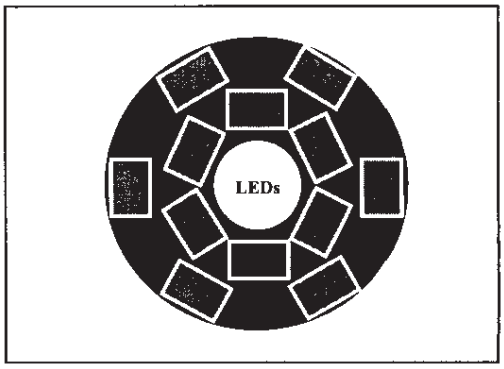


Figure 1.5: The outer-ring configuration, where the photo-diodes, depicted with black rectangles, are located radially around the LEDs located in the centre[6].

rounding the LEDs [44, 45]. Similarly to the probe shown in Figure 1.5, the effective area of photodiodes has been increased to maximise the amplitude of the PPG signal by collecting a larger number of photons. However, instead of utilising a number of discrete photodiodes radially distributed around LEDs, an annular photodiode with an effective area as large as 18 mm^2 is microfabricated on the silicon substrate. The ring-shaped PD collects a large number of photons by increasing the photodiode's photosensitive area. However, such large photodiodes exhibit a high output capacitance (e.g. 34.5 nF in [44]), which severely degrades the performance of the analog front-end processing the photocurrent generated by the photodiode.

The settling time of the front-end is determined by the size of the PD output capacitance. Therefore, the increase in the settling time of the analog front-end caused by using a PD with large active area must be either compensated by

increasing the LEDs duty cycle or designing a front-end with wider bandwidth. The former increases the power consumption of the whole system aggressively since almost 90 % of the overall power is consumed by the LEDs, as reported in [7, 40]. The latter, on the other hand, leads to front-end stability degradation.

The study which proposed the ring-shaped photodiode [44] acknowledged this stability degradation, but clearly a larger photosensitive area for acquiring the PPG signal is very desirable. Our study, therefore, aims to design a low-power stable PO front-end capable of supporting such large photodiode assemblies.

1.3 Pulse Oximetry Front-end Design

The settling time of the resistive TIA, the architecture of choice in many pulse oximetry frontends, is calculated in chapter 3. The mathematical analysis manifested in this chapter suggests that the TIA settling time is determined by the size of the feedback resistor, the op-amp bandwidth and size of the PD output capacitance.The settling time requirement of modern PO TIAs are relatively restricted because the LEDs are switched on only for a short time period in each cycle (e.g. a few hundreds micro seconds) to save power. This leads to the generation of a photodiode current with a relatively small duty-cycle (see chapter2). The TIA settling time, therefore, must be small enough in order to read-in such a signal.

Bandwidth extension techniques with on-chip monolithic inductors and transformers are proposed in [46, 47]. Although these techniques are practical in

the GHz range in which small inductors are sufficient to amend the closed-loop bandwidth of the system, the PO front-ends cannot use these techniques simply because they are operating at low frequencies whereby the inductors available on-chip are short-circuited.

Resistive TIA is also used widely in the PO front-ends used both in academic studies [40, 42, 48, 49] and commercial PO chips such as the Texas Instruments integrated analog front-end for pulse oximeters (AFE4490). We dedicate Chapter 3 of this thesis to a comprehensive analysis of the performance of the resistive TIAs.

Tavakoli et al. have proposed an alternative PO front-end architecture in which the TIA core op-amp is a distributed amplifier comprised of three cascaded, first-order gain stages with similar DC gain and bandwidth as depicted in Figure 1.6 [7].

The feedback resistor is also replaced by a CMOS transistor biased in the weak-inversion Which provides a logarithmic trans-impedance gain. This, interestingly leads to:

$$V_{out} = \frac{U_T}{k} \times \frac{i_{ac,in}}{I_{DC,in}} = \frac{i_{ac,in}}{gm_{Q1}} \tag{1.7}$$

By considering Equations 1.7 and 1.5 together, it can be seen that the output of this TIA generates the ratio required for the calculation of Λ.

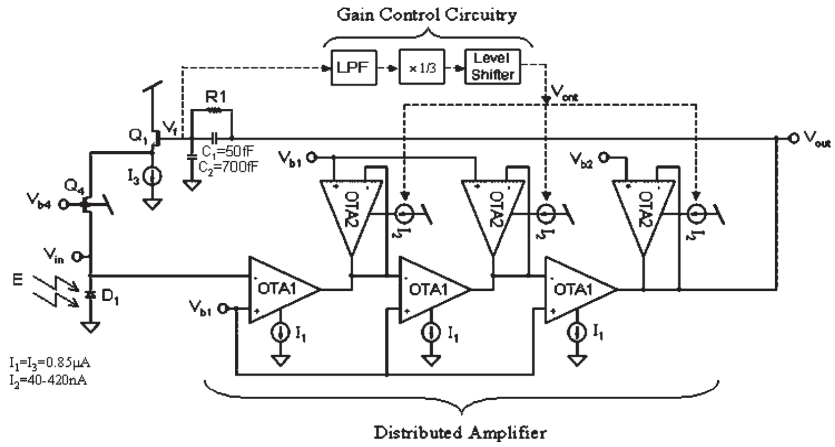


Figure 1.6: The distributed amplifier architecture proposed by Tavakoli et al. as an alternative to the conventional resistive TIA. Source [7].

The bandwidth of the TIA proposed in [7] has increased by applying negative feedback. Mathematical analysis of the feedback loop depicted in Figure 1.6 confirms that the dominant pole of the closed-loop TIA transfer function moves to $\omega_p = \frac{1+A}{C_D/gm_1}$ where C_D is the photodiode output capacitance, gm_1 is the feedback CMOS transconductance, and A is the total voltage gain of the distributed amplifier. As expected, the negative feedback trades the gain with the bandwidth.

There are also three non-dominant poles in the closed-loop transfer function of the Tavakoli's TIA, which corresponds to each stage of the distributed amplifier. Root locus analysis can confirm that as the dominant pole moves toward higher frequencies, one of the non-dominant poles moves toward lower frequencies. Therefore the TIA closed-loop transfer function becomes similar to

that of a second-order system. A second-order system step response exhibits "ringing" when its poles frequencies become too close, which can increase the settling time of the system. In extreme cases, the TIA dominant and non-dominant pole can become two conjugate poles and move toward the the $j\omega$ axis. Under this circumstance, the TIA might exhibit oscillatory behaviour, which impairs its functionality.

The oscillatory behaviour can occur in Tavakoli's PO front-end because of the dominant pole frequency dependency to gm_1, defined by the DC level of the PPG current generated by the photodiode. The design has tried to mitigate this problem by adding a gain control scheme, which monitors the DC level of the PPG signal and adjusts the distributed amplifier gain accordingly. However, since the PPG current is square-wave modulated wave, a low-pass filter with a low cut-off in frequency is required to extract the PPG DC component (See Figure 1.6). Such filter is slow in nature and cannot react swiftly to sudden changes in the PPG DC level caused by motion artefacts.

Finally, Tavakoli's PO front-end has employed a CMOS as its feedback element, which corrupts the PPG current signal with its thermal and flicker noise. This can further degrade the noise performance of the PO front-end in comparison with that of the resistive TIA, where the resistor flicker noise is negligible.

A switched integrator transimpedance amplifier cab also be used as the PO TIA [8]. Figure 1.7 depicts the front-end architecture proposed in [8]. The switched integrator output voltage can be calculated as:

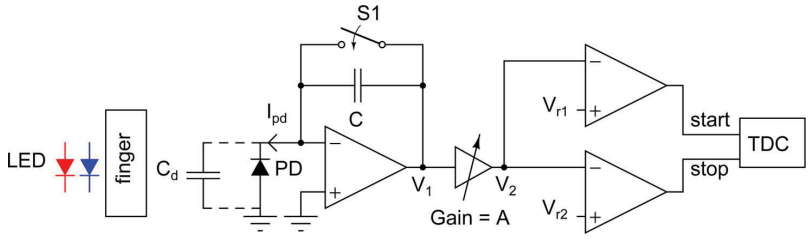


Figure 1.7: The PO front-end proposed in [8], where a switch integrator amplifier is employed as the TIA. Source [8].

$$V_{out}(t) = \frac{1}{C_f}\int_{tr}^{t} I_{pd}dt + V_{ref} \tag{1.8}$$

This architecture suffers from a severe disadvantage imposed by microfabrication principles, the absence of on-chip large capacitors. The maximum capacitor allowed on-chip is usually 100 pF. Let's assume that the photodiode current is square-wave modulated current with 100 Hz frequency, 3% duty-cycle and Iin_{max}=500 nA. Even if a 100 pF capacitor is used in the feedback, the output DC level will settle at 1.5 volts above the V_{ref} which can saturate the output stage of the op-am.

The other challenge in designing PO front-ends using switch integrators is the stability of the system during the reset phase. This phase occurs periodically before the integration to deplete the charge of the feedback capacitor. At this phase, the reset switch which is placed in parallel with the feedback capacitor,

short the two terminals of the feedback capacitor. The op-amp, therefore, operates with a unity feedback while its output is loaded with photodiode output capacitor. Therefore, it can be very challenging to keep the loop stable during the reset phase, particularly when photodiodes with large active areas are used.

The aim of this study is to design and develop an stable analog low-power PO front-end capable of recording PPG signals from an array of photodiode with large photo-sensitive area, while adaptively controlling the light intensity of LEDs to optimise their power consumption. In chapter two we characterise PO front-end as a system for which and analog front-end must be designed. Chapter three, analyses the nonidealities of the conventional resistive transimpedance amplifiers. The novel analog front-end proposed for this study is analysed in chapter four and five. The evaluation results of the analog frontend designed for this work are presented in chapter six. This setup uses the PO chip microfabricated for this study to record PPG signals. Finally, the thesis summary and scope for future work can be found in chapter seven.

1.4 Contributions

The original contributions of this work include:

1. In-depth theoretical analysis of the pulse oximetry opto-pair physical principles and non-idealities.

2. Mathematical modelling, circuit analysis, and simulation of the resistive transimpedance amplifier along with its trade-offs.

3. Proposition of a novel trans-impedance amplifier whose overall performance is significantly better than that of the state-of-the-art published PO TIAs.

4. Proposition of a novel LED light calibrator, which monitors the PPG DC level continuously and adjust the LED light intensity in a way that signal level always remains whithin a certain boundary.

5. Design and fabrication of a novel low-power current read-out front-end (ASIC) capable of operating with photodiode arrays and handling photocurrent with wide dynamic range.

Chapter 2

Working principles of Pulse Oximetry systems

The evolution of pulse oximetry sensors from single photodiodes to ring-shaped photodiodes has been explained in Chapter 1, together with the advantages of the more modern devices, such as their larger photocurrent, improved contrast, and higher signal-to-shot-noise ratio. The objective of this chapter is to determine the specifications for an optimal current read-out analog front-end (AFE) compatible with such state-of-the-art sensors.

A typical pulse oximetry system is depicted in Figure 2.1. The AFE interfaces with the SpO_2 sensor, an opto-pair comprised of an optical detector (either a single photodiode or an array) and two LEDs, with an analog-to-digital (A/D) converter. The main function of the AFE is to collect the relatively small square-wave modulated wide-band current generated by the PO pho-

todiode and convert this into an amplified, continuous-in-time narrow-band voltage, which can be delivered to an A/D converter. In addition, the AFE provides the required reverse bias voltage for the photoconductive operation of the photodiodes and drives the LEDs. Some modern AFEs are also capable of adaptively maintaining the integrity of the measured signal by controlling the LEDs light intensity or duration [8, 40]. The AFE, therefore, should be designed as part of the entire PO system encompassing photodiodes, LEDs, controllers, and the A/D converter, because its specification will inevitably involve performance trade-offs imposed by these other components. Thus, the first step toward developing an optimal AFE is to characterise the PO system as whole.

This chapter initially discusses the optical behaviour, non-idealities and biasing requirements of modern PO optical detectors. The frequency range and the temporal behaviour of the PPG signal generated by such detectors are mathematically analysed to determine the characteristics (e.g. bandwidth and contrast) of the signal that the AFE must be capable of handling. The chapter then studies the effects of the LEDs on the overall power consumption and quality of oxygen measurement. LED drivers which can control the luminescence intensity and duration are also examined to assess any adverse effects on LED performance. Finally, the essential features required for low-power, high-performance A/D conversion is presented. Having studied all the components operating in conjunction with the AFE, as depicted in Figure 2.1, chapter 3, 4 and 5 are dedicated to develop an analog system, which can perform as the sensor front-end for the PO systems.

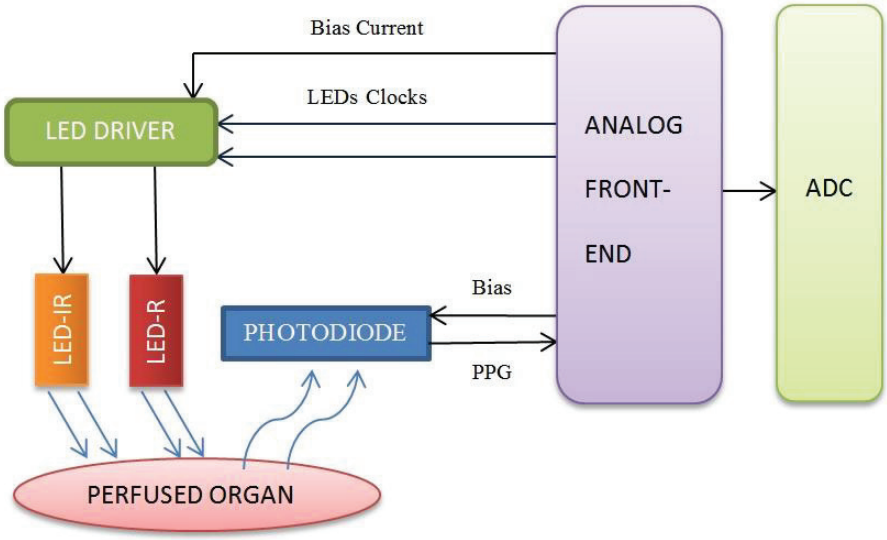


Figure 2.1: System level pulse oximetry block diagram. The analog frontend (AFE) enables the measurement by providing time-interleaved clock signals that power up one LED at a time, and a bias current the amplitude of which determines the LED luminescence intensity. It also provides the reverse bias to enable the photodiode to operate in photoconductive mode. The generated photocurrent is linearly proportional to the intensity of the light reflected from the perfused organ, and after processing it is delivered to an A/D converter.

2.1 The physics of the photoconductive planar p-n photo-diodes

Silicon p-n photodiodes are widely used as photoreceptors in PO systems. Particularly when operated in photoconductive mode, where it can provide a relatively linear relationship between incident light intensity and photocurrent.

Any reverse-biased p-n junction is in theory photoconductive and can be used as an optical detector. There are two other modes of p-n photodiode operation: photovoltaic and avalanche. These are generally used to detect light intensities that are much smaller than a typical PPG signal, which is why the photoconductive mode is assumed in this study.

The physical principles governing the conversion of light to electric current in photoconductive devices are explained thoroughly in numerous standard works. In brief, a planar p-n diode is formed when a p-type semiconductor is deposited within an n-well. A small potential difference known as the built-in voltage appears across the p-n junction owing to the diffusion of electrons from the n-region to the p-region, which leads to the electron hole recombination on the P side of the junction. This process creates negative ions, the atoms that accepted an electron, of the p-side of the junction and positive ions, the atoms that donated an electron, on the n-side of the junction. These ions are also known as the space charges.

The region around the pn junction where the space charges are located is known as the depletion layer. The placement of the opposite ions across the junction forms an electrical field which prevents further electron flow from the n-side to p-side. If a reverse-bias is applied across such a p-n junction by connecting the cathode (n-terminal) to a higher voltage than the anode (p-terminal), then the depletion layer expands producing a non-uniform vertical electrical field with a maximum at the junction. The depth of this depletion region W_d is approximated by Equation 2.1:

$$W_d = \sqrt{2\epsilon_{si}\epsilon_o\mu\rho(V_A + V_{bi})} \tag{2.1}$$

where $\epsilon_{si} = 11.9$ is the silicon dielectric constant, $\mu = 1400\ cm^2/V_s$ is the mobility of the electrons at 300 K, ρ is the resistivity of the silicon which depends on the doping concentration, $\epsilon_o = 8.85 \times 10^{-14}\ F/cm$ is permittivity of the free space. V_A and V_{bi} are the applied bias and the built-in voltages, respectively.

Photoconductive p-n photodiodes generate an electric current that corresponds to the effective radiation energy of photons absorbed in the depletion layer. Each photon with an energy greater than 1.2 eV (the bandgap energy) excites an electron from the valence band to the conduction band, leaving a hole behind. The built-in vertical electric field in the depletion layer then accelerates the electron toward the cathode and the hole toward the anode, which leads to injection of an electric current equal to the charge on an electron into the read-out circuit. Thus, on the macro scale, the electric current generated is proportional to the number of photons absorbed, and hence the intensity of the incident radiation.

The planar photodiodes (Advanced Photonix SD 100-11-21-221) used in this study are not uniformly responsive to all frequencies of light due to the inverse relationship between the silicon light absorption coefficient and photon wavelength, according to the manufacturer data-sheet. For instance, a high-energy "blue" photon (short wavelength) cannot penetrate deep enough into

the silicon to reach the depletion region and excite an electron, but is absorbed instead in the diode surface. On the other hand, a low-energy photon with a wavelength longer than 1500nm does not carry the 1.2 eV bandgap energy required to excite an electron. Silicon is, therefore, transparent to such photons. A planar photodiode with a depletion layer of a certain depth, hence, is only responsive to a certain range of light frequencies.

The output capacitance of the photodiode, also known as the junction capacitance, is increased in a way that is directly proportional to area of the depletion region (A_d) and inversely proportional to its depth (W_d), as in Equation 2.2. This capacitance is particularly important due to its effect on the overall speed of the measurement. Most state-of-the-art PO systems have been developed in such a way that the photodiode shunt capacitance and the AFE input resistance form a complex pole, which defines the settling and time of the the analog front-end [7, 40].

$$C_d = \frac{A\epsilon_{si}\epsilon_o}{W_d} \tag{2.2}$$

There are two important conclusions that can be drawn from Equations 2.1 and 2.2 :

1. The size of the photodiode shunt capacitance decreases as the reverse-bias increases, which means that a large reverse-bias is associated with a read-out channel that settles quickly. This is essential when LEDs are

switched on for only a few hundreds of microseconds, as in modern PO devices.

2. The use of larger photodiodes to provide better PPG signal acquisition has the effect of also enlarging the shunt capacitance. An obvious solution would seem to be to increase the reverse-bias so as to compensate for this unwanted rise. However, this may not resolve the problem completely since there is a limit to the reverse-bias that most modern CMOS chips are able to support (namely, 3.3 volts for 350nm technology and 1.2 volts for 90nm technology).

Another way to mitigate the effect of a large shunt capacitance on the settling time would be to decrease the input resistance of the read-out channel by means of negative feedback. However, as will be explained in Chapter 3, this almost always leads to excessive power consumption and stability degradation. In this study, we employ a third approach, which is elaborated in Chapter 4, namely sensor decoupling. This uses an operational current amplifier(CA) in the class A or AB mode to eliminate the capacitive loading of the photodiode on the read-out channel, effectively shifting the slow pole due to the sensor shunt capacitance to a much higher frequency.

The incident light on the surface of the photodiode is not the only source of energy capable of exciting electrons into the conduction band. The ambient thermal energy can also do this, generating a current proportional to the ambient temperature and known as the dark current. This constitutes a temperature-dependent DC error in PO measurements given by the Shockley

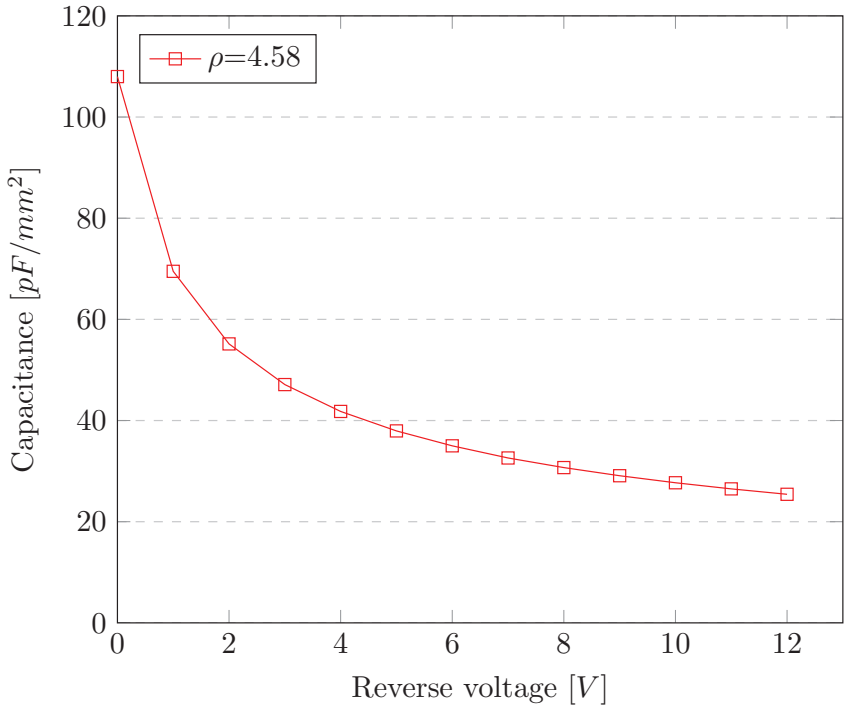


Figure 2.2: Photodiode output capacitance for various reverse voltages at 300°K temperature. The graph is drawn by MATLAB for this study using Equation 2.2 for silicon resistivity of ρ=4.85, which corresponds to the impurity, phosphorus, at a concentration of $10^{15} cm^{-3}$. The built-in potential is assumed to be 0.7 V.

diode equation (Equation 2.3):

$$I = I_0(e^{V_{diode}/U_{th}} - 1) \tag{2.3}$$

where V_{diode} is the voltage across the p-n junction (which is negative under the reverse-bias). The temperature dependent variables in this equation are

I_0, the dark saturation current, and U_{th}, the thermal voltage, which is equal to kT/q and approximately 25 mV at the room temperature.

Under a large reverse voltage, the contribution of the exponential term in Equation 2.3 is infinitesimal, so the dark current can be calculated by 2.4:

$$I_0 = Aqn_i^2\Big[\frac{D_n}{L_nN_A} + \frac{D_p}{L_pN_D}\Big] \tag{2.4}$$

Where where D_n and D_p are the diffusion coefficients of electrons and holes respectively, N_A and N_D are the concentration of acceptor and donor atoms respectively, L_p is the hole diffusion length within the quasi-neutral n-type region and L_n is the electron diffusion length within the quasi-neutral p-type region. A is the junction area and q is the charge on an electron.

The dark current in Equation 2.4 can be re-written as a function of temperature by combining all the temperature independent variables into a constant, as in Equation 2.5:

$$I_{dark} = Ak_0T^{3/2}exp\{-E_g/2kT\} \tag{2.5}$$

Within the operational temperature range of a typical PO device (40-125°K) the relationship between I_{dark} and temperature is shown in Figure 2.3. It

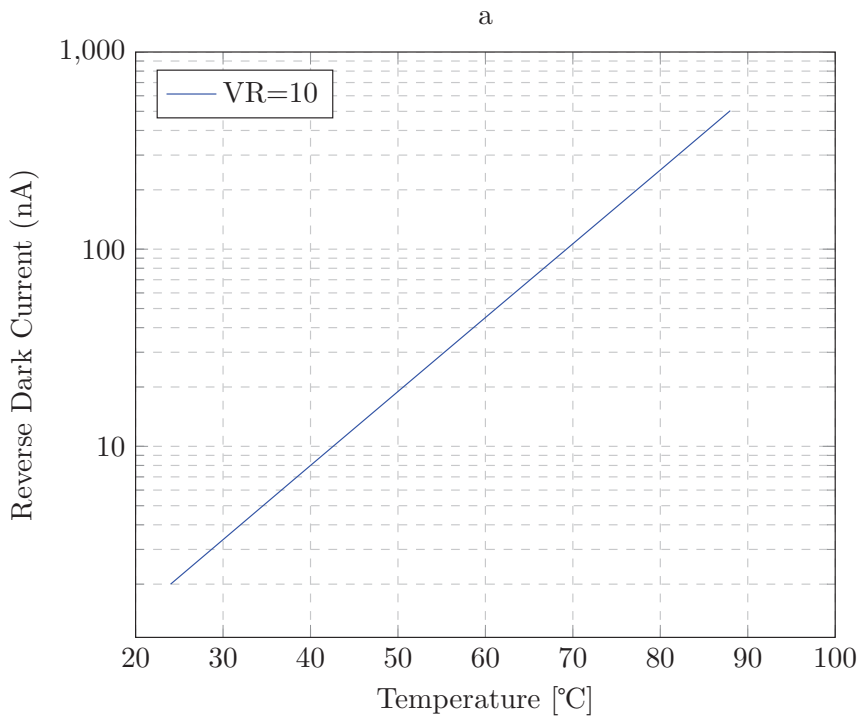


Figure 2.3: the temperature dependency of the dark current. Source: [Vishay Electronics PN photodiodes datasheet]. The graph shows that the dark current is monotonically increasing with the temperature.

can be seen that the dark current, which generates an error that reduces the accuracy of the measurement, typically doubles in magnitude for every 8°K rise in temperature.

The detector size also has a significant effect on the magnitude of the dark current. This is important since it highlights the benefit of a greater photocurrent, which a larger detector might provide, would be to some extent offset by the

increased dark current error. As will be explained in Chapter 5, in the AFE proposed in this study, the dark current error is eliminated by the adoption of a dual sampling technique.

2.2 PO Optical Sensor: LEDs

The power consumed by the AFE and A/D converter in modern PO systems has been considerably reduced by the use of more power-efficient analog-processing techniques and the availability of sub-micron CMOS microfabrication. This means that it is the LEDs that are the components that demand most power, accounting for up to 90 % of overall power consumption in modern pulse oximetry systems. One way to reduce this would be to develop an adaptive calibration algorithm capable of automatically adjusting the luminescence of the LEDs in real time so that it responded to the level of the PPG signal. Thus, if a patients PPG signal was strong, the LED power consumption would be reduced, whereas a weak PPG signal would be compensated by an increase in LED luminescence. The use of photodiodes with a larger photo-sensitive area could also lower the LED power consumption, since the collection of more light might mean that lower levels of LED luminescence would be sufficient to obtain accurate measurements. Chapter 5 includes a description of a novel techniques developed in this study for calibrating LED luminescence.

2.2.1 The physics of p-n LEDs

Under a forward bias condition, p-n photodiodes can be used to generate light of a specific wavelength. The underlying physical principles of such photon emission are relatively straightforward. As they cross from the n-side of the junction to the p-side, electrons that have been excited into the high energy conduction band return to the low energy band valence band and combine with holes. The net change in their energy (the bandgap energy) can be dissipated either in the form of heat or light. A radiative electron-hole recombination leads to the generation of a photon, the wavelength of which is inversely proportional to the bandgap energy and can be calculated from Equation 2.6:

$$\lambda = c.\frac{h}{W_g} \tag{2.6}$$

where λ is the wavelength of the emitted light, h is Plancks constant, W_g is the bandgap energy and c the is the speed of light. However, this equation assumes that the bandgap energy is totally converted to light. In practice, a portion of bandgap energy dissipates in the form of vibration energy of the semiconductor lattice, which leads to the generation of a relatively narrow spectral emission profile around the nominal wavelength [50].

Since semiconductor materials are characterised by a range of bandgap energies, LEDs producing light of different wavelenghts can be fabricated. AlGaInP

(aluminium-gallium-indium-phosphate) and InGaN/GaN (indium-gallium-nitride /gallium-nitride) produce red to yellow and green to blue LEDs, respectively [50]. A recent study has reported that both n-type and p-type doping in AlN (aluminium nitride) can produce radiation with a wavelength as short as 210nm, which is well into the ultra-violet region [51].

2.2.2 Temperature dependence of LED luminescence

Empirical data provided by the manufacturer indicates that LED luminescence falls as the junction temperature increases (Figure 2.4). This reduction inevitably means that the PPG signal acquired by the photodiodes of a PO system becomes weaker as the temperature rises. The problem of temperature-dependence becomes even more evident if Figures 2.3 and 2.4 are considered together. The combined effect of reduced LED luminescence and increased dark current means that temperature has a severe adverse effect on the accuracy of PO measurement.

This study addresses these two challenges separately. First, all non-optically generated current, including the dark current, is subtracted from the recorded signal. The temperature dependence of the LEDs is then compensated by an integrated automatic luminescence calibrator that reacts to any drop in the DC level of the generated photocurrent, whatever the reason. It is important that the two are performed in this order to ensure that a relatively error-free signal is used as the reference for the LED calibration.

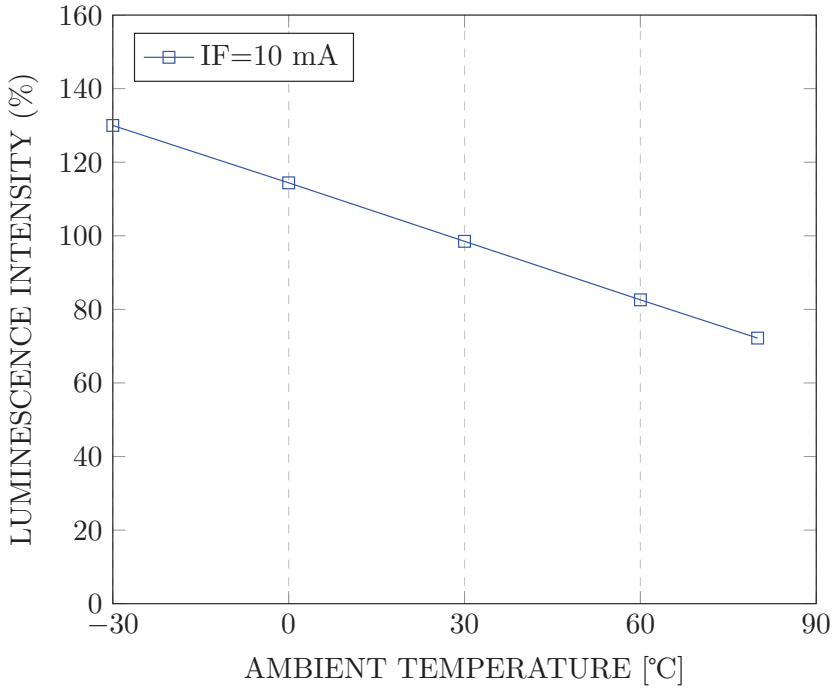


Figure 2.4: Luminescent intensity of Marktech LED, MTE5066S1J-UR, as a function of temperature. The measurement was conducted under a constant forward bias current of 10 mA. The data confirms that the light intensity drops as the temperature rises. [Source: Marktech Optoelectronic LED datasheet]

In addition to these two major concerns, temperature can have other kinds of negative impact on the reliability of the LEDs in a PO system. It can shrink the bandgap, thus changing the frequency of the emitted light.

2.2.3 LED Biasing and Luminescence Calibration

As explained above, a forward bias across the p-n junction of an LED is necessary to generate a flux of excited electrons. The brightness of the light produced is directly determined by the number of electrons crossing from the n-side to the p-side of the junction and participating in radiative recombination with holes. Thus, the LEDs luminescence can be controlled by the amount of forward bias applied. In fact, empirical data provided by the manufacturer for a typical LED shows an almost linear relationship (Figure 2.5).

Pulse oximetry requires the transmission of two wavelengths of light, namely red (660nm) and infra-red (950nm). These are generated by two different LEDs that, to economise on power consumption, are powered up in a phased fashion to produce a series of non-overlapping alternating flashes. The duration required for each flash has been significantly reduced in recent PO designs [40].

Since the LEDs are never both powered at the same time, a single front-end channel is sufficient to collect the PPG signal corresponding to both wavelengths. However, as mentioned earlier, the signal deriving from the infrared light is intrinsically stronger than that from the red light due to the difference in the depth that each wavelength of radiation penetrates. The luminescence level of each LED therefore needs to be calibrated independently to maintain the optimum power consumption.

The LED calibration circuit proposed in this study can both control the duration of the luminescence and also calibrate its power; See chapter 5. The former can be simply achieved by applying a square wave-modulated bias current with

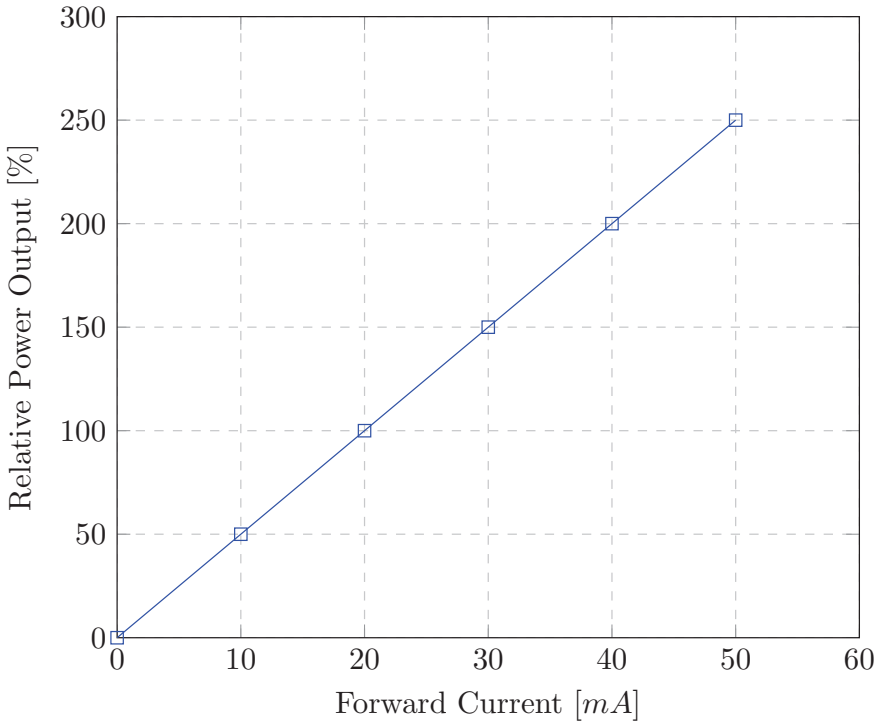


Figure 2.5: The LED relative output power as a function of forward current. The graph confirms that the luminescence is linearly related to the forward bias current. Source: Marktech Optoelectronic LED datasheet, device number: MTE5066S1J-UR.

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adjustable duty-cycle, in its simplest form by connecting a square-wave voltage to the power-down switch of a current mirror. The latter, however, requires modification of the amplitude of the bias current. The novel LED light intensity calibration algorithm developed for this study is explained thoroughly in chapter 5.

2.3 Frequency and Time Domain Analysis of the PPG Signal

The square wave-modulated bias current required to control the timing of the LED flashes can be modelled in the time domain as a series of delayed step function pairs with opposite polarity, as in Equation 2.7 below.

$$I_{LED}(t) = I_0 \sum_{n=1}^{\infty} u(t - NT) - u(t - (NT + DT)) \tag{2.7}$$

where I_0 is the amplitude of the bias current, T is the period and D is the duty-cycle of the square-wave. The Fourier expansion of this series is formulated in Equation 2.8, which can be used in conjunction with Parseval's theorem (Equation 2.9) to define the effective bandwidth of the bias current within which 99 % of the biasing energy is concentrated.

$$\begin{aligned} a_n &= \frac{2I_0}{n\pi} sin(n\pi D) \qquad \text{n=1,2,3,..} \\ a_0 &= I_0 D \\ b_n &= 0 \end{aligned} \tag{2.8}$$

where n is the harmonic number.

$$\sum_{n=0}^{\infty} a_n^2 = \frac{1}{T}\int_{t=0}^{t=T} I_{LED}(t)^2 dt \tag{2.9}$$

The first step in calculating this bandwidth is to determine the right side of Equation 2.9, which gives the power of the square wave-modulated bias current in the time domain. The second step is to calculate the minimum number of harmonics (K) among which more than 99 % of this power is distributed. This can be calculated by solving the inequality 2.10. Since K is the only variable, it is solely a function of the duty-cycle. The effective bandwidth can then be obtained by multiplying K by the frequency of the square-wave, f_0, which is 100 Hz in this study.

$$\sum_{n=0}^{K} a_n^2 > 0.99 D I_0^2 \tag{2.10}$$

Having calculated the a_n and K for a certain duty-cycle, the time domain expression for the bias current can be re-written as a summation of multiple sine-waves by using the inverse-Fourier series (Equation 2.11).

$$I_{LED}(t) = I_0(\frac{1}{2}D + \sum_{n=0}^{K} \frac{2}{n\pi} sin(n\pi D)\cos(n\omega_0 t)) \tag{2.11}$$

As explained earlier, when this square-wave bias current is applied to an LED,

it produces a regular series of flashes of light. The quantum efficiency of the LED (QE_{LED}), as reported by the manufacturer, can then be used to calculate the corresponding luminescence. As the light passes through the patients tissue, much of its power is dissipated and its amplitude attenuated as a result. We model this by a coefficient, α, which represents the average attenuation due to general transmission losses of this kind. It should be noted that as mentioned that attenuation coefficient is not the same for both wavelengths. As mentioned in the previous chapter, biological tissues are relatively transparent to the near infra-red light, which leads to less attenuation of infra-red light inside the tissue in comparison with the red light. Therefore $\alpha_R > \alpha_{IR}$.

The amplitude of the emitted light is also modulated because of the periodic variation of HbO_2 and Hb concentration in the blood, which the PO system is designed to monitor. When the light eventually reaches the photodiode, the photocurrent can be mathematically expressed by Equation 2.12,

$$I_{PhotoCurrent}(t) = \underbrace{QE_{LED}\alpha R_\lambda}_{\text{attenuation factor}} I_{LED}(t)(\underbrace{1}_{\text{DC component}} + \underbrace{i_{ac}(t)}_{\text{normalised AC}}) \quad (2.12)$$

where R_λ, is the spectral responsivity.

For the sake of simplicity, the normalised AC component of the photocurrent can be mathematically modelled by a single tone multiplied by the contrast factor(c), as in Equations 2.13 and 2.14 below.

$$c = \frac{i_{peak-to-peak}/2}{I_{DC}} \tag{2.13}$$

$$i_{ac}(t) = c \times \cos(\omega_{PPG_{max}} t) \tag{2.14}$$

The contrast is affected by a number of factors, including the spatial distribution of photodiodes and their proximity to the LEDs [44]. Most of the collected light has passed through non-perfused tissues, such as skin and bone, which are characterised by time-invariant optical absorption coefficients; this produces the dominant DC component of the photocurrent. The AC component, on the other hand, is significantly smaller in amplitude and corresponds to the periodic changes in the concentration of HbO_2 in perfused tissues due to the heartbeat. Thus, the PPG is a relatively low contrast signal (e.g. -40dB to -50 dB) [44], which makes its accurate measurement challenging. More than 99 % of the AFE headroom is occupied by the DC component, which means the AC component can be severely corrupted by A/D noise. This problem is addressed in the design proposed in this study by enhancing the signal contrast prior to digitisation with a contrast-enhancing pseudo-resistive amplifier (see Chapter 5). Moreover, the AFE must be low noise to maintain the integrity of the AC component prior to the ADC. Particularly, the transimpedance amplifier, the first block in the AFE chain must be design carefully to amplify the PPG signal without corrupting it with too much noise (see Chapter 4).

Analysis of the photocurrent properties in the time domain is completed by substituting Equation 2.11 in Equation 2.12, which leads to Equation 2.15 and Figure 2.6:

$$\begin{aligned} I_{PhotoCurrent}(t) &= I_0 Q E_{LED} \alpha R_\lambda \{\frac{1}{2}D + \sum_{n=0}^{K} \frac{2}{n\pi} sin(n\pi D)\cos(n\omega_0 t) \\ &+ \frac{c}{2} D\cos(\omega_{PPG_{max}} t) + \sum_{n=0}^{K} \frac{c}{n\pi} sin(n\pi D)\cos(n\omega_0 \pm \omega_{PPG_{max}} t)\} \end{aligned} \tag{2.15}$$

Previous PPG measurement result reported in other studies has led to two observations that are relevant to the time-domain characteristics of the photocurrent given by Equation 2.15:

- the bandwidth of the AC component is reported to be in the range 1 - 10 Hz [7, 52]. This implies that the fundamental frequency of the square wave-modulated bias current (f_0) must be at least 20 Hz to prevent aliasing (see Figure 2.6). f_0 is, therefore, set at 100 Hz to prevent the ubiquitous 50 Hz interference from folding into the base-band.

- there are other forms of low frequency interference which are not included in Equation 2.15. The motion artifact is particularly problematic since it lies within the PPG bandwidth and so cannot be readily filtered. There are advanced signal processing techniques, however, which are capable of removing this artifact from the PPG signal ([53, 54]).

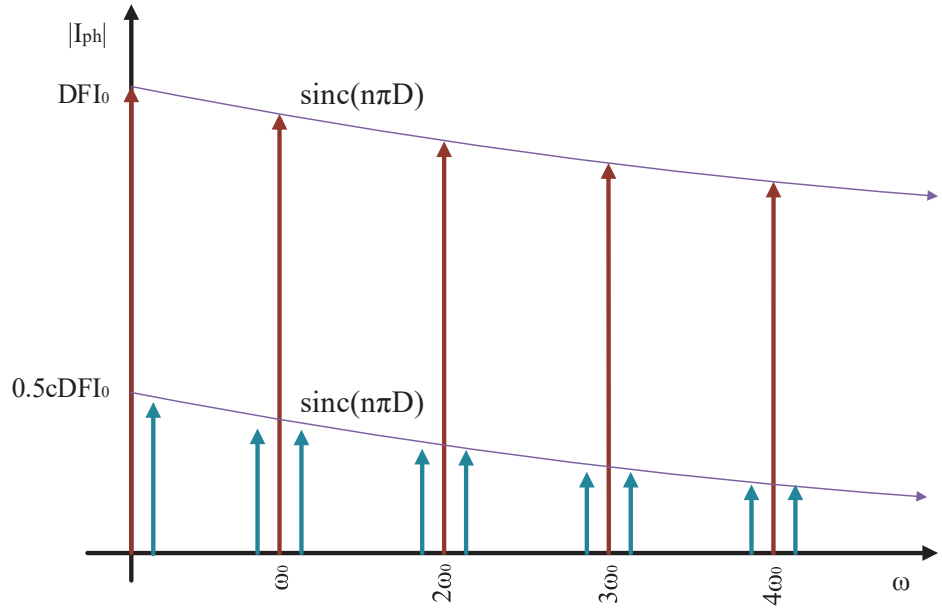


Figure 2.6: Frequency domain representation of the photodiode current as analysed in Equation 2.15. The AC component of the PPG signal appears as a series of pulses since it is modelled as a single tone. The plot is not to scale and relative dimensions have been exaggerated for the sake of clarity.

It can be seen from Equation 2.15 that the harmonics present in the photocurrent are related to the duty-cycle of the square wave-modulated bias current that is applied to the LED. Thus, as the duty-cycle decreases, high frequency harmonics become stronger and low frequency ones diminish. This redistribution of the power across a wider bandwidth adversely affects the signal-to-noise ratio (SNR) in the photodiode output. It also means that the current read-out amplifier following the photodiode must have a relatively small input impedance in order to ensure that the bandwidth of the system is sufficient to capture 99 % of the photocurrent energy.

The maximum acceptable input resistance can be calculated in the frequency domain by determining the required effective bandwidth using Equation 2.10, providing that the output capacitance of the photodiode is known.

The minimum required bandwidth to capture a square wave-modulated photocurrent can be calculated using Equation 2.16 :

$$\begin{aligned} \omega_{amp} = \frac{1}{R_{in}C_{PD}} &> \frac{5}{D} \\ \longrightarrow R_{in_{max}} &= \frac{D}{5C_{PD}} \end{aligned} \tag{2.16}$$

where C_{PD} is the photodiode output capacitance , D is the duty-cycle, and R_{in} is the front-end input resistance.

The circuit analysis provided in Chapter 3 addresses the complexity of designing a stable wide-band amplifier suitable for battery-operated system-on-a-chip (SoC) PO devices. The alternative would be to employ a narrow-band amplifier that captured, perhaps, only the 10 % of the signal concentrated in low frequencies. However, the SNR in this case would be severely degraded by the noise of the frontend, the trans-impedance gain of which would need to be 20 dB larger to compensate for the loss of signal.

2.4 Photodiode Noise and its effect on the overall resolution of SpO_2 measurement

We have seen that an LED-photodiode opto-pair can be regarded as a quasi-linear time-invariant system which converts the LED bias current into an amplitude-modulated photocurrent with similar spectral characteristics. Thus, applying a square wave-modulated bias current with wide effective bandwidth to the LED leads to a similarly wideband photocurrent at the output of the photodiode.

A reverse-biased photodiode also generates a form of wide-band noise due the quantised nature of light. The precise number of photons collected by the photodiode over a specific measurement period is subject to random variation, even though the average number of collected photons over a sufficiently large period of time remains relatively constant. As a result, the output current of the photodiode is contaminated with an additive Poisson noise, known as "shot noise".

The power spectral density (PSD) of the shot noise can be calculated from Equation 2.17:

$$I_{n,shot}^2 = 2qI_{ph}B \tag{2.17}$$

Where I_{ph} is the photocurrent amplitude and q is the electric charge of an electron. The total shot noise power can be calculated by integrating the noise PSD over the photocurrent bandwidth.

In the case of square-wave modulated photocurrent, higher harmonics of f_0 contain approximately equal proportions of the overall signal power when the duty-cycle is less than 3%. An optimal AFE should, therefore, provide a flat noise floor across the entire bandwidth to ensure that higher frequency harmonics are also processed acceptably. These can then be demodulated to the base-band by a switched capacitor circuit without compromising the overall SNR of the measurement. Such a demodulator effectively converts the wide-band discrete-in-time PPG signal into a relatively narrowband continuous-in-time signal that can be delivered to the A/D converter. Reducing the signal bandwidth in this way is essential for high resolution analog to digital conversion by allowing a larger over-sampling ratio.

As will be explained in Chapter 3, most modern PO systems can not achieve such a flat noise floor across the AFE bandwidth. Instead, for reasons associated with the photodiode capacitance, the noise floor increases monotonically as the signal frequency rises. One of the advantages of the novel design proposed in Chapter 4 is that, by decoupling the photodiode from the AFE, this noise problem is significantly ameliorated.

As reported earlier, the bandwidth of the AC component of a PPG signal is typically less than 10 Hz. Thus, provided that the AFE is capable of demodulating all the photocurrent harmonics into the baseband, the minimum

sampling rate required to digitise the signal without aliasing can be as low as 20 Hz (based on the Nyquist theorem). This means that a 10-bit A/D converter with a 20 kHz sampling rate could oversample by a factor of 1000. Equations 2.18 and 2.19 compare the ADC SNR for a signal sampled at the Nyquist frequency and one oversampled at ratio R, respectively.

$$SNR_{dB} = 6.02N + 1.76 \tag{2.18}$$

$$SNR_{dB} = 6.02N + 1.76 + 10.log10(R) \tag{2.19}$$

The extra resolution achieved by oversampling can be regarded as an increase in the effective number of bits (ENOB) of the A/D converter. For instance, a 10-bit A/D converter with 20 kHz sampling rate digitizing a typical PPG signal with a 10 Hz effective bandwidth, would provide an SNR of approximately 92 dB, which would be the same as that provided by a 15-bit A/D converter sampling at 20 Hz (the signal Nyquist frequency).

High SNR A/D conversion is particularly important in PO devices because, as mentioned earlier, the PPG is a low contrast signal with a DC component typically 40 dB larger than its AC component. Thus, A/D conversion with less than 80 dB SNR would not be able to maintain the DC component of such a signal while simultaneously digitising its AC component with the SNR required for an accurate SpO_2 measurement.

A great deal of research has sought to amplify the AC component of biosignals without saturating the frontend output with amplifying the DC component. This can be conducted either by controlling the DC component to remain at a certain value using a negative feedback loop [40, 55] or amplifying the AC component with an active high-pass filter which uses a pseudo-resistor at its feedback to create a low-frequency pole [9, 56, 57]. Both of these approaches, however, increase not only the power consumption, but also the settling time of the system. A high-resolution A/D converter, on the other hand, might be capable of digitising the low contrast PPG signal without requiring AC pre-amplification.

2.5 Conclusion

This chapter has sought to identify the features of an optimal AFE as part of a modern PO system. The key factors in this regard are the LED bias duty-cycle, the PPG signal contrast, the photodiode output capacitance and the A/D converter resolution. The elements of the required AFE specification can now be summarised as follows:

- the AFE must provide a DC voltage to reverse bias the photodiode(s).
- the input resistance of the AFE must be relatively small to ensure that most of the photodiode current energy is captured.
- the AFE must convert the discrete-in-time, wide-band PPG current to a continous-in-time narrow band signal which can be digitised by a low

power oversampling A/D converter.

- the AFE must not add significant noise while processing the photodiode current. Ideally, the AFE noise floor should not add any noise much stronger than the photodiode (shot) noise to the measured PPG.

The next chapter mathematically analyses the complexity of AFE design for PO systems.

Chapter 3

Analog Front-end: Low Noise Current to Voltage Conversion

The system level requirements of an ASIC analog front-end (AFE) capable of interfacing with a PO opto-pair, processing the measured data, and driving an ADC efficiently have been discussed in Chapter 2. The aim of Chapters 3, 4 and 5 is to investigate circuit architectures at the transistor level that might be used in the design of such AFEs.

The fundamental components of an AFE are identified as: a low noise transimpedance amplifier (LNTIA), a correlated dual sampler, a luminescence calibrator and a contrast enhancer amplifier (CEA).

The LNTIA reads the PPG signal directly from the photodiode, ideally without corrupting the signal significantly with its noise. The transistor level design of a such low noise block can be challenging due to the loading effect of the pho-

todiode output capacitance. The dual-sampler compares the LNTIA output voltage when the PPG signal is present and when it is absent, thereby Canceling the DC offset of the LNTIA and other DC errors. The switch-capacitor sampler then converts the high frequency harmonics of the PPG signal into the baseband, which reduces the bandwidth of the signal. As explained in Chapter 2, such bandwidth contraction is an essential feature of the ADC design. The DC level of the down-converted signal is then used by the luminescence calibrator to assess the strength of the PPG, and the LED light intensity is adjusted to ensure that the required SNR is preserved. Finally, the CEA increases the signal contrast.

In this and the following chapter, the specification that the LNTIA must provide, such as noise, gain, input/output impedance, distortion and bandwidth, are determined and each is then designed at transistor level with 350 nm CMOS AMS technology. The Cadence Spectre simulator is used to investigate the performance of the LNTIA and identify any limitations in the design.

3.1 The low noise trans-impedance amplifier (LNTIA)

The first component in the AFE chain is a low noise trans-impedance amplifier(LNTIA), which provides a DC voltage to reverse bias the photodiode and thus reads-in the photocurrent, ideally without adding significant noise. It also provides high trans-impedance gain, which ensures that the noise generated by

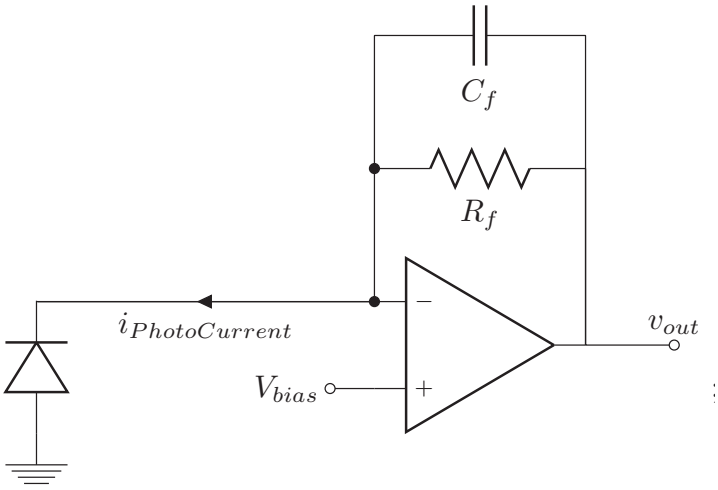
the following blocks does not compromise the overall SNR of the measurement.

Since the DC level of the PPG signal can vary within several orders of magnitude, the gain of the LNTIA must be programmable to prevent saturation of its output. The current to voltage conversion provided by this block is also vital, since most conventional post processing blocks, such as data converters, operate in the voltage domain. As explained in chapter 2, the square-wave modulated LED bias current has a small duty cycle (1 - 5 %), which leads to the generation of a wide-band photocurrent at the output of the photodiode. The LNTIA, therefore, must also have a relatively small duty cycle to capture most of the photocurrent signal energy.

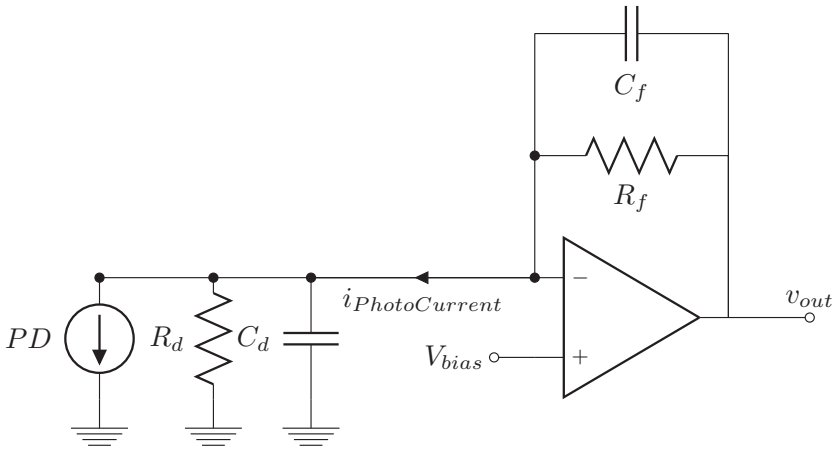
This section analyses the performance and stability of a resistive TIA, used as the sensor front-end in a number of other studies, such as [40, 42, 48, 49], and in the TEXAS INSTRUMENTS pulse oximeters IC (AFE4490), which does have some limitations and involves significant trade-offs.

A typical resistive TIA architecture is illustrated in Figure 3.1a. It is realised by a negative feedback loop through a resistor that, providing the op-amp has a large voltage gain, minimises the voltage difference between the op-amp input terminals. As a result, a positive bias voltage occurs across the photodiode, which makes it operate in photoconductive mode. Under these conditions, the photodiode can be modelled as an independent current source in parallel with a resistor and a capacitor [see Figure 3.1b].

Similar to any negative feedback system, the one depicted in Figure 3.1*b* can be modelled as a 3-element block consisting of a forward path transfer function,



(a)



(b)

Figure 3.1: (a) A resistive trans-impedance amplifier with a connected photodiode functioning in photoconductive mode as a result of the application of a positive bias voltage via a negative feedback loop (b) The photodiode is replaced by an equivalent R-C model.

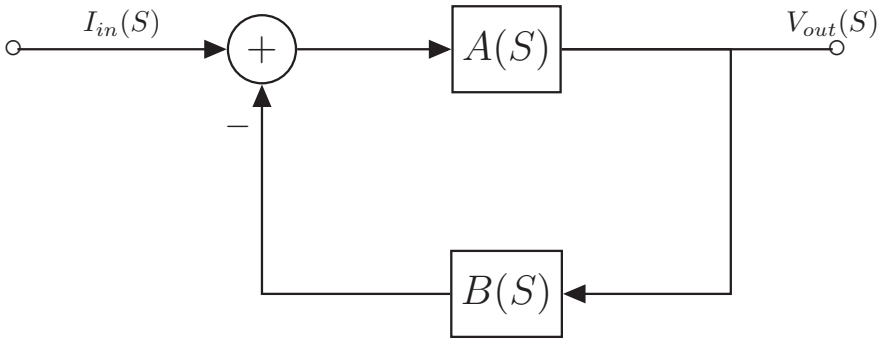


Figure 3.2: Block diagram representation of a negative feedback system.

A(S), a feedback path transfer function, B(S), and a comparator [see Figure 3.2].

Providing that A(S) and B(S) transfer functions can be calculated for a closed-loop system, it is easy to calculate its transfer function, and hence the gain and bandwidth, using Equation 3.1.

$$\frac{V_{out}(S)}{I_{in}(S)} = \frac{A(S)}{1 + AB(S)} \tag{3.1}$$

In addition, the product of the A and B transfer functions, known as the loop-gain transfer function, can be used in a margins analysis to assess the stability of the negative feedback loop.

The first step in calculating the A(S) and B(S) transfer functions is to define a transfer function for the op-amp. For the sake of simplicity, we model the

op-amp as a first-order low-pass amplifier with a DC gain, A0, [see Equation 3.2].

$$\frac{V_{out}}{V_{inp} - V_{inn}} = \frac{A_0}{1 + \tau_a s} \tag{3.2}$$

It should be noted that the first-order assumption is not always justified: devices that use more stages to provide higher DC gain, such as Miller op-amps, have more poles and zeros. Nevertheless, the single pole assumption is still valid if there is only one dominant pole.

Having defined the transfer function for the op-amp, the Kirchhoff's current law can be applied to its negative input terminal in the Laplace domain, leading to Equation 3.3.

$$G_f V_{out}(1 + \frac{C_f s}{G_f}) = G_f V_{inn}(1 + \frac{(C_f + C_D)s}{G_f}) + I_{in} \tag{3.3}$$

By replacing Vin in Equation 3.3 with a function of Vout from Equation 3.2, we obtain Equation 3.4, which has the same form as Equation 3.1, so A(S) and B(S) can be simply extracted from it.

$$V_{out}(S)(1+\underbrace{\frac{A_0(1+\frac{C_f s}{G_f})}{(1+\tau_a s)(1+\frac{(C_f+C_D)s}{G_f})}}_{\text{A(S)B(S)}}) = \underbrace{\frac{R_f A_0}{(1+\tau_a s)(1+\frac{(C_f+C_D)s}{G_f})}}_{\text{A(S)}} I_{in}(S) \quad (3.4)$$

The transfer function of the resistive TIA loop is then calculated by substituting the A(S) and B(S) obtained from Equation 3.4 into Equation 3.1, which leads to the closed-loop transfer function formulated in Equation 3.5.

$$\frac{V_{out}}{I_{in}} = \frac{R_f A_0}{T_a R_f (C_D + C_f)s^2 + (R_f(C_D + C_f) + T_a + R_f A_0 C_f)s + (A_0 + 1)} \quad (3.5)$$

The DC gain of the resistive TIA can be calculated from this equation for the case when $s{=}j\omega{=}\ 0$ [see Equation 3.6].

$$\frac{V_{out}}{I_{in}}|_{s=0} = R_f \frac{A_0}{A_0 + 1} \approx R_f \quad (3.6)$$

Since a high trans-impedance gain (R_f) is a system requirement for our AFE, we need to examine the effect of such a high R_f value on the overall performance of the resistive TIA to check whether this architecture is suitable for a pulse oximetry system. As discussed in Chapter 2, there are two other

key features that are also required: a short settling time and low integrated noise with the kind of resistor values that are typically available on a chip. A large feedback resistance is necessary to amplify the photocurrent sufficiently so that noise generated by following blocks in the AFE chain does not affect the overall SNR too much. However, the value of the feedback resistor also directly affects the noise performance of the TIA itself. Furthermore, a large value resistor has an adverse effect on the settling time of the TIA and limits the output voltage headroom. The output voltage is given by Equation 3.7:

$$V_{OUT} = V_{BIAS} + R_f I_{in} \tag{3.7}$$

Equation 3.7 indicates that, if R_f is chosen to be very large, then the output voltage (V_{OUT}) could saturate the op-amp output. This problem is even more pronounced in pulse oximetry systems due to the wide dynamic range of the PPG signal DC level which can vary from one patient to the other. One solution would be to make the trans-impedance gain programmable by replacing the feedback resistor with a number of smaller resistors connected in series. The overall resistivity could then be controlled by short-circuiting some of these. Assuming that the maximum and minimum resistivity obtainable in this way corresponds to the dynamic range of the input DC, then the voltage headroom problem could be resolved. However, for a conventional resistive TIA, the associated reduction in R_f might lead to TIA feedback loop stability degradation, increasing the settling time and degrading the systems stability.

Clearly, the trade-off between these various interconnected factors needs to be carefully assessed. In the following section we seek to mathematically analysing the adverse effect of the feedback resistor on the output settling time and system stability, and investigating the effect of R_f on noise performance.

3.2 The stability and settling time of a resistive TIA

We set the feedback resistance at 1 MΩ as the starting point for this analysis. The output capacitance of the photodiode (C_D) is defined by the active size of the photodiode and the reverse-bias voltage applied across it (as discussed in Chapter 2). For the analyses throughout this chapter, we set C_D at 10 nF. We also assume that the photodiode shunt resistor is large enough to be considered as an open-circuit. The TIA modelled in this study is required to be capable of handling photodiodes with large output capacitance without compromising the stability or the speed of the measurement. The settling time of a generic second-order system is, in general, given by Equations 3.8 and 3.9 :

$$H(S) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n + \omega_n^2} \tag{3.8}$$

$$T_s = \frac{4}{\zeta\omega_n} \tag{3.9}$$

Equation 3.5 can be rewritten in a form which is similar to Equation 3.8 [see Equation 3.10]:

$$H(S)_{TIA} = R_f \frac{\frac{A_0+1}{R_f(C_D+C_f)\tau_a}}{s^2 + \frac{1+\omega_a[R_fC_D+(1+A_0)R_fC_f]}{R_f(C_D+C_f)}s + \frac{A_0+1}{R_f(C_D+C_f)\tau_a}} \tag{3.10}$$

By comparing Equation 3.10 with Equations 3.8 and 3.9, the settling time is thus given by Equation 3.11:

$$T_s = \frac{8(C_D + C_f)}{\frac{1}{R_f} + \omega_a[(C_D + (1 + A_0)C_f]} \tag{3.11}$$

This equation suggests that it would be possible to compensate for a large settling time by increasing the DC gain of the op-amp (A_0). This gain, however, needs to be large enough to make $(1+A_0)C_f$ comparable to C_D if the settling time is to be significantly reduced, which is difficult to achieve using a single-stage op-amp, such as the one depicted in Figure 3.4 . As a result, recent studies have used op-amps with multiple gain stages, such as the Miller op-amp [40] or a distributed amplifier [7]. A drawback of the former is the power consumption due to the need to shift the second stage pole to relatively high frequencies in order to minimise the adverse phase shift effect on the phase margin when its output is loaded with the feedback network and

the photodiode output capacitance [as in Figure 3.1b]. A distributed amplifier comprised of a cascade of three first-order low-pass gain stages can be a preferable alternative. As explained in [7], this kind of structure can provide a relatively large gain-bandwidth product with moderate power consumption.

As mentioned above, Equation 3.11 indicates that having a wide-band op-amp (i.e. large ω_a) at the core of the resistive TIA loop will reduce the settling time. More specifically, if $\omega_a \gg \frac{1}{R_f[C_D+(1+A_0)C_f]}$, then the settling time becomes inversely proportional to the bandwidth of the amplifier. This way of reducing the settling time has a number of advantages:

1. Since modern photodiodes tend to have a relatively large output capacitance and feedback resistors are usually large to minimise noise (as discussed later in this chapter) $W_c = \frac{1}{R_f[C_D+(1+A_0)C_f]}$ is usually small. In our calculation, where C_D=10 nF, C_f=10 pF, R_f=1 MΩ and A_0=50dB, it is less than 100($rads^{-1}$). This leads to a further simplification of the settling time formula (Equation 3.12):

$$T_s = \frac{8}{\omega_a} \tag{3.12}$$

where ($\omega_a \geq 10\ \omega_c$). This equation allows the designer to determine the op-amp bandwidth on basis of the duty cycle of the LED square-wave modulated bias current, simply by setting the TIA settling time to be 5 times smaller than the photocurrent pulse width.

2. We assume that the core op-amp is a two-stage Miller, the first stage of which is depicted in Figure 3.4 with $\omega_a = \frac{GDS_p + GDS_n}{C_c}$. Since G_{DSn} and G_{DSp} are directly proportional to the tail current (I_{tail}), the op-Amp bandwidth can be simply controlled by adjusting I_{tail}. This produces a front-end that can handle photocurrents with various duty cycles, which is particularly advantageous when it is used in conjunction with adaptive algorithms that change the bias current duty cycle in a real-time fashion in order to maintain the SNR of the measurement while saving power [8].

3. In addition to providing a wide bandwidth, a large I_{tail} is also desirable for op-amp thermal noise attenuation, since the trans-conductance of the input PMOS increases as the tail current increases This is discussed further later in this chapter.

4. The stability of the resistive TIA negative-feedback loop is also enhanced by using a wide-band op-amp. This is quantitatively analysed below by investigating the phase margin.

3.2.1 Assessment of stability by phase margin calculation

The TIA negative feedback loop phase margin can be calculated from Equation 3.13, using the loop gain transfer function AB(S) from Equation 3.4:

$$AB(S) = \frac{A_0(1 + \frac{C_f s}{G_f})}{(1 + \frac{s}{\omega_a})(1 + \frac{(C_f + C_D)s}{G_f})} \tag{3.13}$$

The TIA loop gain transfer function has two poles and one zero at ω_{p_1}=$\frac{G_f}{C_f+C_D}$, ω_{p_2}=ω_a=$\frac{GDS_p+GDS_n}{C_c}$ and ω_{z_1}=$\frac{G_f}{C_f+C_D}$. The phase margin analysis measures the phase of the loop gain transfer function at crossover, where ||AB(ω_C)||= 0dB. This phase should be at least 60 degree to ensure that the polarity of the feedback loop remains negative even in the presence of the circuit noise.

Each pole shifts the loop gain transfer function phase by -90 degree, whereas a zero shifts the phase by +90 degree. Thus, if $\omega_a \geq \omega_{z_1}$, the phase shift caused by the second pole is neutralised by the zero phase shift. This effectively means that only the first pole shifts the phase of the transfer function, which ensures that the phase margin remains close to 90 degree, since the DC phase of the transfer function is 180 degree, irrespective of the crossover frequency.

On the other hand, if $\omega_a \ll \omega_{z_1}$ then both poles shift the loop gain phase, which dramatically reduces the phase margin. As mentioned above, the op-amp modelled in this study is assumed to be a first-order low pass system with a constant DC gain. This assumption is justified for the Miller op-amp used in this stability analysis, providing that the second- stage bias current is at least double the I_{tail}.

We continue our phase margin analysis by investigating the effect of R_f on the loop stability. As mentioned in Chapter 2, the photocurrent obtained in pulse oximetry devices can vary significantly. In the AFE developed for

this study, a calibrator tracks the DC output signal and adjusts the LED light intensity in a real time fashion to keep this current within a defined range. An alternative arrangement, discussed above, would be to make the trans-impedance gain programmable by replacing the single feedback resistor with a number of smaller resistors connected in series. The gain could then be altered by shorting out or adding in these small resistors as required. However, since the R_f value defines the frequency of the dominant pole and the zero in the loop gain transfer function (Equation 3.13), changing its value could degrade the stability of the loop. To be more precise, if the R_f value were reduced to accommodate a larger input DC level, the dominant pole and the zero would move toward higher frequencies whilst the op-amp pole remained at its original frequency. This would adversely affect the loop stability if the frequency difference between the two poles became relatively small, because the positive phase shift due to the zero would no longer be sufficient to compensate for the negative phase shift of the poles.

This behaviour has been confirmed by a stability analysis using Cadence to measure the phase margin of the resistive TIA loop depicted in Figure 3.2b. By varying Rf while all other parameters are kept constant, Cadence simulates the negative-feedback loop and calculates the phase margin for a range of Rf values. The result of this simulation is provided in Table 3.1.

As our previous analysis has suggested, the phase margin degrades as R_f is reduced. It should be noted that Cadence simulates PM=phase($AB(j\omega_c)$). PM is usually regarded as the loop stability safety margin in a closed-loop system with two poles. However, if the open-loop transfer function has a

zero at frequencies higher than that of the poles, the PM might not be an accurate indicator of the safety margin. In the Resistive TIA loop case, for instance, for some R_f values, the TF phase might fall rapidly toward zero as frequency increases, due to the presence of two poles at frequencies significantly lower than the crossover frequency. The phase might then recover at higher frequencies due to the positive phase shift of the high frequency zero. In such a situation, the reported phase margin might be misleadingly reassuring.

R_f	PM	Min Phase
1 MΩ	85	60
800 KΩ	83	55
500 KΩ	82	46
100 KΩ	65	30

Table 3.1: Simulated PM and minimum phase values for different values of feedback resistor. Where C_D=10nF, A_0=100, C_f=10pF and W_a=$\frac{1}{500kHz}$.

3.3 Noise analysis for a resistive TIA

Having investigated the stability of an AFE that uses a resistive TIA, we turn now to examine the question of noise. As we have repeatedly stressed, the contribution of the TIA to the overall noise of the AFE must be relatively low because the current produced by the photodiode is weak. In addition, since the

PO signal energy is distributed around multiple harmonics of the square-wave modulated photocurrent [as discussed in Chapter 2], the TIA must provide a uniform noise power spectral density (PSD) across a relatively wide bandwidth.

The mathematical analysis developed later in this section will show that the noise generated by conventional resistive TIAs is significantly increased at frequencies higher than $f_c = \frac{1}{2\pi C_D R_f}$, which leads to a non-uniform noise PSD. As explained in Chapter 2, modern oximeters use ring-shaped photodiodes to maximise the number of reflected photons. These are characterised by a relatively large output capacitance (C_D), of the order of tens of nanofarads. In addition, as we have explained above, R_f must be large (of the order of hundreds of KΩ) to keep the TIA's noise contribution low and provide a sufficiently large trans-impedance gain to compensate for the noise generated by later stages of the AFE, thus maintaining a high overall SNR. Nevertheless, having a large R_f when C_D is large too, leads to the shift of f_c to very low frequencies, which leads to significant amplification of the noise throughout the working bandwidth.

A further complication is that modern PO systems save power by using square-wave modulated current with a small duty cycle to bias the LEDs. This can mean that the working bandwidth of the photocurrent expands beyond the fc, with the effect that the core op-amp and bias regulator become the main contributors to the total input-referred noise. This can severely reduce the SNR and significantly increase the power consumption of the device.

Since the TIA amplifies its own input-referred flicker noise, the op-amp input

stage, which is the source of flicker noise, must be designed large to reduce this. For instance, the op-amp used in [40] employed gigantic CMOS transistors (1000μM/40μM) in its input stage.

The aim of this section is to analyse the noise performance of a resistive TIA in order to assess the trade-offs between power, area and noise. Since the photocurrent is already corrupted by the shot-noise when it reaches the amplifier, a TIA can be considered as low noise if its input-referred noise power is at least comparable with that of the shot noise. In order to make a fair comparison, the noise PSD curve must be integrated over the photocurrent effective bandwidth. This integrated noise can then be compared with $2qI_DB$, which is the integrated shot-noise power over the same bandwidth.

The theoretical analysis that follows is supported by simulation results provided by Cadence Spectre. In this way, we highlight the importance of designing a novel TIA which either eliminates the need for these trade-offs or optimises them, while at the same time providing acceptable noise performance.

The principal sources of noise in the TIA are the photodiode, the V_{bias} regulator, the feedback op-amp and the feedback resistor. Since these are all independent of each other, their noise contributions can be calculated individually and then added together, using the superposition principle. For instance, the feedback op-amp can be considered as the only noise generating component in the TIA circuit. The noisy op-amp is then modelled by a noiseless one that has a separate noise source attached to its positive input terminal [see Figure

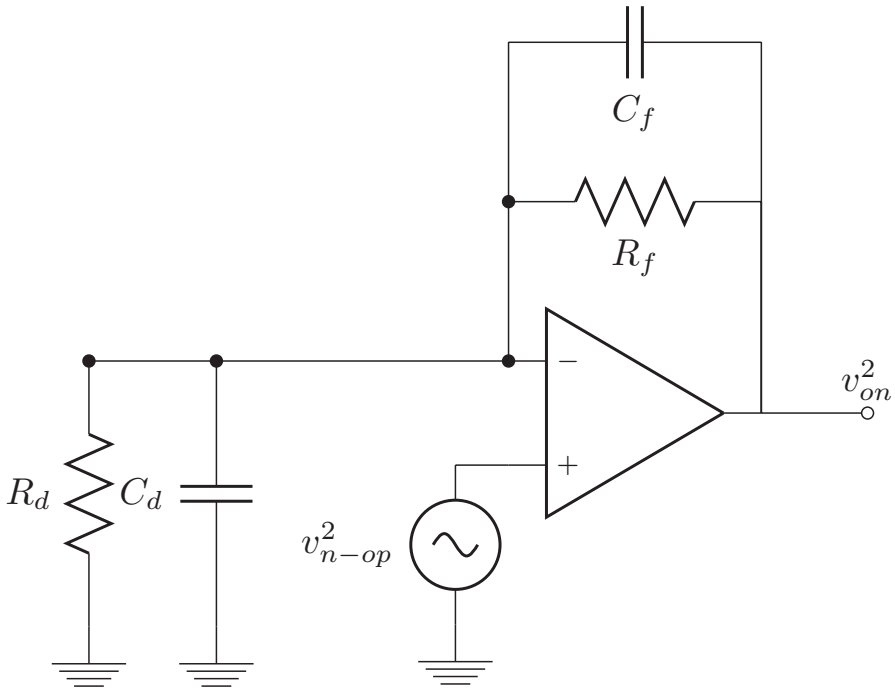


Figure 3.3: The resistive transimpedance with a noisy core op-amp which is modelled as an op-amp with a noise source at it positive terminal.

3.3]. This noise source models the input-referred noise voltage of the feedback op-amp, calculated for the specific architecture employed. The op-amp input-referred noise is finally referred to the input of the TIA, assuming that all the other components in the TIA circuit are noiseless.

By independently calculating the noise contribution of each source in a similar way, we can formulate the overall input-referred noise as the sum of series of noise current terms, as in Equation 3.14:

$$i_N^2 = i_{n,source1}^2 + i_{n,source2}^2 + i_{n,source3}^2 + i_{n,source4}^2 \tag{3.14}$$

3.3.1 Noise contribution of the op-amp

The contribution of op-amp noise to the overall input-referred noise current can be calculated by using Equation 3.15, 16 and 17 in following steps:

1. The transfer function from v_{n-op} to the output is calculated by applying the Kirchhoff's current low on the negative input terminal of the op-amp, leading to Equation 3.16.

2. By comparing the first term of Equation 3.16 with the loop gain transfer function, A(S)B(S), calculated in Equation 3.4, the denominator can be re-written to symplify the remainder of the calculation.

3. The input noise spectrum contributed by the op-amp noise, $\frac{i_{n-op}^2}{v_{n-op}^2}$, can be calculated as: $\frac{v_{on}^2}{v_{n-op}^2} \times \left|\frac{1}{H(S)}\right|^2$, as formulated in Equation 3.15, which leads to Equation 3.17.

$$\frac{i_{n-op}^2}{v_{n-op}^2} = \frac{v_{on}^2}{v_{n-op}^2}\left|\frac{1}{H(s)}\right|^2 \tag{3.15}$$

$$\begin{aligned}
\frac{v_{on}^2}{v_{n-op}^2} &= \left| \frac{1+\frac{Z_f}{Z_D}}{\frac{1}{A_0}(1+\tau_a)(1+\frac{Z_f}{Z_D})+1} \right|^2 \\
&= \left| \frac{\frac{1+R_f(C_D+C_f)s}{1+R_fC_fs}}{\frac{(1+R_f(C_D+C_f)s)(1+\tau_a)}{(1+R_fC_fs)A_0}+1} \right|^2 \\
&= \left| \frac{\frac{1+R_f(C_D+C_f)s}{1+R_fC_fs}}{\frac{1}{A(S)B(S)}+1} \right|^2
\end{aligned} \tag{3.16}$$

$$\begin{aligned}
\frac{i_{n-op}^2}{v_{n-op}^2} &= \left| \frac{\frac{1+R_f(C_D+C_f)s}{1+R_fC_fs}}{\frac{1}{A(S)B(S)}+1} \right|^2 \times \left| \frac{1+A(S)B(S)}{A(S)} \right|^2 \\
&= \left| \frac{1+R_f(C_D+C_f)s}{1+R_fC_fs} \right|^2 \times \left|B(S)\right|^2 \\
&= \left|1+R_f(C_D+C_f)s\right|^2 \times \frac{1}{R_f^2} \\
&= \left[\frac{1}{R_f^2}+(C_D+C_f)^2\omega^2\right]
\end{aligned} \tag{3.17}$$

The op-amp noise contribution (i_{n-op}^2) to the total input referred-noise current cannot be calculated from Equation 3.17 without knowing the corresponding

input referred-noise voltage (v^2_{n-op}). As mentioned earlier, this is determined by the architecture of the op-amp. However, since the first stage of the op-amp (a PMOS differential pair with active NMOS load) usually provides a large voltage gain, when it operates in the weak inversion region, it is safe to assume that the noise contribution of the following stages is negligible. This assumption has been made in other published studies [58]. As a result, the input-referred noise voltage of the differential stage (see Figure 3.4) can be treated as the total input-referred noise voltage of the op-amp (v^2_{n-op}).

v^2_{n-op} is calculated in Equation 3.18, where KF_P = 1.91e-26 and KF_N = 2.17e-26 are the flicker noise coefficients of the PMOS and NMOS devices respectively. The assumed temperature (T) is 300K; K is the Boltzmann constant $K = 1.38 \times 10^{-23} J/K$; C_{ox} is the gate oxide capacitance per unit area calculated in Equation 3.19 for the 350 nm technology; gm is the transistors' trans-conductance determined by the transistor operating region, dimensions and bias current [see Table 3.2]; W and L are the transistors' channel width and length respectively; and γ is the channel noise coefficient, a complex function of the transistors' basic parameters and bias condition (it is close to 2/3 for long channel devices).

$$v^2_{n-op} = \underbrace{2 \times 4kT\gamma\left[\frac{gm_n}{gm_p^2} + \frac{1}{gm_p}\right]}_{\text{Thermal Noise}} + \underbrace{\frac{2}{C_{ox}f}\left[\frac{KF_N gm_n^2}{(WL)_n gm_p^2} + \frac{KF_P}{(WL)_p}\right]}_{\text{Flicker Noise}} \tag{3.18}$$

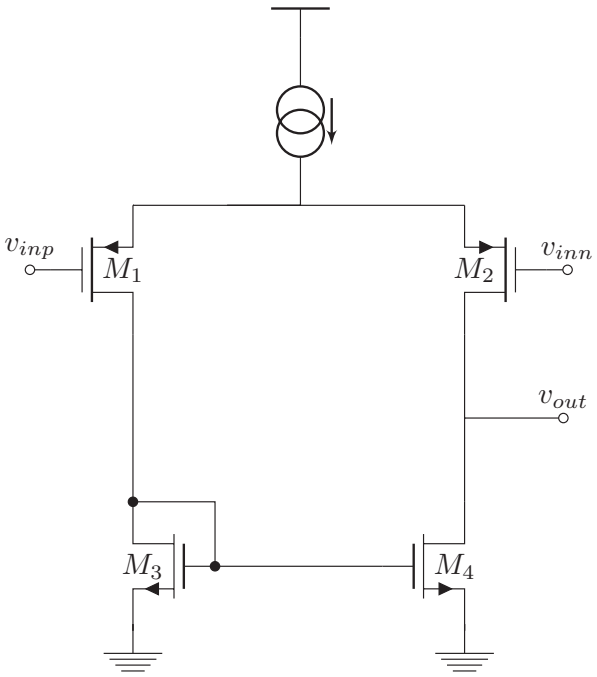


Figure 3.4: PMOS differential Gain stage with a voltage gain, Av= A_v = $g_m p \times (r_o p || r_o n)$, which can be as large as 40-50 dB while operating in the moderate inversion region. This stage is used as the feedback op-amp first stage throughout this section. Such a large voltage gain provided by the first stage is crucial to attenuate the noise contribution of the following stages.

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.9 \times 8.85e - 12}{7.6e - 9} = 1.16 \times 10^{-3} \tag{3.19}$$

Since $I_{DP} = I_{DN} = \frac{I_{tail}}{2}$, the following realistic assumptions can be made to further simplify equation 3.18 :

Region of operation	Transconductance (g_m)	Bias Condition
Strong inversion	$\sqrt{2\mu C_{ox}\frac{W}{L}I_D}$	$IC > 10$
Moderate Inversion	$\frac{kI_D}{V_T(\sqrt{IC+0.25}+0.5)}$	$0.1 < IC < 10$
Weak Inversion	$\frac{kI_D}{V_T}$	$IC < 0.1$

Table 3.2: CMOS transistor transconductance (g_m) for different operation regions. k is the gate coupling coefficient which models the coupling of the gate to the surface potential. $V_T = \frac{k_B T}{q}$ is the thermal voltage which is approximately 26 mV at the room temperature. $IC = \frac{I_D}{I_S}$ is the inversion coefficient, where $I_S = \frac{2\mu C_{ox} V_T^2}{k}\frac{W}{L}$ is the moderate inversion characteristic current.

1. The PMOS input pair shown in Figure 3.4 are assumed to operate in the moderate inversion region, i.e. where $0.1 < IC = \frac{I_D}{I_S} < 10$. Table 3.2 shows that for a fixed drain current (I_D) the CMOS transistor exhibits the largest g_m when it is operating in the weak inversion region. This is, therefore, the most power-efficient region of operation. Such a large g_m leads to further PMOS transistors thermal noise attenuation in Equation 3.21 for a specific bias current. However, biasing the CMOS transistor in weak inversion when the drain currents are relatively large is only possible if the CMOS aspect ratio $\frac{W}{L}$ is large, which increases the microfabrication cost. Thus, for a moderate area and power consumption, moderate inversion is the region of choice.

2. The width and length of the transistors used in the op-amp first stage (as shown in Figure 3.4) are assumed to be $W_n = \frac{1}{\alpha}W_p$ and $L_n = \alpha \times L_p$,

which leads to $(\frac{W}{L})_p = \alpha^2(\frac{W}{L})_n$, where $\alpha > 1$. This assumption, in conjunction with the fact that $I_{Dn} = I_{Dp} = \frac{I_{tail}}{2}$ and $k_n \approx k_p \approx 0.7$ can be used to calculate the ratio of inversion coefficients as in Equation 3.20.

$$\frac{IC_n}{IC_p} = \frac{I_{Sp}}{I_{Sn}} = \frac{\mu_p \times \alpha^2}{\mu_n} \approx \frac{\alpha^2}{3} \tag{3.20}$$

For large values of α and I_D, the NMOS transistors might operate in the strong inversion region whilst the PMOS transistors operate in moderate or weak inversion regions. Such operation in different inversion regions minimises the $\frac{g_{mn}}{g_{mp}}$ ratio while keeping W_nL_n=W_pL_p, which can significantly reduce the noise contribution of the NMOS transistors (see Equation 3.18).

These two noise-reducing assumptions are introduced into our noise analysis and later into our simulation in order to estimate the noise performance of a TIA realistically. Since our eventual goal is to compare the noise performance of the novel TIA developed for this study with that of a conventional resistive TIA, it is important to simulate the best possible resistive TIA to keep the comparison fair.

Figure 3.5 shows that, for the range of drain current values between 50 μA to 400 μA. $\frac{g_{mn}}{g_{mp}}$ is proportional to α. The g_m ratios depicted in Figure 3.5 are calculated for $W_p = 400\mu M$, $L_p = 1\mu M$, $W_n = \frac{W_p}{\alpha}$ and $L_n = \alpha L_p$. These device geometries leads to the operation of PMOS and NMOS devices in moderate and strong inversion regions respectively, for $6 \leq \alpha \leq 11$, which

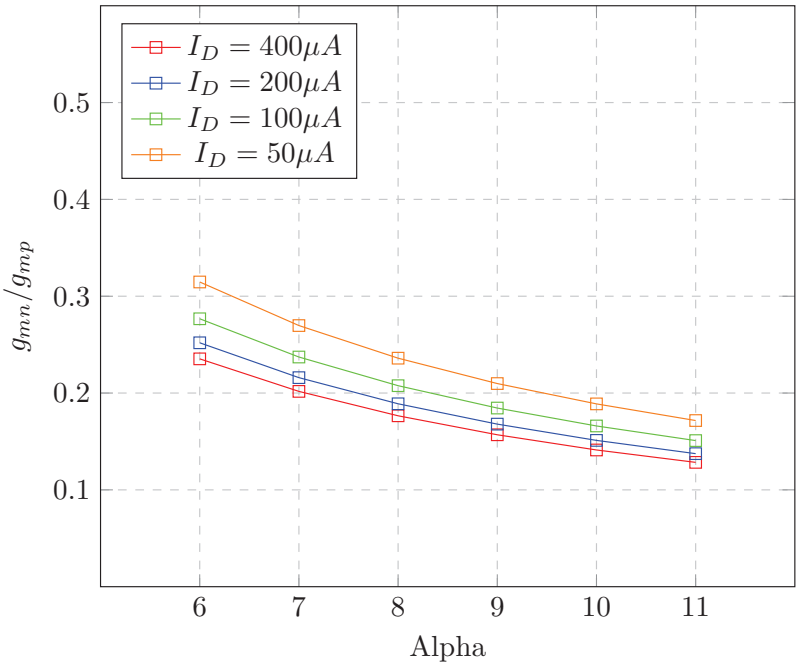


Figure 3.5: g_m ratio versus alpha (α) for I_D= 50, 100, 200 and 400μA, where W_p=αW$_n$=400μM, L_p=$\frac{1}{\alpha}L_n$=1μM and I_{Dn}=I_{Dp} = I_D. For all these drain currents the NMOS device operates in the strong inversion whereas the PMOS device operate in the moderate inversion [see table 3.2].

confirms that our two assumptions are realistic and non-contradictory.

For the sake of this analysis, let α=10 , so $\frac{g_{mn}}{g_{mp}}$ ≈0.2 [see Figure 3.5]. This means that Equation 3.18 can be rewritten as Equation 3.21:

$$v_{n-op}^2 = \frac{16kT}{3}\frac{2.4}{gm_p} + \frac{2K_p}{C_{ox}fWL} \tag{3.21}$$

The value of v_{n-op}^2 calculated from Equation 3.21 can then be placed into Equation 3.17 to calculate the contribution of the op-amp input referred-noise voltage to the overall input referred-noise current, giving Equation 3.22:

$$i_{n-op}^2 = \Big[\frac{16kT}{3}\frac{1.2}{gm_p} + \frac{2K_p}{C_{ox}fWL}\Big]\Big[\frac{1}{R_f^2} + (C_D + C_f)^2\omega^2\Big] \tag{3.22}$$

This equation can be re-written for frequencies $f \geq f_c = 10 \times \frac{1}{2\pi R_f(C_D+C_f)}$ to give Equation 3.23:

$$i_{n-op}^2 = \Big[\frac{32kT\pi^2 f^2}{gm_p} + \frac{8K_p(C_D + C_f)^2\pi^2 f}{C_{ox}WL}\Big] \tag{3.23}$$

Equation 3.23 confirms that for $f \geq f_c$ the input referred noise current PSD of the resistive TIA become frequency dependent, which leads to significant increase in noise power at higher frequencies. In addition, since the gm_p can only attenuate the thermal noise, the core op-amp must be designed using quite large devices, as mentioned earlier in this section, to reduce the flicker noise.

The severity of this problem becomes clearer when f_c is numerically compared with the working bandwidth of the TIA. For instance, if the LED is forward-biased with a square-wave modulated bias current of 100 Hz frequency and with a 1% duty cycle, The TIA must settle within 100 s. By using Equation 3.12, we can calculate the core op-amp bandwidth required for this settling time as $f_a = \frac{W_a}{2\pi} = \frac{8}{2\pi 100\mu s} = 12.7$ kHz. The input referred-noise PSD should be integrated across this bandwidth to calculate the noise power required for the SNR calculation. We can, then, calculate $f_c \approx 16$ Hz for $C_D = 10$ nF, $C_f = 10$ pF and $R_f = 1$ MΩ. This leads to the conclusion that for all frequencies above 160 Hz, the resistive TIA operates in the high noise region, whilst the

bandwidth of interest is 0.1 Hz - 12.7 kHz.

3.3.2 Noise contribution of the V_{bias} regulator

The regulator circuit which generates the V_{bias} voltage, used in the RTIA circuit depicted in Figure 3.1b, also contributes to the overall input-referred noise current. This contribution can be calculated in a way that is similar to that of the core op-amp. The only difference is the noise voltage source added to the positive input terminal of the op-amp in Figure 3.5 must be replaced with a source which models the regulator circuit, shown in Figure 3.6, output noise voltage (v_{n-bias}), which is calculated in Equation 3.24.

$$v_{n-bias}^2 = \left(\frac{4KT}{R_1}R_2^2 + \frac{4KT}{R_2}R_2^2 + 4\zeta\frac{2KT}{g_{mp}} + \frac{2K_{Fp}}{c_{ox}fW_pL_p}\right)\left(\frac{1}{(\frac{R_1+R_2}{R_1})^2 + \omega^2 c_L^2}\right) \tag{3.24}$$

Equation 3.24 suggests that the regulator noise can be attenuated by choosing small R_1 and R_2, which increases the regulator power consumption since $I_{DM1} = \frac{v_{bandgap}}{R2+R1}$. If these resistor values are chosen to be equal and so small that their noise contribution becomes negligible, then we can simplify Equation 3.24 to Equation 3.25 because the $\left[(\frac{R_1+R_2}{R_1})^2 + \omega^2 c_L^2\right]$ can be approximated by 4 unless a very large C_L value is chosen (which would require off-chip components).

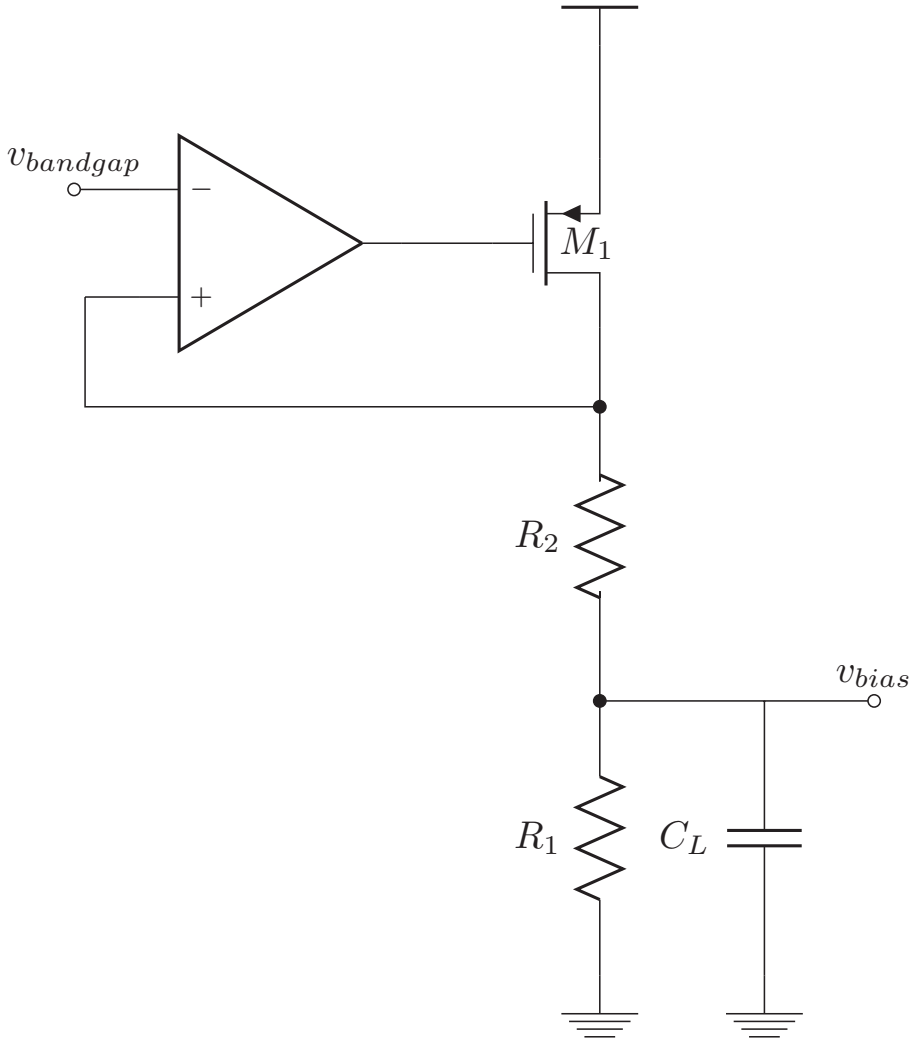


Figure 3.6: Low dropout regulator using a resistive voltage divider to generate the $V_{bias} = V_{BG} \times \frac{R_1}{R_1+R_2}$. A load capacitor can be added to the output node to filter the LDO noise at high frequencies.

$$v_{n-bias}^2 = \left(\frac{4}{3} \frac{KT}{g_{mp}} + \frac{K_{Fp}}{2c_{ox} f W_p L_p} \right) \tag{3.25}$$

Since the regulator output is connected to the positive terminal of the op-amp, its noise affects the TIA input referred-noise current in the same way as the core op-amp noise, which means that the performance of the op-amp used in the regulator must be comparable to that of the core amplifier. This requirement could potentially double the overall power and silicon consumption of the device. A solution to this problem is explained in Chapter 4; it involves a sensor decoupling approach which to an extent cancels the contribution of the regulator noise to the overall input noise current.

3.3.3 The total input-referred noise

Having calculated the noise contributions of the core op-amp and the regulator, it is now possible to incorporate the noise of the TIA feedback resistor and the photodiode shot noise into our analysis, to give Equation 3.26, which is the total input referred-noise current of the resistive TIA:

$$i_{n-total}^2 = 2qI_D + \frac{4KT}{R_f} + (v_{n-bias}^2 + v_{n-op}^2)\Big[\frac{1}{R_f^2} + (C_D + C_f)^2\omega^2\Big] \qquad (3.26)$$

It can be seen that the input referred-noise current monotonically increases with frequency for frequencies higher than a few hundred Hertz. As a result, the portion of photocurrent signal power concentrated at higher frequencies is corrupted by much greater noise than the base-band harmonic.

The noise performance of the resistive TIA depicted in Figure 3.2b has also been simulated in Cadence using the circuit parameters listed in Table 3.3.

Parameter	Value	Parameter	Value
$M_{1,2}$	$400\mu/1\mu$	$M_{3,4}$	$40\mu/10\mu$
R_2	20KΩ	R1	100KΩ
C_D	10nF	R_D	OC
C_f	10pF	R_f	800KΩ
C_c	1pF	R_c	200
C_{LDO}	5pF	V_{BG}	1.2

Table 3.3: Circuit component parameters used for the noise simulation.

The resistive TIA input-referred noise current simulated PSD curve are shown in Figure 3.7, Which confirms that the Input-referred noise floor increases monotonically with the frequency.

The resistive TIA input-referred RMS noise current is compared with that of the novel TIA designed for this study in chapter 4. To permit a fair comparison, the power consumption of each design is also included in the analysis provided in chapter 4.

3.4 conclusion

We conclude this chapter by summarising the non-idealities which limit the suitability of a resistive TIA for a pulse oximetry device. Some of these limitations can only be rectified by increasing the power aggressively, whereas others require extremely large on-chip components, which increases the microfabrication cost.

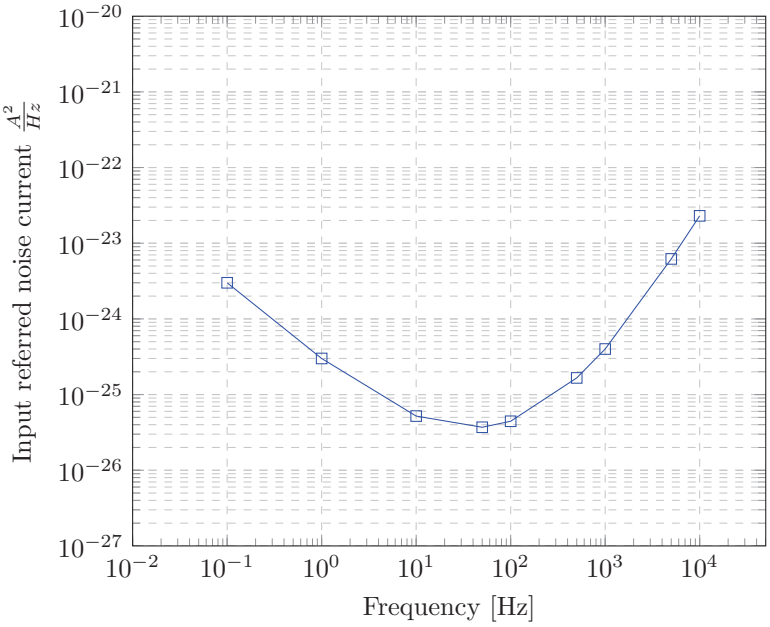


Figure 3.7: Simulated front-end input referred noise current PSD comprised of the core op-Amp, regulator and feedback resistor noise. The simulation is conducted using the resistive TIA architecture shown in Figure 3.2b, in conjunction with the V_{bias} regulator depicted in Figure 3.6.

1. The photodiode bias voltage consumes the available DC output headroom. This effectively limits the maximum value allowed for the feedback resistor.

2. The photodiode output capacitance and the feedback resistor form a low frequency zero in the input referred-noise PSD, which leads to the amplification of the core op-amp and regulator noise at frequencies higher than a few hundred hertz.

3. The regulator op-amp noise contribution to the overall input referred noise is similar to that of the core op-amp, which effectively means that

the resistive TIA requires two low noise op-amps instead of one.

4. The resistive TIA open loop transfer function has two poles and one zero where the frequency of one pole and one zero are defined by the feedback resistor. Analysis shows that, due to this dependency, the stability of the loop can be compromised if the R_f is reduced while other parameters remain constant. This effectively means that the trans-impedance gain cannot be programmed.

Interestingly, all of these limitations are ultimately due to the loading effect of the photodiode on the TIA negative feedback loop. We have therefore developed a decoupling circuit which completely eliminates them by separating the photodiode from the trans-impedance loop. The design of this novel feature is discussed in the following chapter.

Chapter 4

Low Noise TIA with Sensor Decoupling

The noise and stability analyses presented in Chapter 3 suggested that most of the limitations of trans-impedance amplifiers in AFEs are due to the loading effect of the photodiode. This chapter contains further analyses and simulations which confirm that decoupling the photodiode from the TIA negative-feedback loop by inserting a current amplifier (CA) between the photodiode and the resistive TIA, as shown in Figure 4.1, can largely overcome these problems and eliminate the associated trade-offs. The performance of this novel low noise transimpedance amplifier (LNTIA) is also assessed using various simulations, presented throughout this chapter.

The decoupling CA must provide a DC voltage large enough to reverse bias the photodiode, and its input impedance must be small enough to ensure that

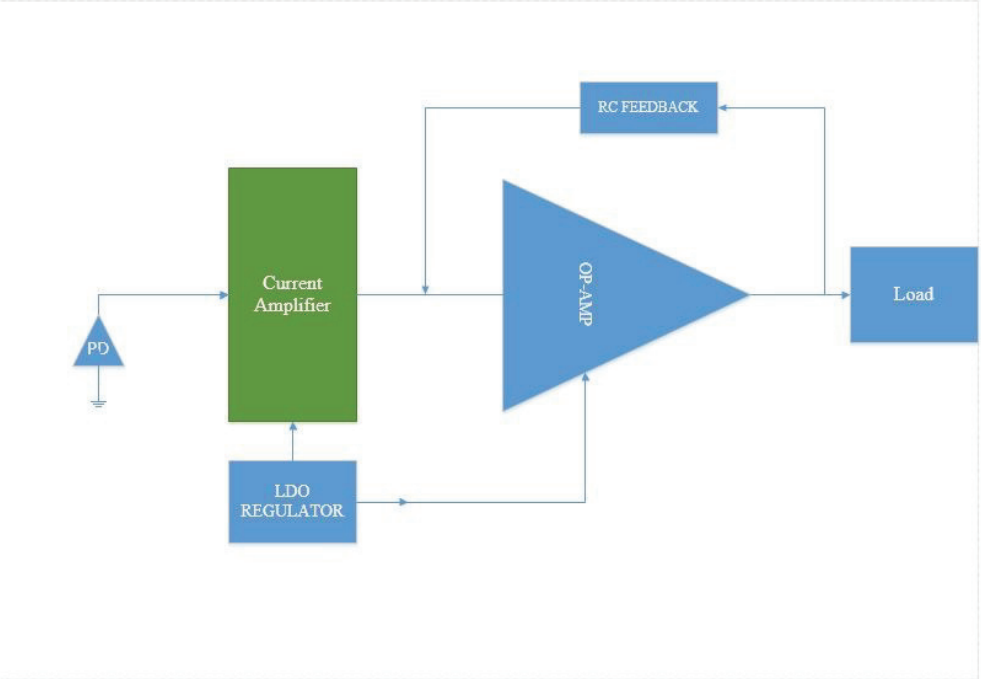


Figure 4.1: The Proposed LNTIA including a current amplifier to decouple the photodiode from the resistive TIA loop.

the AFE can read in square wave- modulated photocurrents with a small duty cycle (of the order of 1 %). It must also provide a moderate current gain to minimise the TIAs contribution to the overall input-referred noise current.

The transistor-level architecture for such a CA, along with the photodiode electrical model, is shown in Figure 4.2.

Sections 4.1, 4.2 and 4.3 mathematically investigate the circuit characteristics and noise performance of this CA, and Section 4.4 simulates the combined CA, TIA and photodiode set-up (as in Figure 4.1) using Cadence Design Framework (CDF). Taken together, this analysis provides the data necessary to compare

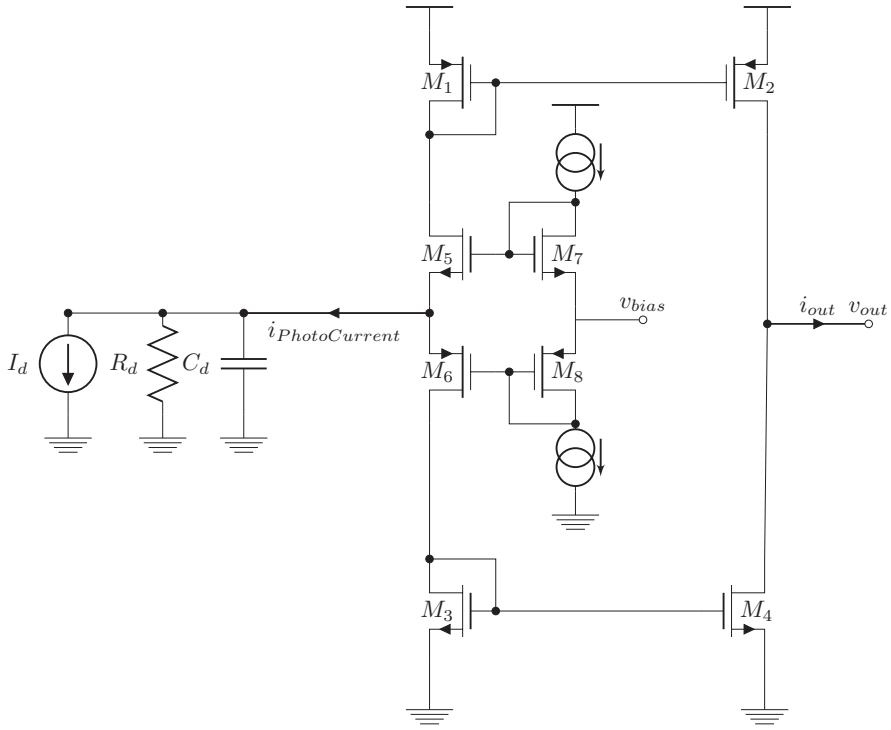


Figure 4.2: The current amplifier circuit loop along with the photodiode RC model.

the performance of the novel LNTIA proposed with that of a conventional resistive TIA.

4.1 Sensor decoupling current amplifier: architecture and analyses

The DC operating points of the CA shown in Figure 4.2 can be studied by identifying the trans-linear loop formed by the M_{5-8} transistors, leading to

Equation 4.1:

$$I_{D5} \times I_{D6} = I_{D7} \times I_{D8} \tag{4.1}$$

where I_D stands for the drain DC current. By using this equation in conjunction with I_{D7}=I_{D8}=I_{bias} and I_{D5}=I_{D6}, it can be shown that I_{D5}=I_{D7}=I_{bias}, which leads to V_{PD} = V_{S5}=V_{S7}=V_{bias}. Thus, the proposed architecture keeps the V_{bias} voltage provided by a regulator across the photodiode, as required for the reverse biasing.

The trans-linear loop exploited in Equation 4.1 is only valid when M_{5-8} are operating in the weak-inversion region, i.e. their VDS $\geq$ 4VT = 100 mV at room temperature. As explained later in this chapter, operating the M_{5-8} transistors in this region is desirable because the gm is maximised, leading to a minimum settling time for any specific I_{bias}. By contrast, it is preferable to operate M_{1-4} devices in the strong inversion region, where gm is minimum for a given bias current, so as to minimise their drain noise current.

The maximum reverse-bias voltage is given by:

$$V_{bias_{max}} = VDD - \left[\sqrt{\frac{2I_{bias}}{\mu_p c_{ox}(\frac{W}{L})_{M1}}} + V_{th}\right] - 4V_T \tag{4.2}$$

The above DC analysis does not take the photocurrent DC into account. The

physics of a reverse-biased photodiode dictates that the sensor sinks a current from the CA. Including this factor in the analysis, V_{PD} can be calculated more completely as:

$$V_{PD} = V_{bias} - \log\left[\frac{I_{in}}{I_0}\frac{L}{W}\right]\frac{V_T}{k} \tag{4.3}$$

where I_0 is a process- dependent constant and $k = \frac{C_{ox}}{C_{ox}+C_{dep}}$, is the gate coupling coefficient.

The simulation results reported in section 4.4 confirm that, for the large aspect-ratio values necessary to keep M5 and M6 transistors operating under weak-inversion conditions, V_{PD} remains relatively constant for a wide range of input currents. An interesting consequence of the decoupling provided by the CA is that, unlike a conventional resistive TIA, the photodiode bias voltage does not limit the output voltage headroom. This allows a larger photodiode bias voltage, which reduces the PD output capacitance as explained in chapter 2. The reduction of PD output capacitance, as explained later in this chapter, decreases the settling time of the LNTIA.

The above analysis assumes that M_5 and M_7 are perfectly matched. However, this is not always the case when the circuit is microfrabicated on a sillicon wafer. The effect of device mismatches can be simulated using the Monte Carlo (MC) analysis provided by Cadence. This simulation calculates the DC operation points of the CA for various MC samples. ($V_{SourceM5}$) must remain

larger than 1.5 V for all MC samples to guaranty the photodiode reverse bias at the presence of random matches between the CA transistors. The result of the MC simulation is presented later in this chapter.

4.2 Current amplifier: gain and input impedance

As discussed in Chapter 2, the reverse-biased photodiode depicted in Figure 4.2 sinks the photocurrent from the positive supply through the M_1 and M_5 devices. The CA bias current, I_{bias}, also flows through these transistors. Therefore, by including the current mirror principles into the calculation, i_{OUT} is given by:

$$i_{OUT} = \left[\frac{\left(\frac{W}{L}\right)_{M2}}{\left(\frac{W}{L}\right)_{M1}}\right]\left[I_{BIAS} + i_{IN}\right] - \left[\frac{\left(\frac{W}{L}\right)_{M4}}{\left(\frac{W}{L}\right)_{M3}}\right]\left[I_{BIAS}\right] \tag{4.4}$$

The current gain can be extracted from 4.4, by assuming $\left[\frac{\left(\frac{W}{L}\right)_{M2}}{\left(\frac{W}{L}\right)_{M1}}\right] = \left[\frac{\left(\frac{W}{L}\right)_{M4}}{\left(\frac{W}{L}\right)_{M3}}\right]$, as:

$$A_i = \frac{\left(\frac{W}{L}\right)_{M2}}{\left(\frac{W}{L}\right)_{M1}} \tag{4.5}$$

The condition of identical aspect ratios, however, might not hold in the presence of mismatch between the current mirrors transistors. Therefore, since

PMOS devices exhibit relatively better matching than NMOS devices, a portion of CA bias current might bleed into the next stage and generate a DC offset. Chapter 5 will describe a novel correlated dual-sampler that can eliminate this DC offset provided that it does not saturate the output. Thus, A certain level of matching between mirror devices is required, which can be achieved by designing the devices as multiples of unit transistors connected in parallel. For instance, a current gain of A_i=5 (A/A) can be obtained by making $(\frac{W}{L})_{M_1} = 2 \times \frac{20\mu M}{10\mu M}$ where $\frac{W}{L}_{M_2} = 10 \times \frac{20\mu M}{10\mu M}$. In this case, M1 consists of two unit transistors connected in parallel, while M2 comprises 10 such unit transistors. The M1 and M2 unit transistors can be symmetrically interdigitated when the devices are fabricated to maximise the matching between them.

4.2.1 The input impedance

Equation 4.6 gives the input impedance of the of CA shown in Figure 4.2, where $(gm_5 + gm_{b5})r_{DS5} \gg 1$. This equation can be used to estimate the frequency of the LNTIA dominant pole, which is determined by the photodiode output capacitance and the CA input impedance.

$$Z_{in}(s) = \frac{1}{gm_5 + gm_{b5}} || \frac{1}{(C_{gs5} + C_{bs5})s} \tag{4.6}$$

Equation 4.7 highlights the relationship between the overall trans-conductance of M_5 and the pole frequency. For a certain drain current, the latter can be maximised when M_5 is operating in the weak inversion region.

$$\omega_p = \frac{gm_5 + gm_{b5}}{C_{gs5} + C_{bs5} + C_D} \approx \frac{gm_5 + gm_{b5}}{C_D} \tag{4.7}$$

Operation in the weak inversion region also leads to a further simplification:

$$\omega_p = \frac{\frac{kI_D}{V_T} + \frac{(1-k)I_D}{V_T}}{C_D} \approx \frac{I_D}{V_T C_D} \tag{4.8}$$

Where I_D=$I_{Bias} + I_{PD}$. Having calculated the dominant pole frequency, the settling time is given by:

$$T_s = \frac{5}{\omega_p} \tag{4.9}$$

The CA depicted in Figure 4.2 works in class AB mode if $I_{Bias} \leq I_{PD}$. This mode of operation is characterised by efficient power consumption owing to the fact that the CA mainly draws power when there is a photocurrent, which is only 3-5 % of the time. The I_{Bias}, however, must be sufficiently large to ensure that the CA settling time remains reasonably small when the photocurrent is weak. In such a case, the CA operates in Class A mode. The AFE proposed in this study utilises an LED light calibrator (see Chapter 5) which increases

the LED bias current when the photodiode DC level is low. Therefore, the class AB operation is restored when this current rises.

4.3 LNTIA: Feedback loop stability enhancement

Placing the CA between the photodiode and the resistive TIA cancels the loading effect of the photodiode output capacitance, because of which the resistive feedback loop phase margin is degraded. The typical RTIA loop transfer function formulated in Chapter 3 as:

$$AB(S) = \frac{A_0(1 + \frac{C_f s}{G_f})}{(1 + \frac{s}{\omega_a})(1 + \frac{(C_f + C_D)s}{G_f})} \tag{4.10}$$

Where C_D denotes the photodiode output capacitance in the absence of the sensor decoupling amplifier. This equation can be modified to formulate the resistive TIA open-loop transfer function when the CA is placed in the AFE chain simply by replacing C_D with $C_{gd4} + C_{gd3}$, (see Equation 4.11).

$$AB(S) = \frac{A_0(1 + \frac{C_f s}{G_f})}{(1 + \frac{s}{\omega_a})(1 + \frac{(C_f + C_{gd4} + C_{gd3})s}{G_f})} \approx \frac{A_0}{(1 + \frac{s}{\omega_a})} \tag{4.11}$$

The CA output capacitor size, $C_{gd_4} + C_{gd_3}$, is significantly lower than the feedback capacitor, C_f, which leads to $\omega_{p_2} \approx \omega_z$. Therefor, the second pole is canceled by the zero. The open-loop transfer function therefore has only one pole, which shifts its phase by at most 90. It should be noted that the feedback op-amp second-stage pole, which is not included in this calculation, can still affect the open-loop phase margin. Nevertheless, by adding a compensation capacitor, sufficient pole separation can be achieved.

The zero-pole cancellation also eliminates the adverse effect of R_f on the loop stability, which allows stable programmable trans-impedance gain. This has been verified using Cadence stability analysis to simulate the phase margin of the TIA loop for a range of R_f values (see Table 4.1). As predicted by the above analysis, this simulation confirms that the stability of the proposed LNTIA feedback loop is not affected by varying R_f. Thus, the insertion of the CA offers the possibility of adding programmable gain, in the form of adjustable R_f, which is not available in a conventional resistive TIA.

R_f	PM	Min Phase at $\omega \leq \omega_{CO}$
250 KΩ	59	59
125 KΩ	57	57
62.5 KΩ	60	60
22 KΩ	67	67

Table 4.1: Resistive TIA negative feedback loop phase margin for various R_f values. The loop Phase margin is simulated using Cadence stability analysis.

4.4 LNTIA: Settling Time

The transfer function of a resistive TIA with a photodiode connected to its input is formulated in Equation 3.10, in the previous chapter. This equation can be updated to represent the transfer function of resistive TIA embedded in the LNTIA circuit depicted in Figure 4.1, by replacing the C_D with $C_{gd4}+C_{gd3}$, the output capacitance of the CA, assuming that $(C_{gd4} + C_{gd3}) \leq C_f$.

$$H(S)_{TIA} \approx R_f \frac{\frac{A_0+1}{R_f C_f \tau_a}}{s^2 + \frac{1+\omega_a[(1+A_0)R_f C_f]}{R_f C_f} s + \frac{A_0+1}{R_f C_f \tau_a}} \tag{4.12}$$

The settling time of the resistive TIA, therefore, can be calculated as:

$$T_s = \frac{8}{\frac{1}{R_f C_f} + \underbrace{\omega_a(1+A_0)}_{\text{OP-AMP GBP}}} \approx 8 R_f C_f \tag{4.13}$$

The advantage of including sensor decoupling amplifier in the LNTIA becomes clear when this settling time is compared with that of a conventional TIA, which was calculated in Equation 3.12 as $T_s = \frac{8}{W_a}$. Interestingly, the settling time of the decoupled TIA can be controlled by its feedback network rather than its core amplifier, provided that the op-amp gain-bandwidth product is sufficiently small. This effectively means that the op-amp can be designed independently of the rest of the LNTIA circuit and photodiode. Alternatively, by choosing the op-amp gain-bandwidth product to be much larger than $\frac{1}{R_f C_f}$,

the designer can make the loop settling time independent of the R_f and C_f values. This gives the designer the freedom to program the R_f value, for gain control, without altering the loop settling time.

The LNTIA architecture depicted in Figure 4.1 is comprised of two cascade stages, the CA and the resistive TIA. Each of these blocks has a settling time which can be calculated separately. The CA is a open-loop amplifier the settling time of which can be calculated by knowing the frequency of its dominant pole, (see Equation 4.8 and 4.9). The LNTIA settling time, therefore, can be defined as:

$$T_{s,LNTIA} = MAX[8R_fC_f, \frac{5I_D}{V_TC_D}] \tag{4.14}$$

4.5 LNTIA: Noise Analysis

The analysis in this chapter so far has shown that adding a decoupling CA enhances the feedback loop stability by converting the RTIA open-loop transfer function from a two-pole / one-zero to a single-pole system that is unconditionally stable. Moreover, the sensor decoupling makes the settling time independent of the op-amp bandwidth. In this section, the noise performance of this proposed design is investigated.

The input-referred noise current spectrum of the proposed LNTIA, can be calculated using Equation 4.15:

$$i_{n,in}^2 = i_{n,in_{CA}}^2 + \frac{i_{n,in_{RTIA}}^2}{A_i^2} \tag{4.15}$$

where $i_{n,in_{CA}}^2$ and $i_{n,in_{RTIA}}^2$ denotes the input-referred noise current of the CA and resistive TIA, respectively, and A_i is the CA current gain calculated in Equation 4.5. This equation suggests that the noise contribution of the RTIA to the overall input-referred noise current of the LNTIA can be minimised by selecting a moderate gain for the CA. Interestingly, the addition of the CA also significantly reduces the noise contribution of the feedback and bias op-amp by decoupling the photodiode output capacitance from the RTIA feedback loop.

The contribution of the feedback op-amp noise to the overall input-referred integrated noise current of the RTIA has been calculated in Equation 3.23. This equation can be modified to model the situation when a CA is inserted between the RTIA input and the photodiode output, by replacing the CD with $C_{gd_4} + C_{gd_3} \ll C_f$. This substantially reduces the magnitude of the $(C_D + C_f)^2\omega^2$ component in Equation 3.23, and hence the total input-referred integrated noise of the resistive TIA.

A Cadence noise simulation is presented later in this section (Table 4.5) which confirms that, due to the CA current gain, the contribution of the RTIA noise to the overall input referred current noise is negligible compared to that of the CA. In fact, the CA is the dominant noise contributor, even for a CA gain as small as A_i=5.

The key factor in our noise analysis is therefore a calculation of the input-referred noise current of the CA. The first stage of this calculation is to identify

the sources which make little or no contribution to the overall noise. It is possible to deduce from a consideration of the CA circuit topology shown in Figure 4.2 that the noise of the bias circuitry and M5-8 are cancelled at the CA output. This is because any noise current generated by the M5-8 devices is amplified by M_1-M_2 and M_3-M_4 current mirrors with the same gain but different polarities. These noise current are combined in the CA output and cancel each other. Complete mutual cancellation only occurs when the mirror devices are perfectly matched. In practice, since this cannot be guaranteed, some residual M_{5-8} noise current is expected. Nevertheless, this will be significantly smaller than that due to the M_{1-4} devices.

This theoretical deduction of noise cancellation is confirmed by the noise simulation reported later in this chapter, and is another advantage of the novel LNTIA topology proposed. In addition, unlike the conventional RTIA discussed in Chapter 3, the regulator circuit responsible for the generation of the photodiode bias voltage, makes a very insignificant contribution to the overall input-referred noise. This simplifies the design of the regulator circuit and reduces the power and area consumption considerably.

$$\begin{aligned} i_{n-CA}^2 = & \frac{8}{3}KT\gamma(gm_{M1}+gm_{M3}) + \frac{8}{3}KT\gamma(gm_{M2}+gm_{M4}) \times \frac{1}{A_i^2} \\ & + \frac{K_p}{C_{ox}f(WL)_{M1}}gm_{M1}^2 + \frac{K_p}{C_{ox}f(WL)_{M2}}gm_{M2}^2 \times \frac{1}{A_i^2} \\ & + \frac{K_n}{C_{ox}f(WL)_{M3}}gm_{M3}^2 + \frac{K_n}{C_{ox}f(WL)_{M4}}gm_{M4}^2 \times \frac{1}{A_i^2} \end{aligned} \tag{4.16}$$

The overall input-referred noise current spectrum of the CA is given by Equation 4.16. Equation 4.14 can be simplified by factoring in the current mirroring of M_1-M_2 and M_3-M_4, i.e. $(WL)_{M2} = A_i \times (WL)_{M1}$ and $(WL)_{M3} = A_i \times (WL)_{M4}$. The gm coefficients can be calculated as $gm_{M2} = A_i \times gm_{M1}$ and $gm_{M4} = A_i \times gm_{M3}$. By including these and setting A_i=5, Equation 4.16 can be rewritten as:

$$\begin{aligned} i^2_{n-CA} &= 1.2 \times \frac{8}{3} KT\gamma(gm_{M1} + gm_{M3}) + 1.2 \times \frac{K_n}{C_{ox} f (WL)_{M3}} gm^2_{M3} \\ &+ 1.2 \times \frac{K_p}{C_{ox} f (WL)_{M1}} gm^2_{M1} \end{aligned} \tag{4.17}$$

4.6 Simulation results

The design specifications for the proposed LNTIA that have been derived above by theoretical analysis have been assessed using simulation tools provided by the Cadence Design Framework using the AMS 350 nm Technology Process Design Kit. This section reports the results of this modelling exercise.

The specifications considered include: settling time, input referred noise, power consumption and DC offset. These were combined into the following figure of merit (FOM):

$$F.O.M = \frac{1}{I_{n,rms} I_{total}} \tag{4.18}$$

Where $I_{n,rms}$ denotes the total input-referred noise of the TIA and I_{total} represents the total static current sinked form the power supply. This FOM was calculated for both the proposed LNTIA and conventional TIA topologies, using various simulations, to provide a quantitative comparison between the performance of the LNTIA and the conventional TIA, explained in chapter 3.

The components in the electrical model of the photodiode must be defined for the simulation, because, as explained earlier, the size of the PD output capacitor limits the bandwidth and affects the noise performance of the TIA. It might be thought that the same capacitance should be used for both the proposed and conventional architectures in order to make the comparison fair. However, as explained in Chapter 2, the PD output capacitance is inversely proportional to the PD bias voltage, so the extra bias voltage provided by the proposed LNTIA should be factored into the simulation. This was done by reducing the C_D value using Equations 2.1 and 2.2. The appropriate ratio of PD output capacitance for the conventional and proposed TIA can thus be calculated as :

$$\frac{C_{D,LNTIA}}{C_{D,TIA}} = \frac{\sqrt{V_A + V_{bi,TIA}}}{\sqrt{V_A + V_{bi,LNTIA}}} \tag{4.19}$$

where, $V_{bias,TIA}$ and $V_{bias,LNTIA}$ denote the PD bias voltage supplied by the conventional TIA and the novel LNTIA, respectively. Thus if we consider, for example, a case where $V_{bias,TIA}$= 1V, $V_{bias,LNTIA}$ = 2V and V_A = 0.4V, then the $C_{D,TIA}$-to-$C_{D,LNTIA}$ ratio used in the simulation test-bench should be 1.3.

The DC level of the photocurrent (I_{PD}) affects gm_{M1} and gm_{M3} values, especially when the CA is operating in class AB mode, so it too must be specified. For the simulation presented in this section it is set at 1 μA.

Table 4.2 lists the dimensions of the CA transistors and the sizes of the PD output capacitance used.

Device	type	dimension/size	Device	type	dimension/size
M_1	PMOS	$20\mu/10\mu$	M_5	NMOS	$400\mu/0.5\mu$
M_2	PMOS	$100\mu/10\mu$	M_6	NMOS	$400\mu/0.5\mu$
M_3	NMOS	$20\mu/10\mu$	M_7	PMOS	$400\mu/0.5\mu$
M_4	NMOS	$100\mu/10\mu$	M_8	PMOS	$400\mu/0.5\mu$
C_D	CAP	3.8 nF	R_D	RES	inf

Table 4.2: CA device size/dimensions used for the simulation presented in this section.

Two DC voltages are involved in the biasing of the LNTIA: $V_{CA,bias}$ and $V_{OPAMP,bias}$. An LDO regulator feedback loop with two resistive voltage dividers can be used to generate these (as shown in Figure 4.3).

An important advantage of conducting the simulation with actual regulators rather than ideal voltage sources, is that it is possible to verify the extent of the noise cancellation provided by the proposed LNTIA.

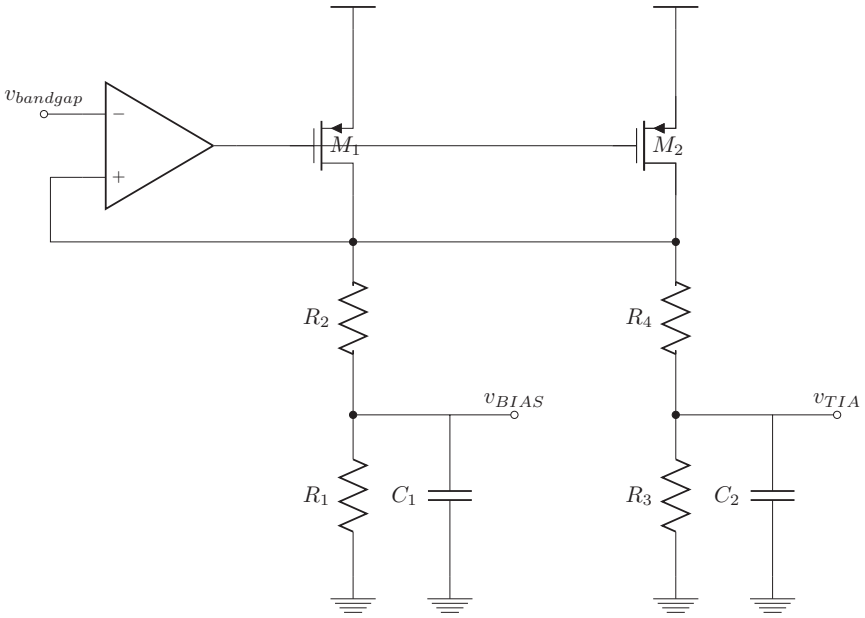


Figure 4.3: A possible LDO regulator circuit to generate $V_{CA,bias}$ and V_{OPAMP_bias} required to bias the photodiode and TIA, respectively, in the LNTIA circuit depicted in Figure 4.1

As discussed in Chapter 3, the second stage of the LNTIA developed for this study consists of an op-amp and a feedback resistor. The two-stage Miller op-amp with PMOS input pair that was used to represent a conventional TIA in Chapter 3 was also used as the LNTIA feedback op-amp in the Cadence simulation in order to provide a fair comparison between the two topologies [see Figure 4.4].

The theoretical analysis, presented earlier suggests that neither the bandwidth nor the noise performance of the feedback op-amp significantly affects the

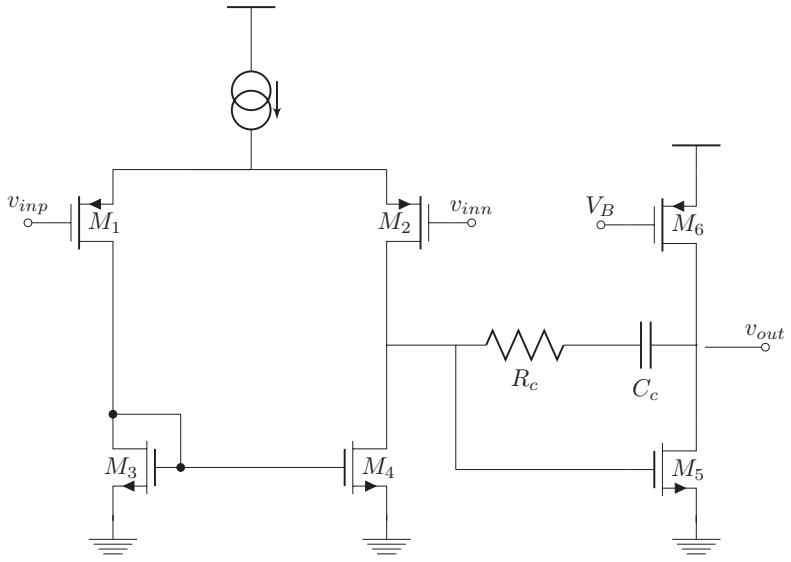


Figure 4.4: Two stage Miller op-amp used as the feedback op-amp in the second stage of LNTIA.

performance of our proposed LNTIA, so the magnitude of its first and second stage bias currents were reduced by a factor of 70. This significantly reduces the overall power consumption of the AFE. In addition, since the phase margin of the feedback loop is no longer affected by the size of the feedback resistor, programmable gain was added to the capability of our LNTIA by making the feedback resistor adjustable. Table 4.3 specifies the device dimension used in the LNTIA second stage, the resistive TIA.

4.6.1 DC Simulation Results

As explained earlier in this chapter, the CA uses a TL loop to maintain the required V_{bias}, generated by a regulator, across the photodiode. Translinear

Device	type	dimension/size	location
$M_{1,2}$	PMOS	$400\mu/1\mu$	input diff pair
$M_{3,4}$	NMOS	$40\mu/8\mu$	active load
C_c	NMOS	9 pF	compensation
R_f	RES	200 Ω	compensation
C_D	CAP	3.8 nF	Photodiode
$Ibias_1$	CUR	500 nA	First stage bias
$Ibias_2$	CUR	8 μA	Second stage bias

Table 4.3: Specifications of LNTIA second stage components used in the noise simulation presented in this chapter.

principles usually assume perfect matching between the transistors forming such a loop. This assumption, however, might not hold in our device due to chance mismatches between the transistors used. To deal with this uncertainty, the Monte Carlo (MC) analysis provided by the Cadence Design Frame was used to model the voltage variations that would occur across the photodiode electrical model due to such a mismatch. The result of this MC analysis is shown in Figure 4.5 and confirms that the CA architecture is capable of maintaining a relatively constant voltage across the photodiode.

A mismatch between the M_1-M_2 and M_3-M_4 transistors (which respectively form the PMOS and NMOS 1-to-5 current mirrors in the CA) would mean that $ID_{M2} \neq ID_{M4}$ in the absence of input current. As a result, a portion of the CA's I_{bias} could bleed into the RTIA stage, thus generating a DC offset voltage at the output of the LNTIA. The op-amp also generate an offset voltage at the output of the LNTIA mainly due to the mismatch between its input-pair transistors and also between its load transistors.

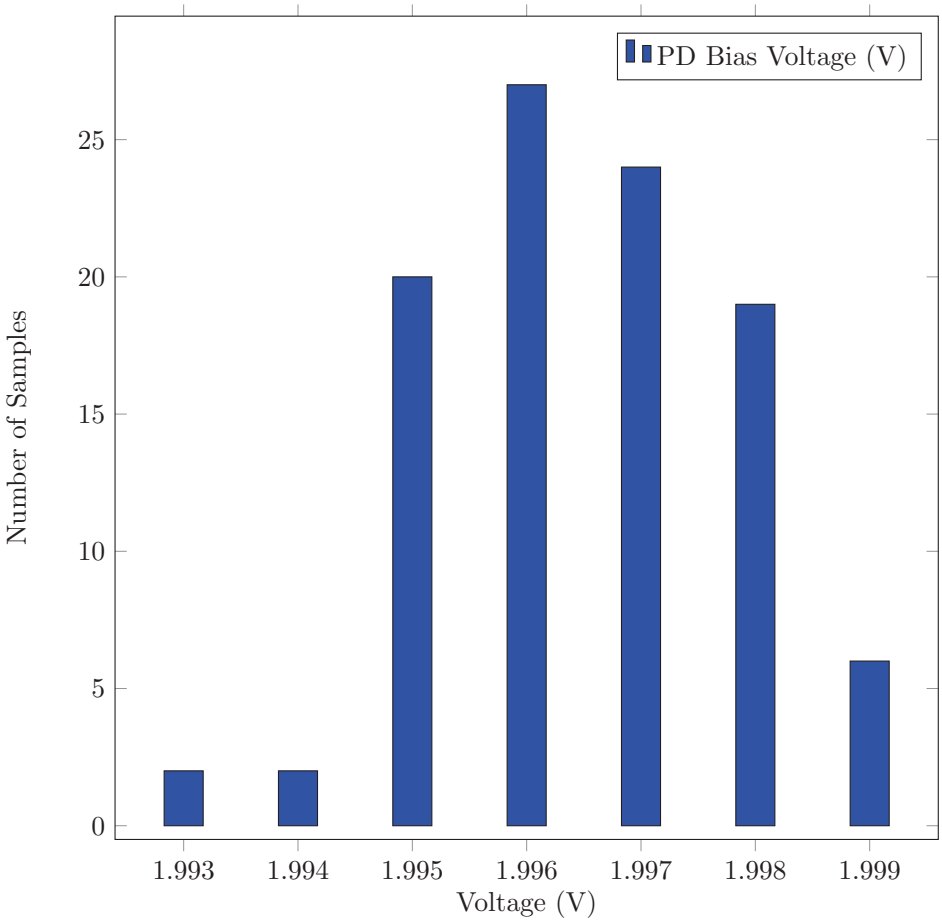


Figure 4.5: PD bias voltage provided by the CA, reported for 100 MC samples, the DC voltage at the positive terminal CA is 2V.

As explained in Chapter 1, since the DC level of the PPG signal is used in the blood oxygen level calculations, any DC offset added to the LNTIA output voltage should be considered as an error in the oxygen measurement. To reduce the risk of this, a correlated dual sampling (CDS) block that can remove most of any such DC offset from the output voltage waveform is incorporated in the post processing unit (see Chapter 5). Nevertheless, if the DC offset were large

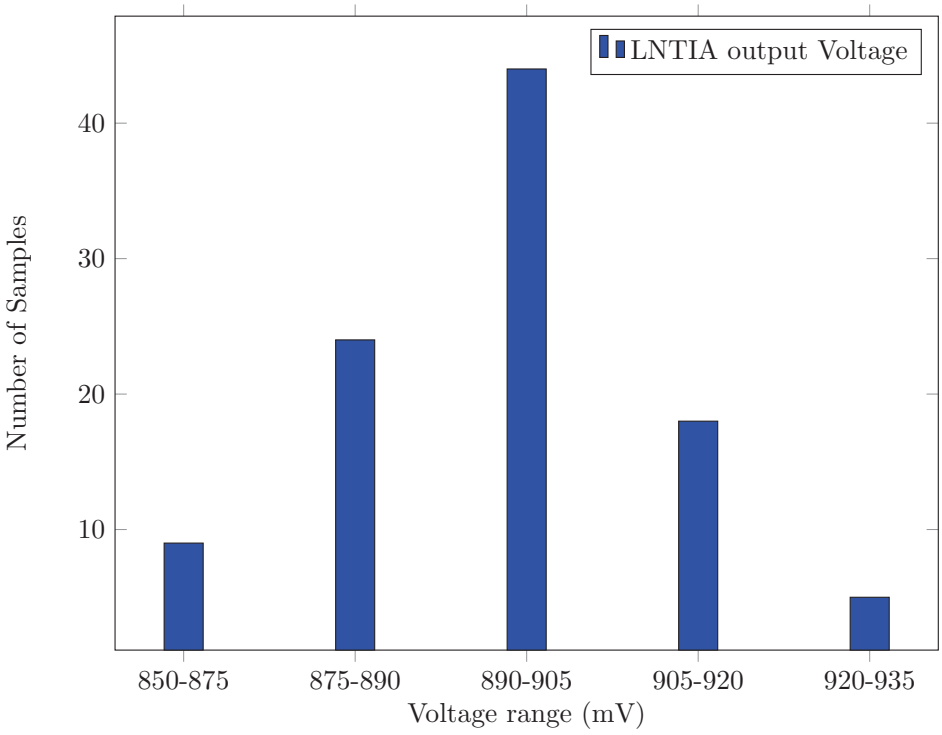


Figure 4.6: LNTIA output DC voltage reported for 100 MC samples where the input DC current is 2 μA, RTIA Transimpedance gain is 500 kΩ and the DC voltage at the positive terminal of the feedback op-amp is 2 V.

enough to saturate the LNTIA output, the CDS would not be able to recover the signal. To address this potential weakness in the design, Cadence MC analysis was used to assess the vulnerability of the proposed LNTIA topology to the DC offset problem. The output DC voltage for 100 MC samples was simulated [see Figure 4.6].

The MC results presented in Figure 4.6 show that, although the LNTIA output voltage could vary significantly due to transistor mismatch, the LNTIA would still operate without output saturation.

Cadence DC analysis can also be used to simulate the power consumption of each block in LNTIA and typical TIA topology. Table 4.4 lists the power consumption of each block in the proposed LNTIA circuit and compares it with that of its counterpart in a conventional TIA topology. This confirms that the overall power consumption of LNTIA is indeed significantly lower than that of the typical TIA.

Block	Typical TIA	LNTIA
Feedback Op-Amp	735 μW	35 μW
LDO Regulator	280 μW	200 μW
CA	NA	25 μW
Totall	1.015 mW	260 μW

Table 4.4: The power consumption of the sub-blocks in each topology when both provide an approximately equal settling time.

4.6.2 Noise Simulation Results

Cadence Noise simulation was used to identify the devices contributing most to the overall input referred integrated noise current of the LNTIA circuit proposed throughout this chapter. The device dimensions listed in Table 4.2 and 4.3, corresponding to a CA gain of 5, were used for the simulation. The photocurrent DC level was also included in the noise simulation by the insertion of a DC current source sinking 1 or 2 μA from the input transistor of the current amplifier, LNTIA first stage.

The result of the noise simulation is reported in Table 4.5, and confirms that most of the input noise current is generated by the CA transistors. Thus, the noise performance of the regulator and feedback op-amp are not affecting the noise performance of the proposed LNTIA, and their power consumption could be reduced without any significant adverse effect on the measurement SNR.

Device	Type	Noise Contribution	% of total
M_3(CA)	Thermal	3.8e-10 A^2	15.2
M_1(CA)	Thermal	3.3e-10 A^2	13.3
M_3(CA)	Flicker	2.8e-10 A^2	11.2
LDO	Thermal	2.14e-10 A^2	9
R_1(LDO)	Thermal	1.2e-10 A^2	8
LDO	Flicker	9e-11 A^2	4
CA (other)	Mix	NA	40

Table 4.5: The main noise contributors to the LNTIA overall integrated output noise current across the 0.1 Hz to 3 kHz band.

The simulated LNTIA input-referred noise current PSD plotted in Figure 4.7 confirms that, as anticipated in our earlier theoretical analysis, the photodiode decoupling provided by the CA leads to a flat PSD. A flat noise PSD within the working bandwidth is particularly advantageous when the duty-cycle of the photocurrent is small.

The simulation does, however, reveal an exception to this flat PSD. Figure 4.7 indicates that, for photodiodes with larger output capacitance, the noise PSD increases at higher frequencies. This was not included in our earlier theoretical discussion, and requires clarification.

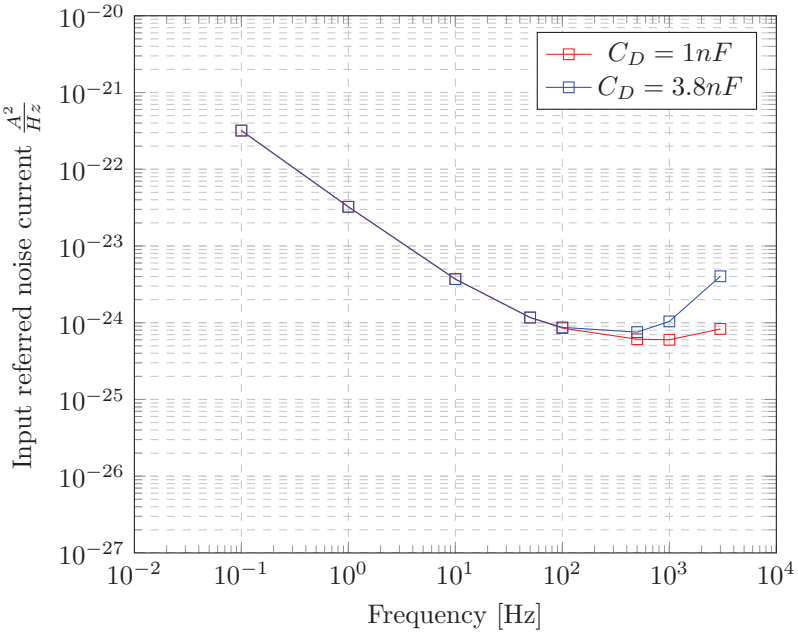


Figure 4.7: LNTIA input-referred noise current for two different photodiode output capacitance values. Simulation result obtained using Cadence noise simulation.

As explained earlier in this chapter, the regulator noise cancellation provided by our proposed CA topology, relies on the PMOS M_1-M_2 and NMOS M_3-M_4 current mirrors replicating the $M_5 - M_6$ drain current noise into the output branch but with an opposite polarity. At low frequencies, this cancellation is completely successful, so all the M5,M6 and bias circuit noise is removed from the CA output current. However, at higher frequencies the photodiode output impedance ($\frac{1}{C_D\omega}$) becomes comparable to $\frac{1}{gm_5}$ and $\frac{1}{gm_6}$. As a result, a portion

of the bias and regulator noise currents at the drain of M5-6 transistors also flows into the CA input. This adversly affect the noise cancellation, since the M5 and M6 noise current is no longer perfectly copied by the PMOS / NMOS mirror and this causes the observed noise peaking at high frequency in Figure 4.7.

4.6.3 Overall simulated performance comparison

The above simulation results can be used to compare the overall performance of our proposed LNTIA with that of a conventional resistive TIA. A quantitative comparison of the efficiency of each topology can be made by calculating the FOM, as formulated in Equation 4.16, in each case (see Table 4.6 below)

Architecture	Power	Int Noise(0.1-3KHz)	FOM
RTIA	1.015 mW	5 e-11 A	2e13
LNTIA	260 μW	8 e-11 A	4.8e13

Table 4.6: LNTIA vs Resistive TIA FOM calculated using simulation result obtained.

4.7 Conclusion

This chapter has investigated the effect of decoupling the photodiode from the negative-feedback loop of our proposed TIA by inserting a current amplifier

(CA). The performance of this novel LNTIA has been compared with that of the conventional RTIA studied in the previous chapter.

A summary of the advantages that have been identified for our proposed system is provided below:

1. Unlike a conventional RTIA, the settling time of our proposed LNTIA does not depend on the feedback op-amp bandwidth.

2. In the first stage of our proposed LNTIA, the current amplifier (CA) gain minimises the contribution of the feedback op-amp and LDO regulator to the overall input referred noise current, which means the power consumption of these components can be dramatically reduced.

3. Unlike a conventional TIA, the feedback loop phase margin of our LNTIA does not depend on the size of the feedback resistor, so programmable gain can be incorporated, which compensates for resistor size variation across the process corners.

4. The PD bias voltage provided by our LNTIA does not limit the output voltage, which permits larger PD bias voltages to be used than in a conventional TIA. This in turn leads to smaller PD output capacitance, which further improves the FOM of our proposed LNTIA.

It is clear from both our theoretical analysis and the simulation results that the novel LNTIA design we have proposed significantly outperforms a conventional TIA. The next chapter discusses the post-processing and LED calibrator

blocks, which further enhance the performance and reduce the power dissipation of the Pulse oximetry AFE.

Chapter 5

PO Frontend: Post Processing and LED light Calibration

This chapter describes the post processing blocks following the LNTIA in our proposed PO frontend chain.

- A number of studies have reported that the PPG signal DC level can vary significantly due to variation in the optical properties of the patients skin [59] and motion artifacts [60, 61]. This can lead to a saturated front-end output and impaired measurement. In our proposed system, an active LED light intensity calibrator is, therefore, designed and added to the PO analog frontend. The calibrator tracks the DC level of the PPG signal and adjusts the light emitted by the LED accordingly. A novel calibration algorithm has been developed and implemented with digital circuits for this calibrator, described later in this chapter.

- Since the LNTIA is an LTI system, the frequency profile of its output signal is similar to that of the photocurrent, and occupies a relatively large bandwidth. As explained in chapter 2, for a specific sampling frequency, the oversampling ratio provided by the ADC following the PO front-end is determined by the input signal Nyquist frequency. As explained in chapter 2, larger oversampling ratios leads to larger ADC effective number of bits(ENOB). Therefore, it is crucial to limit the output signal bandwidth. A track-and-hold circuit added to the post processing, which reduces the effective bandwidth of the output square-wave by increasing its duty cycle to almost 100 %.

- As the Monte Carlo results presented in chapter 4 has shown, in converting the square-wave modulated photocurrent to a square-wave modulated voltage, the LNTIA can introduce a DC offset error due to mismatch between its transistors. A correlated dual sampler is embedded in the post-processing block proposed in this chapter, which is capable of removing the LNTIA offset.

- PPG signal AC-to-DC ratio, also known as the contrast, is reported in other studies to be between 0.5 and 5 % [62]. A contrast enhancer amplifier is, therefore, designed and implemented as the last block of the AFE chain to increase the signal contrast. Low contrast can significantly limit the dynamic range of the ADC following the PO front-end.

A diagram of the post-processing architecture is shown in Figure 5.1, where, at the first phase, the front-end DC offset is removed from the square-wave mod-

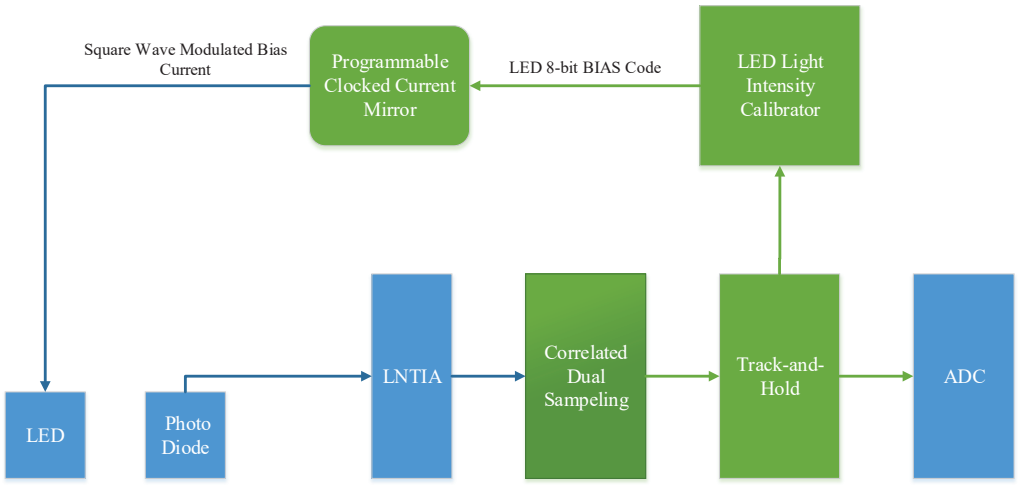


Figure 5.1: The block diagram representation of the proposed post-processioning and LED light calibration blocks, in green, embedded within the AFE chain.

ulated LNTIA output voltage using an active CDS block followed by a track-and-hold circuit, which effectively increases the duty cycle of the square-wave to almost 100%, and since the effective bandwidth of a square-wave is determined by its duty cycle [see Chapter 2], the effect is to reduce the bandwidth of the signal as required. At the end of the this phase, the amplitude modulated square wave discrete-in-time PPG signal is converted to a continuous-in-time signal with a very small contrast. The LED light calibrator, then, compares the DC level of the continuous-in-time signal with its predefined threshold voltages and adjust the LED bias current magnitude accordingly, in a real time fashion. This can be considered as the second phase of the post processing. At the final phase, the contrast enhancement amplifier increases the AC component of the signal while keeping its DC component constant. Throughout the rest of this

chapter, each of these phases are explained extensively.

5.1 DC offset removal

The CDS circuit, shown in Figure 5.2, samples the LNTIA output voltage in the absence of any PPG signal and stores it as electric charge on a capacitor (C1) using a CMOS transmission gate controlled by a clock signal (Q1). This represents the sum of all the unwanted DC voltages, namely the photodiode dark-current voltage, the LNTIA and regulator offset (as explained in Chapter 4). The LNTIA output voltage is then sampled again in the presence of the PPG signal and stored on another capacitor (C2) during Q2. In the final phase, (Q3), the charges stored on C1 and C2 are combined with opposite polarities and stored on C3. The voltage across C3 represents the uncorrupted PPG signal, with all the unwanted DC removed. Equation 5.1 gives the CDS input-output time domain relationship.

$$C_3 v_{out} = C_2 v_{in}(t - T1) - C_1 v_{in}(t - T2) \tag{5.1}$$

Equation 5.1 can be further simplified by including $C_1 = C_2 = C_3$, $V_{in}(t - T2) = V_{offset}$ and $V_{in}(t - T1) = V_{offset} + V_{LNTIA,out}$ into the calculation, which leads to:

$$V_{out} = V_{cm} + \frac{C_1}{C_3} \times V_{LNTIA,out} \tag{5.2}$$

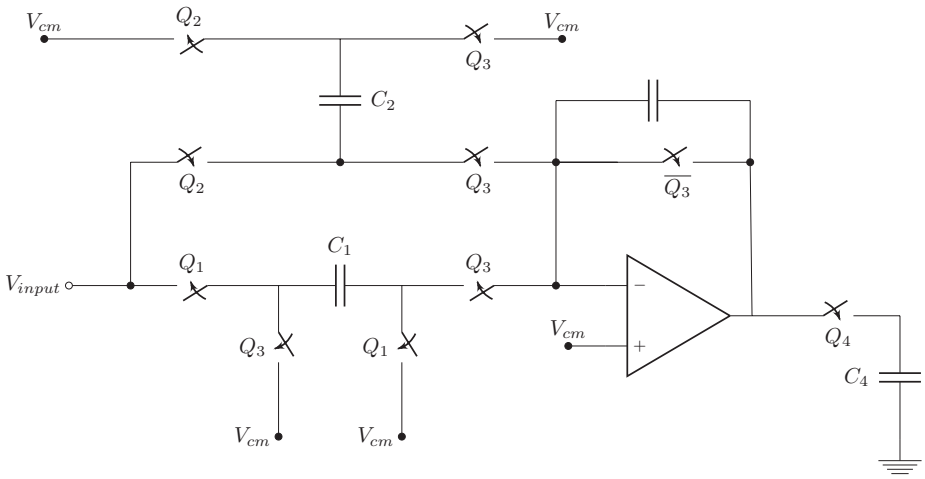


Figure 5.2: Circuit level implementation of the CDS block, followed by a track-and-hold circuit, implemented by Q4 switch and C4 capacitor.

The timing of the clock signals used in the CDS and the track-and-hold circuit is shown in Figure 5.3. The clock signals are also buffered in such a way that the charge injection error of the Q1 and Q2 switches are input independent. For instant the Q1 switch, connected to the input of the CDS block, must be switched slightly after the Q1 switch connected to the V_{cm}. The amplitude of the generated charge injection is also minimised by using the minimum size CMOS complementary switches.The PMOS and NMOS transistors in the CMOS switches are connected in an anti-parallel fashion to cancel a portion of each others charge injection[63].

The only switch that generates signal-dependent charge injection is Q4. The non-linearity caused by this switch can be suppressed by using a large C4 capacitance. The leakage from the large C4 capacitor could also deplete the

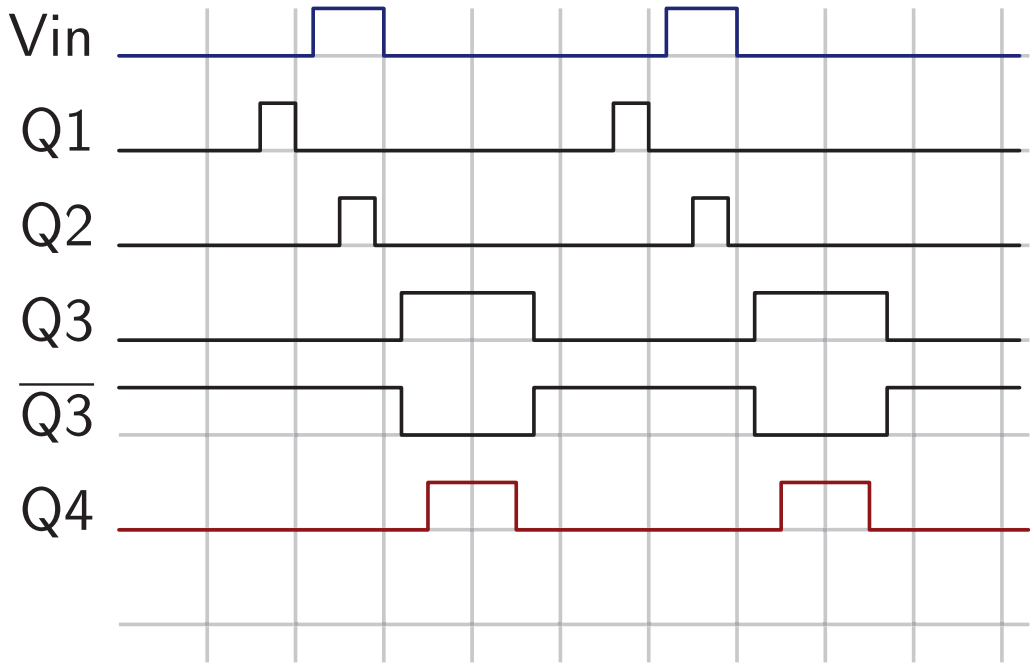


Figure 5.3: The timing diagram of the CDS circuit clock signals (in black) and its square wave-modulated input signal.

stored charge, leading to a systematic DC error. However, leakage from the poly capacitors used in this design, even when these are large in size, is comparatively small.

The T/H circuit designed for this study, must remain stable during the time that the op-amp feedback CMOS switch is closed (when Q3 is low). During this time, the op-amp is in a unity negative feedback loop, which is the worst case for the stability. Therefore, the op-amp must be designed in a way, that the loop phase margin remains above 60 degree. This was achieved for this design by including the Miller compensation technique in the design of the op-amp.

5.2 LED Light Calibrator

The output DC level of the track-and-hold circuit is used as an indicator of the collected light strength. The LED light intensity calibrator is designed to keep this level between two threshold voltages. The calibration algorithm is depicted in Figure 5.4, which indicates that if front-end output DC level falls below the calibrator lower threshold ($V_{Th,Low}$) at any point during the measurement, the calibrator digital engine reacts by inserting a "1" into its output 10-bit-register at the next rising edge of the calibration clock signal. This causes a 10 % increase in the LED bias current magnitude. If this is sufficient to raise the output DC voltage to a level between the threshold voltages, then the comparator output goes from high to low, which disconnects the calibrator hardware from its clock signal to stop further calibration. On the other hand, if the output DC level is still below $V_{Th,Low}$, the digital engine inserts another "1" into the 10-bit-register at the next clock rising edge, and so on.

The reverse iteration occurs if the output DC level is larger than the higher threshold voltage ($V_{Th,High}$), i.e. a "1" is removed from the output digital 10-bit word at the next rising edge of the calibration clock.

By setting the output 10-bit digital word to "0000000000" at the start of a PO measurement, the front-end ensures that the calibration begins in the $V_{OUT} < V_{Th,Low}$ state. The engine then inserts "1's" into the digital output word until $V_{OUT} \geq V_{Th,Low}$. The engine then locks the output digital word and remains inactive as far as $V_{Th,Low} \leq V_{OUT} \leq V_{Th,High}$.

The Circuit level implementation of the LED light calibrator digital engine is

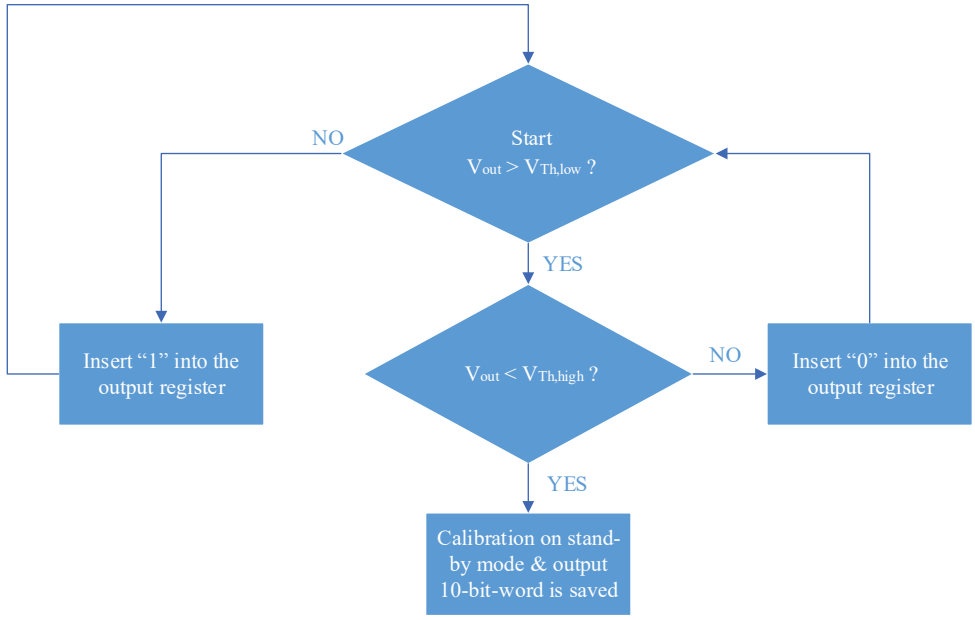


Figure 5.4: LED light intensity calibrator algorithm.

depicted in Figure 5.5, where two auxiliary shift registers are used to insert "1's" and "0's" into the output JK flip-flop array. These shift registers operates only at the rising edge of the calibration clock signal, the frequency and duty cycle of which is similar to that of the track-and-hold clock signal. This rising edge of the calibration clock signal occurs half a clock period later than that of the track-and-hold clock signal to let the output voltage settle.

The engine's output digital word is translated into an LED DC bias current by an programmable current mirror in which the overall aspect ratio is determined by the number of 1s in the 10-bit word. This digitally calibrated DC current

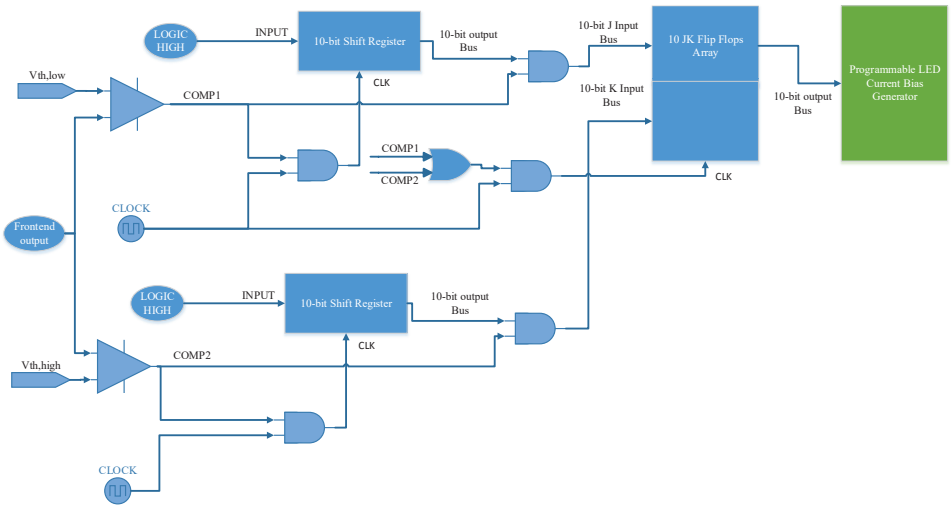


Figure 5.5: Circuit level implementation of the LED light calibrator digital engine.

is then modulated with a square-wave using the enable switch added to the reference branch of the current mirror (see Figure 5.6).

The calibration clock frequency is chosen to be the same as that of the LED square-wave modulated bias to maintain the stability of the calibration loop and ensure that the system has sufficient time to respond to the LED light adjustment.

An additional advantage of this calibration algorithm is that, by limiting the LED bias current change to 10 % per clock edge, the calibrator ensures that anomalous increases in the PPG signal due to patient-related artifacts can not severely disturb the calibration procedure.In other word, the engine does not react to changes.

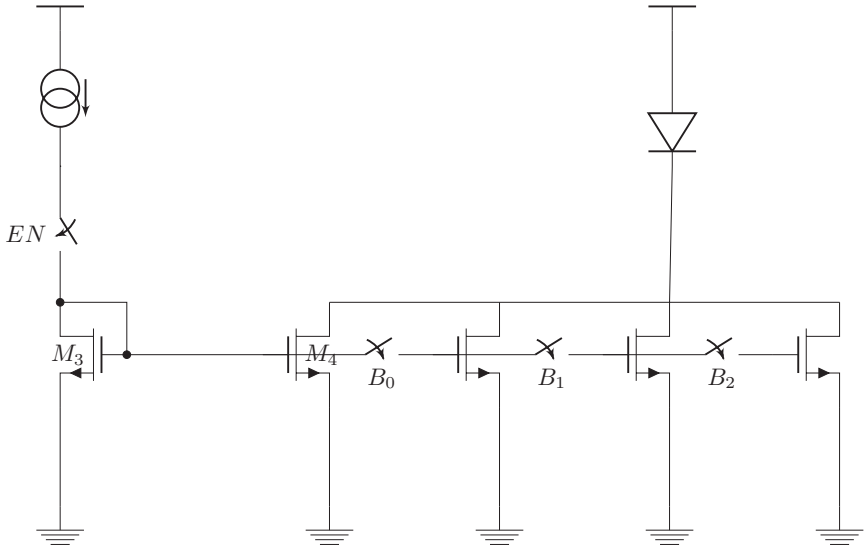


Figure 5.6: Programmable current mirror for converting the calibrators digital output word into a DC bias current, which can be square-wave modulated by connecting its enable (EN) switches to a clock signal. It should be noted each switch is comprised of two CMOS transmission gate with complimentary enable bits. The mirror transistors gates are either connected the reference diode-connected or connected to the ground. This ensures that the gates are always connected to a known voltage.

5.3 Contrast Enhancer Amplifier

Even though the effect of the ADC noise is minimised by ensuring that the bandwidth of the front-end output signal is small, the low contrast nature of the PPG signal means that the ADC following the PO front-end must provide a considerably large dynamic range to digitise the PPG signal with high reso-

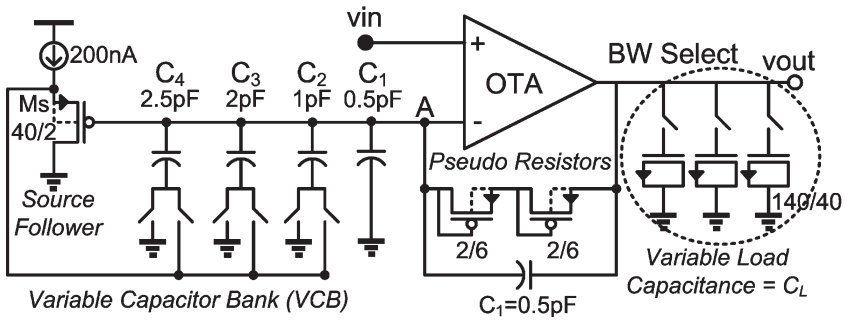


Figure 5.7: Contrast Enhancer Amplifier with the $A_{v,DC}$=1 and $A_{v,AC}$=1+$\frac{C_{in}}{C_f}$. Source [9].

lution. A contrast enhancement amplifier, which amplifies the AC component of the PPG signal while maintaining its DC component, is therefore included as the final block in the front-end chain. The circuit level implementation of the CEA block is shown in Figure 5.7, which was originally proposed in [9].

It can be proven mathematically that for frequencies lower than f_c=$\frac{1}{C_f R_f}$, the voltage gain of the CEA is unity, whereas for frequencies higher than f_c, it is $\frac{C_{in}}{C_f}$. The AC gain of the CEA can therefore be programmed by changing the C_{in} value, which is designed as a combination of a number of capacitors connected in parallel. Each capacitor, thus, can either be connected in parallel with other capacitors in the C_{in} capacitor bank or short circuited through the negative feedback loop provided by the auxiliary op-amp, added to minimise the leakage from the capacitors by equalising the DC voltage across the disconnected C_{in}. Therefore, the CEA architecture designed for this study

is the same as the one depicted in 5.7, with the difference that the source follower in 5.7 is replace with a op-amp buffer to minimise the leakage even further.

In the absence of this buffer, the leakage current generated by the disconnected C_{in} capacitors would flow into the pseudo-resistor, leading to a reduction in its resistivity and a consequent increase in the pole feedback frequency, which would impair the CDS functionality.

5.4 conclusion

The post processing block presented in this chapter uses a CDS circuit to remove DC errors from the amplified PPG signal. An additional track-and-hold circuit converts the square-wave modulated signal to a continuous-in-time base band signal with a very narrow bandwidth. Finally, an LED light calibrator is embedded in the post-processing block. This monitors the DC output level in real time and adjusts the LED forward bias current so that the output level always remains between two predefined threshold voltages.

The next chapter reports the performance of PO front-end microfabricated for this study on a silicon die in AMS 350 nm technology.

Chapter 6

Proposed Front-end Physical Implementation and Validation

Chapter 4 and 5 have described the architecture of a novel PPG recording channel compatible with modern photodiodes with large active area. This chapter reports the implementation of these blocks at transistor level and the verification of the circuitry using Cadence spectre simulator. The verification process involves the simulation of the circuit using a process design kit (PDK) provided by the AMS foundry for the 350 μm technology. This technology is relatively mature and the simulation model files used in its PDK have been updated multiple times. The simulations result, nevertheless, might not include the effect of all non-idealities and interference affecting the performance of the circuit when it is implemented on silicon. Therefore, the ultimate proof of concept would be to microfabricate the proposed PPG channel and validate its performance in the lab.

In this chapter, the implementation process (i.e. the layout) is described. The validation process developed to test the PPG channel microchip in the lab, is then explained. This process involves the implementation of the PPG acquisition system on a printed circuit board (PCB), which uses the PPG micro-chip as its sensor front-end. This system is then used to record PPG signal from the author finger tip presented later in this chapter.

6.1 Physical implementation of PPG acquisition front-end

The Cadence Layout Editor was used to draw the layout for PPG acquisition front-end. This was then streamed as a GDS file from which AMS foundry develops a number of optical masks to facilitate the microfabrication of the circuitry. The front-end top level layout is depicted in Figure 6.1. The inner-circuits are connected to the outside world through the IO pads placed in the form of a pad-ring around the chip. These pad rings are equipped with Electrostatic Discharge (ESD) protection circuitry depicted in Figure 6.2.

The pad ring shown consists of analog and digital half-rings separated by a blocker cell at each end. Each half ring has a separate supply and ground pad ring, which allows the isolation of analog and digital domains. These supply and ground connections must be connected first during the chip start-up to ensure that the ESD protection is activated prior to the main circuit power-up.

The isolation of the analog circuit protects the analog signals from digital

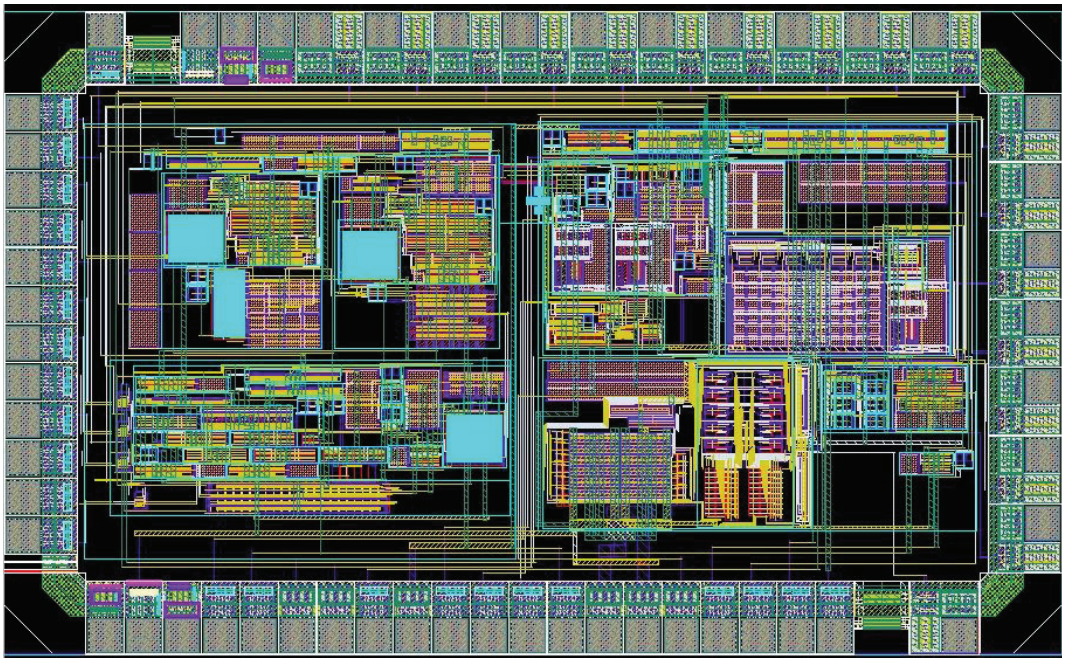


Figure 6.1: The PO front-end layout designed using Cadence Layout Editor for AMS 350 nm technology.

interference. However, since the digital and analog parts of the chip are still in the same conductive substrate, some digital noise can be seen at the bulk connection of the analog circuitry which can adversely affect the performance of the analog circuits. Therefore, the analog front-end was place within a guard ring which connects the substrate to a low noise ground connection. In addition, the sensitive analog circuits, i.e. the LNTIA, was located as far as possible from the digital pad ring and the LED digital calibration engine.

The frontend input signal is a relatively weak current generated by an array of photodiodes, which must travel form the input pad to the LNTIA input through a metal track. The metal resistance can add thermal noise to the input current. In addition, the metal track passes above the chip substrate

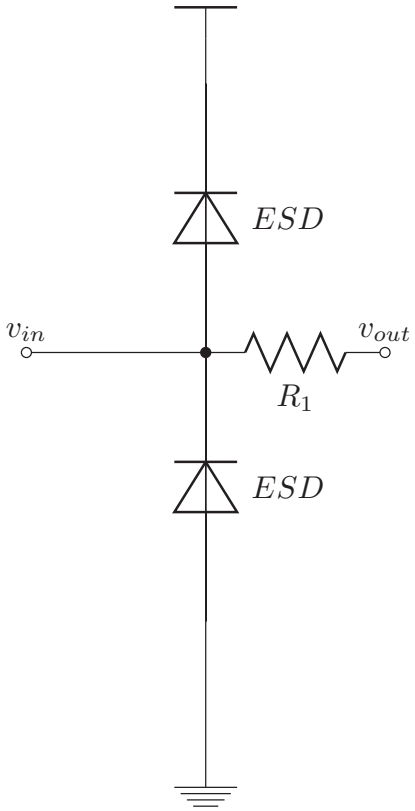


Figure 6.2: ESD protection circuitry used for IO pads. The reversed bias diodes ensures that when the magnitude of the terminal voltage exceeds the supply voltage by more than the diode threshold voltage, the pad will be shorted to either positive or negative supply. This structure protects the on-chip devices from experiencing large voltage. The resistor, on the other hand, protect the on-chip devices from large currents.

corrupted with the digital noise which can be coupled to the signal. The resistance of the metal, therefore, was decreased by using wide higher metals, such as metal three or four. This metal is then shielded from the substrate

by placing a wider rectangular lower level metal, such as metal one or two, connected to the low noise ground, underneath it .

The other source of noise corrupting the input current signal is the thermal noise generated by the ESD resistor. The value of this resistors was reduced to 50 Ω, the minimum value allowed by the foundry, to minimise its noise contribution.

6.2 Test bench design for PPG acquisition using the PO microchip validation

A test bench was designed and implemented using discrete components, such as an A field-programmable gate array (FPGA), voltage regulators and LED-PD opto pair, on a PCB, depicted in Figure 6.3 and 6.4. This provided a platform to validate the PO chip performance and recording a PPG signal.

An FPGA is coded and included on the PCB to provide the clock and enable signals required for the full functionality of the PO front-end. The FPGA device is configured with VHDL code that generates the non-overlapping clock signals required for the CDS, track-and-hold, LED calibrator engine and LNTIA gain. The FPGA also generates the "enable" and "power-down" signals required for the off-chip regulators. Since the on-chip ESD protection circuity and the front-end circuit are both supplied by off-chip regulators, the FPGA is coded in such a way that the former is powered-up and operational before the latter, which ensures the full ESD protection.

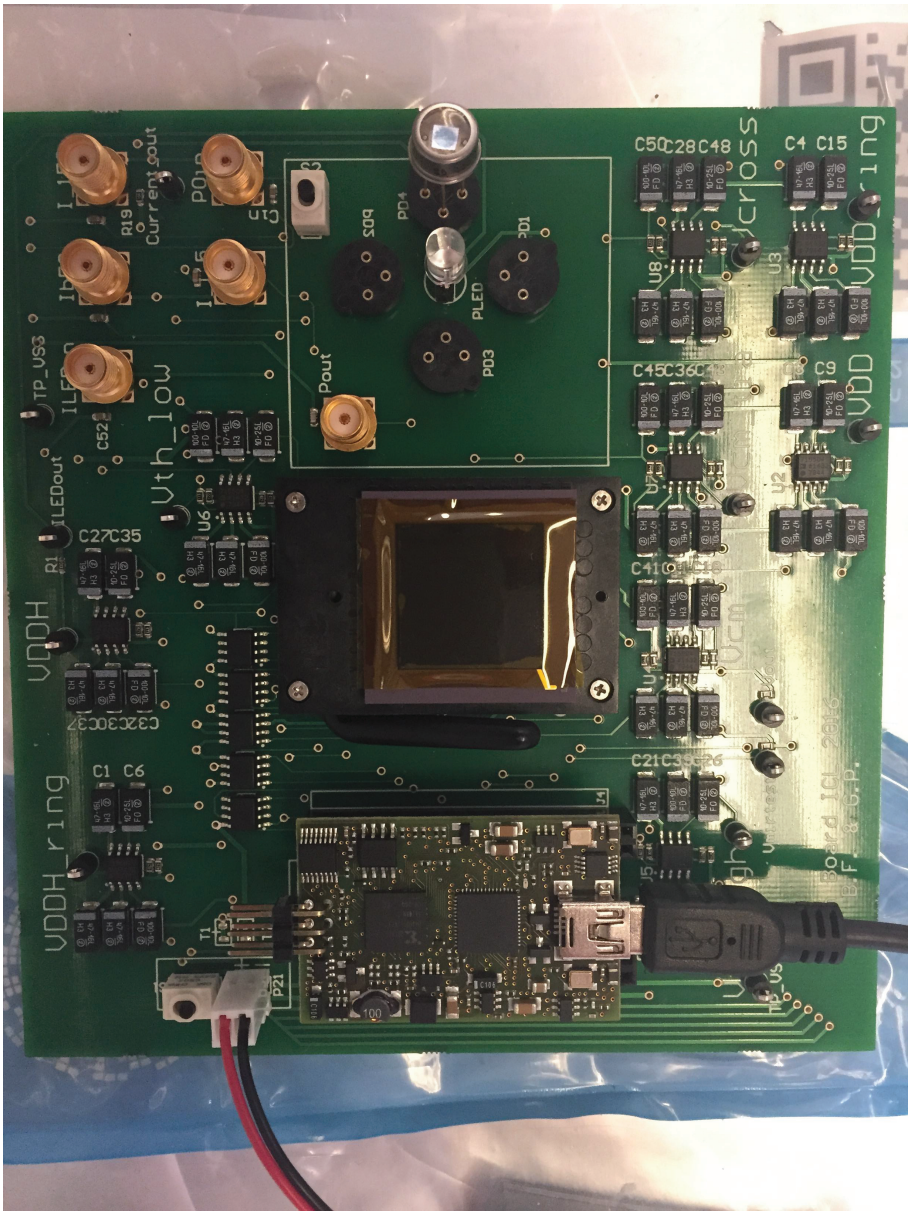


Figure 6.3: The PO test bench implemented on a PCB.

The PO front-end bias voltages are generated with off-chip regulators (ANALOG DEVICES ADM7155) whilst the bias currents are supplied using external stand-alone Keithley current sources. The regulator ICs utilise off-chip resistors to generate the voltages required for the front-end operation from a 4.5-volt electric battery. The output voltage of the regulator circuit shown in Figure 6.5 can be calculated as:

$$V_{out} = 1.2 \times \frac{R_1 + R_2}{R_2} \tag{6.1}$$

The size of C_{BYP} determines the integrated voltage noise at the output of the regulator, while C_{in}, C_{out} and C_{reg} are decoupling capacitors [64]. As mentioned earlier, in order to minimise the digital noise on the analog power supply, we used two regulators for analog supplies and two regulators of digital supplies. The digital and analog grounds are also connected to the negative terminal of the battery using a star connection in order to minimise the digital interference on the analog ground.

The PO chip output is connected to a stand-alone LabVIEW ADC via an SMA connector mounted on the test bench PCB. This 12-bit-ADC digitises the continuous-in-time PPG signal and saves the data in a format which is compatible with MATLAB. The sampling rate of the ADC was set at 100 K sample per second to provide sufficient oversampling ratio. The recorded data was, then, further filtered in MATLAB to enhanced its SNR by limiting the bandwidth of the recorded signal to 10 Hz.

The analog input of the chip is connected to four photodiode (Advanced Pho-

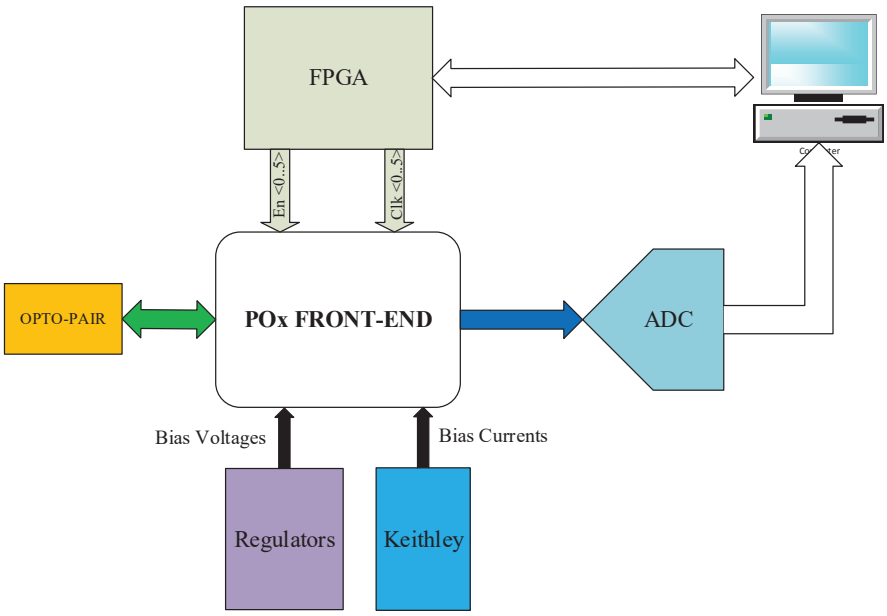


Figure 6.4: The block diagram representation of the PPG acquisition setup, which illustrates the interaction between the off-chip devices and the PO microchip.

tonix SD 100-11-21-221) placed symmetrically around a red LED (Marktech MTE5066S1J-UR), emitting a wavelength of 660 nm, a configuration that was suggested in Chapter 1 to maximize the reflected light absorption. The LED is forward-biased by a 100 Hz, square-wave modulated bias current provided by the PO chip, the magnitude of which is determined in a real-time fashion by an on-chip LED light intensity calibrator engine (as explained in Chapter 5).

The small signal characteristics of the proposed PO front-end, such as bandwidth, noise performance and average power consumption, are evaluated using an external Keithley current wave-generator capable of generating DC and AC

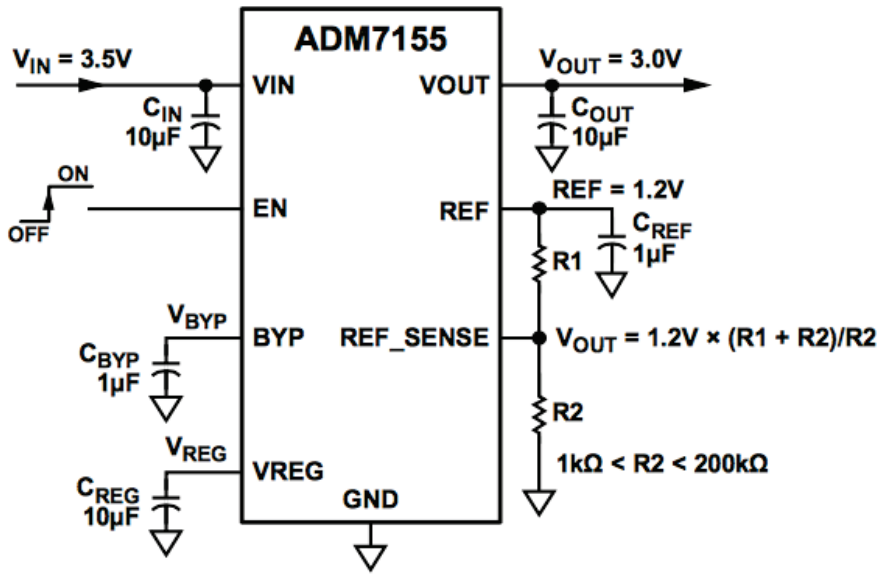


Figure 6.5: Manufacturer proposed architecture for biasing ADM7155 regulator. Source: Analog Devices ADM7155 data-sheet.

current simultaneously. This current was sunk from front-end analog input via an SMA connector. As explained in Chapter 4, the size of the PD output capacitance determines the bandwidth and total integrated noise of the the PO front-end. Therefore, in order to assess the chip performance fairly, the analog input was loaded with a 3 nF capacitor during the evaluation tests to mimic the PD output.

A mechanical switch capable of disconnecting the photodiode(s) from the front-end input was also added to the test PCB.

6.3 PPG acquisition using the PO micro-chip designed and microfabricated for this study

This section reports the use of the microfabricated system described above (see Figure 6.4) to record the PPG signal obtained from the author's index finger-tip (see Figure 6.6). This experimental evidence is presented as a proof of the functionality of the system.

As explained in the Introduction, modern PO devices require the simultaneous acquisition of PPG readings from two LEDs: red (R) and infra-red (IR). The novel front-end architecture reported here supported only a single LED, as this was sufficient to prove the functionality and performance of the design with minimum fabrication cost. However, it could be easily upgraded to a dual channel front-end by the addition of an extra LED light calibrator, a CDS-T/H block and a CEA (see Figure 6.7).

The LNTIA and CDS blocks could process both R and IR channels concurrently by using a time interleaving arrangement, with the CDS clock signals running at 200 Hz, instead of 100 Hz. However, since the T/H block converts the signal from square-wave modulated to continuous-in-time, the T/H and all the blocks following it, including CEA and ADC, would have to be duplicated to process R and IR channels simultaneously.

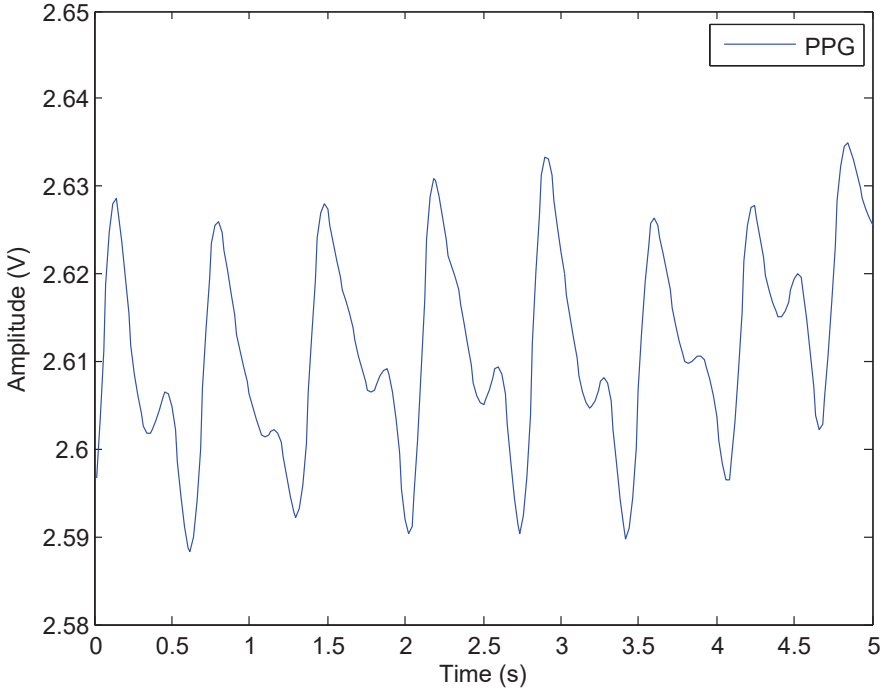


Figure 6.6: The filtered PPG signal recorded from the author fingertip using the PPG acquisition setup depicted in Figure 6.3. (LED square wave modulated current frequency = 100 Hz; duty cycle = 5%; amplitude = 12 mA LNTIA overall transimpedance gain=1.1 MΩ; CEA AC gain = 28 dB)

6.4 Validation of the PPG front-end and chip performance

This section reports the measurement of the performance and power consumption of the PO front-end crucial sub-blocks using the data collected in the lab. These measurements permit the quantitative comparison between this design

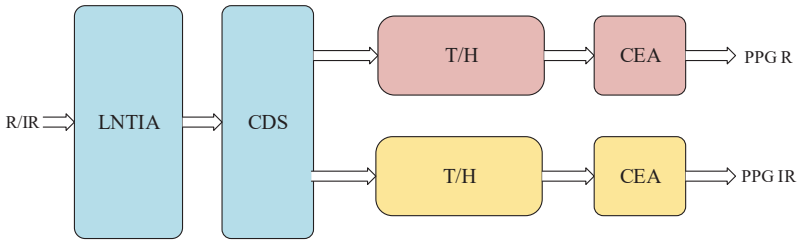


Figure 6.7: Additional blocks required to upgrade the proposed PO front-end to operate with two LEDs (red and infra-red) simultaneously.

and other state-of-the-art PO architecture. The signal at the output of each sub-block in the front-end chain was measured separately using an analog multiplexer added to the design on-chip. This multiplexer receives a 3-bit digital word from the FPGA and connects each of the eight crucial voltages, including the sub-block outputs, to the output pad via an analog buffer.

6.4.1 LNTIA transfer function

The transfer function of the LNTIA was calculated from multiple single-tone experiments using a Keithley current wave-generator. In each experiment, the current generator sinks a sine-wave current with a certain frequency and a DC offset form input of the PPG front-end. The voltage amplitude at the output of the LNTIA was then measured for each frequency. The amplitude of the input current sin-wave was set at 10 nA for all frequencies while the DC component

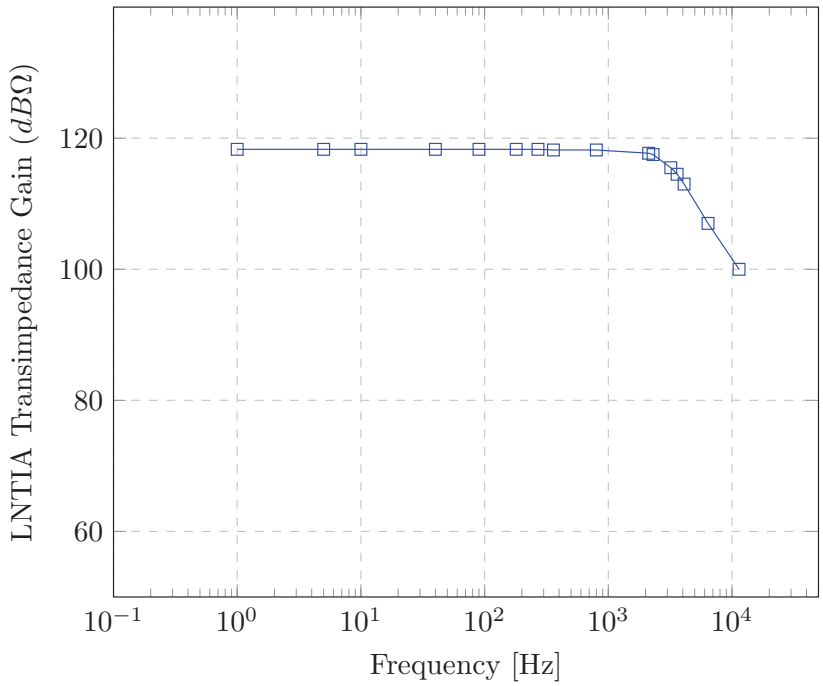


Figure 6.8: The LNTIA transfer function calculated by applying multiple sine-wave currents at various frequencies to front-end analog input using Keithley current wave-generator and the output voltage amplitude is measured at the output of the LNTIA.

was 1 μA. During these experiments, the photodiodes were disconnected from the front-end analog input and a 3nF capacitor was connected instead via a mechanical switch on the PCB. This capacitor emulates the output capacitance of photodiodes and enable a fair assessment of the LNTIA bandwidth. Figure 6.8 shows the transfer function of the LNTIA (the input current frequencies are indicated with squares).

The LNTIA -3dB bandwidth was found to be 3.2 kHz. This allowed the output

of the LNTIA to fully settle even when the input square-wave modulated current duty cycle was as small as 3 to 5 %. If required, the bandwidth can be further extended by increasing the current amplifier bias current, (as explained in chapter 4), although this would also increase the thermal noise.

6.4.2 LNTIA step response

One of the main objectives of the sensor decoupling technique used in the proposed LNTIA is to enhance the stability of the system (See Chapter 4). In the experiment presented in this section, a step input current, in the form of a low frequency square-wave modulated current with 1 μs rise and fall time, was sunk from the analog input of the front-end using a Keithley current wave-generator.

The LNTIA step response wave-form was then recorded and depicted in Figure 6.9. During this test, the LNTIA gain was set to its minimum value, which results in the worst case scenario for the stability because of the proximity of the LNTIA op-amp dominant and non-dominant poles. The depicted step response confirms that even at lowest gain, the LNTIA loop is stable and no oscillation was observed.

The other important characteristic of the front-end is its LNTIA noise. Since the LNTIA is the first block in the front-end chain, its noise is the largest contributor to the total input-referred noise of the front-end. The following section measures the LNTIA noise and calculate the SNR at it's output.

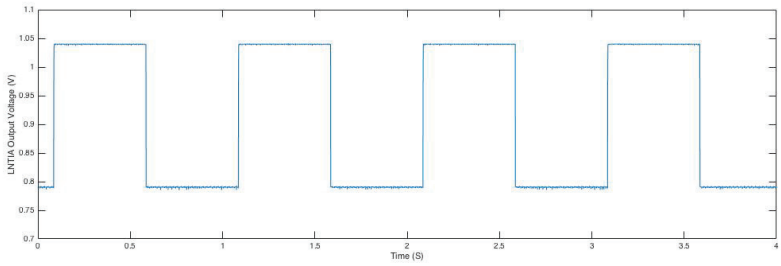


Figure 6.9: LNTIA step response.

6.4.3 LNTIA noise performance and signal-to-noise ratio

The SNR calculated at the output of the LNTIA is approximately the same as SNR at the front-end output. This is mainly because, as the T/H concentrates the signal power into DC, it folds all the noise into the baseband as well. This phenomenon is known as noise fold-over and has been discussed in [63]. Therefore, the noise and signal power are approximately the same at the output of the LNTIA and T/H block. The difference is that the T/H circuit concentrate the signal and noise power within DC to $F_s/2$ band, where F_s is the T/H sampling frequency. The contribution of the T/H circuit noise to the overall input-referred noise is negligible comparing to that of the LNTIA. Similarly, the contrast enhancement amplifier, which is the last block in the AFE, amplifies the noise and signal together. Therefore, its effect on the SNR would be negligible.

Table 6.1 reports the RMS integrated noise voltage at the output of the LNTIA for various DC input currents. The reported values were obtained using a DC current input provided by a Keithley generator. The input was also connected

to a 3 nF off-chip capacitor in order to model the PD output capacitance. The recorded voltage therefore includes both the DC and noise components. This voltage was then converted to digital using LabVIEW. MATLAB frame work was used to filter the output voltage. The RMS noise was then calculated as:

$$V_{out,noiseRMS}[n] = \sqrt{\frac{1}{m-1}\sum_{n=1}^{m}\left(V_{out}[n]^2 - V_{out,DC}^2\right)} \tag{6.2}$$

$I_{input,DC}(\mu A)$	RMS integrated noise 0.1-20KHz (μV)
0.1	225
0.25	230
0.5	240
0.75	280
1.0	350
1.25	375

Table 6.1: RMS integrated noise voltage at the output of the LNTIA for various DC input current.

Having calculated the RMS integrated noise voltage for the bandwidth of interest, the SNR at the output of the LNTIA can be approximated as:

$$SNR = \frac{DI^2c^2A_\Omega^2}{\frac{1}{m-1}\sum_{n=1}^{m}V[n]^2} \tag{6.3}$$

Where D is the photocurrent duty cycle (5% for this study), I is the magnitude of the DC component of the photocurrent, c is the photocurrent contrast and A_Ω is the transimpedance gain of the LNTIA (set at 1 MΩ for our experiments).

In order to calculate the SNR more accurately, we measured the contrast, $\frac{AC_{peak-to-peak}/2}{DC}$, of the PPG signal at the output of the LNTIA. Although the contrast value can slightly vary with time, the average value remained with the 2.5-3.5 % range, which is consistent with those reported in other studies [40, 44]. The contrast value for SNR calculation, therefore, was set to 3 %. Since both signal power and noise power at the output of the LNTIA vary with photocurrent DC level, the SNR for each DC level was calculated using Equation 6.3 and the RMS noise reported in Table 6.1 for each DC level; see Figure 6.10.

As expected, for photocurrents greater than 0.5 μA, our LNTIA outperformed the state-of-the-art PO front-ends reported in [40, 48].

6.4.4 Front-end Offset cancellation

The CDS block which follows the LNTIA cancels the voltage offset at the output of the LNTIA. The DC voltage at the output of the CDS block for 10 different microchips and reported in Figure 6.11. Although these results are promising, one should note that since the measurement has been done only for 10 microchips, the chip with worst case offset might not be among them. To address this issue we repeated the experiment with various DC input currents. In other word, we introduced offset to system and the same result were achieved. In fact, even with a 500mV offset at the LNTIA output, the CDS was still able to successfully cancel it.

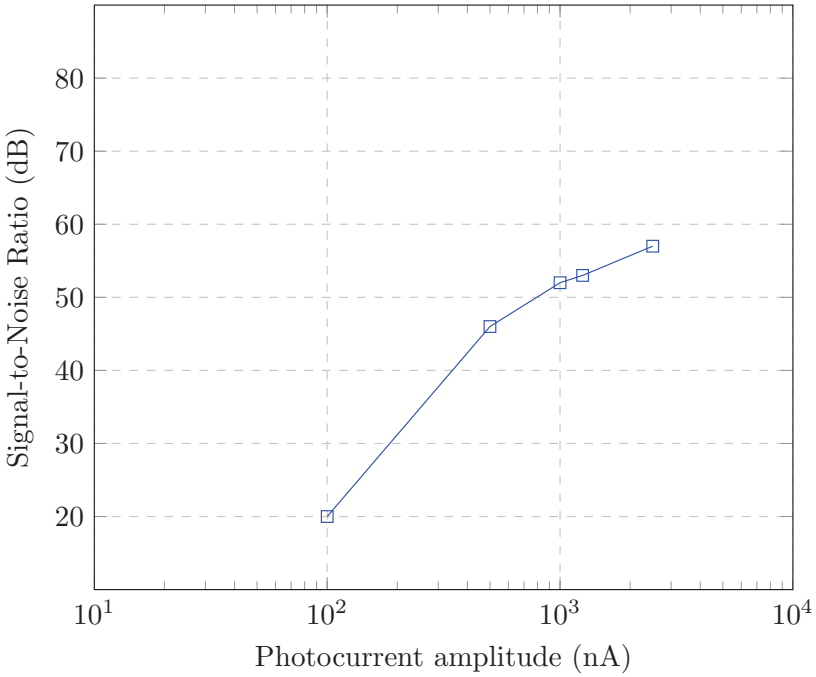


Figure 6.10: Measured SNR for various input DC levels where Duty cycle=5%, contrast= 3% and transimpedance gain= 120 dBΩ.

6.4.5 Static power consumption

We measured the DC current consumption of each sub-block in PPG recording chip by measuring the DC current sunk from the block main supply line. This was easily done by adding a 500 Ω resistor in series with the supply line and measuring the voltage drop across it. We added these resistors on the PCB since the voltage regulators are off-chip in this design. The static power consumption can be calculated using Equation 6.4, where I_{supply} and V_{supply}

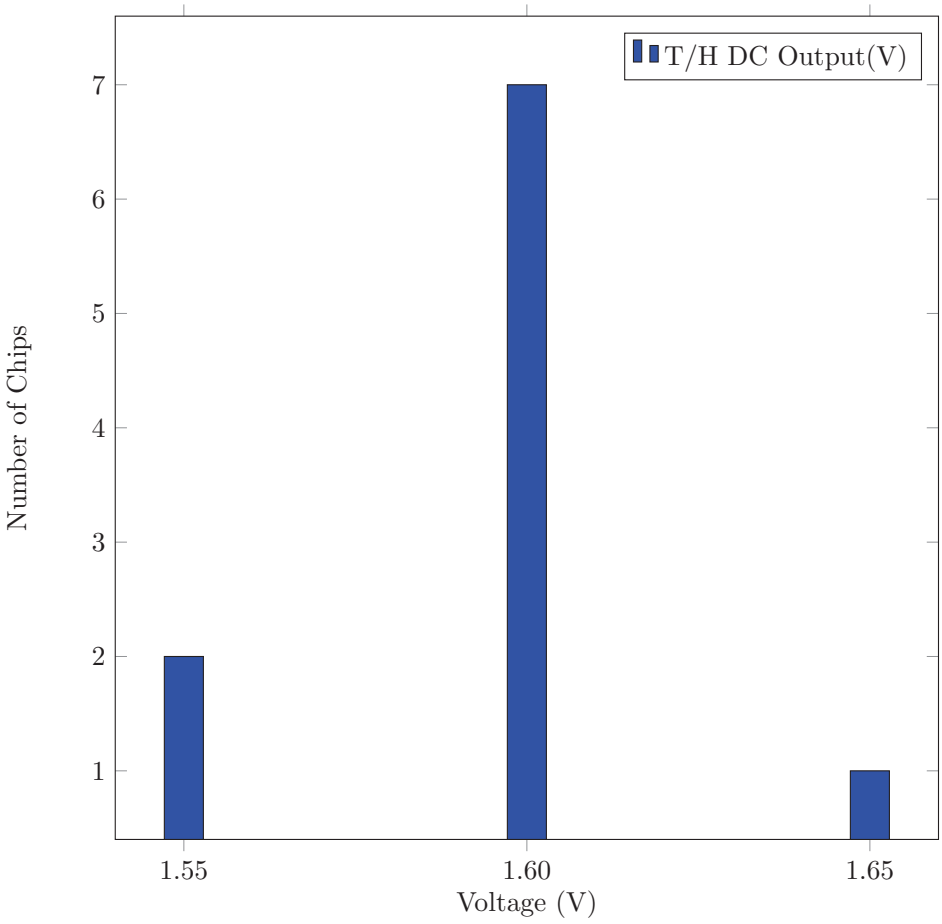


Figure 6.11: The LNTIA output voltage FFT, where the input is 1 μA DC current provided by a Keithley wave-generator.

denote the supply DC current and voltage, respectively.

$$P_{static} = I_{supply} \times V_{supply} \tag{6.4}$$

Table 6.2 reports the measured power consumption of each sub-block in PPG recording chip. With this information, it is possible to estimate how long a battery could be expected to support the frontend before a replacement would

be needed. We can also compare the power consumption of this design with other state-of-the-are designs published in other studies.

Sub-Block	This work	[40]	[7]
AFE per channel (without ADC)	113μV	180μV	190μV
LED and its driver (per LED)	1.38mW	0.9mW	2.2mW
LED light calibrator	42μV	NS	NS
Bias current and voltage generator	Off-chip	NS	11μV
overall (per channel)	1.535mW	0.8-1.9mW	2.4mW

Table 6.2: Measured static power consumption of each block in PPG recording chip (NS= Not Specified).

This calculation confirms that our low-power AFE could be part of a battery-powered device suitable for use in an ICU to monitor brain tissue oxygenation. For example, four Fujitsu 1.2V 2550mAh AA batteries connected in series can supply power for the PO chip designed for this study for more than 5000 hours with losing only 20% of their stored power capacity. However, it must be highlighted that by adding the ADC and bias circuit to the PO chip, the power consumption of the chip increases. This leads to further reduction of battery life-time.

In this chapter, we have reported a quantitative evaluation of the performance and power consumption of our proposed AFE. The parts not included in our microfabricated chips, such as the regulators and ADCs, are well-studied blocks that could be easily added to the AFE chip. We conclude that our proposed design has been successfully tested and offers a significant improvement on current state-of-the-art PO devices.

Chapter 7

Thesis Summary and the Scope for future work.

The goal of this research project was to design and develop a low-power, high performance AFE suitable for use in modern pulse-oximetry devices. In order to maximise the number of photons collected, these typically employ photodiodes with a very large photosensitive area and, therefore, a large output capacitance.

The analysis presented in Chapter 3 quantified the adverse effects of such a large photodiode output capacitance on the stability, noise performance and output voltage headroom of the kind of resistive trans-impedance amplifier (TIA) commonly used as the first stage in conventional commercial pulse oximeters, such as those marketed by Texas Instruments(Component code :AFE4490). A novel low-noise trans-impedance amplifier (LNTIA) has,

therefore, been successfully designed to mitigate this problem.

The proposed LNTIA, as presented in Chapter 4, includes a current amplifier (CA) to decouple the photodiode from the resistive TIA. Simulation results have demonstrated that this is a very effective way to improve the stability of the resistive TIA feedback loop, the output voltage headroom, and the PD reverse bias voltage.

The LNTIA architecture also softens the specification of the resistive TIA feedback op-amp in regard to bandwidth and input-referred noise, which means the op-amp consume less power. In addition, the dependency of the resistive TIA phase margin on the feedback resistor size is eliminated, which means the trans-impedance gain can be programmed.

The post-processing block described in Chapter 5 is inserted after the LNTIA and comprises a CDS circuit to eliminate the DC offset error added to PPG signal by the LNTIA, and a track-and-hold circuit which down-converts the PPG signal into the baseband.

A novel LED light intensity calibrator has also been designed for this study and embedded into the pulse oximetry front-end. This monitors the DC level of the PPG signal at the output of the post-processing module and adjusts the magnitude of the LED bias current in such a way that the PPG signal DC remains within a predetermined boundary. This calibration mechanism makes the LED power consumption adaptive to the strength of the measured PPG signal.

The proposed front-end has been successfully microfabricated on a silicon chip

using AMS 350 nm technology and connected to a photodiode-LED opto-pair on a PCB designed for PPG signal acquisition. The PPG signal acquired from this setup was then filtered in MATLAB to limit the recorded signal bandwidth and provide a high-resolution PPG signal. The voltage noise at the output of the LNTIA block was also recorded. The overall performance of the prototype device, both in terms of general functionality and noise, was highly satisfactory.

7.1 Future Work

The pulse oximetry front-end that has been successfully developed in this project could provide the starting point for future investigation into how the whole PPG acquisition chain can be improved. It should be possible to fabricate, not only the PO front-end, but also the clock generator circuitry, the ADC, the digital low-pass filter and the RF transmitter, all on one single chip. This System-On-Chip solution would allow the designer to optimise each sub-block. It would also be highly desirable commercially, where the cost of a single chip could be significantly reduced by economies of scale.

The front-end designed for this study could also be further improved by the inclusion of additional circuitry capable of compensating for factors that affect the PPG signal integrity, such as motion artifacts and ambient light.

The front-end could also be upgraded to calculate the SpO_2 level on-chip using digital or analog peak-detection techniques. This would significantly reduce

the rate of data generation, which would permit the SpO_2 data to be sent to a monitoring device via a radio transmission link. One advantage of this might be that the radio link would only report the SpO_2 level if it was not within the normal range, permitting all RF circuitry to be switched off the rest of the time, thus significantly reducing the power consumption.

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