

On-Probe Neural Interface ASIC for Combined Electrical Recording and Optogenetic Stimulation

Reza Ramezani, Yan Liu, *Member, IEEE*, Fahimeh Dekhoda, *Member, IEEE*,
Ahmed Soltan, *Member, IEEE*, Dorian Haci, *Member, IEEE*, Hubin Zhao, *Member, IEEE*,
Dimitrios Firfilionis, Anupam Hazra, Mark Cunningham, Andrew Jackson,
Timothy G. Constandinou, *Senior Member, IEEE*, Patrick Degenaar, *Senior Member, IEEE*

Abstract—Neuromodulation technologies are progressing from pacemaking and sensory operations to full closed loop control. In particular, optogenetics – the genetic modification of light sensitivity into neural tissue allows for simultaneous optical stimulation and electronic recording. This paper presents a neural interface ASIC for intelligent optoelectronic probes. The architecture is designed to enable simultaneous optical neural stimulation and electronic recording. It provides four low noise ($2.08 \mu\text{V}_{\text{rms}}$) recording channels optimized for recording local field potentials (0.1 – 300 Hz bandwidth, $\pm 5 \text{ mV}$ range, sampled 10-bit@4 kHz), which are more stable for chronic applications. For stimulation it provides six independently addressable optical driver circuits, which can provide both intensity (8-bit resolution across a 1.1 mA range) and pulse-width modulation for high radiance LEDs. The system includes a fully-digital interface using a Serial Peripheral Interface (SPI) protocol to allow for use with embedded controllers. The SPI interface is embedded within a Finite State Machine (FSM) which implements a command interpreter that can send out LFP data whilst receiving instructions to control LED emission. The circuit has been implemented in a commercially-available $0.35 \mu\text{m}$ CMOS technology occupying a $1.95 \text{ mm} \times 1.10 \text{ mm}$ footprint for mounting onto the head of a silicon probe. Measured results are given for a variety of bench-top, *in vitro* and *in vivo* experiments, quantifying system performance and also demonstrating concurrent recording and stimulation within relevant experimental models.

Index Terms—Optogenetics, optrode, optoelectrode, neural recording, neural interface, implantable, channelrhodopsin.

I. INTRODUCTION

NEUROPROSTHETIC technologies have been steadily improving over the decades. In the 1990's deep brain stimulus (DBS) technologies became available with implantable control systems which provided therapeutic modulation [1]. In tandem, cortical devices such as the Utah array [2] began to provide recording and stimulus of the cortical regions In

R. Ramezani, F. Dekhoda, A. Soltan, D. Firfilionis, P. Degenaar are with the School of Electrical & Electronic Engineering (EEE), Newcastle University, UK. (e-mail: {reza.ramezani, fahimeh.dekhoda, ahmed.abd-el-aal, Dimitrios.Firfilionis, patrick.degenaar}@newcastle.ac.uk).

A. Hazra, M. Cunningham, A. Jackson are with Institute of Neuroscience, The Medical School, University of Newcastle upon Tyne, UK. (e-mail: {Anupam.Hazra, mark.cunningham, andrew.jackson}@newcastle.ac.uk).

H. Zhao was formerly with the School of EEE, Newcastle University, and is currently with the Department of Medical Physics and Biomedical Engineering, University College London, Gower Street, London WC1E 6BT, UK. (e-mail: hubin.zhao@ucl.ac.uk).

Y. Liu, D. Haci, T. G. Constandinou are with the Department of Electrical & Electronic Engineering, Imperial College London, South Kensington Campus, London, SW7 2AZ, UK. (e-mail: {yan.liu06, d.haci14, t.standinou}@imperial.ac.uk).

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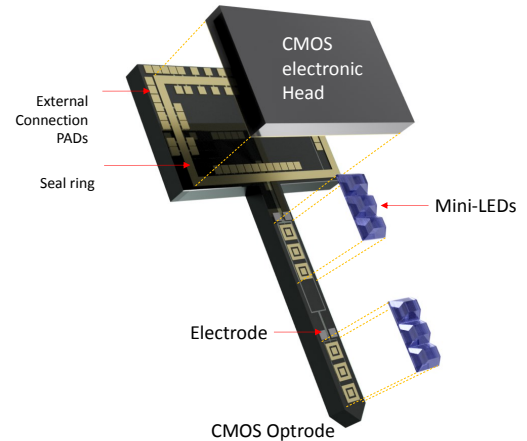


Fig. 1. Proposed optrode concept with passive silicon probe bonded to an active CMOS neural interface ASIC (the focus of this paper). Other examples of optrode implementations can be seen in [4]–[6]. Light emission may be via mini or μLED . In our case recording sites are primarily tuned to local field potential recordings. The neural interface ASIC utilizes a standard SPI protocol for communication an external embedded controller.

recent years, there is a strong push to advance the field towards closed loop systems. Examples include systems which monitor brain activity of epileptic patients and intervene in the case of seizure [3].

A key advance in this drive towards closed loop systems has been optogenetics – the genetic modification of light sensitivity into nervous tissue. This can be achieved by genetically expressing Channelrhodopsin-2 photosensitive ion-channels [7] (or variants thereof) onto the membranes of neurons. There are two key advantages with this approach: The first is that optical stimulus will not interfere with electrical recordings. In contrast, there is a strong stimulus artefact in electronic systems. This can be important for real-time closed loop requirements such as for epilepsy. The second is that through genetic manipulation, it is possible to target specific cells in specific neural sub-circuits [8]. Furthermore, it allows for simultaneous optical stimulation and electrical recording. The medical frontier for this technique is to use it to treat neurological conditions such as Epilepsy, Parkinson's disease or Depression [9]–[11] or provide improved sensory prosthetics such as visual [12]. At the time of writing, the first human trials of optogenetic retinal prosthesis by an independent team have been underway for one year (since 2016). However, clinical results have not yet been published.

The primary issue for optoelectronic approaches to prosthet-

ics is that visible light, and in particular, blue light scatters strongly in neural tissue [13]–[15]. Thus, in order to stimulate deeper areas of the brain, light must be either guided in from afar, or generated locally. Some of the earliest optoelectronics systems have either used single light guiding fibres with deposited electrode materials [16], integrated optic fibres with Utah recording electrodes [17], or made arrays of penetrating optic fibres [18]. The key issue with such approaches is that number of emitted light channels can be limited. Furthermore, subsequent optical emission is transverse through the cortical layer structures. Zorzos et al [19] advanced on these designs by developing a probe with multiple light guiding structures. Emission was improved to a 45° angle. However, optical multiplexing and connectivity is very challenging.

The alternative to light guiding is to generate the light directly at the target site deep in the neural tissue. McAlinden et al demonstrated an optical probe fabricated directly from an LED Gallium Nitride substrate [4]. In tandem, Doroudchi et al [5] and Cao et al [6] have demonstrated silicon probes with bonded on mini ($100\text{ }\mu\text{m}$ to $500\text{ }\mu\text{m}$ width/length dimensions) or micro scale (sub $100\text{ }\mu\text{m}$ dimensions) Light Emitting Diodes (LEDs). A key advantage with this approach is that the light emission can be in parallel with the cortical layering, thus providing better control than with light guiding methods.

These solutions however, have needed to be driven via external electronics. This means that multiple stimulation and recording sites will require a large number of connective wires. This is highly undesirable for devices aiming for clinical translation. As such, a more scalable approach is to integrate intelligent multiplexing of signals onto the probe itself.

A number of highly integrated electronic probes with large numbers of electrical stimulation and recording sites have been previously described. For example, Shulyzki et al [20] have demonstrated a chip which can be combined with existing 8×8 Utah style probes and up to 256 external recording pads. Furthermore, both Lopez et al [21], and Angotzi et al [22] have demonstrated probes fabricated from a CMOS base which incorporate respectively 455, and 512 recording electrodes.

Our interest in this work is therefore to develop an electronic control system, which can both drive high radiance μLEDs and perform electronic recording. To date, there is only one other example of this in the literature [23]. In that work, the stimulator circuitry is designed primarily for laser control, and the electronic recording is designed for single unit (action potential) recordings. In our case, we propose an architecture designed for long term chronic use when integrated onto implantable probes. We have thus designed stimulator drivers to utilize high efficiency ($\sim 30\%$) LEDs, which can achieve total system efficiencies in excess of 20%. This is important for both minimizing undesirable surface heating and ensuring low-power battery operation. Our design records local field potentials as these have proven to be most stable for long term chronic studies [24], [25]. Our also design builds on our previous efforts in neural recording [26], [27] where we demonstrated analogue front-end for low-noise low-power neural recording. It also builds on or previous efforts in developing CMOS driven high radiance neural stimulators for retinal prosthetics [28], [29].

This paper describes a neural interface ASIC that records field potentials from electrode sites on the sides of a silicon probe, and facilitates optogenetic stimulation through driving μLEDs with a precise pulse output. This ASIC has been designed to be mounted to the head of a silicon probe (concept shown in Fig. 1). Overall system design joint with only preliminary simulation results of recording and stimulation subsystems were initially reported in [30]. This paper discusses detailed system operation, circuit design, proposed form factor and *in vitro* test results. We envisage this form factor to be better suited to chronic studies in neuroscience, and towards developing a clinically relevant system. The motivation here is to develop a probe-head that can be hermetically sealed to a probe body. We would envisage such that internal electronics are fully protected from the tissue fluids. Vias in the probe body would then allow connection to probe electrode and light emitter drive lines. We expect this to reduce implant corrosion by containing all DC voltages within the hermetic seal. We then also, implement a symmetric biphasic stimulus to minimize corrosion at the LED stimulation sites. The system additionally has an onboard digital control system which utilizes a standard SPI for external communication with an embedded controller.

The remainder of this paper is organized as follows: Section II describes the concept for neural interfacing; Section III details the system architecture and circuit implementation; Section IV describes the device fabrication; Section V presents experimental results; and Section VI concludes this paper.

II. NEURAL INTERFACE CONCEPT

A. Observing Neural Activity

Neural activity can be observed extracellularly at single unit level using penetrating implantable electrodes, and electronics to amplify and sample this with sufficient bandwidth (typically 10-20 kHz). Although such technology has been the workhorse for most experimental neuroscientists over recent decades, observing this activity chronically has proven challenging. This is because of a number of reasons stemming from the fact that any silicon probe is essentially a ‘foreign body’, with different mechanical/material properties to the surrounding tissue, and the insertion will cause short term damage (rupturing blood vessels, cutting through tissue), and longer term effects (foreign body response, gliosis/scar tissue growth, cell death). Furthermore, there could also be secondary effects due to the integrity of the probe itself (electrode damage, corrosion, mechanical failure during insertion, etc). These challenges are described in some detail in recent reviews by Chen et al [31] and Szostak et al [32].

There has recently been significant interest in instead utilizing local field potentials (LFPs) as the early evidence suggests these may be more resilient to the neural recordings ‘fading’ over time [33], [34]. LFPs are primarily in the 1-100 Hz range, but high frequency oscillations can extend to hundreds of Hz. It has been shown however that even the lower frequency LFPs have useful information content [24], [25], [35], [36].

The work presented herein thus utilises low frequency LFPs for two reasons: firstly to exploit this ‘improved’ chronic stability (compared to single unit recordings); and second to

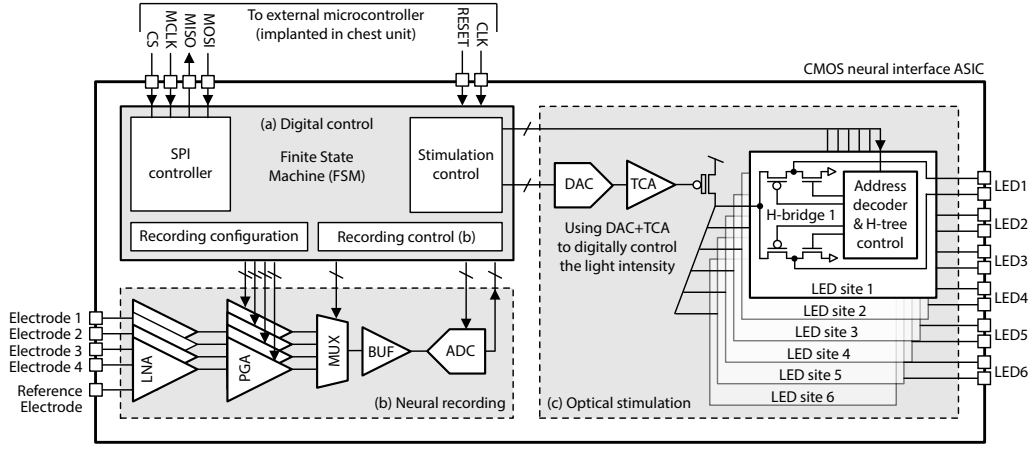


Fig. 2. System architecture for the proposed neural interface ASIC. This supports 4 neural recording channels and 6 optical stimulation sites. The system utilizes a digital unit to facilitate the SPI communication in addition to controlling the recording and stimulation. The internal FSM interprets a custom instruction set which, an external processor can use to configure the system, fetch recorded signals and/or control optical stimulation.

allow for increased scalability – as these recordings require a lower data bandwidth, more channels are possible for a given power budget. Our ultimate aim is to develop devices capable of controlling the dynamics of neural populations, such as abnormal oscillations and or seizures. Such population dynamics is readily observed in the local field potential so we are focussing on this signal.

B. Optical Neuromodulation

Optical stimulation can be physically conducted using high efficiency light emitting diodes (LEDs). Gallium Nitride μ LEDs implemented onto passive optrodes, have been described previously by McAlinden et al [4], have demonstrated efficiencies of around 5%. We have recorded similar efficiencies in our past efforts with such devices [28], [29], [37]. Mini LEDs can provide higher efficiencies as they can be driven at much lower current densities for the same amount of light. We have utilized CREE (DA2432), which provides up to 30% efficiency in the driving range required for optogenetic stimulation. Implementations of similar devices onto passive optrodes has previously been described by Doroudchi et al [5] and Cao et al [6].

Optogenetically encoded cells will integrate light over a period of milliseconds to tens of milliseconds which then modifies their baseline activity [38], [39]. Thus, light can be either driven as a modulated intensity signal over time, or as a fixed intensity with pulse width modulation. I.e. it is the integral photon flux which will drive the response. The developed stimulation system provides both options either separately or in tandem.

III. SYSTEM IMPLEMENTATION

The overall system architecture of the neural interface ASIC is shown in Fig. 2. This has 3 key blocks: (a) digital controller for external communication, interpreting and executing commands; (b) neural recording system for amplifying, filtering, and digitizing biopotential signals; and (c) optical stimulation

system for generating, timing and driving μ LEDs to facilitate optogenetic neural stimulation.

The system has two power domains: 3.3 V (using native devices) and 5 V (using thick oxide devices). The 3.3 V is used for all circuits (digital, recording, stimulation control and generation) except the stimulation output stage. The 5 V supply is required to drive blue μ LEDs. This type of LEDs are known to have considerably higher threshold voltage compared to conventional ones. Using 5 V supply, LEDs can be driven to produce a wide range of output light power.

A. Digital Control

The digital controller provides the following functions: (1) SPI communication interface with external processing and control units; (2) a finite state machine (FSM) with defined instructions which can control the μ LED driving circuits, configure and control the acquisition of data from recording circuits.

The FSM has been designed to operate with minimum latency with respect to incoming SPI commands. This receives configuration, issues stimulation timing and control signals, and fetches recording data upon request. This has been designed to be tightly integrated within the interacting sub-blocks.

All operations in the digital controller are synchronized to a master clock, except for the SPI transceiver, which uses the SPI clock MCLK. An external reset is used to provide a global reset of all internal states.

1) *Serial Peripheral Interface (SPI)*: Both commands received (i.e. configuration and control) and transmitted output (i.e. recording) data are processed as either 8 or 16-bit packets on a SPI protocol. These packets have the LSB (least significant bit) first, rising edge data-in and falling edge data-out. The Master, i.e. external controller will assert an active low CS (chip select) before providing the SPI clock signal. The SPI slave, i.e. this system, will update the serial output MISO (master in slave out), and shift in the serial input MOSI (master out slave in) at the falling edge of the MCLK. On the 8th falling edge, the SPI slave will put D0 of the next SPI packet on MISO. A

TABLE I
IMPLEMENTED COMMAND SET WITH CORRESPONDING OPERANDS

Instruction	Purpose	Parameter	Extended data
0001xxxx	Set LED status OFF	Mem. addr.	N/A
0010xxxx	Set LED status ON	Mem. addr.	N/A
0101xxxx	Set LED value	N/A	8-b DAC for LED
0111xxxx	Read recording	N/A	Two 8-b words
1000xxxx	Set recording clock	Ratio	N/A
1001xxxx	Set sampling frequency	Ratio	N/A
1011xxxx	Enable recording	N/A	N/A
1111xxxx	Empty for data fetch	N/A	N/A

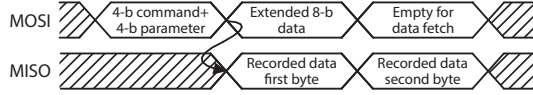


Fig. 3. Timing diagram for the SPI protocol that uses an 8-bit data packet to transmit instructions and receive data. The first byte contains the 4-bit command and a 4-bit coefficient (LED address or clock ratio). The second byte is used to adjust the light intensity of the μ LED (8-bit DAC value) or to read the first 8-bits of recorded LFP data. In order to read the remaining bits, an empty command is transmitted (i.e. recorded data requires 12-bits).

custom instruction set (listed in Table I) has been designed and implemented to allow the SPI master tight low-level control of the neural interface ASIC. Each command packet has an 8-bit length, with the first 4-bits specifying the instruction, and last 4-bits a parameter that is specific to each command. If the command is to Set LED value, an additional 8-bit parameter is required from the master, corresponding to the DAC value. This is illustrated in Fig. 3.

2) *Finite State Machine*: The FSM controls all aspects of the operation of the neural interface ASIC, setting the state of both the stimulation and recording sub-systems, and responding to any inputs from the SPI interface. This has a total of 10 states: 8 that are directly related to instructions, one idle state and one error state. A valid SPI command described in the previous section will trigger the FSM to enter the corresponding state, and generate relevant control signals and/or set the SPI output data buffer. All states, and corresponding conditions are shown in Fig. 4.

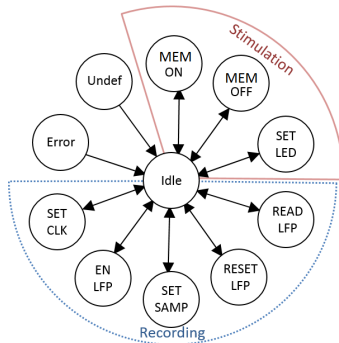


Fig. 4. State transition diagram for the optrode controller that has been implemented as an 10-state FSM. In addition to the 8 states that are directly selected by the SPI command interpreter, two additional states have been included to avoid error and/or undefined states which may occur due to glitches. The corresponding instructions are listed in Table I.

B. Neural Recording

Each electrical recording sub-system will continuously observe LFP signals at that site. LFP signals can have amplitudes up to 5-10 mV, with a power spectrum predominantly below 100-200 Hz (down to sub-Hz). The LFP recording sub-system in the optrode includes four recording channels, a shared ADC and corresponding control logic. Each recording channel consists of a low noise Front-End Amplifier (FEA) to couple to electrode and provide low-noise amplification, and a 2^{nd} gain stage for further amplification with relaxed noise requirements. The ADC is shared by multiple neural recording channels. Therefore, a buffer with sufficient drive strength is required to reduce the settling error and crosstalk between multiplexing.

1) *Design considerations for LFP recording*: In order to amplify low level (i.e. sub-millivolt) neural signals to fill the dynamic range of the ADC, a large voltage gain is required with minimal added noise. This can be achieved using a capacitive network that provides efficient feedback with good matching and power consumption. Multiple capacitive-coupled amplifiers can subsequently be cascaded to achieve the high gain without requiring a large (ratio) capacitor array and open loop gain [21], [27], such that noise of the following stage can be minimized when referred to the input.

Chopper-based FEAs can generally achieve better low frequency noise performance, however this is at the expense of a reduced input impedance, switched-capacitor induced thermal noise and requiring an extra clock source [40], [41]. These are therefore mainly used in EEG (electroencephalogram) and ENG (electroneurogram) recording applications (that have relaxed requirements on input impedance). In implantable devices however that require LFP recording, any reduction in the input impedance of the front-end may lead to long term electrode degradation. Although recently there have been techniques proposed to boost the input impedance in such circuits, these require precise device matching and/or auto-zeroing techniques [42]. Taking these factors into account, the design presented herein has used an AC-coupled approach that balances the area/power trade-off achieving an equivalent noise performance. [27]

2) *Low Noise Front-end Amplifier (LN-FEA)*: The LN-FEA couples to the electrode (rejecting any DC offset) and amplifies the input signal with minimal added (electronic) noise. To ensure a sufficient signal-to-noise ratio (SNR) and thus to maximize the observed input signal, a large input impedance is required relative to the source (i.e. electrode) impedance (typically 10-100 k Ω). In this design, the FEA is based on the widely-used topology first proposed by Harrison [43], which a capacitive ratio to define the AC gain (i.e. capacitively coupled input with capacitive feedback). By using a relatively large input capacitance (≈ 3.4 pF), the input impedance over the 100 Hz signal bandwidth will be in the order of 100 M Ω , which is 3-4 orders of magnitude greater than a conventional electrode impedance. However, an electrode fabricated on-chip may exhibit a larger than anticipated input impedance (i.e. > 100 k Ω).

The LN-FEA design is shown in Fig. 5(a). Pseudo-resistors are used to set the DC operating point at the input of the amplifier. Capacitive feedback is then used to define the gain

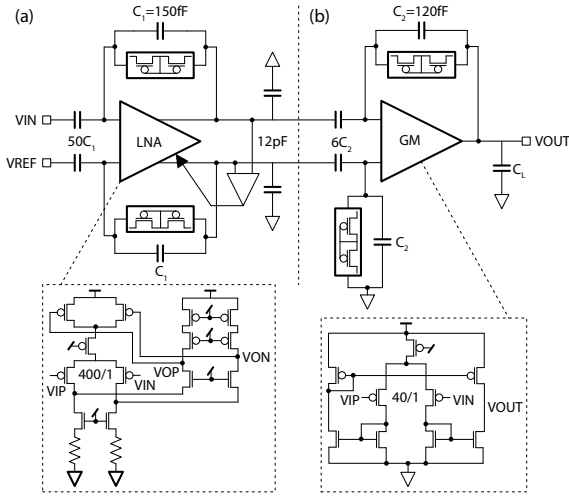


Fig. 5. Circuit schematic of the analog front end (AFE) neural recording system. Shown are the first two gain stages including: (a) fixed gain ($\times 50$) low noise amplifier (LNA); and (b) programmable gain ($\times 1$ -6) amplifier (PGA). The LNA has been based on a folded-cascode topology to ensure good noise efficiency. The PGA then provides additional gain if required.

(set to 50, i.e. 33 dB), with a unit capacitance of 150 fF. The amplifier uses a fully-differential folded-cascode operational trans-conductance amplifier (OTA) topology with resistive source degeneration for noise suppression [44]. Input transistor size have been designed to minimize flicker noise without introducing large parasitic capacitance for noise. Deep triode transistor are used for continuous-time common-mode feedback (CMFB) circuit, with an PMOS to boost the tail current source impedance. Two pairs of pseudo-resistors (connected in series) are used to place the pole below 0.1 Hz, in order to remove electrode offset and any low frequency drift (i.e. at frequencies below 1 Hz). To compensate temperature variation and device mismatch, cascaded diode-connected PMOS pairs are used to increase the resistance, such that the high pass pole is well beyond the signal bandwidth, and PVT induced variation has a minimal effect on signal integrity. The low-pass (LP) pole is defined at around 7 kHz, determined by the load capacitor (12 pF), which is realized using MOS-cap devices.

3) *Programmable Gain Amplifier (PGA) Stage*: As the gain of the FEA is only 50, i.e. 33 dB, a second gain stage is needed to amplify the LFP signal such that it fills the input range of the ADC. Therefore a 2^{nd} stage gain of 6 is needed, to avoid saturating the supply voltage range. This is achieved by using a single-ended amplifier with capacitive feedback. This amplifier uses a fully-symmetrical OTA Harrison [43] with schematic shown in Fig. 5(b). The response of the first two gain stages is shown in Fig 6.

4) *Analog-to-Digital Conversion (ADC)*: The outputs from the four PGAs are fed into a 4:1 analog multiplexer, which is controlled by a select signal generated by the recording control block. It uses complementary switch pairs with size of $32\mu\text{m}/0.35\mu\text{m}$. To drive the relatively large capacitive load of the ADC input, a buffer stage is used after the multiplexer output. It uses symmetric OTA, similar to the PGA, but with increased current bias ($2.5\mu\text{A}$) to boost the bandwidth and slew rate. The ADC used by our LFP recording is based on

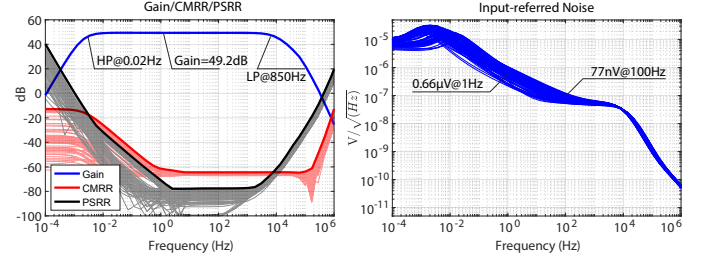


Fig. 6. Neural recording analog front-end (AFE containing LN-FEA and PGA) performance. Shown are: (a) frequency response of gain, CMRR and PSRR; (b) input-referred noise characteristic.

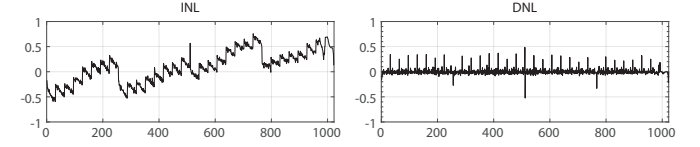


Fig. 7. Measured integral and differential non-linearity (INL and DNL) of the 10-bit SAR ADC.

a 9:1 split array charge-redistribution fully differential SAR (successive approximation register) ADC with 10-bit resolution and 33 fF unit capacitance. The measured INL and DNL for the ADC is shown in Fig. 7.

5) *LFP Streaming*: In order for LFP data to be received, the SPI master must first issue a read LFP data command. This requires three 8-bit data packets: one byte to set the state, and another two bytes to transmit the output data. The recording data requires 12-bits (consisting of a 2-bit channel index and 10-bit data sample), plus one additional bit to store the register index. Two 12-bit registers are required within the FSM to store the input value from LFP sub-system. These are selected alternately by the read and write processes. Once the read process is initiated through an SPI command, the first 8-bits are placed on the SPI bus, until they are read on the next rising edge. The remaining bits are then placed on the bus to subsequently be read.

C. Optical Stimulation

The proposed system allows for up to six optical stimulation sites that can be positioned along the length of the optrode shaft, delivering light to perform multi-layer neural stimulation.

The architecture has been designed for use with multiple different types of light emitting diode – both mini-LED and μLED . To exemplar this work, we have been utilizing a mini-LED from CREE DA2432. The LED-only performance for can be seen in Fig. 8. The CREE LED has dimensions of $320 \times 240\mu\text{m}$, so the current density ranges from 0 - 65 mA/mm^2 (5 mA) compared to an excess of $15,000\text{ mA/mm}^2$ for micro-LED devices of diameter $20\mu\text{m}$. As such the response profile of radiance vs current is largely linear in this range, with minimal droop profile. The efficiency peaks at $\sim 30\%$ subsequent decay is due to increased drive voltage requirement. To compare with previous literature, both Wu et al [45] and McAlinden et al [4] developed passive probes with micro-LEDs. Wu et al used LED currents of $45\mu\text{W}$ to generate $8\mu\text{W}$ of optical power and McAlinden et al used currents of up to 5 mA to generate

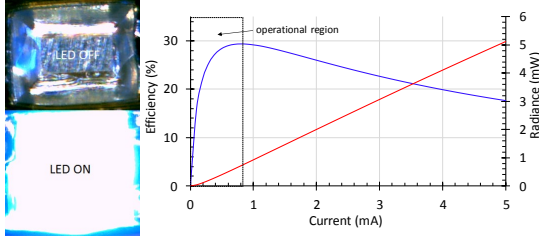


Fig. 8. Optical output power and efficiency of the utilised CREE mini-LED as a function of input current. It can be observed that the efficiency can reach up to 30%. Output power was measured using an integrating sphere.

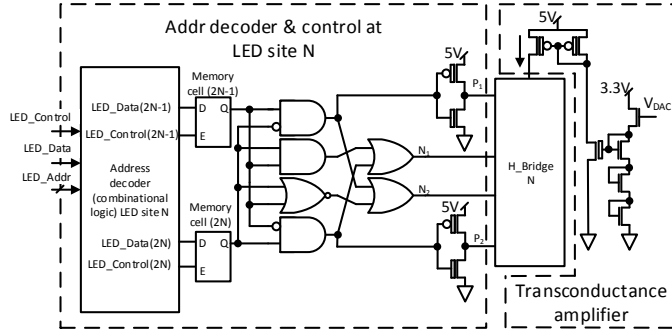


Fig. 9. Circuit schematic of the LED control, address decoder, and stimulus generation. Each site driving an LED contains an H-bridge and control logic. A single transconductance amplifier is shared across all 6 output channels.

radiance of $600 \mu\text{W}$. Both modeled the expected penetration depth into tissue for an irradiance of $1 \text{ mW}/\text{mm}^2$. The former ($45 \mu\text{W}$) achieved $60 \mu\text{m}$, whereas the latter ($600 \mu\text{W}$) achieved $175 \mu\text{m}$ of penetration. As such, we believe that LED drive currents in the region of $0\text{--}1 \text{ mA}$ are sufficient to stimulate bulk neural tissue. This region is highlighted in yellow in Fig. 8

1) *Stimulation Commands*: The optical stimulation architecture is shown in Fig. 9. Intensity can here be controlled via both pulse width modulation and intensity control. The latter can be achieved with an 8-bit value sent to the Set LED state. Pulse width modulation of ON and OFF states are achieved by programming the two memory cells. There is an additional Read LED state to return the value of the memory cell. Each memory cell is accessible by a unique address value.

2) *H-Bridge*: The simplest mode of operation would be to have a single PMOS transistor which varies in analog between fully ON and OFF. Intensity control can then be achieved with pulse width modulation. Grossman et al [39] previously demonstrated that the most efficient way to drive optically encoded neurons is via short high intensity pulses of light. However, at this stage, it may be also useful to modulate the intensity in analog – hence, we developed a circuit to implement both. An additional challenge for chronic use is to minimize undesirable net electric fields across exposed implantable components. We thus implemented an H-bridge configuration which allows for the voltage profile to be reversed thus generating a biphasic electric field. The different states of operation of the H-bridge are listed in Table II.

3) *μLED light intensity control*: Intensity can be control via a voltage DAC which is then converted to a current via

TABLE II
H-BRIDGE OPERATION STATES

Operation	Mem. cell 1	Mem. cell 2	P1	P2	N1	N2
OFF/Cathode to GND	0	0	1	1	0	1
Forward Stimulation	1	0	0	1	0	1
Reverse-biased	0	1	1	0	1	0
OFF/Anode to GND	1	1	1	1	1	0

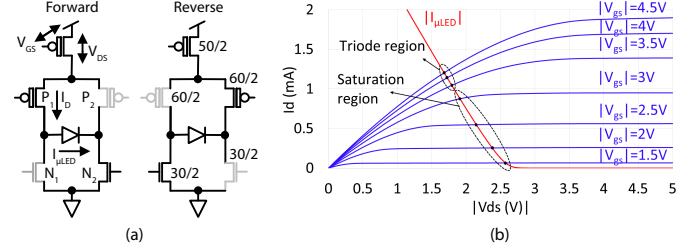


Fig. 10. H-bridge circuit operation showing: (a) the forward and reverse bias configurations (note that N1 and N2 are 3.3 V transistors); (b) output driver transistor characteristic (overdrive voltage versus drain current) against μLED current (load line).

a transconductance amplifier shown in Fig. 9. The DAC has 8-bit resolution and a 0 to 3.3 V output range which provides a current range of $0\text{--}1.1 \text{ mA}$ through the TCA and H-bridge. This will produce up to 0.8 mW optical stimulation at μLED .

The TCA is not an ideal current amplifier. A load line plot for the drive transistor and measured data from the LED can be seen in Fig. 10. For much of the curve, the resultant operation is in the triode region, which means it will also be limited by factors such as sheet resistance of the optrode lines and contact resistances during bonding. However, we would argue that it is better to operate in the triode region, as more of the drive voltage then drops across the LED resulting in an overall more power efficient operation. Device variability can be smoothed out by varying the stimulation time.

IV. PROBE INTEGRATION

The neural interface ASIC was fabricated in AMS $0.35 \mu\text{m}$ 2P4M CMOS technology (C35B4C3). The microphotograph of the die is shown at Fig. 11(a). The prototype occupies total area of $1.95 \times 1.1 \text{ mm}^2$. The die has been designed to then be flip-chip bonded onto a passive optrode, similar to those previously described in the literature [4]–[6].

A. Passive optrode

The microphotograph of the passive optrode designed in this work is shown at Fig. 11(b). This optrode was fabricated in the same technology as the ASIC. The head and the shank regions occupy $2.3 \times 1.5 \text{ mm}^2$ and $2.73 \times 0.28 \text{ mm}^2$ respectively. The shank contains pads to deposit 4 electrodes and 6 LEDs. The head region contains the pad arrangement to match ASIC layout when flip-chip bonding as well as connections to the components down the shank. The seal ring around the head region indicates the borders, where the ASIC will be positioned. This ring is essential to isolate the ASIC from moisture when the device is implanted in tissue [46], [47], though we do not demonstrate this post-fabrication here.

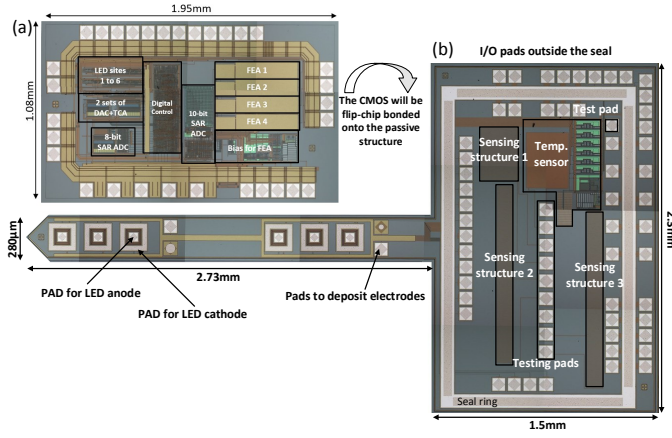


Fig. 11. Fabricated device microphotograph showing: (a) the neural interface ASIC implemented in 0.35 μm CMOS technology; (b) CMOS-based probe with pads for μLED and electrodes and head template for flip-chip bonding of the electronics. The seal ring on the head section is essential to hermetically seal the electronics against any liquid percolation. [46]

B. Temperature monitor

The literature on long term effects of hot probes on neural tissue is still unclear. However, the American Association of Medical Instrumentation (AAMI) recommend a limit of $dT = +2^\circ\text{C}$. i.e. any exposed surface to the tissue should be $\leq 39^\circ\text{C}$. We propose the use of relatively efficient LEDs ($\sim 30\%$ at the LED). But nevertheless, the thermal limit is small, and thus it can be useful to monitor overheating. Should a sensor indicate that this is occurring, the LED pulse widths can be adapted accordingly.

Temperature can be monitored as a resistance change on surface resistors. We therefore implemented resistors as a spiral coil and placed in each gap between the anode and cathode pads for the LED, and is covered by the passivation layer without direct contact with LED. Metal tracks of $0.6\mu\text{m}$ wide, total length of $3100\mu\text{m}$, was used as the sensing elements with equivalent resistance of 220Ω . An amplification stage is used to output the temperature, shown in Fig 12.

These temperature sensors were characterized without LEDs bonded in an ESPEC temperature chamber with temperature changing from 20°C to 50°C . The measured voltage output of two sensors show a sensitivity of 2mV per degree, as seen in Fig 12. It can be found that these temperature sensors exhibits large offset which varies from sensor to sensor. Thus there would need be a calibration step for each prior to use. There is also a further complication in that there will be a temperature difference between the location of the sensor and the surface. This would need a further calibration step as it will depend on the passivation layer properties and thickness. As such probe fabrication details go beyond the scope of this paper, we do not explore this here.

V. MEASURED RESULTS

To fully characterize the design, a set of bench-top, *in vivo* and *in vitro* experiments were conducted. *in vivo* recording of cortical neural activity in non-human primate verified the operation of for our long-term aims for medical translation. We

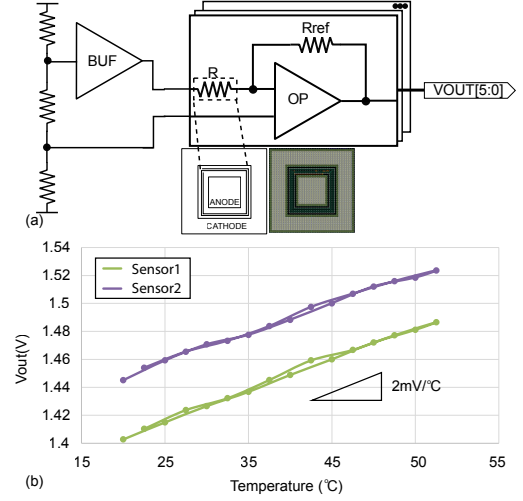


Fig. 12. (a) Temperature sensors and readout circuits; (b) Measured temperature response.

did not however have a genetically modified non-human primate expressing channelrhodopsin-2. We therefore demonstrated the efficacy of the LED illumination using *in vitro* rodent brain tissue.

A. Probe verification

The proposed probe has been validated using a microcontroller-based test platform providing a USB2 PC interface for control and data visualization. This is based on an ARM Cortex-M4 device (Freescale Kinetis K64F) that is configured to be SPI master connecting to the ASIC digital interface. The test configuration is shown in Fig 13.

B. Bench-top testing

The detailed communication handshake during the read recording command (see Table I) is shown in Fig. 14(a). As it can be observed, the digital controller is running at 12MHz clock frequency (master clock), with the SPI clock set at 6MHz . It is worth mentioning that the digital controller can also be reliably operated at a lower frequency e.g. 300kHz in reduce power consumption mode. The stimulation operation – SPI communication) followed by μLED being pulsed is shown in Fig. 14(b). As can be observed, with a 12MHz master clock frequency, the LED ON/OFF frequency can reach up to 50kHz . The limiting factor is the SPI handshake sequences.

Accurate optical measurements have been done by connecting the neural interface ASIC to the target LED (CREE DA2432) that is placed inside an integrating sphere (P10 from Artifix). The output stimulus was then adjusted by sweeping the DAC range. The measured results are shown in Fig. 15. This shows that an optical stimulus of up to 0.8mW can be illuminated to the adjacent tissue.

C. Experimental (*in vivo/in vitro*)

All animal experiments were approved by the local ethics committee at Newcastle University and performed under appropriate UK Home Office licenses in accordance with the

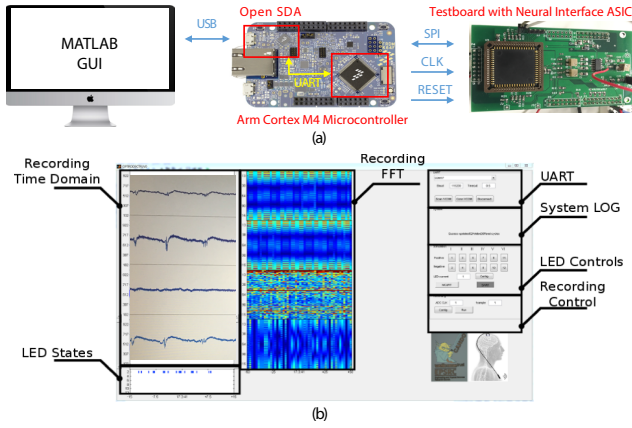


Fig. 13. Test configuration showing (a) Microcontroller-based embedded test platform; (b) MATLAB-based GUI for device control and data visualization.

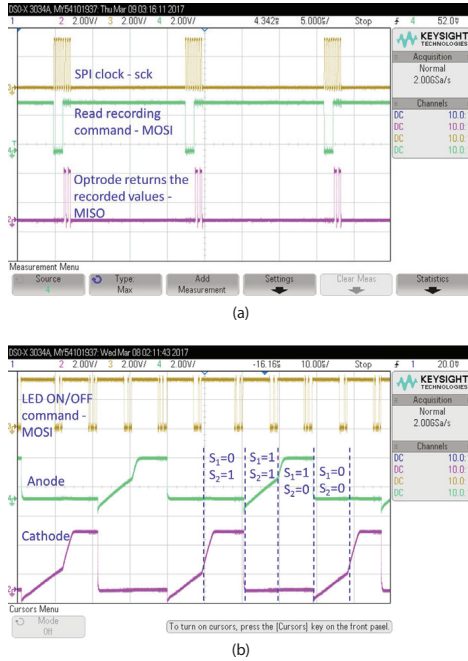


Fig. 14. Measured system response during SPI communication showing: (a) neural recording command issued followed by output data packet; (b) optical stimulation command (set ON followed by set OFF) followed by μ LED response. S1 and S2 represent memory cells 1 and 2 switching to '0' and '1' to each SPI command received.

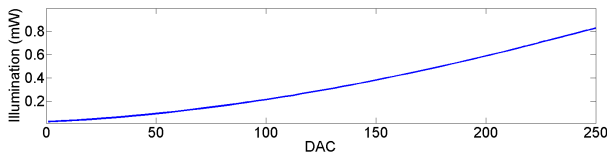


Fig. 15. Measured response of μ LED across output range of DAC values showing the range of illumination power.

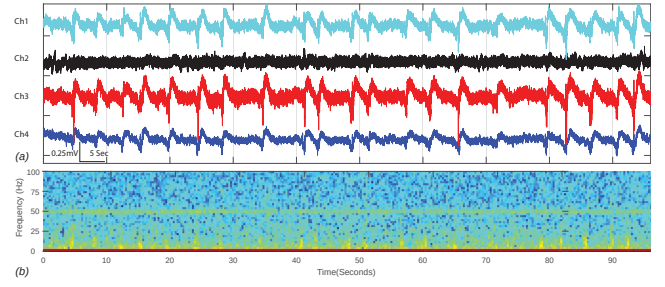


Fig. 16. Sample neural (LFP) recording from non-human primate (macaque monkey). Data has been captured via SPI after 10-bit ADC conversion at a 2.5 kHz sampling rate. Data in frequency domain is shown only for 0-100 Hz range where the LFP data are expected.

Animals (Scientific Procedures) Act 1986. The animal reported here had already been implanted with a chronic electrode array for the purposes of another ongoing study relating to Brain-Machine Interfaces, and the data documented here were taken during a scheduled sedated recording session associated with that study. Therefore no additional licensed procedures were required to collect this data.

The recording sub-system was validated *in vivo* in a rhesus macaque with moveable microwire electrodes (50 μ m tungsten with Teflon insulation) [48] implanted into the motor cortex (M1) and protected with surgical cement and a skull mounted titanium case.

Impedance measured for channel 1,3, and 4 were around 200 k Ω at 100 kHz. The recording gain was 300 and sampling frequency was 2.5 kHz. It should be noted that the Channel 2 did not record valid data due to electrode failure (Measured impedance >4 M Ω). We observed large 'K-complex' events that are characteristic of sedation with ketamine. Spectral analysis (Fig. 16(b)) suggests that these events are associated with increased power in the delta (1-4 Hz) and alpha (10 Hz) bands. The continuous band of power at 50 Hz reflects mains interference. Fig. 16(b) shows the spectrum diagram of channel 1, with most energy spread within 20 Hz and 50 Hz interference.

One important practical point to note is that the AFE is only accessible via the 10-bit ADC. Therefore, the overall operational frequency is limited between the low cut of frequency of the LNA and the sampling frequency of the ADC.

In order to perform optical stimulation on non-human primate, genetic engineering is required which would have gone beyond the existing ethical remit. Therefore of this part of the work, we utilised a transgenic mouse which had channellrhodopsin-2 encoded into its core genome. We also decided to use ex-vivo brain slices rather than full in-vivo measurements. In part this was to minimize impact on the animal at this early stage of the research. But it also made the calibration and experimental setup more straightforward.

The *in-vitro* experiment is done using a 400 μ m thick brain slice. This brain slice has been pharmacologically manipulated with bath-application of 4-Aminopyridine, which renders it hyperexcitable. Fig. 17 shows the voltage waveform of neural activity while optical stimulation is applied.

The oscillatory activity that is seen emerging following the optical stimulation represents a seizure-like event that

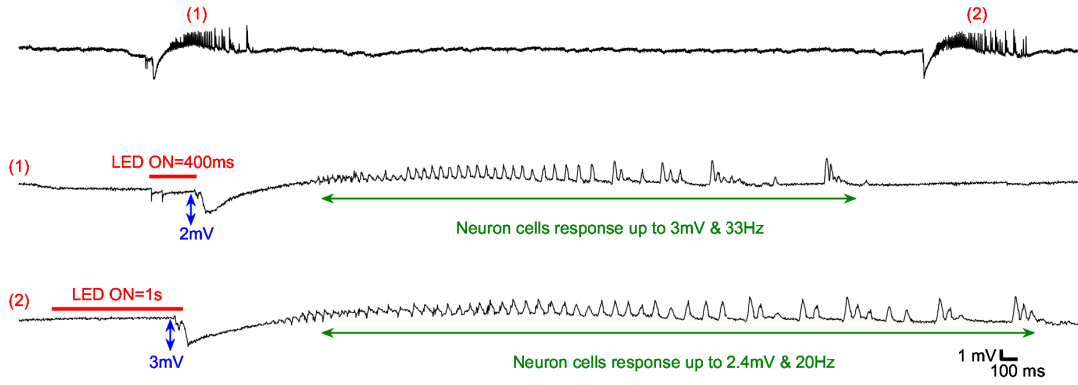


Fig. 17. *in vitro* neurological recordings (LFP recording) from transgenic mouse (genetically modified to have light-sensitive cells) brain slice while optical stimulation is applied. Observed data contains cell depolarization and neural cell responses. According to this experiment, neural activity up to 3 mV and 33 Hz are recorded in response to 0.8 mW illumination power.

has been elicited by the optical stimulation. These seizure-like events reach up to 2 mV in amplitude and 16 Hz in frequency. Parameters such as the degree of light-sensitivity of the tissue and illumination power of the μ LEDs play the key role to sufficiently stimulate the cells. This design provides up to 1.1 mA current to the μ LED which produces up to 0.8 mW of illumination power. One could increase the driving current if more illumination and better stimulation is required. This, however, increases the power consumption (more heat dissipation).

VI. CONCLUSION

This paper has presented a neural interface ASIC that connects to a passive optrode to facilitate electrical recording and optical stimulation. The design supports four low noise neural recording channels and six optical stimulation channels. The neural recording and stimulation electronics have been optimized for observing LFPs from electrode, and driving μ LEDs sites respectively all positioned along the length of the optrode shaft. The design also includes an integrated digital controller that implements a custom command interpreter and enables communication and system control using an external embedded processor via a SPI bus. After CMOS fabrication of the electronics, the design has undergone additional fabrication stages to meet the requirements for clinical operation. The overall specification of this optrode are listed in Table III and comparison with other existing designs is shown at Table IV. Future work will explore the post-fabrication requirements to implement the ASIC into a fully encapsulated probe as well as long term use in neural tissue.

ACKNOWLEDGMENT

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TABLE III
ACHIEVED SYSTEM SPECIFICATIONS

Parameter	Value	Unit
Analog Front-End (AFE) Neural Recording		
Recording channels	4	-
Input-referred noise (0.1 Hz-300Hz)	2.08	μV_{rms}
NEF	6.69	-
High pass f_0	0.02	Hz
Low pass f_0	830	Hz
Gain	49.54	dB
PSRR @ 10 Hz	83	dB
CMRR @ 10 Hz	65.88	dB
THD (40 Hz, 4 mV _{p-p})	0.89	%
Power (LNA+PGA) – per channel	9.80	μW
Power (buffer) – shared	8.05	μW
Power (bias) – shared	53.06	μW
Analog-to-Digital Converter (ADC)		
ENOB	8.9	bit
Noise	200	μV
DNL	<0.6	LSB
INL	<1.1	LSB
ADC power @ 16 kHz	31.68	μW
Neural Stimulation		
Stimuli	Optical pulses	-
Number of μ LEDs	6	-
μ LED power supply	5	V
Stimulus type	Biphasic	-
Max. μ LED current	1.1	mA
Max. output light power	≈ 0.8	mW
μ LED efficiency	Up to 30	%
Data Communication		
Protocol	SPI	-
Packet size	8	bit
Max. System Power Consumption		
3.3 V supply – without power gating	3.5	mW
5 V supply – all LEDs on at full power	9.9	mW

TABLE IV
COMPARISON WITH STATE-OF-THE-ART

Parameter	[unit]	Fully electrical (electrode-based)				This work	Optogenetic (optrode-based)		
		[49]	[20]	[50]	[23]		[45]	[51]	[52]
Technology	[μm]	0.18	0.35	0.18	0.18	0.35	PCB	PCB	0.35
Integrated AFE	-	Yes	Yes	Yes	Yes	Yes	No	No	No
Recording channels	-	4	256	16	1	4	32	No	No
Neural signal	-	LFP	LFP	AP, LFP	AP	LFP	AP, LFP	N/A	N/A
Gain	[dB]	54	53	40	50	50	-	N/A	N/A
Noise	[μV_{rms}]	6.3	8.0	4.6	4.6	2.1	2.0 [†]	3.0	2.4 [‡]
Noise bandwidth	[Hz]	0.6-6k	0.1-10k	0.3-7k	300-5k	0.1-300	0.1-10k [†]	3-8k	0.1-10k [‡]
NEF	-	3.76	8.9	4.77	-	6.69	-	-	-
ADC	-	Pipeline	Single-slope	SAR	N/A	SAR	-	N/A	N/A
Stimulation	-	Electrical	Electrical	Electrical	Optical	Optical	Optical	Optical	Optical
LED efficiency	[%]	N/A	N/A	N/A	N/A	30	0.8	2	10
Closed-loop operation	-	Yes	Yes	Yes	Yes	Yes	-	N/A	Yes

[†]based on Intan Tech RHA2132 datasheet, [‡]based on Intan Tech RHD2132 datasheet

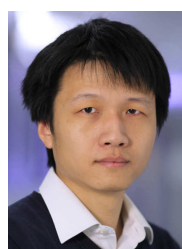
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Reza Ramezani received his M.Sc. degree in communication and signal processing with distinction in 2009 and Ph.D. degree in microelectronics in 2014 from Newcastle University. In September 2012, he joined ARM Ltd. design team which developed the first 64-bit system-on-chip utilizing the big-LITTLE architecture for mobile applications. Since August 2014, he has worked with CANOD (<http://www.cando.ac.uk>) research team at Newcastle University to develop the first in-human bioelectronic treatment for epilepsy. His main research interest is biomedical implantable CMOS for neural interfacing, specially designing electronics for chronic optical stimulation of neurons using advance Optogenetics tools. He is also interested in developing circuit solutions and VLSI implementation for mixed-signal problems in power supply electronics within any energy deficient environments. He received the award "Innovator of the Year 2012" from Newcastle University for his research entitled Energy-modulated computing: a new paradigm for designing circuits and systems in energy-constrained environments.



Yan Liu (AM'08–M'12) received the B.Eng. degree in 2006 from Zhejiang University, China, the M.Sc. degree in 2007 and Ph.D. in 2012 from Electrical and Electronic Engineering at Imperial College London, UK. He is now a research fellow in Centre of Bio-inspired technology, Electrical and Electronic Engineering at Imperial College London. His research area includes: CMOS based lab-on-chip devices and platforms, brain machine interface, and novel mixed signal circuits for biomedical applications.

Fahimeh Dehkhoda received M.Sc and Ph.D degrees in electrical engineering from the University of Tabriz, Tabriz, Iran in 2004 and 2012, respectively. She was a visiting researcher in the Centre of Biomedical Engineering at the University of Adelaide, SA, Australia from 2010 to 2011 working on multi-channel receiver for micro-MRI. She joined CANDO project in 2014 to work on implantable electronics at the school of Engineering, Newcastle University, Newcastle, UK. She is currently research associate at the school of Engineering, University of Edinburgh, Edinburgh, UK working on CMOS design for SPAD sensors in QuantIC project. Her research interests are towards biomedical implantable CMOS and sensor interface, CMOS based spectroscopy and SPAD imaging systems.



Ahmed Soltan received the B.Sc. and M.Sc. degrees from the University of Cairo, Cairo, Egypt, in 2004 and 2008, respectively. He received the Ph.D. degree in electronics and communication from Cairo University in 2014. Dr. Soltan awarded the 2014-16 best thesis award from Cairo for his PhD thesis. He worked on circuit and system design in the fractional order domain during his PhD research. He is currently working as a research associate and EDACAD specialist at the School of Engineering, Newcastle University. Dr. Soltan worked as a teacher

assistant at faculty of Engineering, Fayoum University for 9 years and worked as an R&D firmware engineer for 8 years. He also worked as an R&D manager for an LED company at Qatar for one year and half. His current research interests is about smart energy harvesting systems and power management for biomedical implantable devices and lab-on-chip systems. He is interested in the thermal impact of the implantable devices on the human tissues. He is interested in embedded system design for lab-on-chip system. He is also interested in the investigation of fractional circuits and systems, specifically in fractional order analog filters for signal processing and fractional order modelling for biomedical applications.



Dorian Hacı (S'15) received the B.Sc. degree in electronic engineering from the Polytechnic University of Turin, Italy, and the M.Sc. degree in electronic engineering, specializing in communication systems, from the Polytechnic University of Turin, in 2014. He is currently pursuing the Ph.D. degree at Imperial College London. He was awarded a scholarship for developing his M.Sc. thesis Project at Imperial College London, where he designed and implemented an innovative thermally controlled system for bio-applications using low cost PCB technology. He

joined the Next Generation Neural Interfaces Group, Centre for Bio-Inspired Technology, Imperial College London, as a Research Assistant, in 2015. His research interests include neural interfaces, biomedical circuit and systems, implantable medical devices and intrabody communication systems.



Hubin Zhao (S'12–M'16) received the Ph.D. degree in bio-electronics from Newcastle University, U.K., in 2016. He received the Best Paper Award from the IEEE conference on BioCAS 2014. He was the Chair of the IEEE Newcastle University Student Branch from 2014 to 2016 and is the mentor of the IEEE NCL SB from 2016 to 2017. He is currently a Post-Doctoral Research Associate and a Guest Lecturer with the University College London, U.K. He is also with the neoLAB, Cambridge University, U.K. His research interests mainly include brain-computer

interface, implantable and wearable electronics, biomedical circuits and neural interface, and advanced opto-electronic technology.



Dimitris Firfilionis received the M.Eng. degree in Electronics and Computer Engineering from Newcastle University, Newcastle upon Tyne, U.K., in 2016. He is currently a Research Assistant at Newcastle University, working on embedded systems and system integration. He is also working toward the Ph.D. degree in electrical and electronic engineering with Newcastle University. His current interest is the design of low power, low noise and chronically implantable biomedical devices.



Anupam Hazra was born in India in 1976. He received his Ph.D. degree in neuroscience from the University of Houston, Houston, Texas, USA in 2011. His primary research interests include dysregulation of neuronal networks and how it contributes to altered brain functions that lead to epileptic seizures. He is one of the recipients of the American Epilepsy Society predoctoral fellowship award in 2011. Currently, he is holding a senior scientist position in the Institute for Stem Cell Biology and Regenerative Medicine (inStem) in Bangalore, India.



Mark O. Cunningham was born in Newry, Northern Ireland. He received the B.Sc. degree (with honors) in Anatomy and Physiology from Queens University, Belfast, U.K., in 1997, and his Ph.D. degree in Physiology from Bristol University, U.K. in 2001. He has held post-doctoral research positions at Bristol University, University of Leeds, Heidelberg University, and Newcastle University, U.K. He was appointed as a RCUK Academic Fellow at Newcastle University in 2007. He is currently Professor of Neuronal Dynamics at the Institute of Neuroscience,

Newcastle University. He is also an honorary clinical research fellow in the Department of Neurophysiology, Royal Victoria Infirmary, Newcastle. His research interests cover neuronal oscillations in health and disease, with over 50 publications. Prof. Cunningham is a Fellow of the Centre for the Advancement of Sustainable Medical Innovation (CASMI), U.K.



Andy Jackson received the M.Phys. degree in physics from Oxford University, UK, in 1998 and the Ph.D. degree in neuroscience from University College, London U.K., in 2002. He is currently a Wellcome Trust Senior Research Fellow and Professor of Neural Interfaces at the Institute of Neuroscience, Newcastle University, UK. His scientific interests include the neural mechanisms of motor control, spinal cord physiology, oscillations and cortical plasticity. This basic research informs the development of neural prosthetics technology for

stroke, spinal cord injury and epilepsy. He is a graduate member of the Institute of Physics and a member of the Society for Neuroscience.



Timothy G. Constantinou (AM'98–M'01–SM'10) received the B.Eng. and Ph.D. degrees in electronic engineering from Imperial College London, in 2001 and 2005, respectively. He is currently a Reader of Neural Microsystems within the Circuits and Systems Group, Department of Electrical and Electronic Engineering at Imperial College London and also the Deputy Director of the Centre for Bio-Inspired Technology. His current research interests include neural microsystems, neural prosthetics, brain machine interfaces, implantable devices, and low-

power microelectronics. He is a fellow of the IET, a chartered engineer, and member of the IoP. Within the IEEE, he serves on several committees/panels, regularly contributing to conference organization, technical activities, and governance. He chairs the IEEE Sensory Systems Technical Committee, is a member of the IEEE BioCAS Technical Committee, IEEE Brain Initiative Steering Committee, and serves on the IEEE Circuits and Systems Society Board of Governors for the term 2017–2019. He was the technical program Co-Chair of the 2010, 2011 and 2018 IEEE BioCAS conferences, General Chair of the BrainCAS 2016 and NeuroCAS 2018 workshops, Special Session Co-Chair of the 2017 IEEE ISCAS Conference, and Demonstrations Co-Chair of the 2017 BioCAS Conference. He is currently an Associate Editor of the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS.



Patrick Degenaar (SM'15) received a first class (Hons.) degree in applied physics and an M.Res. Degree in surface science from Liverpool University, Liverpool, U.K., in 1996 and 1997, respectively. After a short period as a medical engineering technician, in Northern Ireland, he went on study a Ph.D. in the Japan Advanced Institute of Science and Technology, which was completed in 2001. After another period in the software Industry in the Netherlands, he joined Imperial College, London as a post-doctoral fellow in 2002. In 2005, he received an RCUK Fellowship and was promoted to a junior lecturer position. He was further promoted to a senior lectureship before Departing to join Newcastle University in 2010, where he was promoted to Reader (associate professor) in biomedical engineering. His primary research interests as an academic lie with developing optogenetic forms of prosthetics, and in particular visual prosthetics. Between 2010-2014 Dr Degenaar was the coordinator of the OptoNeuro FP7 project. Since then, he has been the engineering workpackage leader of the flagship CANDO project in clinical biomedical engineering.