Enhancement of Fault Current Contribution from Inverter-Based Resources

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ABSTRACT

The reduction in levels of fault current infeed as inverter-based resources (IBR) displace synchronous machines undermines the ability of a conventional protection system to identify and isolate faults in an effective manner and is therefore a concern for system operators (SOs). This observation provided the motivation to investigate the limitations of IBRs when injecting fault current and to explore how these limitations might be overcome.

This thesis investigates techniques aimed at significantly increasing Fault Current Contribution (FCC) from an IBR system so that renewable energy resources can continue to be deployed without compromising the protection system. The techniques for enhancing FCC are at three different levels of an IBR system: at semiconductor or device level, circuit level and system level.

The first study uses phase change materials (PCM) to provide a short-term overload rating to insulated-gate bipolar transistors (IGBTs) and found them to have very limited potential to provide FCC. A Finite Element Analysis (FEA) of heat-flow concluded that, although the PCM was useful for dealing with short over-load currents, it was unsuitable for facilitating large fault currents of several times normal load current. The view was that if the fault current cannot be created at device level through better thermal management, then a circuit level innovation would be required.

The second study investigates series/parallel switching of submodules in modular converters. This takes advantage of the fact that during a fault, the line voltage is reduced, and if it falls below $0.5\ pu$ then half of the sub-modules (SMs) can be put into parallel with the other half to double the FCC $(2\ pu)$ at half the voltage $(0.5\ pu)$. Similarly, if the voltage drops below $0.25\ pu$, parallel connection of four groups of SMs would enable $4\ pu$ current capability. A model of a static synchronous compensator (STATCOM) was developed, inspired by the alternate arm converter (AAC), with the director switch of the AAC used as part of the reconfiguration circuit. The conclusion of this study was that the penalty paid in power losses in the additional semiconductor devices used for reconfiguration is reasonable for the $2\ pu$ FCC case but not at the $4\ pu$ FCC case.

The third study was based on circuit reconfiguration but beyond the converter itself and in this case the windings of the coupling transformer of a STATCOM. Sections of winding were switched using thyristors to tap-change the transformer by a large factor. Using the proposed

thyristor-based electronic tap-changer (eTC), the number of turns of the grid-side winding was reduced during a voltage dip, so that larger current can be delivered to the network for the same converter current. The STATCOM was controlled in the natural frame (abc frame) and this control is used to actively drive the currents in the tap-changer thyristors to zero when needed so that they can be commuted rapidly. The transformer was configured to give a normal ratio of $1{:}\,4$ and be able to tap-down to $1{:}\,2$ and $1{:}\,1$ to increase FCC to $2\ pu$ or $4\ pu$.

Theoretical analysis of, and operating principles for, the proposed eTC, together with their associated control schemes, are verified by time-domain simulation at full-scale. The case-study circuit demonstrates delivery of substantial fault current contribution (FCC) of up to $4\ pu$ at the point of common coupling (PCC) in less than half a cycle $(10\ ms)$ after detection of three- and single-phase faults. The results demonstrate that the proposed eTC is a good candidate for the enhancement of fault current from IBR systems that employ coupling transformers, allowing them thereby to make a contribution to future electricity networks dominated by IBR.

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NOMENCLATURE

ABBREVIATIONS

3LG	Three Line to Ground Fault
AAC	Alternate Arm Converter
AC	Alternate Current
BESS	Battery Energy Storage Scheme
CCT	Critical Clearing Time
CHB	Cascaded H-Bridge
CHP	Combined Heat and Power
DC	Direct Current
DER	Distributed Energy Resource
DNO	Distributed Network Operator
e-OLTC	Electronic OLTC
EA-OLTC	Electronic Assisted OLTC
ESO (NG)	Electricity System Operator (National Grid)
eTC	Electronic Tap Changer
FCC	Fault Current Contribution
FEA	Finite Element Analysis
FL	Fault Level
FLM	Fault Level Management
GTO	Gate Turn-off Thyristors
HVDC	High Voltage Direct Current

IBR	Inverter-Based Resources
IGBT	Integrated Gate Bi-polar Transistor
LCC	Line Commutated Converter
CSC	Current Source Converter
L-L	Line to line fault
LHTES	Latent Heat Thermal Energy Storage
MMC	Modular Multilevel Converter
M-OLTC	Mechanical OLTC
NGESO	National Grid Electricity System Operator
NGET	National Grid Electricity Transmission
OLTC	On-load Tap-changer
PCC	Point of Common Coupling
PCM	Phase Change Material
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
RES	Renewable Energy Resource
SCL	Short-Circuit Level
SCR	Silicon Controlled Rectifier
SDBC	Sigle Delta Bridge Cell
SLG	Single Line to Ground Fault
SOA	Safe Operating Area
SoC	State of Charge
SLG	Single line to ground fault

SMs (HB / FB)	Sub-Modules (Half Bridge / Full bridge)
SDBC	Single Delta Bridge Converter
SSBC	Single Star Bridge Converter
STATCOM	Static Synchronous Compensator
SynCond	Synchronous Condenser (also known as Synchronous Compensator)
TCE	Thermal Conductivity Enhancer
VSC	Voltage Source Converter
VSM	Virtual Synchronous Machine
ZEFAL	Zero Fault Level Generator

NOTATION

GENERAL SUPERSCRIPTS:

1 (positive sequence), 2 (negative sequence), 0 (zero-sequence), A (Phase A), B (Phase B), C (Phase C)

GENERAL SUBSCRIPTS:

C (converter station), $STATCOM$ (STATCOM after reactor), PCC (Point of Common Coupling – after transformer), Y (grid source)

T (transformer), $W1$ (STATCOM side winding), $W2a, W2b, W2c$ & $W2d$ (Grid side winding)

$S2a, S2b$ & $S2d$ (Thyristor based tap-changer switches)

F (fault)

GENERAL QUANTITIES

$*$	Reference
t	Time

Φ	Flux linkage
I	Current
P	Power
V	Voltage
Z	Impedance

SYMBOLS

THERMAL MANAGEMENT FOR CHAPTER 3

A	Area of each assembly part
d	Depth of assembly part
λ	Thermal conductivity of assembly part
P_{Loss}	IGBT power loss
$R_{th(c\text{-}h)}$	Thermal resistance case to heatsink
R_{th}	Thermal resistance
$R_{th(j\text{-}c)}$	Thermal resistance junction to case
$R_{th(metal\text{-}frame)}$	Thermal resistance of the metal frame in the heatsink
$R_{th(PCM)}$	Thermal resistance of the PCM – LM80
$R_{th(h\text{-}walls)}$	Thermal resistance of the heatsink sidewalls
$R_{th(h\text{-}base)}$	Thermal resistance of the heatsink base
$R_{th(base\ to\ water)}$	Thermal resistance of the heat transfers co-efficient - heatsink to water cooling system
T_c	IGBT assembly case temperature

T_j	IGBT junction temperature
$T_{j(\max)}$	IGBT stated maximum junction temperature
$T_{j\ (op)}$	IGBT stated operating junction temperature
T_h	Heatsink surface temperature
T_q	Thyristor's Turn-off Period
T_{water}	Temperature for water cooling system

SERIES/PARALLEL RECONFIGURATION FOR CHAPTER 4

Dir_SW	Director IGBT switch
Par_SW / Par	Parallel IGBT switch

TAP-CHANGER CIRCUIT FOR CHAPTER 5

d	distance
G_{FL}	Grid fault level or short circuit level
I_{arm}	Arm current
I_{CR}	Crow-bar circuit current
I_{PCC}	Current at PCC
I_{phase}	Phase current
I_F	Fault current
I_H	Thyristor's Holding Current
I_Y	Synchronisation machine/generator current
I_S	Tap-changer switch current

I_W	Transformer winding current
L_{arm}	Phase inductance
L_m	Transformer magnetising inductance
L_{phase}	Phase inductance
N	Number of sub-modules per stack
R_F	Fault resistance
R_L	Transmission line resistance
S	Tap-changer switches
V_{phase}	AC-side phase voltage
V_{DC}	DC-side voltage
V_C	Voltage at the converter station
V_{PCC}	PCC voltage
V_G	Grid source voltage
V_{SM}	Sub-module capacitor voltage
$V_{STATCOM}$	STATCOM voltage
V_{stack}	voltage across SM stack
V_Y	Voltage at bus Y
X_L	Transmission line inductance
Z_C	STATCOM reactor impedance
Z_{ERR}	Error in measured apparent impedance
Z_L	Transmission line impedance
Z_W	Transformer winding impedance

Z_Y	Impedance seen from Bus Y
L_{arm}	Phase inductance
L_m	Transformer magnetising inductance
N	Number of sub-module per stack
R_F	Fault resistance
R_L	Transmission line resistance
S	Tap-changer switches
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Z_Y	Impedance seen from Bus Y

CHAPTER 1 INTRODUCTION

To address climate change concerns, there is a drive for clean energy and a zero-carbon future from the United Kingdom (UK), European Union (EU) member states and many other countries. The EU estimates that meeting current European targets in individual sectors would result in an ~80% reduction in overall greenhouse gas emissions by 2050 [1]. The UK government has recently set a stringent target to achieve net-zero electricity by 2035 [2] which requires large volumes of inverter-based resources (IBR) in the form of wind and solar farms, and battery energy storage systems. This transition would mean a 78% reduction in UK territorial emissions between 1990 and 2035. Wind, solar and batteries are not natural $50/60$ Hz synchronous sources and instead rely on power conversion to interface with the grid which is why they are known as IBR.

IBR have seen significant growth in the last decade and their growth rate is expected to be rapid in the coming decades. The Electricity System Operator (ESO) of Great Britain, National Grid ESO (NGESO), expects this growth to continue as shown in their report on Future Energy Scenarios (FES) 2021 [3]. According to this report, the UK network could see a sharp increase in the total number of IBR connected to the grid, estimated at an increase of over 1,000% by end of 2050 as shown in Figure 1-1. For example, between $50\ GW$ and $100\ GW$ of new wind and solar generation could be installed to meet demand by 2030 [4].

Due to the increased penetration of IBR systems, there has been a notable decommissioning of the conventional centralised generation that employs synchronous generators and with them go their speed governors, short-term over-rating and synchronised inertia which provide important system services [5]. The replacement of electro-mechanical machines by IBR is fundamentally changing the dynamics and stability properties of grids such as changing the voltage strength, frequency regulation response and synchronisation characteristics [6]. The expected change in types of power generation and consumption are also a source of uncertainty and complexity in the future grid. These new features and characteristics which have arisen due to the increased integration of IBR has raised many new challenges for modern power systems, and a great deal of research is now needed to find the right technology and system design guidelines to prepare and manage an electrical network with a high penetration of IBR.

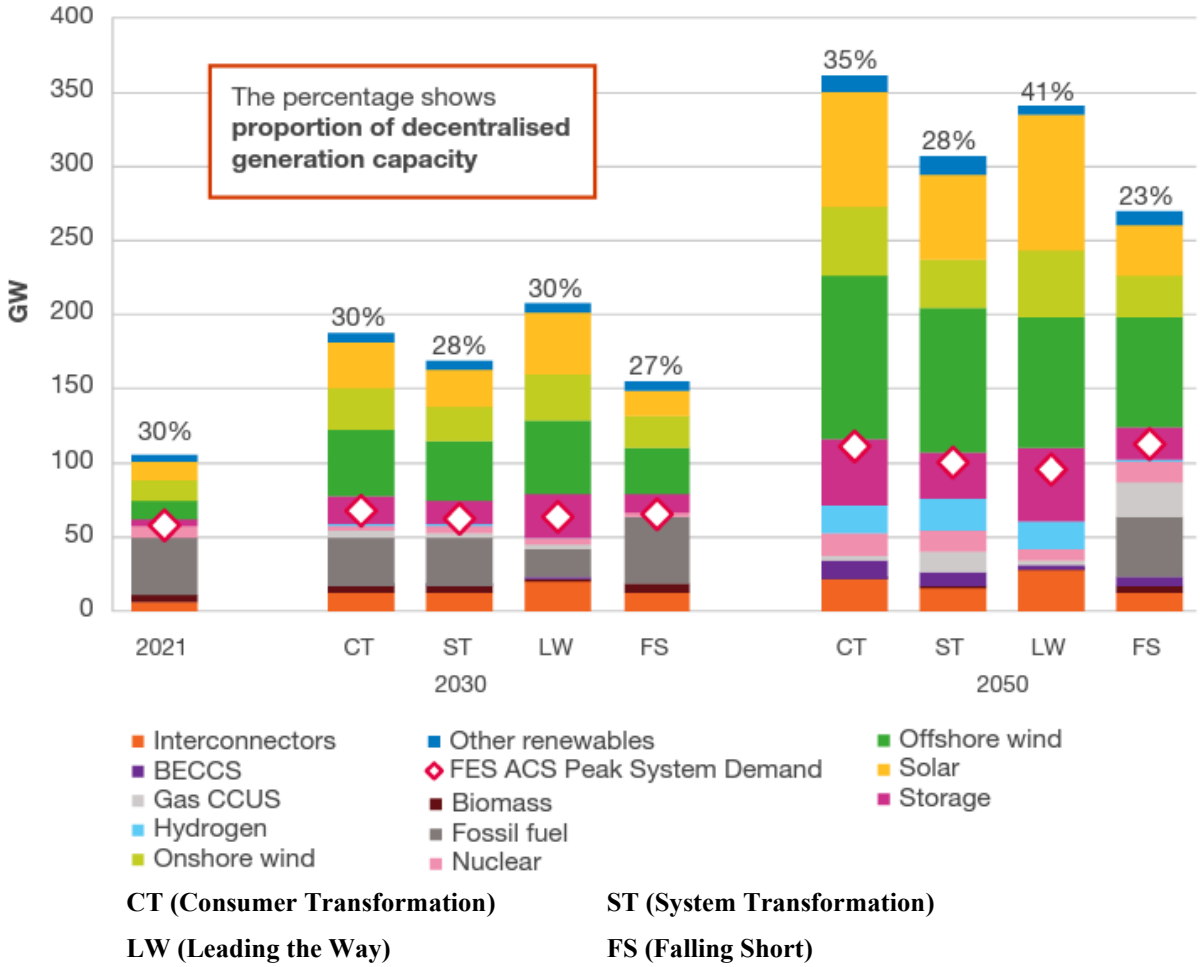


Figure 1-1: Installed electricity generation capacity, plus storage and interconnection [4]

For example, according to NGESO, high penetration of IBR in future grid can have a serious impact on the Short Circuit Level (SCL), also known as the Fault Level (FL) [7]. A reducing level of fault current infeed as IBR displace synchronous machines is a concern for system operators as the magnitude of the fault current is an important parameter in the configuration of protection systems in an electrical network. It determines the ability of the protection system to detect and locate, and subsequently isolate, faults in a reliable and consistent manner. Low SCL not only makes over-current protection impractical but also compromises the integrity of the technique known as distance protection, which is common in transmission grids [8]. Therefore, this thesis aims to investigate methods of designing IBR systems with improved fault current contribution (FCC) such that the existing protection system infrastructure can remain in use or can be readily adapted.

1.1 Short-circuit Level

The short-circuit level (SCL) or Fault level (FL) at a point on the system is defined as the current which would flow in the event of a system short-circuit. The SCL of a point in a network provides some indication of the "electrical proximity" of that point to a low impedance voltage source. There are a number of factors which determine the SCL:

- The volume and characteristics of transmission-connected generation,
- transmission and distribution network configuration (including impedance and substation earthing arrangements),
- direct-online motors (which can supply current during a fault), and
- volume and characteristics of distribution-connected generation.

Figure 1-2 shows that short-circuit FCC for faults in the distribution system is partly infeed from the transmission system and partly contributed from within the distribution system [7]. Similarly, fault current for faults in the transmission system comes partly from within the transmission system and partly as infeed from the distribution system.

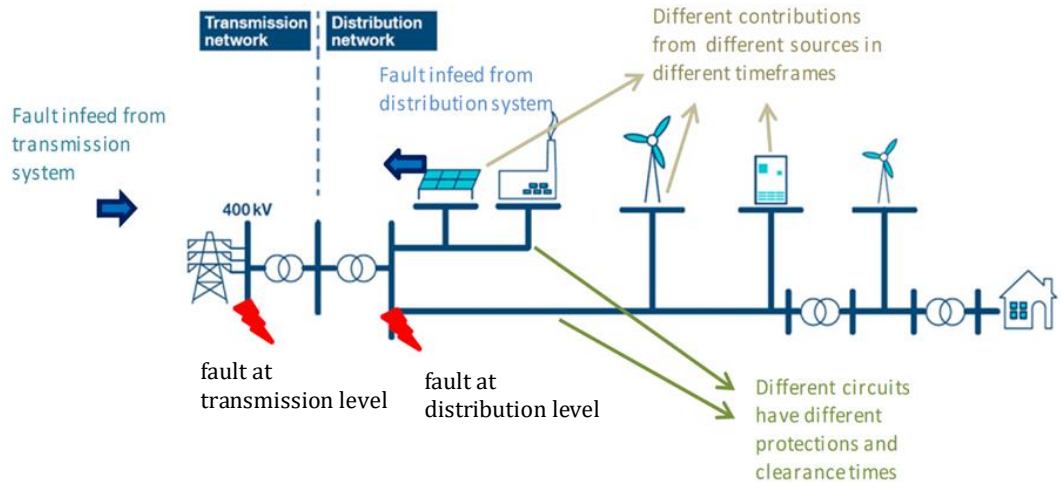


Figure 1-2: View of transmission-distribution fault in-feeds [7]

SCLs at the transmission level are decreasing due to a decreasing number of large synchronous generators and increasing IBR [7].

IBR include on-shore and off-shore wind farms, solar farms, battery energy storage systems (BESS) and High Voltage Direct Current (HVDC) converter stations. Synchronous generators have been the predominant contributors to fault level in electrical networks at the transmission

level [8]. IBR use semiconductor switches with very low thermal inertia and therefore under fault conditions must limit their current. Thus, IBR have a rather small FCC of between 1 and 2 pu. This compares to 5 to 10 pu from synchronous generators [7].

The recent report from NGESO in their System Operability Framework 2019 (SOF) [9], concludes that there are generic impacts of year-round variations in transmission SCL on the distribution networks. The report suggests that the existing IBR are not reliable in providing sustained level of fault current and should not be included as contributing to assessing a minimum current setting for protection operation.

The average rate at which the SCL is set to decline across the four Future Energy Scenarios [9] at transmission level is shown in Figure 1-3. The fault level reaches minimum in 2025 and then subsequently increases as NGESO is expected to add more synchronous machines (i.e. Nuclear Power Plants and Synchronous Condensers) to the Grid. The impact of decline will negatively influence all protection equipment and generators in the electrical network at both transmission and distribution level [8].

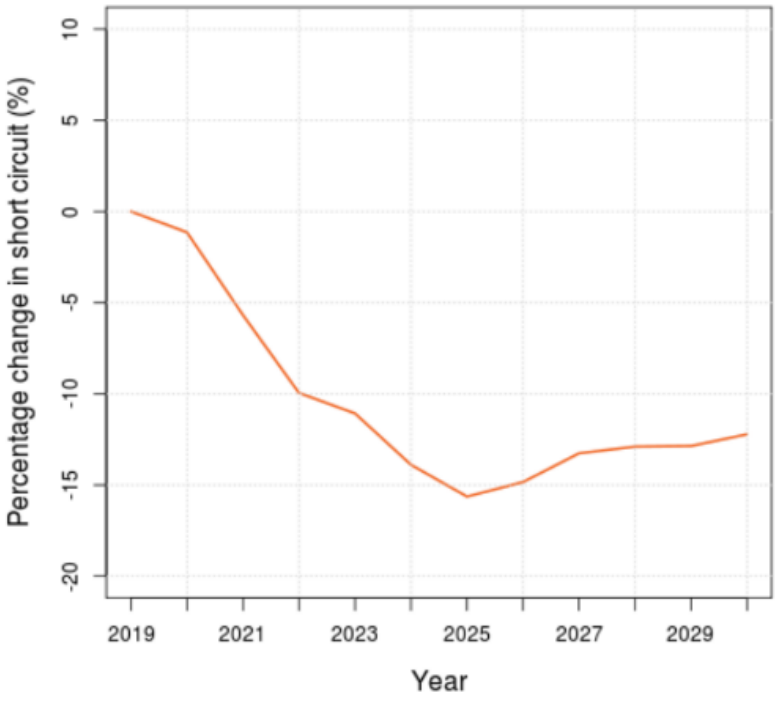


Figure 1-3: Estimated national fault level (2019-2030) [9]

Interestingly, the fault level is declining at thce transmission level but increasing in distribution systems driven by growth in Distributed Energy Resource (DER) [7]. Combined Heat and Power (CHP) plants will normally use synchronous generators; these plants have grown in

number during recent years and are a major cause of increased fault level in distribution networks.

With changing SCL in both transmission and distribution systems, all facets of power systems planning and operations are getting affected [10]. From the perspective of an ESO, these new resources bring challenges. The challenges require a higher level of preparedness for both the ESO and Distributed Network Operator (DNO) so that they can continue to provide cost-effective, resilient and safe networks [6] through a robust Fault Level Management (FLM) system. For example, the "MIGRATE" project, under the framework of European Union's Horizon 2020, focuses on safeguarding grid stability, changes to control functions, and possible adjustments to grid connection requirements [10]. In Norway, the project "ProSmart" aims to improve classical power system relaying by taking advantage of communication technologies [11].

There is also a wider need for FLM for an enhanced understanding of how transmission and distribution networks perform and interact in varying year-round conditions, most importantly in minimum network conditions. The FLM will enable network owners and operators to better understand analysis of minimum network conditions and the impact on minimum fault level both at transmission and distribution level. Power system operators and planners are increasingly realising that fault current analysis needs to play a broader role in operating practices, and in planning policies and decisions.

1.2 Protection Systems

Effective operation of a protection system to deal with occasional equipment faults is key to a safe, reliable and resilient electrical network. Protection systems must detect, locate and isolate faults before safe operation of the grid or the safety of people and assets is compromised. The protection system disconnects affected equipment during fault conditions without compromising the overall operation of the system and to do this a protection co-ordination study establishes how it is ensured that the smallest network portion containing the fault is isolated and that the remaining system is functional to the highest extent possible. The traditional design of a protection system is highly reliant on the flow of substantial current into the low impedance path of a short-circuit or near short-circuit fault, for both detection and location of faults. Increased use of IBR accompanied by retirement of conventional generators

and the resulting reduced fault levels can have a significant impact on protection co-ordination and safety [12].

The protection concept defined for a network must provide protection for each piece of equipment in the network. The main protection scheme protects a set of defined zones in the network, and these have overlapping protection at the interfaces to avoid creation of blind spots in the detection and location aspects. Isolation of faults is achieved through fast acting circuit breakers. The combination of operating times of the detection, location, and isolation aspects is known as the fault clearance time. In the event of a fault not being cleared by the main protection scheme (because of malfunction or inadvertent blind spot), a back-up protection is activated within a specific timeframe. The back-up protection scheme provides a separate arrangement, possessing its own instrument transformers, relays and perhaps also circuit breakers, to isolate the faulty and perhaps a wider region of the network [13].

Changes to SCL in distribution and transmission networks can have a serious impact on protection systems. Very high SCL could cause overstressing of equipment, in particular circuit breakers, or disruptive failure of electricity network assets. Over-stressed switchgear and networks can lead to significant damage resulting in high repair costs, unplanned network outages or safety violations for switchgear operators and the public.

DNOs and TOs have traditionally designed networks with high fault levels so that protection relays can distinguish readily between a high but normal load current and a fault current. If the SCL is low then over-current protection relays, which are the mainstay of protection in distribution networks, will not be able to distinguish between a high load current and a relatively low short-circuit current. This would lead to failure to clear a fault if the trip level is set to high [12] or nuisance tripping if it is set to low. Distance protection relays are a more sophisticated fault location device common in transmission networks in which the distance to the fault is determined, implicitly, by estimating the impedance as the ratio of the voltage to current measured by the protection relays at the ends of the line. If a line has a high fault current infeed from one end but low at the other, the voltage drop across the fault itself caused by the two fault current contributions disproportionately distorts the impedance estimation at the low fault current end and causes maloperation of protection relays [14]. The challenges associated with distance relays will be explored further in Section 2.1.

Further work is required to understand the magnitude of fault current required by the different types of protection relays that are utilised in the network. For example, a distance relay may only require $2pu$ fault current whereas an overcurrent relay may require $5\ pu$.

At low IBR penetration levels (e.g., below 10% of system capacity), conventional protection methods may be adequate. However, at high penetration levels (e.g. exceeding 50% in a region), new guidelines may be necessary. NGESO is currently undertaking industry-wide consultation to address this issue [9]. The regulatory changes will need to ensure the protection systems work effectively to limit the effects of fault level and create a safe and resilient network operation in a low carbon electrical network.

1.3 Motivations and Challenges for Enhancement of Fault Current from IBR

Network operators are facing an interesting conundrum; sometimes a high fault current value above the opening current limit of the breakers is observed [15], while at other times the fault current is low and circuit breakers are unable to distinguish between a load and fault current [16]. There are interesting questions on how to limit and generate fault current. As explained in Section 1.1, both rising and falling SCL can adversely impact the reliable functioning of a network protection system. If appropriate steps are not taken to address both scenarios of high and low fault current, it could potentially compromise the electrical network resilience. There is wider need for FLM for an enhanced understanding of how transmission and distribution networks perform and interact in varying year-round conditions, most importantly, in low fault level conditions.

There has been lot of focus in literature and development of new devices aimed at distribution systems. For example, UK Power Networks is developing and trialling a new fault limiting circuit breaker from ABB [17]. This device is an “hybrid circuit-breaker” that is significantly smaller and more efficient than any similar device currently in use. This project will enable increased capacity for distribution generation, especially CHP units, to connect to the network as low-carbon electricity sources.

With high penetration of IBR systems in grids, new technologies are required to enable the existing and future electrical network operators to inject additional fault current into the network during low fault level conditions. By enhancing the FCC from the IBR systems, it may enable the traditional protection systems to work effectively and reliably with little or no

changes. If this cannot be achieved, then extra network equipment especially to inject fault current or a widespread redesign and reequipping of the protection system would be needed and both of these options could be very costly. This observation provided the motivation to explore the limitations on IBR to inject increased fault current, and how these limitations might be overcome.

The fundamental questions being asked in this thesis are: what are the key factors that limit the FCC capability of an IBR, and whether through innovation in semiconductor devices through better thermal management, or innovation in inverter circuits or through ancillary devices around inverters, increased FCC could be achieved.

1.4 Research Questions

This thesis addresses the following specific research questions.

1. To what extent can improved thermal management techniques at the semiconductor device level increase the ability of a device to carry additional current in the short term?
2. Can the modular multilevel technologies that have proved very successful in high-power converters be adapted through series-parallel reconfiguration to supply additional current during grid faults?
3. Can the combination of an IBR system and its ancillary devices, such as an isolating transformer, be modified to supply increased fault current?
4. How do the three approaches, at component, circuit and system level, compare in their ability to enhance fault current and compare in terms of cost, density and efficiency?

These questions will be addressed through a three-step process that is applied to a variety of circuit topologies that are known from the literature or were created when looking for new applications. The three steps are (i) to analyse the circuits to establish the operating principles and the size of the principal components, (ii) to simulate the circuits at the power ratings envisaged for practical use and to verify the operating principles and (iii) to consider the advantages and disadvantages of the proposed approach.

1.5 Thesis Structure

Chapter 2 provides a review of the relevant background and literature. This chapter will review the literature for thermal management techniques of semiconductor-based switching devices,

operation and design of the multilevel converter topologies and tap-change circuit of a transformer.

Chapter 3 assesses the thermal management of an insulated-gate bipolar transistor (IGBT) for short-term increase of current capability. The thermal network for applied heat distribution techniques is derived. Simulation results demonstrate the increased current capability though efficient thermal management.

Chapter 4 proposes an adapted Modular Multilevel Converter (MMC) topology which can provide increased FCC without significantly compromising the converter efficiency. Operating principles are discussed, and simulation results are shown for validation.

Chapter 5 proposes a tap-changer with a large change in turns-ratio to be added to the interface transformer of an inverter to provide FCC of up to 4 pu. The design trade-offs are investigated, and simulation results of the arrangement applied to a STATCOM are presented for validation.

Chapter 6 provides a summary of the results and conclusions as well as providing suggestions for further work.

1.6 Author's contribution

The original contributions made in this thesis has been described fully in the conclusions in Chapter 6 but are previewed here.

Chapter 3 introduces the Phase Change Material (PCM) for thermal management. The concept of using PCM is not novel and can be found in the literature for use in industrial and consumer products and more recently for mobile phone applications. However, the implementation of PCM with a purpose designed metal frame in the heatsink of an IGBT for thermal management is an original contribution by the author.

Chapter 4 presents a series/parallel reconfiguration circuit in an Alternate Arm Converter (AAC) topology. AAC converter topology is widely seen in the literature, however, the consideration of using the director switch to support series/parallel reconfiguration circuit is original.

Chapter 5 proposed an innovative thyristor-based electronic tap changer (eTC) circuit. The eTC used to create large turns-ratio in the grid connecting transformer during a voltage dip, so that larger current can be delivered to the network for the same converter current is a novel

contribution. Theoretical analysis of, and operating principles for, the proposed eTC, together with their associated control schemes, are verified by time-domain simulation at full-scale. The circuit itself as well as the corresponding analysis and simulation results are original contributions.

1.7 Author's Publications Based on This Work

1.7.1 Conference Papers

N. P. Singh, C. T. Collins and T. C. Green, "Fast fault current VIA STATCOM with electronic tap-changer," *16th International Conference on Developments in Power System Protection (DPSP 2022)*, 2022, pp. 49-54, doi: 10.1049/icp.2022.0910.

CHAPTER 2 BACKGROUND AND LITERATURE REVIEW

In Chapter 1 it was noted that the reducing levels of fault current infeed as IBR displace synchronous machines are a concern for ESOs. During a fault, it is desired that IBR not only remain connected but also provide fault current, ideally comparable to that of a conventional synchronous machine (5-10 pu), for at least the time taken for effective operation of protection systems, and subsequently support voltage recovery after fault clearance [7][18]. However, in the case of IBR, providing the capacity to deliver a large short-circuit current requires larger semiconductor devices than those present for normal load current, and this would be a substantial increase in capital cost. Such a large cost is hard to justify and so this option is not taken. If it were to become a strict requirement to provide large short-circuit currents, then new approaches should be sought that avoid the high cost of simply uprating the semiconductors.

In Section 1.2 the need was identified to maintain substantial fault current to support the existing protection systems, in particular the distance protection. Section 2.1 will explore the magnitude of fault current required from an IBR and how quickly that needs to be delivered in order for the protection system to operate effectively and reliably. These two requirements placed on the fault current will help define the problem for rest of the thesis.

Section 1.4 set out three possible approaches which will be examined in subsequent chapters as follows:

1. Thermal management techniques of switching devices, which relates to more efficient cooling via phase change dispersions, to be studied in Chapter 3,
2. MMC technologies, in particular AAC type, to be studied in Chapter 4,
3. tap-change circuit of a transformer, to be studied in Chapter 5.

The later part of this Chapter sets out the background material and literature on these topics.

2.1 Protection Relays and Total Fault Clearance Times

The role of a protection system is to detect and locate power system faults or abnormal conditions and to isolate such faults or end abnormal operating conditions through the use of circuit breakers. There is a need for a grading of responses so that faults in the highest voltage levels, with the most customers affected, are cleared fastest but faults in lower voltage levels,

affecting fewer customers are cleared a little more slowly to allow for possible action in the high voltage network first. Another grading consideration is that a fault that does not clear as intended is cleared by action of some secondary protection provision that acts a little later and on a wider region of the network.

A common consideration for how fast a fault should be cleared is the risk of a synchronous generator losing synchronism [13]. During a short-circuit fault, a synchronous generator close to the fault accelerates because it cannot export power and if its speed and angle are allowed to deviate too far it may not recover and regain synchronism after the fault clears. This is termed transient stability. Thus, a critical clearing time (CCT) is defined for faults and is, in a traditional network, defined by the characteristic of synchronous generator such as its inertia [8]. The behaviour of IBR during fault conditions is significantly different to synchronous generators, as discussed for example in [19] and depends on its controller design (grid-forming or grid-following). Therefore, with an increase in IBR penetration in the generation mix, a synchronous generator may no longer be the critical factor used to determine the CCT in future grids.

CCT defines the maximum duration of a short circuit on a power network before it has to be removed by action of protection mechanism to allow the system to regain synchronisation once the fault is cleared [20]. It is important to note that this is a co-design issue, not only does the CCT define the necessary speed of operation of the relays circuit breaker depending on typical generator characteristics but when a system wide CCT has been defined for the protection, all generators, and especially new connections, must be suitable for faults of that duration. The operating time of protection equipment can potentially be influenced by a range of factors including fault location, fault type, X/R ratio, fault current, and protection settings. The recommended CCT duration is $150\,ms$ for a network with no redundancy ("N" state) and $120\,ms$ for a network with N-1 situation [21].

The target fault interruption times in UK transmission systems for main in-feeding circuits for different voltage levels are shown in Table 2-1 [22]. The times set out in Table 2-1 are crosschecked directly against the effective fault clearing time of the protection system, which is central to maintaining transient stability on the transmission system. This effective fault clearing time is detailed in the following subsection.

Table 2-1: Target critical clearing time requirements [22]

Nominal Voltage (kV)	Target fault interruption time of main in-feeding circuit (ms)
400	80
275	100
132	120
66	120

2.1.1 Fault Clearance Time

Total time taken to clear a fault will be the sum of the operating time of a number of pieces of equipment that operate in sequence. This includes the following items which will be discussed in the subsections that follow; relay operating times, trip relay operating times, inter-trip operating times and circuit breaker interruption times, all of which apply at both ends of the circuit element that needs to be isolated. The fault clearance time shown in Figure 2-1, is the time between the fault inception and the moment when fault current is cleared, and comprises the relay operating time, trip relay time and circuit breaker interrupting time.

2.1.1.1 Relay Operating Times

The relay operating time is the time taken by the instrumentation transformers to provide signals and for a relay (electromechanical or software) to process the signals, make decision and generate a signal to trigger the circuit breaker to interrupt the current. The relay operation time is influenced by many factors including the protection algorithm type, hardware and software limitations, accuracy of measurement chain and a number of external factors such as fault inception angle, fault location, power flow and fault resistance [23].

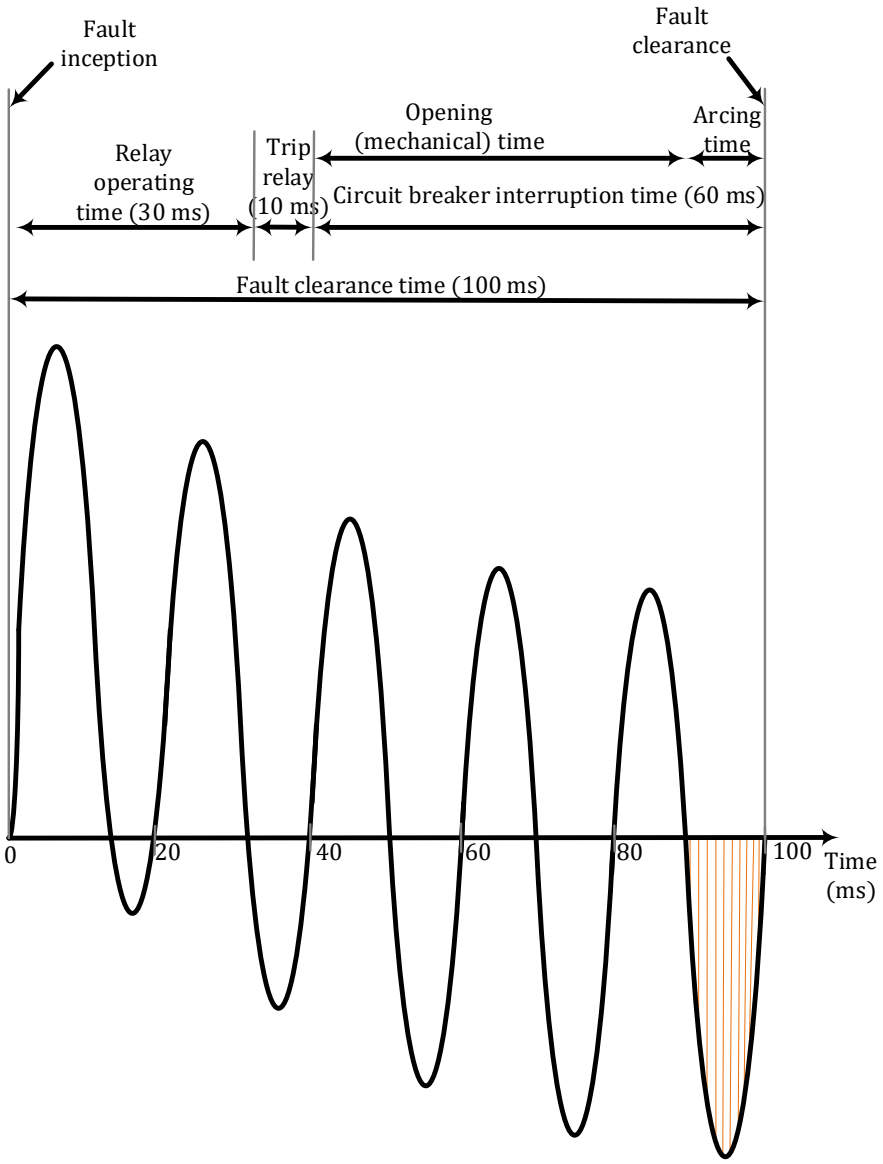


Figure 2-1: Definition of fault clearing time, relay operate time, trip relay time and circuit breaker interrupting time for fault current [23]

2.1.1.2 Trip Relay Operating Times

Trip relays provide suitable contact for the switching of circuit breakers and other equipment. Trip relays have a nominal operating time of 10 ms.

2.1.1.3 Inter-trip Operating Times

Protection schemes, such as distance protection, may be formed by a number of relays located remotely from each other. A communication between distantly located relays is called protection signalling and when protection signalling is used for remote operation of a circuit

breaker, it is known as inter-tripping, to disconnect that part of the circuit due to fault or abnormal conditions. The inter-trip operating time is the duration of flow of these protection signals or communication messages which may involve defined action (trip, block, etc) [24]. For a transmission line, private pilot wires installed by the power authority is the most common type of communication links. Other form of communication includes radio channels at ultra-high frequencies such as optical fibres [24].

2.1.1.4 Circuit Breaker Opening Times

The circuit breaker interrupting time for a circuit breaker is calculated from the receipt of an open signal after detection of a fault, until the end of the arcing time. When the contacts part, current continues to flow until the arcing within the circuit breaker has been quenched to successful interruption at a fault current zero-crossing [23].

The following example in Table 2-2 demonstrates the determination of fault clearance times for substation A. The duration mentioned in Table 2-2 are taken from an existing National Grid Electricity Transmission (NGET) substation but for the security purposes the substation name has not been stated. The operating duration information has been received via private correspondence. This example does not consider the inter-trip operating times and assumes the fault location to be close to substation A (275 kV).

As seen from Table 2-2, the slowest fault clearance at Substation A occurs when the 2nd Main distance protection fails to operate, and the fault is cleared by the 1st Main unit protection.

In the example shown in Table 2-2, the individual relay operating times generally have 1-2 cycle to detect the fault. This would imply that the fault current needs to be present within the first half cycle ($10\ ms$) of the fault to support the fault detection. This thesis will investigate the feasibility of injecting increased fault current within the first cycle of the fault.

Table 2-2: Example Case Details the methodology involved in determining the fault clearance times

Site	Substation A	
Protection type	1st Main – Unit protection scheme	2nd Main – Distance protection scheme
Individual relay operating times	30 ms	25 ms (Zone 1)
Trip relay	10 ms	10 ms
Protection signalling/inter-trip	N/A	N/A
Circuit breaker interruption time	60 ms	60 ms
Total	100 ms	95 ms

2.1.2 Challenges with Distance Protection

The relatively simple to use distance relays has served as both primary and secondary (back-up) protection for transmission lines for more than a century. Distance protection schemes have several relays and associated equipment to provide protection covering more than one zone. The underlaying principle of distance protection is that the impedance of a transmission circuit is proportional to its length. A distance relay can measure the impedance of a circuit with inputs derived from voltage transformers and current transformers. If a fault occurs on the line being protected, the impedance will drop to a value determined by the distance to the fault. This can be used to assess whether or not the fault is in the zone that is to be protected by that relay [13].

Traditional distance protection techniques plot the measured impedance on the complex plane $(R + jX)$. In a perfect case, the measured impedance would lie on the line determined by the angle of the line impedance. As errors are to be expected, a region is defined and if the measured impedance lies in the region, then an in-zone fault is declared. This region is known as a mho region. With early electro-mechanical relays, it was convenient to define a circular area [25]. In modern processor-based relays, any shape could be used and a quadrilateral mho,

that allows for large errors in the resistive term, are common as shown in Figure 2-2. An impedance function with a quadrilateral characteristic involves the implementation of the following [26].

1. Reactance element determines the impedance "reach",
2. two resistance elements determine the resistive coverage of the fault on the left- and right-hand sides,
3. a directional element that detects whether the faults in the forward direction (along the line rather than behind the relay on a different line).

A distance element uses the local voltages and currents to respond to faults located within its predetermined reach set by the user for protection of short-circuits on the protected line [27].

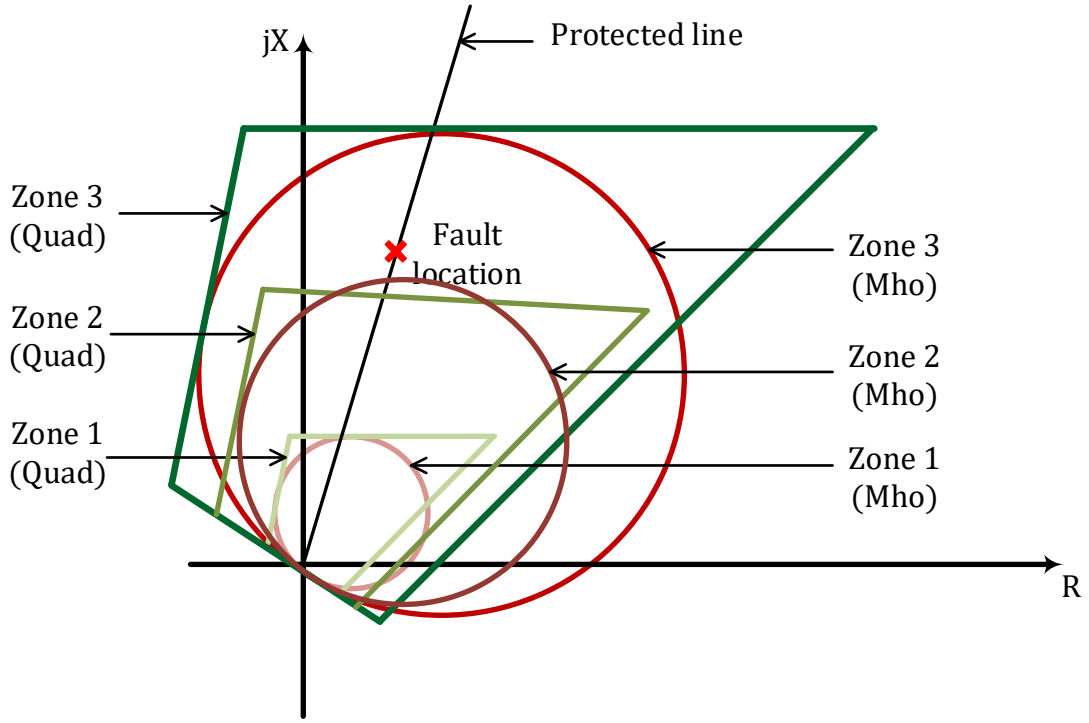


Figure 2-2: Typical circular and quadrilateral mho regions for different zones [26]

A typical microprocessor-based distance protection scheme is provided with three independent zones of protection, normal termed Zone 1, Zone 2 and Zone 3. Each protection zone is responsive to all types of short-circuit fault (symmetric and asymmetric) located within its "reach". Algorithms are employed to detect each type of line-to-line fault and each type of line-to-earth fault simultaneously. During load encroachment conditions the quadrilateral settings

can adopted for proper discrimination, but this is not possible for relays with Mho characteristics [26].

The literature contains several reports of the difficulties posed to distance protection relays by the presence of an IBR, for example, incorrect zone selection [28]-[29] or phase selection [30][31] resulting in incorrect functioning of directional elements. To understand why an IBR may cause difficulties for distance protection, one should consider how they differ from synchronous generators. IBR systems have control loops which control fault currents to a predetermined magnitude and angle which is different to synchronous generators [32] and they have a strict current rating meaning that they can only supply a limited amount of fault current [33].

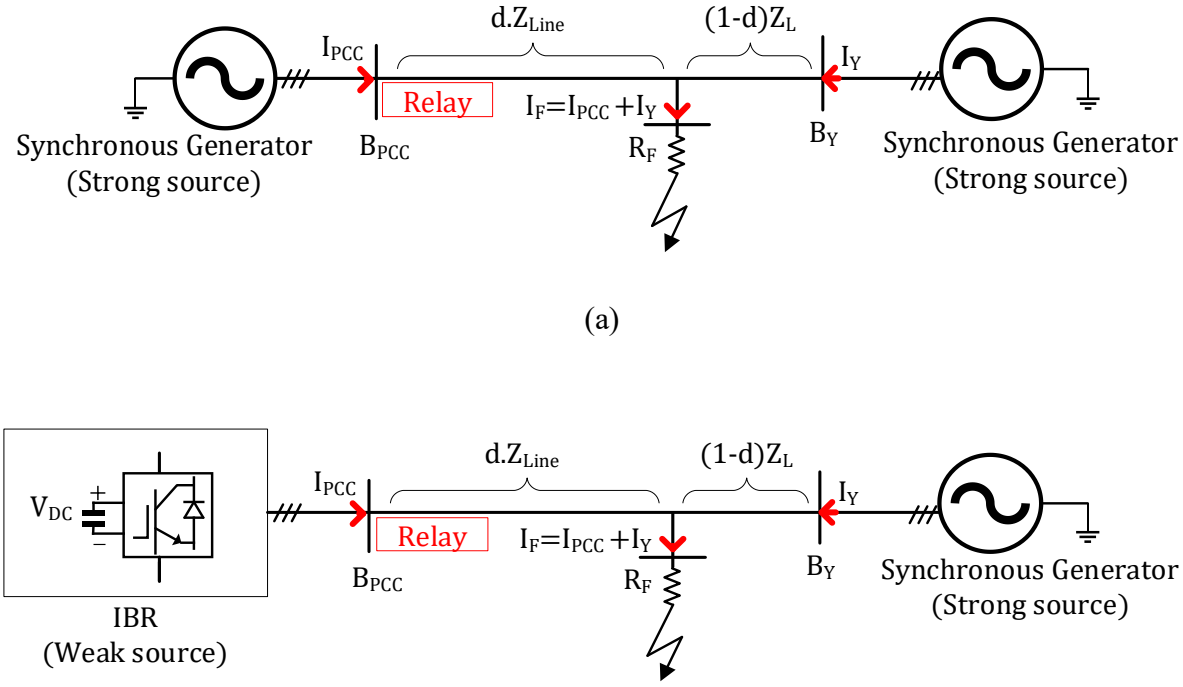


Figure 2-3: Resistive fault midway on the transmission line (a) for network with two synchronous generators (b) for network with IBR and synchronous generator

Figure 2-3 shows a line between two buses in a system with generators at both ends and a low impedance resistive fault (R_F) part way, d, along the line. Part (a) illustrates two synchronous machines and part (b) illustrates one IBR and one synchronous machine. In Figure 2-3 (a), the fault current contribution from one synchronous machine is I_Y and the other synchronous machine (on the left) is I_{PCC} (the point of common coupling, PCC

is where the equipment being studied will be placed). In Figure 2-3 (b), the fault current contribution from the synchronous machine is I_Y and from the IBR is I_{PCC}. The total fault current through the fault resistor is sum of fault current from each end ($I_F = I_{PCC} + I_Y$). The relay in Figure 2-3 at the PCC end measures an apparent impedance (Z_{APP}) as follows.

$$Z_{APP} = \frac{V_{PCC}}{I_{PCC}} = \frac{I_{PCC}\, d\, Z_{Line} + (I_{PCC} + I_Y)R_F}{I_{PCC}} \qquad \textbf{(2.1)}$$
$$= d\ Z_{Line} + R_F(1 + \frac{I_Y}{I_{PCC}})$$

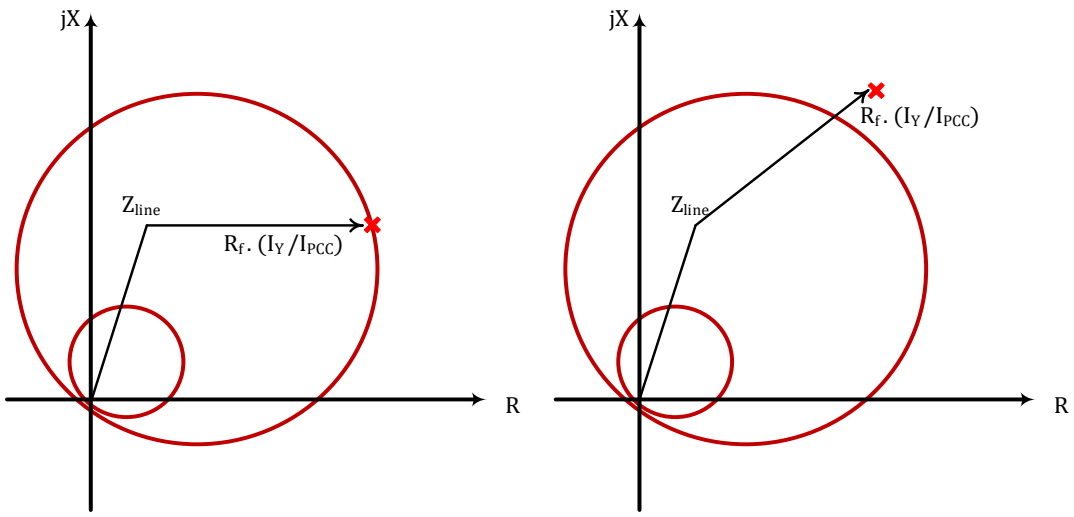
For protection purposes, we wish to accurately identify the term $d\, Z_{line}$. The measured apparent impedance includes an error component (Z_{ERR}) proportional to the product of fault impedance R_F and the ratio of the fault current contribution from the remote and local sources. This Z_{ERR} is given by:

$$Z_{ERR} = R_F\left(1 + \frac{I_Y}{I_{PCC}}\right) = R_F + R_F\frac{I_Y}{I_{PCC}} \qquad \textbf{(2.2)}$$

In a traditional network, the error component is relatively small because

1. R_F is small compared to the line impedance for most faults,
2. the sources at the two ends of a transmission line can provide similar magnitudes of fault current (typically 5-10 pu) such that $I_{PCC} \approx I_Y$ and,
3. the angle of the fault current provided by the sources are similar (being driven by voltage of similar phase angle through impedances of similar angle) such that the error impedance will be predominantly resistive and relatively straightforward to discount by extending a quadrilateral mho region in the resistive direction.

As a result, the measurement of fault is expected to be within the mho region of the distance relays as shown in Figure 2-4 (a).



(a) $I_Y \approx I_{PCC}$ (b) $I_Y \gg I_{PCC}$ with angle difference

Figure 2-4: Apparent impedance for the line faults when (a) $I_Y \approx I_{PCC}$ for a transmission line with a synchronous generator on two ends (b) $I_Y \gg I_{PCC}$ for transmission with a current-limited IBR on one end and synchronous generator on the other end.

During the fault in a network with an IBR, the fault current contribution from the local IBR source is weak, limited to $1\,pu$ or a little above because of the thermal limitation of the semiconductor devices which is a lot less than from a strong source (5-$10\,pu$). Thus, the magnitude of the ratio of the two currents will be considerably greater than 1. Furthermore, the IBR when current limiting acts as a current source where the angle of current injection is set by the control scheme and may be quite different to the current from a synchronous generator. The error impedance can thus be large and have a substantial reactive part and when added to the line impedance may falsely give a line impedance outside the mho of the distance relays as shown in Fig 2 (b). This would cause miss operation of the distance relay and/or a failure to operate the circuit breaker. It is fair to say that where one end of a line produces much lower fault current than the other end and at a different angle, distance protection may be difficult to configure to achieve reliably accurate operation.

2.1.2.1 Available techniques for distance protection

In the literature, various techniques have been presented to enhance distance protection relays to improve impedance estimation for fault location in a network with high penetration of IBR. Some of these are reviewed below.

1. Redesign the mho characteristic region

Advances have been made in shaping mho regions to improve fault location. Distance protection systems typically apply a reliable angle reference for directional discrimination, and this has been particularly helpful in shaping of mho regions. However, a mho distance relay element may fail to operate when providing discrimination between close-in forward and close-in reverse faults, when the relay voltage reaches or becomes close to zero [27]. The study in [27] shows that when the fault is very close to the relay, the voltage will be very small and cannot be accurately measured.

In [34] a pre-fault positive sequence voltage is used to dynamically change the quadrilateral characteristics and provide additional resistance coverage. With the help of microprocessors. protection engineers have been able to dynamically change the quadrilateral characteristics to provide adaptive distance protection as shown in Figure 2-5.

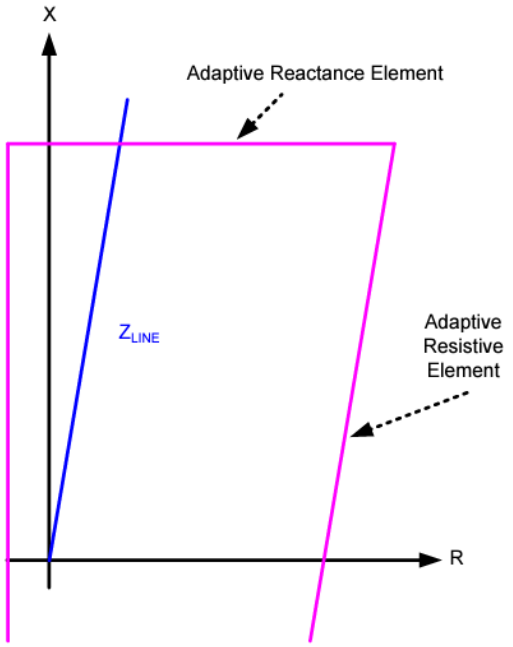


Figure 2-5: Quadrilateral distance element characteristics with adaptive reactance and resistance elements [35]

The adaptive scheme in [35] changes quadrilateral distance element characteristics based on the direction of the load flow and the resistance element. Most of such schemes in the literature, including the study in [35], are developed considering the system to be homogeneous, which is not true in the presence of an IBR. The adaptive technique in [37] showed limited performance for faults with high fault resistances. The adaptive distance scheme in [38] uses available communication facilities and the data concentrator of Phasor Measurement Units which suffers from latency that delays the decision taken by such schemes using remote end real-time data during faults.

The single-end distance relay measurement-based methods are simple and cost effective, their accuracy might be affected by current infeed and fault and network parameters. In a large, meshed network, estimating the impedance would require extensive computation and would cause further delay.

Moreover, many of the existing distance protection relays are traditional electromechanical devices with circular mho fault detection [27] and it would require significant capital to replace the electromechanical systems with microprocessors.

2. Communication-assisted tripping schemes

Communication-assisted tripping schemes are found to provide accelerated protection at two ends, which use either a zone-1 or zone-2 decision of distance relay. Schemes using zone-1 based decisions show limited performance for high resistance faults and system non-homogeneity [39]. Zone-2 covers a large area, therefore decisions by zone-2 are vulnerable to load encroachment and power swing [39]. Moreover, communication latency may delay the decision taken by such schemes using remote end real-time data during a fault and this presents a significant security and dependability issue.

3. Differential relays

Line differential relays operate on the difference between the current into one end of a line and the current out of the other end. Such a scheme requires synchronized real-time data from two of the ends, and the performance gets affected in case of current transformer saturation [40]. NGET has started implementing two sets of differential relays - one on each end of the transmission line and distance protection is then used as a back-up protection. This is confirmed through private communication. However, having three protection schemes on a single transmission line would become extremely costly.

4. Changes to IBR fault response

The equation (2.2) shows that the error in impedance measurement can be made resistive by aligning the angle at which the fault current is injected to the grid current from the other end. A resistive error can be mitigated by careful choice of mho shape. This approach requires enhancing the fault current response from the IBR. The literature records two possible ways forward in terms of fault current angle and magnitude, as described below.

The IBR control system could also utilise a reference angle determined by the pre-fault voltage and inject fault current at a chosen angle relative to that reference angle, but to maintain an accurate angle relative to pre-fault conditions the IBR must have an accurate measurement of the frequency. If the distance element uses the pre-fault voltage angle and extrapolates it using pre-fault frequency but the IBR operates at a somewhat different frequency to the pre-fault frequency, then the angle of injection, gradually becomes inaccurate with the passing of time [8].

The control strategy proposed in [32] utilises the reference current and current controller to generate balanced positive sequence currents and to make the angle of that current similar to that produced by a synchronous generator operating into a typical fault. This is expected to make the fault current contribution from the two ends of the line consistent in terms of angle and thus the error term, Z_{ERR}, in the measured impedance is resistive only, resulting from the resistance of the fault itself. A quadrilateral mho that extends widely in the resistive direction will ignore this error and avoids "under-reach" in which the distance relays fail to operate for faults within their intended reach. The same authors use measured zero-sequence current resulting from ground faults to estimate the fault current angle to be injected in [30]. This is possible because the zero-sequence current provides a better relay voltage measurement, and the relay current angle can be made to match the fault current angle. This scheme does not work for line-to-line faults because no zero-sequence current is produced. The authors in [41] use negative-sequence voltage measurement to estimate the fault current angle which can also be used during line-to-line faults.

Various approaches are possible for increasing the short-term current capability of inverters during faults. Improved thermal management of semi-conductor devices using a phase-change material to extend the safe operating area (SOA) for fault current purposes has been demonstrated but requires modification of the power module [18]. Moreover, the ability to commutate during fault current conditions needs be extended to match the new thermal limit.

Concepts such as virtual synchronous machines (VSM) have been advanced to mimic properties of synchronous machines including fault current, but they are still limited by the rating of the semiconductor devices [42].

These enhanced fault current control schemes improve the impedance measurement but none of these have provided an ideal solution yet to distance protection in a network with high penetration of IBR. In order to support the distance relays and make a reliable assessment of the fault location, the IBR system needs to enhance its fault current contribution to become comparable to that of a synchronous generator. The objective of this thesis is to investigate different methods to enhance fault current contribution to around $5\ pu$ from an IBR.

2.2 Thermal Management of Semiconductor Devices

IBRs are subject to strict limits on their maximum current because the semiconductor switches can only safely and reliably operate when their junction temperature remains within their SOA. If they are operated in overload conditions, that is beyond the design current, the junction temperature will rise quickly and breach the limit for safe operation and the switching module will be at increased likelihood of failure due to thermal breakdown or latch-up [18].

The junction temperature should not rise above their stated maximum junction temperature, $T_{j(\max)}$, typically $150℃$ even for short periods. It is common to set an operating limit for maximum temperatures below the device limit, $T_{op(\max)}$, of say $125℃$. The cooling arrangement to remove heat dissipated in the semiconductors and hold the temperature below the limit can take several forms ranging from finned heat sinks with convection air flow or forced air flow to water-cooled cold plates [43]. Forced-air cooling is used for some IBR [44] but this thesis is going to concentrate on large, multi-megawatt converters such as HVDC [45], STATCOM [46] and offshore wind farms [47], where liquid cooling is the preferred method.

The most sophisticated cooling systems are seen in high voltage converter stations. They use a mixture of de-ionised water and glycol pumped between the cold plates on which the devices are mounted and a radiator or heat exchanger. For example, the valve cooling system in Guangzhou converter station uses the parallel water-cooling principle as shown in Figure 2-6 in closed loop systems [48]. The stacked switching modules have heat sinks on either side. The parallel cooling circuit ensures that the same water temperature is available to all the semiconductor devices. Redundant circulating pumps, each pump having a capacity of 100%, are provided to ensure continued operation through pump failures and allow maintenance

during operation. The high-quality instrumentation with redundancy provides accurate temperature control and heat transfer to ambient is provided by evaporative coolers. However, their cooling system does not allow much additional current before this maximum permissible junction temperature is reached.

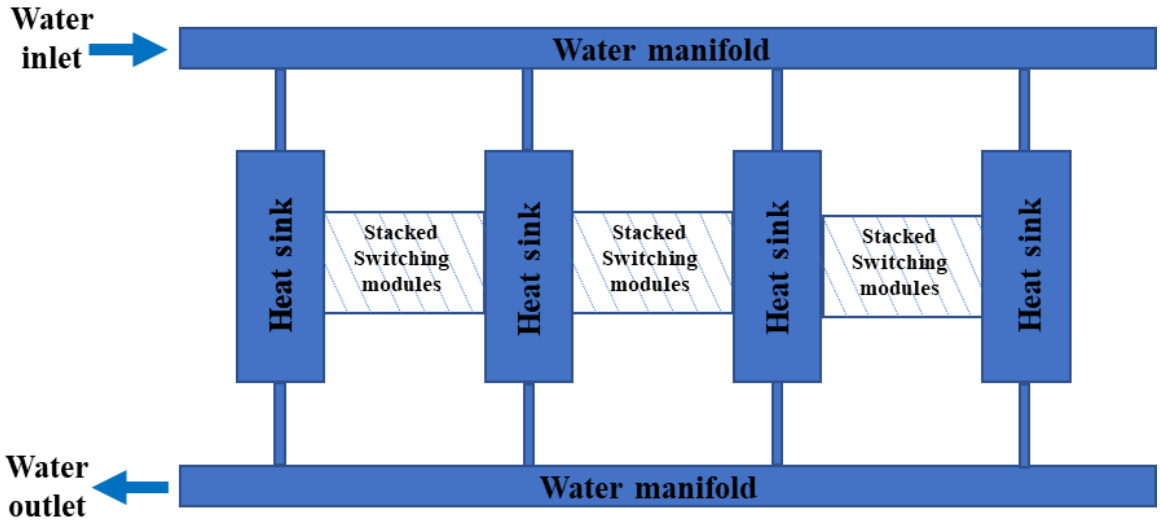


Figure 2-6: Closed cooling arrangement of module cooling circuit (stacked switching modules, heat sink and manifold) [48]

If IBR are to source fault current many times their normal value, the over-temperature failures in the switching devices will need to be prevented through enhanced cooling. One option is to exploit the large amount of thermal energy that can be stored / released during the phase change process (solid to liquid or liquid to solid) which occurs at a nearly constant temperature. Materials that are designed for this purpose are known as phase change material (PCM). Thermal energy storage with PCM is a technology based on the principle of latent heat thermal energy storage (LHTES) [49].

Several factors need to be considered when selecting a PCM for semiconductor cooling, most importantly the latent heat, specific heat, density, thermal conductivity and melting temperature.

Paraffin wax is employed for thermal energy storage in many applications due to high heat of fusion, appropriate melting temperature, high specific heat capacity, chemically inert, stable, noncorrosive and nontoxic properties [50]. By varying the length of hydrocarbon chains, manufacturers of paraffin wax can present a large selection of melting points. They are also chemically compatible with most metals. The change in volume during the phase change from

solid to liquid means that providing appropriate voids is an essential part of the design. The low thermal conductivity of wax requires the provision of good heat conduction paths to enable uniform spread of heat.

PCMs comprising hydrated salts have a high latent heat per unit weight and volume and have a relatively high thermal conductivity for non-metals [51]. They also show a small volume change between solid and liquid phases but are corrosive by nature and long-term stability is uncertain. Table 2-3 shows comparisons between different types of PCMs.

Table 2-3: Properties of different types of phase change materials [51]**.**

	Paraffin Wax	**Non-Paraffin Organics**	**Hydrated Salts**	**Metallics**
Heat of Fusion	High	High	High	Medium
Thermal Conductivity (W/m.K)	Very Low	Low	High	Very High
Melting Temperature (°C)	-20 to 100+	5 to 120+	0 to 100+	150 to 800+
Latent Heat (kJ/kg)	200 to 280	90 to 250	60 to 300	25 to 100
Corrosive	Non-Corrosive	Mildly Corrosive	Corrosive	Varies
Thermal Cycling	Stable	Elevated temperatures can cause decomposition	Unstable over repeated cycles	Stable
Weight	Medium	Medium	Light	Heavy

As shown in Table 2-3, organic and non-paraffin organic-based PCMs satisfy the requirement of high latent heat storage capacity, but they usually possess very low thermal conductivity, which makes heating and cooling slow during PCM melting and solidification. The enhancement of heat transfer in a PCM is usually achieved by inserting a high thermal-conductivity material, known as thermal conductivity enhancer (TCE), into the PCM.

Metallic PCMs provided the highest thermal conductivity among all the other PCMs. This is important in a heat sink design since during normal operation, when the PCM is not being actively used, the PCM must still provide a good heat path between the device and the cold plate. However, metallic PCMs have low latent heat values and relatively high weights.

PCMs have been reported in many applications such as buildings and portable handheld devices [52], [53]. The use of PCMs has also been proposed as a passive cooling technique in [54], [55], [56]. There has been interest in application of PCMs in cooling, heating and power generation in different temperature ranges for different industries such as buildings, defence and power electronics [57].

2.3 Role of PCMs in Fault Current Enhancement

There has been some work on using PCMs in individual semiconductor modules for power electronic equipment. With enhanced thermal management, the semiconductors (e.g. IGBT) can potentially be run at higher current density [56] and this could be useful for supplying fault current into the network during a fault under the control of an appropriate control system.

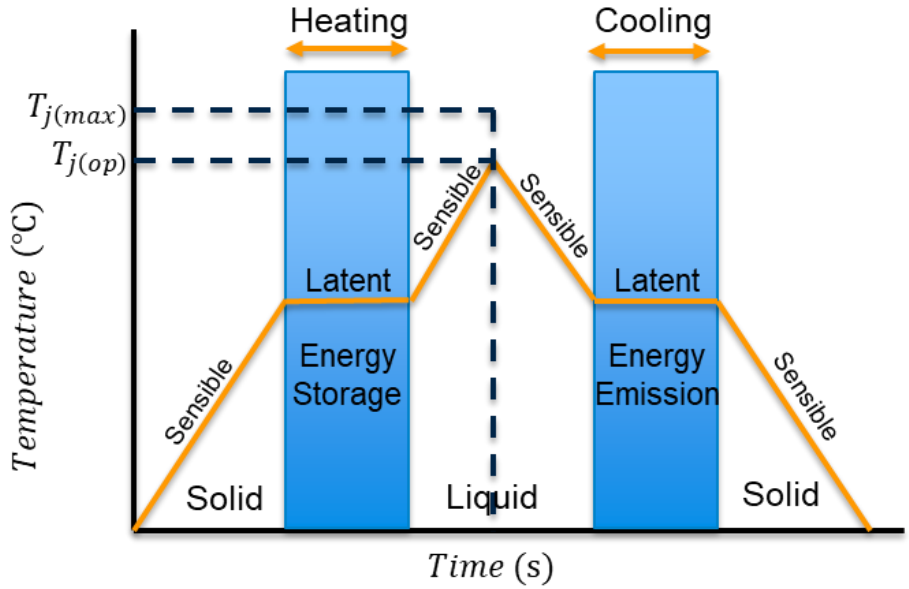


Figure 2-7: Schematic diagram of the phase change transition of a PCM

Figure 2-7 shows the "sensible" region, where the PCM absorbs and releases a large amount of energy at a certain temperature during the phase change transition period with a high heat fusion around its phase change temperature range. During the overload conditions, the IGBT junction temperature should remain below its rated $T_{j(max)}$ to ensure the safety of the device.

Several configurations for incorporating PCMs into heat sinks have been suggested in the literature, summarised in [58] [59] [60] [61] [62] [63] [64] [65] and Figure 2-8. In Figure 2-8 (a), the tips of the fins are immersed in a PCM. In this configuration, a large section of the heat sink can be left open for air flow and the thermal resistance from heat source to the air

would be comparable to that of a conventional heat sink. The disadvantages include slow heat transfer to the PCM because it is distant from the heat source and the amount of PCM that can be included is smaller than in other configurations [66].

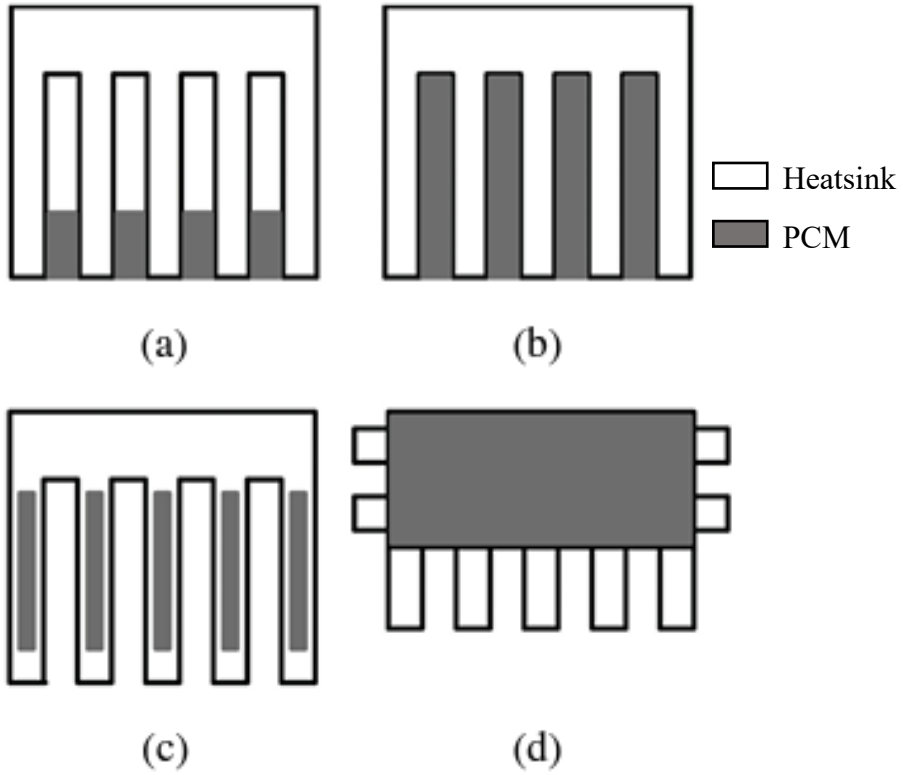


Figure 2-8: Various configuration of PCM with heatsinks in literature, PCM shown in grey. (a) heat sink fins tip immersed in PCM. (b) Heat sink channels filled with PCM. (c) Heat sink fins filled with PCM. (d) PCM compartment directly underneath a heat source and surrounded by fins [66]**.**

Figure 2-8 (b) shows an arrangement where the area between the fins is filled with PCM. Although this provides a comparably good amount of PCM, there is no airflow between the fins which would lead to large thermal resistance due to poor conductivity of PCMs and would result in a low heat flow to the ambient for a given temperature rise [58] [63] [67] [68].

The study in [65] uses the configuration of Figure 2-8 (c), where the PCM is embedded in the heat sink fins. In order to have an appropriate amount of PCM, the fin thickness needs to be in the region of a few millimetres. The disadvantage with this configuration is that it may prove difficult to manufacture. Also, by putting the PCM there, the aluminium heatsink is long and thin reducing the conductivity and is therefore bad for steady state temperature rise.

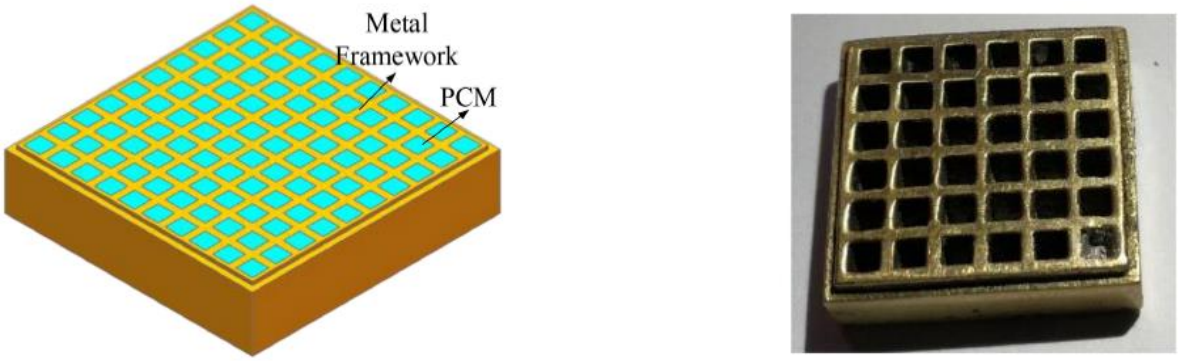
In Figure 2-8 (d), where the heat source is placed on top of a large PCM filled compartment [60]. With PCM closer to the heat source, it allows for rapid heat absorption but due to low conductivity of the PCM, the heat sink performance in normal conditions would be poor.

The study in [61] [62] showed a placement of PCMs beneath the chip which improves dynamic performance of the thermal management during increased current flow. However, the duration in which temperature is held constant by the phase change is short because of the small quantity of PCM that can be accommodated.

It is apparent that some trade-offs exist when including a PCM in a heatsink. A greater volume of PCM results in a longer period over which temperature can be held low but, if the PCM has a high thermal resistance, the greater depth of PCM degrades heat flow and raises the device temperature in normal use. The combination of thermal resistance and heat capacity needs to be considered because it produces a time-constant that sets how quickly the temperatures transition between different operating conditions.

With the help of TCE, a good spread of the heat through the PCM can potentially be achieved. This was explored with the concept of combining a PCM with metal foam in [66]. The study in [66] showed that by using TCE, the heat spread within the PCM took between 30-50 s before the junction temperature was actively held. This is inadequate to deal with fault in the grid and provide fault current.

A study by *Shao et al* in [18] to assess increased short-term current capability by using a PCM inside a semiconductor module, showed that PCM offered a modest short-time rating increase of SOA in the device without increasing its $T_{j(max)}$ [18]. A quick spread of heat (within 10 ms) is achieved by using a metal framework as TCE and melts the PCM in few seconds as shown in Figure 2-9 (a) and (b). To verify this, the study [18] developed a melting process model and the equivalent thermal resistance of the designed power module is calculated. Similar to synchronous machines, the IBRs will be expected to provide fault current to support the protection system in the scale of a few milliseconds if not a few seconds.



(a) (b)

Figure 2-9: (a) Structure of a PCM with TCE (metal framework). (b) Prototype of 3-D printed metal framework [18]**.**

The results reported in the literature have shown that PCMs coupled with a good TCE have the potential to provide some short duration management of junction temperature during periods of high-power loss in semiconductors. The various arrangements of a PCM within a heatsink create different trade-offs between the duration for which the junction temperatures are held by the PCM transition and the impact of the PCM on normal operating temperatures. There is a need for a study that focuses on how that trade-off can be struck for the particular case of fault currents which are in the order of 100 ms and whether over that period a sufficient increase in maximum current can be achieved. This will be the focus of Chapter 3.

2.4 Modular Multilevel Converter (MMC)

Line Commutated Converters (LCC), a type of Current Source Converter (CSC), have long been the dominant converter technology in high power applications. For example, Three Gorges-Changzhou and Three Gorges Guangdon HVDC bipolar links have a nominal rating of 3 GW and also have a five second overload rating of 4.5 GW [69]. Innovations in power electronic devices have resulted in a shift towards multilevel Voltage Source Converters (VSC). Multilevel converters, in particular the Modular Multilevel Converter (MMC) [70][71], are now well-established in industry for use in a wide range of high-power applications [33]. The available power rating of MMC based converter stations and their associated cables and other ancillary systems have seen significant growth. The MMC is composed of many (typically many hundreds) of submodules in series connection. This brings several advantages such as an ability to provide high quality voltage waveforms with very low switching power loss and an ability to introduce redundant sub-modules to provide high reliability. The modular

structure is of interest in this research because of the possibility to reconfigure between series and parallel combination to modify the current and voltage rating of the converter during operation and particularly during faults. This will be the topic in CHAPTER 4

While there are many other circuits similar to MMC, offering different features, none are as well established or widely used as the MMC. This subsection provides a review of the MMC and briefly introduces the alternate arm converter (AAC) which has some interesting features that may lend itself to series/parallel reconfiguration.

The MMC, first proposed in [71], has been adopted as a standard voltage source converter for high power IBR applications, as well as high-voltage DC (HVDC) and medium-voltage DC (MVDC) systems due to their scalability and low AC filtering requirements. Multi-level converters are implemented as an important technique to build high voltage power converters from semiconductor devices of a much lower voltage rating. The MMC has been studied extensively and can be constructed from several hundred individual Sub-Modules (SMs), the most common of which are the full-bridge (FB) and half-bridge (HB) SMs, each with a capacitor controlled around a nominal voltage [72]. The HB-MMC has a higher efficiency and lower device count; however, the FB-MMC is capable of DC fault ride-through. An MMC is shown in Figure 2-10 with HB-SMs and FB-SMs.

The converter is made up of six arms, with two arms per phase. Each phase arm consists of a series stack of SMs. The number of SMs per stack, N, is such that the maximum voltage capability of the stack must exceed the DC-side voltage, V_{DC}, giving

$$N \geq \frac{V_{DC}}{V_{sm}} \qquad \textbf{(2.3)}$$

Where V_{sm} is the nominal sub-module voltage.

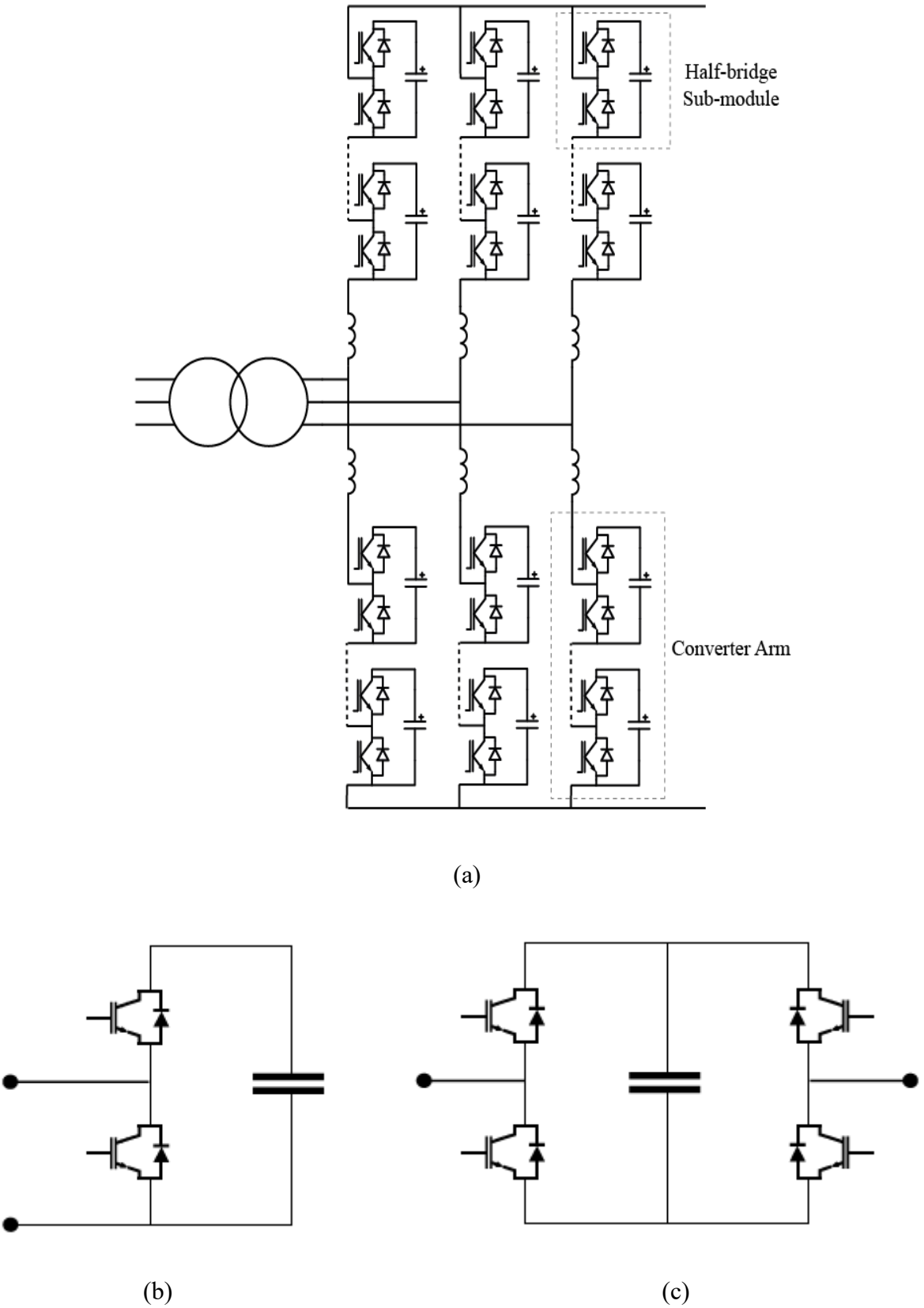


Figure 2-10: Circuit schematic of the (a) Modular Multilevel Converter with half-bridge sub-modules (b) Single half-bridge Submodule and (c) Single full-bridge sub-module.

Each stack is able to control its voltage output by inserting or bypassing the capacitor of each SM. Thus, by controlling the number of inserted capacitors in each arm of the converter a staircase AC voltage waveform with low harmonic distortion is generated which requires little to no filtering at the AC terminal [71]. As this AC voltage waveform is the sum of the individual SMs, the switching frequency of the individual SMs is reduced, bringing the converter efficiency close to that of a thyristor-based CSC station [33]. The modular topology allows converter stations to have power ratings up to gigawatts and operating voltage at several hundred thousand kilovolts. The MMC is constructed using forced commutation devices such as standard IGBT modules and control circuitry designed for drive applications. The low rate at which individual IGBTs are switched in the MMC results in low overall switching losses and high efficiency [73]. However, additional control is required to maintain the overall energy balance within the converter as well as to balance the individual voltages of SMs.

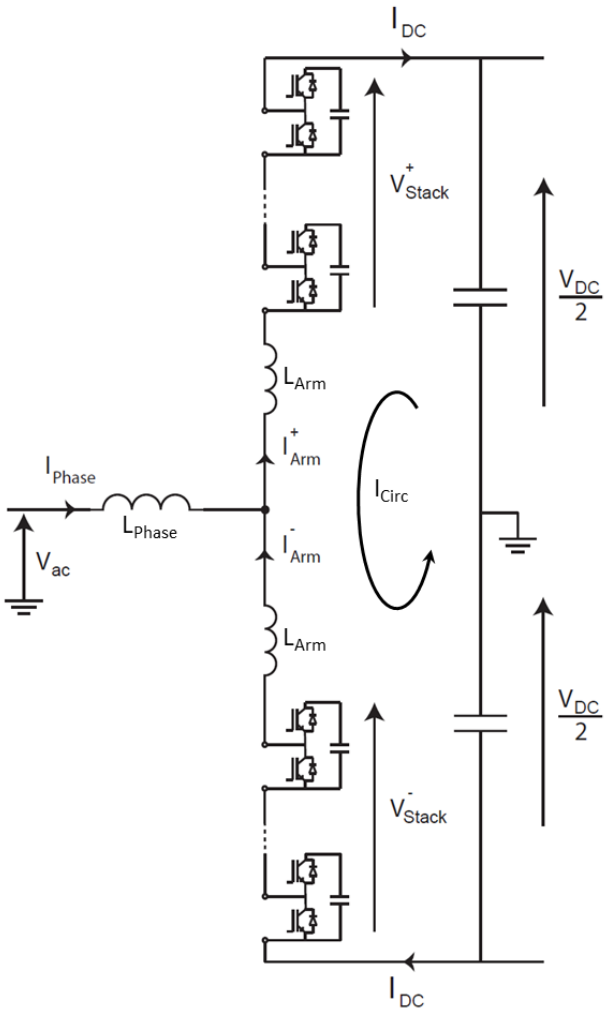


Figure 2-11: Per Phase Representation of Modular Multilevel Converter

A Per Phase Representation of the MMC is shown in Figure 2-11. In the standard operation of an MMC, the DC current is split evenly among the three phases and each phase current is split between the upper and lower arms of each phase. The currents flowing through the converter are given by equations (2.4) - (2.5).

$$I^{A+}{}_{arm} = \frac{I^{A}_{phase}}{2} + \frac{I_{DC}}{3} + I_{circ} \tag{2.4}$$

$$I^{A-}{}_{arm} = -\frac{I^{A}_{phase}}{2} + \frac{I_{DC}}{3} + I_{circ} \tag{2.5}$$

In a well-controlled converter, the circulating current term can be suppressed completely [74]. The voltage that the upper and lower arms, equations (2.6) and (2.7) respectively, have to generate are given by equation.

$$V^{+}_{Stack} = \frac{V_{DC}}{2} - L_{arm}\frac{dI^{+}_{arm}}{dt} - L_{phase}\frac{dI_{phase}}{dt} - V_{phase} \tag{2.6}$$

$$V^{-}_{Stack} = \frac{V_{DC}}{2} - L_{arm}\frac{dI^{-}_{arm}}{dt} + L_{phase}\frac{dI_{phase}}{dt} + V_{phase} \tag{2.7}$$

The MMC has an equal number of SMs in each arm and each of those arms is rated to the DC-link voltage. This means if a SM fails, the DC-link would no longer be supported, and the converter would have to shut down to prevent further failures. The modular design of the MMC makes it possible to place a percentage of redundant SMs within an arm of the converter to tolerate several SM failures between maintenance periods. This provides MMC a key advantage over other converter topologies.

Other multilevel converter topologies have been proposed, such as the hybrid-MMC [75] [76], the AAC [77], and the AC-side cascaded H-bridge converter (2L-AC-CHB) [78].

2.4.1 Alternate Arm Converter

The AAC is a hybrid between a 2-level converter and an MMC [77]. The converter has a modular design, with each phase arm consisting of a series stack of SMs or cells which is then in series with a switch composed of further IGBTs. Each SM / cell contains IGBTs in a full-bridge (FB-SM) or half-bridge (HB-SM) arrangement, and a cell capacitor controlled around a nominal voltage. As shown in Figure 2-12, the AAC consists of many SMs inserted in series within six arms, with two arms per phase, like the MMC (Section 2.4).

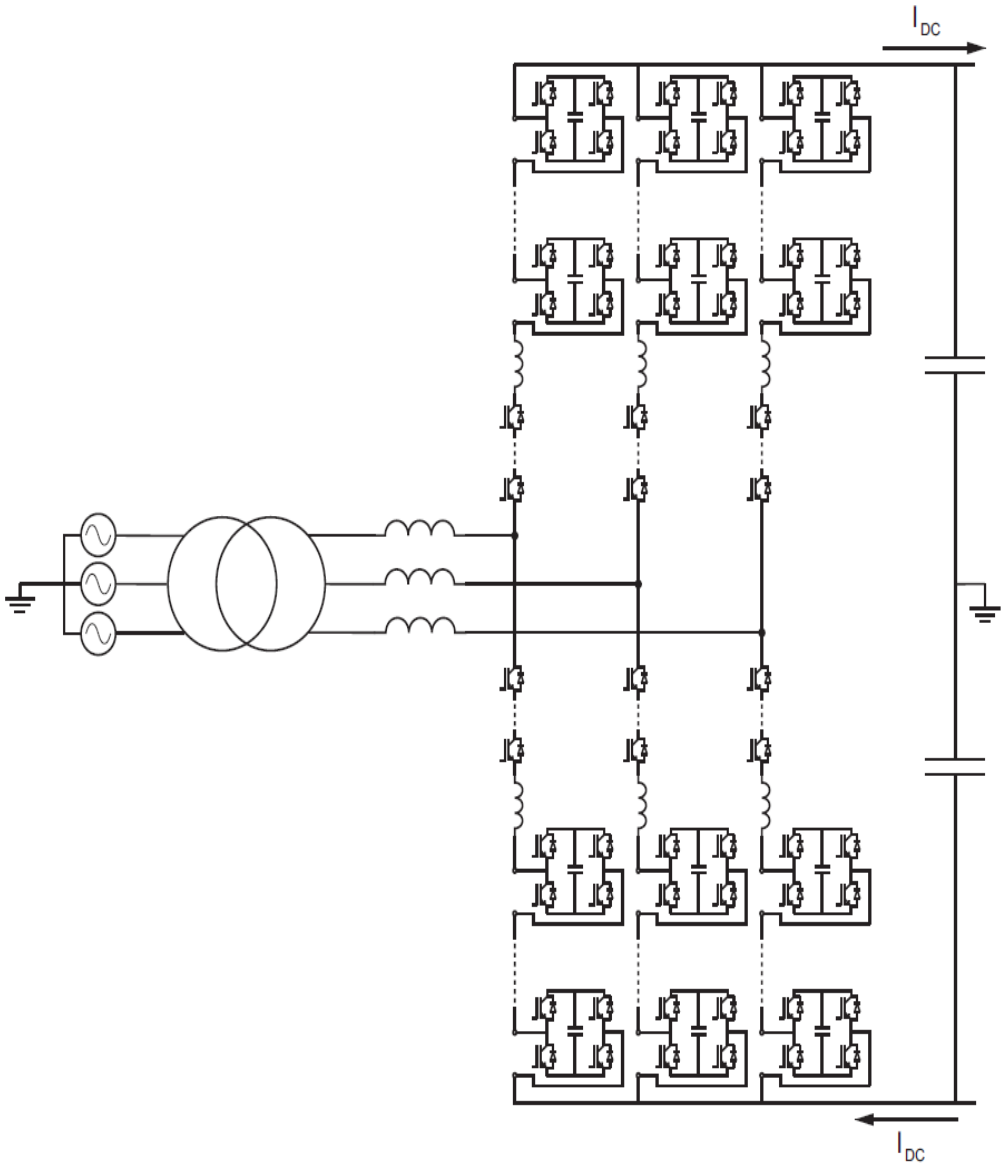


Figure 2-12: Alternate arm converter with full H-bridge sub-modules and series connected director switches for three-phase [33]

The difference between the AAC and MMC is that the AAC has director switches within each arm of the AAC, which consists of series connected IGBTs, while the MMC only has its SMs. In each phase of the AAC, the director switches act like the IGBTs within the 2-level converter, inserting the upper arm into conduction during the positive part of the AC waveform, and the lower arm during the negative part of the cycle. The arm that is in conduction can switch the SMs within its arm in and out of conduction, like the MMC, to create the staircase AC waveform [77]. This flexibility provides the AAC with the advantage over MMC to lower its total stack voltage capability requirement by approximately half. This results in an

approximately 50% [49] reduced number of required SMs per stack and lowers its overall losses. The total SM energy storage requirement is also reduced to $\sim 10\ kJ/MVA$ for $\pm 10\%$ voltage ripple [45]. The advantages of AAC and extended overlap AAC (EO-AAC) was further studied in [77] and [79].

The expected services from such a large power rated converter station may include additional ancillary services such as fast frequency support, fault current contribution and power flow control during electrical system disturbance. MMCs typically have very little overload capacity and thus are unable to provide these services.

2.5 Static Synchronous Compensator (STATCOM)

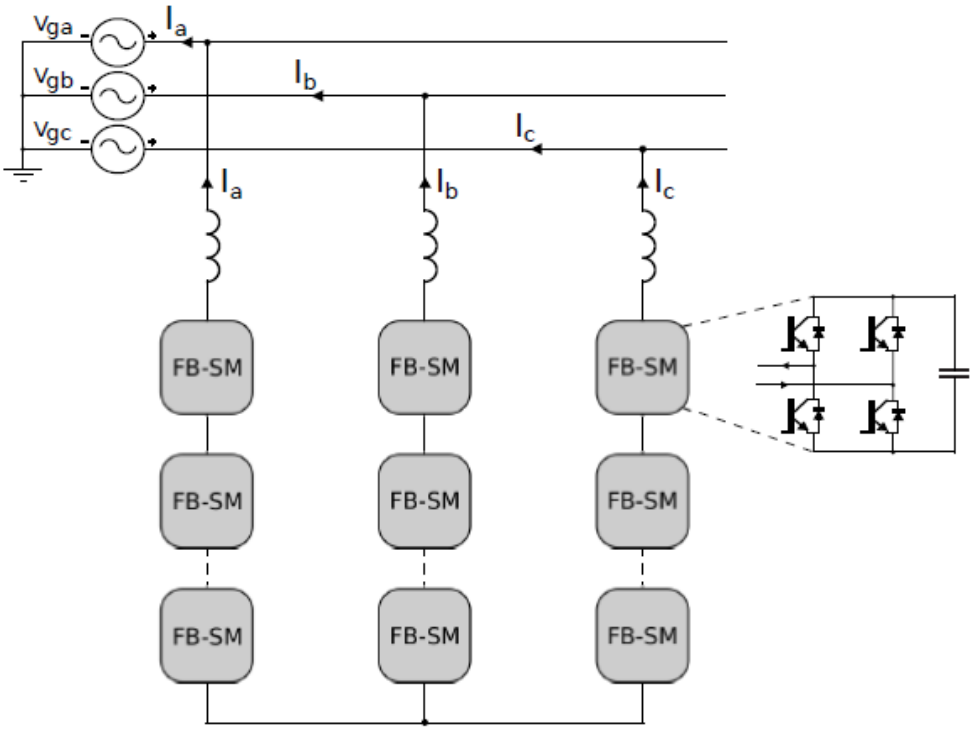
A Static Synchronous Compensator (STATCOM) is a common piece of network equipment and is used in this thesis as an example for fault current enhancement. STATCOM is based on a VSC and can provide reactive power compensation for a grid. The STATCOM regulates the voltage at the point of common coupling (PCC) by either injecting or absorbing reactive power from the grid. When the grid voltage is low, the STATCOM responds by generating a capacitive current to the grid and injecting reactive power. If the grid voltage is high, the STATCOM responds by generating an inductive current to the grid and thereby absorbing reactive power. The classic STATCOM only delivers reactive power but may be functionally enhanced to provide active power if connected to a power source such as energy storage.

STATCOM is typically interfaced to the grid via a coupling transfer. The presence of the coupling transformer gives an opportunity to incorporate a tap-changer with a large tap-ratio and change the current and voltage rating of the STACOM system during a fault. Using this principle to produce fast fault current will be described in Chapter 5. A STATCOM is a type of IBR and the principle of adding a tap-changer for fault management could perhaps be extended to other IBR.

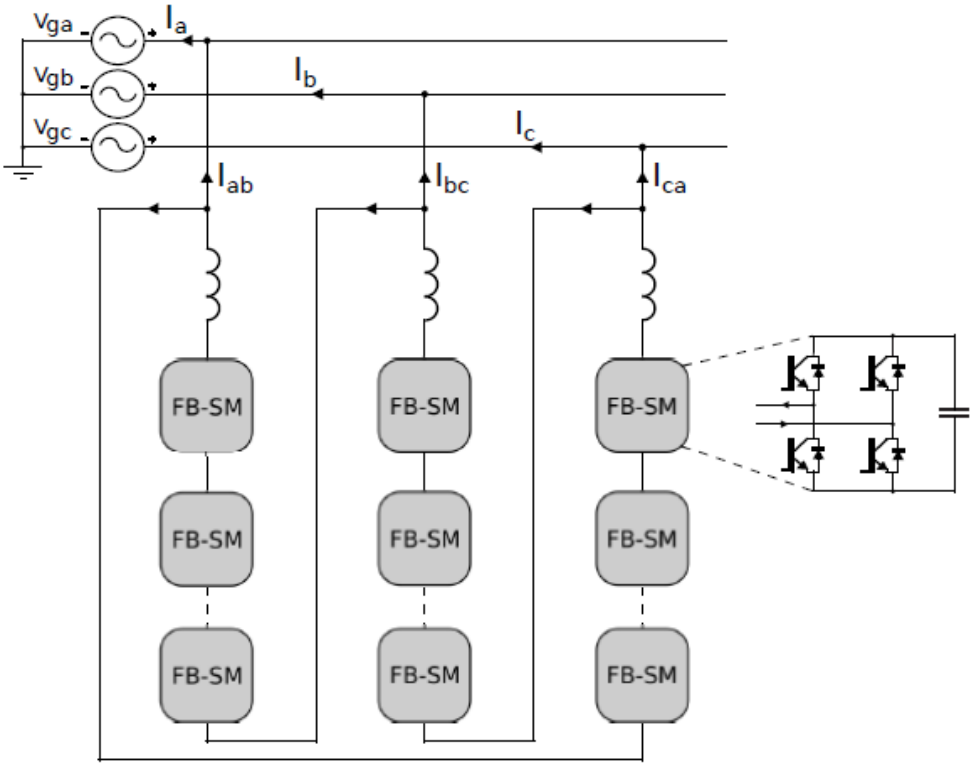
2.5.1 The Cascaded H-Bridge Converter based STATCOM

The Cascaded H-Bridge (CHB)-based STATCOM was identified for use in the studies of Chapter 4 and 5 of this thesis because of its advantage of modularity and suitability for high voltage application. The CHB Converter can achieve high voltage outputs as they have identical and substitutable series connected SMs, where a DC source can be distributed at SM level rather than provided as a single item on the DC-link. This need for an individual isolated

DC source means that the CHB converters requires isolated transformers [80]. Capacitors can be used as the DC sources if only reactive power generation is required. Additional controls to manage critical parameters such as state of charge (SoC) is required to prevent capacitor voltage deviation. This topology is commonly used in STATCOM applications. The circuit diagram for the CHB based STATCOM in star and delta configuration is shown in Figure 2-13. In both STATCOM solutions Single Star Bridge Converter (SSBC) and Single Delta Bridge Converter (SDBC) there is no common DC bus, which means each FB-SMs have separate DC sources [70]. The FB-SMs provide positive and negative voltages that are required for the operation of the converter.



(a) Single Star Bridge Converter



(b) Single Delta Bridge Converter

Figure 2-13: CHB-based STATCOM (a) Single Star Bridge Converter (b) Single Delta Bridge Converter [70]

2.6 Tap Changer Circuits

Existing transmission and distribution network voltage-control mechanisms rely extensively on tap changer circuits in transformers, in particular the on-load tap-changers (OLTCs). They are designed to provide voltage regulation within the defined limits. The tap-change circuits enable adjustments of the turns-ratio of transformers. They are described as on-load tap changers if the change in turns-ratio can be performed while the transformer is carrying load current while it is supplying its load.

Currently, mechanical OLTC are commonly used to perform turns-ratio adjustments but they suffer from needing a long time to perform a tap-change. An electronic tap changer (eTC) has a significantly faster operation time than that of its mechanical counterpart. It is anticipated that fast tap changes will be required for fault management. The eTC using thyristors and IGBTs have been proposed in the literature for an improved voltage regulation for distribution transformers [81] where a tap range of up to $\pm 10\%$ is normal. The proposed eTC scheme in CHAPTER 5 builds on the approach used in [82] to create a tap-changer with a large change in turns-ratio in the STATCOM coupling transformer windings in order to provide a large change in available current. This following subsection describes different types of tap-changers with a focus on eTCs.

2.6.1 On-load tap-change circuits (OLTCs)

The main objective of an OLTC in a transformer is to regulate the amplitude of the bus voltage to maintain a pre-set voltage reference and minimise fluctuation. OLTC-enabled transformers can be located at in-feed and out-take points of the transmission network, including points of common coupling or connection points of large generation units. The super grid transformer operate at transmission level such as between the transmission voltages at 400 kV and 275 kV to sub-transmission network 132 kV [22].

The OLTC switches between the tapped windings of a power transformer to modify output voltage. NGESO or DNOs take advantages of modified output voltage to keep bus voltage levels. This has increasingly become important as the dynamics of the grid changes with increased adoption of IBR.

An OLTC works on the principle of “make before break” circuit. In the “make before break” circuit, connection to the new tap is established before the connection of the old tap is broken so that there is no interruption in the load current.

There are three types of OLTC.

- Mechanical OLTC (M-OLTC)
- Electronic-assisted or hybrid tap changer (EA-OLTC)
- Electronic tap changer (e-OLTC)

The following sub-sections provide overviews of these three types with a focus on the e-OLTC and its speed of tap-change operation.

2.6.2 Mechanical OLTC (M-OLTC)

A typical transmission or distribution-based transformer with M-OLTC, depending on the voltage, may have up to $\pm 10\%$ tap range with 32 positions in total. The M-OLTC is a purely electromechanical system incorporating no semiconductor device and comprising a tap selector section, a diverter section and some associated sensing and control systems. Figure 2-14 is a schematic representation of one phase of the classic OLTC. The combination of diverter and selector system fulfils the need for continuous load current by incrementing or decrementing the tap selection by one each time.

An automatic tap-change control (ATCC) system controls the voltage at LV busbar(s) of super-grid transformer by changing transformer tap positions. An ATCC enabled M-OLTC can take up to 10 seconds to complete a tap-change. The ATCC may also introduce an inter-tap delay time, which could be between 30 and 120 seconds in 5 seconds increments [83].

For a tap-change circuit to be used as part of a fault current enhancement device, operation needs to occur quickly enough for protection relay operation which would be less than two cycles of mains and preferably in the sub-transient period of a fault in the first cycle. The mechanical movement in M-OLTC makes it difficult to make tap-change transition in the required time period.

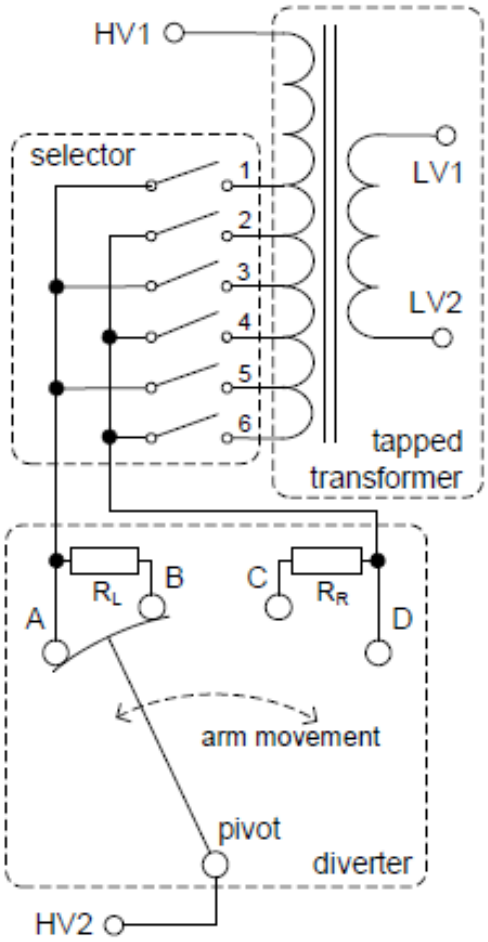


Figure 2-14: Schematic representation of the classic OLTC (single phase) [84]

2.6.3 Electronic assisted or hybrid tap changer (EA-OLTC)

The literature contains examples of hybrid OLTC designs that use modern semiconductor devices to assist mechanical switches to enhance the speed of the tap-change operation and increase the number of lifetime operations.

Figure 2-15 shows the conceptual design of a single phase of an EA-OLTC scheme [84]. Similar to most OLTCs, the conceptual design of a single phase of the OLTC can be separated into a selector section and a diverter section. The selector and diverter section connects to the selected tap position by following the philosophy of make before break circuit. The diverter part scheme presented in Figure 2-15 consists of two mechanical switches, two sets of anti-parallel thyristors and a voltage or current controlled source. The EA-OLTC scheme provided precise control over the path taken by load current (zero-current, zero-voltage switch conditions) that eliminated arcing during contact, potentially increasing the switch lifetimes.

EA-OLTCs use mechanical switches in steady state to lower conduction losses in semiconductors. In this way, the strengths of both devices are exploited to lower on-state resistance and wear-less commutation capability. However, this EA-OLTC has not yet been demonstrated to work well with a large change in turns-ratio where the electronic elements are exposed to larger voltages.

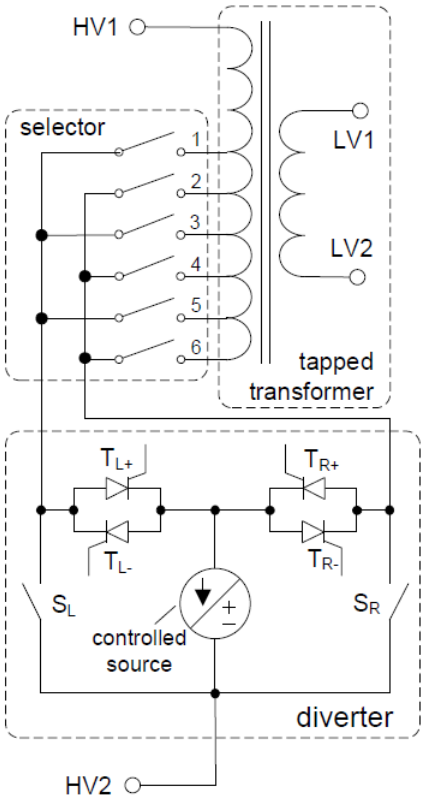


Figure 2-15: Schematic representation of the classic EA-OLTC (single phase) [84]

Generally, the tap-changing process of a mechanical tap-changer is slow and can be as long as 10 s where springs have to be mechanically charged [85]. Even relatively fast vacuum tap-changers are not a viable option for responding to a need for fault current injection. OLTCs based on vacuum interrupters utilise only one or two devices per phase, in which the selector switches remain as a set of standard mechanical contacts operating in oil or air [86]. Vacuum interrupters can manage high speed diverter operation due to short distances its contact has to move. However, completing a rapid tap change remains a challenge due to the slow speed of the selectors.

With increased IBR in the network, the voltage control using traditional OLTC in transformers are unable to meet the high number of tap-changes required without reducing the lifetime of

the mechanical taps due to arcing [84]. This results in lower lifetime of the tap-changer switches and requires repeated maintenance. Nevertheless, these mechanical taps have the advantage of high overload rating and low conduction losses.

2.6.4 Electronic tap changer (e-OLTC)

The principles of electronic tap changing systems are a relatively new technology [87] [88] [87] in which gate-controlled devices such as back-to-back silicon-controlled rectifiers (SCRs) and gate turn-off thyristors (GTO) have been used. More recently IGBTs have been proposed as switching devices in tap-changing circuits [90]. E-OLTC can provide significantly higher speed performance than that of its mechanical counterpart due to the lack of moving parts, and the ability to jump from one tap to any other tap repeatedly at short intervals of half cycles (10 ms). Power electronic switches will allow the tap changer to operate sufficiently fast to deliver fault current in a cycle of the grid voltage or less. Replacement of the mechanical switches by electronic switches to form an e-OLTC can potentially provide continuous control of the transformer voltage and current. The fundamental differences between mechanical and complete semiconductor-based tap-changers are discussed in [85]. To gain acceptance, e-OLTC need to be economically competitive, not just technically attractive.

Figure 2-16 shows an example of an e-OLTC with SCR-based tap-change circuits. With a careful switching strategy, excessive circulating current can be avoided to implement a make-before-break circuit. In this scheme, during the tap-down sequence, the transformer voltage and current product should be negative and during tap-up sequence, the current and voltage product should be positive which allows the incoming SCR pair to always pick up the load current without creating any circulating current [91].

The e-OLTC designed in [81] uses a significantly lower number of thyristor-based power electronic switches compared with those reported in the literature. The same authors proposed an IGBT-based e-OLTC for distribution transformers [91]. A thyristor-based e-OLTC was incorporated into a feeder distribution transformer to provide reactive power for voltage regulation in [92]. Thyristors chosen for the tap change switches can provide low conduction losses and high surge current capability when compared to IGBTs, which will be important during normal use of the tap changer circuit.

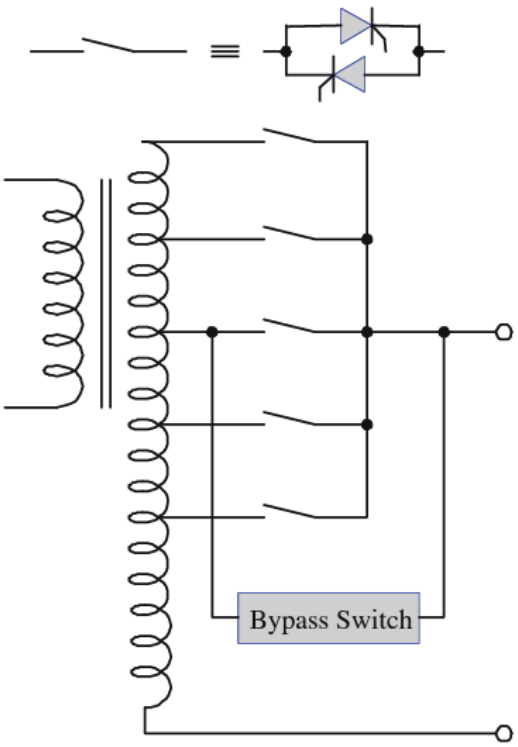


Figure 2-16: An electronic tap-changer with no passing impedance [91]

The eTC using thyristors and IGBTs have been proposed in the literature for an improved voltage regulation where typically a tap range of up to ±20% is normal to comply with the IEEE/IEC 60214 standards [93].

The proposal to use a tap changer to achieve a $2:1$ or $4:1$ increase in fault current requires a tap-change in the transformer winding higher than the normally considered $\pm 10\%$ used for voltage management. Such tap-changer circuits making high turns-ratio change is not seen in transformers, but the study completed in [82] implements a fast thyristor-based tap-changer in a double-fed induction generator to create a $3:1$ voltage-turns ratio change in the rotor winding. The tap changer circuit proposed in Chapter 5 improvises on the methodology used in [82] to create a tap-changer to achieve a large voltage turns-ratio in the STATCOM coupling transformer windings.

The study in [82] takes the doubly-fed induction generator concept as an opportunity to design a new type of generator that combines the robust construction of induction machines and the control flexibility of power electronics. Figure 2-17 shows a double fed induction generator single phase equivalent circuit. During normal operation, the stator and rotor windings are magnetically coupled and interact such that the currents flow through the stator and rotor

windings. Here the parameters R_s and R_r are the wiring resistances. The parameters L_{ls}, L_{lr}, L_{ms} and L_{mr} are the stator and rotor leakage inductances, stator and rotor magnetising inductances, respectively. Φ_m contains the mutual inductances. Table 2-4 shows other parameters used in this study [82]. Applying Kirchhoff's voltage and current laws and adopting the generator convention of positive current flowing out, the voltage across the stators winding (v_s) and the rotor winding (v_r) can be calculated by considering the rotor current (i_r) and stator current (i_s) and the flux linkages between the two windings.

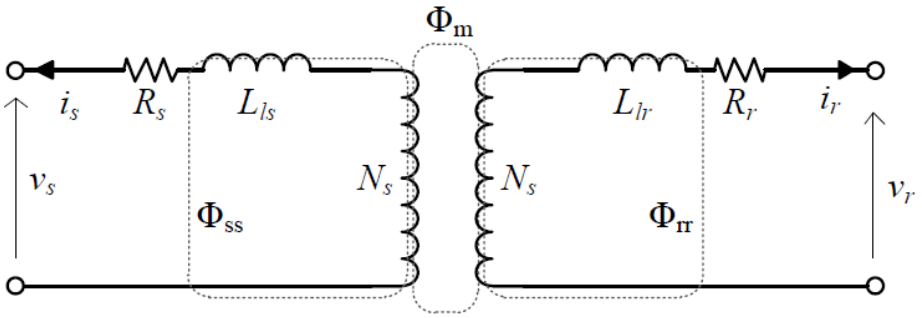


Figure 2-17: Doubly fed induction generator single phase equivalent circuit [82]

During the fault, the Zefal generator is concerned with decreasing the generator fault current contribution to zero [82]. The proposed scheme reduces the interaction between the rotation rotor flux and stationary remainder of the stator flux with the stator and rotor windings, respectively. By minimising the interaction, the fault current can be diminished.

The proposed generator in [82] consists of a wound rotor induction machine, a back-to-back voltage source inverter and a tap changer circuit. The rotor winding of the induction machine are tapped in such a way that it represents two series connected windings. Figure 2-18 shows a single-phase equivalent circuit diagram of the ZEFAL generator, stator winding, the split rotor winding, and the tap-changer S. By changing the selecting position of S, either the full rotor winding is excited or only a section, leaving the remaining winding open circuit. The point in the winding where the tap is made is denoted by n such that $N_r = N_{r1} + N_{r2} = nN_r + (1-n)N_r$, where N_{r1} and N_{r2} are the number of turns on the first and second rotor windings, respectively.

$$n = \frac{N_{r1}}{N_{r1} + N_{r2}} \qquad \textbf{(2.8)}$$

During a fault situation, a power controller regulates the current in the rotor winding to reduce the current flowing in the stator winding, or to synchronise the magnetic field of the rotor winding with the magnetic field of the stator winding and thereby reducing their interaction. This reduction in mutual inductance between the two windings is achieved through a tap changer circuit in the second winding, which reduces the number of turns through which the current in the second winding flows.

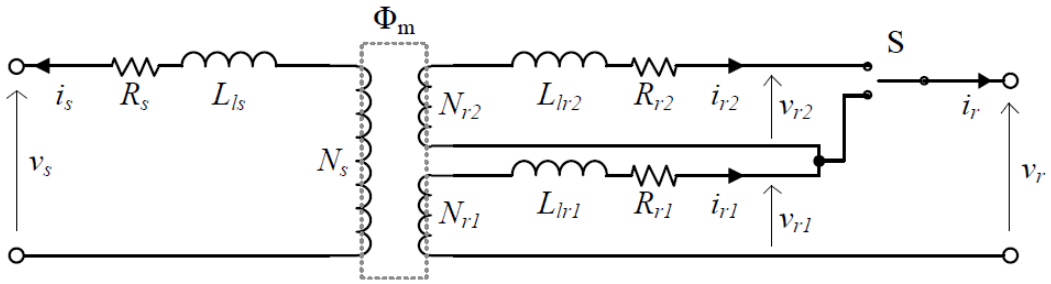


Figure 2-18: Split rotor winding doubly fed induction generator single phase equivalent circuit [82]

Table 2-4: Parameters of split rotor winding double fed induction machine

Parameters	Symbol	Unit
Number of turns on stator winding	N_s	Turns
Number of turns on first rotor winding	N_{r1}	Turns
Number of turns on second rotor winding	N_{r2}	Turns
Stator winding resistance	R_s	Ω
First rotor winding section resistance	R_{r1}	Ω
Second rotor winding section resistance	R_{r2}	Ω
Stator winding leakage inductance	L_{ls}	H
First rotor winding section leakage inductance	L_{lr1}	H
Second rotor winding section leakage inductance	L_{lr2}	H
Magnetising inductance	L_m	H

The proposed Zefal tap changer uses a conventional VSC phase leg with IGBTs in S1 and S2 as modulating switches as shown on the right in Figure 2-19 [82].

The diverter switch functionality is realised by the thyristor network of Thy1, Thy2, Thy5 and Thy6. By switching the different thyristors, the pulse width modulation (PWM) waveform has the capability to either excite the entire rotor winding (rotor 1 and rotor 2) or only part of the rotor winding (rotor 1). Throughout the tap change sequence, there is current continuity for inductive load currents and diodes D1 and D2 located anti-parallel to the modulating switches provide the anti-parallel path. However, during partial tap operation, the voltage that is applied across rotor 1 exceeds the DC rail and diodes cannot be used as anti-parallel paths for the full winding as they would forward bias and short the winding end to the DC rails rather than leaving it open-circuited. Hence thyristors, Thy3 and Thy4 are used instead to behave like diodes when they are switched on but appear open circuit when switched off.

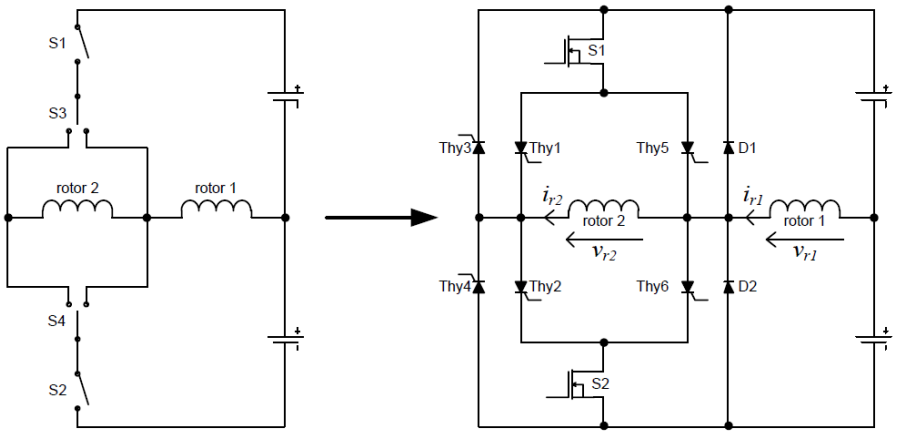


Figure 2-19: Hardware layout for a single phase of the machine side converter and tap-changer [82]**.**

In this tap-change circuit the combination of IGBTs and thyristors enable a tap change sequence. Thyristors have high i^2t- ratings and are suited to deal with over-currents. Due to the absence of natural current zero, the thyristors are force commutated by injecting current into their gate. But they naturally commutate off when reverse current flows through them and have no gating signal applied. This property of thyristors is important when the current from rotor 1 is transferred to rotor 2 after the tap change command to ensure Thy3 and Thy4 turn-off at the current cross over.

The drawbacks associated with semiconductor-based tap change schemes are based on the fact that these electronic switches must continually conduct the load current. This leads to penalty in terms of power loss when compared to the classic OLTC diverter. Also, the semiconductor switches have high voltage drop compared to the small resistive drop of a mechanical contact. Although the semiconductor switches provide flexibility and speed in different design of tap-change circuits and lead to better thermal management of devices, they incur an increased operating cost. Moreover, the e-OLTC needs to offer reliability lifetimes equivalent to the mechanical systems that they are replacing.

Thyristors or GTO based OLTC systems can offer significant reduction in operating losses compared to IGBTs because for similar voltage and current ratings, the thyristor and GTO devices have lower on-state voltage compared to IGBTs and this would result in lower conduction losses. Because the switching is at very low frequency, switching power losses are not significant.

2.7 Chapter Summary

Fault current has always been an important research area due to its impact on the operation of protection systems. In recent years, the negative impact of falling fault level on distance protection has emerged as a vital topic to support the integrity of the existing protection systems and promote greater renewable energy integration.

IBR have the potential to solve the low fault level issues seen due to displacement of synchronous machines. Section 2.1 reviewed some of basics of protection system which has given indication on speed and magnitude of the fault current required, which provides the challenge of work reported in this thesis. Section 2.2 discussed thermal management in heatsinks of switching devices, in particular the use of PCM, to pause the rise of junction temperature during increased current flow. The questions that will be addressed in Chapter 3 is whether PCM is suitable for a large amplitude fast current. Section 2.3 reviewed the basics of MMC and AACs. Chapter 4 will look at whether there are ways of doing series parallel switching to enhance fault current injection. Finally, Section 2.4 reviews STATCOM and tap-changers to provide a basis for Chapter 5, where tap-changers are used to increase fault current contributions.

CHAPTER 3 ASSESSMENT OF PHASE CHANGE MATERIALS FOR SEMICONDUCTOR THERMAL MANAGEMENT

3.1 Introduction

The challenge with IBRs regarding fault current is the absence of any significant short-term over-current capability. The short term over-current capability is typically limited to no more than $1.2\ pu$ primarily because of the thermal characteristics of the semiconductors and the difficulties of removing heat that is generated by the power losses in the semiconductor. Semiconductors cannot tolerate even short duration temperature rises above their stated maximum, typically $150℃$. The maximum permissible junction temperature ($T_{j(max)}$) of an IGBT, for example, must be treated as a hard limit and a suitable thermal management technique must be adopted such as providing an operating junction temperature ($T_{j(op)}$) below this maximum.

Enhancing the thermal management of the semiconductor devices in the IBR systems can perhaps help these devices contribute to fault current injection for short durations of, say, less than one second. If additional current above the rated value can be supported for more than a second, then auxiliary services such as fast frequency support might be provided from power electronic interfaced generators even when they are already operating at full power.

A possible way to provide some short-term relief to the thermal management problem of over-current is to place some PCM close to the semiconductor [18]. The idea is that the PCM absorbs heat during a phase-transition, most likely that from solid to liquid for this application, and in doing so prevents the temperature of the semiconductor rising as quickly as it would otherwise. The design of the cooling system is such that the PCM remains a solid during normal operation but during an overload condition, as temperatures rise, it transitions to liquid and gives a period of some seconds of overload capability while the transition is happening. Once the transition is complete, the temperature will rise quickly to unacceptable levels and so the over-current condition will have to be terminated through control action. This overload capability in the switching devices can contribute towards finding solutions to increased FCC from IBR

systems. This opportunity requires that other limits to additional current flow, such as the commutation current limit of an IGBT are not violated.

The first study undertaken in this thesis uses Finite Element Analysis (FEA) to assess the incorporation of PCM in the heatsink to increase short-term current capability at device level. Others had proposed an inclusion of PCM inside the IGBT package, but inclusion in the heat sink would allow standard IGBTs to be used and allow for a larger volume of PCM to be used. This study combines the thermal energy storage capabilities of PCM and a heat distribution system within the PCM volume consisting of a metal framework. This metal framework improves heat transfer to the PCM during overload but also compensates for the relatively poor thermal conductivity of the PCM during normal operation. This improvement directly affects the period for which the junction temperature of an IGBT remains below its maximum SOA, during a short-term current (or equivalent heat flux) increase.

3.2 Finite Element Analysis and Power Dissipation Modelling

Finite Element Analysis (FEA) can provide validation through virtual experiments of systems which involve fields of various types, and it can reduce product validation or testing costs. It was decided to assess the effectiveness of adding PCM to the heat-sink of an IGBT for thermal management through FEA. In the finite element method, a numerical method is used to solve the partial differential equations of a field, in our case a thermal field with a heat flow. This method provides only an approximate solution by discretization of the structure into small portions or elements. There are different types of elements that can be used to create such as 1D lines and 3D solid elements. The connecting points between elements are called nodes. They can be applied to several physical domains such as structural and thermal / fluid. The FEA procedure includes the following:

1. Pre-processing
    a. Discretization of the structure – meshing
    b. Assign element types and properties
    c. Assign material properties
    d. Apply boundary conditions and loads
2. Solution
    a. Appropriate solver selection
    b. Calculate element stiffness matrices

c. Solve for displacement, strains, stresses etc.

3. Post-processing
    a. Display / output results
    b. Calculate user defined parameters from the results

During FEA it is essential that units are consistent across all parameters and material properties are assigned accordingly. The boundary conditions for each zone must reflect the actual problems' requirements.

Fluent (a commercial product from Ansys) was selected as the FEA software package to be used and it provides all of the features listed above. The thermal model of the IGBT and PCM thermal management system will need to be provided with information about the heat dissipation in the IGBT that arises from its conduction and switching. This is not modelled within Fluent but in a separate modelling exercise that would provide a description of heat dissipation as a function of time.

The IGBT module selected for this study is manufactured by ABB with part number 5SNA 1200E330100 and is widely used in high-power applications [94]. This IGBT's voltage and current ratings are $3.3\,kV$ and $1.2\,kA$ respectively. The intention of the study is to understand the relationship between over-current magnitude and the time taken for the temperature to rise to the limit of safe operation. A large synchronous generator can also contribute 3 - $10\,pu$ fault current, depending on fault impedance, and that a value at the lower end of the range is typical for a more remote fault [7]. At this stage, the model will be first examined for estimated power losses, which would be comparable to the device conducting three times its nominal current rating or $3\,pu$. Although power loss is not strictly proportional to current it is quite close to proportional for a high power IGBT.

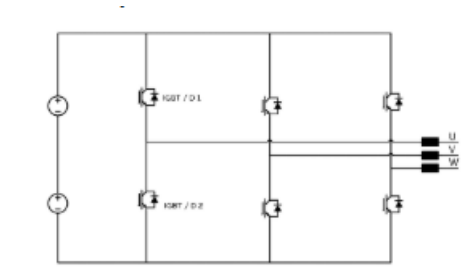
ABB, the selected module manufacturer, provides an online power loss simulation tool for its own products known as SEMIS. This online thermal simulation tool helps designers improve the energy efficiency and performance of power converters. It evaluates semiconductor switching waveforms and power losses for devices chosen from its product range for more than 20 example circuits and standard modulation schemes. The SEMIS simulations are based on the Plecs® Software and provides detailed graphical and numerical reports covering currents, voltages, power losses and junction temperatures [95]. It can be used to determine swiftly critical elements that can be changed to improve converter efficiency, cost and lifetime.

To explore the power losses seen in the selected module for an operational configuration, this online thermal simulation tool was used. The simulation shows a power loss of $2.67\ kW$ per module when utilised in a 3-phase two-level VSC circuit operating at $850\ A$ phase current from a $1{,}800\ V$ DC link, as shown in Figure 3-1.

A key question to answer is over what duration an over-current can be sustained before breaching thermal SOA of the semiconductor. The time duration available from a PCM-equipped power converter can then be compared to that from a typical synchronous generator.

A possible limitation of PCM as a thermal management tool is the non-uniform temperature distribution across the PCM due to their low thermal conductivity and the impediment this presents to storing or discharging heat energy within the depths of the material. In [96], an aluminium metal foam with PCM in within the foam structure was seen to reduce the time for discharging the stored heat by 42% and decreased charging time by 15%. It also reduced the maximum temperature during heating by almost 11% and improved the uniformity of heat distribution. To improve heat distribution to the PCM, a copper "mesh" was formed with the PCM inserted in the voids of this mesh.

This study involves simulation of the thermal network of a power module with different packaging structure and materials with the transfer of heat loss from top layer of silicon to the bottom layer of heat sink. A 3D model of an example IGBT, heatsink and metal-mesh/PCM insert will be built to enable further understanding of the thermal properties of power electronics systems under over-load conditions. Understanding how temperatures evolve over time with and without PCM and for various dimensions of each element may enable development of technologies to improve energy density or overload capability.



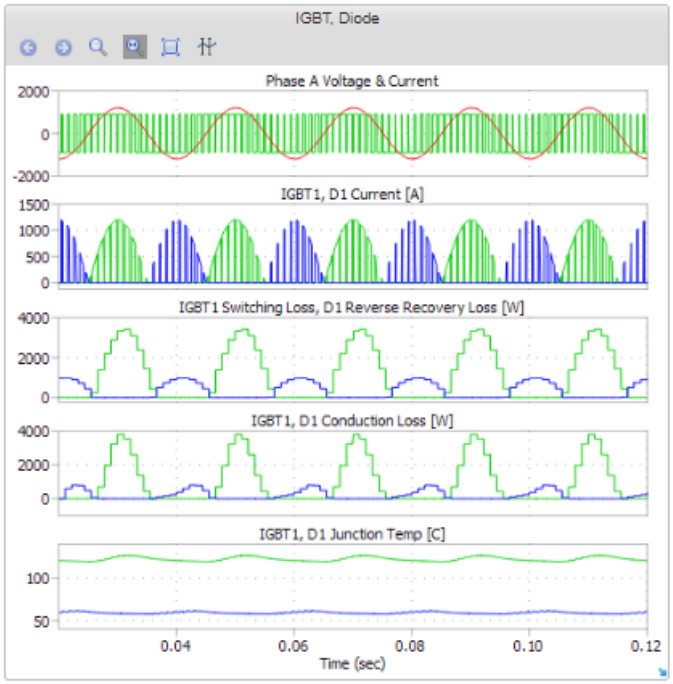
CONVERTER OPERATION:	Inverter
AMBIENT TEMPERATURE:	20 °C
SYSTEM FREQUENCY:	50 Hz
SWITCHING FREQUENCY:	900 Hz
PWM STRATEGY:	Sinusoidal PWM
MODULATION INDEX :	0.8
DC VOLTAGE:	1800 V
AC REFERENCE PARAMETERS:	AC Current
AC SIDE CURRENT (RMS):	850 A
POWER FACTOR VALUE:	0.8
POWER FACTOR TYPE:	Inductive (Converter)
HEAT SINK THERMAL RESISTANCE:	0.01 K/W
IGBT MODULE TYPE:	HiPak
IGBT SELECTION:	3.3 kV
MODULE CONFIGURATION:	Single IGBT

Matching IGBTs:

- 5SNA 0800N330100 800 A
- ☑ 5SNA 1200E330100 1200 A
- 5SNA 1200G330100 1200 A
- 5SNA 1000N330300 1000 A, 150C
- 5SNA 1500E330305 1500 A, 150C
- 5SNA 1800E330400 1800A - PRELIMINARY

Steady State | Hold result

Analysis completed.



Device Losses & Temperatures

	Switching	Conduction	Combined Losses	TvjAvg	TvjMax	TvjBLS
per IGBT	1.152 kW	977.62 W	2.129 kW	122.27 °C	127.07 °C	126.32 °C
per Diode	339.42 W	198.92 W	538.35 W	59.03 °C	61.81 °C	60.83 °C
Converter Losses	8.95 kW	7.06 kW	16.01 kW			
% Losses			1.52 %			

AC Parameters

	Real Power	Reactive Power	Phase Voltage (RMS)	Phase Current (RMS)	Output Frequency	Power Factor
	1.038 kkW	778.8 kVAR	509 V	850 A	50 Hz	0.80

DC Parameters & Control Parameters

	DC Power	DC Voltage	Switching Frequency	Modulation Index
	1.054 kkW	1.800 kV	900 Hz	0.80

Figure 3-1: ABB thermal simulation tool provides power loss of 2.67kW per module when utilised in a three-phase two-level VSC circuit topology [95]

3.3 Analysis of the Proposed System

Manufacturers typically require that the maximum temperature at the junction of the silicon dies of an IGBT to be limited to below 150℃, and that the operating temperature under normal conditions be limited to 80% that of the maximum value [33]. Devices with higher current ratings are typically limited to a lower $T_{j(max)}$ value of 125℃. Operating the device above its rated $T_{j(max)}$ can lead to a breakdown in reverse voltage blocking capability and thermal runaway, leading to device destruction. The system must be designed so that the junction temperature never exceeds the rated $T_{j(max)}$ value [97] .

A designer will calculate the operating temperature, $T_{j(op)}$ for normal operation using the sum of the conduction losses and the switching losses together with the thermal impedance. During the design process, an upper limit will be placed on $T_{j(op)}$ that is considerably below $T_{j(max)}$ so as to provide a safety margin, even in the case of overloads, and to also reduce the ageing effect of operating at higher temperatures. In this study, the maximum value of $T_{j(op)}$ for normal operation has been set at 80℃ but during the overload condition, the device T_j is allowed to rise to 140℃, which is below the rated $T_{j(\max)}$ of 150℃ for the selected IGBT.

In addition to the damage to the device caused by excessive temperatures, any cycling of power losses and junction temperature that a module undergoes during its operation can have a large impact on the expected lifetime of the module [18]. This cycling is broken down into two-time scales. The first timescale, called power cycling, occurs at time frames of around $2\,s$. This thermal cycling causes stress in the soldering of the electrical connections within the IGBT module due to the different coefficients of linear expansion. If the power cycling causes the soldering to deteriorate sufficiently then the device will experience electrical failure. Cycles at a longer timescale and with a larger change in temperature (i.e. $4 \times T_j$) are referred to as thermal cycling. This causes unequal expansion of the insulation substrate and the copper base-plate within the modules, which results in fatigue to the solder layer between them [98]. This can lead to device failure as it causes the thermal resistance of the module to increase, leading to thermal runaway as the device can no longer dissipate the power-losses incurred within the silicon dies.

Manufacturers usually provide information on power cycle and thermal cycle capability as a set of curves for IGBT modules which allow the estimation of the lifetime of the modules. The

degradation of lifetime is dependent on absolute junction temperature as well as the magnitude of the power or thermal cycle [98]. Looking beyond lifetime issues for high power applications, it is desirable to keep the junction temperature as low as reasonably possible. This is because the level of thermally generated electron hole pairs increases with temperature, thus decreasing the conductivity of the device and leading to an increase in power losses.

The external view of the model of an IGBT module (5SNA 1200E330100), together with IGBT and diode arrangement and an illustration of the internal construction are shown in Figure 3-2 subplot (a), (b) and (c) respectively.

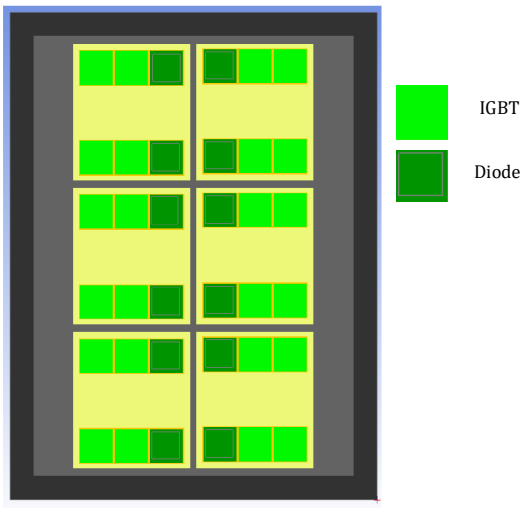
Each IGBT module is formed by a parallel connection of several IGBT dies and diode dies that are connected together through an internal busbar and wire-bond connections. For a high-power IGBT, such as the one used in this chapter, there can be as many as 24 IGBT dies connected in parallel with 12 diode dies Figure 3-2 (b). The electrical connections to the module are made via bolts that protrude from the top of the devices case. These bolt connection points are directly connected to aluminium busbars within the module. These busbars are connected to the IGBT and diode silicon dies within the module. These dies are grouped in three, two IGBT dies and one diode die, mounted upon a copper sub-busbar. Two of these groups are then mounted upon a ceramic insulator, six of which form the overall module. The Aluminium Nitride (AlN) ceramic insulators are bonded to a baseplate formed of Aluminium Silicon Carbide (AlSiC). The baseplate forms the outer surface of the bottom of the IGBT module packaging.

The density, specific heat capacity and conductivity values of the modules' internal layers are given in

Table 3-1. These are the values used in the Ansys Fluent model and have been taken from [33].



(a) External View - Source: ABB.



(b) IGBT and diode arrangement in the module



(c) Internal Construction

Figure 3-2: IGBT Hi-Pak Module [33]

Table 3-1: Devices internal layers physical properties

Material	Density (kg/m^3)	Specific Heat ($J/kg\ K$)	Thermal Conductivity ($W/m\ K$)
Silicon and Solder	2,330	556.9	130
Copper	8,933	195	387.6
Aluminium Nitride (AlN) - Solder and Copper Layer	4,172.4	249	153
Thermal Grease	1,000	1,000	1
Aluminium Silicon Carbide (AlSiC)	2,890	808	165
Extruded Aluminium	2,800	900	205

The considered IGBT module internal layers and their dimensions are shown in Table 3-2. It is expected that thermal impedance from the silicon dies, through the bond-wires and the modules busbars path is dominated by the route down through the module's baseplate to the heatsink. It is noted that several layers are combined for modelling purposes following the approach adopted in [33].

3.3.1 Simulation Pre-Processing – Geometry Construction of the IGBT

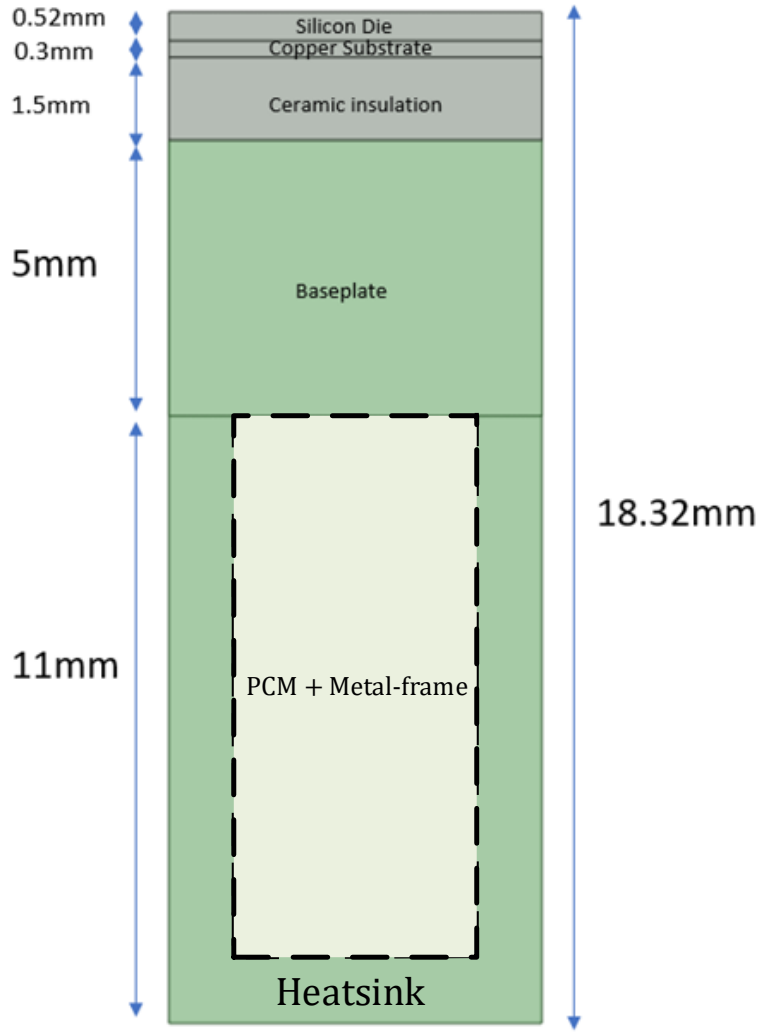
The FEA requires significant computing power to simulate a full model of an IGBT. Given the computation time needed for large structures, only one of the twenty-four units of IGBT is modelled. The simulation volume consisted of all the layers of the module plus metal frame and PCM embedded in the heatsink. A single-die geometry was constructed for the FEA simulation as shown in Figure 3-3 and Figure 3-4.

Table 3-2: IGBT module internal layer dimension

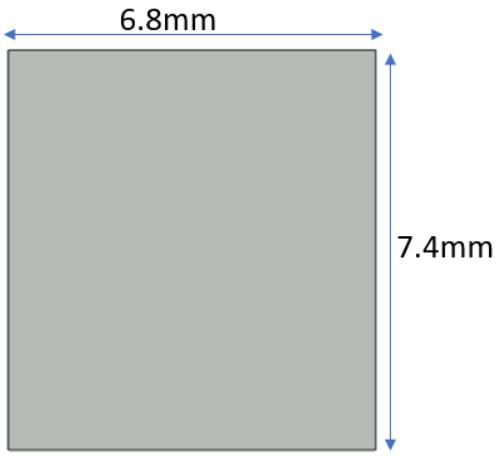
Layer	Material	Length (mm)	Width (mm)	Depth (mm)
Silicon Die	Silicon and Solder	14.06	14.34	0.52
Copper Substrate	Copper	45	15.17	0.3
Ceramic Insulation	AlN, Solder and Copper Layer	49.53	58	1.5
Baseplate	AlSiC	137	187	5
Thermal Grease	Thermal Grease	137	187	0.05
Heat-Sink	Extruded Aluminium	157	207	10

Most of the heatsink volume is occupied by the metal frame and PCM. The walls and base of the heatsink are 1 mm thick to provide mechanical strength and an additional heat conduction from baseplate of the module to the base of heatsink. The scaled geometry and metal frame have been created in the SpaceClaim component of Ansys Workbench. The PCM fluid region has been created around the metal framework with the inverse "volume methodology" using the DesignModeller component of Ansys Workbench. The copper-based metal framework was created to resemble a honeycomb structure to maximise the surface interaction with the PCM.

As was noted in Section 2.2, it is expected that modifying a heatsink in this fashion to accommodate PCM within a metal frame will be somewhat easier than making changes in semiconductor package. With "spherical" shaped holes in the metal frame, a PCM volume of $\cong 225\ mm^3$ was created, which forms approximately 41% of the total volume of the heatsink region. The iterative simulation results showed that maximum thermal flow occurred from silicon die to heatsink when the volume of PCM and metal frame was between 40% and 42% of the total volume of the heatsink region.



(a) Side View



(b) Top View

Figure 3-3: Modelled IGBT (ABB 5SNA 1200E330100) with Heatsink

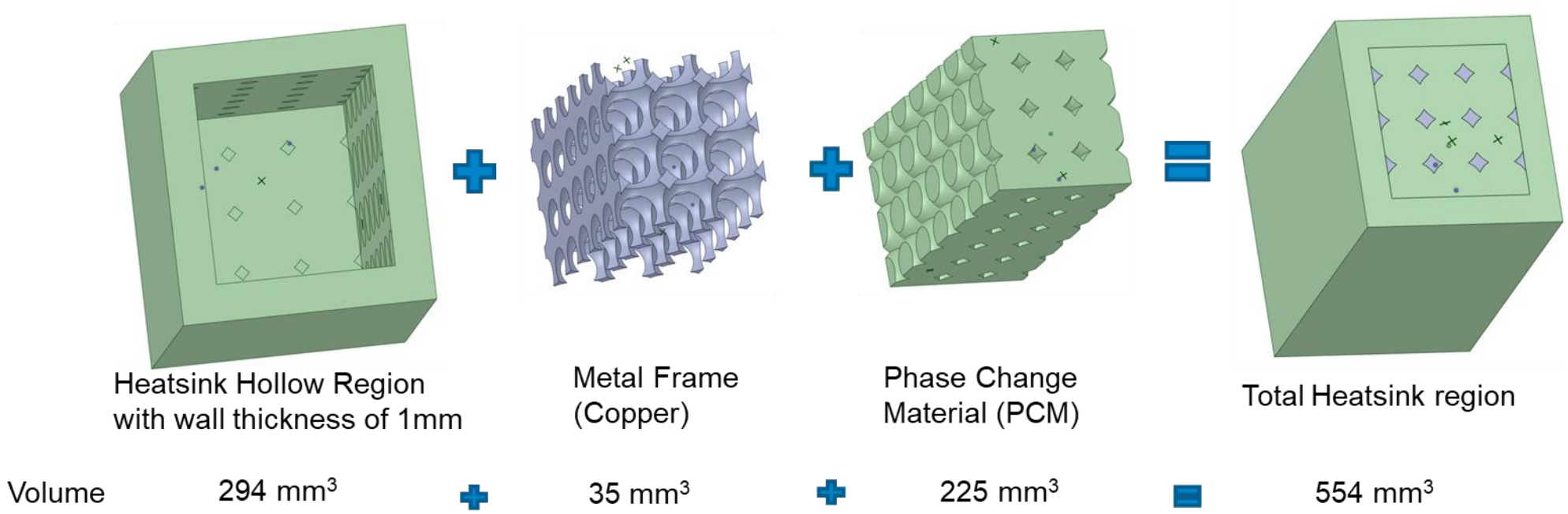


Figure 3-4: Heatsink Integrated with Metal Frame and PCM

3.3.2 Phase Change Material Selection

A particular thermal metal paste, LM80 [18], has been chosen over other candidate materials because of its high density, leading to high latent heat, and reasonably good thermal conductivity properties. The properties of LM80 [18][18][18][17][16]are listed in Table 3-3 [18]. The LM220 material also listed here is similar to LM80 in all regards except for the melting temperature which is much higher and above the operating temperatures. It will be used as a comparison case in which the PCM is not activated.

Table 3-3: PCM Materials physical properties [18]

	PCM Materials	
	LM80	LM220
Density (kg / m^3)	6,300	6,300
Specific Heat (J / kg.K)	250	250
Thermal Conductivity (W / m.K)	35	35
Pure Solvent Melting Heat (kj / kg)	115	115
Solidus Temperature (°C)	79	119
Liquidus Temperature (°C)	80	220

3.3.3 Simulation Conditions

The assessment of the performance of PCM in a heatsink was through time-step simulation of the FEA model as described in this section.

All regions of the single-die volume were defined as solid apart from the PCM. To simulate a PCM in Ansys Fluent, the material is initially classified as fluid region even though the

solidification and liquification temperature are provided. For this simulation, there was no need to create a void in the heatsink for expansion of the PCM liquid because the metallic PCM has high density, and the volume increase is small.

The IGBT module used in this study is identical to the one used in the experimental set up of [99] and so it is reasonable to use some of the results from that study to create the case-studies here. In [99], boundary conditions were defined for each named selection and the silicon die (IGBT) was subjected to heat flux. The heat flux power density of $4\ kW$ was taken as $1\ pu$ following the example quoted in the experimental results in [99]. In this experimental set [99], measurement of junction temperatures of dies inside a $3.3\ kV$, $1.2\ kA$ HiPak IGBT module from ABB was performed using infrared sensing. The measured temperatures were compared to a 3D-FEM model of the power module and a water-cooled heatsink. The thermal measurements of the open module confirmed the accuracy of the 3D-FEM model. It is worth noting however that the module heat dissipation of $4\ kW$ observed in [99] is 30% higher than the value obtained from the SEMIS tool when modelling a three-phase bridge with the conditions shown in Figure 3-1. Nonetheless, $4\ kW$ was taken as the heat dissipation for the rated operating point ($1\ pu$). The $1\ pu$ value was divided by the baseplate area of $0.0256\ m^2$ (Table 3-2) to give a heat flux density of $156\ kW/m^2$ which was rounded to $160\ kW/m^2$ for the simulation. The rounding of the heat flux density is expected to account, in part, for the inaccuracy introduced by combining layers of the IGBT. For the case $3\ pu$ the heat flux densities were set at $480\ kW/m^2$.

For the purposes of the simulation, lateral heat transfer between 24 PCM elements embedded in the heatsink is ignored on the basis that they are identical. It also ignores the fact that some heat-loss will occur through the sidewalls at the edges of the group of 24. As shown in Figure 3-5, it is assumed that all the heat is flowing from silicon die to the base of the heatsink. Also, the heat transfer into the water of the water-cooled baseplate has not been modelled and instead the boundary condition for the base of the heatsink is set to be a temperature of $20℃$ with transfer coefficient $4{,}400\ W/(Km^2)$. The heat transfer co-efficient value for water cooling was taken from the experimental set up of [99], in which the water temperature at the inlet of the pipes is at $20℃$, the water flow through the plate was set to $23.3\ litres/minute$.

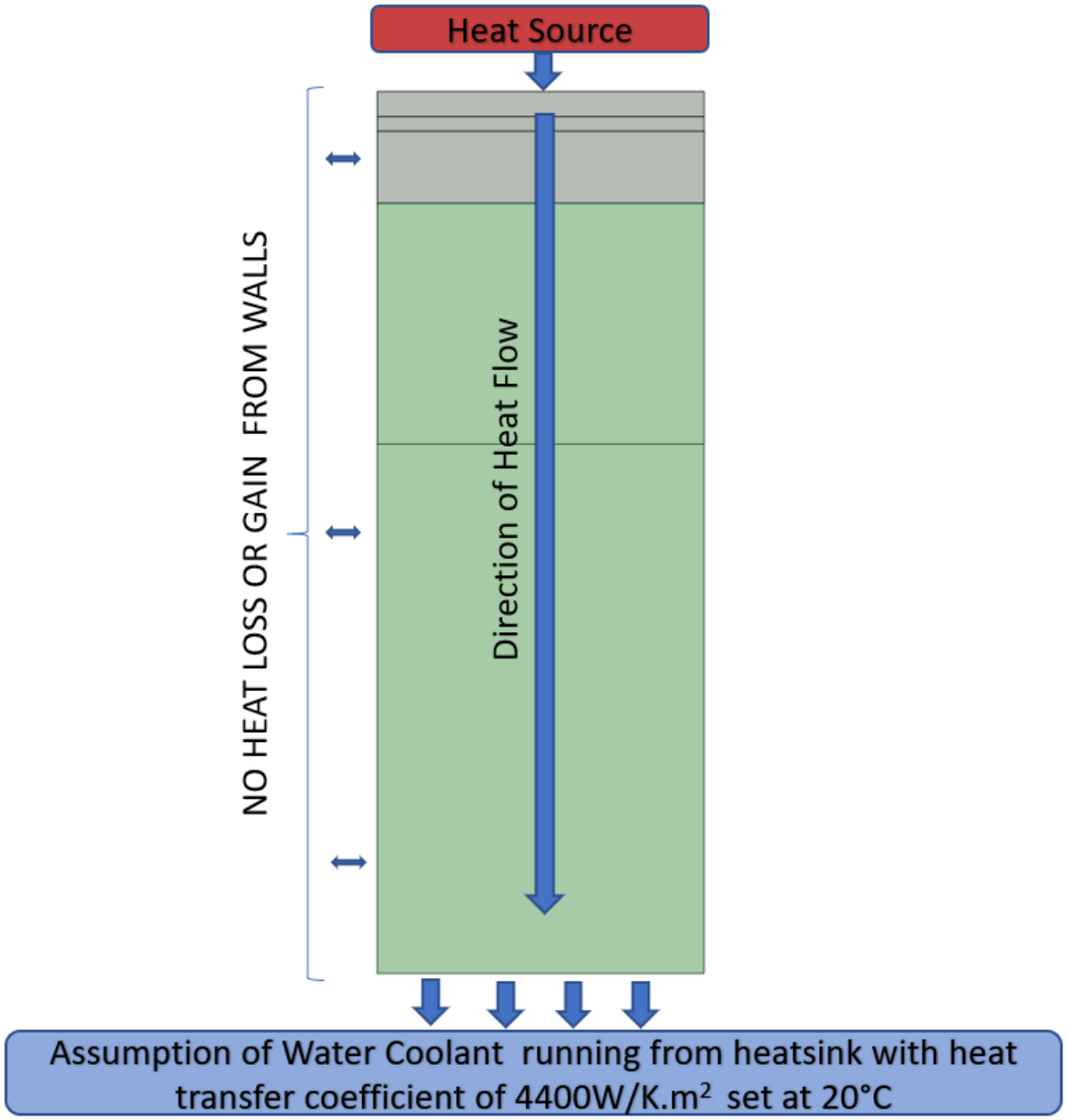


Figure 3-5: Simulated model in Ansys Fluent

This study will assess the time for which the junction temperature can be held low by the presence of PCM by comparing the LM80 PCM with an inactive (high temperature) PCM, LM220. The conditions for the tests are detailed in Table 3-4.

In order to describe and understand the temperature profile of the silicon die (IGBT) and PCM in each of the case studies, the graphs have been divided into different zones. In general, the graph can be divided into four zones, namely the initial temperature rise zone (Zone 1) as the simulation starts-up, the initial steady-state zone (Zone 2) as the temperatures settle for the 1 pu heat loss condition, the heat-increase transient zone (Zone 3) which covers the rise of

temperature when the heat flux is increased (and includes PCM melting where that applies) and final steady-state temperature zone (Zone 4) when the new settled temperatures for the high heat flux case are seen. The temperatures recorded during the simulation are an "Area-Weighted Average" calculated within Fluent across the surfaces in question such as the surface of the IGBT or PCM [100].

Table 3-4: Two cases considered for simulation

Simulation Cases	Heat flux (kW/m^2)	PCM melting temperature (℃)
Case 1 - One step-change ($1\ pu$ to $3\ pu$)	160 to 480	80 and 220
Case 2 - Two step-changes, ($1\ pu$ to $3\ pu$ and back to $1\ pu$)	1st step change: 160 to 480 2nd step change: 480 to 160	80

3.3.4 Thermal Network of the Proposed System

An approximate thermal network for the proposed system of IGBT with integrated PCM heatsink is shown in Figure 3-6. Notations in Figure 3-6 are defined as follows (subscripts denote a particular location or part of the expected assembly):

P_{Loss} IGBT power loss (kW)

T_j IGBT junction temperature (℃)

$R_{th(j\text{-}c)}$ Thermal resistance junction to case (Ω)

T_c IGBT assembly case temperature (℃)

$R_{th(c\text{-}h)}$ Thermal resistance case to heatsink (Ω)

T_h Heatsink surface temperature (℃)

$R_{th(metal\text{-}frame)}$ Thermal resistance of the metal frame in the heatsink (Ω)

$R_{th(PCM)}$	Thermal resistance of the PCM — LM80 (Ω)
$R_{th(h\text{-}walls)}$	Thermal resistance of the heatsink sidewalls (Ω)
$R_{th(h\text{-}base)}$	Thermal resistance of the heatsink base (Ω)
$R_{th(h\text{-}water)}$	Thermal resistance of the heat transfers co-efficient — heatsink to water cooling system (Ω)
T_{water}	Temperature for water cooling system (℃)

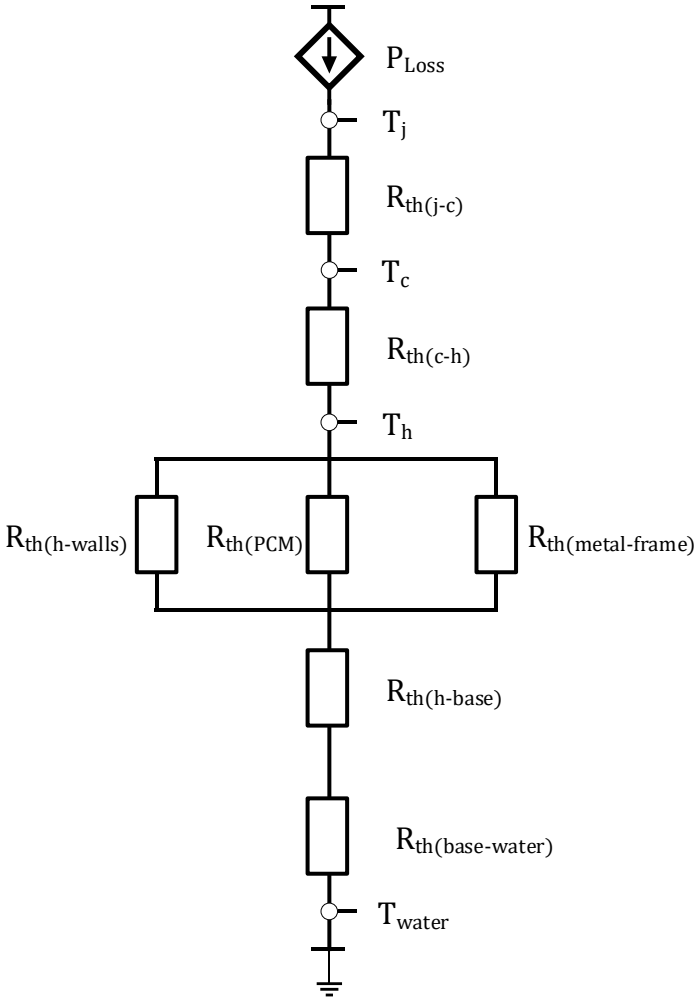


Figure 3-6: Approximate Thermal Network for the Proposed System of IGBT Hi-Pak Module with PCM and metal-frame

Using the approximate thermal network, the average junction temperature can be calculated by using equation (3.1).

$$T_j = P_{Loss}\left[R_{th(j\text{-}c)} + R_{th(c\text{-}h)} + R_{th(h\text{-}water)}\right] + T_{water} \quad \textbf{(3.1)}$$

The thermal resistance between heatsink and the cooled water includes thermal resistance of the heatsink walls, metal-frame and PCM in parallel (Figure 3-6) and is represented by equation (3.2). This equation considers the area-weighted average of the heatsink, metal-frame and PCM.

$$\frac{1}{R_{th(h\text{-w})}} = \frac{1}{R_{th(h\text{-}walls)}} + \frac{1}{R_{th(PCM)}} + \frac{1}{R_{th(metal\text{-}frame)}} \quad \textbf{(3.2)}$$

The thermal resistance for each sub-assembly can be calculated by taking into account the geometry of the area and its thermal conductivity. This can be expressed as the equation (3.3).

$$R_{th} = \frac{d}{\lambda \times A}\ (K/W) \quad \textbf{(3.3)}$$

Where:

$d =$ depth of assembly part (m);

$A =$ area of each assembly part (m^2);

$\lambda =$ thermal conductivity of assembly part $(W/m.K)$.

The calculated total resistance ($\boldsymbol{R_{th(total)}}$) of the proposed IGBT assembly with PCM and metal frame is $\mathbf{7.04\ K/W}$ and the calculation is shown in Table 3-5. The values of area and depth are taken from the geometry created in Ansys (DesignModeller). Thermal conductivity of each sub-assembly of the proposed assembly is listed in

Table **3-1** and Table 3-3.

At $1\ pu$, the P_{Loss} is expected at $160\ kW/m^2$ and considering an area of $50.32\ mm^2$, for the case of a single die, the P_{Loss} for the simulation is $8.05\ W$. The reasoning for selecting P_{Loss} of $160\ kW/m^2$ was detailed earlier in the Section 3.3.3. In this set-up, the ambient temperature (T_a) is the water temperature (T_{water}), which is expected to be maintained at $20℃\ /\ 293\ K$.

Using equation 3.1, T_j can be estimated at 76.6℃ during normal operation $(1\ pu)$ as given by equation (3.4).

$$T_{j\,(1\,pu)} = P_{Loss}\, R_{th(total)} + T_{water} = 8.05\ \times 7.04 + 20 \cong 76.6℃ \qquad \textbf{(3.4)}$$

Similarly, for overload condition at $3\ pu$, the P_{Loss} expected at $480\ kW/m^2$. The T_j can be analytically estimated to reach 190℃ during overload condition $(3\ pu)$ if allowed to persist, as given by equation (3.5).

$$T_{j\,(3\,pu)} = P_{Loss}\, R_{th(total)} + T_{water} = 24.15\ \times 7.04 + 20 \cong 190℃ \qquad \textbf{(3.5)}$$

The above analysis shows that the junction temperature of an IGBT goes beyond its maximum operating temperature of **150**℃, when it is subjected to three times its nominal current. The FEA will show if the PCM can delay this rise in the junction temperature of the IGBT when there is a surge of heat-flow.

Table 3-5:: Thermal resistance calculation for each sub-assembly of the proposed IGBT

Assembly part	Area (mm^2)	Depth (mm)	λ $(W/m.K)$.	Thermal Resistance (K/W)
IGBT	50.32	0.52	130	0.079
Copper	50.32	0.3	387.6	0.015
Ceramic	50.32	1.5	153	0.195
Baseplate	50.32	5	165	0.602
Heatsink walls	26.4	11	205	1.63
Metal-frame (inside the heatsink - average cross-sectional weighted area)	3.53	10	387.6	7.3
PCM (inside the heatsink -average cross-sectional weighted area)	22.4	10	31	14.4
Heatsink walls, metal frame and PCM in parallel				1.22
Heatsink base	26.4	1	205	0.409
Heat transfers co-efficient from base to water estimated at 4,400 $W/K.m^2$	50.32			4.52
Total Combined Thermal Resistance of the proposed assembly with PCM and metal frame $(R_{th(total)})$	0.079 + 0.015 + 0.195 + 0.602 + 1.22 + 0.409 + 4.52 = **7.04** K/W			

3.3.5 Mesh

After the geometry was finalised, it was meshed in preparation for FEA. Ansys Workbench Mesh was used for this task, and it created a tetrahedral mesh. However, the meshing was further improved by Ansys Fluent Mesh and was converted to polyhedral mesh for the baseplate and heatsink regions to achieve a greater accuracy with a lower cell count [101]. The geometry was developed using "Share Topology" to allow a conformal mesh within the model. An inflation mesh was used for the melting zone of PCM and around the metal framework to ensure more accurate resolution of the boundary layer. Using Ansys Fluent successive smoothing sweeps were performed on the mesh to improve the representation. Figure 3-7 shows the cross-section view of the mid-point in the geometry. The tetrahedral and polyhedral meshes can be identified.

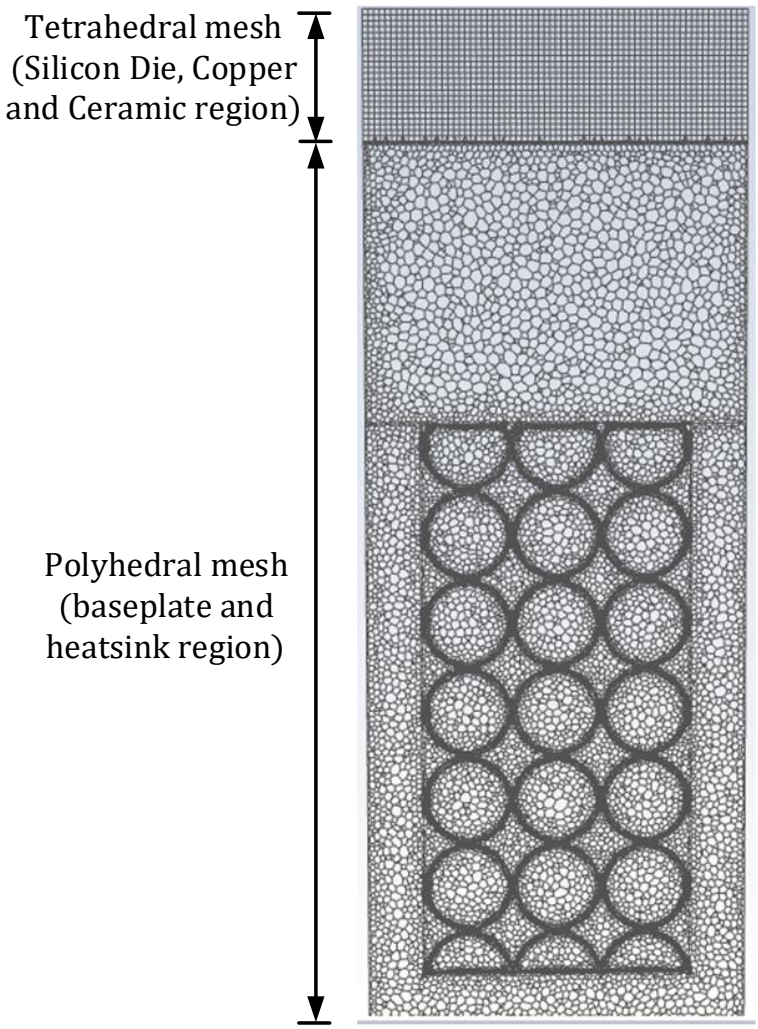


Figure 3-7: Cross section view of the mid-point in the geometry

3.4 Simulation Results

The simulation results for the two cases are presented below.

3.4.1 Case 1: Heat flux increased from 1 pu to 3 pu

In this case study, a comparison of the temperature profile for silicon die / IGBT and PCM is carried out between active and inactive PCM. In the first simulation the PCM melting temperature is set to its rating of 80℃ for LM80 and then in a second it is set at 220℃ for LM220 so that in effect the PCM is deactivated. The data points for area weighted average temperature for IGBT and PCM are transferred from Fluent to Excel for analysis. The percentage of volume of PCM that has melted is also recorded. The simulation results for the LM80 and LM220 cases are then overlaid on a single graph for analysis as shown in Figure 3-8.

Within zone 1 of the results the model is subject to 1 pu heat flux. At 1 pu, the LM80 PCM does not melt as the highest average temperature is 63.4℃ and well below the melting temperature of 80°C. At the end of zone 2, the IGBT and PCM temperature for LM80 and LM220 settle at the same final values of 77.07℃ and 63.5℃ respectively.

At 100 s, the step change in heat flux is initiated and is raised to 3 pu which marks the beginning of zone 3. Figure 3-8, shows that the temperatures in the PCM rises rapidly because the step-change in heat-flux to 3 pu. Only 0.8 s after the increase of heat dissipation, the LM80 PCM starts to melt which can be seen in the the slower rise of temperature of the LM80 (purple trace) than the LM220 (green trace). There is a corresponding lower rate of rise of temperature of the IGBT in the LM80 case (orange) versus LM220 case (yellow). The assumed maximum junction temperature of 140℃ (the datasheet allows for 150℃ but a safety margin has been added) is used as the threshold for comparison. With the LM80 PCM, the IGBT reaches 140℃ after 19.8 s, following application of the 3 pu step change, whereas with LM220 (an inactive PCM) it takes only 7.2 s. Thus, the use of a PCM extends the time at which the IGBT can operate at 3 pu heat loss by 12.6 s.

For a solid aluminium heatsink, that is, with no PCM (the blue trace), the IGBT temperature rises to a maximum of 178℃ when the heat-flux is increased to 3 pu and takes 9.8 s to reach 140℃, so the LM80 PCM provides an advantage of 10.0 s longer before this temperature is reached. The case of the LM220 PCM is also shown. It is not expected that the LM220 PCM

will melt and because it is of poorer conductivity than aluminium and occupies 41% of the heat-sink region. As can be seen by the yellow trace, the no-PCM case stays below 140℃ for 2.6 s longer.

Zone 4 of Figure 3-8 shows that ultimately the IGBT and PCM temperatures for LM80 and LM220 settle at the same final values of 190.9℃ and 150.2℃, respectively. However, these are conditions that should not be allowed to occur, and the over-current condition should be terminated with the IGBT safely below these high temperature conditions.

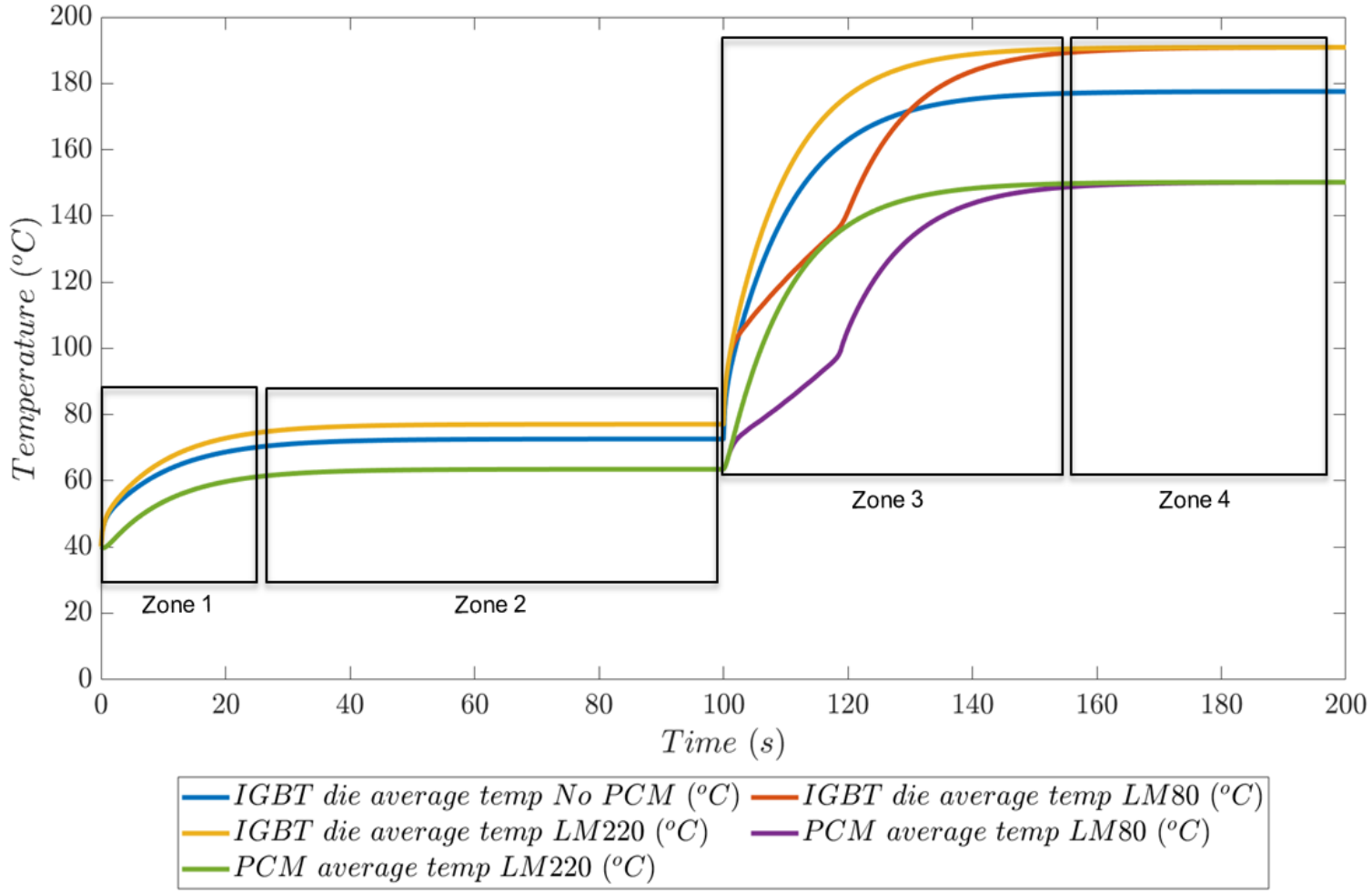


Figure 3-8: Silicon Die (IGBT) and PCM Area Weighted Average temperature when PCM melting temperature set at 80℃, 220℃ and with no PCM; Heat flux set @ 1 pu (160 kW/m^2) and step changed to 3 pu (480 kW/m^2)

Figure 3-9 shows that the PCM melts in the first simulation (LM80) but does not in second simulation (LM220) as the melting temperature is increased artificially for comparison purposes. The PCM reached a maximum value of 150.2℃ and 100% of the PCM melts within 18.2 s from the step change. Case 1 results are summarised in Table 3-6.

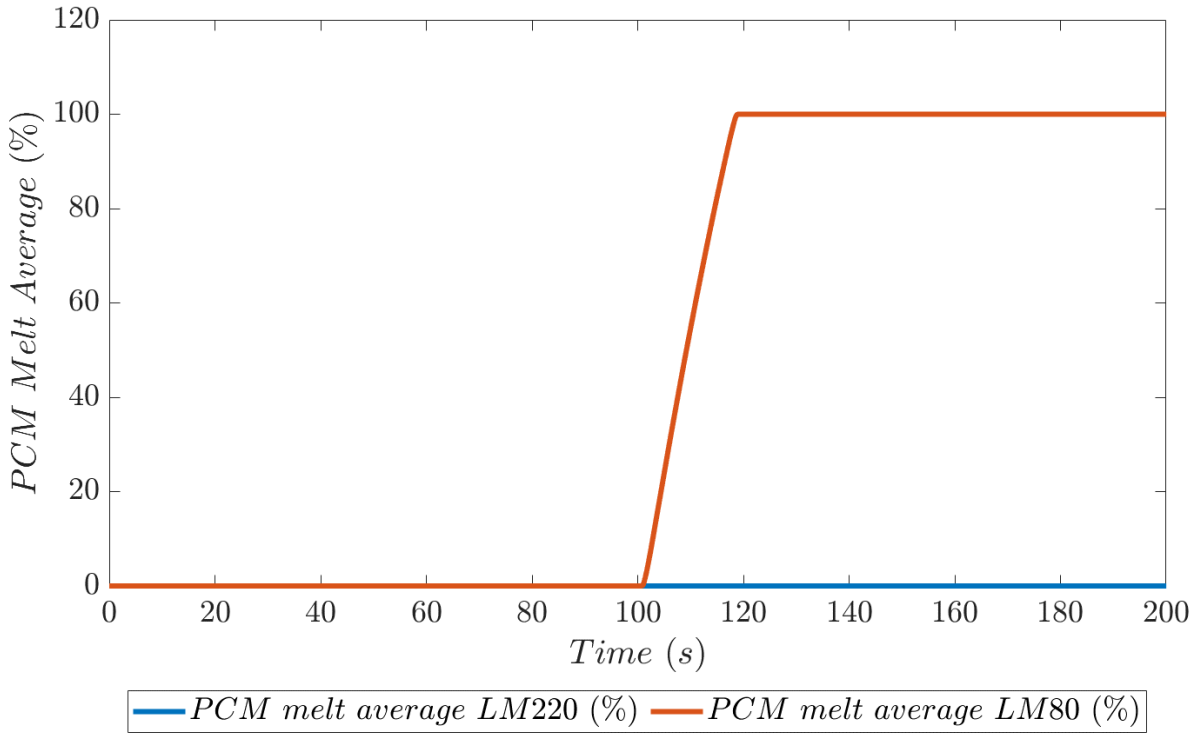


Figure 3-9: Phase Change Material (PCM) Average Melt (%) when PCM melting temperature set @ 80℃ and 220℃; Heat flux set @ 1 pu (160 kW/m^2) and step changed to 3 pu (480 kW/m^2)

Table 3-6: Case 2- Results Summary

	LM80	LM220	No PCM
Maximum IGBT temperature @ 3 pu	190.9℃	190.9℃	177.58℃
Maximum PCM temperature @ 3 pu	150.2℃	150.2℃	N/A
Time to initiate melting when heat flux changed from 1 pu to 3 pu	1.0 s	N/A	N/A
Time duration for IGBT temperature from 77.07℃ to 140℃	19.8 s	7.2 s	N/A
Time to melt 100% of the PCM when heat flux increased from 1 pu to 3 pu	18.8 s	N/A	N/A

3.4.2 Case 2: Heating and Cooling of PCM — Heat flux increased from 1 pu to 3 pu and back to 1 pu

In this case study, both the energy storage and energy release properties of the PCM are analysed through two step changes in heat flux density. The first step change increases the heat flux from 1 pu to 3 pu and the second step change reduced it back to 1 pu. Only the LM80 PCM was examined. As in case 1, the heat flux from 1 pu to 3 pu is applied after 100 s. The results are shown in Figure 3-10 and Figure 3-11. The temperatures observed in zones 1, 2 and 3 are similar to those in case 1, as expected. The second step change, which restores the heat-flux to 1 pu is initiated very shortly after the IGBT temperature reaches 140℃. Figure 3-10 shows the PCM melt average for case 2. The PCM melt average reaches 100% and starts to solidify as soon as the heat flux returns to 1 pu. Zone 4 of Figure 3-11 shows that the PCM takes ≅ 73 s to re-solidify 100% through release of its thermal energy. However, for the IGBT and PCM temperatures the return of the IGBT temperatures to their steady-state values (the beginning of zone 5) takes further 55 s. In total then, a recovery period before the next overload can be allowed of 128 s, or approximately 2 $miutes$ should be allowed. Figure 3-11 shows

that the PCM melting and solidifying durations in the 1st and 2nd step at ≅ 19.8 s and ≅ 73 s respectively. Case 2 results are summarised in Table 3-7.

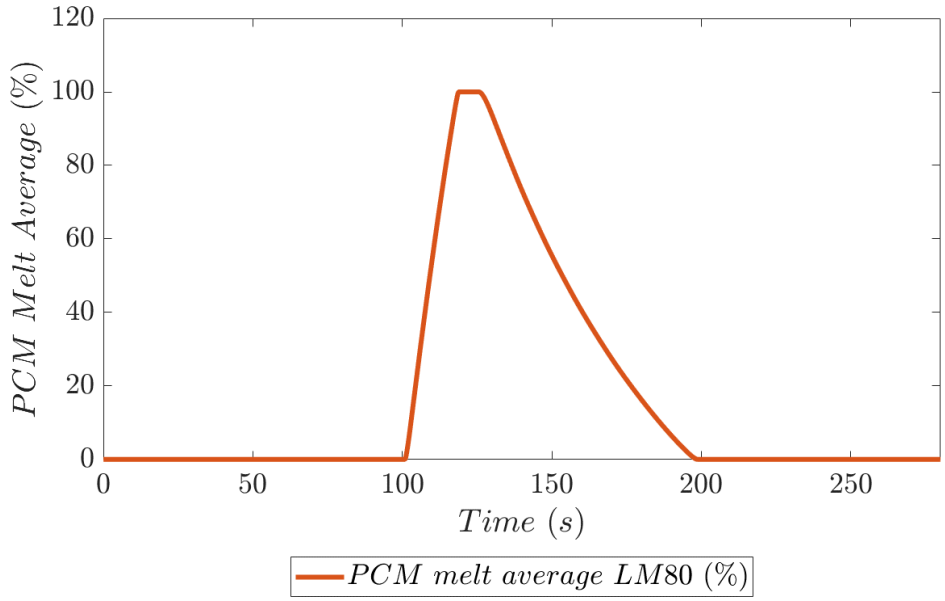


Figure 3-10: Phase Change Material (PCM) Average Melt (%) when PCM melting temperature set @ 80℃; Heat flux set @ 1 pu (160 kW/m^2) and first step changed to 3 pu (480 kW/m^2) and second step changed back to 1 pu (160 kW/m^2)

Table 3-7: Case 2 - Results Summary

	LM80
Maximum IGBT temperature @ 3 pu when heat flux reduced from 3 pu to 1 pu is initiated	141.3℃
Maximum PCM temperature @ 3 pu when heat flux reduced from 3 pu to 1 pu is initiated	105.7℃
Time to initiate solidification of PCM from heat flux reduced from 3 pu to 1 pu	0.6 s
Time to solidify 100% of the PCM when heat flux reduced from 3 pu (141.3℃) to 1 pu (77.07℃)	73 s
Recovery period for PCM – i.e., time taken from 3 pu (141.3℃) to 1 pu (77.07℃)	128 s

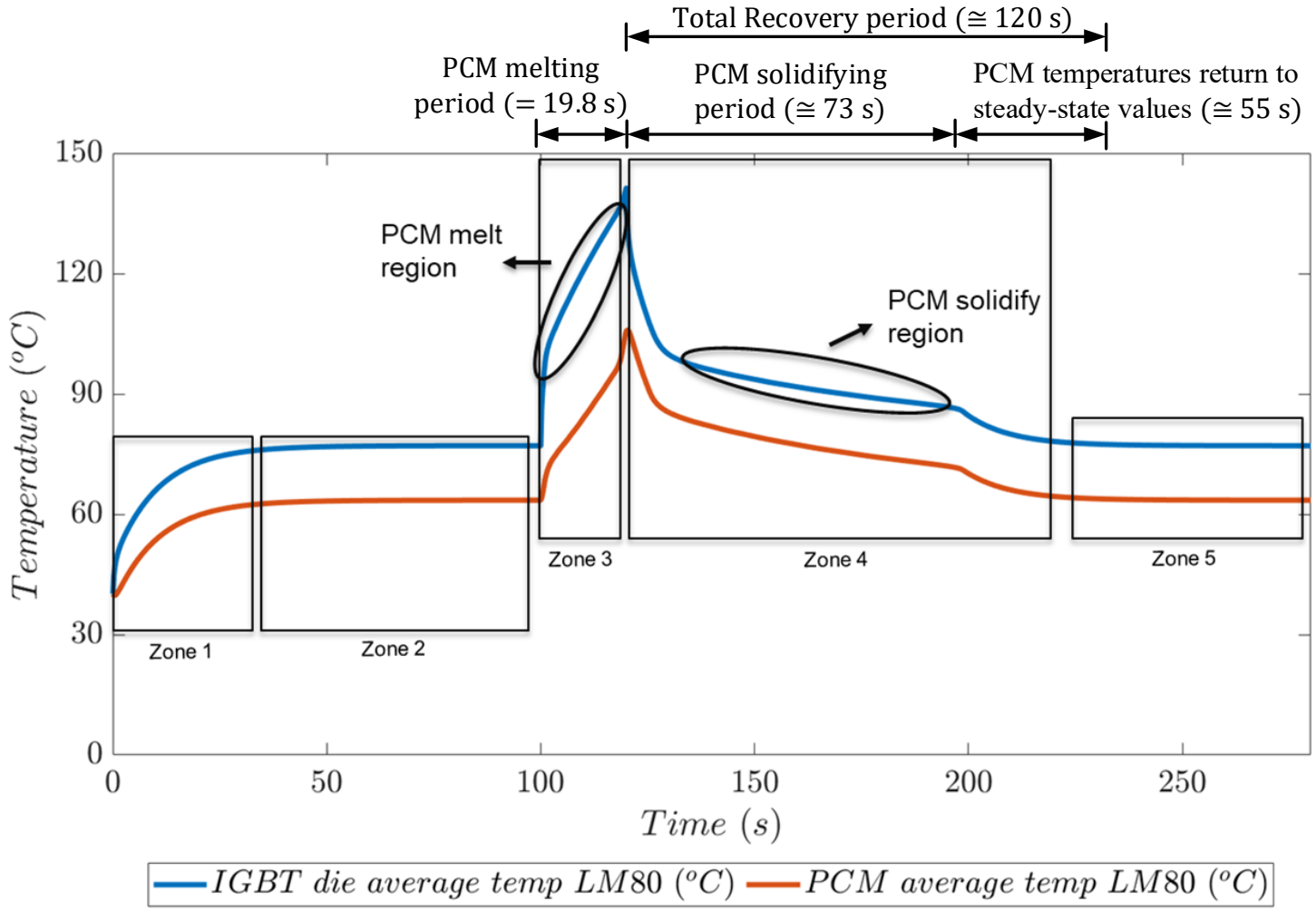


Figure 3-11: Silicon Die (IGBT) and PCM Area Weighted Average temperature when PCM melting temperature set @ 80℃; Heat flux set @ 1 pu (160 kW/m^2) and first step changed to 3 pu (480 kW/m^2) and second step changed back to 1 pu (160 kW/m^2)

3.5 Chapter Conclusions

The study used FEA to assess the incorporation of a PCM in the heat sink. This study demonstrates that by combining the thermal energy storage capabilities of a PCM and a metal framework, the period for which the junction temperature of an IGBT remains below its maximum temperature following a rise in heat dissipation, can be increased and could allow short periods of current flow above $1\ pu$ and the additional heat dissipation that implies.

The PCM LM80 has been chosen due to its high density and high latent heat. The thermal conductivity is also better than many other PCMs such as paraffin wax.

In the first case-study with the LM80 PCM, the IGBT reaches its operating limit of $140℃$ in $19.8\ s$ after the heat dissipation was raised from $1\ pu$ to $3\ pu$, whereas with LM200 (an inactive PCM) it takes only $7.2\ s$. Thus, the use of a PCM extend the time at which the IGBT can operate at $3\ pu$ heat loss by $12.6\ s$. The second case study shows that a recovery period of $2\ minutes$ is estimated before the PCM is ready to again provide short-term over-current capability.

The thermal energy absorption provided by PCM enabled an IGBT to operate at higher-than-normal currents for short periods of around $20\ s$. This short term last long enough for operation of a protection systems but the increase in magnitude is not sufficient for over-current protection. The design could be re-worked for higher currents with greater volumes of PCM but the commutation limit of the IGBT may then prove to be the limiting factor.

The IGBT typically has maximum DC-current that the IGBT-part of the module can conduct is rated at case temperature of $80℃$ but the module has maximum junction temperature of $150℃$. This implies that the IGBT typically has less than twice the thermal limit as its commutation limit [94]. Moreover, the maximum duration of a short-circuit current pulse through the IGBT is limited to $1\ ms$ [94]. Exceeding this duration limit may lead to turn-off failures and depending on pulse duration, may also lead to over-heating of the device resulting in device failure.

It can be concluded that the current limitation in the semi-conductor devices rating meant that thermal management at semiconductor device level was not sufficient for enhanced fault current purposes. If, as indicated here, device-level innovation cannot provide the fault current, then circuit level innovation is required.

3.5.1 Further work

Further investigation could be undertaken to assess whether PCM could facilitate a few seconds of addition load, such as the in-rush current of a new large load. Moreover, a scaled down experimental study would provide further understanding on the methods of implementing the PCM in the heatsink and confirm the results seen in the FEA study.

CHAPTER 4 SERIES / PARALLEL RECONFIGURATION OF MODULAR CONVERTERS

4.1 Introduction

Increasing numbers of IBR are adopting the MMC topology to take advantage of its modular design and low switching power loss. The fact that the MMC is composed of SMs opens the possibility that these SMs can be reconfigured between a series and parallel connection. In normal use, an MMC has many SMs in series to support a high grid voltage. It is possible to build SMs for currents of up to $2{,}000A$ and so parallel connection is not normally required. The opportunity for fault current enhancement is created during a reduced grid voltage (such as a fault condition), where not all the series connected SMs are required for operation at that reduced voltage. Thus, when the stack voltage is reduced, the current flowing through the stack can be increased by taking SMs not needed for voltage support and placing them in parallel for additional current capability. The converter's apparent power rating is not increased because that is fixed by the sum of the ratings of the SMs but voltage is being traded for current through reconfiguration. If, for instance, a fault causes a voltage reduction to less than $0.5pu$ then the series connection of SMs could be split in half and the two halves placed in parallel. This doubles the available current for conditions of halved voltage during faults. The increased current is an increased FCC to the grid that assists effective operation of the protection system. Similarly, if the fault causes a voltage reduction to less than $0.25pu$ then the series SMs could be split into four groups and placed in parallel giving four times the current at a quarter of the voltage. This is the basic idea that will be investigated in this chapter.

It is desirable to provide fault current from all IBR, so, at first, a DC/AC converter (inverter) was examined for series/parallel reconfiguration. This series/parallel reconfiguration takes advantage of the reduced AC voltage to drop the arm voltage, but the DC bus voltage does not reduce. As each arm still needs to support the DC voltage, circuit reconfiguration is not possible, unless the DC bus itself could be isolated from the arms. Isolating the DC bus from the arms would require switches of full DC bus voltage rating, and this additional switch would add to the device count and conduction losses. However, a STATCOM which does not use a common DC bus would not have this problem. A STATCOM can be controlled to provide

rated current as inductive or capacitive reactive current regardless of the grid voltage [70]. This feature of a STATCOM is essential to supply full capacitive current at very low voltage. This feature could be further enhanced if rather than simply rated current, an increased current could be provided at times of severely reduced voltage such as during and after the faults.

4.2 Operational Principles of the Proposed Series/Parallel Circuit

Figure 4-1 shows the proposed series/parallel reconfigurable circuit and its two modes of operation, series mode in subplot (a) and parallel mode in subplot (b). The circuit consists of two stacks of series connected HB-SMs, each rated to 0.5 pu, separated by a break switch and further connected by two parallel switches. In series mode, the break switch remains closed while the two parallel switches are open. This connects the two stacks in series such that they act as one large stack of HB-SMs with a voltage capability of 1 pu. However, the inclusion of the break switch results in increased conduction losses compared to a typical stack of HB-SMs.

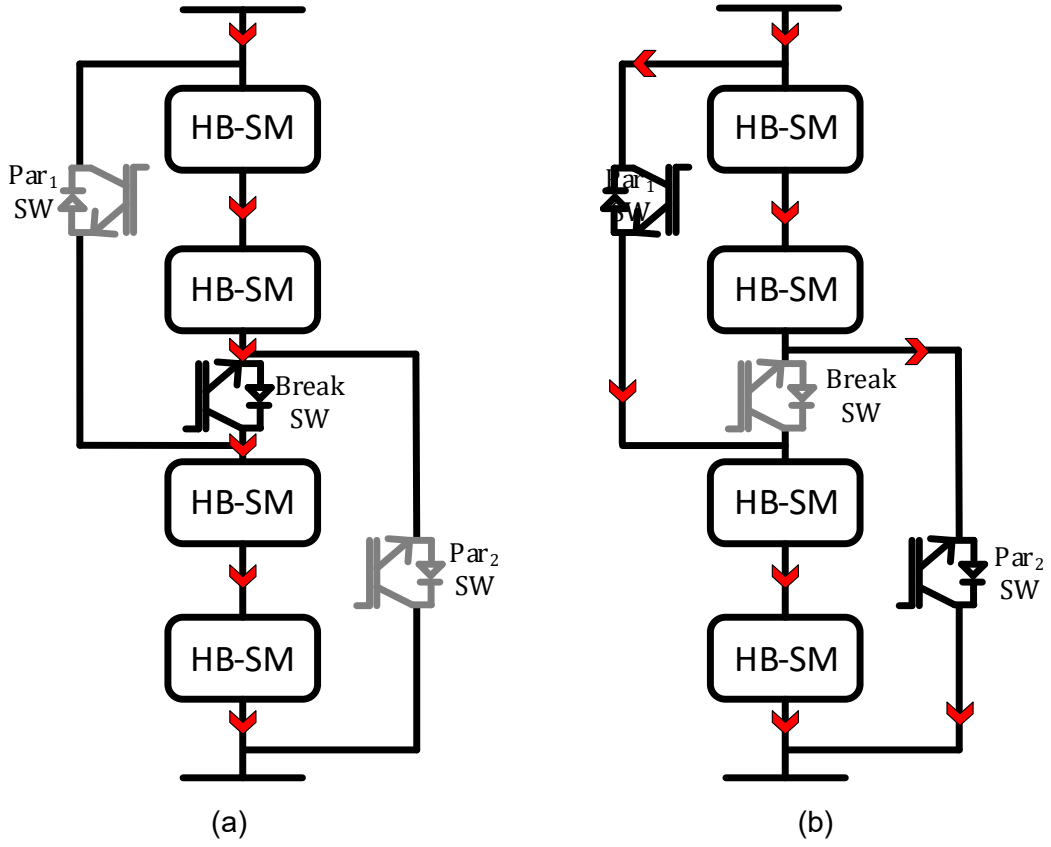


Figure 4-1: Proposed series/parallel reconfigurable circuit with HB-SMs for 2 pu current (conceptual) (a) series operation (b) parallel operation

In parallel mode, the two parallel switches ($Par_1\ SW$ & $Par_2\ SW$) are closed and the break switch is open. This connects the two stacks in parallel. This reduces the voltage rating of the circuit by a factor of two but enables 2 pu of current flow through the circuit while each device in the SMs needs only to conduct 1 pu and thus are not over-stressed. The ability to trade voltage capability for additional current can then be utilized to increase FCC of such a converter.

This circuit can be extended to enable the parallel connection on four stacks of HB-SMs each with a rating of 0.25 pu, however this significantly increases the complexity of the circuit. This would increase the number of breaker and parallel switches required to three and six, respectively. In series mode, shown in Figure 4-2 (a), all four stacks are connected in series to give 1 pu voltage and current. In parallel mode, shown in Figure 4-2 (b), all four stacks are placed in a parallel which gives a voltage capability of 0.25 pu but a current capability of 4 pu.

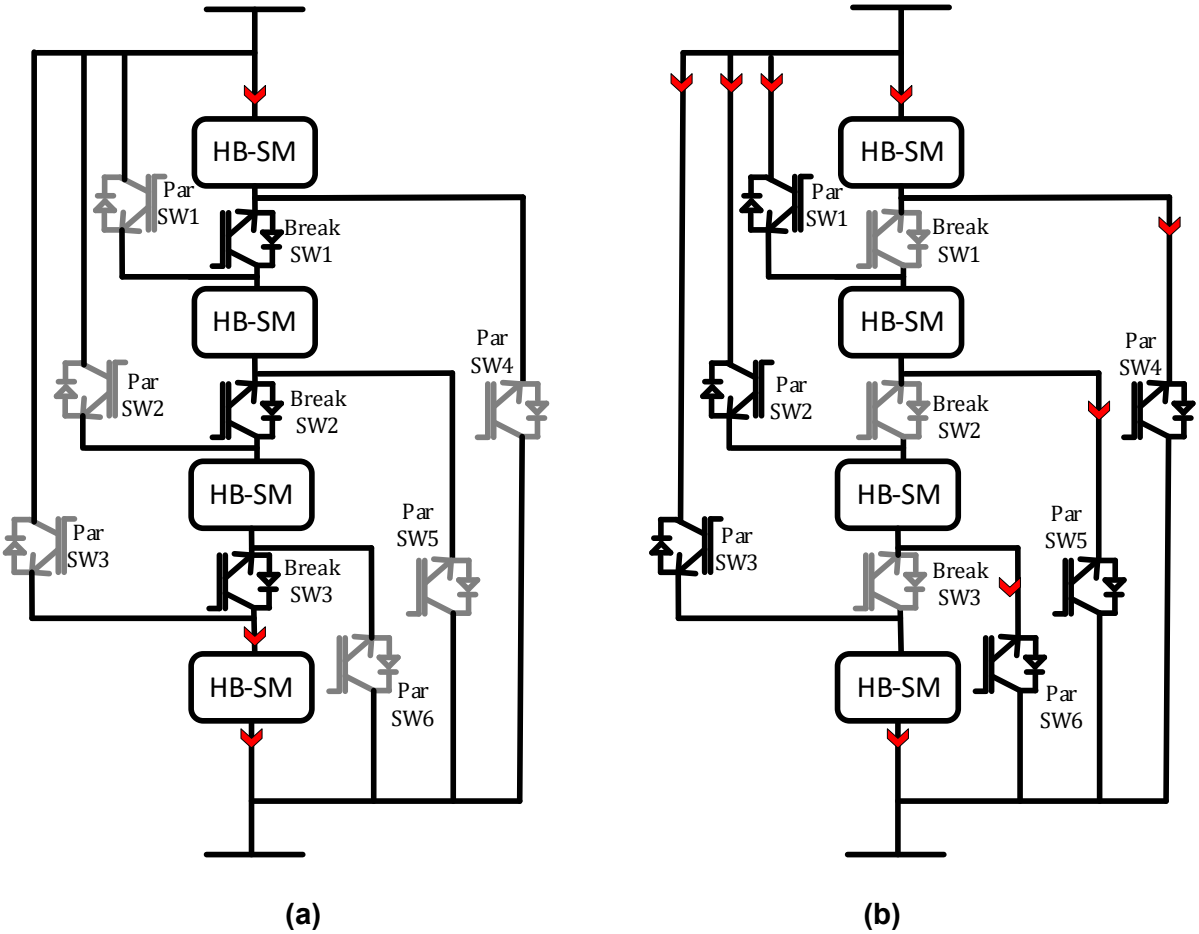


Figure 4-2: Proposed series/parallel reconfigurable circuit with HB-SMs for 4 pu current (conceptual) (a) series operation (b) parallel operation in 2 pu or 4 pu

From the discussion above, it can be gathered that the number of additional switches required for $4\,pu$ is 300% more than the $2\,pu$ circuit. In particular, the requirement of three breaker switches will significantly increase conduction losses during series operation which is the normal mode of operation. This first proposal for a series/parallel reconfiguration circuit to generate $4\,pu$ current is an unattractive option.

The primary drawback of the proposed circuit is the additional conduction loss as a result of the break switches in the current path during series mode. This prompted consideration of reconfiguration of the AAC. AAC style converters, discussed in Section 2.4.1, already require a director switch in series with stack of SMs and thus it may be possible to utilise the existing director switch as the break switch in a series/parallel reconfigurable circuit.

4.3 Series/Parallel Reconfiguration Circuit in a Delta configured STATCOM

A delta-connected chain link STATCOM [70] is a suitable target circuit for the series/parallel technique. The block diagram for the delta configured STATCOM is shown in Figure 4-3. Taking advantage of this relocated director switch, a series/parallel reconfiguration method was tested to evaluate the device count as well as their rating for a lower fault current generation (such as for $2pu$). If this method proved feasible at a lower FCC of $2pu$, then this idea could be expanded for higher FCC ($4pu$). The proposed series/parallel circuit was adopted in a STATCOM with director switches (inspired by AAC) where the director switches were to be used as part of a reconfiguration.

Only HB-SMs are needed in each arm of the AAC-like structure because each of the alternate arms needs to produce voltage of one polarity only. HB-SMs were adopted to build a 5-level AAC for each phase of the STATCOM model to assess the circuit reconfiguration. The model was developed in a MATLAB / Simulink environment. The arm of series connected HB-SMs will be rated to meet the phase stack and arm voltage requirements. The current rating of these HB-SMs will be the maximum current that will flow during the parallel configuration. Director switches are connected in series with each HB-SM. When operating as a break switch to reconfigure the HB-SMs in parallel, it will be rated to block the HB-SM voltage rating. Parallel switches will be added and rated accordingly to block the HB-SMs voltage when not in operation. The current rating of the all HB-SMs, director and parallel switches will remain at the nominal current rating of the STATCOM.

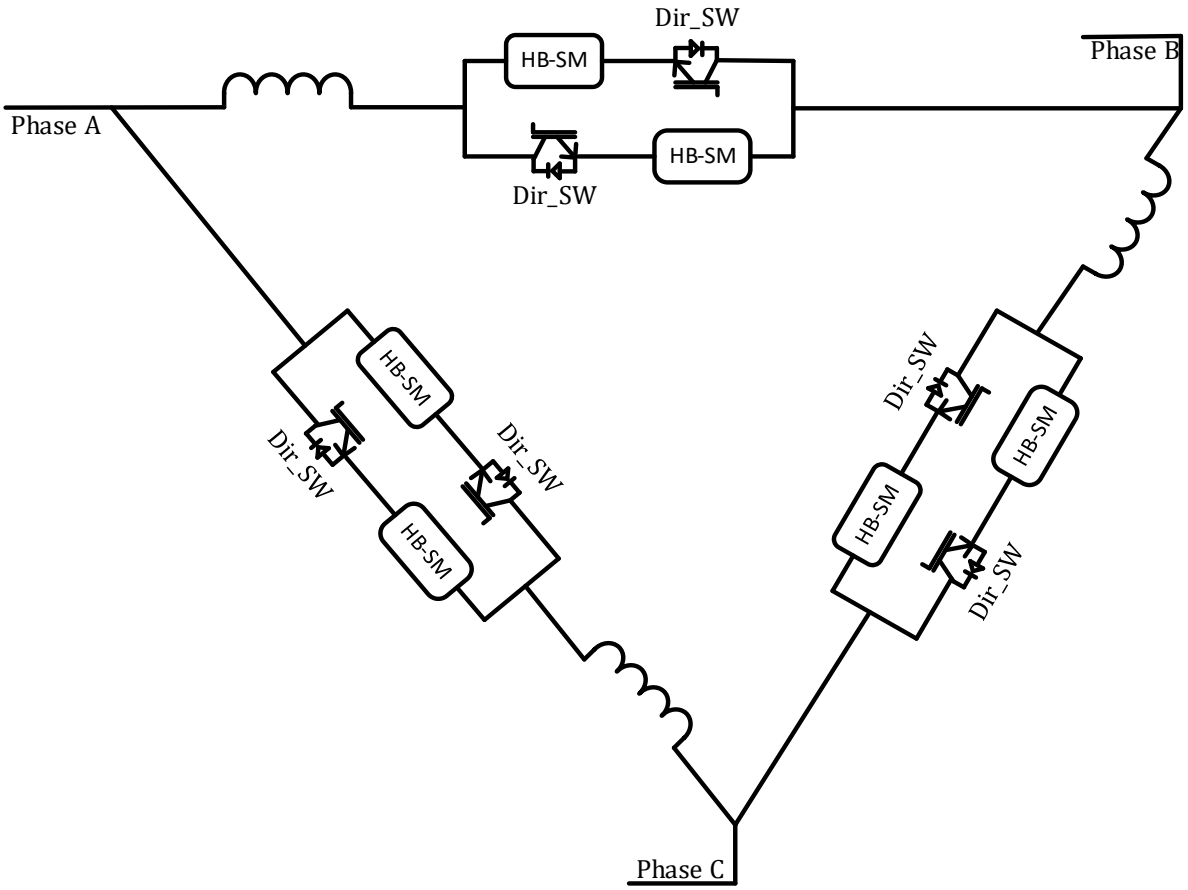


Figure 4-3: Delta Configured STATCOM with HB-SMs stack

Figure 4-4 shows the Simulink model reduced to a single phase, to assess the feasibility of circuit reconfiguration in generating a $2pu$ fault current. The positive and negative arms of the phase have similar arrangements of switches and SMs, but the negative arm (shown in blue) is rotated by $180°$ with respect to the positive arm (shown in red) to support voltage in the opposite polarity.

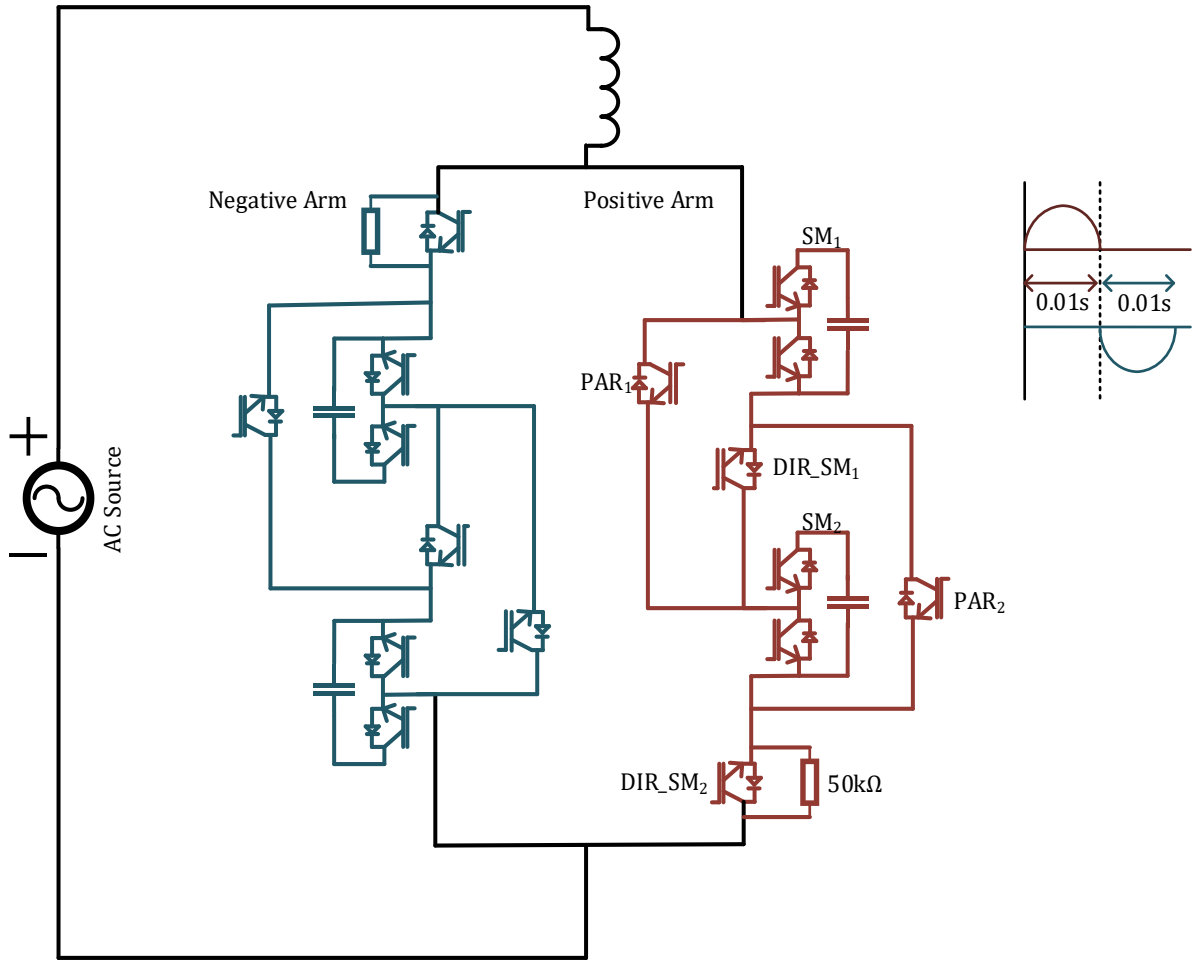


Figure 4-4: Per-phase representation of the AAC based STATCOM with 2 SM per Arm

The investigation started with the simple example of an AAC STATCOM with 2 SMs per phase, one in the positive arm and another in the negative arm. For the purpose of a simulation study, each SM was rated at base peak voltage of 2 kV and a base peak current 1 kA. Hereafter, this base SM rating is called 1 pu rating. This meant that each phase or stack was rated for a peak voltage of 4 kV. This enables an operation with a peak AC voltage of 4 kV and therefore it matched the AC grid of slightly lower peak voltage of 3.5 kV to allow some voltage drop across the coupling inductor and allow some control headroom. The additional switches across each SM are rated at 1 pu voltage and current (the same as the SM) to enable a series/parallel reconfiguration. These switches are called parallel switches.

The voltage and current rating of the director switch (DIR_SM_1) between the SMs is 1 pu. But the voltage and current rating for the second director switches (DIR_SM_2) is 2 pu. Voltage rating was 2 pu because it should be capable of blocking the negative arm voltage while acting as a director switch.

Figure 4-5 shows the simulated circuit, in which each SM has its own parallel switch and a director switch to enable a series/parallel reconfiguration.

The current reference was set to a peak of $1\ kA$ $(1\ pu)$ and through a closed loop current feedback a voltage reference was generated. The voltage reference is then converted into a PWM signal which drives the gate signals to the IGBT switches.

The model simulated the series / parallel switching of SMs in an AAC type modular converter by following the sequence below:

1. During a fault, the line voltage is reduced,
2. if it falls below $0.5\ pu$ then half of the SMs can be put in parallel, and
3. The other half can be used to double the current $(2\ pu)$ at half the voltage $(0.5\ pu)$.

It is to be noted that this switching reconfiguration cannot be used during an overload condition (cold load pick-up) because the line voltage is not reduced in those cases.

As the positive- and negative-polarity behave similarly, the assessment focusses on the positive-half only. Figure 4-5 (a) shows the series operation of the positive half of the phase. The positive half of the phase is connected in series at the start of the simulation. The parallel switches PAR_1 and PAR_2 are tuned off (no gate signal applied), and all the other switches are turned on (gate signal applied). Parallel operation is initiated at $0.25s$, and the AC source voltage is reduced to $0.5pu$, representing the line voltage drop during a fault condition. For convenience, it was assumed that the detection of drop in line voltage and the initiation of parallel reconfiguration occurred at the same time. At $0.25s, DIR_SM_1$ is turned off by removing its gate signal. At the same time, gate signals are applied to PAR_1 and PAR_2 to turn them on. This is shown in Figure 4-5 (b). As shown in Figure 4-6 (a) and (b), the phase voltage and current magnitude follow their respective references during a series or parallel operation.

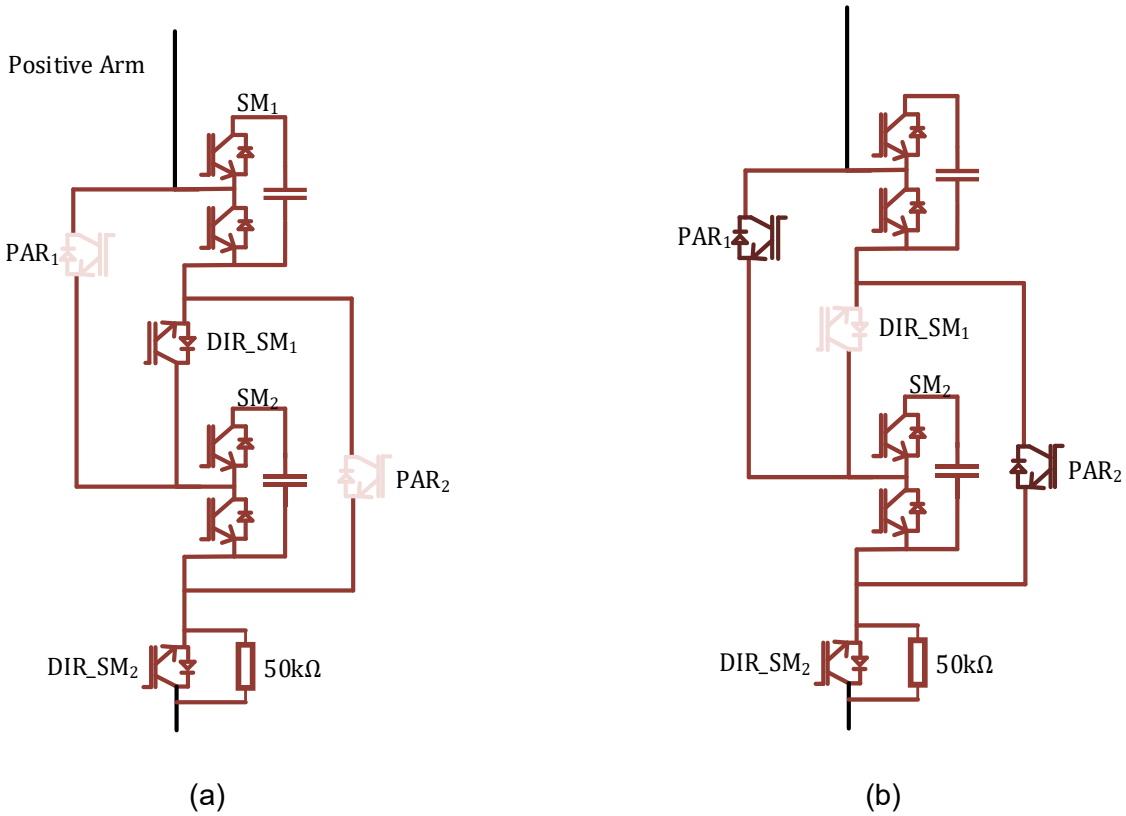
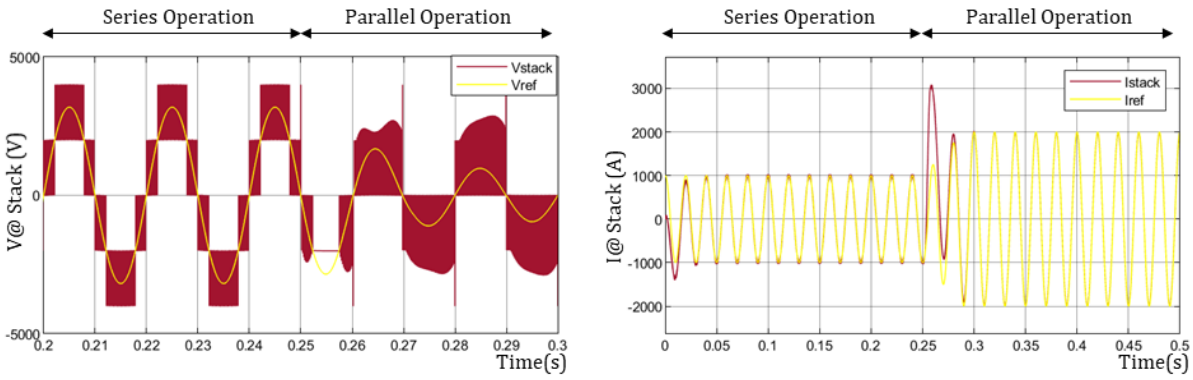


Figure 4-5: Positive half of each phase in (a) series and (b) parallel operation

As the parallel reconfiguration is completed, the phase voltage drops to $0.50pu$ (Figure 4-6 (a)) to match the line voltage drop. This means that the phase current had increased to $2pu$ (Figure 4-6 (b)). Hence, a $2:1$ circuit reconfiguration is possible to increase the FCC to $2pu$.

Figure 4-7 shows the voltage and current stress of the director switch DIR_SM_2 showing (i) the need to block a minimum of $4kV$ $(2\ pu)$ when in the negative half cycle of voltage and (ii) the need to carry $2pu$ current during parallel reconfiguration. The equivalent director switch in the negative half will have the same voltage and current rating requirement.



(a) (b)

Figure 4-6: Voltage (a) and Current (b) in Stack

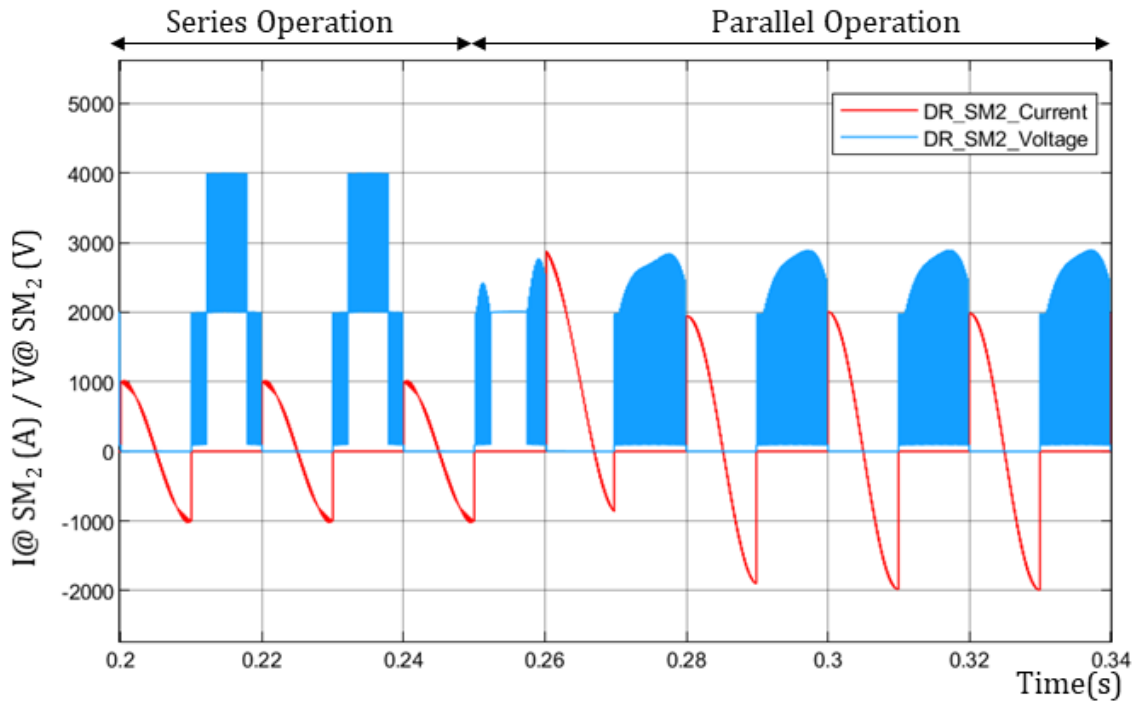


Figure 4-7: Voltage and Current in Director Switch of SM2 (DIR_SM$_2$)

4.4 Comparison of a Base Case against the series/parallel reconfiguration Method

To assess the feasibility of this series/parallel switching arrangement, it needs to be assessed against a base case to compare the total number of devices in the network and in the conduction path when the current is $1\ pu$ and $2\ pu$.

The series/parallel switched STATCOM is compared to a first base case (BC1) of an ACC-style STATCOM with non-reconfiguration circuit and to a second base case (BC2) of a single MMC STATCOM.

A similar rated 5-level delta-configured MMC type STATCOM with FB-SMs is shown in Figure 4-8. To generate an FCC of $1\ pu$, FB-SMs use four switches in each SM and can operate in both the positive- and negative-half of the waveform. If the switches rating remained identical to the proposed method, the total number of switches required to build this base case would be eight for each phase.

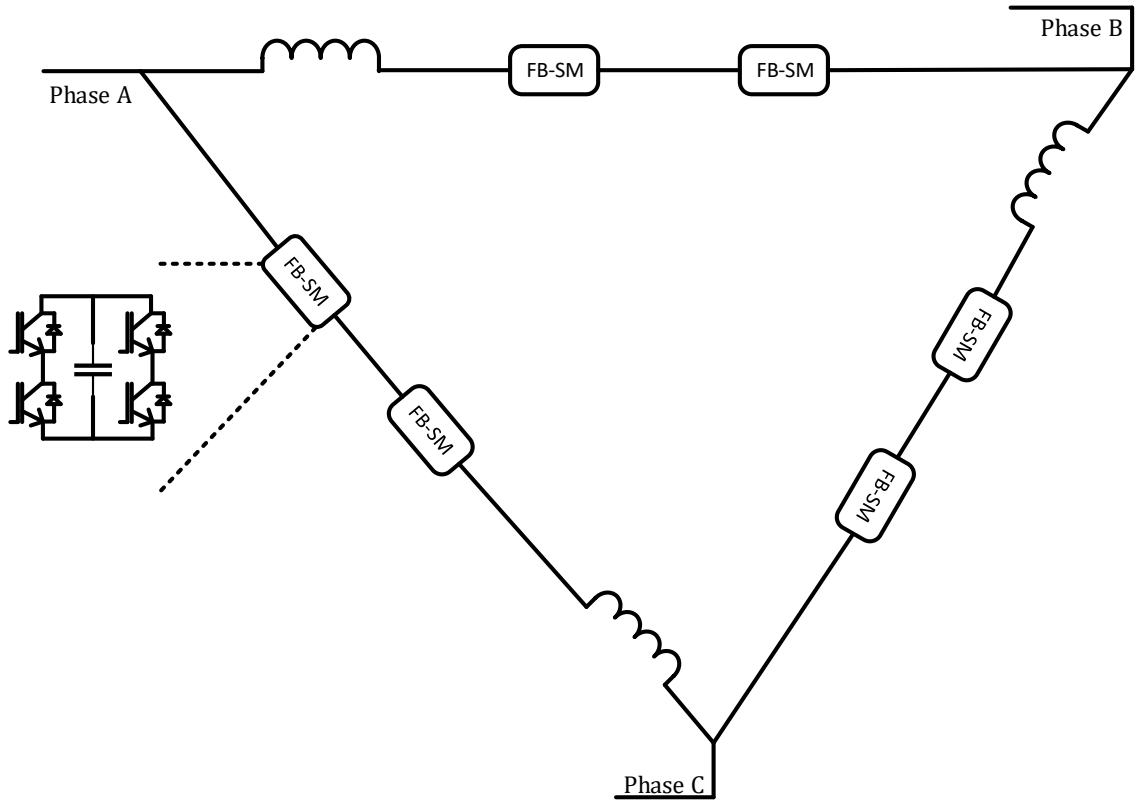


Figure 4-8: 5-Level Delta Configured MMC with FB-SMs

As shown in Table 4-1, the total number of switches required in a series/parallel method and the base case is equal. The number of switches in the conduction path of the series/parallel network is 50% more than the base case. Moreover, the two director switches per phase will need to be $2pu$ voltage and current rated.

Table 4-1: Comparison between Base Case and Proposed Method per phase

	Base Case 1 (MMC style STATCOM)	Base Case 2 (AAC style STATCOM without series/parallel)	Proposed series/parallel switching (AAC style STATCOM)
Total number of IGBT	8	12	16
Number of IGBT in Conduction Path	4	6	6 in Series[1] & 8 in Parallel[1] ([1] -DIR_SM2 will be rated for $2pu$ voltage and current)
Maximum FCC	1pu	1pu	2pu

4.5 Series/parallel reconfiguration to generate higher FCC ($4\ pu$)

The proposed STATCOM series/parallel circuit with a $2:1$ reconfiguration ratio worked well to generate a current of $2\ pu$. However, the FCC contribution from an IBR needs to be comparable to a synchronous generator. This would mean FCC contribution from IBR at least should be in the region of $5\ pu$ and $10\ pu$.

The circuit developed for $2:1$ series/parallel reconfiguration ratio can be enhanced to enable $4:1$ series/parallel reconfiguration ratio. The proposed circuit will be capable of producing current of $2\ pu$ and $4\ pu$ depending on the line voltage. For the STATCOM to generate FCC of $4\ pu$, the voltage in each phase needs to drop to $0.25\ pu$ and match the line voltage drop,

which would have reduced to lower than $0.25\ pu$ as well. A positive half of each phase capable of producing $4\ pu$ current is shown in Figure 4-9. The voltage and current rating for the SMs and switches are shown next to them in pu. Again, a $2\ kV$ and $1\ kA$, is considered for a $1\ pu$ rating for the switches and SMs. With this $1pu$ rating, the number of HB-SMs, director switches and the parallel switches will be increased by 125% compared to a circuit with $2{:}\,1$ reconfiguration capability. The three switches would have a voltage and current rating of $2\ pu$. But the director switch (DIR_SM_2) located at the end of the circuit will need to block a $4\ pu$ voltage and conduct current of a $4\ pu$ in a parallel configuration. This means that this director switch will have a voltage and current rating of $4\ pu$. The circuit in parallel reconfiguration is shown in Figure 4-10.

The director switch with a current rating for $4\ pu$ proves to be a key technical challenge. An IGBT switch with a high current rating of $4\ pu$ $(4\ kA)$ is not achievable unless current rating during normal operation is reduced. Reducing the current rating during normal operation would reduce the nominal power rating of the STATCOM.

As FCC is required only few times in a year, the additional number of switches required for a $4{:}\,1$ circuit reconfiguration makes this unattractive due to cost as they are sitting idle for most of year. If the circuit reconfiguration ratio is increased further, then the number of switches would increase accordingly but most importantly the current rating (DIR_SM_2) of the director switch will need to be increased further.

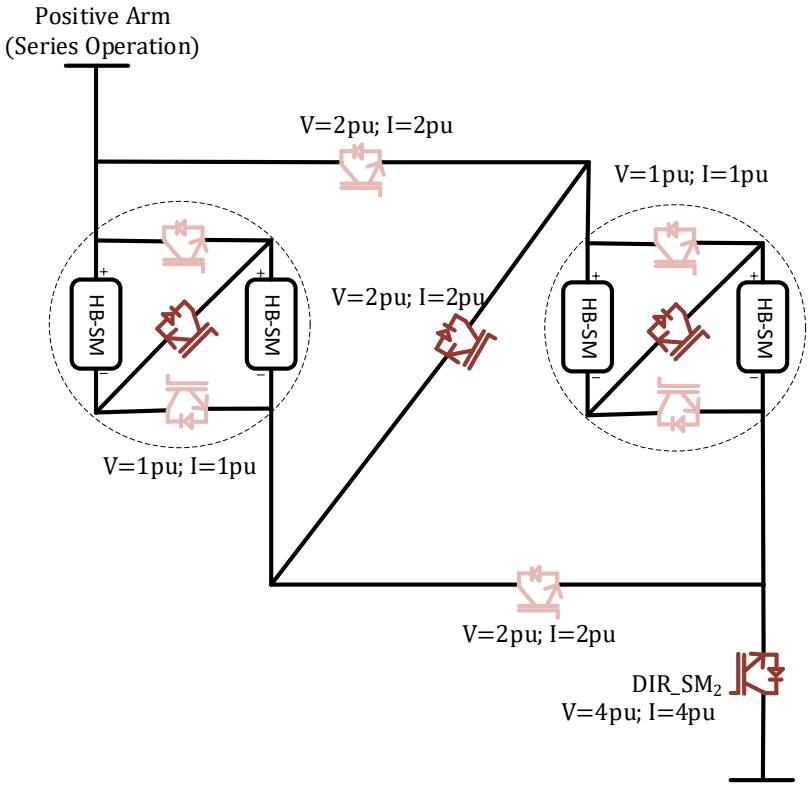


Figure 4-9: Positive half of each phase in series with 4:1 circuit reconfiguration

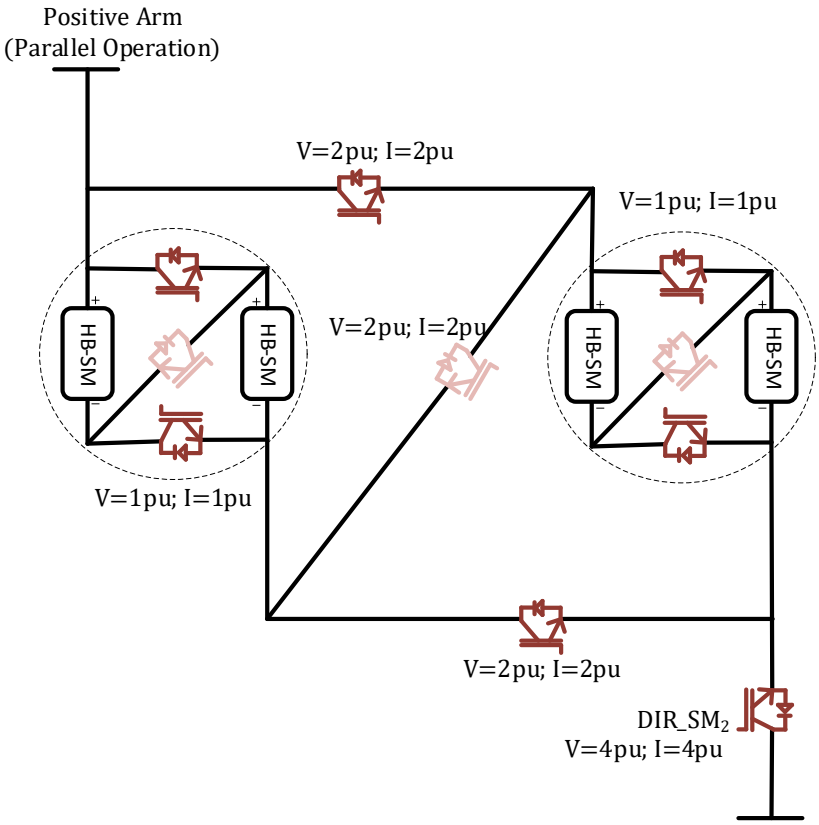


Figure 4-10: Positive half of each phase in parallel with 4:1 circuit reconfiguration

4.6 Chapter Conclusion

The study of the proposed series/parallel reconfiguration method has established that during a fault in which the line voltage is reduced below $0.5pu$, then half of the SMs can be put in parallel with the other half and therefore the FCC is doubled ($2pu$). The proposed series/parallel switching was applied to an AAC-style STATCOM. In series operation, the proposed series/parallel circuit compared to base case 1 (AAC style STATCOM without series/parallel circuit) had an equal number of devices in the conduction path but when compared to base case 2 (MMC STATCOM) the number is 50%. However, the series/parallel reconfiguration circuit had the capability to provide FCC of up to $2\ pu$ compared to $1\ pu$ FCC from base case 1 and 2.

It was also noted that this switching reconfiguration cannot be used to provide additional current during an overload event (such as cold load pick-up) because the line voltage is not reduced in those cases.

A circuit with a $4{:}1$ series/parallel reconfiguration would have its number of switches increased by 125% compared to a circuit with $2{:}1$ circuit. Moreover, two of the director switches in each phase would need current ratings of $4pu$ which may require parallel IGBTs and added complexity. As the circuit reconfiguration ratio increases ($4\ pu\ or\ higher$), the total number of switches and the current rating of two director switches in each phase increases. As the FCC required from IBR are limited to a few times in a year, this increase in number of switches, some of which are in the normal current path, add to power losses. Thus, alternative solutions needed to be investigated in other parts of the circuits such as IBR's OLTC-enabled coupling transformer to increase FCC.

CHAPTER 5 FAST TAP-CHANGING FOR FAULT CURRENT ENHANCEMENT

5.1 Introduction

A decrease in the SCL in a network can adversely impact the accuracy of protection systems to detect and isolate faults [102]. System operators such as NGESO have begun procuring additional fault infeed from non-generation assets such as synchronous condensers. Synchronous condensers have high standing power losses, and it would be beneficial to instead use a power electronic device such as a STATCOM, but a STATCOM, as a type of inverter, has a strictly limited fault current.

In CHAPTER 3, it was shown that the limitation in the rating of the semiconductor devices meant that even after improving the thermal management, it was not possible to increase the fault current of an inverter sufficiently for protection purposes. In CHAPTER 4, a series/parallel reconfigurable circuit in a STATCOM was proposed to increase the fault current available when the voltage at the connection point is reduced by a fault. However, the large increase in the number of semiconductor switches needed for the circuit reconfiguration meant that the proposal was not attractive.

The study in this section is the third approach to increase fault current. Like the study in CHAPTER 4, it uses the philosophy of circuit reconfiguration but here the reconfiguration is applied to the windings of the coupling transformer of a STATCOM. In STATCOMs, and several other types of IBRs also, coupling transformers are typically used to connect to the grid and perform any step-up of voltage needed and provide galvanic isolation. Switching transformer windings does a very effective job of trading voltage for current. A $4{:}\,1$ change in turns ratio causes a 4:1 change in voltage that is complemented by a $1{:}\,4$ change in current. This would work very well if a series/parallel switching of windings is used, but this means that switches in the circuit would have to be of high rating for reconfiguration duty. Instead, this study takes advantage of the commonly used principle of tap-changing to reduce the number of turns of HV winding. Normally tap-changing makes small adjustments to the turns-ratio (k_T) to trim the voltage by a few percent but in this proposal, large sections of the winding will be switched in and out to affect a large turns ratio change.

This chapter proposes a novel scheme using a STATCOM which has an eTC added to its coupling transformer. The proposed scheme adjusts the transformer voltage turns ratio during a fault while the voltage is depressed. The decrease in voltage ratio is accompanied by an increase in current ratio that delivers enhanced FCC. Changing the k_T of the transformer is effectively trading the voltage capability of the STATCOM for current and allows the combination to provide enhanced fault current without raising the current rating of the STATCOM.

An eTC using thyristors and IGBTs has been proposed in the literature for improved voltage regulation for transformers [93] where a tap range of up to $\pm 20\%$ is normal. The proposed scheme in this chapter, builds on the approach used in [82] to create a tap-changer with a large change in k_T in the STATCOM coupling transformer windings. Through tap-switches in the coupling transformer, the k_T can be switched between 1:4, 1:2 and 1:1 which can be used to increase the FCC at the PCC up to $4\ pu$, while the converter in the STATCOM continues to operate at $1\ pu$ current. The HV winding will carry a higher current than normal during the fault, but this will be accommodated in the "overload" rating of the winding because transformers can experience up to $10\ pu$ of their nominal current rating during faults and their design takes this into consideration.

The sections below are arranged as follows. The system design and application of the eTC is described in Section 5.2. The comprehensive analysis of the proposed circuit with a single line to ground fault (SLG) is described in Section 5.3. The conditions for simulations and the simulation results are considered in Section 5.4 before concluding in Section 5.5.

5.2 System Design — Application of Tap Changer Circuit

In many IBR systems, a coupling transformer will be present to connect to a grid to provide both galvanic isolation and a step up from the inverter voltage to the grid voltage. Because the transformer is dedicated to the IBR, it can be designed with tapped windings with large ratio changes to suit the proposed fault current enhancement scheme.

Generally, the tap-changing process of a mechanical tap-changer is slow and can be as long as $3\ s$ to $5\ s$ where springs have to be mechanically charged [85]. Even relatively fast vacuum tap-changers are still too slow to be a viable option for responding to a need for fault current injection [84]. As discussed in Section 2.1, protection system needs the IBR to provide fault current almost immediately after the fault on the system. Power electronic switches will allow

the tap changer to operate sufficiently quickly to deliver fault current in a cycle or less of the grid voltage. Thyristors have been chosen for the tap change switches due to their low conduction losses when compared to an IGBT which will be important during normal use of the STATCOM. In addition, the high surge current capability of thyristors allows their use in the grid connection carrying the increased current, whereas IGBTs can be used in the STATCOM converter itself which continues to operate at $1\ pu$ current. Fast commutation of the outgoing tap-selector thyristors is required rather than waiting for the natural zero-crossing of the current. To achieve this, the STACOM will actively control the current to force thyristor currents to be zero when they need to be turned off.

5.2.1 Operational Principles of the Proposed Thyristor based Electronic Tap Changer Circuit

The circuit configuration for the proposed STATCOM with eTC is shown in Figure 5-1. A STATCOM based on the SSBC circuit is connected to a star-star configured step-up coupling transformer. The SSBC circuit was chosen for the STATCOM, which allowed independence of operation of each phase during asymmetric faults. In normal use, the transformer is a 1:4 step-up transformer. The eTC is connected on the grid side of the transformer.

The three phases of the transformer will have eTC that are designed to work independently and so in the event of an unbalanced fault only the faulted phases will be tapped and produce enhanced fault current. To accommodate this, current control of the STACOM converter will also be independent of its three phases.

The STATCOM will be assessed in a case where it is at one end of transmission line with grid source at the other end as shown in Figure 5-1. Bus C (B_C) is the point at which the converter voltage (V_C) and current (I_C) output is measured. The STATCOM reactor with impedance (Z_C) is located between the converter station and the secondary winding of the transformer. Bus STATCOM $(B_{STATCOM})$ is the point at which the STATCOM voltage $(V_{STATCOM})$ and current $(I_{STATCOM})$ output is measured. The neutral of the star (Y) configured STATCOM-side winding of the transformer and STATCOM are connected, before solidly connecting it to the ground. The grid-side of the transformer is solidly grounded. Bus PCC (B_{PCC}) is the point of common coupling (PCC), where the equipment being studied will be placed. The voltage (V_{PCC}) and current (I_{PCC}) measured at B_{PCC} are used by the STATCOM current

controller. The STATCOM coupling transformer is connected at one end of a long transmission line with impedance (Z_L) and grid source (V_G) at the other end.

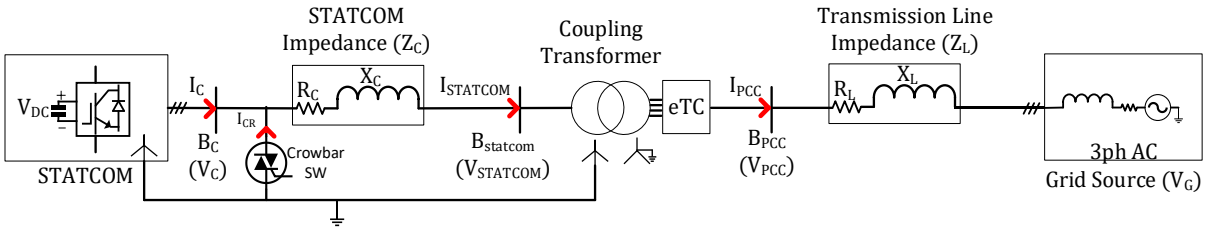


Figure 5-1: The STATCOM, tap-changer in the coupling transformer, transmission line and grid source arrangement

In order to understand the operational principles of the proposed thyristor based eTC, the focus will be on the step-up coupling transformer and its tap-changer circuit. Figure 5-2 shows the single-phase version of the proposed network concentrating on the tap-changer circuit of the transformer.

The grid-side (high voltage) winding (W2) is divided into four equal sections (W2a to W2d) with switches S2a, S2b and S2d (comprising anti-parallel thyristors) able to select turns-ratio of 1:4, 1:2 and 1:1 as shown in Figure 5-2. The impedances $Z_{W2a}, Z_{W2b}, Z_{W2c}$ and Z_{W2d} represent the winding leakage reactance and winding resistance of each section.

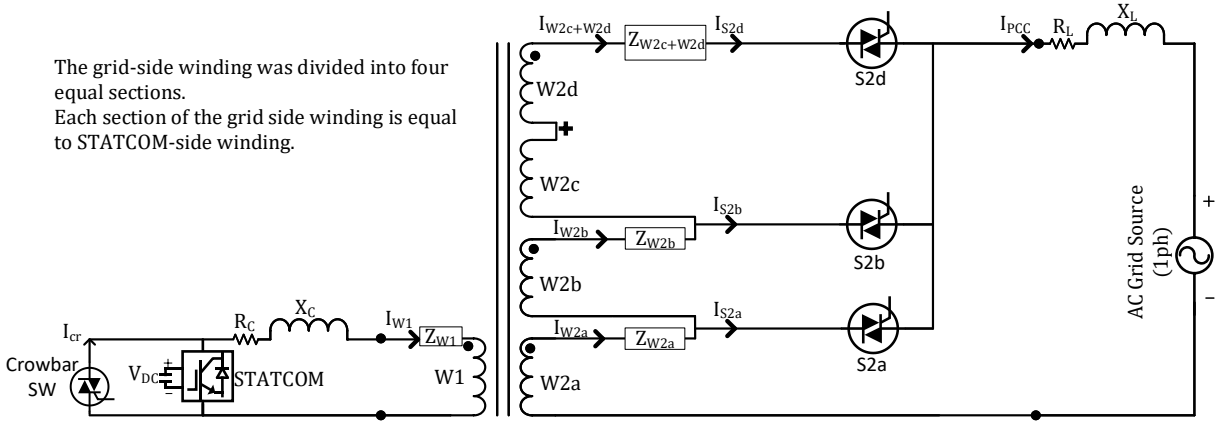


Figure 5-2: Proposed circuit with tap switch arrangement (showing single phase)

The depth of voltage dip appearing at the PCC resulting from a fault determines how far voltage can be traded for current using the eTC. When the retained voltage at PCC is between 0.5 pu

and $0.25\ pu$ the transformer will operate with a k_T of $1:2$ (with tap-switch S2b switched on) sufficient for the STATCOM to match the voltage and be able to deliver $2\ pu$ fault current into the PCC. When the voltage at the PCC drops below $0.25\ pu$, tap-switch S2a is used to create a 1:1 ratio and the fault current can be increased to $4\ pu$. In all cases, the current in the converter-side of the transformer (W1) remains $1\ pu$. Additional switches could be added to provide further changes in k_T allowing finer choices of fault current and higher fault current at the cost of more thyristors and a more complex transformer. Windings W2a and W2b are required to withstand the elevated fault-current, of $4\ pu$ and $2\ pu$ respectively, during the fault. Typical surge current ratings of high voltage transformer windings [103] and high current rated thyristors [104] are in the region of $10\ pu$ and therefore additional over-rating is not expected to be required. Those windings will be required to carry the fault current for the fault-clearance time (typically 80 ms), but this is a normal requirement of a transformer.

5.2.2 Impact of Retained Voltage on Tap-Change Circuit Arrangement

It is important to note that the depth of voltage dip or retained voltage appearing at the PCC resulting from a fault determines how far voltage can be traded for current using the eTC. During a close three phase to ground (3LG), single phase to ground (SLG) and phase to phase to ground (2LG) faults, the voltage at PCC could fall well below $0.25\ pu$. If the retained voltage is below $0.25\ pu$, then the eTC arrangement shown in Figure 5-2 allows the change of turns ratio to $1:1$ and inject fault current up to $4\ pu$. If the fault is further away from PCC and/or has a high fault resistance, the voltage at PCC may not drop below $0.25\ pu$ and only $2\ pu$ fault current may be possible.

A close-up line to line (L-L) fault does not give a large voltage magnitude reduction at PCC and will only go down to $0.577\ pu$ in the two faulted phases [13]. Again, if the fault location is further away from PCC and/or has high fault resistance, then the retained voltage would be above $0.577\ pu$. With this eTC arrangement in the windings, a change of split with different winding turns ratio would be required to support to 60% voltage reduction rather than 50%. Another way would be to over-rate the STATCOM voltage rating to support tap-change at 60% of the line voltage.

Additional switches could be added to provide further changes in k_T allowing fine choices of fault current and higher fault current at the cost of more thyristors and a more complex transformer.

5.2.3 Operation in Normal Grid Conditions

During normal operation, the eTC operates with a turns-ratio of 1:4, with S2d in conduction and all four sections of the grid-side windings connected in series, as shown in Figure 5-3. S2b and S2a are switched off. In this mode of operation, the eTC acts no differently to a standard 1: 4 transformer turns ratio, although with increased conduction loss from S2d, and both STATCOM current and the PCC current are at 1 pu. The S2d connects the HV winding to the grid. The figure also shows the gate signals (GS) at 1 or 0, for the tap switches to indicate if they are turned on or off respectively.

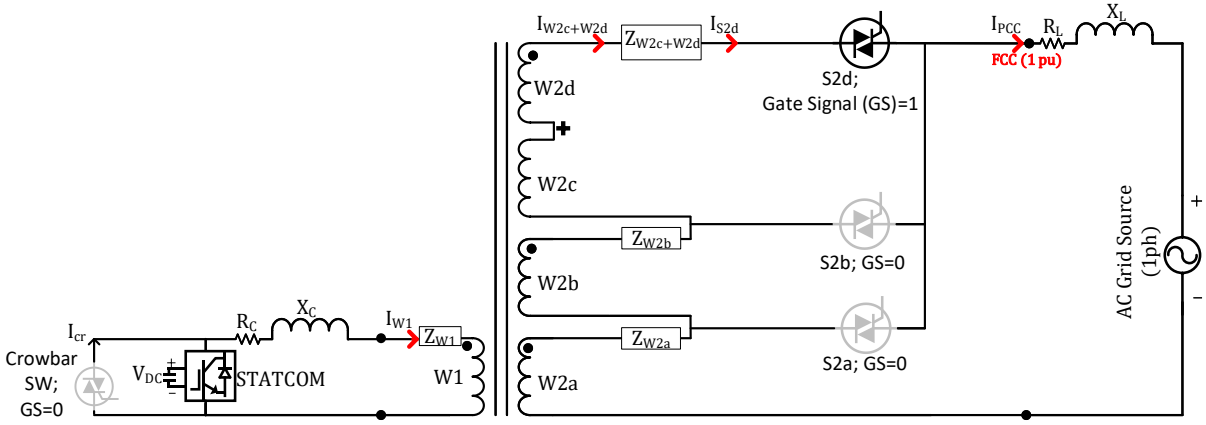


Figure 5-3: Proposed circuit with tap changer and k_T of 4:1 (showing single phase)

5.2.4 Tap-down Sequence to Increase Fault Current

The opportunity for a fault current injection is created during a reduced grid voltage (fault condition), where not all the HV windings (grid side) of the coupling transformer are required to operate at that reduced voltage. If the PCC voltage drops below 0.5 pu the k_T is to be reduced from 1:4 to 1:2. This requires S2d to be switched off and S2b to be switched on. A key point here is that S2d can be force commutated by the STATCOM converter because it is able to very rapidly drive the current below the holding current (I_H) of the thyristor. This is followed by a brief period, known as turn-off duration (T_q), of holding the current close to zero to allow for complete turn-off of S2d before S2b is switched on and current supply by the STACOM converter resumes. W2c and W2d are now switched out of the circuit, thereby reducing the number of turns in the conduction path by 50% giving a turns ratio of 1:2 with voltage magnitude on the grid side (relative to converter side) having reduced by half but the current on the grid-side having doubled. Thus, when the STATCOM current is ramped back to 1 pu,

the current produced at the PCC rises to 2 pu. In this way, the FCC of the STATCOM can be increased without exceeding the nominal rating of the IGBTs within the converter as shown in Figure 5-4.

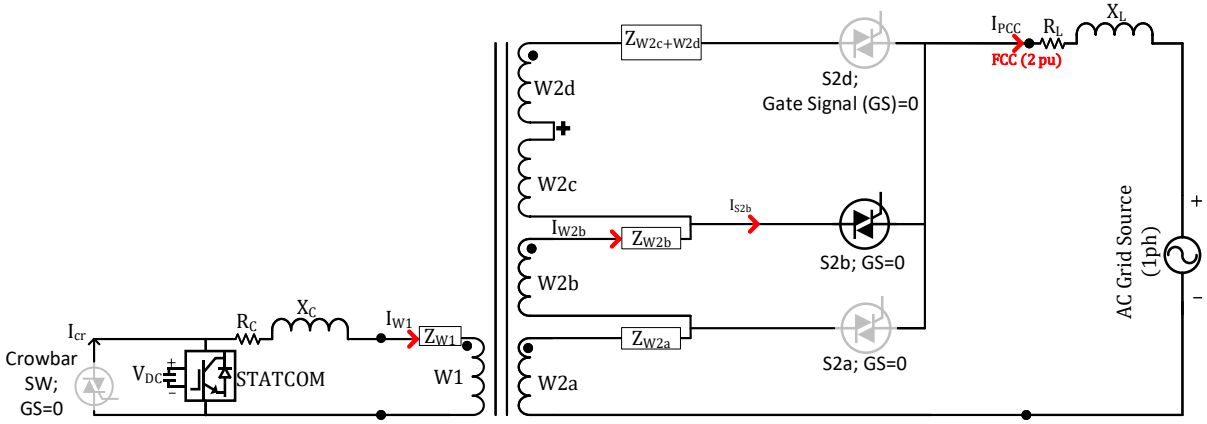


Figure 5-4: Proposed circuit with tap changer and k_T of 2:1 (showing single phase)

If the fault causes a grid voltage reduction to less than 0.25 pu, the forced commutation process can be repeated to turn-off S2b and S2d, and turn-on S2a such that only W2a is in circuit, the k_T is then 1:1 and an FCC of 4 pu can be provided as shown in Figure 5-5.

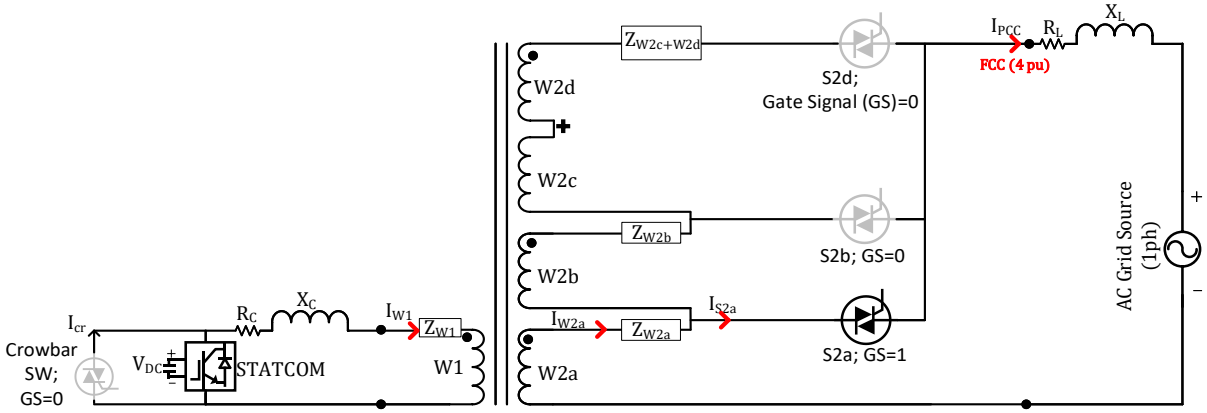


Figure 5-5: Proposed circuit with tap changer and k_T of 1:1 (showing single phase)

5.2.5 Tap-up Sequence to Restore Normal Operation

Following the clearance of the fault, the grid voltage will rise, and the k_T will need to be returned to 1: 4 by switching off S2a or S2b (as appropriate) and switching on S2d. This follows a similar forced commutation process to that described above for tap-down with the STATCOM converter being controlled to set thyristor currents to zero and hold zero while

turn-off is accomplished. The key here is to rapidly detect the rise in PCC voltage such that the tap-up sequence is completed before the grid-side voltage fully recovers. If this is not achieved, then the converter-side voltage (produced by the grid voltage and the transformer in a low turns ratio state) exceeds the capability of the converter and control over the current is lost. Without current control, forced commutation of the tap-switches is not possible and excessive current flows through the STATCOM until the next zero-crossing, likely damaging the IGBTs within. However, typical voltage recovery is relatively slow, allowing for the successful completion of the tap-up sequence. Voltage recovery is dependent on several factors including network impedance, load and generator characteristics and fault type. Nevertheless, an internal protection scheme is needed in the event of fast recovery of the PCC voltage, as described in the next section.

5.2.6 Protection of STATCOM against Tap-up sequence failure

In the event of fast-voltage recovery causing a loss of ability to force commutate the thyristors, the IGBTs within the STATCOM need to be protected from over-current. The proposed protection scheme is a crow-bar circuit to divert current away from STATCOM devices. The crow-bar consists of an anti-parallel pair of bypassing thyristors in parallel with the converter as shown in Figure 5-6.

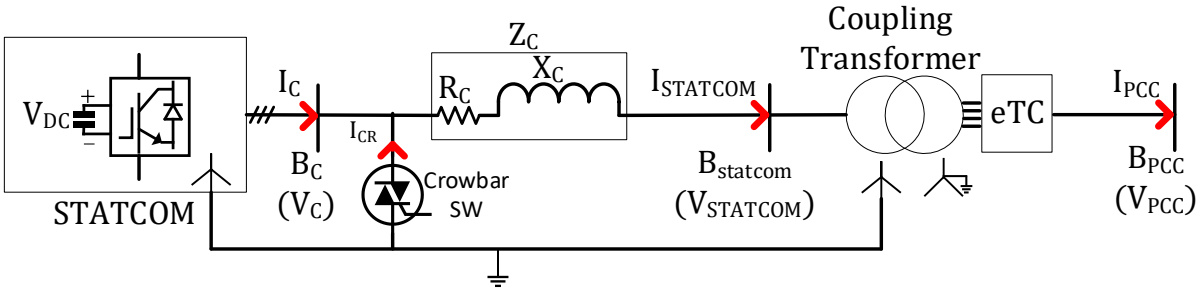


Figure 5-6: Crow-bar circuit in operation protecting the STATCOM

In the event of step-up sequence failure and the detection of an over-current in the STATCOM converter, the bypass thyristor is switched on providing a low impedance path for the grid current thereby redirecting the current away from the STATCOM. The crowbar thyristors conduct the large surge current until the next zero crossing, when the tap-switches can be naturally commutated, and the tap-up sequence can be completed. The magnitude of the over-current that the crowbar must carry depends on several factors: the combined impedance of the STACOM reactor, transformer, and grid; the rate-of-rise of PCC voltage and the point-on-wave

of the fault clearance. The crow-bar thyristors, tap-selector thyristors and transformer windings will have to be rated to sustain the surge current for approximately half a cycle.

5.3 Analysis of the Proposed System

The proposal to increase the fault current from a STATCOM using a tap-change transformer was evaluated for asymmetric faults (i.e., unbalanced voltage dips). The most common fault type in the electrical distribution network is the SLG fault, accounting for 50 - 80% of faults on the network [105] and this is the focus of this sub-section. The performance of the proposed STATCOM with eTC was analysed for a variety of scenarios such as different values of fault resistance, system fault level and fault location.

The current seen in the faulted phase during a SLG fault would also be seen in three phases during a three line to ground fault (3LG) and if operation is satisfactory for a SLG fault then it will be for 3LG also. As noted earlier, the eTC and current control of the three-phases will be designed to be independent of each other. The other fault type considered for analysis is a line to line (L-L) fault.

The desired outcome of the proposed system is that the STATCOM with eTC produces fault currents similar to those of a conventional generator or synchronous condenser (SynCond), since this ensures effective operation of conventional protection systems in the network [106]. Further analysis was completed to gain understanding of how the current supplied by an SynCond and a STATCOM compare for an SLG fault. The comparison will be made in terms of sequence sets of the current at PCC by considering that the SynCond would be treated as a standard synchronous machine whereas the STATCOM would appear as a current source and an unbalanced one during faults.

5.3.1 Proposed network for STATCOM with Electronic Tap Changer

The proposed network shown in Figure 5-1 (Section 5.2.1) was adopted for the analysis. The operation of the proposed STATCOM with eTC was analysed using a 132 kV case study network shown in Figure 5-7. The analytical study was completed using code written in MATLAB.

The system consists of a 60 MVA rated STATCOM with a 33 $kV/132\ kV$ step-up coupling transformer with a thyristor based eTC. The STATCOM fault level ($STATCOM_{FL}$) would be 240 MVA when producing 4 pu of fault current. The STATCOM is at the end of 50 km long

transmission line with an internal generator voltage (V_G) at grid source of $132\,kV$. The impedances included in the network are the STATCOM reactor (Z_C), coupling transformer (Z_T), transmission line (Z_L) and the grid impedance (Z_G). It should be noted that the short-circuit level or fault level (G_{FL}) of the grid will be determined by the grid impedance.

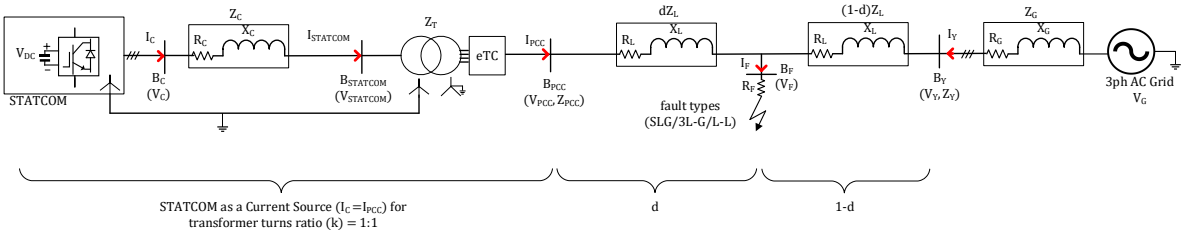


Figure 5-7: The STATCOM, tap-changer in the coupling transformer, transmission line and grid source arrangement

The STATCOM reactor impedance (Z_C) of $0.1\,pu$ are considered as per industry practice. The complete calculation for STATCOM inductor is shown in Appendix A.

The short transmission line impedances (Z_L) are taken from [13]. For simplicity, the maximum fault resistance (R_F) for SLG for a short transmission line of $50\,km$ is considered to be $0.03\,pu$ ($10\,\Omega$).

Impedance values for the coupling transformer (Z_T) were taken from a two-winding transformer of similar power and voltage rating obtained from UK Power Networks (UKPN) from one of its recent installations. UKPN is the Distribution Network Operator (DNO) for London and Southeast England. This information has been received via private correspondence. The transformer winding impedances calculations are detailed in Appendix B. The voltage and current ratings of the thyristors used as switching devices in the eTC are detailed in Appendix C. The parameters of the proposed STATCOM with eTC network are summarised in Table 5-1.

The SLG fault with fault resistance (R_F) was applied at a distance "d" per unit from the terminal B_{PCC} and is swept along the full length of the transmission line. The measured voltage (V_{PCC}), current (I_{PCC}) and impedance (Z_{PCC}) will be analysed from B_{PCC} for the STATCOM. The measured voltage (V_Y), current (I_Y) and impedance (Z_Y) will be analysed from terminal B_Y and the SLG fault would be at a distance (1-d) from B_Y. It should be noted that the grid current (I_G) and the measured current at B_Y are equal ($I_G = I_Y$).

Table 5-1: Network Parameters

Parameters	Values
STATCOM impedance (Z_C)	$0.1\ pu$
Coupling Transformer (Z_T)	$0.13\ pu$
Line impedance (Z_L) per 25 km	$0.035\ pu$
Fault resistance (R_F)	$1\ m\Omega, 100\ m\Omega, 1\ \Omega, 10\ \Omega$
Grid 3ph SC or fault level(G_{FL})	$250\ MVA, 500\ MVA, 1000\ MVA, 3000\ MVA$
Grid X/R ratio	7

5.3.2 Single Line to Ground Fault

The fault response of IBR is related to the converter capacity or rating, its control system and the control strategies in place to interface with the grid. Typically, IBR control strategy supports balanced fault current for unbalanced faults, with the current limited during faults to protect the converter's components, and not provide zero- and negative-sequence currents [16].

Due to the current control properties of typical STATCOM systems, the STATCOM can be modelled as an unbalanced current source which can inject positive, negative and zero sequence current regardless of network conditions. The impedance in series with the current source plays no role in the calculation of the fault current and hence the varying transformer impedance as a result of the eTC does not need to be taken into consideration.

Figure 5-8 shows the complete sequence network connection for a SLG fault for the proposed network for STATCOM with eTC. The positive, negative and zero-sequence are connected in series for a SLG fault such that the positive-sequence fault current (I_F^1), negative-sequence current (I_F^2) and zero-sequence current (I_F^0) are all equal. The direction of the current in each sequence network is defined to be out from the fault terminal (V_F) to flow via the fault impedance and the other sequence networks to return to the neutral terminal (N_F).

The fault point (F) is between the two sources (the STATCOM and the grid) and so the fault current in each sequence network is divided between the two branches according to the impedance and the voltage sources (if present) and then recombine to enter the next sequence network. The voltage at the fault location is given by $3\ R_F\ I_F^1$ and the contribution from each sequence network can be found by standard circuit theory and is detailed below.

Notations in the figure are defined as follows (superscript $1, 2, 0$ denotes the positive-, negative- and zero-sequence component respectively; subscripts denote a particular location or equipment in the proposed network):

V_G^1, V_G^2, V_G^0	The sequence components of fault voltage for grid source (kV)
I_G^1, I_G^2, I_G^0 I_Y^1, I_Y^2, I_Y^0	The sequence components of fault current for grid source (kA)
I_C^1, I_C^2, I_C^0	The sequence components of fault current for the STATCOM (kA)
V_F^1, V_F^2, V_F^0	The sequence components of fault voltage at fault point (kV)
Z_L^1, Z_L^2, Z_L^0	The sequence components of line impedance (Ω)
Z_G^1, Z_G^2, Z_G^0	The sequence components of impedance at grid source (Ω)
Z_C^1, Z_C^2, Z_C^0	The sequence components of impedance of STATCOM reactor (Ω)

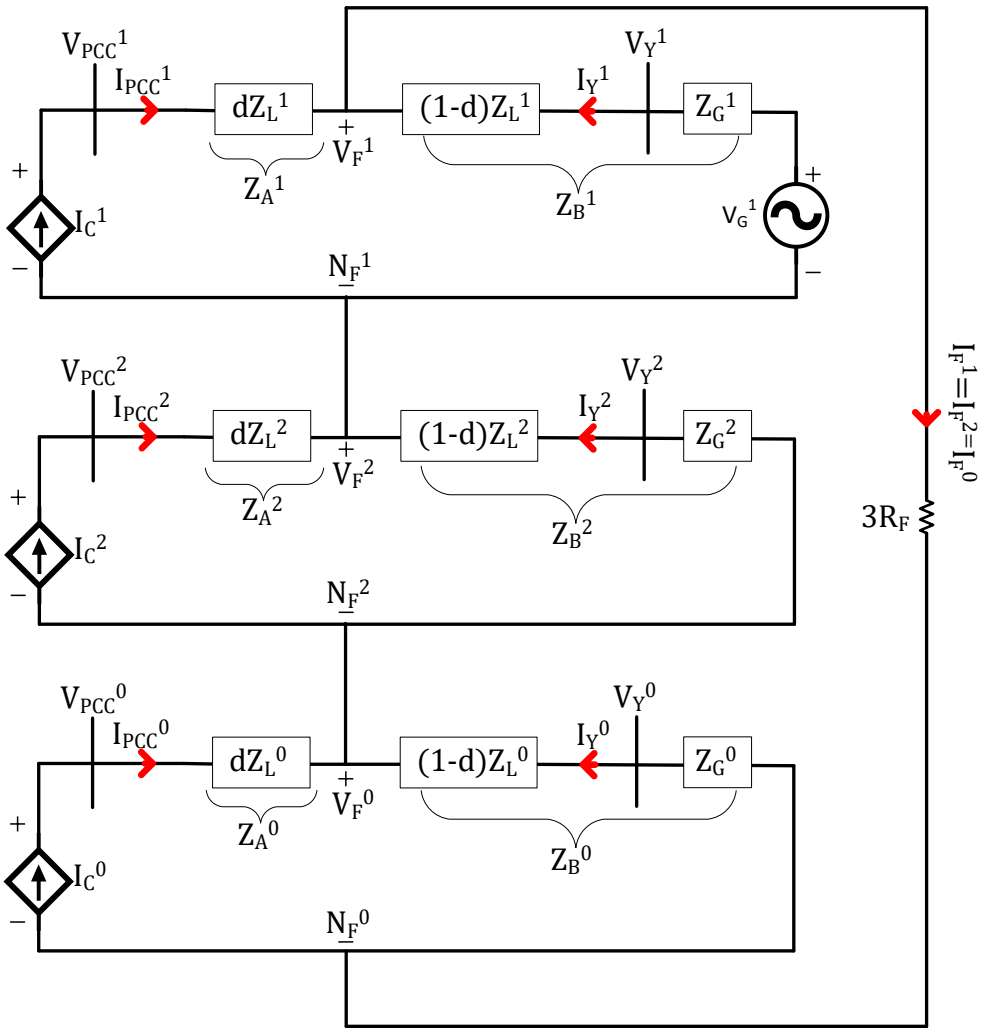


Figure 5-8: Sequence network connection for a SLG fault @ B_{PCC} for STATCOM with an eTC network

As seen in Figure 5-5, for SLG the coupling transformer k_T in the faulted phase (Phase A) is 1: 1, then I_C would be equal to I_{PCC}. In the other two phases, k_T remains 1: 4. The faulted phase would see the current rising to 4 pu and the two phases the current would remain at 1 pu. The STATCOM would be supplying a capacitive reactive current and would lead the voltage source by 90° or ($\varphi = -\frac{\pi}{2}$).

The STATCOM current in the three phases is shown in the following equations:

$$I_{PCC}^{A} = 4\, I_{\text{base}} \angle\varphi \qquad \textbf{(5.1)}$$

$$I_{PCC}^{B} = I_{\text{base}} \angle\left(\varphi - \frac{2\pi}{3}\right) \qquad \textbf{(5.2)}$$

$$I_{PCC}^{C} = I_{\text{base}} \angle \left(\varphi + \frac{2\pi}{3}\right) \quad \textbf{(5.3)}$$

The 120° angle rotation can be defined by using the STATCOM currents in three phases, the sequence components can be derived by using the standard method and are shown in equations (5.4), (5.5) and (5.6).

$$I_{PCC}^{1} = \frac{1}{3}\left(I_{PCC}^{A} + a\, I_{PCC}^{B} + a^2 I_{PCC}^{C}\right) \quad \textbf{(5.4)}$$

$$I_{PCC}^{2} = \frac{1}{3}\left(I_{PCC}^{A} + a^2\, I_{PCC}^{B} + a\, I_{PCC}^{C}\right) \quad \textbf{(5.5)}$$

$$I_{PCC}^{0} = \frac{1}{3}\left(I_{PCC}^{A} + I_{PCC}^{B} + I_{PCC}^{C}\right) \quad \textbf{(5.6)}$$

Where $a = e^{\frac{2\pi i}{3}}$.

Similarly, using the phase grid voltage in three phases, the sequence component can be derived as V_G^1, V_G^2 and V_G^0.

As shown in Figure 5-8, the impedance $Z_A = d\, Z_L$ and $Z_B = (1-d)\, Z_L + Z_G$ represents impedance of transmission line at a distance d as seen from B_{PCC} and B_Y respectively.

The zero-sequence currents are present in all phases of a transposed line, and it incorporates the self and mutual impedances. This suggests that zero-sequence impedance of transmission line is greater than the positive- and negative-sequence impedances [$(Z_A^0 > Z_A^1, Z_A^2)$ or $(Z_B^0 > Z_B^1, Z_B^2)$] [107]. However, in this analysis the length of transmission line is only $50\ km$ and the impact of mutual impedances will be limited. Hence, for convenience, the three sequence components of Z_A ($Z_A^1 = Z_A^2 = Z_A^0$) and Z_B ($Z_B^1 = Z_B^2 = Z_B^0$) terms are equal.

From Figure 5-8, and by using Kirchhoff's circuit laws, the voltage drop at point of fault in the positive, negative and zero sequence network can be given by (5.7), (5.8) and (5.9). The sum of the three-sequence set fault voltages is equal to the positive sequence fault current flowing through the fault resistance (5.10). In SLG, all three-sequence components' currents are equal and is expressed by (5.11). The relationship between the STATCOM current and fault current and grid current in positive sequence network is expressed by (5.12). This relationship remains true for all three sequence networks. It is noted that all impedance term related to STATCOM, and transformer become irrelevant because the STATCOM is a constant current source.

$$V_F^1 = V_G^1 - I_Y^1 Z_B \quad \textbf{(5.7)}$$

$$V_F^2 = -I_Y^2 Z_B \quad \textbf{(5.8)}$$

$$V_F^0 = -I_Y^0 Z_B \quad \textbf{(5.9)}$$

$$3 I_F^1 R_F = V_F^1 + V_F^2 + V_F^0 \quad \textbf{(5.10)}$$

$$I_F^1 = I_F^2 = I_F^0 \quad \textbf{(5.11)}$$

$$I_F^1 = I_Y^1 + I_{PCC}^1 \quad \textbf{(5.12)}$$

Positive sequence fault current (I_F^1) was calculated by considering equation (5.10), substituting for sequence fault voltage from equations (5.7), (5.8) and (5.9) and considering the relationship of equation (5.11) and (5.12). This is expressed by (5.13).

$$I_F^1 = \frac{V_G^1 + Z_B^1(I_{PCC}^1 + I_{PCC}^2 + I_{PCC}^0)}{3R_F + 3\,Z_B^1} \quad \textbf{(5.13)}$$

Since the fault current sequence sets are equal and the sequence set current from the STATCOM at B_{PCC} is known, the grid current sequence sets can be calculated by adapting equation (5.12) and is expressed in (5.14). The sequence set for voltage at fault can be expressed by (5.15). Similarly, by considering the current and impedance term in the respective branch, the voltages at B_Y and B_{PCC} can be calculated in sequence set terms as expressed in (5.16) and (5.17).

$$I_G^{120} = I_F^{120} - I_{PCC}^{120} \quad \textbf{(5.14)}$$

$$V_F^{120} = V_G^{120} - I_Y^{120} Z_B \quad \textbf{(5.15)}$$

$$V_Y^{120} = V_G^{120} - I_Y^{120} Z_G \quad \textbf{(5.16)}$$

$$V_{PCC}^{120} = V_F^{120} + I_{PCC}^{120} Z_A \quad \textbf{(5.17)}$$

Using the standard method from [13], the sequence set terms can be transformed into their respective three phase terms. This converted phase terms were further analysed for the fault phase (Phase A) at B_{PCC} and B_Y. The expression for the phase voltage at the B_{PCC} is given in

equation (5.18), this gives the impedance measured at the PCC, shown in (5.19) and (5.20). This measured impedance consists of two terms; the line impedance between the PCC and the fault, and an error term which arises as a result of the fault resistance as shown in (5.20). The error in measured impedance increases with increase in the ratio of FCC from each of the side (equation 5.21). As the FCC of IBR systems is limited this term can be very large causing maloperation of distance protection systems. In order to reduce this error, the FCC from the STATCOM or other IBR systems needs to be increased.

$$V_{PCC}^{A} = dZ_L\, I_{PCC}^{A} + R_F\, I_F^{A} \tag{5.18}$$

$$Z_{PCC}^{A} = \frac{V_{PCC}^{A}}{I_{PCC}^{A}} = \frac{dZ_L\, I_{PCC}^{A} + R_F(I_Y^{A} + I_{PCC}^{A})}{I_{PCC}^{A}} \tag{5.19}$$

$$Z_{PCC}^{A} = dZ_L + R_F \frac{I_Y^{A}}{I_{PCC}^{A}} + R_F \tag{5.20}$$

$$Z_{PCC}^{error} = R_F \frac{I_Y^{A}}{I_{PCC}^{A}} + R_F \tag{5.21}$$

Similarly, the error in impedance measurement can be calculated at B_Y.

$$V_Y^{A} = (1-d)\, Z_L\, I_Y^{A} + R_F\, I_F^{A} \tag{5.22}$$

$$Z_Y^{A} = \frac{V_Y^{A}}{I_Y^{A}} = \frac{(1-d)\, Z_L\, I_Y^{A} + R_F(I_Y^{A} + I_{PCC}^{A})}{I_G^{A}} \tag{5.23}$$

$$Z_Y^{A} = (1-d)\, Z_L + R_F \frac{I_{PCC}^{A}}{I_Y^{A}} + R_F \tag{5.24}$$

$$Z_Y^{error} = R_F \frac{I_{PCC}^{A}}{I_Y^{A}} + R_F \tag{5.25}$$

The equations (5.21) and (5.25) shows that the measured apparent impedance includes an error component (Z^{error}) proportional to the product of a fault resistance and an expression that involves the ratio of the remote and local currents. It is important to realize that if the local source is IBR or non-synchronous and therefore weak, the magnitude of the ratio of the two currents may be considerably greater than 1. As a result, the distance protection relays may suffer from ineffective operation.

In the sub-sections ahead, these derived equations for a SLG fault would be used to determine the behaviour of the measured voltage, current and impedance as seen from B_{PCC} and B_Y for varying R_F, I_{PCC} and G_{FL}.

5.3.2.1 Single Line to Ground Fault with Varying Fault Resistance

In this sub-section, the SLG fault is analysed to understand the error in the impedance measurement (Z^{error}) with increasing R_F and as the fault location d moves away from B_{PCC} to B_Y. The G_{FL} had been fixed at $1{,}000\ MVA$ at $132\ kV$ in the UK power distribution or transmission systems. The G_{FL} is relatively strong compared to STATCOM, which is rated at $60\ MVA$ during normal operation.

The analytical results for the faulted phase (Phase A) are shown in Figure 5-9, and depicts the voltage, current and impedance as seen from at B_{PCC} and B_Y for varying R_F. The current contribution from the STATCOM is fixed as shown subplot (c) at $1{,}050\ A$ ($4\ pu$). As fault location moves away from B_{PCC}, the V_{PCC} increases (subplot (a)) which in turn increases the calculated Z_{PCC} (subplot (e)). The offset seen in the V_{PCC} for $1\ \Omega$ (0.003 pu), $5\ \Omega$ ($0.17\ pu$) and $10\ \Omega$ ($0.03\ pu$) is because of voltage drop caused by grid current.

In subplot (e) the dotted line shows impedance $d\ Z_L$ and the coloured lines show apparent impedance ($d\ Z_L + \frac{I_Y^A}{I_{PCC}^A} R_F + R_F$) or impedance measured at B_{PCC}. As R_F is increased the error term in the impedance measurement increases. As the fault location moves away from B_{PCC}, the transmission line impedance increases and adds to the error in the impedance measurement. When R_F is $10\ \Omega$, the error in impedance measurement is higher than for than that of lower R_F values.

As the fault location moves closer to B_Y, the measured V_Y increases with increase in R_F as shown in subplot (b). The offset seen in the V_Y for different R_F is because of the voltage drop caused by I_{PCC}. For various R_F values, the change in I_Y minimal except when the fault is nears B_Y ($d = 0$). The I_Y increases as the fault location moves closer to B_Y as shown in subplot (d) because Z_L reduces and voltage drop caused by the I_{PCC} increases.

In subplot (f) the dotted line shows impedance $(1\text{-}d)\ Z_L$ and the coloured lines shows apparent impedance $((1\text{-}d)\ Z_L + \frac{I_{PCC}^A}{I_Y^A} R_F + R_F)$ as seen from B_Y. As R_F increases, the error term in the impedance measurement increases. It can also be concluded that the greater the difference in

FCC between STATCOM and grid voltage source, the larger margin of error during impedance measurement. As the fault location gets closer to B_Y, the transmission line impedance decreases and adds to the error in the impedance measurement. When R_F is 10 Ω, the error in impedance measurement is higher than that of other lower R_F values.

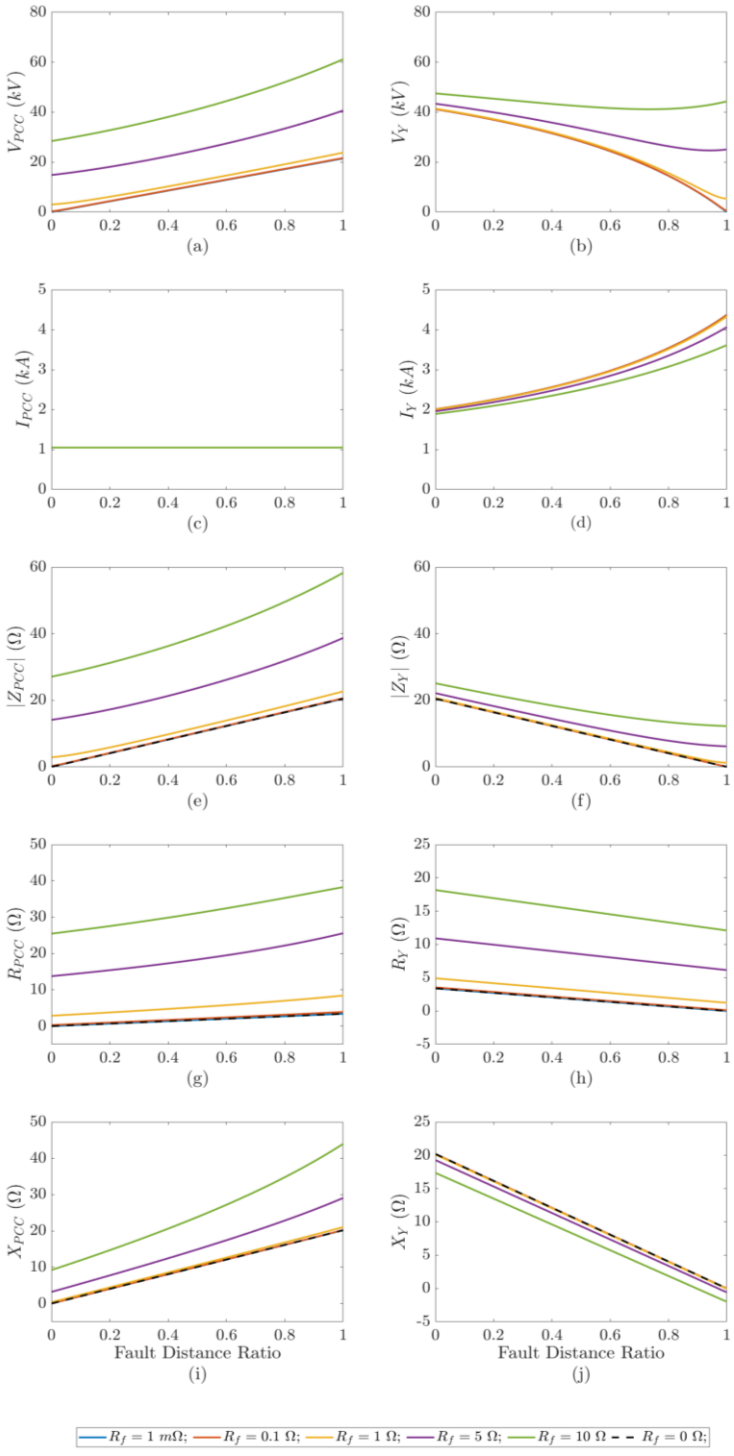


Figure 5-9: Analytical results for varying fault resistance and real and imaginary part of measured Z_{PCC} and Z_Y; (G_{FL} = 1,000 *MVA* *STATCOM*$_{FL}$ = 240 *MVA*) for Phase A.

It should be noted that at higher R_F, such as 10 Ω, the V_{PCC} can become higher than $0.25\ pu$ and this would mean that a STATCOM with eTC may not be able to inject FCC of $4\ pu$. This practical constraint of $4\ pu/2\ pu$ has been ignored in the analysis presented here.

To examine closely $|Z_{PCC}|$ and $|Z_Y|$, the real and imaginary part of the measured impedance had been split and is shown in subplots (g), (h), (i) and (j). When the fault resistance is increased, it leads to slight error in the reactance or imaginary part (see subplot (i) and (j)) of the impedance. However, the difference was mostly observed in the real or resistive part of the impedance (see subplot (g) and (h)). This can be attributed to the fact that the FCC from the STATCOM is injected at 90° to the grid voltage but this may not be the case in practice if the synchronisation of the STATCOM controller is disturbed by the voltage dip.

5.3.3 Single Line to Ground Fault with Varying Fault Current Contribution from STATCOM with eTC

It is important to understand the impact of increasing FCC from STATCOM with eTC on the impedance measurement error term ($\boldsymbol{Z^{error}}$), when the grid fault level and the fault resistance have been fixed. The analysis completed for various $\boldsymbol{R_F}$ is extended to assess the impact on the error in impedance measurement at $\boldsymbol{B_{PCC}}$ and $\boldsymbol{B_Y}$ with increasing FCC from STATCOM with eTC. For this part of the analysis, $\boldsymbol{R_F}$ was $\mathbf{1\ \Omega}$ and $\boldsymbol{G_{FL}}$ of the grid voltage source was $\mathbf{1000\ MVA}$. The other parameters of the proposed network Figure 5-7 remained the same. The FCC from STATCOM is increased from $\mathbf{1\ pu}$ to $\mathbf{10\ pu}$ as shown in sublot (c) of Figure 5-10. And the other subplots of Figure 5-10 show the results of the analysis.

As the FCC is increased the impedance measurement error decreases as observed in subplot (e). Equation (5.21) indicates that as the FCC increases the error term get reduced and lowers the margin of error during impedance measurement.

The increase in FCC from the STATCOM has negligible impact on the current contribution from the grid voltage source as observed in subplot (d). This is because even with $\mathbf{10\ pu}$ FCC from the STATCOM, the considered value of $\boldsymbol{R_F}$ is low to make a significant voltage drop ($\boldsymbol{I_{PCC}\ R_F = 260\ A\ \times 10 \times 1 = 2{,}600\ V}$) and reduce the current contribution from the grid. With increased $\boldsymbol{R_F}$ ($\mathbf{= 10\ \Omega}$) the voltage drop would increase to $\mathbf{26\ kV}$.

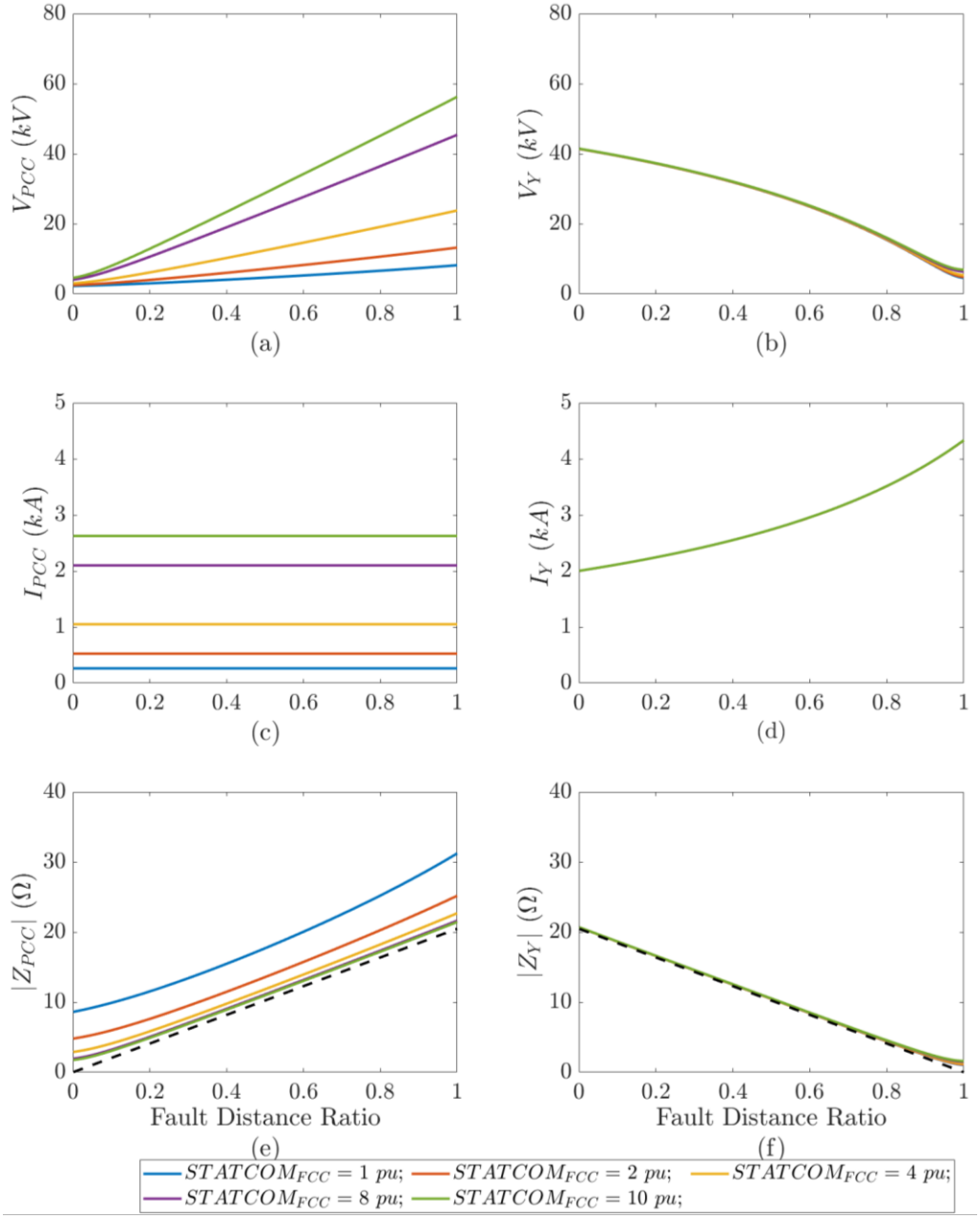


Figure 5-10: Analytical results for varying fault current contribution from STATCOM with eTC ($G_{FL} = 1000\ MVA$; $R_F = 1\ \Omega$; $STATCOM_{FL} = 240\ MVA$) in Phase A. Black dashed line represents impedance $d\ Z_L$ in subplot (e) and $(1\text{-}d)\ Z_L$ in subplot (f).

5.3.4 Single Line to Ground Fault with Varying Fault Level of the Grid Voltage Source

This analysis focuses on the impact on impedance error (Z^{error}) when varying the fault level of the grid, while fixing the FCC from STATCOM with eTC and fault resistance parameters. Similar to previous analysis, the impact of varying the grid fault level is assessed for impedance

measurement error at B_{PCC} and B_Y. This is done by fixing the R_F $(= 1\ \Omega)$ and FCC from STATCOM $(STATCOM_{FCC} = 4\ pu)$.

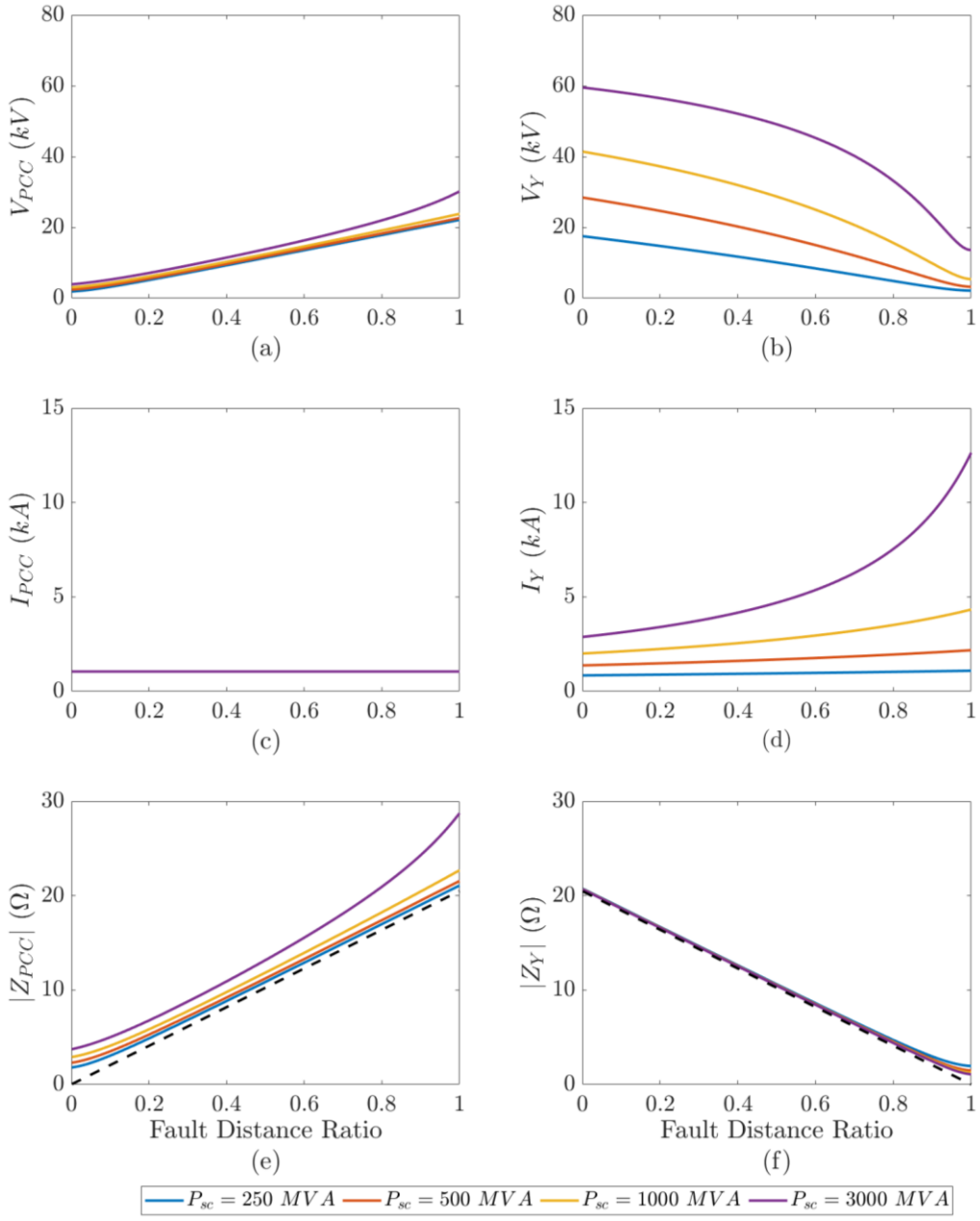


Figure 5-11: Analytical results for varying grid fault level (G_{FL}); ($R_F = 1\ \Omega$ $STATCOM_{FL} = 240\ MVA$) for Phase A. Black dashed line represents impedance $d\ Z_L$ in subplot (e) and $(1\text{-}d)\ Z_L$ in subplot (f).

The other parameters of the proposed network (Figure 5-7) remained the same. Increase in G_{FL} means that the grid "strength" has increased and the impedance between the grid voltage source and terminal B_Y decreases. The subplot (d) of Figure 5-11 shows the increase in FCC from grid as the grid strength is increased. At $d = 0$, when the fault level of the STATCOM $(240\ MVA)$

and the grid ($250\ MVA$) are approximately equal, impedance measurement error is the lowest at B_{PCC}. As the grid strength increases, difference between FCC from STATCOM and the grid increases at B_{PCC}, which in-turn increases the impedance measurement error (see subplot (e)).

5.3.5 Line to line Fault with Varying Fault Resistance

The L-L fault throws up different problems to the already investigated SLG fault. During a close-up zero-resistance L-L fault, the voltage in the faulty phases drops to a little above $0.577\ pu$, which means that the maximum FCC delivered after tap-change at PCC may be limited to $2\ pu$ or less. As suggested in section 5.2.2, an over-rated STATCOM has been considered for this analysis to support a tap-change at 60% of the line voltage and produce $2\ pu$ FCC from the STATCOM with eTC. The G_{FL} and R_F values were at $1{,}000\ MVA$ and $1\ m\Omega$. The L-L fault is between Phase A and Phase B.

The analytical results for one of the faulted phases (Phase A) is shown in Figure 5-12. The current contribution from the STATCOM is fixed as shown in subplot (c) at $525\ A\ (2\ pu)$. At $d = 0$, the offset in V_{PCC} is caused by grid current. It can be observed from subplot (e) of Figure 5-12 that the impedance measurement error (Z^{error}) seen from B_{PCC} increases with increase in fault resistance.

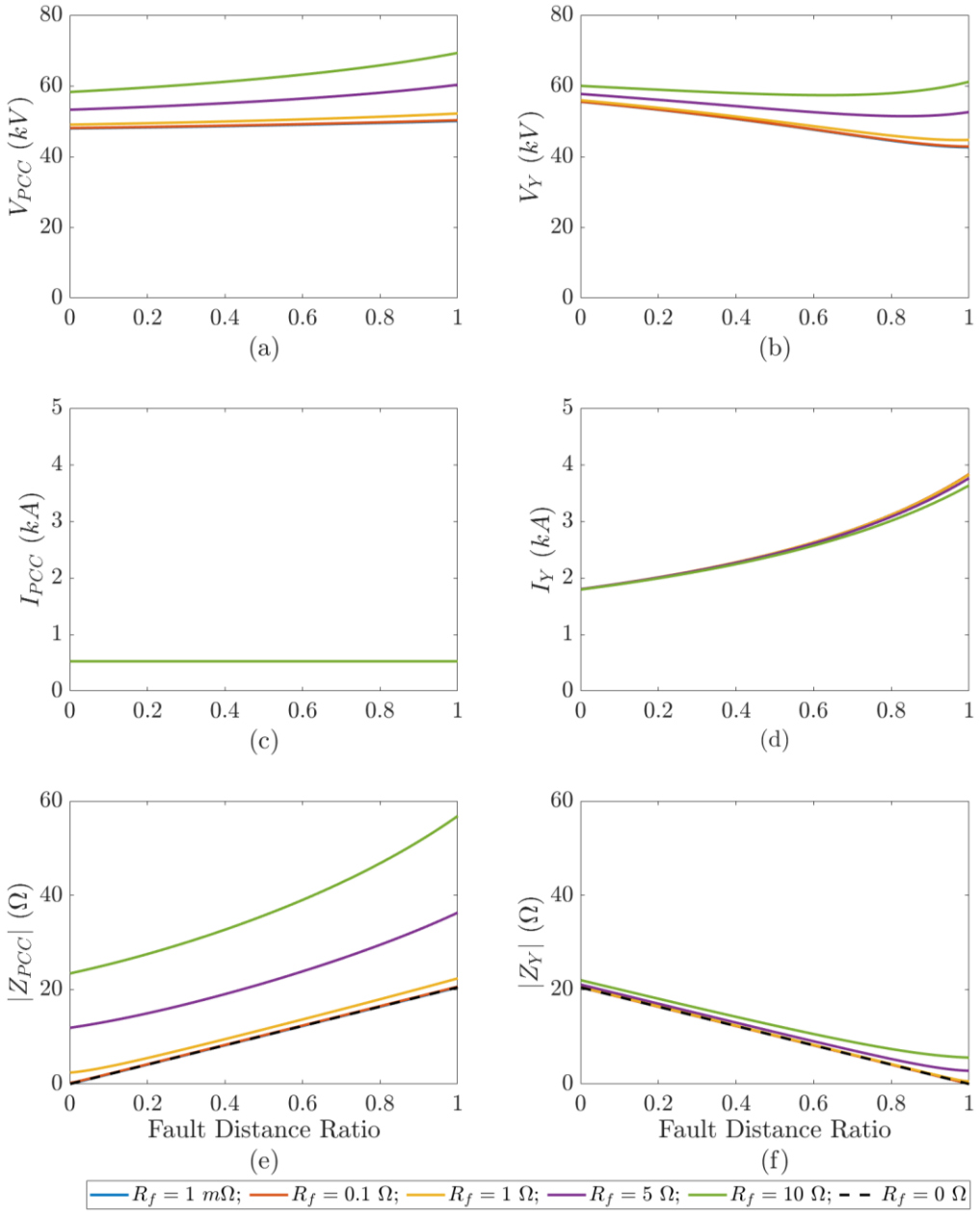


Figure 5-12: Analytical results for line to line fault with varying fault resistance (R_F); ($G_{FL} = 1,000\ MVA$; $STATCOM_{FL} = 240\ MVA$) for Phase A.

5.3.6 Comparison of FCC between Synchronous Condenser, STATCOM with Tap Changer Circuit and Standard STATCOM

Several grid operators whose systems have high penetration of IBR have commissioned synchronous condensers (SynCond) to provide various services that IBR do not normally provide [108]. Notable among the services is inertia, but also gaining importance is fault current infeed. A SynCond is essentially a synchronous generator without a prime mover, but which has an exciter system that allows reactive power to be produced. The SynCond inherits the inertia, reactive power supply and fault current of the standard synchronous machine. A SynCond has the capability to support a power network with reactive power thereby avoiding voltage collapse and ensuring good dynamic voltage recovery after severe system faults, but it can also supply a large magnitude current during a short-circuit fault to ensure accurate operation of protection relays. Because of these attributes, several grid operators are adding SynCond to their networks [109].

The objective of this sub-section is to gain understanding of how the fault current supplied in three cases compares. The cases are a SynCond, a STATCOM with eTC and a standard STATCOM. They will be compared for a SLG fault under a fixed value of R_F and G_{FL}. To create a reasonable comparison between the three cases, the positive sequence impedances of the network in all cases were made equal, and the three different sources of reactive compensation were configured to provide the same pre-fault current at B_{PCC}.

A standard STATCOM can be connected to the grid with or without a coupling transformer but the STATCOM with eTC requires an interface transformer. To enable a fair comparison, a coupling transformer was used in both of these cases. However, the standard STATCOM was a delta-star configuration, with delta winding on the STATCOM-side as is normal practice for a STATCOM.

To set a benchmark for operation under unbalanced conditions, a SynCond will be tested in the network shown in the Figure 5-13 (which is a single line diagram). Bus B_{PCC} is where the current from the SynCond is measured, Bus B_F is for the total fault current and Bus B_Y is for the fault current from the grid source. The currents observed during faults will be analysed as positive-, negative- and zero-sequence components at B_{PCC}. The parameters for the transformer used for connecting the SynCond are matched to those of the STATCOM network except that

the SynCond-side winding is delta configured. The grid-side windings of the SynCond are connected in star with the neutral grounded.

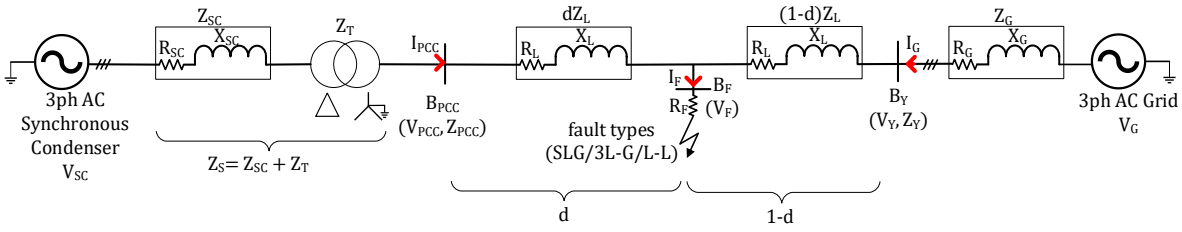


Figure 5-13: The synchronous condenser, coupling transformer, transmission line and grid source arrangement.

5.3.6.1 Excitation Voltage of the Synchronous Condenser

To calculate the excitation voltage required, the assumption was made that the two voltage sources (SynCond and Grid) were in phase, that is δ =0, which is true if no real powers flow in a reactance dominated line as indicated by equation **(5.26)** as is the case for a SynCond.

$$P_e = \frac{V_t E_i sin(\delta)}{X_{SC}} \qquad \textbf{(5.26)}$$

Where exported electrical power is P_e, machine reactance is X_{SC}, internal voltage is E_i, terminal voltage is V_t and δ is the angle between the voltages.

To achieve export of reactive power, the value of E_i is set according to equation **(5.27)** .

$$Q = \frac{V_t\,(E_i \cos(\delta) - V_t)}{X_{SC}} \qquad \textbf{(5.27)}$$

For the test network, the grid voltage, and the internal voltage of the SynCond are separated by impedances of SynCond phase impedance (Z_{SC}), coupling transformer (Z_T), transmission line (Z_L) and grid source impedance $((Z_G)$.

To supply rated current of equal to STATCOM with eTC, the capacitive reactive current is $I_{PCC} = -j1.0\ pu$, the voltage E_i required is given by:

$$E_i = V_G + I_{PCC}(Z_{SC} + Z_T + Z_L + Z_G) \qquad \textbf{(5.28)}$$

The calculated value of E_i ensures that the total positive-sequence impedance and current in normal operation for the STATCOM and SynCond cases were equal.

5.3.6.2 Sequence Network Connection Diagram for SLG

The sequence network connection for a SLG fault for SynCond network is shown in Figure 5-14. The notation used in this figure remain mostly the same as for the STATCOM with eTC. The voltage source of SynCond ($V_{SynCond}$) is shown in the positive sequence network. The positive and negative sequence network connection include SynCond impedance ($Z_{SynCond}$) and the transformer impedance (Z_T) as Z_S. As two sources in the proposed network are voltage sources, they do not appear in the negative- and zero-sequence connection diagram. Moreover, due to delta configured windings on the SynCond side, the impedance of the SynCond is not included in the zero-sequence connection diagram.

The positive, negative and zero-sequence are connected in series for a SLG fault such that the positive-sequence fault current (I_F^1), negative-sequence current (I_F^2), and zero-sequence current (I_F^0) are all equal. The direction of the current in each sequence network is defined to be out from the fault terminal (F) to flow via the fault impedance and the other sequence networks to return to the neutral terminal (N).

The fault point (F) is between the two sources (the SynCond and the grid) and so the fault current in each sequence network divides into the two branches according to the impedance and the voltage sources (if present) and then recombine to enter the next sequence network. The voltage at the fault location is given by $3\ R_F\ I_F^1$ and the contribution from each sequence network can be found by standard circuit theory similar to a STATCOM with an eTC network.

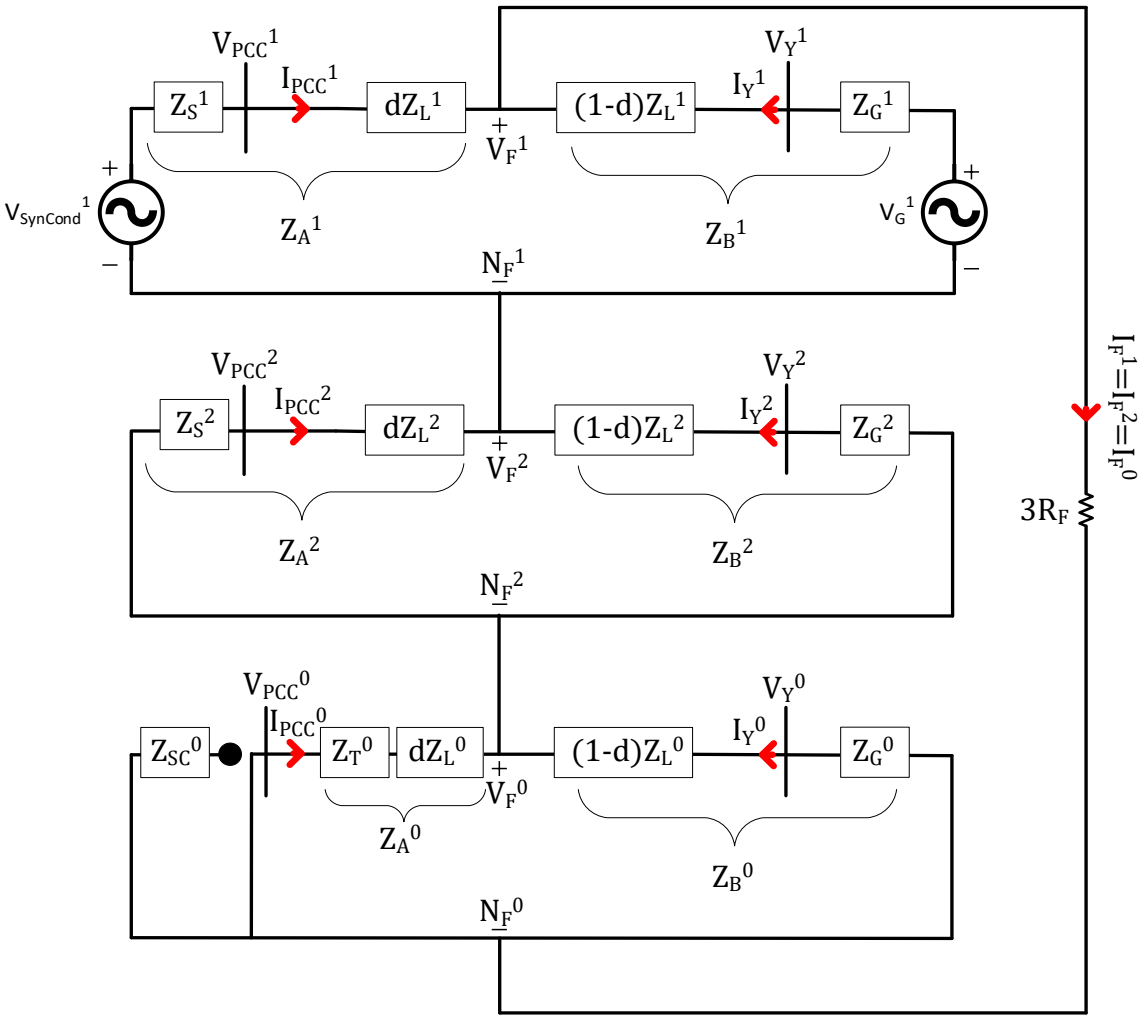


Figure 5-14: Sequence network connection for a SLG fault @ B_{PCC} for synchronous condenser network

The sequence network connection for a SLG fault for a standard STATCOM network is shown in Figure 5-15. The STATCOM is modelled as a positive sequence current source as typical STATCOM current control systems are designed to prevent the injection of negative sequence current and so the negative sequence branch is open circuit. The zero-sequence branch of the converter is also open-circuit but the delta-star configuration of the coupling transformer creates a low impedance branch.

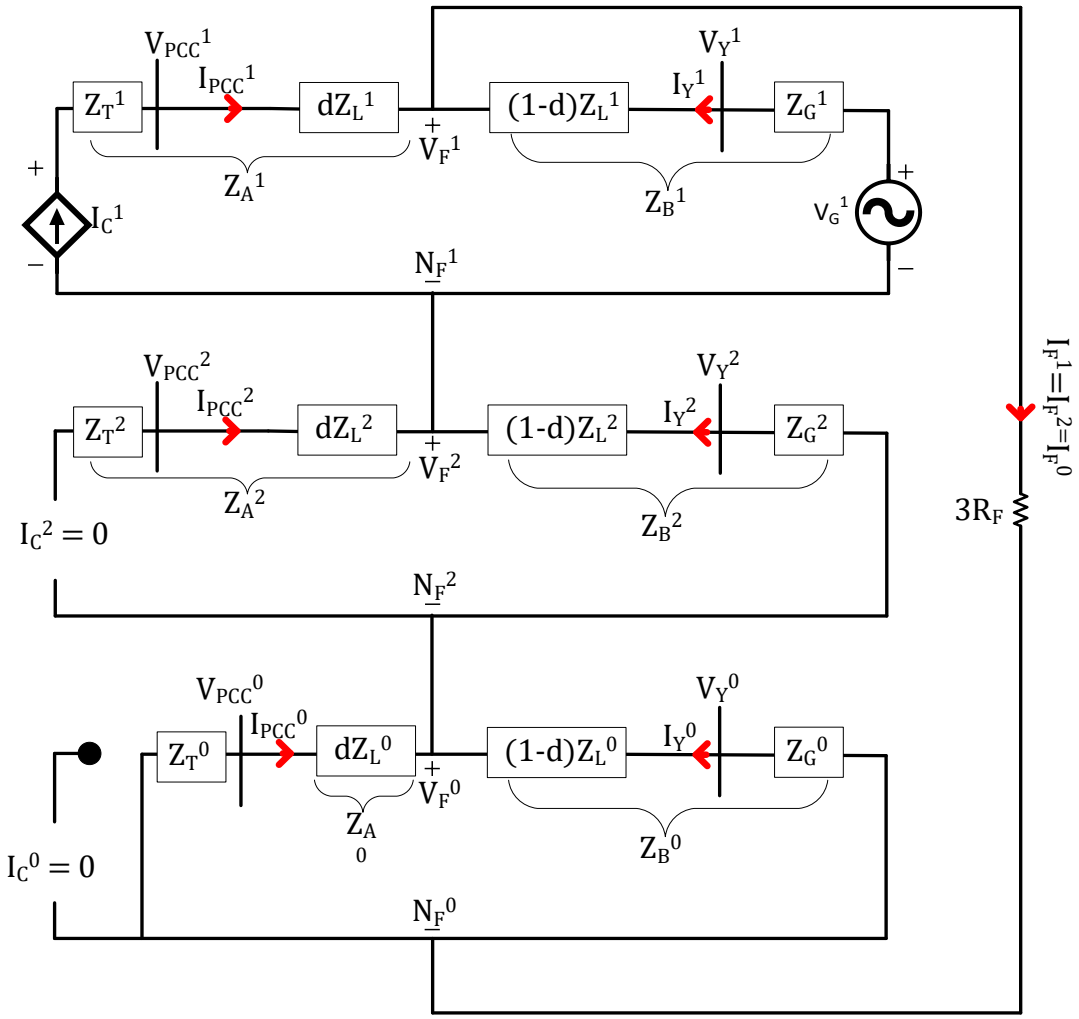


Figure 5-15: Sequence network connection for a SLG fault @ B_{PCC} for a STATCOM (SSBC) with coupling transformer (delta-star) network

5.3.6.3 Fault Current Contribution Comparison for SLG

Figure 5-16 shows how the voltage, current and impedance as seen from B_{PCC} and B_Y changes for varying fault locations. The FCC for SynCond is greater than STATCOM with eTC, which in turn is greater than the standard STATCOM. The FCC from STATCOM remains independent of fault location as current is controlled to the reference value. In contrast, the FCC from the SynCond is seen to be lower for more distant faults due to the increased line impedance between the SynCond and the fault. The FCC from the grid remains largely unchanged across the different types of sources (SynCond, STATCOM with eTC and standard STATCOM) but it does change with fault distance.

At $d = 0$; the current at B_{PCC} for standard STATCOM is the two-thirds of that of STATCOM with eTC. Further analysis will be conducted in the next section, when the sequence set currents are examined.

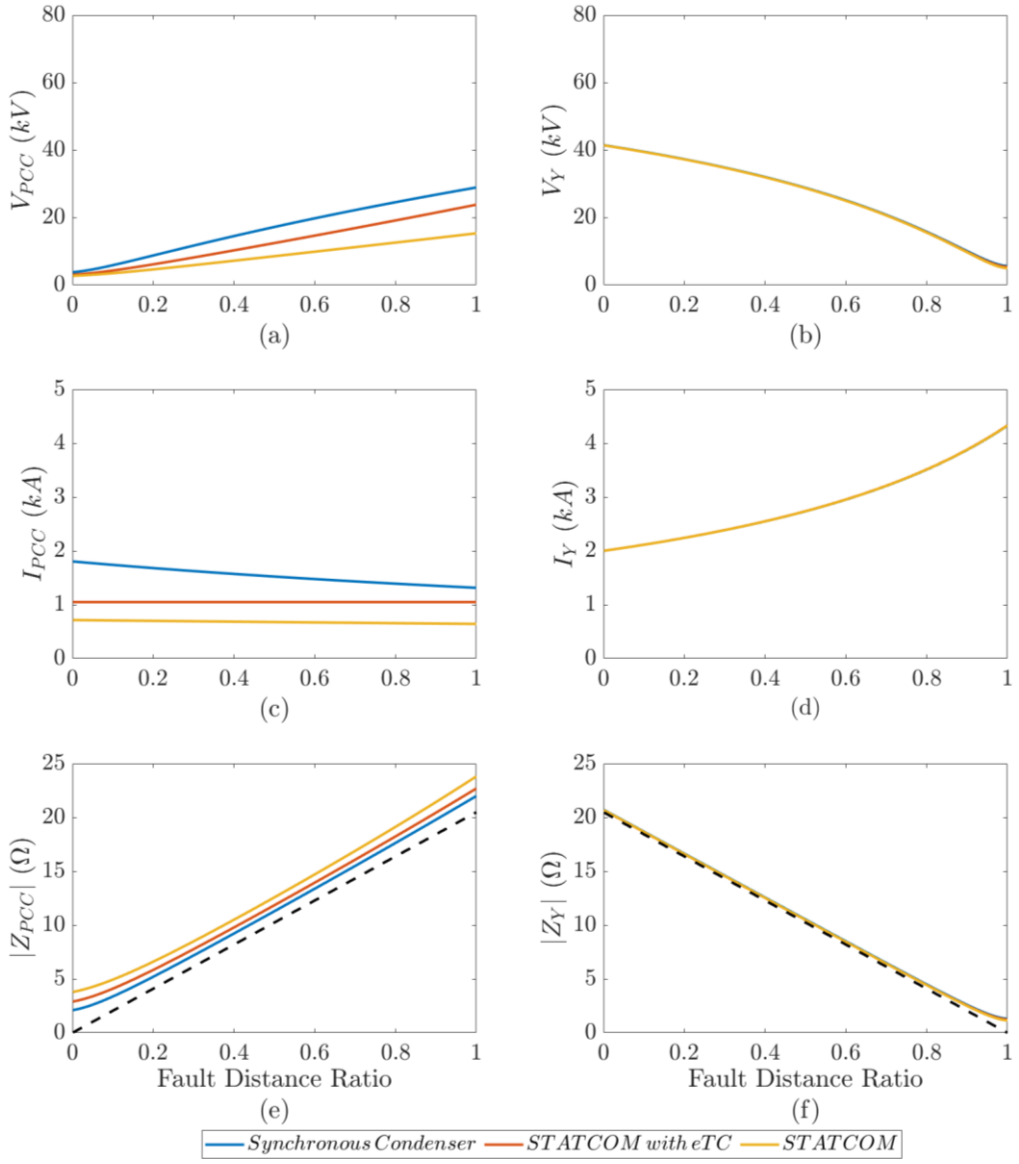


Figure 5-16: Comparison of voltage, current and impedance at B_{PCC} and B_Y with synchronous condenser, STATCOM with tap-change circuit and STATCOM without tap-change ($R_F = 1\ \Omega$; $G_{FL} = 1000\ MVA$; $STATCOM_{FL} = 60\ MVA$; $STATCOM\ with\ eTC_{FL} = 240\ MVA(4\ pu\ FCC)$). Black dashed line represents impedance $d\ Z_L$ in subplot (e) and $(1\text{-}d)\ Z_L$ in subplot (f).

For a fault near to B_{PCC}, the magnitude of SynCond current and grid current are approximately equal but as the fault moves away from the SynCond and towards the grid source, the FCC from the grid increases. This is due to change in the impedance between the grid source and

the fault on the one hand and between the SyndCond and the fault on the other. As the impedance increases the current decreases. For faults close to B_{PCC}, with greater FCC from SynCond, the error seen in impedance measurement at B_{PCC} is the lowest among the three sources. The FCC from STATCOM with eTC is $\approx 1\,pu$ more than the FCC from a standard STATCOM. The increase in FCC contributes towards reduced error seen in STATCOM with eTC.

5.3.6.4 Current Sequence-set Comparison for Synchronous Condenser, STATCOM with eTC and STATCOM during SLG fault

For STATCOM with eTC, it is expected that during the fault the transformer is tapped-down to $1{:}\,1$ on phase A to produce a $4\,pu$ fault contribution with the other two phases staying at $4{:}\,1$ and producing $1\,pu$ current. This can be viewed as a $1\,pu$ balanced current with an additional $3\,pu$ on phase A.

The additional $3\,pu$ single-phase current can be decomposed as a combination of $1\,pu$ in each of the sequence components. In total, the STATCOM with eTC current seen at B_{PCC} is expected to be:

- positive-sequence current $= 1\,pu + 1\,pu = 2\,pu$
- negative-sequence current $= 1\,pu$
- zero-sequence current $= 1\,pu$

The results in Figure 5-17 validate this. Recall that these currents are expressed in terms of rms current with $1\,pu \approx 262\,A$. At $d = 0$, the positive-, negative- and zero-sequence FCC capability of the STATCOM with eTC is approximately two-thirds, half and one-thirds that of the SynCond, respectively. It is worth noting that in sequence terms, the additional fault current appears small even though the current in the faulted phase is reasonably large. In phase terms it is $4\,pu - 1\,pu = 3\,pu$. In sequence terms it is $\frac{3\,pu}{3} = 1\,pu$.

The large difference in contribution in zero-sequence current can be attributed to the low impedance in the zero-sequence network of the SynCond that is provided by the path through the delta-star transformer. The zero-sequence current flows via the ground of the grid-side winding which can be arranged to be low impedance. In contrast, the STATCOM with an eTC network adopted a Y-Y transformer configuration which means the zero-sequence current must

flow via the power converter of the STATCOM and thus it must be limited to prevent damage to the power electronics.

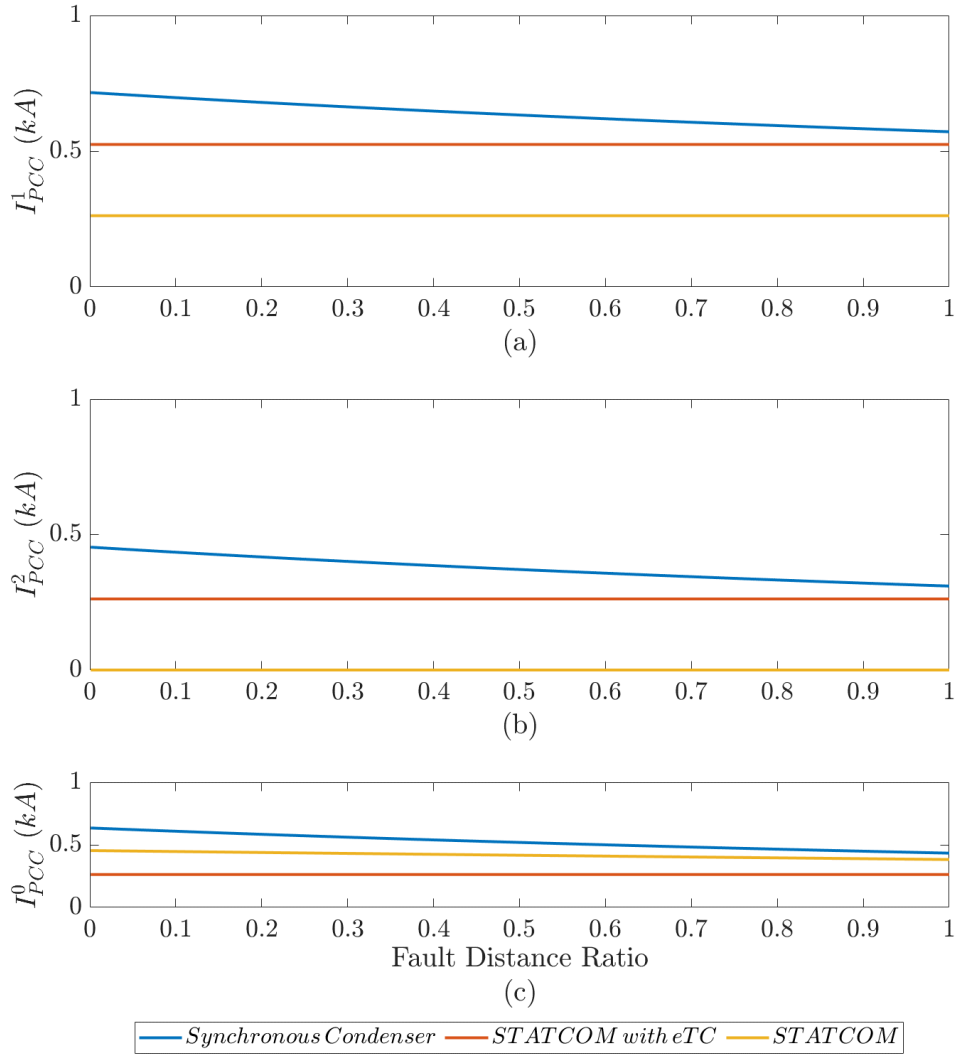


Figure 5-17: Comparison of positive, negative and zero sequence current at R_1 with synchronous condenser, STATCOM with eTC and STATCOM without eTC ($R_F = 1\ \Omega$; $G_{FL} = 1000\ MVA$; $STATCOM_{FL} = 60\ MVA$; $STATCOM\ with\ eTC_{FL} = 240\ MVA(4\ pu\ FCC)$).

The results also show that the positive-sequence current in the standard STATCOM with a delta-star configured coupling transformer is half of that of the STATCOM with eTC because of the inability to increase the current under fault conditions. For the zero-sequence, the standard STATCOM produces about twice the current compared to the STATCOM with eTC. This is attributed to the low impedance in the zero-sequence network of the delta-star configured transformer. It was assumed that the standard STATCOM did not produce any

negative-sequence current. It should be noted that the standard STATCOM, like other IBR systems, can generate negative-sequence current if the current reference is determined in the sequence sets and the control is in phase coordinates or dual positive and negative rotating dq frame but that was not provided here.

The sequence current set comparison for a fault at B_{PCC} or $d = 0$, is also shown in

Table 5-2. The standard STATCOM takes advantage of the low impedance in the zero-sequence network, and it produces a $2\ pu$ zero-sequence current.

The analysis shows that there is a significant advantage in using a delta-star configured coupling transformer for the standard STATCOM. The standard STATCOM produces a combined FCC of $\cong 2.7\ pu$ in the faulted phase (Phase A) with a large contribution of zero-sequence current because of the delta-star transformer but no negative-sequence current. The STATCOM with eTC achieved 4 pu total FCC with equal amounts of negative- and zero-sequence current.

Table 5-2: SC vs STATCOM with eTC vs STATCOM sequence currents for a SLG fault @ B_{PCC}; ($R_F = 1\ \Omega$; $G_{FL} = 1000\ MVA$)

	Synchronous Condenser	**STATCOM with eTC**	**Standard STATCOM**
Positive-sequence	$\sim 716\ A\ (2.73\ pu)$	$\sim 524\ A\ (2\ pu)$	$\sim 262\ A\ (1\ pu)$
Negative-sequence	$\sim 453\ A\ (1.73\ pu)$	$\sim 262\ A\ (1\ pu)$	$0\ A$
Zero-sequence	$\sim 634\ A\ (2.42\ pu)$	$\sim 262\ A\ (1\ pu)$	$\sim 454\ A\ (1.7\ pu)$
Combined FCC in faulted phase (Phase A)	$\sim 1{,}803\ A\ (6.8\ pu)$	$\sim 1{,}050\ A\ (4\ pu)$	$\sim 716\ A\ (2.7\ pu)$

During solid L-L fault, the STATCOM with eTC will provide $2\,pu$ in the faulted phases compared to the standard STATCOM, which can only provide $1\,pu$. The transformer delta-star configuration provides no advantage during a L-L fault because zero-sequence current is not available in L-L fault.

This sequence set comparison will also help inform further work on how the control system and its current references for the standard STATCOM and STATCOM with eTC changer should be configured for effective operation of distance protection scheme in network with high penetration of IBR systems.

5.3.6.5 Electronic Tap Change circuit with Grounding Transformer

The previous sub-section showed that the standard STATCOM with a delta-star configured coupling transformer provided more zero-sequence current ($\approx 2\,pu$) than the proposed STATCOM with a star-star eTC. It is therefore interesting to consider adding a zero-sequence path to the STATCOM with star-star eTC. This cannot be done with a delta-star coupling transformer because of the difficulty of combining the eTC and its current control with a delta winding that will be discussed in Section 5.3.7.1; instead, a grounding transformer is considered. Figure 5-18 shows a grounding transformer added to the previous circuit configuration on the grid-side of the coupling transformer just before the PCC. The currents at the eTC are now labelled I^A_{eTC}, I^B_{eTC} and I^C_{eTC}.

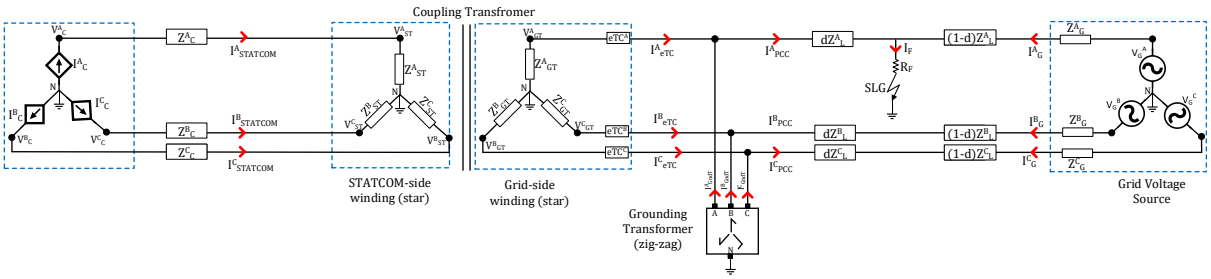


Figure 5-18: The delta configured STATCOM (SDBC), tap-changer in the coupling transformer, transmission line and grid source arrangement (showing three phase)

Ground transformers are used in distribution networks to provide a neutral point in a three-phase system. A grounding transformer is typically a three-phase two-winding transformer with winding 1 and winding 2 connected in series in the so-called zig-zag configuration [110].

The sequence network connection diagram for a SLG fault is shown in Figure 5-19. In the zero-sequence connection diagram, the grounding transformer provides another low impedance path for the fault current. The impedance of the grounding transformer is labelled as Z_{GndT}.

During a SLG fault on Phase A, the fault current, through the fault resistance, returns to the source through the ground and neutral of the grounding transformer. Because of the nature of the winding arrangement of the grounding transformer, it provides a low impedance path for zero-sequence current (labelled as Z_{GndT} in zero-sequence section of Figure 5-19) but a high impedance for the positive- and negative-sequence currents (so no additional paths are present in Figure 5-19).

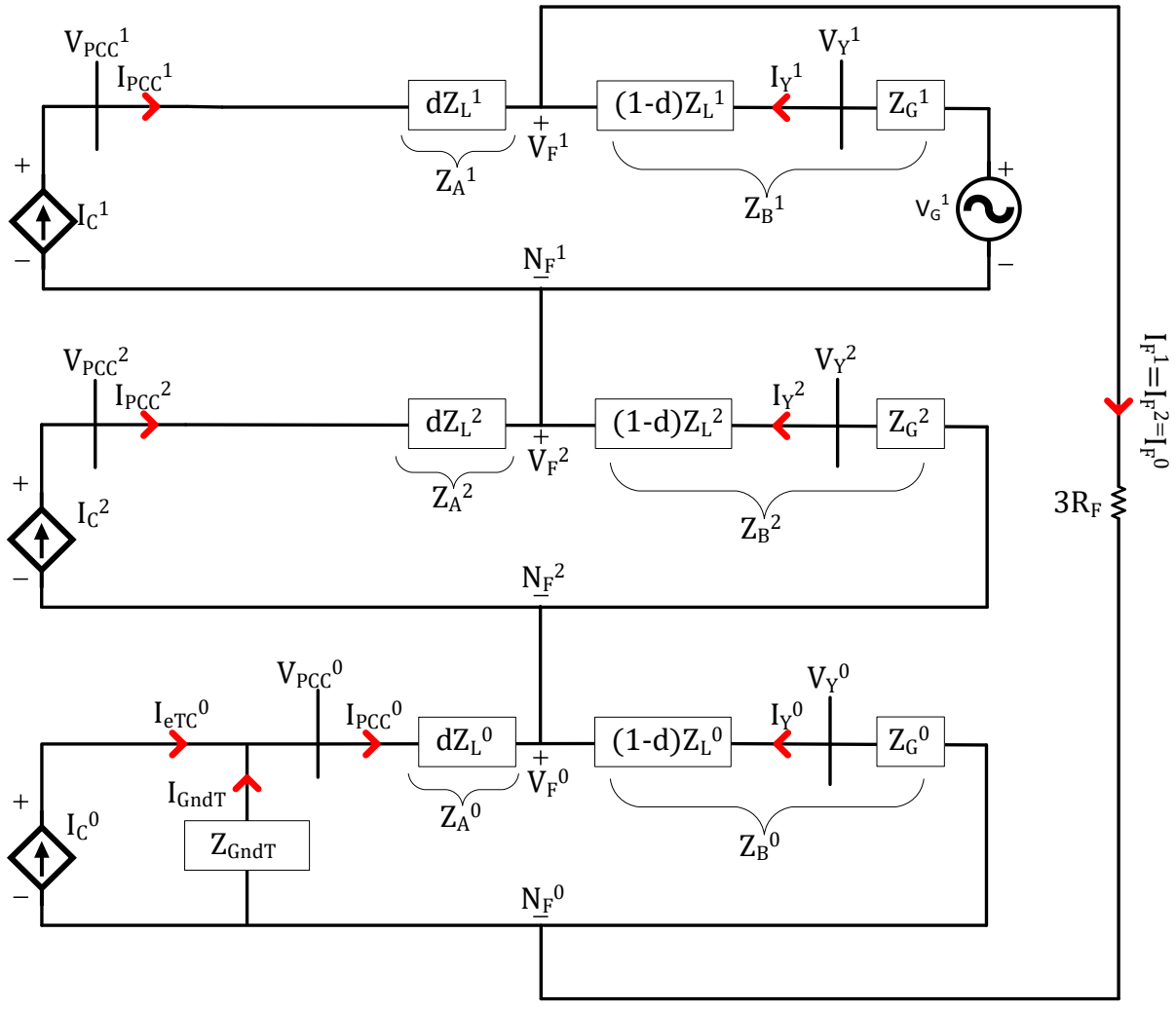


Figure 5-19: Sequence network connection for SLG fault @ B_{PCC} for a STATCOM (SDBC) with coupling transformer (delta-star) network

The sequence network diagram is further analysed in Appendix E to calculate the zero-sequence current at PCC (I^0_{PCC}) expressed in equation (5.29). The fault current in each sequence network ($I^1_F = I^2_F = I^0_F$) is given by expression (5.30).

$$I^0_{PCC} = \frac{I^1_F\, Z^0_B + I^0_C\, Z^0_{GndT}}{Z^0_{GndT} + Z^0_A + Z^0_B} \tag{5.29}$$

$$I^1_F = \frac{V^1_G + I^1_C\, Z^1_B + I^2_C\, Z^2_B + I^0_C \left(\frac{Z_{GndT}\, Z^0_B}{Z_{GT} + Z^0_A + Z^0_B}\right)}{3\, R_F + Z^1_B + Z^2_B + \left(\frac{Z^0_B\, (Z_{GndT} + Z^0_A)}{Z_{GndT} + Z^0_A + Z^0_B}\right)} \tag{5.30}$$

The presence of Z_{GndT} directly impacts the magnitude of I^0_{PCC}. With lower Z_{GndT}, the I^0_{PCC} can be increased as it provides a low impedance path for I^1_F. With additional zero-sequence current, the current in the faulted phase (I^A_{PCC}) increases. With increased FCC, after the addition of low impedance grounding transformer, the proposed STATCOM with eTC can lower the impedance measurement error.

The positive impact of adding a grounding transformer is in increasing the zero-sequence current at the PCC seems to be accompanied by a disadvantage in that it may add to the crow-bar current when the crowbar is used to protect the STATCOM from a rapid rise in voltage after fault clearance. The recovering PCC voltage will drive excessive current towards the STATCOM converter which is an unbalanced current which is aided by a low impedance path for its zero-sequence component through the grounding transformer. Simulation results which illustrate this point are included in Appendix E.

The simulation results added to the Appendix E show that $I_{CR} \cong 3.32$ kA (Figure E-2). When simulated in similar conditions, the proposed network of STATCOM with eTC without a grounding transformer sees $I_{CR} \cong 2.2$ kA (Section 5.4.2 and Figure 5-28).

5.3.7 Delta Configured STATCOM

The recent publication [70], shows that partially rated battery storage (PRS) can be added to a delta configured STATCOM to allow the STATCOM to offer some short-term real power services at a relatively low cost. This subsection assesses the feasibility of implementing the eTC on a delta configured STATCOM interfaced through a star-star coupling transformer.

A preliminary investigation suggests that the proposed eTC circuit in the coupling transformer can be extended to a SDBC configured STATCOM, as shown in Figure 5-20 and [70]. The SDBC arm currents ($I_C^{AB}, I_C^{BC}, I_C^{CA}$) are based on the line current at eTC ($I_{eTC}^{A}, I_{eTC}^{B}, I_{eTC}^{C}$). The impedances of STATCOM-side winding in three phases are shown as Z_{ST}^{A}, Z_{ST}^{B} and Z_{ST}^{C}. The impedances of the grid-side winding are shown as Z_{GT}^{A}, Z_{GT}^{B} and Z_{GT}^{C}.

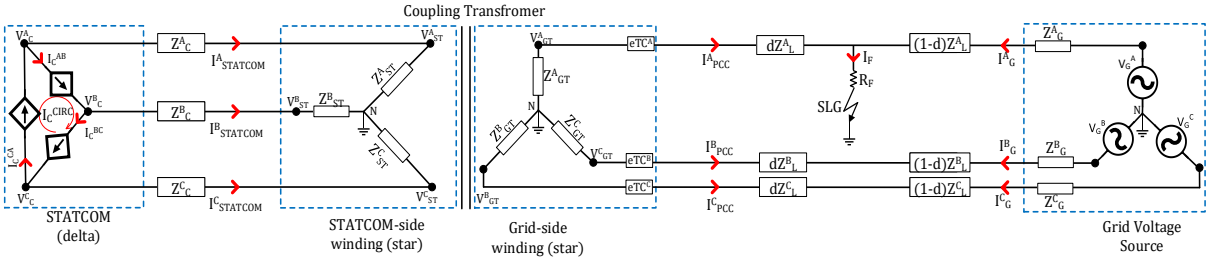


Figure 5-20: The delta configured STATCOM (SDBC), tap-changer in the coupling transformer, transmission line and grid source arrangement (showing three phase)

The current controller needs to map between the currents in the delta arms of SDBC and the currents in the lines of the eTC. For SDBC, the current references for STATCOM can be expressed as functions of the grid current references plus a zero-sequence arm current reference that flows within the triangle of the STATCOM. This zero-sequence or circulating current (I_C^{CIRC}) in SDBC can be used for internal balancing of the controller if needed.

The STATCOM controller needs to reduce the current at eTC to 0A and hold it for suitable duration to allow the tap-changer thyristors to turn off and must do that by control of the currents in the SDBC arms. This would require the arrangement of the new set of current control referencing for symmetrical and asymmetrical faults on the grid.

It is also important to note that when translating the grid current into the arm current of the converter, the feedback signals for the controller is multiplied by transformer turns ratio. The multiplication factor changes with the change in tap position or transformer turns ratio. It should be noted that zero-sequence current is removed before translating the grid current into the arm current of the converter.

In the SSBC (star configured STATCOM) case, the STATCOM current was controlled on a per-phase basis and the eTC was operated separately for each phase. In the SDBC (delta configured STATCOM) case, the current reference needs to be changed for all three phases

simultaneously and then the eTC can be operated in the faulted phase/s to change the turns ratio. This will not let a zero-sequence current appear in the SDBC.

It should be noted that the SDBC network would provide similar zero-sequence current to that achieved with SSBC network because of the star-star configured coupling transformer. Further work is required to ensure that the arm currents and the crow-bar circuit in the SDBC works effectively and are within limits to ensure the safety of SMs. The circulating current within SDBC can further be utilised for the SMs voltage management as described in [70].

Looking more broadly, there would be value in developing a system that can provide reactive power, fault current and inertia and frequency response through a single system. Currently, ESOs are adopting synchronous condensers to provide reactive power, fault current and inertia but not frequency response. Separate BESS systems are being installed for frequency response ancillary services. The recent publication proposed a delta-connected Modular Multilevel STATCOM with partially rated storage (PRS-STATCOM), capable of providing both reactive and active power support [70]. Additional work is required to tie together a BESS backed STATCOM with tap-changer capability in the coupling transformer. A STATCOM that can provide (i) reactive power regulation, (ii) frequency response services and (iii) increased FCC, could be beneficial for future networks.

5.3.7.1 Delta-Star Configured Coupling Transformer

IBR systems generally utilise a delta-star configured coupling transformer to connect to the Grid. This sub-section will discuss why the proposed eTC cannot be added to a conventional delta-star configured coupling transformer.

A preliminary investigation suggests that an eTC circuit cannot be implemented in a delta-star configured transformer for SSBC (Figure 5-21) or SDBC (Figure 5-22). This is due to the delta-star transformer which blocks the STATCOM from being able to control the zero-sequence current at PCC (I_{PCC}^{0}). Therefore, it is impossible for the STATCOM to drive the current in the thyristors of the eTC to zero for forced commutation.

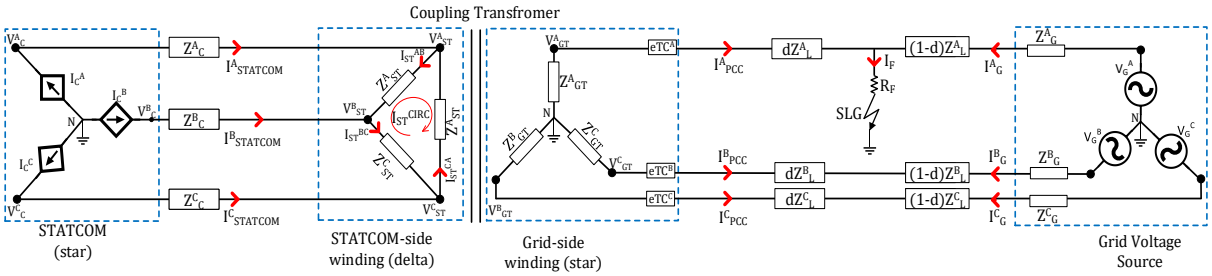


Figure 5-21: The star configured STATCOM, tap-changer in the delta-star configured coupling transformer, transmission line and grid source arrangement (showing three phase)

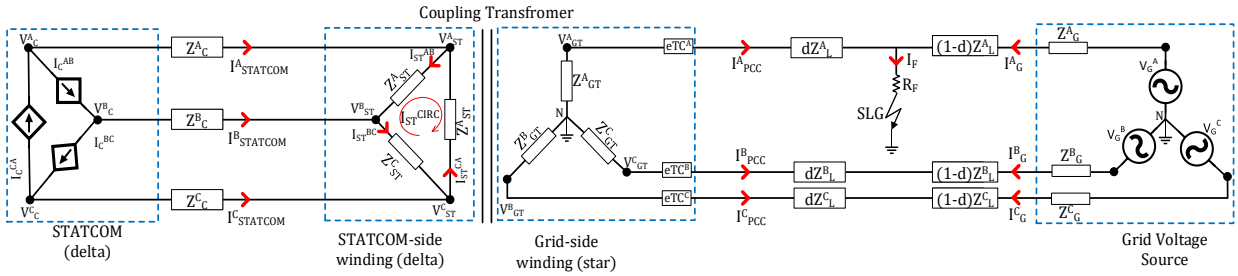


Figure 5-22: The delta configured STATCOM, tap-changer in the delta-star configured coupling transformer, transmission line and grid source arrangement (showing three phase)

For example, SLG faults on the star configured grid-side windings translates (or results) to a collapse in the L-L voltage on the delta configured STATCOM-side windings. Normally in a delta configured winding, the balanced set of voltages in three phases sum to zero [70].

During a SLG fault on the star-configured grid-side windings, the voltages on the delta configured STATCOM-side windings are no longer balanced and do not sum to zero [70]. The presence of voltage in the delta windings initiates a circulating current (I_{ST}^{CIRC}) which will be a zero-sequence current because it is common to all three phases. Due to normal transformer action, this zero-sequence current is also seen in all three phases of the star-side including the faulted phase (I_{PCC}^{A}).

The equivalent sequence network diagram for delta-configured STATCOM with delta-star configured coupling transformer is shown in Figure 5-23. In the zero-sequence network section, the delta winding provides a short path for the returning I_F^0. Hence, neither the circulating current (I_{ST}^{CIRC}) in the delta winding nor the zero-sequence current in the thyristors

of the eTC can be controlled to zero because it does not flow through the STATCOM and is not subject to it its current controller.

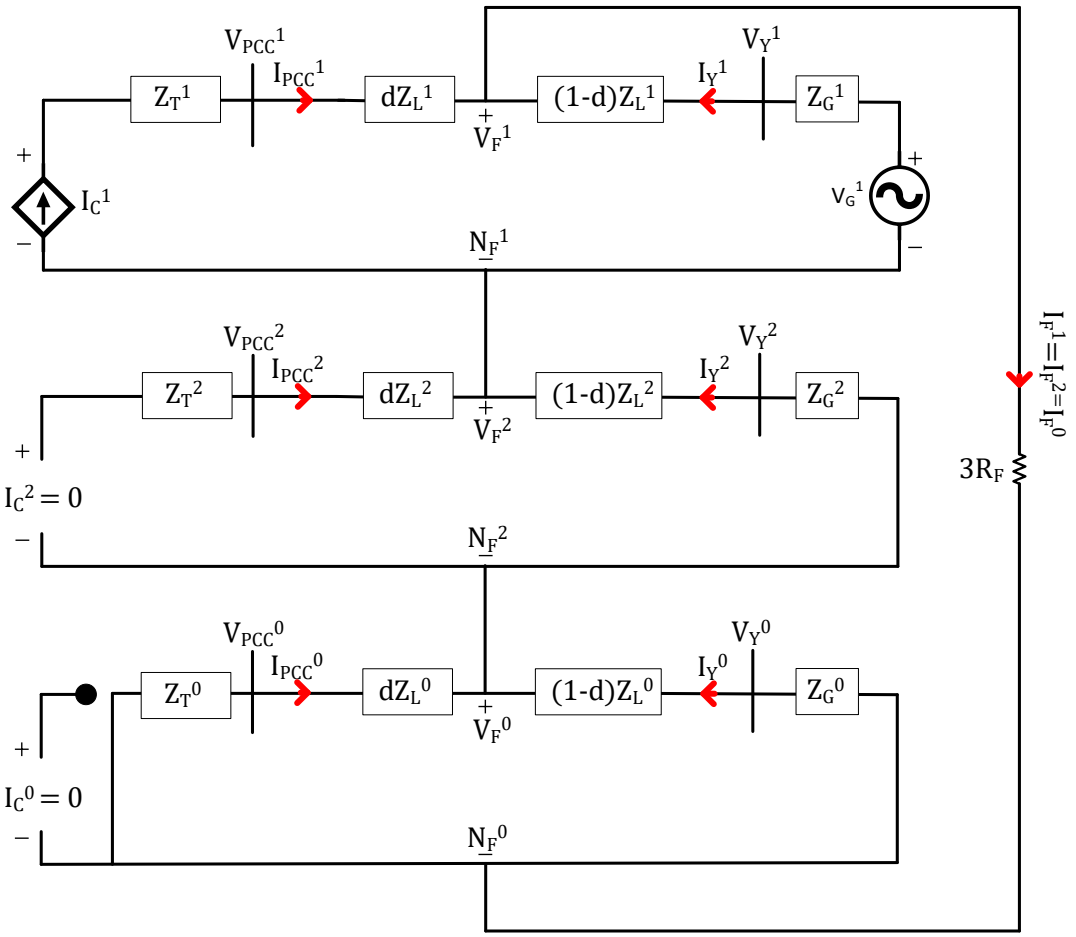


Figure 5-23: Sequence network connection for a/an SLG fault @ B_{PCC} for a STATCOM (SDBC) with coupling transformer (delta-star) network

The sequence network connection for SLG fault with star-configured STATCOM will remain largely similar to the diagram shown in Figure 5-23 and it will have a current source available in both negative- and zero-sequence connection diagrams. The presence of a current source in zero-sequence network does not change the impact of the delta configured STATCOM-side windings discussed above.

5.4 Simulation Verification

The operation of the proposed STATCOM with eTC was verified using the same case study network of the 132 kV network used for the analysis in Section 5.3 and shown again here in Figure 5-24. The case-study network was built in MATLAB/Simulink using the Simscape toolbox.

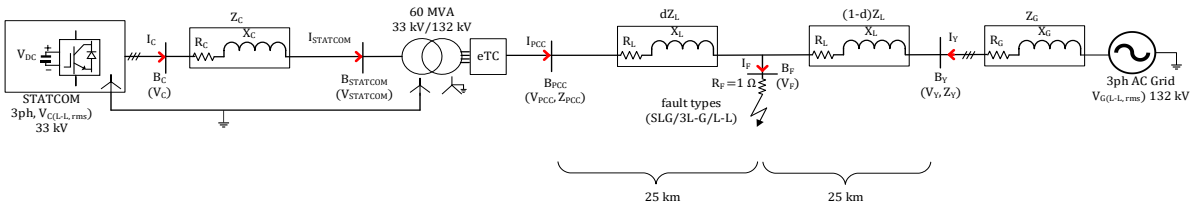


Figure 5-24: The STATCOM, tap-changer in the coupling transformer, transmission line and grid source arrangement were simulated in Simulink

For convenience, the following key features are repeated here. The network consists of a $60\ MVA$ STATCOM with a $33\ kV/132\ kV$ step-up coupling transformer with a thyristor-based eTC. The STATCOM is at one end of $50\ km$ long transmission line with a $1{,}000\ MVA$ fault level and $132\ kV$ rated grid voltage source at the other end. The fault is applied part way (fraction d) along the transmission line. The parameters of the system are summarised in Table 5-3. Transformer winding impedance values were taken from the similarly rated transformer, with the grid-side winding split into four equal sections.

Table 5-3: Network Parameters

Parameters	Values
STATCOM impedance (Z_C)	0.1 pu
Coupling Transformer (Z_T)	$0.13\ pu$
Line impedance (Z_L) per 25 km	$0.035\ pu$
Fault resistance (R_F)	$1\ M\Omega$; $10\ \Omega$, $1\ \Omega$ & $1\ m\Omega$
Grid Source Line-to-Line Voltage (kV)	$132\ kV$
Grid fault level (3ph)	$1{,}000\ MVA$
Grid X/R ratio	7

As suggested in Section 5.2 and for simplicity in the initial study, the SSBC circuit was chosen for the STATCOM, which was modelled using a switching-based model, and coupled to a star-star transformer with the proposed eTC. This allowed independence of operation of each phase during asymmetric faults. The voltage rating of the STATCOM is set at 50% above the nominal $33\ kV$ voltage to provide a large headroom for control action, particularly for fast commutation of the eTC switches, and to increase the tolerance of fast post-fault voltage recovery. This will also enable the STATCOM with eTC to inject $2\ pu$ FCC during a close L-L fault. This

represents an increased capital cost compared to common STATCOM practice where the converter would be rated 10-20% above nominal voltage. For simplicity, the STATCOM SMs capacitors were modelled with infinite capacitance such that no SM voltage balancing needed to be implemented in the tests.

Proportional-Resonant (P+R) control in the natural reference frame was selected for current control so that each phase could be independently controlled during asymmetric faults [111]. With a separate current controller for each phase, and the STATCOM can be decoupled into three single-phase systems where the line-to-neutral voltage measurement at B_{PCC} (V_{PCC}) is used as a feedforward voltage in the controller to the corresponding phase leg. Further details about the P+R controller have been included in Appendix D.

Energy storage capabilities were not built into the STATCOM in this study, but this can be considered as a part of future work. The STATCOM was designed to provide and absorb reactive power as part of a wider scheme to regulate voltage of the $132kV$ grid. The study focussed on providing reactive power to support the grid during voltage suppression or fault.

A basic fault classifier is built for the simulation that detects the voltage amplitude in each phase at the PCC by using a moving-window RMS measurement and a threshold detector. For example, during a SLG fault on Phase A, depending on the voltage amplitude at PCC at Phase A, the gate signals to the thyristors of eTC are changed to implement a new turns ratio only in Phase A.

For 3LG and SLG faults, the turns ratio (k) of $1:4$ is used if the V_{PCC} threshold is above $0.7\ pu$. When the V_{PCC} is between $0.7\ pu$ and $0.28\ pu$, the transformer's turns ratio is changed to $1:2$. When V_{PCC} amplitude is below $0.28\ pu$, a turns ratio of $1:1$ is implemented. Further work is required to build a robust fault classifier to improve tap-change sequence process for different range of R_F. Further details of the fault classifier are explained in Appendix D.

5.4.1 Three-line to ground fault

Use of the tap-changer for fault current enhancement needs to be evaluated with symmetric faults (i.e., balanced voltage dips). The simulation results for a 3LG fault at 25 km ($d = 0.5$) are shown in Figure 5-25 and will be discussed in the following sub-sections.

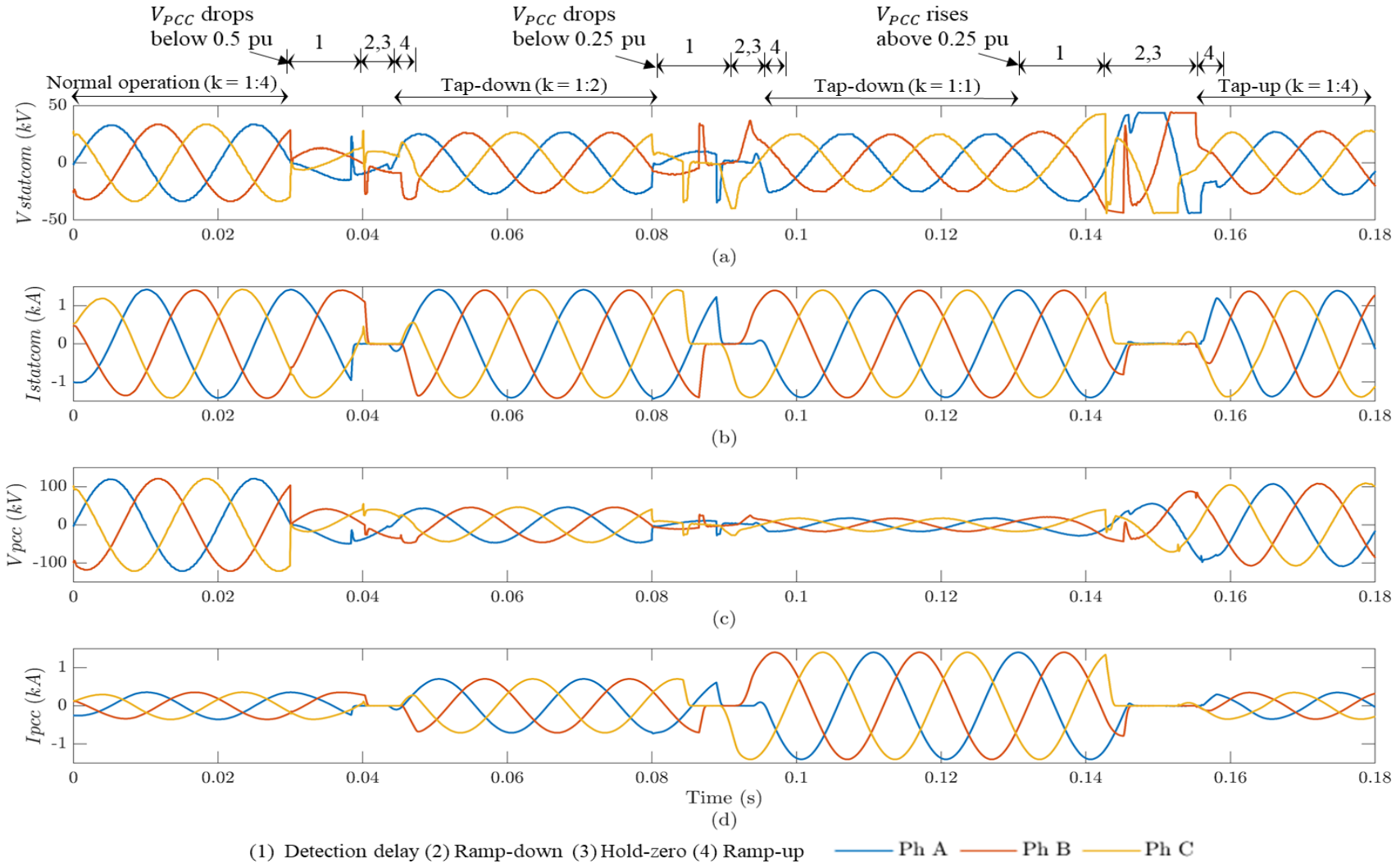


Figure 5-25: Application of three phase to ground (3LG) fault at $0.03\ s$ showing tap-down and increase in fault current in a single stage (a) Voltage at $B_{STATCOM}$ (b) Current $I_{STATCOM}$ (c) Voltage at B_{PCC} and (d) Current I_{PCC}.

5.4.1.1 Normal STATCOM Operation

The STATCOM is initially operating under nominal conditions with the tap-changer set to a k_T of $1:4$ with the STATCOM producing $1\ pu$ capacitive reactive power. On the converter-side of the transformer $33\ kV$ and $1\ kA$ is observed whereas on the grid-side $132\ kV$ and $0.25\ kA$ is observed.

5.4.1.2 Tap-down sequence

At $0.003\ s$, the 3LG fault is applied with a fault impedance of $10\ \Omega$. Subplot (c) of Figure 5-25 shows that the phase voltage at PCC drops rapidly to below $0.5\ pu$ but remains above $0.25\ pu$. The voltage dip is detected by a moving RMS measurement and threshold detector that takes $10\ ms$, (detection delay marked as 1 in the Figure 5-25) so the tap-down sequence is initiated at $0.04\ s$. At this point the current reference for each phase is inverted (multiplied by -1) so that the STATCOM controller drives the current toward zero but the gate-signals for the thyristors in S2d are turned-off so the current does not reverse but the conducting thyristor ceases conduction. This process of "ramp down", marked as 2 in the Figure 5-25, takes 1 ms but the condition is maintained for a "hold zero" period so that the outgoing thyristor is held below its holding current (I_H) value for a turn-off period (T_q). A typical T_q period is 1-2 ms but for demonstration, the hold zero period is set at $5\ ms$, marked as 3 in Figure 5-25, to make it more obvious in the figure. Following the hold-zero period, S2b is switched on and the current reference is raised to $1\ pu$ ($1\ kA\ RMS$) on the converter side in the "ramp-up" period marked as 4 in Figure 5-25. This is seen in subplot (b), which will now be $2\ pu$ ($500\ A\ RMS$) on the grid-side, as seen in subplot (d) because only W2a and W2b are in the current path so the number of turns in the grid-side winding has halved.

At $0.08\ s$ the fault impedance is reduced to $1\ \Omega$ which causes the voltage at the PCC to fall below $0.25\ pu$. The tap-down sequence is initiated again after a detection delay of $10\ ms$. The commutation process described above is repeated except that S2b is being turned off and S2a is turned on after the hold-zero period. This time the turns ratio is reduced to 1:1 and fault current on the grid side is increased to $4\ pu$ ($1\ kA\ RMS$).

5.4.1.3 Tap-up sequence

At $0.13\ s$ the fault was cleared. To mimic the gradual recovery of grid voltage that is commonly seen, the fault resistance was gradually increased to $1\ M\Omega$ over a period of $25\ ms$. Subplot (c)

of Figure 5-25 show the gradual recovery of voltage. When the voltage exceeds $0.25\ pu$ (and after the detection delay), the tap-up sequence is initiated to return the STATCOM to normal operating conditions. The tap-up sequence follows the same procedure as the tap-down sequence, except that S2a (or S2b) is switched off and S2d is switched on to return the turns ratio to $1{:}\,4$. At the end of the hold-zero period, the STATCOM current reference is returned to $1\ pu$ reactive power support and this corresponds to $250\ A$ at the grid side.

5.4.2 Single line to ground fault (SLG)

Use of the tap-changer for fault current enhancement needs to be evaluated with asymmetric faults (i.e., unbalanced voltage dips). The simulation results for a SLG fault on Phase A with fault at 25 km (d=0.5) are shown in Figure 5-26 and will be discussed in the following sub-sections. The fault occurs at $0.03\ s$ and after a detection delay of $8\ ms$ the Phase A current is driven down to zero to facilitate commutation of the eTC. In this case, with fault impedance $1\ \Omega$, the PCC voltage drops below $0.25\ pu$ and so the k_T is set to $1{:}\,1$ and the grid-side current in Phase A is raised to $4\ pu$ while the other two phases (Phase B and Phase C) remain at $1\ pu$. The details of the tap-up sequence are discussed in the next sub-section.

5.4.2.1 Rapid rise of voltage

As described in Section 5.2.5, if post-fault recovery of voltage at the PCC is rapid, there may be insufficient voltage available in the STATCOM converter to control the current and therefore the current cannot be driven to zero in the thyristors meaning that commutation and tap-up cannot occur until the next natural zero-crossing of current. To evaluate this case, the rate of rise of fault resistance during fault clearance is increased, such that full voltage recovery is achieved within $2.5\ ms$.

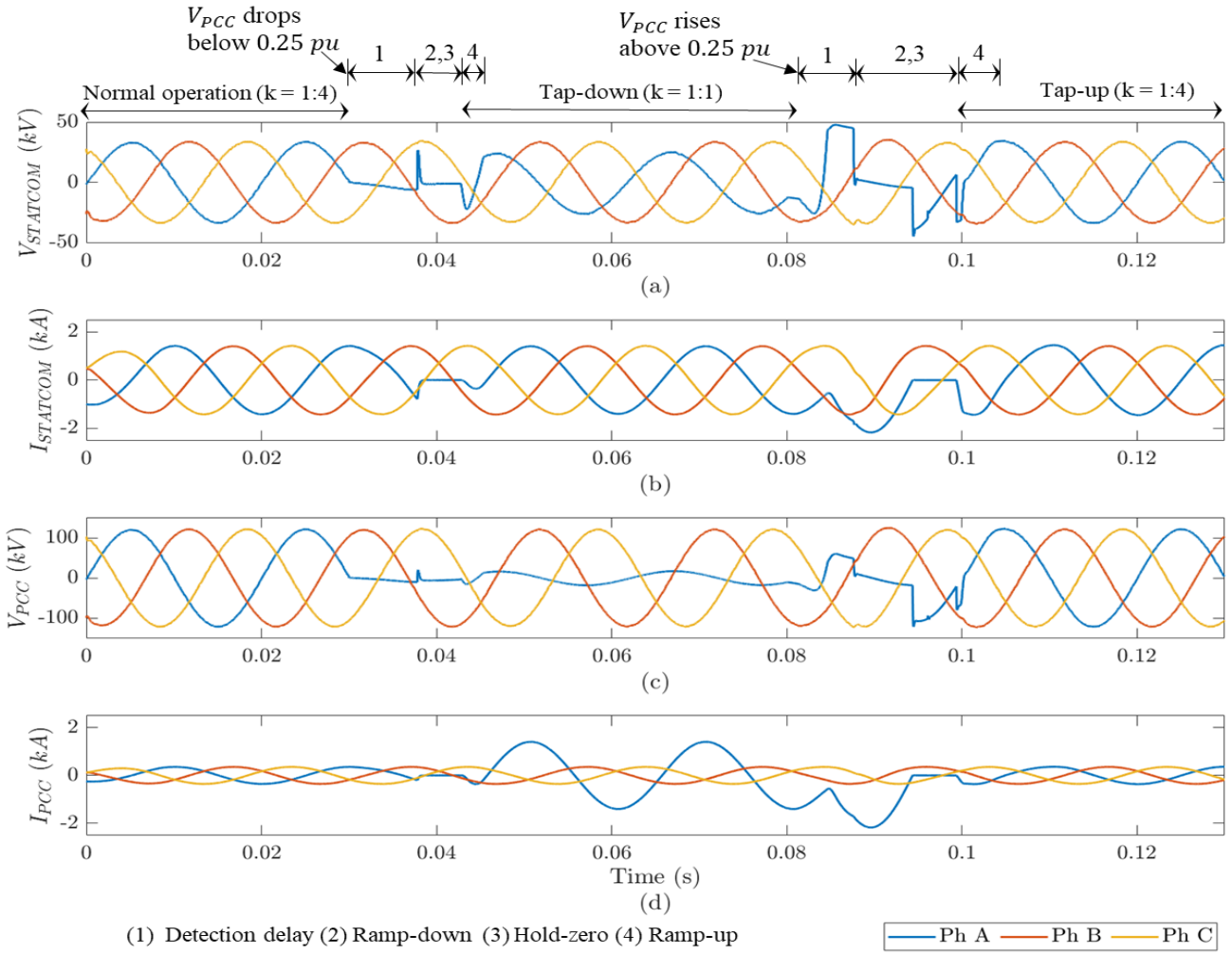


Figure 5-26: Application of single phase to ground at $0.03\ s$ showing tap-down and increase in fault current in a single stage (a) Voltage at $B_{STATCOM}$ (b) Current $I_{STATCOM}$ (c) Voltage at B_{PCC} and (d) Current I_{PCC}

For convenience, the crow-bar circuit in operation protecting the STATCOM has been repeated below as Figure 5-27.

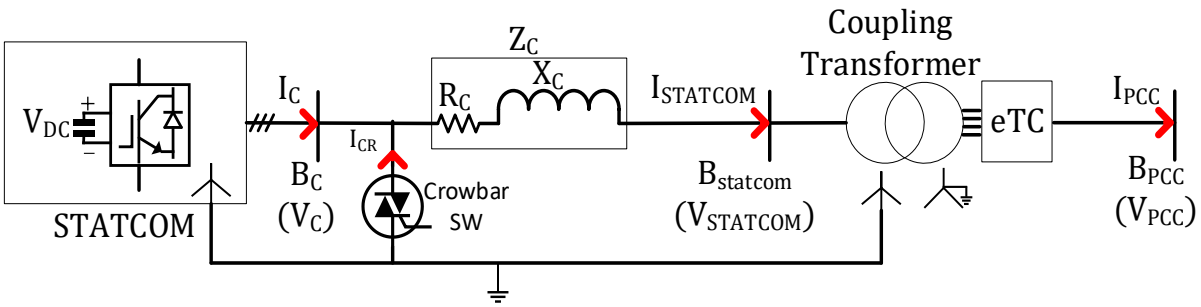


Figure 5-27: Crow-bar circuit in operation protecting the STATCOM

The results for this case are shown in Figure 5-28 for a SLG fault on Phase A. When the fault is cleared at 0.08 s, the PCC voltage rises rapidly and the current in the STATCOM rises as it is driven by the large grid voltage and opposed by a relatively small STATCOM voltage. This is considered a failure of current control and the normal commutation sequence because the thyristors of S2a cannot be turned off during a period of sustained zero current. The current will eventually cross zero under the influence of the grid voltage, but the recovering PCC voltage will drive excessive current through the STATCOM converter potentially damaging the IGBTs within. When an overcurrent is detected, defined here as 25% above nominal converter current, the crow-bar protection scheme is initiated. The crowbar thyristors switch on providing a lower impedance current path than the converter, thereby directing the current away from the SMs, as seen in subplot (b) of Figure 5-28. The surge current can be seen flowing though the crowbar circuit until the next zero crossing when the current can finally be interrupted. The amplitude of the crowbar current (I_{CR}) is set by the combined impedance of the transmission line, grid, transformer and STATCOM reactor. The amplitude of the converter current (I_C) drops to 0 A and the converter is protected from the surge current.

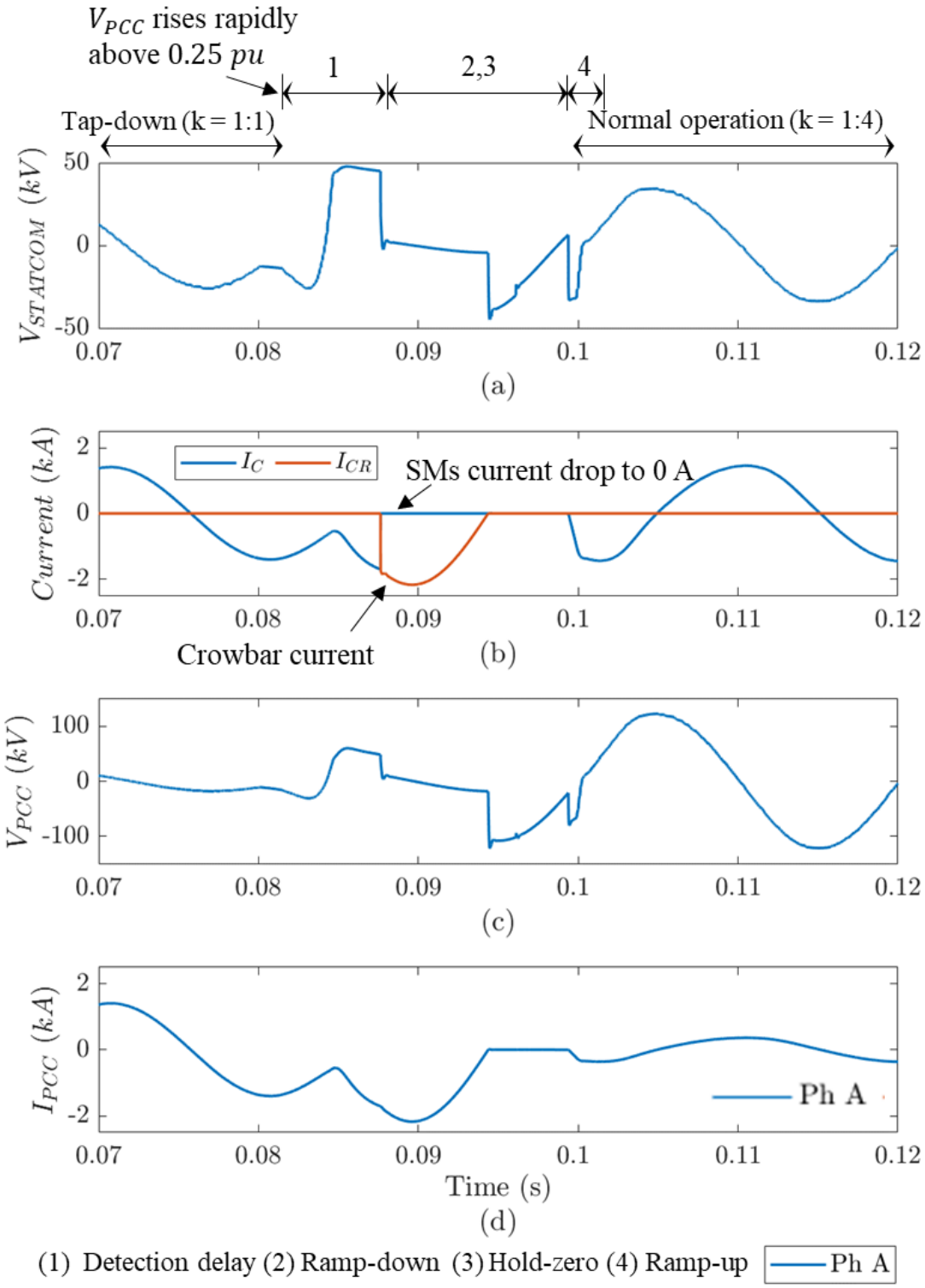


Figure 5-28: Results for SLG fault showing crowbar current during tap-up sequence failure (a) Voltage at $B_{STATCOM}$ (b) Current in Ph A Sub-Modules (I_{SM}) and crowbar circuit (I_{CR}) (c) Voltage at B_{PCC} and (d) Current I_{PCC}.

The maximum crow-bar current expected in each phase can be determined by equation (5.31).

$$I_{CR} = I_C^{t=0} + \frac{V_G/\sqrt{3}}{(Z_C + Z_T + Z_L + Z_G)} \quad \textbf{(5.31)}$$

The transformer impedance (Z_T) would be determined by the k_T at the time of fault recovery. It should also be noted that when the fault clears (i.e. $t = 0$), the phase peak current at STATCOM ($I_C^{t=0}$) can potentially be $1{,}414\ A$ before the excessive current drives into the STATCOM, which will add to the overall current seen in the crow-bar circuit.

The thyristors in S2a of the Phase A turn-off at the next zero-crossing and following a brief hold-zero period S2d is turned on, returning the transformer's turns ratio to $1{:}\,4$. The STATCOM reference current is returned to $1{,}000\ A$ in the ramp-up period and the reactive current delivered to the grid returns to $1\ pu$.

5.4.3 Line to Line fault (L-L)

Similar to 3LG and SLG faults, the STATCOM with eTC was evaluated for a L-L fault by controlling the three phases independently. Figure 5-29 shows results for a L-L fault between Phase A and Phase B at $25\ km$ ($d = 0.5$). The fault occurs at $0.03\ s$ and after a detection delay of $8\ ms$ the Phase A and Phase B currents are driven down to zero to facilitate commutation of the eTC. A low fault resistance of $1\ m\Omega$ will allow the V_{PCC} in faulted phases to drop below the threshold limit of $0.7\ pu$ and inject $2\ pu$ FCC.

In the test case, with fault resistance of $1\ m\Omega$, the PCC voltage drops below $0.7\ pu$ but above $0.28\ pu$ and so the k_T is set to $1{:}\,2$ and the grid-side current in Phase A and Phase B is raised to $2\ pu$ while the other un-faulted phase (Phase C) remains at $1\ pu$.

The over-rating of STATCOM, 50% above the nominal $33\ kV$ voltage, provides a large headroom for control action to complete the tap-change sequence even at $0.7\ pu$ of the line voltage in the faulted phases.

Due to rapid post-fault recovery of voltage at PCC in the faulted phases, tap-up sequence failure is seen in Phase A and Phase B. The thyristors of S2a in two faulted phases cannot be turned off during a period of sustained zero current. I_{CR} eventually crosses zero under the influence of the grid voltage as seen in subplot (b) and (c) of Figure 5-29. The surge current flows though the crowbar circuit until the next zero crossing when the current can finally be interrupted. The

thyristors in S2a of the Phase A and Phase B turn-off at the next zero-crossing and following a brief hold-zero period, S2d is turned on returning the transformer's turns ratio to $1:4$. The STATCOM reference current is returned to $1{,}000\ A$ in the ramp-up period and the reactive current delivered to the grid returns to $1\ pu$.

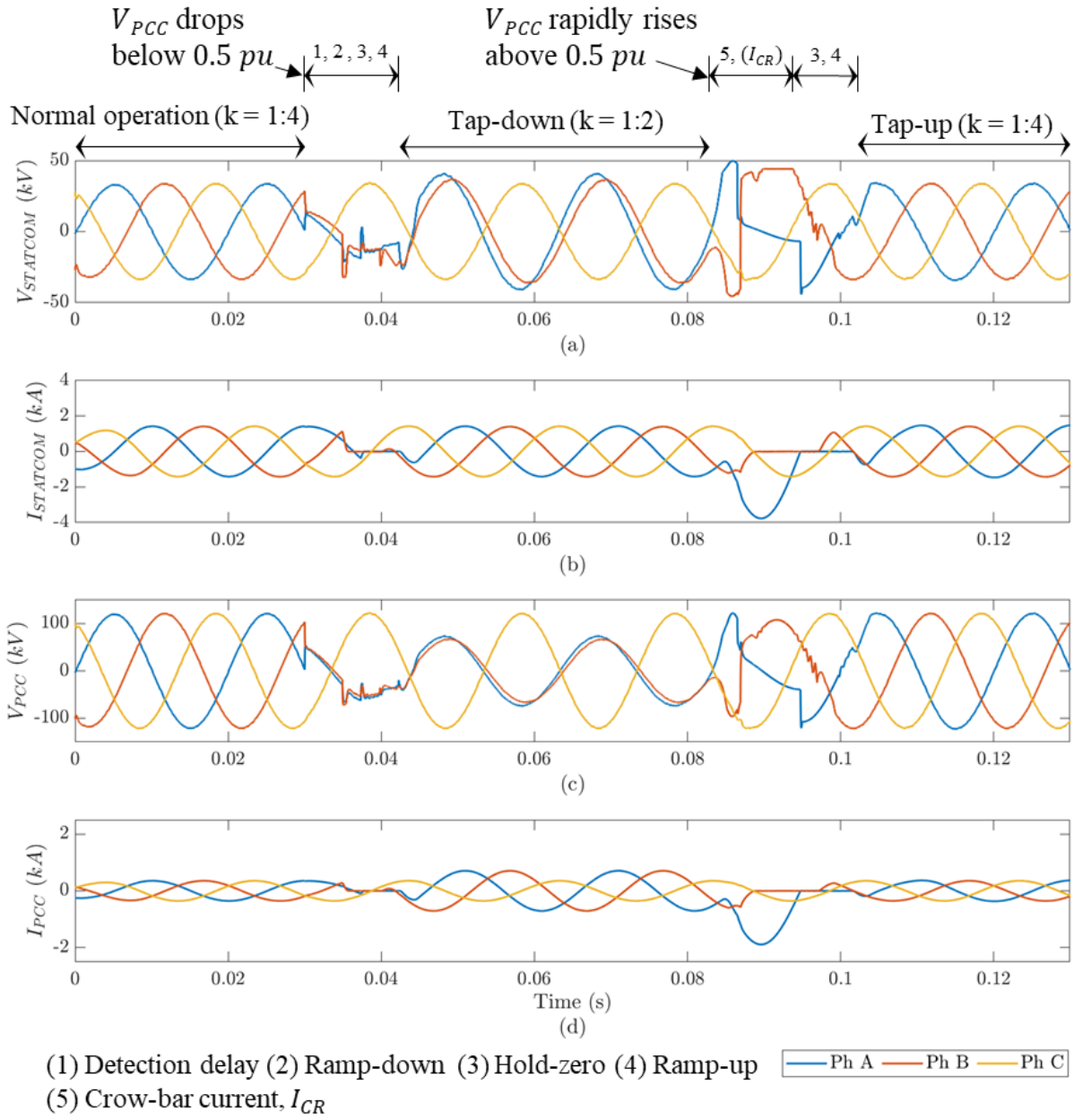


Figure 5-29: Application of line to line fault at 0.03 s showing tap-down and increase in fault current to 2 pu for Phase A and Phase B in single stage ($R_F = 1\ m\Omega$ & $G_{FL} = 1,000MVA$). L-L fault showing crow-bar current during tap-up sequence failure (a) Voltage at $B_{STATCOM}$ (b) Current $I_{STATCOM}$ (c) Voltage at B_{PCC} and (d) Current I_{PCC}.

5.5 Chapter Conclusions

The increasing penetration of IBRs has led to decreasing SCL in the network, which can impact the ability of the protection system to detect and locate faults effectively. This chapter proposed a novel method of raising fault-current during voltage dips via an electronic tap-changer fitted to the coupling transformer of an IBR. The proposed eTC uses thyristor-based switches to switch in and out large sections of winding to achieve large changes in k_T. This takes advantage of the reduced voltage ratio needed in the coupling transformer during a deep voltage dip and this creates a matching increase in the current ratio so that increased fault current can be delivered without the need to increase the rating of the semiconductors in the IBR.

The effectiveness of the proposed thyristor-based eTC switches was demonstrated for a STATCOM coupling transformer. The transformer was configured to give a turns ratio of $1:4$ in normal operation and be able to tap-down to $1:2$ or $1:1$ to increase fault current to $2\ pu$ and $4\ pu$ respectively. Fast commutation of the tap-selector thyristors can be achieved by actively controlling the current through them to zero when they need to be turned off rather than waiting for natural zero crossing of the AC sine wave. It was shown that fault current of up to 4 pu could be delivered at the PCC in less than half a cycle $(10\ ms)$ after the detection of the fault. The tap change sequence delay comprises of $10\ ms$ of detection time plus $1\ ms$ of current reduction control and $5\ ms$ of hold time to guarantee thyristor commutation. It was shown that the proposed STATCOM plus eTC is capable of delivering increased fault current during SLG, L-L and 3LG faults. For a L-L fault, the FCC magnitude is limited to $2\ pu$ current and even that is only achieved by over-rating the STATCOM by 50%.

A difficulty in commutating the thyristors was identified when the voltage recovery after fault clearance was very quick. In such a case or during a tap-up sequence failure, a crowbar circuit can be used to divert current around the IGBTs of the STATCOM. The crowbar thyristors, tap-selector thyristors and transformer windings will have to be rated to sustain that current for approximately half a cycle. The section of grid-side winding that remains in circuit during the fault is required to carry the fault current for the fault-clearance time (typically $80\ ms$), but this is a normal requirement of a transformer.

The proposed STATCOM with eTC was analysed under different conditions to assess the operation of the circuit and relative magnitude of fault current contribution from STATCOM and grid. Under the condition where the fault resistance was increased the error term in the

impedance measurement also increased. It was also concluded that the greater the difference in FCC between STATCOM and grid voltage source, larger the margin of error during impedance measurement. The STATCOM with eTC provided greater fault current and therefore reduced the error in the impedance measurement.

5.5.1 Further Work

Further work is required to assess if the speed of fault current delivery for the proposed STATCOM with eTC can be improved by changing the naturally commutating thyristors based eTC to forced commutating semiconductors (i.e. IGBT) based eTC. In the proposed STATCOM with eTC and a grounding transformer (Figure 5-17), the force commutating devices can interrupt current after the detection delay in the voltage magnitude measurement at PCC. The quicker interruption by the IGCTs/IGBTs based eTC will stop the crow-bar current from rising too high or above the rating of the equipment in the crow-bar current path. It should be noted that changing the commutation device will not impact the magnitude of fault current delivered at the PCC.

The disadvantage of using IGBTs/IGCTs would include the necessary comprehensive design of a snubber circuit to prevent voltage transient effects when interrupting high currents on the grid side. Moreover, the increased power losses and cost associated with IGCTs/IGBTs, and its snubber circuit needs to be assessed.

A robust fault classifier is also required to enable the simulation to work effectively for various values of fault impedances.

The enhancement of fault current through an electronic tap-change transformer could be extended beyond the STATCOM case investigated here to other large single converters such as HVDC converter stations and to collections of many small converters in wind farms interfaced through a single transformer.

CHAPTER 6 CONCLUSIONS

Increasing penetration of inverter-based resources (IBR) have led to decreasing Short-Circuit Level (SCL) in networks which can impact a protection system's ability to detect and locate faults effectively. Improved Fault Current Contribution (FCC) of IBRs has been identified as needed so that conventional protection systems can continue to be used as IBRs displace synchronous machines. However, as of yet, no suitable way of producing substantially increased fault current for IBR, i.e. more than $2\ pu$, has been identified other than the costly approach of overrating the switching devices. This is due to the absence of any significant short-term over-current capability in the semiconductor devices. This thesis has investigated approaches to increase FCC from IBRs at device, circuit, and system level.

In the first investigation aimed at device level, a possible way to provide short-term relief to the temperature rise problem of over-current is to place some Phase Change Material (PCM) close to the semiconductor which will limit the rate-of-rise of temperature while the phase-change occurs. This approach has been investigated in general but here it was investigated with the amplitude and duration of fault currents in mind and for the case where the PCM is placed within the heatsink rather than within the semiconductor package. PCMs take advantage of the large amount of energy that can be stored or released during a phase change process (solid to liquid or liquid to solid), which occurs at a nearly constant temperature, and can be a useful tool for thermal management. Finite Element Analysis (FEA) was used to assess various configurations of PCM placed in the heat sink between the semiconductor module baseplate and the cold plate. A metal framework, acting as a thermal conductivity enhancer (TCE), was used to ensure that a good thermal path exists through the PCM so that the whole volume of the PCM was used effectively and so that temperature rise during normal operation was not degraded too far. In the case-study with LM80 PCM (with a melting point of $80℃$), the time for which the IGBT can operate at $3\ pu$ heat loss was found to be $12.6\ s$. The duration of increased current is more than sufficient for fault current purposes but $3\ pu$ heat loss would allow less than $3\ pu$ current (because heat loss is a quadratic function of current) which is low when compared with the current available from synchronous machines during faults. A recovery period of $2\ minutes$ was required before the PCM was ready to again provide short-term over-current capability which would need to be significantly reduced for use in auto-recloser systems with possibly two fault events in less than $1\ s$.

The combination of PCM and TCE design could be re-worked for higher currents with greater volumes of PCM but the limitation on junction temperature is not the only limit affecting the ability of an IGBT to carry increased current. IGBTs have a commutation current limit which is typically less than twice the thermal current limit of the IGBT and this may well be the limiting factor. Moreover, IGBTs typically have limits placed on short-duration current pulses, typically of $1\ ms$ [11]. It was concluded that the current limitation in the semiconductor device operation meant that thermal management at semiconductor device level was not sufficient on its own for enhanced fault current purposes. If, as indicted here, device-level innovation cannot provide the fault current, then circuit level innovation is required.

The second investigation, at circuit level, features series/parallel switching of submodules (SMs) in modular converters, taking advantage of the fact that, during a fault, the line voltage is reduced. If grid voltage falls below $0.5\ pu$ then half of the SMs can be put in parallel with the other half to double the FCC without device over-current. A delta-connected chain-link STATCOM was developed, inspired by the alternate-arm converter (AAC) in which a director switch was used as part of the circuit reconfiguration. The circuit uses only half-bridge SMs (HB-SMs) since each arm of the AAC-like structure only need to produce voltage of one polarity. The series/parallel reconfiguration method was analysed to evaluate the number of additional devices needed for reconfiguration and the rating of those devices for a fault current of $2\ pu$ and $4\ pu$.

For the case of $2\ pu$ fault current, each SM stack is divided in half and the two halves placed in parallel by using the two director switches of the AAC supplemented with two additional switches. The investigation showed that the director switches and additional switches need to block a minimum of the full stack voltage. Although the additional switches and SMs carry only $1\ pu$ current when configured for fault current (parallel configuration), one of the director switches has to carry $2\ pu$ current in this configuration. This meant that the blocking voltage and forward current ratings of one director switch in each polarity is higher than they would be in a standard AAC configuration, which, together with the two additional switches, is the price paid for the reconfiguration capability.

The number of devices in the current path during normal (series) operation is also an important consideration because it influences the conduction power loss. The proposed series/parallel circuit (for 2 parallel paths) has an equal number of devices in conduction path compared to an

AAC style STATCOM without series/parallel circuit. When compared to an MMC style STATCOM there is an 50% increase.

If the proposed series/parallel system was used to generate $4\ pu$ fault current, the circuit with a $4{:}\,1$ series/parallel reconfiguration, the number of switches more than doubles (increases by 125%) when compared to the circuit with a $2{:}\,1$ ratio circuit. As the circuit reconfiguration ratio increases, the total number of switches and the current rating of two director switches in each phase increases. Because a fault response is required from an IBR for only a small number of times in a year, this increase in number of switches which is present all the time makes this circuit unattractive. Penalties in power loss, and device-count and rating mean that this circuit reconfiguration may be tolerable for $2\ pu$ current ($2{:}\,1$ ratio parrel-series reconfiguration) but not at $4\ pu$ current ($4{:}\,1$ ratio parallel-series reconfiguration) or higher.

In the system level investigation, a method of raising fault-current during voltage dips via an electronic tap-changer (eTC) fitted to the coupling transformer of an IBR was proposed. The proposed eTC uses thyristor switches to connect or disconnect large sections of winding to achieve large changes in turns-ratio. This takes advantage of the reduced voltage ratio needed in the transformer during a deep voltage dip to increase the current ratio so that increased fault current can be delivered without the need to increase the rating of the semiconductors in the IBR.

The effectiveness of the proposed thyristor-based eTC switches was demonstrated for a STATCOM coupling transformer. The transformer was configured to give a turns ratio of $1{:}\,4$ in normal operation and be able to tap-down to $1{:}\,2$ or $1{:}\,1$ to increase fault current to $2\ pu$ and $4\ pu$ respectively. To do this, the grid-side winding was divided into four equal sections.

Fault current of $4\ pu$ could be provided in less than half a cycle ($10\ ms$) from fault detection for voltage dips below retained voltage of $0.25\ pu$. The depth of voltage dip resulting from the fault determines how far voltage can be traded for current using the tap-change transformer such that if the retained voltage is between $0.5\ pu$ and $0.25\ pu$ then only $2\ pu$ fault current is provided. In all cases, the current delivered by the STATCOM circuit that flows in the STATCOM-side of the transformer remains at $1\ pu$. A greater number of choices of fault current for finer choices of voltage dip could be created by providing more taps in the transformer winding and more thyristor switches.

Fast commutation of the tap-selector thyristors can be achieved by actively controlling the current through them to zero when they need to be turned off. Thyristors had been chosen for this role because of their low conduction losses. For simplicity in the initial study, the STATCOM circuit chosen was the Single Star Bridge Cells (SSBC) circuit coupled with star-star transformer. This allowed independent operation of each phase during asymmetric faults. The STATCOM control was in phase coordinates with proportional-plus-resonant (P+R) controllers.

A difficulty in commutating the thyristors was identified when there was a rapid voltage recovery after fault clearance. It takes time to detect the voltage recovery, to determine that a tap-change should happen and to control the current to zero. If the PCC voltage when referred to the STATCOM exceeds the maximum voltage available from the STACOM then control of the current is not possible and the thyristor will not commutate off until the next natural zero-crossing of current. In such a case, the recovering PCC voltage will drive excessive current through the STATCOM via its internal diodes. To avoid that, it is proposed to use further thyristors as a crowbar circuit to divert current away from the IGBTs of the STATCOM. The crow-bar thyristors, tap-selector thyristors and transformer windings will have to be rated to sustain that current for approximately half a cycle. The magnitude of the current depends on several factors: the combined impedance of the STATCOM reactor, transformer, transmission line and grid; the rate-of-rise of PCC voltage and the point-on-wave of the fault clearance. The section of grid-side winding that remains in circuit during the fault is required to carry the fault current for fault-clearance time (typically $80\,ms$). It is expected that this will be within the normal short-term rating of the winding in terms of thermal loading but this and the mechanical strength to withstand the forces on the conductors would need to be ensured.

The independent control of each phase of the STATCOM and the star-star coupling transfer were demonstrated to work effectively with single-phase-to-ground (SLG) faults and three-phase-to-ground (3LG) faults. A line-to-line (L-L) fault raises a problem which is that the retained voltage on the faulted phases does not experience a deep dip that would allow the tap-changer to trade voltage for current. At best, for a close-up zero-resistance L-L fault, the retained voltage drops to only $0.577\,pu$. But if the voltage rating of the STATCOM is set at 50% above the nominal voltage to provide a large headroom for control action, then the proposed STATCOM can deliver $2\,pu$ fault current.

6.1 Future Work

This section will suggest areas relating to this thesis which merit further investigation.

Further work could focus on the development of lab-scale prototypes for thermal management of IGBT using PCM. This will assist in further validating the results shown in this thesis. In particular, the ability to inject substantial fault current (more than $2\ pu$) without damaging the device and return to normal operation can be investigated.

In the tap-change fault current enhancement case, the investigation reported in the thesis covered symmetric (3LG) and some asymmetric faults (SLG and L-L) and it is suggested that further work should consider other types of faults, such as three phase faults not involving ground (3L), two-phase-to-ground fault (2LG) and open-circuit faults [13]. Further work is also needed to determine the influence the tap-change sequence, for different types of faults under a range of conditions, has on SM capacitor sizing and SM voltage balancing. A cost-comparison for replacement of tap-selector thyristors with GTO thyristors or IGCT that can be force commutated should be considered. This comparison will enable designers to make the decision to keep or remove the crow-bar circuit and the influence of that on thermal and current up-rating of the transformer windings to cope with rapid rise of PCC voltage.

More generally, this thesis has shown that substantial fault current can be injected from IBR systems through thermal management of semiconductors devices and by designing transformers with tap-change capabilities in IBR systems. The two concepts could be combined in an IBR system and could be taken further and considered for a variety of converter topologies beyond the STATCOM example used. More research into the potential negative implications of this hybrid approach should also be considered, such as the increased cost of converter and of transformer maintenance, and the effect on reliability.

Furthermore, the adoption of wide band-gap semiconductors could be considered because of their higher operating temperatures and high voltage capabilities, although recognising that at present they are not offered in current ratings compatible with transmission systems.

REFERENCE

[1] European Commission, “Roadmap 2050,” Luxembourg, 2012. doi: 10.2833/10759.

[2] Committee on Climate Change, “The Sixth Carbon Budget: The UK’s path to Net Zero,” *Carbon Budg.*, no. December, p. 448, 2020, [Online]. Available: https://www.theccc.org.uk/publication/sixth-carbon-budget/.

[3] National Grid, “Future Energy Scenarios (FES) 2019,” *2019*. http://fes.nationalgrid.com/.

[4] National Grid Electricity System Operator, “Future Energy Scenario 2022,” 2022. [Online]. Available: https://www.nationalgrideso.com/document/263951/download.

[5] K. N. Bangash, M. E. A. Farrag, and A. H. Osman, “Impact of energy storage systems on the management of fault current at LV network with high penetration of distributed generation,” *Int. J. Smart Grid Clean Energy*, vol. 6, no. 3, pp. 195–206, 2017, doi: 10.12720/sgce.6.3.195-206.

[6] A. Z. Adnan, M. E. Yusoff, and H. Hashim, “Analysis on the impact of renewable energy to power system fault level,” *Indones. J. Electr. Eng. Comput. Sci.*, vol. 11, no. 2, pp. 652–657, 2018, doi: 10.11591/ijeecs.v11.i2.pp652-657.

[7] National Grid, “SOF18 Whole system short circuit levels,” 2019.

[8] B. Kasztenny, “Line Distance Protection Near Unconventional Energy Sources,” 2022, [Online]. Available: https://selinc.com.

[9] National Grid, “SOF 18 Impact of Declining Short Circuit Level (SCL),” 2019.

[10] “Migrate 2020.” https://www.h2020-migrate.eu/about.html.

[11] Several, “Pro-Smart Consortium.” https://www.ntnu.edu/prosmart/home (accessed May 17, 2021).

[12] G. R. Jenkins and V. Hamidi, “Assessment of Fault Ride Through Requirement for Distributed Generators,” in *3rd Renewable Power Generation Conference (RPG 2014)*, 2014, pp. 1–4, doi: 10.1049/cp.2014.0870.

[13] B. M. Weedy and B. J. Cory, *Electric power systems*, 5th Editio. Wiley IEEE Press, 2016.

[14] K. Jia, Z. Yang, Y. Fang, and T. Bi, "Impact of Inverter-Interfaced Renewable Energy Generators on Distance Protection and an Improved Scheme," *IEEE Trans. Power Electron.*, vol. 34, no. 12, pp. 11843–11855, 2019, doi: 10.1109/TPEL.2019.2904715.

[15] A. Kazerooni, S. Jupe, J. Berry, N. Murdoch, and P. Brinckerhoff -Uk, "Sensitivity analysis of fault level assessments in HV networks," *Cired Work. - Rome*, no. 0200, pp. 1-5, 2014, [Online]. Available: http://www.cired.net/publications/workshop2014/papers/CIRED2014WS_0200_final.pdf.

[16] S. Gordon, Q. Hong, and K. Bell, "Implications of Reduced Fault Level and its Relationship to System Strength: A Scotland Case Study," pp. 1–10, 2022.

[17] "PowerFul CB." http://innovation.ukpowernetworks.co.uk/innovation/en/Projects/tier-2-projects/powerful-cb/.

[18] W. Shao *et al.*, "Power Module with Large Short Term Current Capability by Using Phase Change Material," *2018 1st Work. Wide Bandgap Power Devices Appl. Asia, WiPDA Asia 2018*, vol. 2019, no. Acdc 2018, pp. 305–310, 2018, doi: 10.1109/WiPDAAsia.2018.8734577.

[19] S. K. Ma, H. Geng, L. Liu, G. Yang, and B. C. Pal, "Grid-synchronization stability improvement of large scale wind farm during severe grid fault," *IEEE Trans. Power Syst.*, vol. 33, no. 1, pp. 216–226, 2018, doi: 10.1109/TPWRS.2017.2700050.

[20] L. Roberts, A. Champneys, K. Bell, and M. di Bernardo, "An algebraic metric for parametric stability analysis of power systems," pp. 1–11, 2015, [Online]. Available: http://arxiv.org/abs/1503.07914.

[21] European Network of Transmission System Operators for Electricity (ENTSO-E), "Determining generator fault clearing time for the synchronous zone of Continental Europe," 2017. [Online]. Available: https://www.entsoe.eu/Documents/SOC documents/Regional_Groups_Continental_Europe/2017/SPD_FCT-BestPractices_website.pdf.

[22] National Grid Electricity System Operator Limited, *The Grid Code*, no. 6. United Kingdom, 2022, p. 606.

[23] S. Zubic, Z. Gajic, and D. Kralj, "Line Protection Operate Time: How Fast Shall It Be?," *IEEE Access*, vol. 9, pp. 75608–75616, 2021, doi: 10.1109/ACCESS.2021.3081993.

[24] Schneider Electric, *Signalling and Intertripping in Protection Schemes*. United Kingdom: https://www.se.com/ww/en/tools/npag-online-re14y/pdf/D2-Signalling_and_Intertripping_in_Protection_Schemes.pdf.

[25] B. Kasztenny and D. Finney, *Fundamentals of distance protection*. 2008.

[26] F. Calero, A. Guzman, and G. Benmouyal, "Adaptive Phase and Ground Quadrilateral Distance Elements," *J. Reliab. Power*, vol. 1, no. 1, pp. 65–82, 2009, [Online]. Available: papers2://publication/uuid/2C99679F-A380-48E7-A9FC-C2A59550CD78.

[27] E. O. Schweitzer and B. Kasztenny, "Distance protection: Why have we started with a circle, does it matter, and what else is out there?," *71st Annu. Conf. Prot. Relay Eng. CPRE 2018*, vol. 2018-Janua, pp. 1–19, 2018, doi: 10.1109/CPRE.2018.8349791.

[28] L. He, C. C. Liu, A. Pitto, and D. Cirio, "Distance protection of AC grid with HVDC-connected offshore wind generators," *IEEE Trans. Power Deliv.*, vol. 29, no. 2, pp. 493–501, 2014, doi: 10.1109/TPWRD.2013.2271761.

[29] C. Brantl, P. Ruffing, and R. Puffer, "The application of line protection relays in high voltage AC transmission grids considering the capabilities and limitations of connected MMCS," *IET Conf. Publ.*, vol. 2020, no. CP771, pp. 1–6, 2020, doi: 10.1049/cp.2020.0062.

[30] A. Hooshyar, M. A. Azzouz, and E. F. El-Saadany, "Distance Protection of Lines Emanating from Full-Scale Converter-Interfaced Renewable Energy Power Plants-Part II: Solution Description and Evaluation," *IEEE Trans. Power Deliv.*, vol. 30, no. 4, pp. 1781–1791, 2015, doi: 10.1109/TPWRD.2014.2369480.

[31] D. López *et al.*, "Negative sequence current injection by power electronics based generators and its impact on faulted phase selection algorithms of distance protection," *Wprc 2018*, no. August, pp. 1–18, 2018.

[32] A. Banaiemoqadam, A. Hooshyar, and M. A. Azzouz, “A Control-Based Solution for Distance Protection of Lines Connected to Converter-Interfaced Sources during Asymmetrical Faults,” *IEEE Trans. Power Deliv.*, vol. 35, no. 3, pp. 1455–1466, 2020, doi: 10.1109/TPWRD.2019.2946757.

[33] Paul Daniel Judge, “Power Converter Design for HVDC Applications - PhD Thesis,” Imperial College, 2016.

[34] D. D. Fentie, “Understanding the dynamic mho distance characteristic,” *69th Annu. Conf. Prot. Relay Eng. CPRE 2016*, 2017, doi: 10.1109/CPRE.2016.7914922.

[35] F. Calero, A. Guzman, and G. Benmouyal, “Adaptive Phase and Ground Quadrilateral Distance Elements,” *J. Reliab. Power*, vol. 1, no. 1, pp. 65–82, 2009.

[36] U. J. Patel, N. G. Chothani, and P. J. Bhatt, “Adaptive quadrilateral distance relaying scheme for fault impedance compensation,” *Electr. Control Commun. Eng.*, vol. 14, no. 1, pp. 58–70, 2018, doi: 10.2478/ecce-2018-0007.

[37] P. K. Nayak, A. K. Pradhan, and P. Bajpai, “A Three-Terminal Line Protection Scheme Immune to Power Swing,” *IEEE Trans. Power Deliv.*, vol. 31, no. 3, pp. 999–1006, 2016, doi: 10.1109/TPWRD.2014.2387873.

[38] V. K. Gaur, B. R. Bhalja, and M. Kezunovic, “Novel fault distance estimation method for three-terminal transmission line,” *IEEE Trans. Power Deliv.*, vol. 36, no. 1, pp. 406–417, 2021, doi: 10.1109/TPWRD.2020.2984255.

[39] S. Paladhi, Q. Hong, and C. D. Booth, “Adaptive Distance Protection for Multi-terminal lines connecting Conveter-Interfaced Renewable Energy Sources,” pp. 1–5.

[40] S. Sarangi and A. K. Pradhan, “Adaptive Direct Underreaching Transfer Trip Protection Scheme for the Three-Terminal Line,” *IEEE Trans. Power Deliv.*, vol. 30, no. 6, pp. 2383–2391, 2015, doi: 10.1109/TPWRD.2015.2388798.

[41] and T. G. S. Yang, Y. Li, Y. Zhu, W. Xiang, H. Zhang, J. Wen, “An enhanced distance protection scheme bene ting from negative-sequence fault current behaviors of ibrs under asymmetric faults (unpublished).”

[42] National Grid, “Virtual Synchronous Machines,” 2018. https://www.nationalgrideso.com/document/103716/download.

[43] M. Alahmad and F. A. El-Aleem, “Heat Transfer Challenges in Semiconductors Processing and the Applications of Heat Pipes for Efficient Heat Removal,” *J. King Saud Univ. - Eng. Sci.*, vol. 15, no. 1, pp. 141–154, 2003, doi: 10.1016/S1018-3639(18)30767-0.

[44] A. Castelan, B. Cougo, J. Brandelero, D. Flumian, and T. Meynard, “Optimization of forced-air cooling system for accurate design of power converters,” *IEEE Int. Symp. Ind. Electron.*, vol. 2015-Septe, pp. 367–372, 2015, doi: 10.1109/ISIE.2015.7281496.

[45] J. S. Kwak, C. K. Kim, and B. E. Koh, “Cooling system of Haenam-Jeju HVDC system,” *IEEE Int. Symp. Ind. Electron.*, vol. 2, pp. 1000–1005, 2001.

[46] T. Bayliss *et al.*, “Development of a modular cooling solution for STATCOM and HVDC transmission schemes,” *IET Conf. Publ.*, vol. 2017, no. CP709, pp. 1–5, 2017, doi: 10.1049/cp.2017.0072.

[47] G. Sheng-Li, L. Ming-Quan, X. Xuzheng, W. Yu-Liang, L. Zhi-Dao, and W. Guang-Wu, “Exploratory research on the cooling mode of offshore wind power converter substation,” *China Int. Conf. Electr. Distrib. CICED*, vol. 2021-April, no. 202005310000061, pp. 168–174, 2021, doi: 10.1109/CICED50259.2021.9556656.

[48] S. Fang, W. Luo, H. Wang, and H. Hu, “Operational performance of the valve cooling system in Guangzhou converter station,” *IET Semin. Dig.*, vol. 2015, no. CP654, pp. 1–5, 2015, doi: 10.1049/cp.2015.0092.

[49] Y. Du and Y. Ding, “Chemical Engineering and Processing : Process Intensi fi cation Towards improving charge / discharge rate of latent heat thermal energy storage (LHTES) by embedding metal foams in phase change materials (PCMs),” *Chem. Eng. Process. Process Intensif.*, vol. 108, pp. 181–188, 2016, doi: 10.1016/j.cep.2016.08.003.

[50] Y. Zhao, S. Thapa, L. Weiss, and Y. Lvov, “Phase change insulation for energy efficiency based on wax-halloysite composites,” *IOP Conf. Ser. Mater. Sci. Eng.*, vol. 64, no. 1, 2014, doi: 10.1088/1757-899X/64/1/012045.

[51] NCT Advance Cooling Technologies, “PCM Types Comparison,” 2019. https://www.1-act.com/products/pcm-heat-sinks.

[52] A. A. A. Abuelnuor, I. H. I. Alhag, A. A. M. Omara, M. K. Awad, and M. H. Mohammed, “Buildings cooling: An experimental study of Phase Change Materials storage for low energy buildings,” *Proc. - 2017 Int. Conf. Commun. Control. Comput. Electron. Eng. ICCCCEE 2017*, pp. 1–5, 2017, doi: 10.1109/ICCCCEE.2017.7867680.

[53] S. C. Fok, W. Shen, and F. L. Tan, “Cooling of portable hand-held electronic devices using phase change materials in finned heat sinks,” *Int. J. Therm. Sci.*, vol. 49, no. 1, pp. 109–117, 2010, doi: 10.1016/j.ijthermalsci.2009.06.011.

[54] Z. Yan, G. Liu, J. M. Khan, and A. A. Balandin, “Graphene quilts for thermal management of high-power GaN transistors,” *Nat. Commun.*, vol. 3, no. May, pp. 827–828, 2012, doi: 10.1038/ncomms1828.

[55] F. Volle, S. V. Garimella, and M. A. Juds, “Thermal management of a soft starter: Transient thermal impedance model and performance enhancements using phase change materials,” *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1395–1405, 2010, doi: 10.1109/TPEL.2010.2040632.

[56] A. Hussain, I. H. Abidi, C. Y. Tso, K. C. Chan, Z. Luo, and C. Y. H. Chao, “Thermal management of lithium ion batteries using graphene coated nickel foam saturated with phase change materials,” *Int. J. Therm. Sci.*, vol. 124, no. May 2017, pp. 23–35, 2018, doi: 10.1016/j.ijthermalsci.2017.09.019.

[57] K. Du, J. Calautit, Z. Wang, Y. Wu, and H. Liu, “A review of the applications of phase change materials in cooling , heating and power generation in di ff erent temperature ranges,” *Appl. Energy*, vol. 220, no. October 2017, pp. 242–273, 2018, doi: 10.1016/j.apenergy.2018.03.005.

[58] S. Krishnan and S. V. Garimella, “Analysis of a phase change energy storage system for pulsed power dissipation,” *IEEE Trans. Components Packag. Technol.*, vol. 27, no. 1, pp. 191–199, 2004, doi: 10.1109/TCAPT.2004.825758.

[59] J. Leland and G. Recktenwald, “Optimization of a phase change heat sink for extreme environments,” *Annu. IEEE Semicond. Therm. Meas. Manag. Symp.*, pp. 351–356, 2003, doi: 10.1109/stherm.2003.1194384.

[60] S. Krishnan, S. V Garimella, and S. S. Kang, “Materials for Transient Thermal Management of Electronics,” *IEEE Trans. Components Packag. Technol.*, vol. 28, no. 2, pp. 281–289, 2005.

[61] B. Liu and P. Majumdar, “Numerical simulation of phase change heat transfer in PCM-encapsulated heat sinks,” *Thermomechanical Phenom. Electron. Syst. -Proceedings Intersoc. Conf.*, vol. 2006, pp. 345–355, 2006, doi: 10.1109/ITHERM.2006.1645363.

[62] E. M. Alawadhi and C. H. Amon, “Thermal analyses of a PCM thermal control unit for portable electronic devices: Experimental and numerical studies,” *Intersoc. Conf. Therm. Thermomechanical Phenom. Electron. Syst. ITHERM*, vol. 2002-Janua, no. 1, pp. 466–475, 2002, doi: 10.1109/ITHERM.2002.1012493.

[63] N. Zheng and R. A. Wirtz, “A hybrid thermal energy storage device, part 1: Design methodology,” *J. Electron. Packag. Trans. ASME*, vol. 126, no. 1, pp. 1–7, 2004, doi: 10.1115/1.1646419.

[64] L. Huang, M. Petermann, and C. Doetsch, “Evaluation of paraffin/water emulsion as a phase change slurry for cooling applications,” *Energy*, vol. 34, no. 9, pp. 1145–1155, 2009, doi: 10.1016/j.energy.2009.03.016.

[65] D. Yoo and Y. Joshi, “Energy efficient thermal management of electronic components using solid liquid phase change materials,” *Intersoc. Conf. Therm. Thermomechanical Phenom. Electron. Syst. ITHERM*, vol. 2002-Janua, no. 4, pp. 800–807, 2002, doi: 10.1109/ITHERM.2002.1012536.

[66] A. Stupar, U. Drofenik, and J. W. Kolar, “Optimization of phase change material heat sinks for low duty cycle high peak load power supplies,” *IEEE Trans. Components, Packag. Manuf. Technol.*, vol. 2, no. 1, pp. 102–115, 2012, doi: 10.1109/TCPMT.2011.2168957.

[67] V. Shanmugasundaram, J. R. Brown, and K. L. Yerkes, “Thermal management of high heat-flux sources using phase change materials: A design optimization procedure,” *32nd Thermophys. Conf.*, 1997, doi: 10.2514/6.1997-2451.

[68] S. Varanasi, “Analysis and Topology Optimization of Heat Sinks with a Phase- Change Material on COMSOL Multiphysics ™ Platform Analysis and Topology Optimization of Heat Sinks with a Phase- Change Material on COMSOL Multiphysics ™ Platform,”

no. December, 2014, [Online]. Available: https://www.researchgate.net/profile/G_Ananthasuresh/publication/267679913.

[69] G. Kumar, Abhay; Weimin, Ma; Ruifeng, "Three Gorges - Shanghai HVDC : Reinforcing Interconnection between Central and East China," 2006.

[70] S. Mian, P. Judge, A. Junyent-Ferre, and T. Green, "A Delta-Connected Modular Multilevel STATCOM with Partially-Rated Energy Storage for Provision of Ancillary Services," *IEEE Trans. Power Deliv.*, vol. 8977, no. c, pp. 1–1, 2020, doi: 10.1109/tpwrd.2020.3029312.

[71] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," *2003 IEEE Bol. PowerTech - Conf. Proc.*, vol. 3, pp. 6–11, 2003, doi: 10.1109/PTC.2003.1304403.

[72] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 37–53, 2015, doi: 10.1109/TPEL.2014.2309937.

[73] X. Xiang, "The Modular Multilevel DC Converters for MVDC and HVDC Applications," 2019.

[74] K. Ilves, A. Antonopoulos, L. Harnefors, S. Norrga, and H. Nee, "Circulating Current Control in Modular Multilevel Converters with Fundamental Switching Frequency," 2012.

[75] R. Zeng, L. Xu, L. Yao, and B. W. Williams, "Design and operation of a hybrid modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1137–1146, 2014, doi: 10.1109/TPEL.2014.2320822.

[76] P. D. Judge, G. Chaffey, M. M. C. Merlin, P. R. Clemow, and T. C. Green, "Dimensioning and modulation index selection for the hybrid modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 3837–3851, 2018, doi: 10.1109/TPEL.2017.2719103.

[77] M. M. C. Merlin *et al.*, "The Alternate Arm Converter : A New Hybrid Multilevel Converter With DC-Fault Blocking Capability," *IEEE Trans. Power Deliv.*, vol. 29, no. 1, pp. 310–317, 2014, doi: 10.1109/TPWRD.2013.2282171.

[78] G. P. Adam, K. H. Ahmed, S. J. Finney, K. Bell, and B. W. Williams, "New breed of network fault-tolerant voltage-source-converter HVDC transmission system," *IEEE Trans. Power Syst.*, vol. 28, no. 1, pp. 335–345, 2013, doi: 10.1109/TPWRS.2012.2199337.

[79] M. M. C. Merlin *et al.*, "The Extended Overlap Alternate Arm Converter: A Voltage Source Converter with DC Fault Ride-Through Capability and a Compact Design," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 3898–3910, 2017, doi: 10.1109/TPEL.2017.2723948.

[80] C. T. Collins, S. Member, T. C. Green, and S. Member, "Comparative Analysis of an MV Neutral Point Clamped AC-CHB Converter With DC Fault Ride-Through Capability," *IEEE Trans. Ind. Electron.*, vol. 67, no. 4, pp. 2834–2843, 2020, doi: 10.1109/TIE.2019.2907511.

[81] J. Faiz and B. Siahkolah, "New Solid-State Onload Tap-Changers Topology for Distribution Transformer," *IEEE Trans. Power Deliv.*, vol. 18, no. 1, 2003.

[82] C. A. Plet, "Fault Response of Inverter Based Distributed Generation," Imperial College, 2011.

[83] National Grid UK, *Automatic Tap Change Control, National Grid Technical Specification NGTS 3.24.61, UK*. United Kingdom, 2000.

[84] D. J. Rogers, "Hybrid and Thin Power Electronics for Electrical Power Networks," Imperial College London.

[85] J. Faiz and B. Siahkolah, "Differences between conventional and electronic tap-changers and modifications of controller," *IEEE Trans. Power Deliv.*, vol. 21, no. 3, pp. 1342–1349, 2006, doi: 10.1109/TPWRD.2005.861323.

[86] D. J. Rogers and T. C. Green, "An active-shunt diverter for onload tap changers," *IEEE Trans. Power Deliv.*, vol. 28, no. 2, pp. 649-657, 2013, doi: 10.1109/TPWRD.2013.2243171.

[87] G. H. Cooke and K. T. Williams, "Thyristor assisted on-load tap changers for transformers," *IEE Conf. Publ.*, no. 324, pp. 127–131, 1990.

[88] A. Torrey, C. Degeneff, K. Schaeffer, and H. Frazer, “a New Approach To Solid-State on Load Tap,” vol. 13, no. 3, pp. 952–961, 1998.

[89] P. Bauer and S. W. H. de Haan, “Electronic tap changer for 500 kVA/10 kV distribution transformers: Design, experimental results and impact in distribution networks,” *Conf. Rec. - IAS Annu. Meet. (IEEE Ind. Appl. Soc.*, vol. 2, no. Mv, pp. 1530–1537, 1998, doi: 10.1109/ias.1998.730344.

[90] R. Fourie and H. Du, “Development of a MV IGBT based solid-state tap changer,” *IEEE AFRICON Conf.*, no. September, pp. 1–6, 2009, doi: 10.1109/AFRCON.2009.5308128.

[91] B. Faiz, Jawad; Siahkolah, *Electronic Tap-changer for Distribution Transformers*. Springer Heidelberg, Germany, 2011.

[92] R. Kabiri, D. G. Holmes, B. P. McGrath, and L. G. Meegahapola, “LV Grid Voltage Regulation Using Transformer Electronic Tap Changing, with PV Inverter Reactive Power Injection,” *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 3, no. 4, pp. 1182–1192, 2015, doi: 10.1109/JESTPE.2015.2443839.

[93] IEEE/IEC International Standard, *TAP-changers --Part 2: Application guidelines*. 2019, p. 17.

[94] ABB, “ABB Hi-Pak IGBT 5SNA 1200E330100,” Datasheet-5SNA 1200E330100, 2016. [Online]. Available: https://search.abb.com/library/Download.aspx?DocumentID=5SYA1563-03&LanguageCode=en&DocumentPartId=&Action=Launch.

[95] “ABB Semis Plecs Software,” 2019. https://new.abb.com/semiconductors/semis.

[96] N. Dukhan and S. Bodke, “An improved PCM heat storage technology utilizing metal foam,” *2010 12th IEEE Intersoc. Conf. Therm. Thermomechanical Phenom. Electron. Syst. ITherm 2010*, pp. 1–7, 2010, doi: 10.1109/ITHERM.2010.5501364.

[97] D. Li, X. Li, F. Qi, M. Packwood, and H. Luo, “Thermal Networks Generation and Application in IGBT Module Packaging,” *2018 19th Int. Conf. Electron. Packag. Technol.*, pp. 23–26, 2018.

[98] Mitsubishi Electric, “IGBT Modules Application Note 12NF 24NF 24A series,” Japan, 2014. [Online]. Available: https://www.mitsubishielectric.com/semiconductors/files/manuals/igbt_note_e.pdf.

[99] U. Drofenik, D. Cottet, A. Müsing, J.-M. Meyer, and J. W. Kolar, “Modelling the thermal coupling between internal power semiconductor dies of a water-cooled 3300V/1200A HiPak IGBT module,” *Proc. Conf. Power Electron. Intell. Motion, Power Qual. (PCIM 2007), Nuremberg, Ger. May*, no. Iii, pp. 22–24, 2007.

[100] Ansys, “Ansys Website,” *R19.1 Help*, 2019. www.ansys.com.

[101] M. Sosnowski, J. Krzywanski, K. Grabowska, and R. Gnatowska, “Polyhedral meshing in numerical analysis of conjugate heat transfer,” *EPJ Web Conf.*, vol. 180, pp. 4–9, 2018, doi: 10.1051/epjconf/201817002096.

[102] R. Li, C. Booth, A. Dyśko, A. Roscoe, H. Urdal, and J. Zhu, “Protection challenges in future converter dominated power systems,” *Int. Conf. Renew. Power Gener. (RPG 2015)*, pp. 1–6, 2015, doi: 10.1049/cp.2015.0392.

[103] T. A. Short, *Electric Power Distribution Handbook*, no. C. Boca Raton: CRC PRESS, USA, 2004.

[104] Prof Barry Wayne Williams, “Principles and Elements of Power Electronics,” in *Principles and Elements of Power Electronics*, Glasgow: Professor of Electrical Engineering, University of Strathclyde Glasgow, 2006.

[105] S. Hänninen and M. Lehtonen, “Characteristics of earth faults in electrical distribution networks with high impedance earthing,” *Electr. Power Syst. Res.*, vol. 44, no. 3, pp. 155–161, 1998, doi: 10.1016/s0378-7796(97)01193-0.

[106] A. Stiger, R. A. Rivas, and M. Halonen, “Synchronous Condensers Contribution to Inertia and Short Circuit Current in Cooperation with STATCOM,” *2019 IEEE PES GTD Gd. Int. Conf. Expo. Asia, GTD Asia 2019*, pp. 955–959, 2019, doi: 10.1109/GTDAsia.2019.8715893.

[107] and S. E. Z. Edmund O. Schweitzer, III, Ph.D., “Introduction To Symmetrical Components,” 2011.

[108] F. O. Igbinovia, G. Fandi, Z. Muller, and J. Tlusty, “Reputation of the Synchronous Condenser Technology in Modern Power Grid,” *2018 Int. Conf. Power Syst. Technol. POWERCON 2018 - Proc.*, no. 201805280000151, pp. 2108–2115, 2019, doi: 10.1109/POWERCON.2018.8601540.

[109] CIGRE Study Committee B5 Colloquium, “Application of synchronous compensators in the GB transmission network to address protection challenges from increasing renewable generation,” in *2017 CIGRE B5 Colloquium - Auckland, New Zealand Duration: 11 Sep 2017 → 15 Sep 2017*, 2017, no. 210, [Online]. Available: https://pureportal.strath.ac.uk/en/publications/application-of-synchronous-compensators-in-the-gb-transmission-ne.

[110] James H. Harlow, *Electric Power Transformer Engineering*. Boca Raton: © 2004 by CRC Press LLC, 2007.

[111] C. A. Plet, M. Graovac, T. C. Green, and R. Iravani, “Fault response of grid-connected inverter dominated networks,” *IEEE PES Gen. Meet. PES 2010*, pp. 1–7, 2010, doi: 10.1109/PES.2010.5589981.

[112] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, “Overview of control and grid synchronization for distributed power generation systems,” *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1398–1409, 2006, doi: 10.1109/TIE.2006.881997.

[113] Y. Li, A. Junyent-Ferré, and J. M. Rodriguez-Bernuz, “A Three-Phase Active Rectifier Topology for Bipolar DC Distribution,” *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1063–1074, 2018, doi: 10.1109/TPEL.2017.2681740.

[114] T.-K. Vu and S.-J. Seong, “Comparison of PI and PR Controller Based Current Control Schemes for Single-Phase Grid-Connected PV Inverter,” *J. Korea Acad. Coop. Soc.*, vol. 11, no. 8, pp. 2968–2974, 2010, doi: 10.5762/kais.2010.11.8.2968.

Appendix A STATCOM Phase Reactor Sizing

The STATCOM's average apparent power (S) rating is estimated at approximately 60 MVA.

$$S_{3ph} = \sqrt{3} * V_{LL} * I_{rms} = \sqrt{3} * 33\ kV * 1000 \approx 57.2\ MVA \quad \textbf{(A.1)}$$

The STATCOM is connected to the grid via a transformer and a phase reactor. The transformer voltage at the primary winding is 132 kV and is 33kV at the secondary winding. The size of the phase reactor is calculated using Ohm's law and inductive reactance equation (A.2). A voltage drop of ~10% across the inductance was considered, per industry practice.

$$L = \frac{V_{sec}^2}{S_{STATCOM_rating}} \frac{X_L}{2\pi f} \quad \textbf{(A.2)}$$

Where,

V_{sec} = transformer secondary voltage,

$S_{STATCOM_rating}$ = STATCOM rated apparent power,

f = system frequency, at 50 Hz

X_L = inductive reactance, at 0.1 pu

L = [H],

By solving the equation (A.2)A.2),

$$L \approx 6\ mH \quad \textbf{(A.3)}$$

Appendix B Transformer Winding Impedances Calculations

B.1 UKPN information on transformer impedance values

Impedance values for a transformer with two windings of similar power and voltage rating to the one required in this study of a STATCOM coupling transformer have been obtained from UK Power Networks (UKPN) from one of its recent installations. UKPN is the Distribution Network Operator (DNO) for London and South East England. This information has been received via private correspondence.

The following parameters were obtained and will be used as a reference in this study:

- Transformer type: Two windings transformer
    - Power Rating: $90MVA$
    - Voltage: $132kV/33kV$
- Impedance Values:
    - Positive Sequence winding reactance $X_1 = 0.1292pu$
    - Positive Sequence winding resistance $R_1 = 0.0063pu$

In this simulation the transformer with vector connection $Yy0$ has been considered. The impedance values given are for a two-winding transformer; and it is assumed that the reactance and resistance values, in pu, for convenience is split equally between the two windings. The reactance of both windings is taken as $0.065pu$ $(= 0.1292/2)$, and the resistance of both windings as $0.0032pu$ $(= 0.0063/2)$. The assumption here is that current density remains same for primary and secondary winding. So, to maintain current density, the cross area of the conductor is reduced on the primary side to reflect the drop of current carrying capacity by a quarter. Also, the length of conductor on primary side is four times the secondary side to maintain 4: 1 winding turn ratio. The value of R will change accordingly on secondary winding for I^2R losses to be same on MV and HV winding.

$$R = \rho \frac{l}{A} \quad \textbf{(B.1)}$$

B.2 Methodology for calculating the impedance of the coupling transformer

The following steps have been considered to calculate resistance and leakage reactance of the two-winding transformer.

Step 1

In a 2-winding step-up $Yy0$ transformer where the HV side is wye-connected and the MV side is wye-connected, and it is rated at $60\ MVA$. It is assumed that STATCOM side winding has 100 turns and grid side winding has 400 turns.

Step 2

The grid side winding will be the same, as it is 400 turns wye-connected with a power rating of $60\ MVA$. The voltage rating associated with every 100 turns can be assumed to be $33\ kV$ and will have a $15\ MVA$ power rating. The top 100 turns of the grid side winding are called W2d. The next 100 turns after W2d are called W2c and the 100 turns following that are called W2b. The last 100 turns are called W2a. When connected in series, the total number of turns will reflect the grid side windings total 400 turns and $132\ kV$ voltage rating.

As seen in Figure 5-2, the single phase grid side winding is going to be tapped at two positions in such a way that it can provide turns-ratios of 1:4, 1:2 and 1:1 and it can be assumed there is no change in $\frac{volts}{turn}$. If we also assume that nothing changed from Step 1; including the conductor size across the transformer but the length of the conductor would change with change in turns-ratio.

Step 3 — Transformer resistance & leakage reactance

Resistance depends on the cross-sectional area and the length of the conductor used for each winding. The length of the conductor depends on the mean diameter of each coil. Therefore, to verify the resistance of each coil for the transformer, the information about the length and cross-sectional area of the conductor of each coil is required.

Assuming windings have been designed for equal current density in the conductors, the windings resistances split equally. The total transformer resistance, $R^{pu}(= 0.0063pu)$, is

assumed to be split equally between the STATCOM (R_{W1}^{pu}) and grid side windings (R_{W2}^{pu}) of the transformer.

$$R_{W1}^{pu} = R_{W2}^{pu} = \frac{1}{2}R^{pu} = 0.00315pu \quad \textbf{(B.1)}$$

For convenience, the total leakage reactance, $X^{pu}(= 0.1292pu)$, is also split evenly.

$$X_{W1}^{pu} = X_{W2}^{pu} = \frac{1}{2}X^{pu} = 0.0646pu \quad \textbf{(B.2)}$$

For simulation purposes, it has been assumed that the cross-sectional area of the conductor of each coil remains constant along the height and length of the transformer coil. Therefore, theoretically it can be assumed that W2d, W2c, W2b and W2a will have an equal number of turns, as well as equal resistance and reactance.

If we consider the grid side winding (HV): then the base power, $S_{base}(= 60MVA)$ and base voltage, $V_{pbase\,(W2)}$ $(= 132kV)$, can be used to calculate the impedance base, Z_{pbase} by using equation (B.3).

$$Z_{pbase\,(W2)} = \frac{(V_{pbase})^2}{S_{base}} = 290.4\,\Omega \quad \textbf{(B.3)}$$

The real (un-normalised) winding impedance of grid-side winding is given by equation (B.4) and (B.5).

$$R_{W2} = R_{W2}^{pu} * Z_{pbase} = 0.00315 * 290.4 = 0.915\,\Omega \quad \textbf{(B.4)}$$

$$X_{W2} = X_{W2}^{pu} * Z_{pbase} = 0.0646 * 290.4 = 18.76\,\Omega \quad \textbf{(B.5)}$$

For STATCOM-side winding, the resistance and reactance can be calculated by taking the equivalent circuit diagram of a transformer grid side winding resistance and reactance can be referred to STATCOM-side windings by considering the turns ratio (k).

$$R_{W1} = R_{W2}\,k^2 = 0.915\,\Omega \times \left(\frac{1}{4}\right)^2 = 0.06 \quad \textbf{(B.7)}$$

$$X_{W1} = X_{W2}\,k^2 = 18.76\,\Omega \times \left(\frac{1}{4}\right)^2 = 1.17\,\Omega \quad \textbf{(B.8)}$$

As for each of the assumed split windings W2a, W2b, W2c and W2d are considered equal, then it would represent 25% in the primary winding. Apportion of R_{W2a} and X_{W2a} represent 25% of the primary winding resistance and reactance. It should be noted that in this simulation, when a section of winding is left open circuit during a tap change sequence, there is no current flowing through it. Hence, there will be no mutual coupling between the part of the winding that is open circuit and the part of the winding that is in operation. Also, after the tap-change, the winding voltage is simply generated by the number of turns in operation using equation (B.).

$$R_{W2a} = 0.25\, R_{W2}\, Z_{pbase} = 0.229\, \Omega \qquad \textbf{(B.9)}$$

When apportioning X_{Wp} $(= 2\pi f L)$, the inductance (L) of the winding and its dependence on the number of turns needs to be considered. Inductance is generally proportional to the number of turns squared, $L \propto N^2$ and so is the reactance $X \propto N^2$.

For the winding HV2a,

$$X_{W2a} = (0.25)^2\, X_{W2}\, Z_{pbase} = 1.172\, \Omega \qquad \textbf{(B.10)}$$

However, there is reason to believe that leakage fluxes are more complex than main path fluxes, and so they may produce inductance proportional to number of turns, $L \propto N$. This would imply,

$$X_{W2a} = 0.25\, X_{W2}\, Z_{pbase} = 4.69\, \Omega \qquad \textbf{(B.11)}$$

It is highly likely that the true leakage reactance of W2a will be between the two values calculated in equations B.10 and B.11. The exact value of the leakage reactance can only be determined either by direct measurement or through finite element analysis (FEA). For this study, a higher reactance value of $4.69\, \Omega$ has been used in grid side winding $(L \propto N)$.

Similarly, the equations from (B.1) until (B.118), can be used to calculate the resistance values for other sub-divided windings: W2b, W2c, W2d.

From the above calculation, theoretically, it can be assumed that the leakage reactance of HV2a can be up to three times the leakage reactance of sum of HV2b, HV2c and HV2d.

Step 4

There will be no change in No-load or Core loss.

The above four steps are theoretical and in practice the values may be. But for the purposes of this simulation, theoretical assumption has been considered.

Step 5

The magnetizing branch, magnetizing losses of 0.2% resistive and 0.2% inductive, have been obtained from a similarly rated transformer datasheet manufactured by ABB. This information has been received via private correspondence. The percentage is converted in pu for winding 1. The magnetizing resistance, R_m of $500pu$ and a magnetizing inductance, L_m of $500pu$ can be estimated.

Base impedance is calculated using equation (B.3), and base inductance is given by equation (B.6) where the R_m and L_m can be converted into SI units.

$$Base\ inductance = \frac{Base\ impedance}{2\pi f} \quad \textbf{(B.6)}$$

The table also shows the transformer winding parameters that have been calculated when following steps 1-5. These parameters have been used in the simulation.

Table B-1 shows the transformer parameters, including all four sections of the grid side winding used in the simulation.

Table B-1: Transformer winding parameters

	Winding 1 (W1)	Winding 2 (W2a + W2b + W2c + W2d)	W2a	W2b	W2c	W2d
Base power rating [MVA] (three phase)	60	60	15	15	15	15
Base power rating [MVA] (per phase)	20	20	5	5	5	5
Base voltage [kV] (ph-ph)	33	132	33	33	33	33
Base voltage [kV] (per phase)	19.05	76.21	19.05	19.05	19.05	19.05
Leakage reactance [pu]	0.0646	0.0646	0.0646	0.0646	0.0646	0.0646
Resistance [pu]	0.00315	0.00315	0.00315	0.00315	0.00315	0.00315
Winding leakage inductance (per phase) [H]	0.004	0.06	0.015	0.015	0.015	0.015
Winding leakage reactance (per phase) [Ω]	1.17	18.76	4.69	4.69	4.69	4.69
Winding resistance (per phase) [Ω]	0.057	0.915	0.229	0.229	0.229	0.229
For the magnetizing branch, magnetizing losses of 0.2% resistive and 0.2% inductive mean a magnetizing resistance Rm of 500 pu and a magnetizing inductance Lm of 500 pu.						
Magnetising branch inductance [H]	28.9 (500 pu)					
Magnetising branch resistance [Ω]	9075 (500 pu)					

Appendix C Tap-changer Switches Ratings

Tap-changer switches applied in the proposed eTC need to be assessed for their voltage and current rating. The voltage across tap-switches is dependent on the transformer's grid-side windings voltage and the grid voltage. This is due to one side of the switch being connected to the grid-side winding and other side being connected to the grid.

The voltage across the grid-side winding changes with the voltage in the STATCOM winding, which in turn, is dependent on the STATCOM voltage and the transformer turns-ratio.

As discussed in Section 5.4 the STATCOM voltage is rated at one and half times $(1.5x)$ its nominal voltage rating, V_{CN}, $(33\ kV)$, to accommodate for a voltage reduction across the phase reactor and coupling transformer. Equations (C.7) and (C.8) below, show the saturation limit in the STATCOM for three-phase and single-phase respectively, while equation (C.9) shows the saturation phase peak voltage. All calculations are n phase peak values to make it easy to read and relate with the values seen in the results.

$$V_{STATCOM} = 1.5 \times V_{CN} = (1.5 \times\ 33)kV = 49.5\ kV \quad \textbf{(C.7)}$$

$$V_{STATCOM}^{rms} = \frac{V_{STATCOM}^{rms}}{\sqrt{3}} = \left(\frac{49.5}{\sqrt{3}}\right) kV = 28.6\ kV \quad \textbf{(C.8)}$$

$$V_{STATCOM}^{pk} = V_{STATCOM}^{rms} \times \sqrt{2} = 28.6\ kV \times \sqrt{2} = 40.4\ kV \quad \textbf{(C.9)}$$

S2d in each phase connects the complete grid-side winding of the transformer with a turns-ratio of 1: 4 to the grid. During each tap-change operation, the phase voltage of the STATCOM reaches its saturation limit, set at the phase peak voltage $40\ kV$ (Equation (C.9), which is reflected on the MV winding of the transformer). Reasons behind the STATCOM phase voltage reaching its saturation limit are analysed in Section 5.4.

In steady state (pre-fault) conditions, the voltage at STATCOM and PCC are in phase with each other. The difference between the voltages is small. During a fault, however, during each tap-change sequence when the STATCOM controller tries to drop the current to $0\ A$, the STATCOM voltage reverses and saturates. When the phase voltage of the STATCOM saturates during a ramp-down and a hold-zero period, all three switches connected to the HV side of the transformer are turned off and no current flows through the circuit. The two time periods and tap-change sequences are explained in Section 5.4.

When all three switches are turned-off, the voltage across the switch is dependent on the grid-side winding terminal voltage and grid voltage. This means that the voltage difference between the STATCOM and PCC now becomes the voltage sum, as the two voltages are in a different polarity of the waveform.

It should be noted that there is a voltage drop across the phase reactor of the STATCOM, that will reduce the voltage across the tap-changer switches. This voltage drop has not been considered, which means the switch ratings will need to be increased slightly.

When the phase voltage of the STATCOM saturates, the phase peak voltage on the grid-side winding is four times the STATCOM-side winding at $160\ kV$. As detailed in Section 5.3, all tap-change occurs when the grid voltage is below $0.5\ pu$. For example, the first tap-down change takes place when the grid voltage drops to $0.5\ pu$. At $0.5\ pu$, the phase peak grid voltage is $\cong 54\ kV$.

The Kirchhoff Voltage Loop (KVL) for S2d consists of the complete grid-side winding and the grid as shown in Figure C-1 (shown in a red colour). Putting the above explanation together and considering the KVL for S2d, the maximum voltage across the switch can be calculated. As discussed earlier, the winding and the grid voltage are in a different polarity in the AC waveform and there is an addition of both phase peak voltages, which would appear across S2d as shown in equation (C.10). This was noted through a series of simulations for one cycle.

$$V_{S2d}^{pk} = V_{W2} + V_G^{pk} = (4 \times V_{STATCOM}^{pk}) + V_G^{pk} = (4 \times 40\ kV) + 54\ kV \approx 214\ kV \qquad \textbf{(C.10)}$$

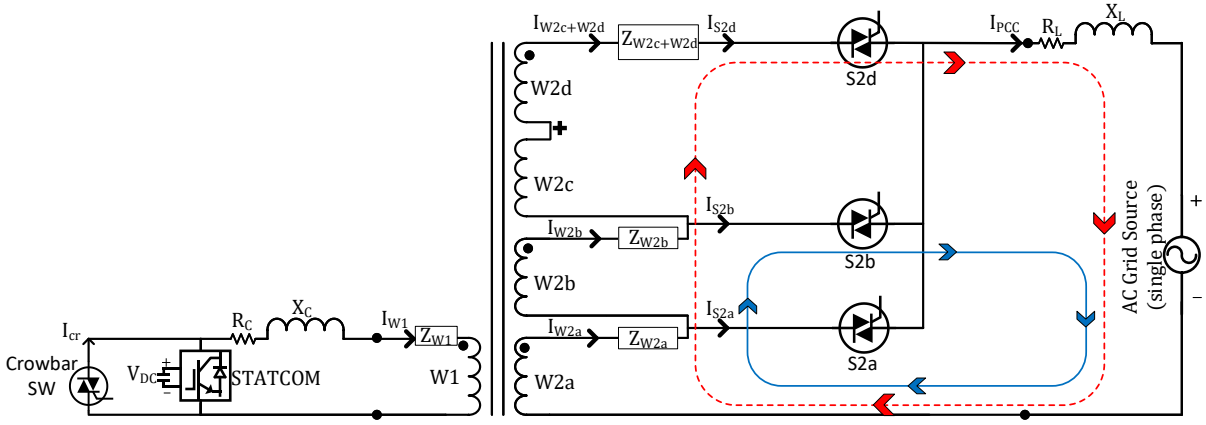


Figure C-1: KVL Loop for S2d in red and S2b in blue

The maximum current flowing through the individual switches depends on the transformer turns-ratio, and this turns-ratio is changed during the tap-change sequence as detailed in Section 5.3. Here, the current ratings for three switches are stated for rating purposes only.

During steady state, the rms and peak current expected to flow through S2d is $250\,A$ and $\sim 354\,A$ respectively. This current rating is $1\,pu$ at PCC, and it is measured when the transformer's TR is $1:4$.

Kirchhoff's Voltage Loop (KVL) for S2b consists of the W2d and W2c part of the grid-side windings and the grid, as shown in Figure C-1 (blue colour). Considering the KVL loop, the maximum voltage across the switch is during the tap-change sequence, when the phase peak voltage on the HV winding, where S2b is connected, is two times the STATCOM-side winding at $80\,kV$. Again, at $0.5\,pu$, the phase peak grid voltage is $\cong 54\,kV$. Similar to S2d, the grid-side winding and the grid voltage are in the same polarity of the AC waveform where there is an addition of both phase peak voltages, and it would appear across S2b as shown in equation (C.11). This was again noted through a series of simulations for one cycle.

$$V_{S2b}^{pk} = V_{W2} + V_G^{pk} = (2 \times V_{STATCOM}^{pk}) + V_G^{pk} = (2 \times 40\,kV) + 54\,kV \approx 134\,kV \quad \textbf{(C.11)}$$

During the first tap-down sequence, the rms and peak current expected to flow through SW2 is $500\,A$ and $\sim 707\,A$ respectively. This current rating is $2\,pu$ at PCC and it is when the transformer's turns-ratio is $1:2$.

For S2a, the maximum voltage across the switch occurs during the steady state operation. In each phase S2a connects winding W2a to the grid. The phase peak voltage rating of W2a is measured on one end of S2a and is at $\cong 27\,kV$. The other end of the switch is at the grid peak phase voltage of $\cong 107.8\,kV$. So, the maximum phase peak voltage across S2a is given by equation (C.12).

$$V_{S2a}^{pk} = V_G^{pk} - V_{W2a} = 107.8kV - 27\,kV \approx 80\,kV \quad \textbf{(C.12)}$$

During the second tap-down sequence, the rms and peak current expected to flow through SW4 is $1000\,A$ and $\sim 1414\,A$ respectively. This current rating is $4\,pu$ at PCC and it is when the turns ratio is $1:4$. Table C-1 shows the maximum voltage rating seen by each tap-change switch. It should be noted that tap-switches need to block voltages in both directions and allow current to flow in both directions.

Table C-1: Tap-change switch rating

	S2d	S2b	S2a
Phase peak voltage (V^{pk})	209 kV	128.5 kV	80 kV
Peak current (I^{pk})	354 A	707 A	1414 A

Appendix D STATCOM Current Controller

The fault response of a grid connected STATCOM is dictated by its adopted current control strategy. Figure D-1 shows a block diagram of the designed controller for phase A of a star-?-configured STATCOM connected to the Grid. As discussed in Section 5.2, a separate controller allowed independence of operation of each phase during asymmetric faults. As can be seen, the current controller consists of three stages according to their functions. The first stage is a phase A line-to-neutral voltage (V_{PCC}^{A}) measurement which is taken at PCC, which determines the fault signal for a tap change sequence. In the second stage, phase A feed forward voltage (V_{C}^{*A}) and reference current input for each phase are put through a Proportional Resonant (P+R) controller to vary the output voltage of each phase of the STATCOM to maintain a constant current output. The reference current I_{C}^{*A} for $1\ pu$ is generated according to support the tap-change sequence as described in Section 5.4. In the final stage, based on the reference current, the coupling transformer-turns ratio is changed to vary FCC to the grid at PCC. The three stages are detailed in the next three sub-sections.

Stage 1: Grid synchronisation & fault detection

The inverter must be synchronised to the grid for the control of FCC to the grid. For the purposes of testing the tap sequence, a grid fault with a lower retained phase voltage (compared to the winding voltage) is used, which is sufficiently below the threshold to trigger a tap-down sequence, but with enough retained voltage to test that the STACOM is able to inject current into that retained voltage. The transformer and its tap positions are detailed in Section 5.3.

In stage 1, for each phase, the single phase PLL block is used to obtain the phase angle of the positive sequence fundamental component of the grid voltage. As shown in Figure D-1, depending on the voltage values at PCC, the fault signals are generated. If the V_{PCC}^{A} is greater than $0.7\ pu$ of its nominal voltage rating, then fault signal 1 (FS1) is generated. The number 1 in fault signal relates to the FCC from the STATCOM in pu. FS1 signifies that an FCC of $1\ pu$ is expected at PCC. Similarly, when V_{PCC} is less than $0.7\ pu$ but greater than its nominal voltage rating by $0.28\ pu$ or more then fault signal 2 (FS2) is generated and FCC contribution of $2\ pu$ is expected. Again, when V_{PCC} is less than $0.28\ pu$ of its nominal voltage rating then a fault signal 4 (FS4) is generated and an FCC contribution of $4pu$ is generated.

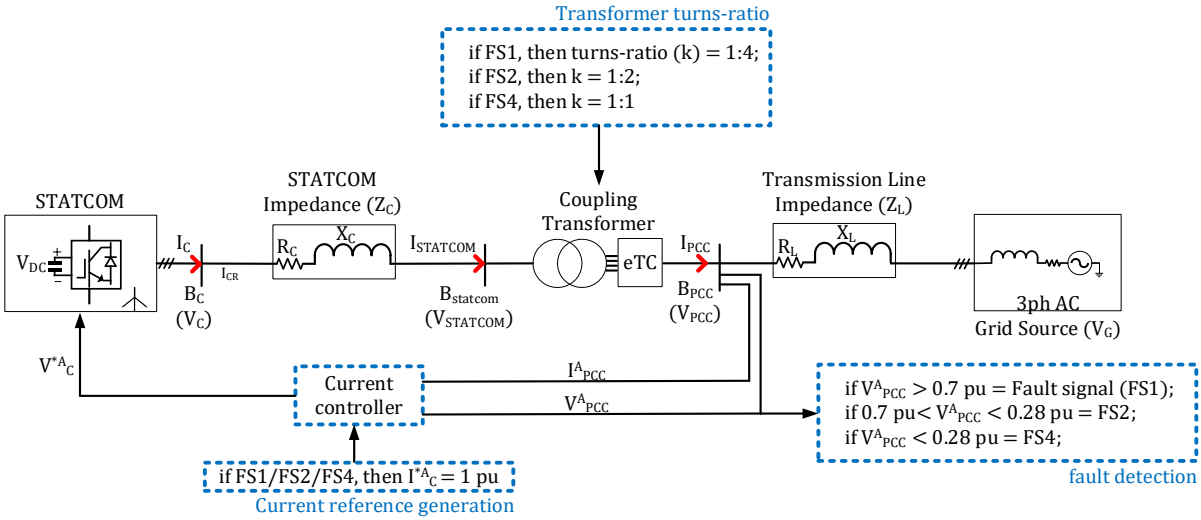


Figure D-1: Grid connected STATCOM control scheme for phase A

The single-phase synchronous reference frame phase locked loop (SRF-PLL) response time to change in the terminal voltage is slower than the three-phase PLL. Further work required to increase accuracy and speed of the single-phase PLL. At this stage, a timed fault detection signal is sent to the STATCOM current controller and transformer tap-change. The timing of the fault signal is based on a response of a three-phase PLL block.

Stage 2: Current controller

Three variable reference frames are normally used when analysing the dynamics of three-phase STATCOM or VSCs and designing their controllers [112]:

(a) natural (abc) frame,
(b) stationary reference $(\alpha\beta 0)$ frame, and
(c) synchronous rotating $(dq0)$ frame.

The transformer consists of three single phase transformers, each phase needs to be controlled separately and treated as a single-phase grid-connected inverter. In a single-phase system, the rotating frame transformation cannot be applied directly. Hence, a Proportional Resonant (P+R) controller can be used as a natural frame current controller for each phase of the STATCOM. Due to infinite gain at the fundamental frequency, the P+R controller can eliminate the tracking error of the sinusoidal current with a zero steady-state error and poor disturbance rejection [113]. The P+R controller which achieves infinite gain at the AC frequency ω_0 can be given by a transfer function equation (D.13) [114]. There can be stability problems associated with an infinite gain. So, the PR controller gains can be adjusted to obtain

a high enough finite gain for eliminating the voltage tracking error, through a cut off frequency ω_c. This can be represented by a transfer function equation (D.14) [114]. In this simulation equation (D.13) is used.

$$G_R(s) = K_p + K_i \frac{s}{s^2 + \omega_0^2} \quad \textbf{(D.13)}$$

$$G_R(s) = K_p + \frac{K_i \omega_c s}{s^2 + 2\omega_c s + \omega_0^2} \quad \textbf{(D.14)}$$

Where

K_p= proportional gain,

K_i= integral gain,

ω_0= AC frequency $(50Hz)$,

ω_c= cut-off frequency.

The current feedback from the PCC bus and the P+R controller ensures a zero steady-state error is achieved by implementing a current controller in the natural reference frame. The aim of the current controller is to change or maintain the magnitude of the current at PCC by following an internally generated current reference, and then by varying the STATCOM output voltage. The generated current reference is changed during the tap-down and tap-up sequence of the coupling transformer. The two sequences have been discussed in detail later in Section 5.4. Feedforward of the voltage at PCC is added to the P+R controller to minimise disturbance in the grid voltage.

If $V^{A}_{PCC} > 0.7$ pu => turns-ratio (k) = 1:4;

If 0.7 pu $< V^{A}_{PCC} < 0.28$ pu => k = 1:2;

If $V^{A}_{PCC} < 0.28$ pu => k = 1:1;

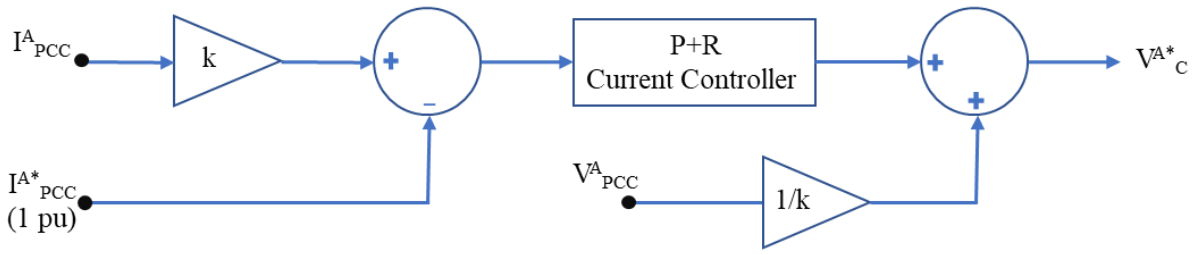


Figure D-1: Grid connected STATCOM control scheme for phase A

Stage 3: Transformer turns-ratio

At the end of stage 2, a reference voltage is generated for each phase of the STATCOM. The three-phases of the STATCOM independently vary their output voltages to follow the respective generated current reference. During normal operation, all three phases maintain a constant current output from the STATCOM.

As shown in Figure D-1, depending on the voltage values at the PCC, fault signals are generated. If the phase voltage is greater than $0.7\ pu$, the turns-ratio remains unchanged at $1:4$. However, if the phase voltage is lower than $0.7\ pu$ but greater than $0.28\ pu$, the turns-ratio is changed to $1:2$ and for phase voltage lower than $0.28\ pu$, the turns-ratio is changed to $1:1$. The change in turns-ratio changes the FCC at PCC.

Appendix E Analysis of the Proposed eTC with Grounding Transformer

This appendix shows the analysis of the proposed SSBC with an eTC network with grounding transformer to calculate the zero-sequence current at the PCC (I^0_{PCC}) and the fault current in each sequence network. Simulation results for this circuit are shown in Figure E-2.

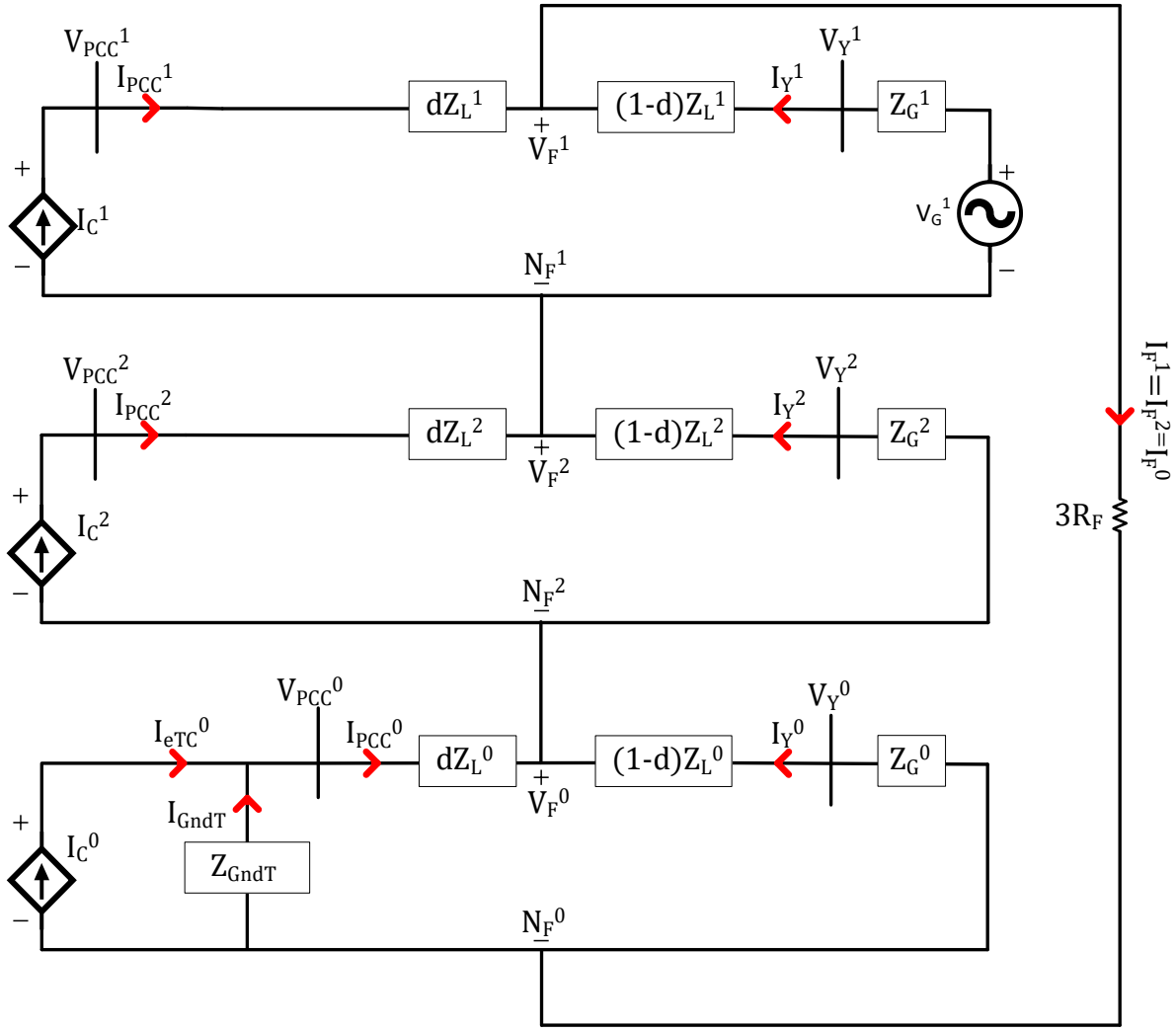


Figure E-1: Sequence network connection for a SLG fault @ B_{PCC} for a STATCOM (SDBC) with coupling transformer (delta-star) network

$$V_F^1 = V_G^1 - I_Y^1 Z_B^1 \quad \textbf{(E.1)}$$

$$V_F^2 = -I_Y^2 Z_B^2 \quad \textbf{(E.2)}$$

$$V_F^0 = -I_Y^0 Z_B^0 \quad \textbf{(E.3)}$$

$$3\, I_F^1 R_F = V_F^1 + V_F^2 + V_F^0 \quad \textbf{(E.4)}$$

Replacing terms of V_F in equation E.4 with equations E.1, E.2 and E.3.

$$3\, I_F^1 R_F = V_G^1 - I_Y^1 Z_B^1 - I_Y^2 Z_B^2 - I_Y^0 Z_B^0 \quad \textbf{(E.5)}$$

$$3\, I_F^1 R_F = V_G^1 - (I_F^1 - I_{PCC}^1) Z_B^1 - (I_F^1 - I_{PCC}^2) Z_B^2 - (I_F^1 - I_{PCC}^0) Z_B^0 \quad \textbf{(E.6)}$$

Rearranging the above equation:

$$I_F^1 (3 R_F + Z_B^1 + Z_B^2 + Z_B^0) = V_G^1 + I_C^1 Z_B^1 + I_C^2 Z_B^2 + I_{PCC}^0 Z_B^0 \quad \textbf{(E.7)}$$

To find the unknown term I_{PCC}^0, zero-sequence network will be analysed:

$$I_{GndT} + I_C^0 = I_{PCC}^0 \quad \textbf{(E.8)}$$

$$I_{PCC}^0 + I_Y^0 = I_F^1 \quad \textbf{(E.9)}$$

$$I_{GndT} Z_{GndT} + I_{PCC}^0 Z_A^0 = I_Y^0 Z_B^0 \quad \textbf{(E.10)}$$

$$(I_{PCC}^0 - I_C^0) Z_{GndT} + I_{PCC}^0 Z_A^0 = (I_F^1 - I_{PCC}^0) Z_B^0 \quad \textbf{(E.11)}$$

Rearranging for I_{PCC}^0;

$$I_{PCC}^0 = \frac{I_F^1 Z_B^0 + I_C^0 Z_{GndT}}{Z_{GndT} + Z_A^0 + Z_B^0} \quad \textbf{(E.12)}$$

Replacing the above term for I_{PCC}^0 in equation (E.7) and rearranging this equation for I_F^1 the following equation (E.13) can be formulated.

$$I_F^1 = \frac{V_G^1 + I_C^1 Z_B^1 + I_C^2 Z_B^2 + I_C^0 \left(\frac{Z_{GndT} Z_B^0}{Z_{GT} + Z_A^0 + Z_B^0}\right)}{3 R_F + Z_B^1 + Z_B^2 + \left(\frac{Z_B^0 (Z_{GndT} + Z_A^0)}{Z_{GndT} + Z_A^0 + Z_B^0}\right)} \quad \textbf{(E.13)}$$

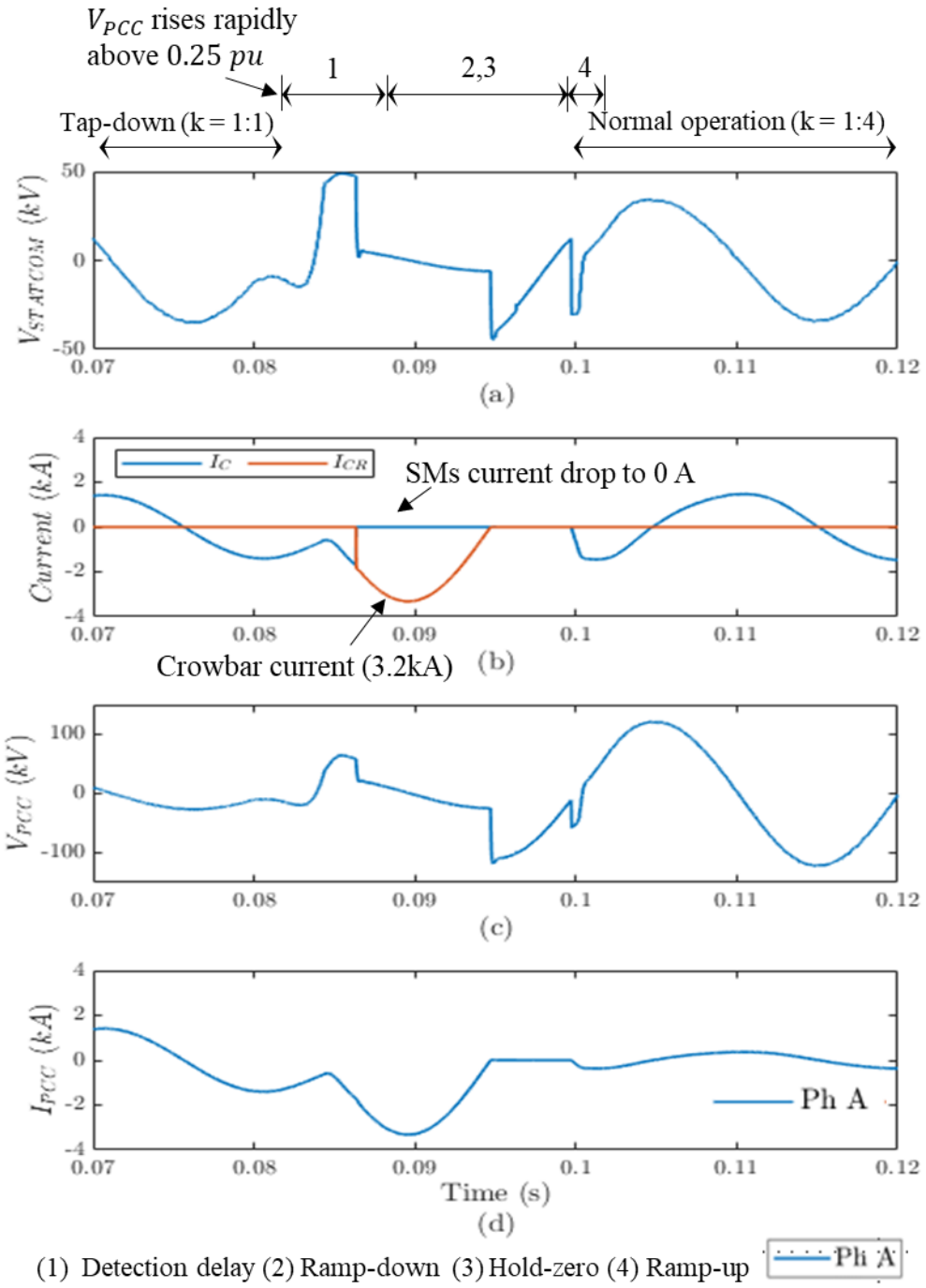


Figure E-2: Results for proposed STATCOM with eTC with grounding transformer for a SLG fault showing crowbar current during tap-up sequence failure (a) Voltage at $B_{STATCOM}$ (b) Current in Ph A Sub-Modules (I_{SM}) and crowbar circuit (I_{CR}) (c) Voltage at B_{PCC} and (d) Current I_{PCC}