

UNIVERSITY OF LONDON
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DEPARTMENT OF ELECTRICAL ENGINEERING

THE PROTECTION AND SWITCHING
OF A HIGH VOLTAGE SUBSTATION
USING LOGICAL METHODS

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by

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ABSTRACT

With the introduction of the 400 kV network it is anticipated that the occurrence of substation busbar faults will increase in number. The planned increase in short circuit capacity of this network requires fast fault detection to limit damage to equipment. Increased switching will be required to maintain the security of the network and any maloperation would have severe consequences over a wide area.

The development of a network simulator to include transient and sub-transient terms so that it is especially suited to short circuit study is described. The simulator is used to produce current and voltage waveforms for healthy and faulted substation busbars. Application of short circuits is from a loaded network condition. Two transmission line simulations for long and short lines are developed.

A method of logic switching suitable for high voltage substations which supervises manual switching and performs automatic reswitching to maintain security on substation busbar faults is developed. The Karnaugh map representation of states in a switching algebra is used to develop the equations in Boolean algebra form which are the basis of the switching operations. An off-line computer program is developed to give a convenient method of determining

these equations in a form suitable for programming a real-time switching controller.

The problems associated with present busbar protection schemes and a technique based on sampling and analogue to digital conversion using a digital summator are discussed. The basis of a busbar protection scheme using switching variables and logic is developed and this method is proposed for further study.

A proposal for a centralised high voltage substation controller to be used for all substation functions is discussed.

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LIST OF SYMBOLS

The most commonly used symbols and notations are defined below. Symbols, which are not listed, are explained in the text.

In general, instantaneous values are denoted by lower case letters and phasor quantities by upper case letters. Values, except where stated, are in per unit.

Main Symbols

i	Instantaneous value of current
I	Phasor value of current or primary network instantaneous current
e	Instantaneous value of voltage
E	Constant or phasor value of voltage
R	Resistance of detection circuit
r	Resistance
x	Reactance or input to logic controller
g	Conductance
c	Capacitance
X	Total reactance
ℓ or l	Leakage inductance or transmission line inductance

L	Total self inductance or primary network inductance
t	Time in seconds
T	Torque or time constant
p	Operator $\frac{d}{dt}$
P	Power
Z	Impedance or output logic variable
Y	Admittance
H	Machine inertia constant
N	Total number of primary feeders
J	Moment of inertia
$x_d(p)$	Operational impedance relating i_d to ψ_d
$x_q(p)$	Operational impedance relating i_q to ψ_q
$G(p)$	Operational quantity relating e_f to ψ_d
α_{d1}, α_{d2} A_{d1}, A_{d2} B_{d1}, B_{d2}	 Coefficients defined in Section 3.2.2
ω	Angular velocity of infinite bus in radians per second
ν	Angular velocity of rotor in radians per second
δ	Load angle of synchronous machine with respect to bus

λ	Phase angle of θ at zero time
ψ	Flux linkage
Y	Logic variable for present state
y	Logic variable for secondary state
f	Function of a switching algebra
$\cdot$	and (binary operation of algebra)
V	or (binary operation of algebra)
$-$	not (unary operation of algebra)
s	Stable state

Subscripts

a	Phase a
b	Phase b
c	Phase c
α	α components
β	β components
o	Zero component or non-transformed value
d	Direct axis
q	Quadrature axis
f	Field winding
e	Electrical or transmission line
m	Mechanical or maximum
t	Turbine or primary network or transposed

s	Secondary network or sending end
md	Direct axis mutual
mq	Quadrature axis mutual
R	Independent
n	n th value
r	Receiving end

Superscripts

'	Transient
"	Sub - transient
*	Modified value or conjugate tensor

Computer Symbols

M	Multiplication operation
D	Division
S	Summation
RES	Resolver
NEG	Negation
AT	Arctan operator
I	Integration
IR	Relay or switch
XE	Transmission line reactance
LE	Transmission line inductance

RE	Transmission line resistance (negative)
RA	Machine resistance
WO	314.16 radians per second
EF	Field excitation
XD	Direct axis reactance
XQST	Quadrature axis sub-transient reactance
TQOST	Quadrature axis open circuit sub-transient time constant
XQ	Quadrature axis synchronous reactance
C1, C2, C3, C4	Constants
TT	Turbine torque
H	Inertia constant
G	Transmission line conductance
C	Transmission line capacitance
IT	Time
EM	1.4142
EMD	0.0
LAM	Machine load angle
RR	Resistance of relay circuit
RS	Resistance of secondary
HALF	- 0.5
ROOT	0.866

CHAPTER 1

INTRODUCTION

1.1 Present Practices in Substation Protection

1.1.1 Busbar Protection by Circulating Current Schemes

In general, busbar protection schemes use Kirchhoff's first law as their principle of operation. Although this basis is sound, difficulties in operation occur as a result of the application of techniques and the physical limitations of the equipment used. Protection systems have evolved by the modification of fundamental systems. The most commonly used at present is the circulating current system (32).

Figure 1.1 shows its application to a single phase circuit. Two equal-ratio current transformers, CT 1 and CT 2, are situated to measure the current at each end of the protected zone and their secondary windings are so connected that current flowing through the zone in the primary circuit does not cause current to flow in the relay connected to the CT secondaries. Assuming a low impedance secondary circuit and CTs which reproduce the primary current waveforms perfectly, the instantaneous current in the relay is proportional to the sum of the instantaneous currents flowing into the protected zone. For a fault outside the zone the sum of instantaneous currents into the zone is zero and therefore no relay current flows;

however on an internal fault the current in the relay is proportional to fault current (4, 5, 66).

1.1.2 Current Transformer Saturation

The difficulty with this type of protection is that CTs are not perfect sensing devices and circulating current schemes have been modified with an aim to giving the required primary fault setting and through fault stability. The equivalent circuit for the arrangement of Figure 1.1 is given in Figure 1.2. This arrangement works well provided one or more CTs do not saturate. When a CT saturates it acts as a parallel path to the relay with an impedance equivalent to the secondary winding resistance, r_s , and its leakage inductance, ℓ_s . The voltage across the relay is therefore the product of the sum of currents from unsaturated CTs and the impedance of the saturated CTs. The maximum possible relay voltage under through fault conditions is therefore

$$V_r = \sum I_s R \quad (1.1)$$

$$\text{where } \frac{1}{R} = \frac{1}{r_{s1}} + \frac{1}{r_{s2}} + \dots \quad (1.2)$$

if I_s is the current from unsaturated CTs and r_{s1} , r_{s2} , ... are the resistances of saturated CTs.

To achieve stability on a through fault it

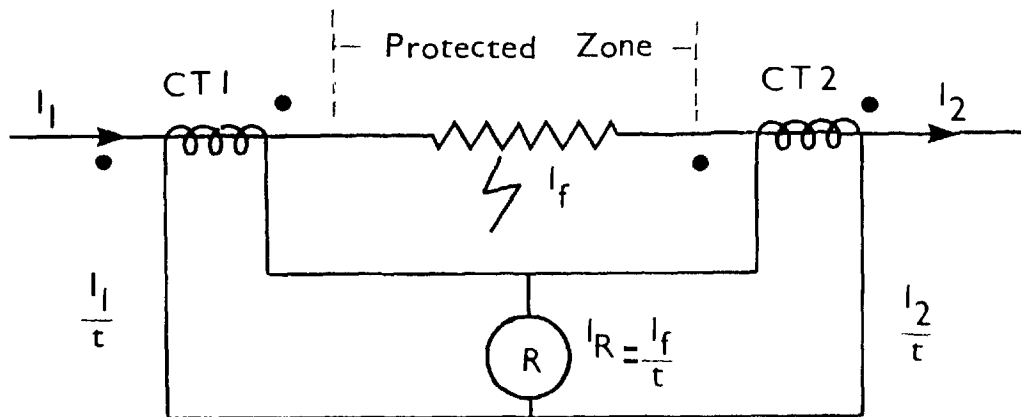


FIGURE I.1 Circulating Current Protection System

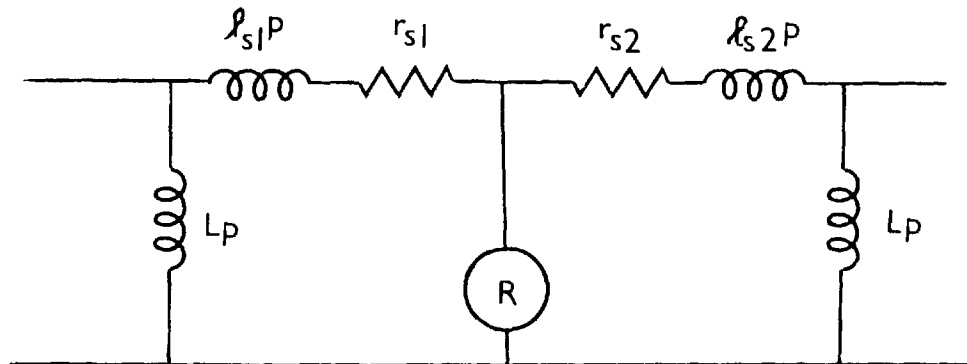


FIGURE I.2 Equivalent Circuit of Circulating Current Protection System

is necessary that the voltage setting of the protective relay be greater than the value of V_r . To obtain this required setting a stabilising resistor is connected in series with the relay current coil. The setting of the relay can be determined as follows:

$$\text{If } I_m = \sum_{n=1}^m I_n \quad (1.3)$$

where there are m feeders each taking I_n magnetising current at a voltage of V_r , the primary fault-setting of the protection is given by

$$I_f = k(I_s + I_m) \quad (1.4)$$

where k is the ratio of turns of the CT from the secondary to primary side. I_s is the relay current.

High impedance relays are used in this scheme and difficulties arise during an internal fault. The CTs try to force a high value of current through the stabilising resistor and relay coil, and the high peak voltage which occurs may damage equipment by exceeding the insulation level. This can result in operation failure. Consequently the peak voltage is limited to an acceptable value by connecting a non-linear resistor in parallel with the operating circuit. To ensure satisfactory operation it is necessary to employ CTs with a high saturation voltage. The criterion used in practice is to specify knee point voltage of CTs as the ratio of secondary open circuit e.m.f. at the knee point to the induced secondary e.m.f.

at one ampere with rated burden. This insures relay operation on internal faults to give a voltage of twice the relay operating voltage (12).

If a low primary fault setting is required the relay must have a low current setting and will thus have a high inductance. The result is that the relay coil voltage setting will be much greater for a.c. than d.c. component. Since the relay must not operate on the d.c. transient component the coil inductance is tuned out by a capacitor or the component is eliminated through a bridge type rectifier. For a fault occurring near a busbar but external to it, the entire fault current from the busbar flows out on one feeder. The current transformer in this feeder must have a constant ratio up to the maximum external fault current (i.e. it must not saturate). Also the d.c. component tends to cause saturation, which produces an unbalance in the protection circuit during transient conditions.

1.1.3 The Prevention of False Operation

Schemes have been devised to prevent false operation of relays during external faults despite CT saturation by providing restraint. Biased percentage differential relays (31) and harmonic restraint (7) have been used; however these result in a delay in speed of clearance on internal faults. Differential biased relays take advantage of the fact that for through faults there are large secondary currents

flowing between CTs and that large secondary currents also flow when a CT saturates if the protection relay has a reasonably high impedance. Thus a percentage of this current is applied to a coil (56, 58) which operates against the tripping coil and will restrain tripping when external faults or saturation occurs; but there is no restraining action on internal faults. Harmonic braking is based on the difference of the harmonic content of the current waveforms in the protection circuit. For a fault in the protected zone detection equipment current waveforms are nearly sinusoidal; however an external fault introduces higher harmonics, particularly third harmonics, in this circuit. This is shown in Figure ^{4.3}~~4.3~~. However this figure also shows that it occurs only under certain conditions.

Since it is not practicable to build CTs with cores of sufficient cross-sectional area to avoid saturation from d.c. transients with long time constants, special types of CTs have been developed. One type has an air gap in the core (68), another has no core at all (24) and is known as a linear coupler. The secondary voltage of the linear coupler is proportional to primary current (see Section 3.3.3); therefore all the secondary windings of the couplers on one busbar are connected in series to the relay (25). The power obtainable from a linear coupler is low and for maximum transfer of energy it is necessary to match the relay impedance to the secondary impedance of the couplers. When operating a relay coil from linear couplers connected in parallel it is necessary to employ secondary branch impedances

of almost equal value if the current from each branch is to be proportional to the primary current. On a through fault the differential current caused by resistance imbalance may cause tripping. The secondary a.c. and transient currents which flow during a through fault add to the problem. Consequently the series arrangement is preferred (45).

1.1.4 Phase Differential Busbar Protection

Another principle in busbar protection is based on the phase difference between currents flowing into and out of the busbar. The principle was used by Steele (64) and also in the Casson-Last system (43) which is shown in Figure 1.3. Basically, there are four high-speed relays, A,B,C and D, which have operating times of the order of one millisecond. Contacts on coils A and B are connected in series to coil P and the coil of A is connected between a positive protection bus and common, and the coil of B is connected between a negative protection bus and common. Each bus is connected through diodes to all the CTs of one phase. On an external fault current flows through the diodes to energise the positive bus and negative bus together. On each half-cycle the coils of A and B, also C and D, are energised together so that their contacts move together. In this way the coils of relays P and Q are never energised. However on an internal fault the positive protection bus and negative protection bus are

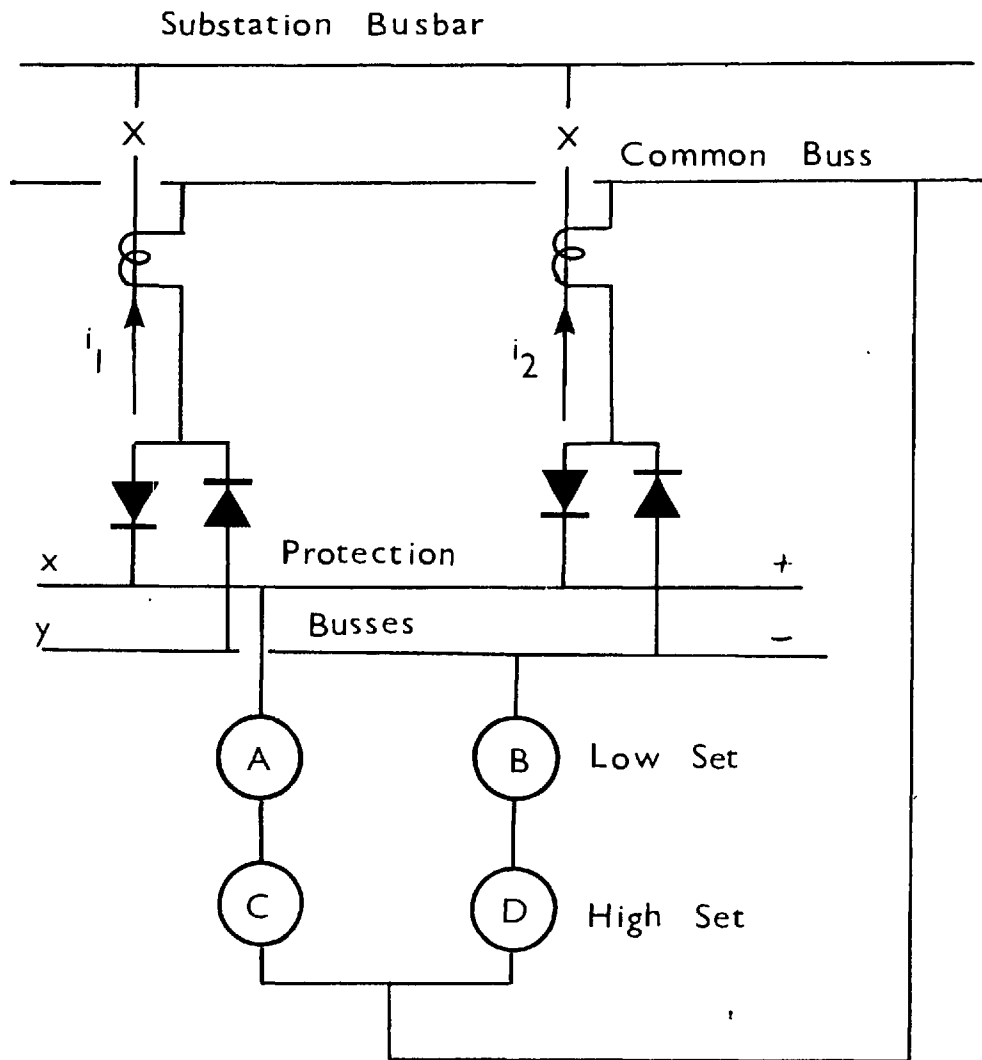


FIGURE 1.3 Casson-Last System Schematic

energised alternately, thus energising coils A and B alternately so that their contacts move out of phase resulting in energising of the relay coils P and Q.

The positive protection bus (x) and the negative bus (y) can be considered to be two logic busses. If x and y signify that they are energised, and $\bar{x}$ and $\bar{y}$ signify that they are not energised, then Boolean expressions (see Appendix 2) can be written for the tripping of breaker on the protected zone. If a and $\bar{a}$ are used to indicate the forward and back contact respectively of relay A, etc., then the Boolean expressions are as follows.

$$\text{TRIP} = p \cdot q \quad (1.5)$$

$$P = (a \cdot \bar{b}) \vee (b \cdot \bar{a}) \quad (1.6)$$

$$Q = (c \cdot \bar{d}) \vee (d \cdot \bar{c}) \quad (1.7)$$

$$A \text{ or } C \subseteq x \quad \text{and} \quad \bar{A} \text{ or } \bar{C} \subseteq \bar{x} \quad (1.8)$$

$$B \text{ or } D \subseteq y \quad \text{and} \quad \bar{B} \text{ or } \bar{D} \subseteq \bar{y} \quad (1.9)$$

Combining (1.5), (1.6), (1.7), (1.8) and (1.9) the Boolean expression for TRIP in bus form becomes

$$\text{TRIP} = (x \cdot \bar{y}) \vee (\bar{x} \cdot y) \quad (1.10)$$

In practice two sets of high speed relays, one low set (A and B) and one high (C and D), are used

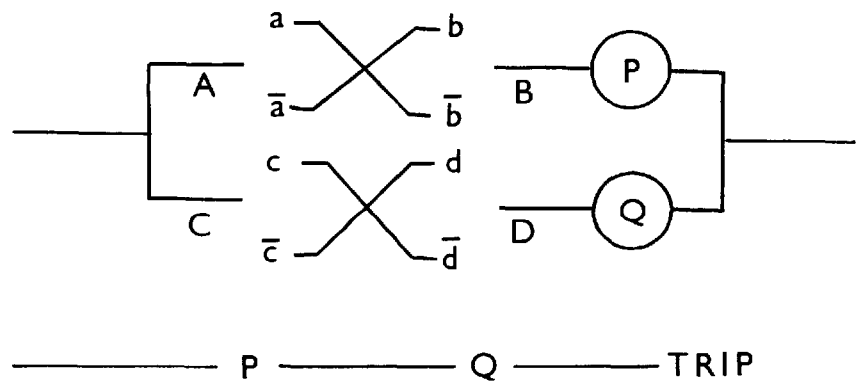


FIGURE I.4 Contact Arrangement for Phase Discrimination

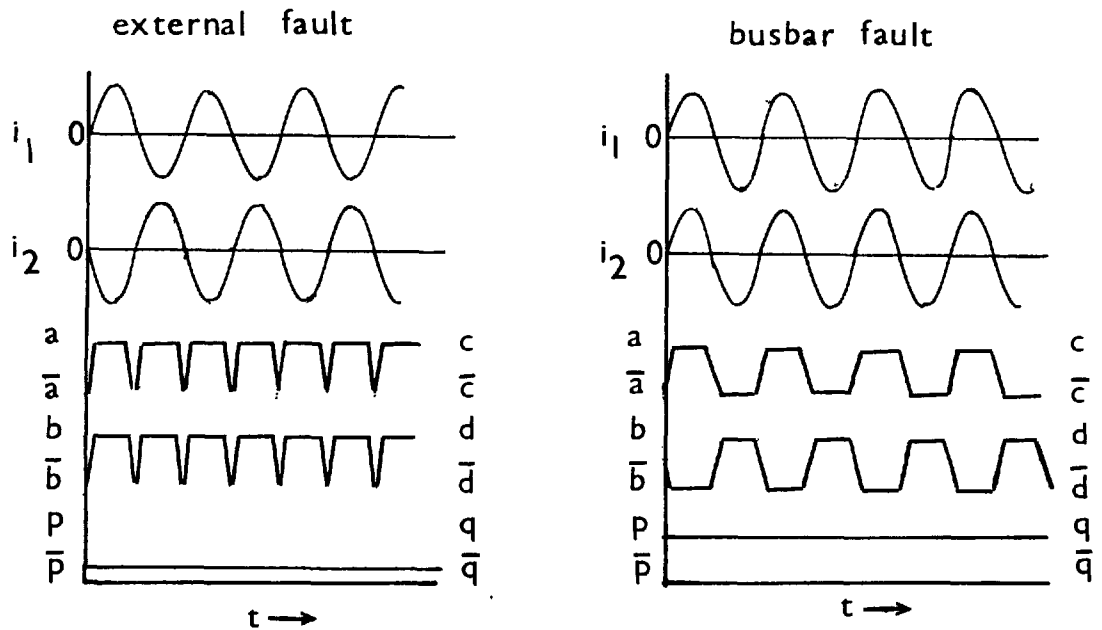


FIGURE I.5 Phase Relation and Contact Movement

to prevent maloperation when unavoidable differences in relay pick-up settings cause one of the pair of relays to close before the other under through fault conditions. The difference between the pick-up current of the two sets of relays is made sufficient to ensure that both relays of the low pick-up current setting operate before either of the high pick-up set. Thus if a condition of through fault occurs which operates only one relay in a set the other set blocks maloperation and ensures stability. ~~Saturation of CTs must be avoided in this system as well.~~ If, under heavy through fault conditions, saturation occurs one of the protection busses will not be energised and the protection will be unstable.

1.1.5 Earth Fault Busbar Protection

If a busbar fault at a substation involves earth the fault current flowing in the earth path can be used to detect the busbar fault. This is achieved by insulating all primary equipment from earth and providing only one path to earth. Detection of current in this path indicates a busbar fault. Systems using this method are called frame leakage protection. The Forrest Flashover protection scheme is completely dependent upon this principle whereas many schemes use frame leakage in conjunction with other principles of protection. Examples of such schemes are the Translay System and the Reynolle Dualock System as outlined by Naylor (43). High voltage substations are

not easily insulated and detection times are many cycles long for this system (63).

1.2 Busbar Protection System Principles

1.2.1 Location of Fault

When a fault occurs on a transmission line some distance from the protective equipment there is great difficulty in differentiating between this fault and transients arising from other causes such as switching. Fault resistance and balance point shifting are among the factors which interfere with the detection of line faults. For a fault that occurs adjacent to the protection equipment the problem is reduced to determining the direction of the fault. When a busbar fault occurs the problems encountered are different from those of line fault conditions. The greatest problem caused by a line fault, that of determining if a fault exists, does not occur on a busbar fault where the protective equipment is adjacent to the fault. But the problem of determining the location of the fault, which is relatively easy for line fault protection equipment, is difficult for busbar faults with the greater number of boundary points which require monitoring. When using the phase difference principle of protection basically each feeder connected to the busbar is tested to determine the direction of flow in relation to all the other feeders. If at one instant in time the flow is in the same direction in all feeders only one protection bus is energised and

tripping occurs. It requires flow in only one feeder to be out of phase to energise the other protection bus and to block operation of all busbar feeder breakers.

1.2.2 Through Fault Stability

An example of a circulating current scheme with three feeders is shown in Figure 1.6. A supply of unit amperes is connected to feeder number 1 and loads equal to one-half unit amperes are connected to feeders 2 and 3. During normal operation primary current flows into the busbar on feeder 1 and flows from the busbar on feeders 2, ^{and 3} ~~and 3~~. The sum of the currents on the feeders is zero. If an external fault causes fault current to flow in feeder 1 and 3 and saturation of CT2, for a typical case the induced secondary current from CT1 is shown in Figure 1.7. The induced secondary current for CT1 on a normally protected internal three phase fault is shown in Figure 1.7 also.

A current summation of protective circuit current for different values of stabilising resistance is shown in Figure 1.8. When an internal fault occurs the current in the protection relay, which is shown in Figure 1.9, exceeds ^a ~~the~~ setting chosen from Figure 1.8.

If the circulating current scheme and the phase difference scheme both have their monitoring

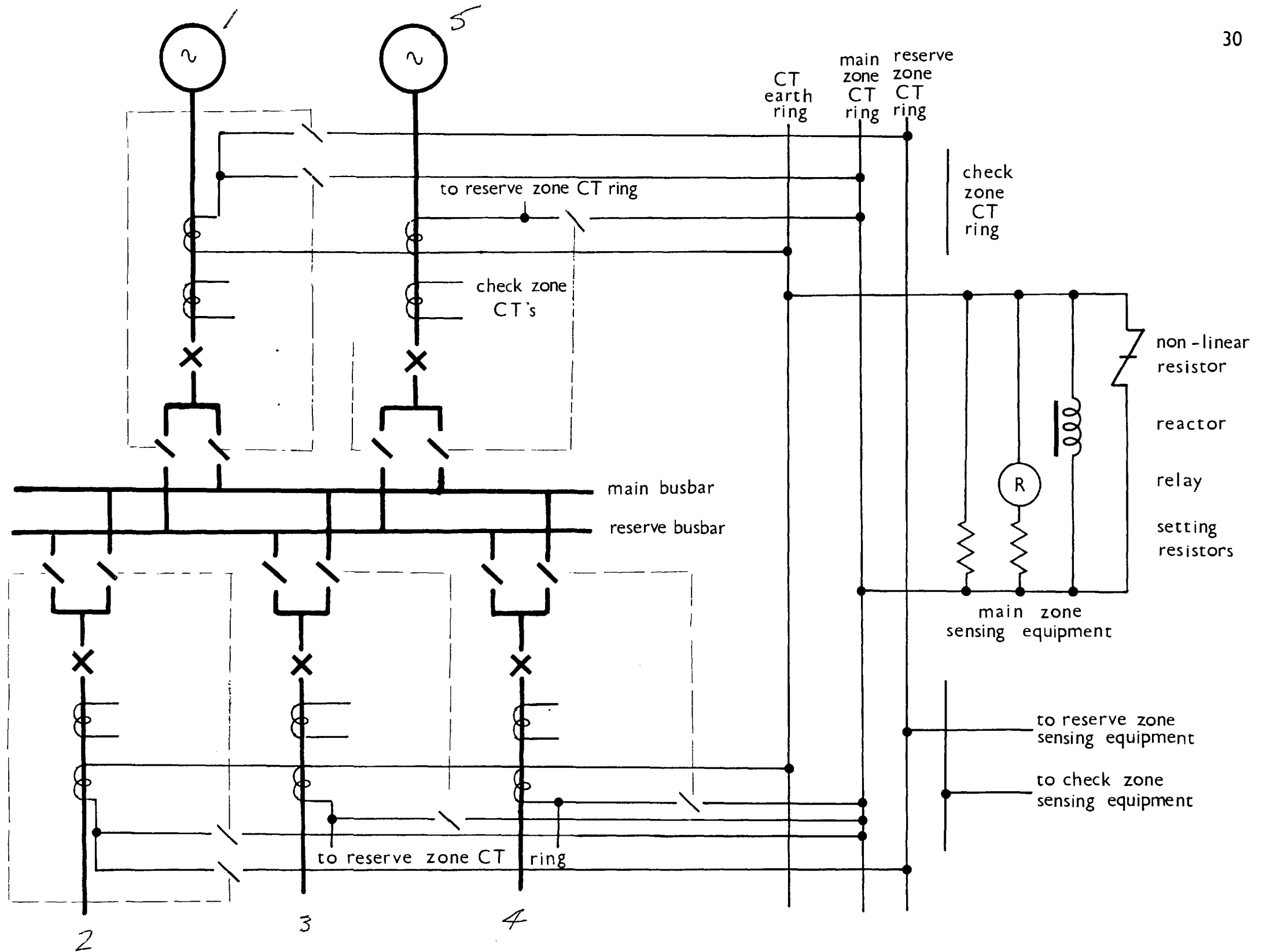


FIGURE I.6 Circulating Current Protection Using High Impedance Relays

devices enclosing a true node (that is, the monitors must not bisect the busbar to be protected) outward flow of power on one feeder will block operation of the protection circuit. The circulating current scheme has the added feature that if two monitors bisect a busbar, tripping will not be blocked by outward power flow on one of these monitors provided that there is an inward flow balance on the other monitor. This feature is used when a check loop or confirming back up protection is required.

Although Kirchhoff's law is a criterion for determination of busbar faults in the primary network, as shown in Figures 1.7 and 1.8, this law cannot be simply mapped onto the secondary or protection circuit of a substation because of the CT characteristics involving non-linearity. While the operating threshold on the primary side is zero current, the threshold on the secondary is determined by the stability requirements. Some tolerance must be permitted in the protection circuit and the corresponding primary circuit unbalance is not determinable.

1.3 Busbar Fault Characteristics

1.3.1 Detection Time

There is, at present, a need to shorten the detection time for 400 kV busbar faults so that the damage, which is possible because of greatly increased

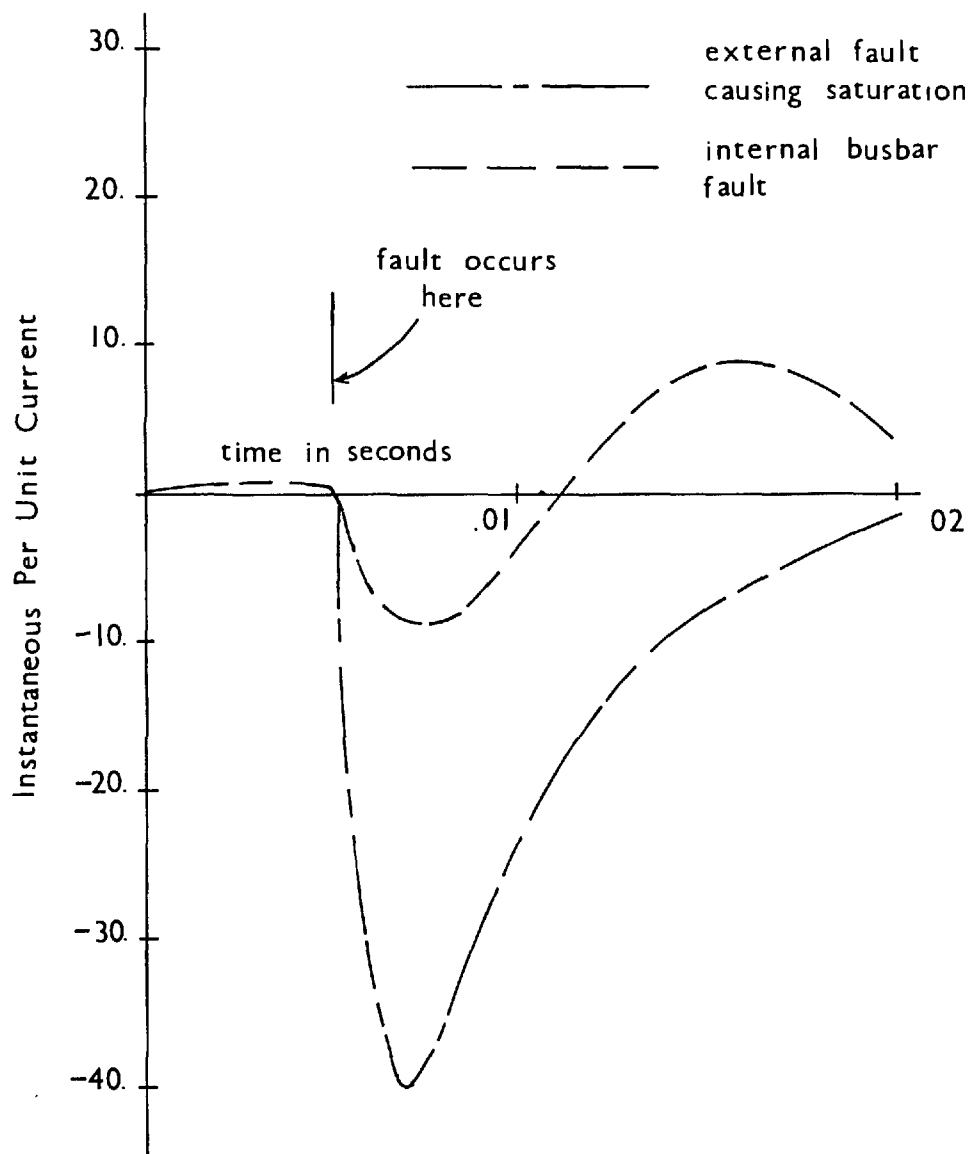


FIGURE 1.7 Secondary Current in CT1

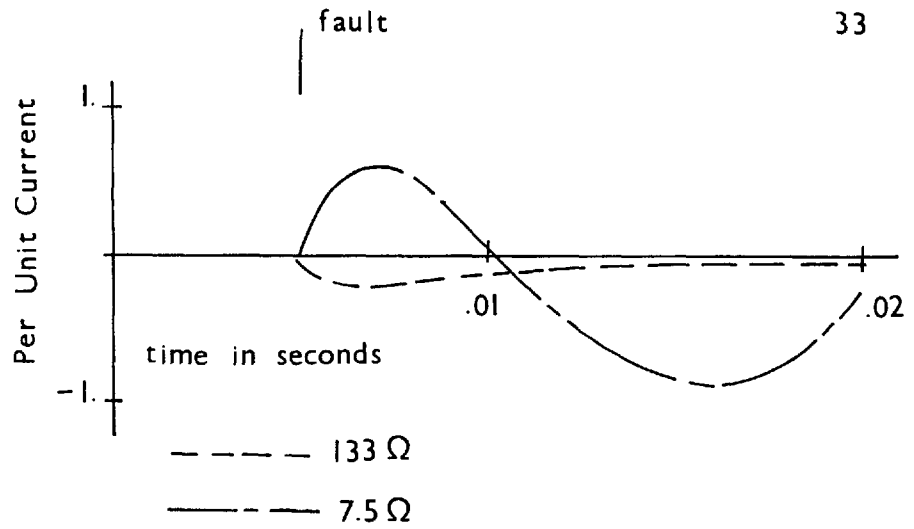


FIGURE 1.8 Stablising Resistance Currents

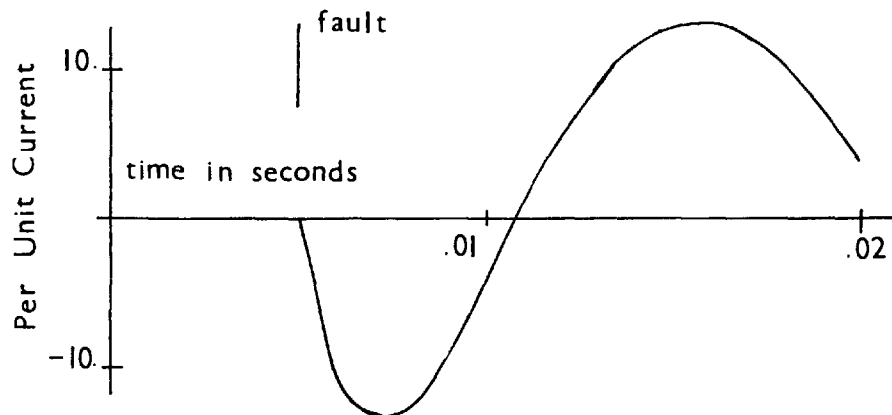


FIGURE 1.9 Protective Relay Current for Internal Fault

system capacity, may be limited. In the development of busbar protection previous investigations have been devoted to the principles of operation of the protective system (60, 62) and CT transient characteristics (15, 57). Although fault detection times are now about two cycles, operating times of from 3 to 6 cycles have been common and the operation of protection equipment has been explained and tested for sustained fault conditions (67). CT transient characteristics are usually studied by the application of 100 percent offset current and are devoted to the application or improvement of CTs.

1.3.2 Busbar Fault Transients

A transient condition between normal and sustained fault must occur rapidly after the occurrence of a fault on a network. If detection time is to be decreased it is necessary to determine the first instant at which the fault can be detected. In order to develop a method of detecting a fault a precise representation of the primary and secondary current and voltage waveforms are needed. The requirements are as follows:

- a) The current and voltage waveforms in all network feeders over the first cycle after the occurrence of a busbar fault
- b) The waveforms for a fault applied at any desired point in a cycle

- c) A method of obtaining, from primary waveforms, the operating instant of present types of protection equipment and of proposed schemes
- d) A representation for a typical substation busbar and feeder network

1.3.3 Transient Study Methods

A practice common in the study of problems in engineering is to develop the complete mathematical theory and then certain simplifying assumptions are made so that these equations can be solved. A physical model is then built in which the complete theory can be represented and the mathematical solution is compared to the result obtained from the physical model. In this way the effect of the assumptions can be determined. However if the solution of the equations do not involve making assumptions the only purposes a physical model serves are to guard against calculating errors or it must give an easier method of solution. If the only physical model which can be built involves more assumptions than other methods of solution it becomes impractical. Some problems dealing with specific equipment in a power network can be investigated by building a physical model but they require a simplified representation when either detail or size must be greatly increased. Because of the difficulties in obtaining the waveforms and the protection operating instant by construction of a physical model other

experimental methods are required.

The values of current and voltage have been determined by the solution of the differential equations of the network. However network equations are, at present, unsolvable without a large number of assumptions which are too sweeping to give a precise reproduction of instantaneous values over the first cycle after a fault. To reduce the number of assumptions these equations can be solved on an analogue computer by using the transforms of two-axis theory of electrical machines, first developed by Park (48) and formulated by Adkins (2). The transforms can be extended to the power network and protection system and this greatly simplifies network and protection system calculations. This method of solution might be compared with an iterative method where the $(n+1)$ value, obtained from the n th value by feedback through an analogue loop, is found by iterating around a numerical loop.

There are nine multiplier units in the Electrical Engineering Department's analogue computer which limits the number of differential equations which can be used as an integral part of the representation. The MIDAS program (51) has been written to allow a digital computer to be used in the same way as an analogue computer. The scope of calculations is greatly increased because a subroutine referenced by a call statement replaces each operational amplifier, multiplier, etc.

1.4 The Switching Controller

1.4.1 Development of the High Voltage Substation

The function of a substation has changed greatly since its conception. Originally substations were used only to convert voltage and frequency to that suitable for utilisation (21). The first electrical networks were direct current. The advantages of static equipment led to the adoption of alternating current for transmission. Substations were required for conversion since generators and loads were direct current. An operator's function was to protect the equipment. The idea of continuity of service has led to the introduction of the double busbar substation which became possible with the development of the circuit breaker. Electric railway breakers were converted by installing overcurrent devices. These breakers were used at the supply end of transmission lines. The first circuit breakers used in substations were 'reversed current circuit breakers' which were complete with tripping devices built in. Breakers were specified for either generating or substation use (65). This arrangement made it theoretically possible to localise faults, limit damage and increase security.

The power network of today consists of a large number of individual or parallel feeders connected to substations which require a great deal of complementary equipment. This equipment has become very complex, and the operator requires aid to adequately control the

modern network. With the new high voltage substation's increased capacity the operator will be faced with increased problems.

1.4.2 Switching and Interlocking

Large substations usually have a control room in which a mimic diagram of the substation switching arrangement is displayed. Hand dressed switches provide remote control of the isolators and circuit breakers. Interlocking of the primary network is used to prevent undesirable or dangerous operation and supervision of the secondary network is used to detect faulty protection equipment (3, 46).

Supervision is used on circulating current protection since open-circuits or short-circuits on CTs or the secondary wiring circuits would upset the balance of current causing unwanted relay operation for a healthy busbar section. Automatic means are used for the detection of such secondary circuit defects and to switch out the protection. Generally a sensitive relay is connected in series or parallel with the protection relay. The presence of current due to secondary defects operate this supervision relay. The removal of protection is delayed to prevent maloperation when faults occur. However it has been known for supervision circuits to render protection inoperative under fault conditions.

Secondary protection circuits must be switched in conjunction with the switching of the protected primary network. Interconnection becomes extensive on double busbars and improper connections can result in open-circuit CT or unbalance because the protection includes a CT on a feeder disconnected from the primary network. To avoid the inadvertent tripping of busbar breakers two complete protection circuits are used. One protection circuit is used on each section of busbar (discriminating group) and a confirmation protection circuit covering the complete busbar installation (check group). The discriminative group is fully discriminative while the check group covers the complete busbar and does not distinguish between faults on different busbar sections. Both the check relay and the section discriminating relay must operate before section breakers are tripped.

In future more switching of the primary network will be required to maintain high security, thus more complex switching operations will be attempted. Switching operations must be considered to operate all switches in one feeder and even groups of feeders from one command. An increase in supervision of system switching will be required as will methods of handling more information concerning the transmission network. Secondary network supervision will have to be simplified.

Many of the protection schemes which are very simple in principle give rapid and accurate indication of the condition of a busbar with respect to faults, but

are unusable because of a single failing. Such schemes could give improved operation if this failing could be overcome. Chapter 7 investigates such schemes. With the inclusion of an adequate system of switching and monitoring their failing can be eliminated.

1.4.3 Logic Methods

Over the past few years devices using high speed logic have been developed and applied to many industrial processes. The use of these devices has increased with the greater understanding of optimum control methods and the design of fast operating and reliable components. Computers are being used to monitor variables, perform calculations, display and store information; and control equipment and output of power stations (59). Electrical transmission and distribution system control has consisted largely of automatic load forecasting dispatching, plant ordering and frequency control (47). However one method of using mathematical logic to describe the switching and interlocking of power system networks and equipment has already been described (16).

A centralised system of substation control would be a desirable development. If this system were complete with a memory unit and a calculating unit capable of great flexibility in operation the scope of possible power system control would be increased. In Chapter 5 one method of simulating switching

arrangements suitable for system switching and monitoring for use in control and protection of electrical networks is developed.

1.5 The Purpose of the Study

The need for high security and reduced fault detection time of the new 400 kV power networks initiated this study.

The thesis describes the development of a digital computer method for the study of busbar fault protection schemes. The results obtained by using this method to study different protection systems for a typical high voltage substation busbar is given. Also a method of determining a simulator, based on logic, to be used for high voltage substation automatic switching is described.

CHAPTER 2

SUBSTATION DIFFERENTIAL EQUATIONS

2.1 General

The differential equations of this chapter form the basis from which the equations for the numerical solutions of busbar and protection circuit waveforms are developed. These equations are rearranged in Chapter 3 for power network simulation by the MIDAS method (51). The theoretical basis for these equations is as follows.

2.1.1 The Operational Equation

The operational equations give the relationship between voltages, currents and flux linkages in a machine. They are the general equations based on two-axis theory. Generally these equations are used for the solution of problems involving symmetrical voltages, however α and β components as given by Concordia (14) have been applied to this type of representation to give a new technique for the determination of variables in an asymmetrically faulted network.

2.1.2 Transformed Equations of Transmission Lines

These equations have been given by Aldred (6). For long transmission lines the differential equations

given by Johnson (29) are transformed.

2.1.3 Protection Circuit Equations

The differential equations which describe the busbar protection equipment for a substation are transformed to two-axis theory equations.

2.2 Per Unit System and Sign Convention

For ease of handling and comparison between generators, loads, transmission lines and protection equipment all primary circuit quantities are reduced to a per unit basis so that the same order of magnitude between quantities from different machines exists. This also greatly reduces the calculation difficulties since, by this arrangement, the complete inductance of a coil is obtained by adding the mutual and leakage inductances. The per unit system adopted is given by Rankin (53). With this definition the unit of power corresponds to unit r.m.s. voltage and r.m.s. current. The unit of speed is given as the radian per second. Thus the unit of torque becomes the torque which produces unit power at nominal speed (54).

Sign conventions are adopted so that the following correlation between electrical and mechanical quantities is followed. Voltage is applied to the terminals and torque is applied to the shaft. Therefore positive voltage and current mean motoring action, and

positive torque and speed mean generating action.

2.3 Assumptions

Park (48) has developed the two-axis theory for an ideal machine with the following generally accepted assumptions.

- a) Per unit mutual inductance for all the coils on one axis are equal.
- b) Complete windings are represented by single coils on each axis.
- c) Zero sequence quantities do not flow in the machine. In this analysis zero sequences in the network are taken as proportional to α components.

2.4 Transformation Formulae

The idealised three phase machine is shown in Figure 2.1. If differential equations are set up for this arrangement inductances vary with θ , the angle of position. The two-axis theory, developed by Park (49,50), makes these differential equations less difficult to solve by replacing phase voltages and currents, $e_a, e_b, e_c, i_a, i_b, i_c$, by the fictitious quantities $e_d, e_q, e_o, i_d, i_q, i_o$ by the following transform.

$$\begin{bmatrix} e_d, i_d \\ e_q, i_q \\ e_o, i_o \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos \theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta - \frac{4\pi}{3}) \\ \sin \theta & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta - \frac{4\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} e_a, i_a \\ e_b, i_b \\ e_c, i_c \end{bmatrix} \quad (2.1)$$

This is the transform from the time plane to the two-axis plane. The parameters e_d, e_q, i_d, i_q are associated with fictitious coils located on the direct and quadrature axes as shown in Figure 2.2.

2.5 Induced Voltage Equation

The equation relating induced voltage, current and flux can be developed for each phase of the machine shown in Figure 2.1. Adkins (2) has given the two-axis equivalent of this equation which forms the basis of the two-axis theory. These equations are as follows.

$$e_d = p \psi_d + v \psi_q + r_a i_d \quad (2.2)$$

$$e_q = -v \psi_d + p \psi_q + r_a i_q \quad (2.3)$$

The quantities e_o and i_o are related to each other independently of the axis quantities. The voltages e_d and e_q can be physically interpreted as impressed voltages on the direct and quadrature axes coils of Figure 2.2. With this interpretation, the two-axis machine in Figure 2.2 can be regarded as the equivalent of the three phase machine in Figure 2.1 in the two-axis

plane.

2.6 Direct and Quadrature Axis Equations

The equations for the system of stationary mutually coupled coils of Figure 2.2 can be written for each axis in terms of their individual currents, flux linkages and mutual and self inductances.

The direct axis equations are as follows.

$$\psi_d = L_{md} i_f + L_{md} i_{kd} + (L_{md} + \ell_a) i_d \quad (2.4)$$

$$e_f = [r_f + (L_{md} + \ell_f) p] i_f + L_{md} p i_{kd} + L_{md} p i_d \quad (2.5)$$

$$e_{kd} = L_{md} p i_f + (r_{kd} + L_{kd} p) i_{kd} + L_{md} p i_d \quad (2.6)$$

Similarly the quadrature axis equations are as follows.

$$\psi_q = L_{mq} i_{kq} + (L_{mq} + \ell_a) i_q \quad (2.7)$$

$$e_{kq} = (r_{kq} + L_{kq} p) i_{kq} + L_{mq} p i_q \quad (2.8)$$

The damper windings KD and KQ are short circuited as in Figure 2.2 and therefore

$$e_{kd} = e_{kq} = 0 \quad (2.9)$$

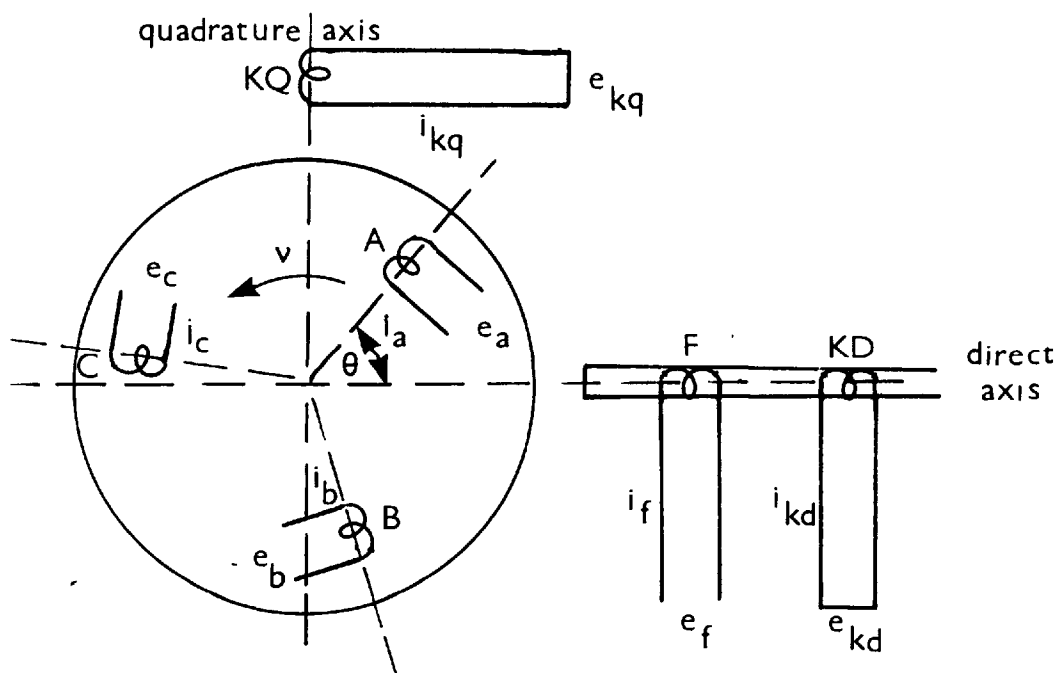


FIGURE 2.1 Idealised Synchronous Machine

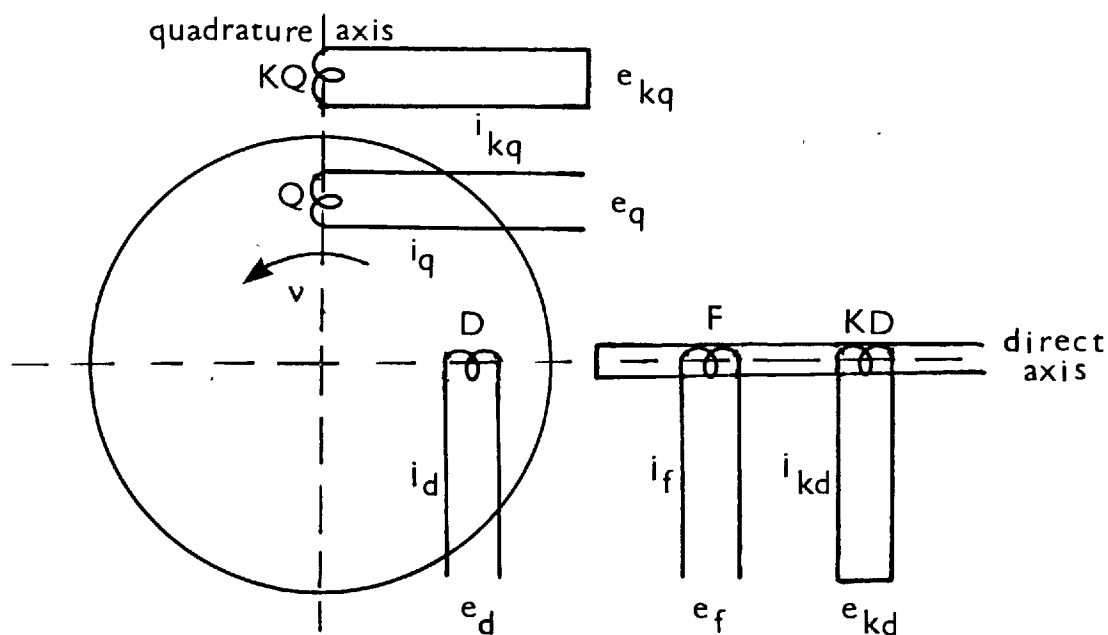


FIGURE 2.2 Two Axis Equivalent Machine Representation

2.7 The Operational Impedances

By eliminating i_f and i_{kd} from the direct axis equations ψ_d may be expressed in the following form.

$$\psi_d = \left[\frac{1 + (T_4 + T_5) p + T_4 T_6 p^2}{1 + (T_1 + T_2) p + T_1 T_3 p^2} \right] L_d i_d + \left[\frac{1 + T_{kd} p}{1 + (T_1 + T_2) p + T_1 T_3 p^2} \right] \frac{L_{md}}{r_f} e_f \quad (2.10)$$

which can be put in the form

$$\psi_d = \frac{x_d(p)}{\omega} i_d + \frac{G(p)}{\omega} e_f \quad (2.11)$$

Similarly by eliminating i_{kq} from the quadrature axis equations ψ_q is expressed in the following form.

$$\psi_q = \frac{1 + T_q'' p}{1 + T_{q0}'' p} L_q i_q \quad (2.12)$$

$$= \frac{x_q(p)}{\omega} i_q \quad (2.13)$$

The functions $x_d(p)$ and $x_q(p)$ are called operational impedances.

The time constants are defined as follows (2).

$$T_1 = T'_{do} = \frac{1}{\omega r_f} (x_{md} + x_f)$$

direct-axis transient open-circuit time constant,

$$T_2 = \frac{1}{\omega r_{kd}} (x_{md} + x_{kd}),$$

$$T_3 = T''_{do} = \frac{1}{\omega r_{kd}} x_{kd} + \frac{x_{md} x_f}{x_{md} + x_f}$$

direct-axis subtransient open-circuit time constant,

$$T_4 = T'_d = \frac{1}{\omega r_f} x_f + \frac{x_{md} x_a}{x_{md} + x_a}$$

direct-axis transient short-circuit time constant,

$$T_5 = \frac{1}{\omega r_{kd}} x_{kd} + \frac{x_{md} x_a}{x_{md} + x_a},$$

$$T_6 = T''_d = \frac{1}{\omega r_{kd}} x_{kd} + \frac{x_{md} x_f x_a}{x_{md} x_a + x_{md} x_f + x_a x_f}$$

direct-axis subtransient short-circuit time constant,

$$T_{kd} = \frac{x_{kd}}{\omega r_{kd}}$$

direct-axis damper leakage time constant,

$$T_q'' = \frac{1}{\omega r_{kq}} x_{kq} + \frac{x_{mq} x_a}{x_{mq} + x_a}$$

quadrature - axis subtransient short - circuit time constant,

$$T_{qo}'' = \frac{1}{\omega r_{kq}} (x_{kq} + x_{mq})$$

quadrature - axis subtransient open - circuit time constant.

The general method of obtaining the solution for these equations is to assume that since T_1 is much greater than T_2 or T_3 , T_2 can be taken as equal to T_3 (2). Since T_3 may be approximately equal to four times T_2 this method has not been used here. T_2 is approximately 10 cycles and covers the duration of the proposed study. Similarly T_5 is generally taken as equal to T_6 . T_5 covers 1 cycle. The method used here enables the instantaneous values to be found without the assumptions required in the analytical technique.

2.8 The Torque Equation

Power in a machine represents ohmic loss, rate of change of magnetic energy and output power corresponding to electrical torque. This torque is developed by the interaction of flux and current which is given by the following equation.

$$P_e = \frac{\omega}{2} (\psi_q i_d - \psi_d i_q) \quad (2.14)$$

Per unit electrical torque is given by

$$T_e = - P_e \frac{\omega}{v} = \frac{\omega}{2} (\psi_d i_q - \psi_q i_d) \quad (2.15)$$

It differs from the externally applied mechanical torque by an acceleration component.

By introducing a reference axis and an angle δ the machine rotor position can be determined and changes in speed can be represented. The position of the reference axis at any instant is given by

$$\theta_r = \omega t \quad . \quad (2.16)$$

The rotor position is

$$\theta = \omega t - \delta + \lambda \quad . \quad (2.17)$$

Speed is obtained by differentiating this equation

$$v = \omega - p \delta \quad (2.18)$$

The acceleration is

$$\frac{d^2}{dt^2} \theta = - p^2 \delta \quad (2.19)$$

The acceleration torque is

$$J \frac{d^2}{dt^2} \theta \quad .$$

In the per unit system the moment of inertia of a machine is expressed by the inertia constant denoted H and the following relationship exists (2).

$$J = \frac{2H}{\omega} \quad (2.20)$$

So that the acceleration torque becomes

$$- \frac{2H}{\omega} p^2 \delta$$

The mechanical torque (T_t) of the prime mover or load is affected by the speed governors and speed torque curve, however over one cycle it is assumed that this torque will be constant. The program is arranged such that this torque can be easily modified. The torque equation is

$$\frac{2H}{\omega} p^2 \delta = - \frac{\omega}{2} (\psi_d i_q - \psi_q i_d) + T_t \quad (2.21)$$

2.9 Transmission Line Equation

If transmission lines are included in this power system network representation it is necessary to transform the differential equations describing the lines into two axis components to conform with the representation of machines and loads. The conventional representation of a transmission line used in stability studies consists of lumped parameters and is shown in

Figure 2.3.

The transmission line equations are as follows.

$$e_r = e_s - Z i_s \quad (2.22)$$

$$i_s = i_r + Y e_r \quad (2.23)$$

With the assumption for short lines that

$$Y = 0 \quad (2.24)$$

the equations become

$$i_s = i_r \quad (2.25)$$

$$e_r = e_s - Z i_r \quad (2.26)$$

If $Z = r_e + \ell_e p \quad (2.27)$

then $e_r = e_s - r_e i_r - \ell_e p i_r \quad (2.28)$

Transforming this equation for phase a, b, and c the direct and quadrature axis components are as follows.

$$e_d^* = -r_e i_d - \ell_e p i_d - x_e i_q + e_d \quad (2.29)$$

$$e_q^* = -r_e i_q - \ell_e p i_q + x_e i_d + e_q \quad (2.30)$$

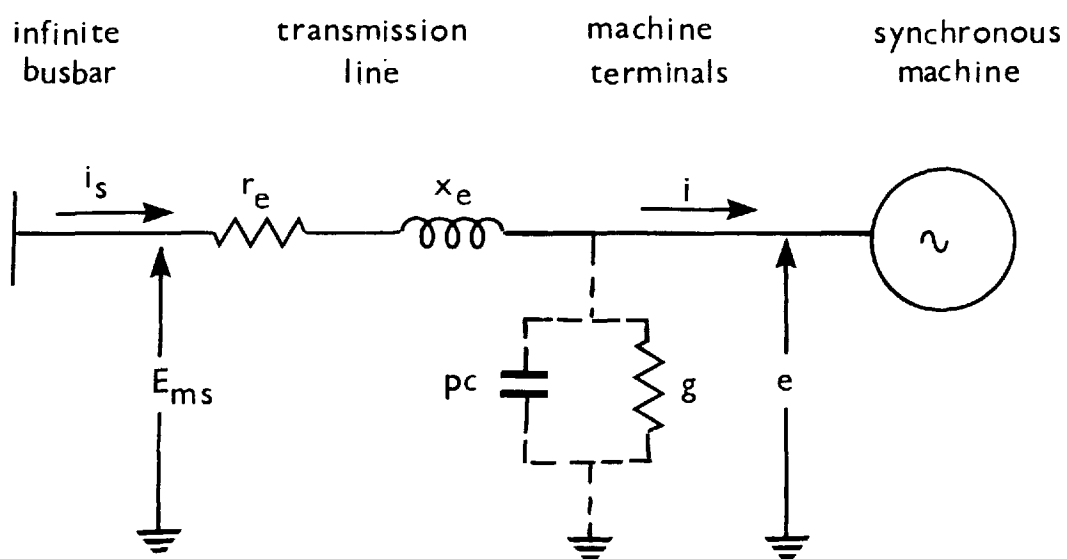


FIGURE 2.3 Representation of Network Arrangement

Aldred (6) has neglected the transient term of $\ell_e p i_d$ and $\ell_e p i_q$. However for this representation the transient terms are required.

The above representation is used for short transmission lines, however for long lines the shunt branch is not neglected. The shunt branch is included by the following representation.

$$Y = g + c.p \quad (2.31)$$

The line equations with this substitution are as follows.

$$i_s = i_r + g e_s + c p e_s - r g i_s - r c p i_s - g \ell p i_s - c \ell p^2 i_s \quad (2.32)$$

and

$$e_r = e_s - r i_r - \ell p i_r - r g e_r - (r c + g \ell) p e_r - c \ell p^2 e_r \quad (2.33)$$

Substituting Equation (2.1) into Equation (2.32) and expanding with the p operator this equation becomes

$$\begin{aligned} i_{ds} \cos \theta + i_{qs} \sin \theta &= i_{dr} \cos \theta + i_{qr} \sin \theta + g e_{ds} \cos \theta \\ &+ g e_{qs} \sin \theta + c p e_{ds} \cos \theta - \omega c e_{ds} \sin \theta \\ &+ c p e_{qs} \sin \theta + \omega c e_{qs} \cos \theta - r g i_{ds} \cos \theta - r g i_{qs} \sin \theta \\ &- (r c + g \ell) p i_{ds} \cos \theta + (r c + g \ell) \omega i_{ds} \sin \theta \\ &- (r c + g \ell) p i_{qs} \sin \theta - (r c + g \ell) \omega i_{qs} \cos \theta \end{aligned}$$

$$\begin{aligned}
& - c \ell p^2 i_{ds} \cos \theta + 2 c \ell \omega p i_{ds} \sin \theta + c \ell \omega^2 i_{ds} \cos \theta \\
& - c \ell p^2 i_{qs} \sin \theta - 2 c \ell \omega p i_{qs} \cos \theta + c \ell \omega^2 i_{qs} \sin \theta
\end{aligned}
\tag{2.34}$$

Similarly Equation (2.33) becomes

$$\begin{aligned}
e_{dr} \cos \theta + e_{qr} \sin \theta &= e_{ds} \cos \theta + e_{qs} \sin \theta - r i_{dr} \cos \theta \\
& - r i_{qr} \sin \theta - \ell p i_{dr} \cos \theta + \omega \ell i_{dr} \sin \theta \\
& - \ell p i_{qr} \sin \theta - \omega \ell i_{qr} \cos \theta - r g e_{dr} \cos \theta \\
& - r g e_{qr} \sin \theta - (rc + g\ell) p e_{dr} \cos \theta + (rc + g\ell) \omega e_{dr} \sin \theta \\
& - (rc + g\ell) p e_{qr} \sin \theta - (rc + g\ell) \omega e_{qr} \cos \theta \\
& - c \ell p^2 i_{dr} \cos \theta + 2 c \ell \omega p e_{dr} \sin \theta \\
& + c \ell \omega^2 e_{dr} \cos \theta - c \ell p^2 e_{qr} \sin \theta - 2 c \ell \omega p e_{qr} \cos \theta \\
& + c \ell \omega^2 e_{qr} \sin \theta
\end{aligned}
\tag{2.35}$$

2.10 Circulating Current Protection System

The impedance to the e.m.f. of a CT secondary in a circulating current system depends upon the primary current in each CT. To determine the relay current the secondary current from each CT is required. In Section 3.2.7 the equation for the current in each

CT is given. In this section the differential equation in terms of all primary and secondary current in one CT only is developed.

A simplified circulating current system with two current transformers is shown in Figure 1.2. The equation for the n^{th} current transformer currents is as follows.

$$Lp I_n + (r_s + \ell p) i_n + \sum_{n=1}^N i_n R = 0 \quad (2.36)$$

where

$$\ell = L + \ell_s \quad (2.37)$$

The $(n+1)^{\text{th}}$ current transformer equation is

$$Lp I_{n+1} + (r_s + \ell p) i_{n+1} + \sum_{n=1}^N i_n R = 0 \quad (2.38)$$

Subtracting Equation (2.38) from Equation (2.36) gives

$$Lp (I_n - I_{n+1}) + (r_s + \ell p) (i_n - i_{n+1}) = 0 \quad (2.39)$$

Continue by substituting all remaining n current transformer equations in Equation (2.38) and adding equations of the form of Equation (2.36) to obtain the following equation

$$L_p N I_n - \sum_{n=1}^N L_p I_n + (r_s + \ell_p)(N i_n - \sum_{n=1}^N i_n) \quad (2.40)$$

and solve for $\sum_{n=1}^N i_n$

$$\sum_{n=1}^N i_n = \frac{L_p N I_n}{(r_s + \ell_p)} - \frac{\sum_{n=1}^N L_p I_n}{(r_s + \ell_p)} + N i_n \quad (2.41)$$

Substitute Equation (2.41) into Equation (2.36) to get

$$L_p I_n + (r_s + \ell_p) i_n + \frac{R L_p N I_n}{(r_s + \ell_p)} - \frac{R \sum_{n=1}^N L_p I_n}{(r_s + \ell_p)} + R i_n = 0 \quad (2.42)$$

This is the equation for the n^{th} CT in terms of its secondary current and the primary currents.

CHAPTER 3

SUBSTATION SIMULATION EQUATIONS

3.1 General

It has already been noted in Chapter 1 that the assumptions made for an analytical solution to determine current and voltage waveforms are difficult to justify for a transient study. In the method explained in this chapter the number of assumptions is limited to those inherent in the basic theory. This method also has advantages over the laboratory model method in that it is much more versatile in the representation of individual components and operating conditions and permits accurately timed switching operations in the development of short-circuit waveforms.

3.2 Formulation of the Equations

The form of the equations derived in Chapter 2 must be modified for the MIDAS method of solution. In this program differentiation in a loop causes instability in iteration as do loops without an integrator, therefore all loops must include at least one integrator. The MIDAS form of the foregoing two-axis equation is as follows.

3.2.1 Fundamental Equations

By substituting Equation (2.18) in Equations

(2.2) and (2.3) and rearranging, the following form is obtained.

$$p \psi_d = e_d - r_a i_d - \omega \psi_q + \psi_q p \delta \quad (3.1)$$

$$p \psi_q = e_q - r_a i_q + \omega \psi_d - \psi_d p \delta \quad (3.2)$$

The MIDAS representations of Equations (3.1) and (3.2) are given in Figures 3.1 and 3.2 respectively. The three left hand terms in each of these figures give a modification developed in Section 3.2.6 for the inclusion of a transmission line. With RE, XE and LE equal to zero the figures give the solution to Equations (3.1) and (3.2).

3.2.2 Direct Axis Current Equation

The operational impedance equation, Equation (2.10), can be expressed in the following form (42).

$$\psi_d = L_d i_d + \psi_{d1} + \psi_{d2} \quad (3.3)$$

where

$$\psi_{d1} = \frac{L_d (A_{d1} p i_d + \alpha_{d1} B_{d1} e_f)}{p + \alpha_{d1}} \quad (3.4)$$

and

$$\psi_{d2} = \frac{L_d (A_{d2} p i_d + \alpha_{d2} B_{d2} e_f)}{p + \alpha_{d2}} \quad (3.5)$$

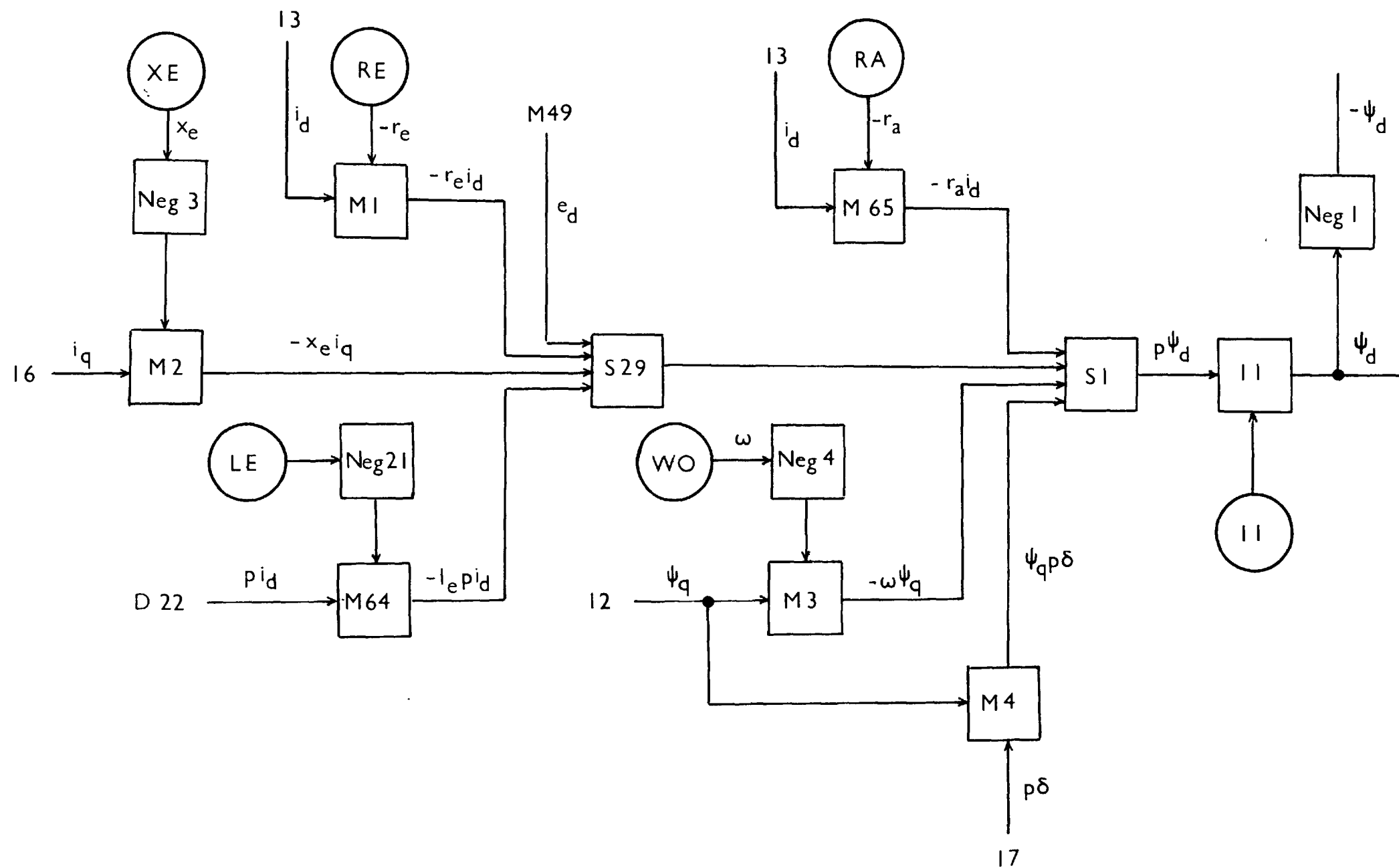


FIGURE 3.1 Fundamental Equation for Direct Axis with Transmission Line

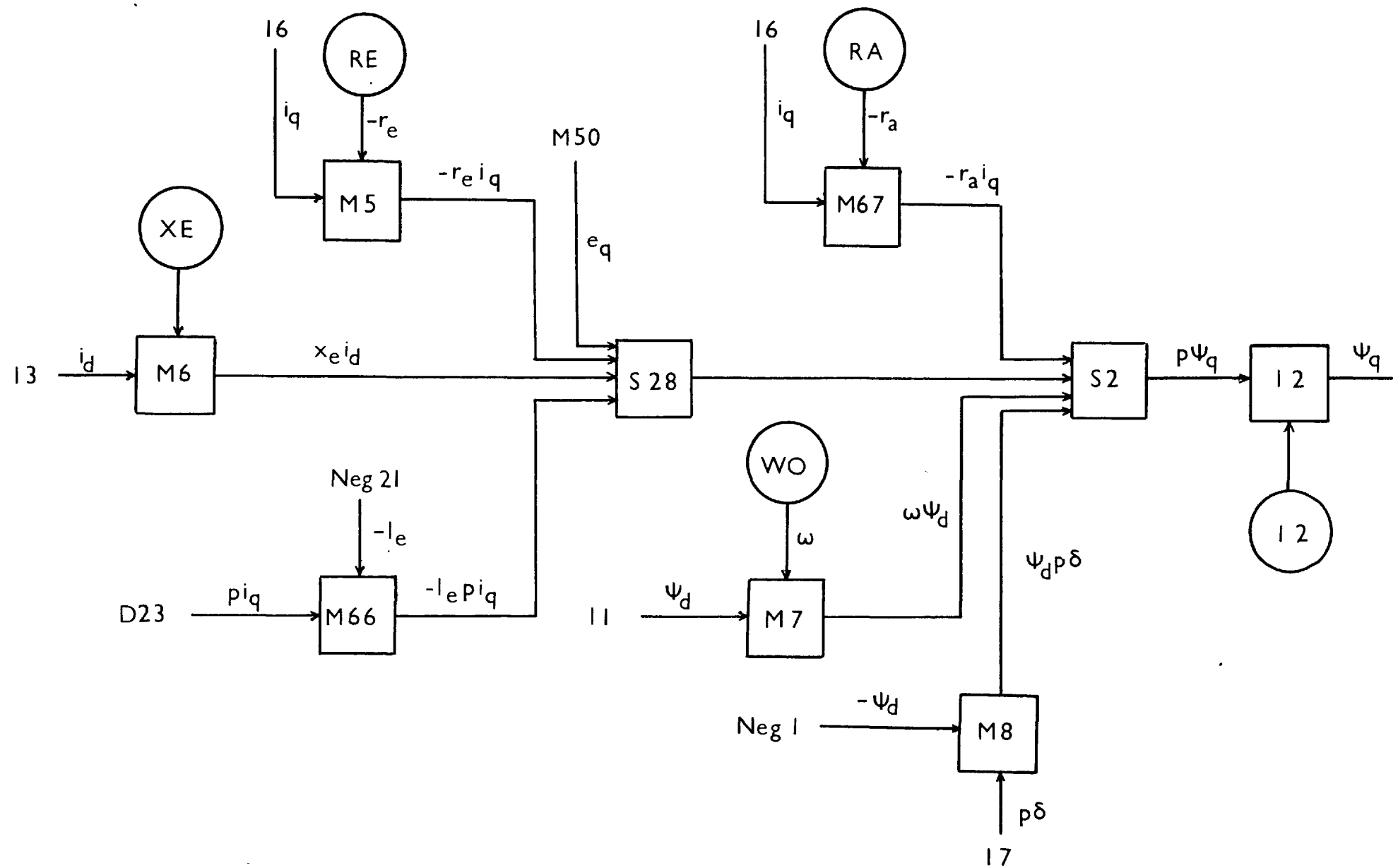


FIGURE 3.2 Fundamental Equation for Quadrature Axis with Transmission Line

Equation (3.4) can be expanded by division as follows.

$$\psi_{d1} = L_d A_{d1} i_d + \frac{L_d B_{d1} \alpha_{d1} e_f}{p} - \frac{L_d \alpha_{d1} (A_{d1} p i_d + \alpha_{d1} B_{d1} e_f)}{p(p + \alpha_{d1})} \quad (3.6)$$

Thus substituting Equation (3.4) in Equation (3.6)

$$\psi_{d1} = L_d A_{d1} i_d - \frac{\alpha_{d1} (\psi_{d1} - L_d B_{d1} e_f)}{p} \quad (3.7)$$

Similarly Equation (3.5) can be expanded and resubstitution gives

$$\psi_{d2} = L_d A_{d2} i_d - \frac{\alpha_{d2} (\psi_{d2} - L_d B_{d2} e_f)}{p} \quad (3.8)$$

By adding Equations (3.7) and (3.8) and substituting in Equations (3.3) and (2.11) the following equation is obtained.

$$\psi_{d1} + \psi_{d2} = \frac{x_d(p)}{\omega} - \frac{x_d}{\omega} i_d + \frac{G(p)}{\omega} e_f \quad (3.9)$$

Alternative forms of $\frac{x_d(p)}{\omega}$, $\frac{G(p)}{\omega}$ and $\frac{x_q(p)}{\omega}$ are given by Malik (42) and are as follows.

$$\frac{x_d(p)}{\omega} = L_d - \frac{(r_f + r_{kd})p + (\ell_f + \ell_{kd})p^2}{r_f r_{kd} + (r_{kd} L_f + r_f L_{kd})p + (\ell_f L_{kd} + \ell_{kd} L_{md})p^2} L_{md} \quad (3.10)$$

$$\frac{G(p)}{\omega} = \frac{r_{kd} + \ell_{kd} p}{r_f r_{kd} + (r_{kd} L_f + r_f L_{kd})p + (\ell_f L_{kd} + \ell_{kd} L_{md})p^2} L_{md} \quad (3.11)$$

$$\frac{x_q(p)}{\omega} = L_q - \frac{L_{mq}^2 p}{r_{kq} + (\ell_{kq} + L_{mq})p} \quad (3.12)$$

Dividing the denominator of Equations (3.10) and (3.11) by $(\ell_f L_{kd} + \ell_{kd} L_{md})$ and equating to zero, the following expression is obtained.

$$p^2 + \frac{(r_{kd} L_f + r_f L_{kd})}{(\ell_f L_{kd} + \ell_{kd} L_{md})} p + \frac{r_f r_{kd}}{(\ell_f L_{kd} + \ell_{kd} L_{md})} = 0 \quad (3.13)$$

which can be factorised. From this the coefficients of Equations (3.7) and (3.8) are as follows.

$$\alpha_{d1}, \alpha_{d2} = \frac{(T_1 + T_2) \pm (T_1^2 + T_2^2 - 2T_1 T_2 + 4L_{md}^2 / r_f r_{kd})^{1/2}}{2T_1 T_2} \quad (3.14)$$

Time constants are defined in Section 2.7

$$A_{d1} = - \frac{(x_d - x_d') \alpha_{d1}}{x_d (\alpha_{d1} - \alpha_{d2})} + \frac{x_{md}^2 (r_f + r_{kd})}{\omega x_d r_f r_{kd} (\alpha_{d1} - \alpha_{d2}) T_1 T_2} \quad (3.15)$$

$$A_{d2} = \frac{(x_d - x_d'') \alpha_{d2}}{x_d (\alpha_{d1} - \alpha_{d2})} - \frac{x_{md}^2 (r_f + r_{kd})}{\omega x_d r_f r_{kd} (\alpha_{d1} - \alpha_{d2}) T_1 T_2} \quad (3.16)$$

$$B_{d1} = \frac{x_{md}(\alpha_{d1}T_{kd} - 1)}{x_d(\alpha_{d1} - \alpha_{d2})T_1T_3\alpha_{d1}r_f} \quad (3.17)$$

$$B_{d2} = \frac{x_{md}(-\alpha_{d2}T_{kd} + 1)}{x_d(\alpha_{d1} - \alpha_{d2})T_1T_3\alpha_{d2}r_f} \quad (3.18)$$

Rearranging Equation (3.3) the direct axis current equations can be written

$$i_d = \frac{\omega}{x_d} (\psi_d - \psi_{d1} - \psi_{d2}) \quad (3.19)$$

Substituting Equations (3.7) and (3.8) in Equation (3.19)

$$\begin{aligned} i_d = \frac{1}{1 + A_{d1} + A_{d2}} & \left[\frac{\psi_d}{L_d} + \frac{\alpha_{d1} + \alpha_{d2}}{L_d} \frac{\psi_d}{p} + \frac{\alpha_{d1}\alpha_{d2}}{L_d} \frac{\psi_d}{p^2} \right. \\ & - (\alpha_{d1} + \alpha_{d2} + A_{d1}\alpha_{d2} + A_{d2}\alpha_{d1}) \frac{i_d}{p} - (\alpha_{d1}B_{d1} + \alpha_{d2}B_{d2}) \frac{e_f}{p} \\ & \left. - (\alpha_{d1}\alpha_{d2}) \frac{i_d}{p^2} - (\alpha_{d1}\alpha_{d2})(B_{d1} + B_{d2}) \frac{e_f}{p^2} \right] \quad (3.20) \end{aligned}$$

Differentiating Equation (3.20) and eliminating the closed loop term

$$\frac{p \psi_d}{L_d}$$

to obtain the rate of change of current required for

network representation the rate of change of direct axis current is as follows.

$$\begin{aligned}
 p i_d = & \frac{1}{1 + A_{d1} + A_{d2} + \frac{\ell_e}{L_d}} \left[\frac{p \psi_d^*}{L_d} + \frac{\alpha_{d1} + \alpha_{d2}}{L_d} \psi_d + \frac{\alpha_{d1} \alpha_{d2}}{L_d} \frac{\psi_d}{p} \right. \\
 & - (\alpha_{d1} + \alpha_{d2} + A_{d1} \alpha_{d2} + A_{d2} \alpha_{d1}) i_d - (\alpha_{d1} B_{d1} + \alpha_{d2} B_{d2}) e_f \\
 & \left. - (\alpha_{d1} \alpha_{d2}) \frac{i_d}{p} - (\alpha_{d1} \alpha_{d2}) (B_{d1} + B_{d2}) \frac{e_f}{p} \right] \quad (3.21)
 \end{aligned}$$

where $p \psi_d^*$ differs from $p \psi_d$ of Equation (3.1) in the term e_d , which is developed in Section 3.2.6.

The MIDAS representation of this expression is given in Figures 3.3 and 3.4.

3.2.3 Quadrature Axis Current Equation

Substituting Equation (3.12) into Equation (2.13) the operational equation of the quadrature axis is as follows.

$$\psi_q = \left[L_q - \frac{L_{mq}^2 p}{r_{kq} + (L_{mq} + \ell_{kq}) p} \right] i_q \quad (3.22)$$

Again dividing numerator and denominator by $(L_{mq} + \ell_{kq})$ and then expanding by division with

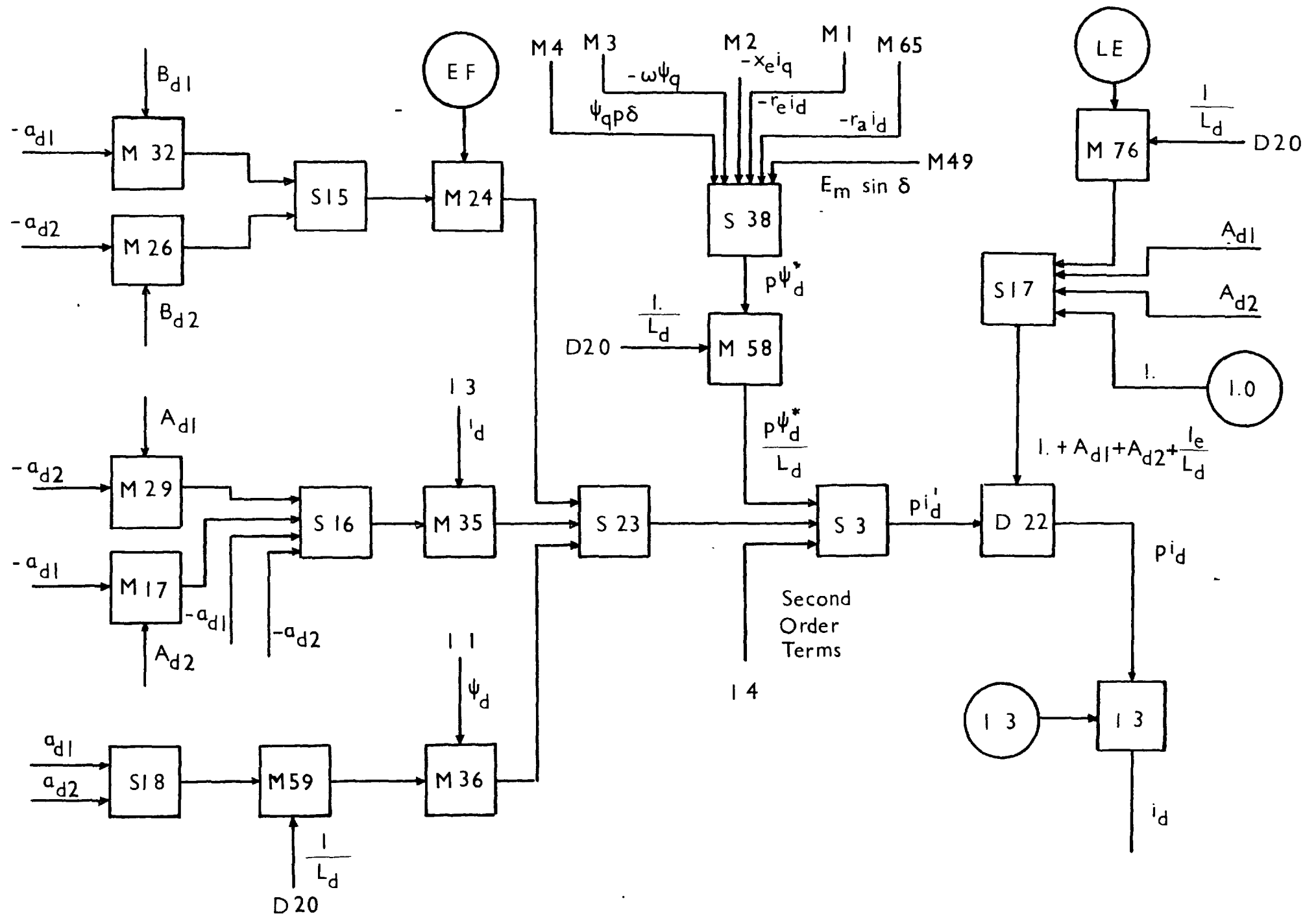


FIGURE 3.3 Direct Axis Current Equation

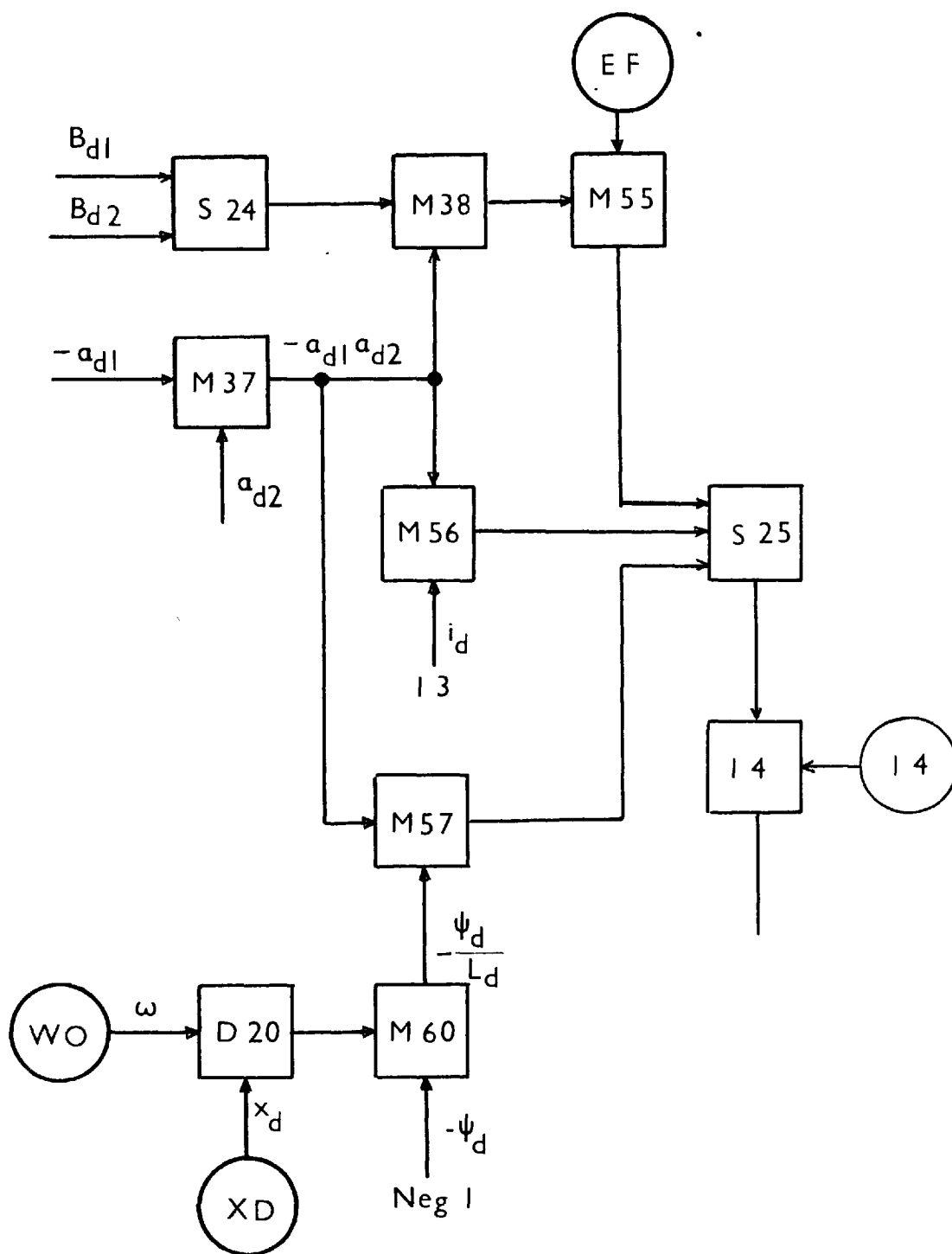


FIGURE 3.4 Second Order Terms of Direct Axis Equation

$$p + \frac{r_{kq}}{(L_{mq} + \ell_{kq})} ,$$

Equation (3.22) becomes

$$\psi_q = \left[L_q - \frac{L_{mq}^2}{(L_{mq} + \ell_{kq})} + \frac{r_{kq}}{(L_{mq} + \ell_{kq})p} \frac{L_{mq}^2 p}{r_{kq} + (L_{mq} + \ell_{kq})p} \right] i_q \quad (3.23)$$

By definition

$$L_q - \frac{L_{mq}^2}{(L_{mq} + \ell_{kq})} = \ell_a + \frac{L_{mq} \ell_{kq}}{(L_{mq} + \ell_{kq})} = \frac{x_q''}{\omega} \quad (3.24)$$

By addition and subtraction of the term

$$\frac{r_{kq} L_q}{(L_{mq} + \ell_{kq})p}$$

and substituting in Equation (3.24), Equation (3.23) becomes

$$\psi_q = \frac{x_q''}{\omega} i_q - \frac{1}{T_{q0}''} \frac{\psi_q}{p} + \frac{x_q}{\omega T_{q0}''} \frac{i_q}{p} \quad (3.25)$$

Rearrangement of this equation gives the quadrature axis current equation.

$$i_q = \frac{\omega}{x_q''} \psi_q + \frac{\omega}{x_q'' T_{qo}''} \frac{\psi_q}{p} - \frac{x_q}{x_q'' T_{qo}''} \frac{i_q}{p} \quad (3.26)$$

Since the rate of change of quadrature axis current is required, differentiating Equation (3.26) gives

$$p i_q = \frac{1}{1 + \frac{\omega \ell_e}{x_q''}} \left[\frac{\omega}{x_q''} p \psi_q^* + \frac{\omega}{x_q'' T_{qo}''} \psi_q - \frac{x_q}{x_q'' T_{qo}''} i_q \right] \quad (3.27)$$

where $p \psi_q^*$ differs from the closed loop term $p \psi_q$ of Equation (3.2) in the term e_q which is developed in Section 3.2.6.

The MIDAS representation of Equation (3.27) is given in Figure 3.5.

3.2.4 Load Angle Equation

The torque equation, Equation (2.21), can be rearranged to give the machine load angle

$$p^2 \delta = - \frac{\omega^2}{4H} (\psi_d i_q - \psi_q i_d) + \frac{\omega}{2H} T_t \quad (3.28)$$

See Figure 3.6 for the MIDAS representation of Equation (3.28).

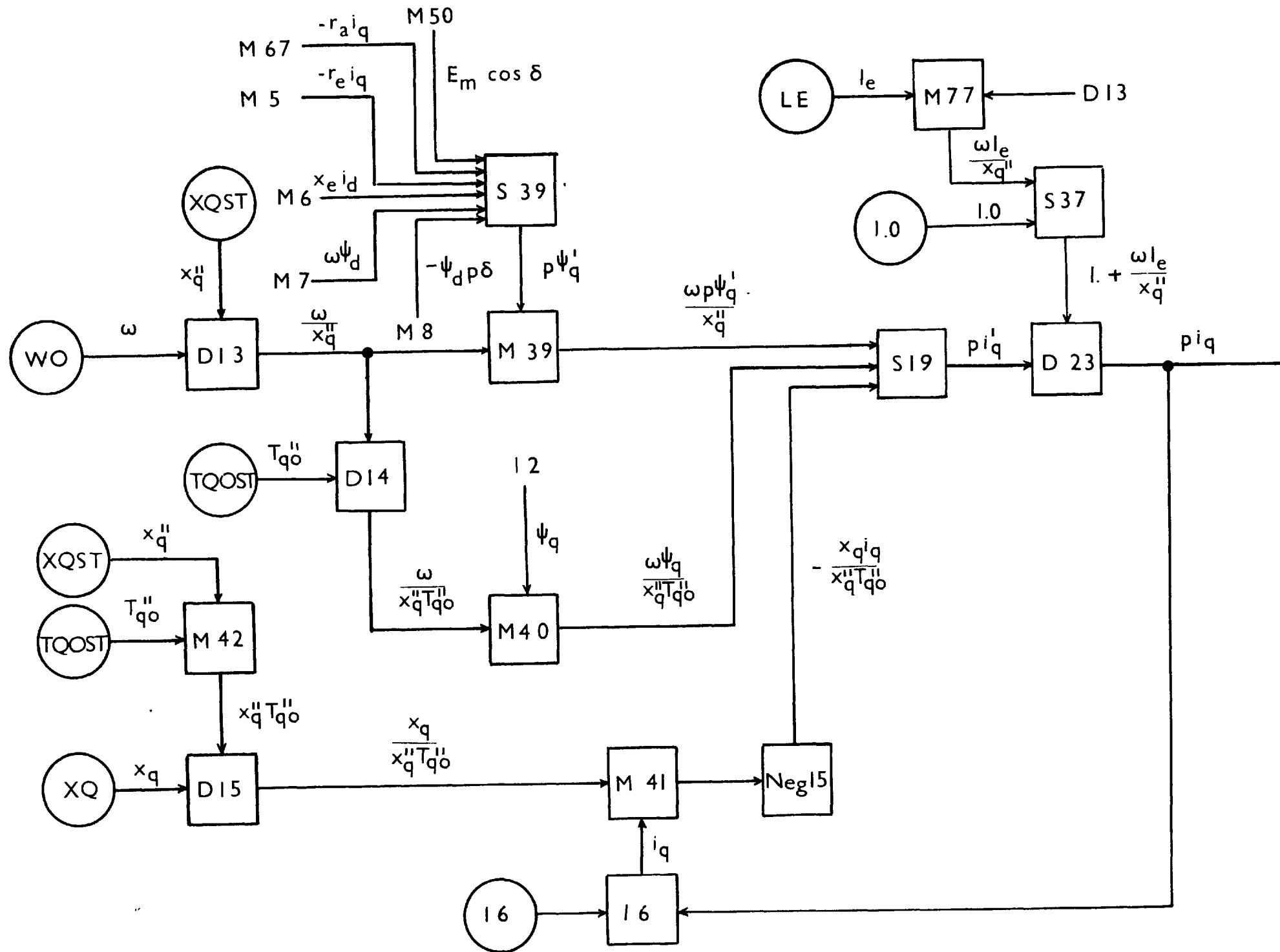


FIGURE 3.5 Quadrature Axis Current Equation

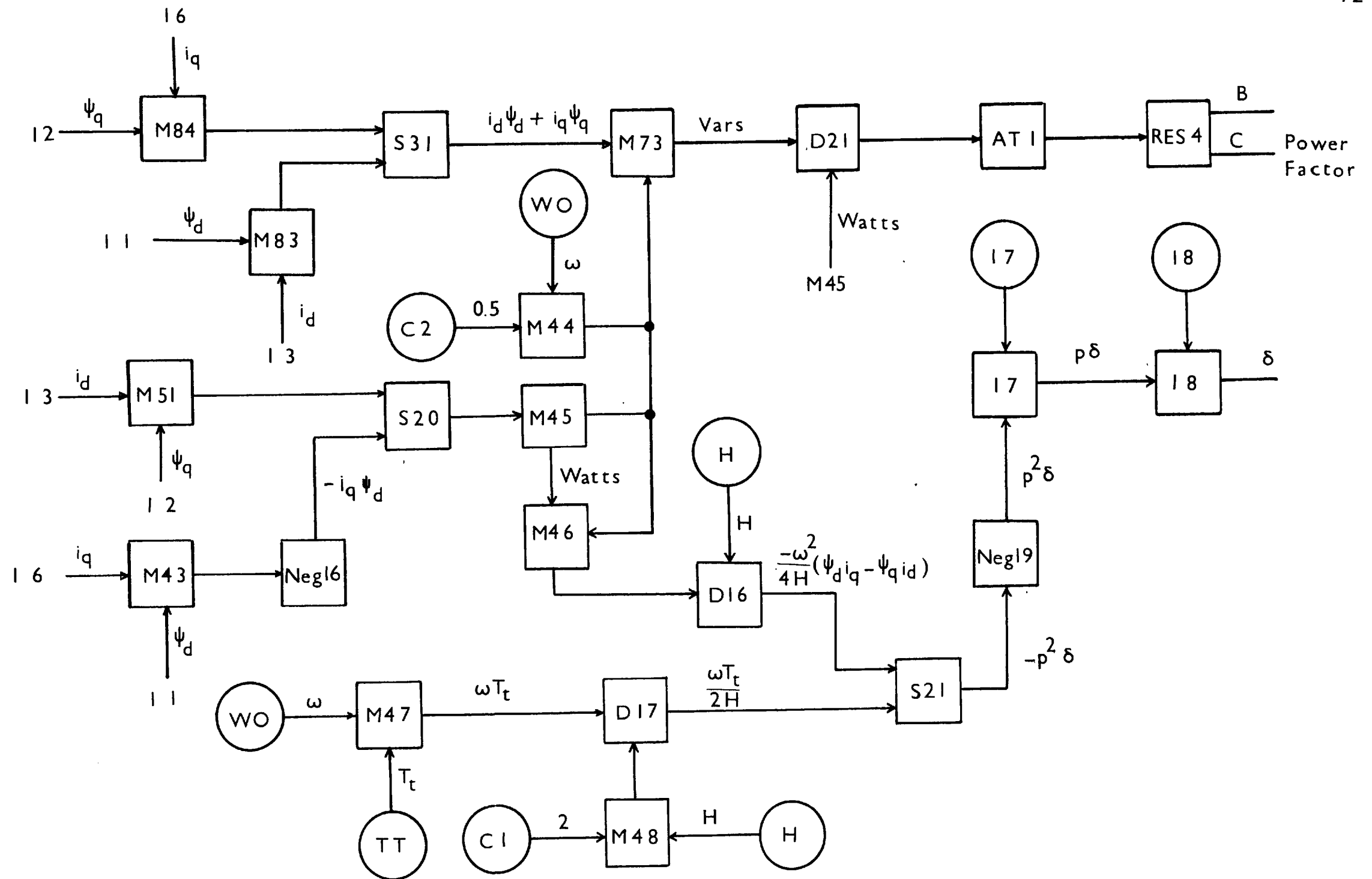


FIGURE 3.6 Load Angle Equation

3.2.5 Power, VARs and Power Factor

Machine power is given in Equation (2.14). This relates to the busbar of Figure 2.3 by Equations (2.2), (2.3) and (2.18) to give

$$P = \frac{1}{2} (e_d i_d + e_q i_q) \quad (3.29)$$

The equation for machine VARs for constant speed, Equation (2.18), is as follows.

$$\text{VAR}_e = \frac{\omega}{2} (\psi_d i_d + \psi_q i_q) \quad (3.30)$$

with busbar VARs again obtained by Equations (2.2), (2.3) and (2.18) to give

$$\text{VAR} = \frac{1}{2} (e_d i_q - e_q i_d) \quad (3.31)$$

Power factor at the busbar is obtained from Equations (3.29) and (3.31) as follows.

$$\text{PF} = \cos(\arctan(\text{VAR}/P)) \quad (3.32)$$

3.2.6 Short and Long Transmission Line Equations

The fundamental equations, Equations (3.1) and (3.2), can be combined with the short transmission line equations, Equations (2.29) and (2.30), to obtain a

modified fundamental equation which includes the transmission line. The overall equations are as follows.

$$p \psi_d = e_d - (r_a + r_e) i_d - \ell_e p i_d - x_e i_q - \omega \psi_q + \psi_q p \delta \quad (3.33)$$

and

$$p \psi_q = e_q - (r_a + r_e) i_q - \ell_e p i_q + x_e i_d + \omega \psi_d - \psi_d p \delta \quad (3.34)$$

since $\ell_e p i_d$ and $\ell_e p i_q$ are closed loop terms they have been eliminated under Section 3.2.2 by using attenuation terms. See Figures 3.1 and 3.2. Equations (3.33) and (3.34) become

$$p \psi_d^* = e_d - (r_a + r_e) i_d - x_e i_q - \omega \psi_q + \psi_q p \delta \quad (3.35)$$

and

$$p \psi_q^* = e_q - (r_a + r_e) i_q + x_e i_d + \omega \psi_d - \psi_d p \delta \quad (3.36)$$

For long transmission line equations the terms for each axis voltage are collected from Equation (2.35) and dividing by p^2 to obtain

$$e_{dr} = \frac{1}{c\ell} \left[\frac{e_{ds}}{p^2} + (c\ell\omega^2 - 1 - rg) \frac{e_{dr}}{p^2} - r \frac{i_{dr}}{p^2} - (rc + g\ell) \omega \frac{e_{qr}}{p^2} \right. \\ \left. + \omega \ell \frac{i_{qr}}{p^2} - \ell \frac{i_{dr}}{p} - (rc + g\ell) \frac{e_{dr}}{p} - 2c\ell\omega \frac{e_{qr}}{p} \right] \quad (3.37)$$

and

$$e_{qr} = \frac{1}{c\ell} \left[\frac{e_{qs}}{p^2} + (c\ell\omega^2 - 1 - rg) \frac{e_{qr}}{p^2} - r \frac{i_{qr}}{p^2} + (rc + g\ell)\omega \frac{e_{dr}}{p^2} \right. \\ \left. - \omega\ell \frac{i_{dr}}{p^2} - \ell \frac{i_{qr}}{p} - (rc + g\ell) \frac{e_{qr}}{p} + 2c\ell\omega \frac{e_{dr}}{p} \right] \quad (3.38)$$

The computer representation of these equations is shown in Figures 3.7 and 3.8.

The axis currents at the busbar are obtained by collecting and rearranging terms of Equation (2.34) to give

$$i_{ds} = \frac{1}{\ell c} \left[\frac{i_{dr}}{p^2} + (c\ell\omega^2 - 1 - rg) \frac{i_{ds}}{p^2} + g \frac{e_{ds}}{p^2} - (rc + g\ell)\omega \frac{i_{qs}}{p^2} \right. \\ \left. + \omega c \frac{e_{qs}}{p^2} + c \frac{e_{ds}}{p} - (rc + g\ell) \frac{i_{ds}}{p} - 2c\ell\omega \frac{i_{qs}}{p} \right] \quad (3.39)$$

and

$$i_{qs} = \frac{1}{\ell c} \left[\frac{i_{qr}}{p^2} + (c\ell\omega^2 - 1 - rg) \frac{i_{qs}}{p^2} + g \frac{e_{qs}}{p^2} + (rc + g\ell)\omega \frac{i_{ds}}{p^2} \right. \\ \left. - \omega c \frac{e_{ds}}{p^2} + c \frac{e_{qs}}{p} - (rc + g\ell) \frac{i_{qs}}{p} + 2c\ell\omega \frac{i_{ds}}{p} \right] \quad (3.40)$$

Figures 3.9 and 3.10 show the computer representation for determination of the busbar current.

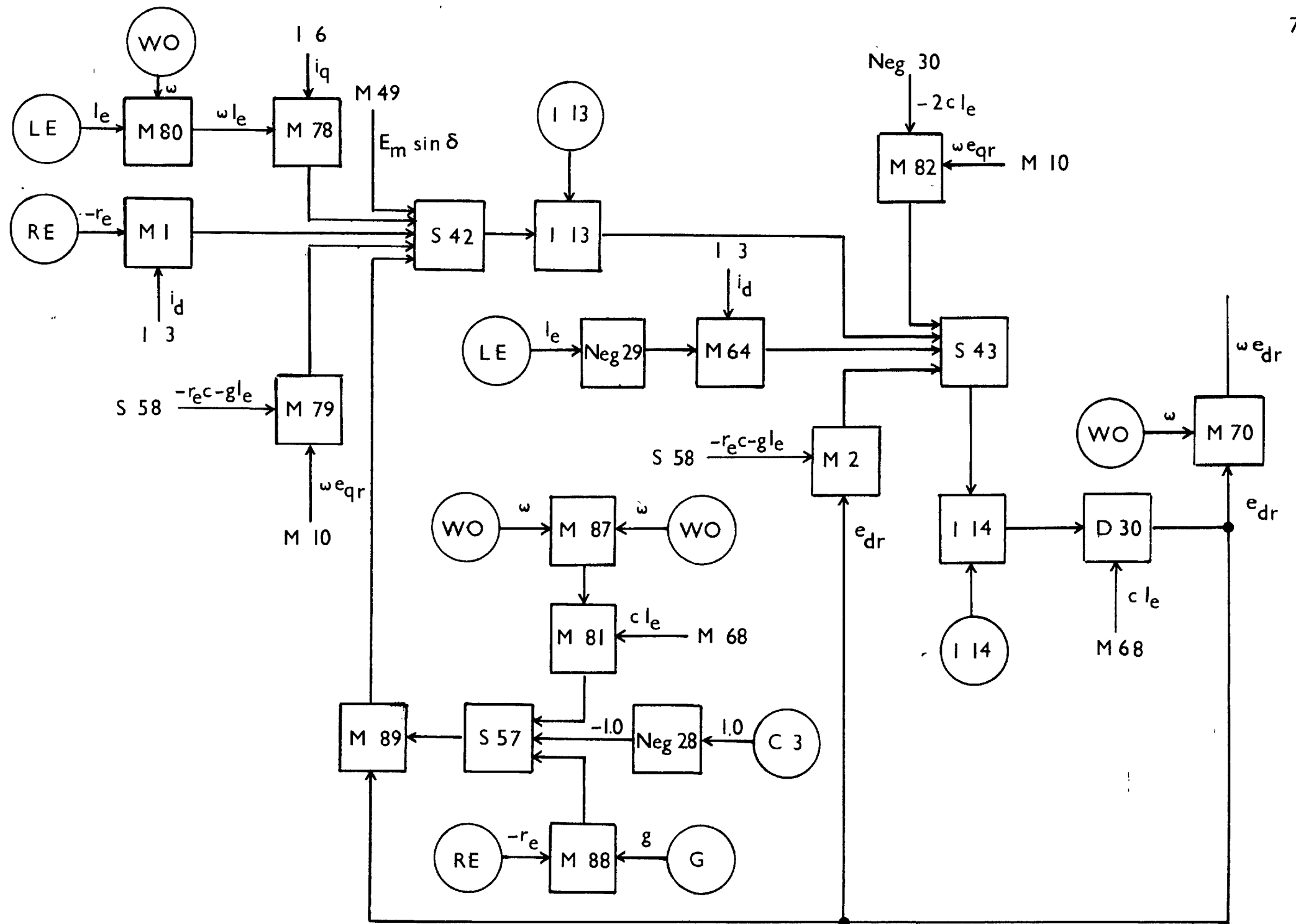


FIGURE 3.7 Long Transmission Line Equation for Direct Component of Voltage Drop

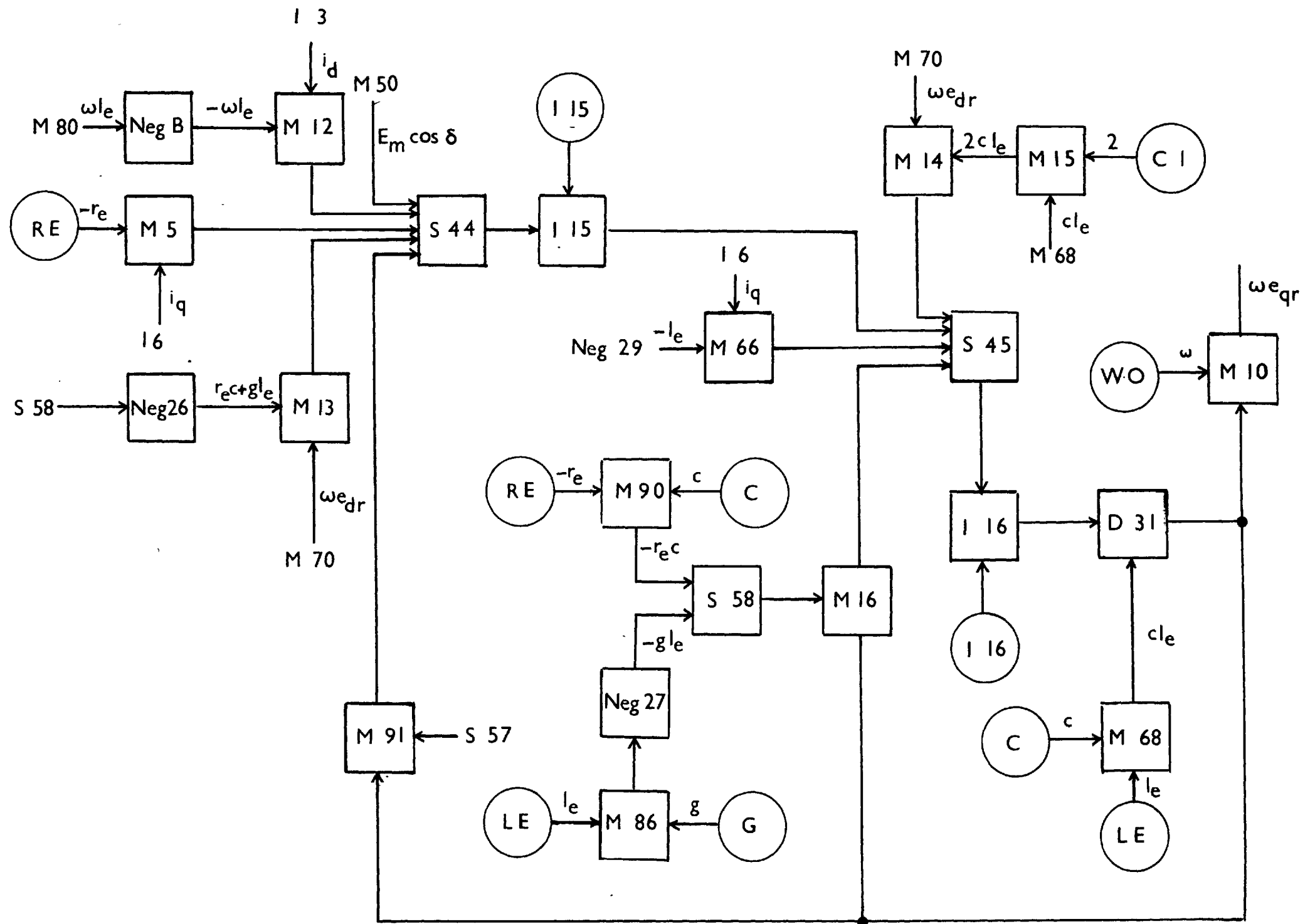


FIGURE 3.8 Long Transmission Line Equation for Quadrature Component of Voltage Drop

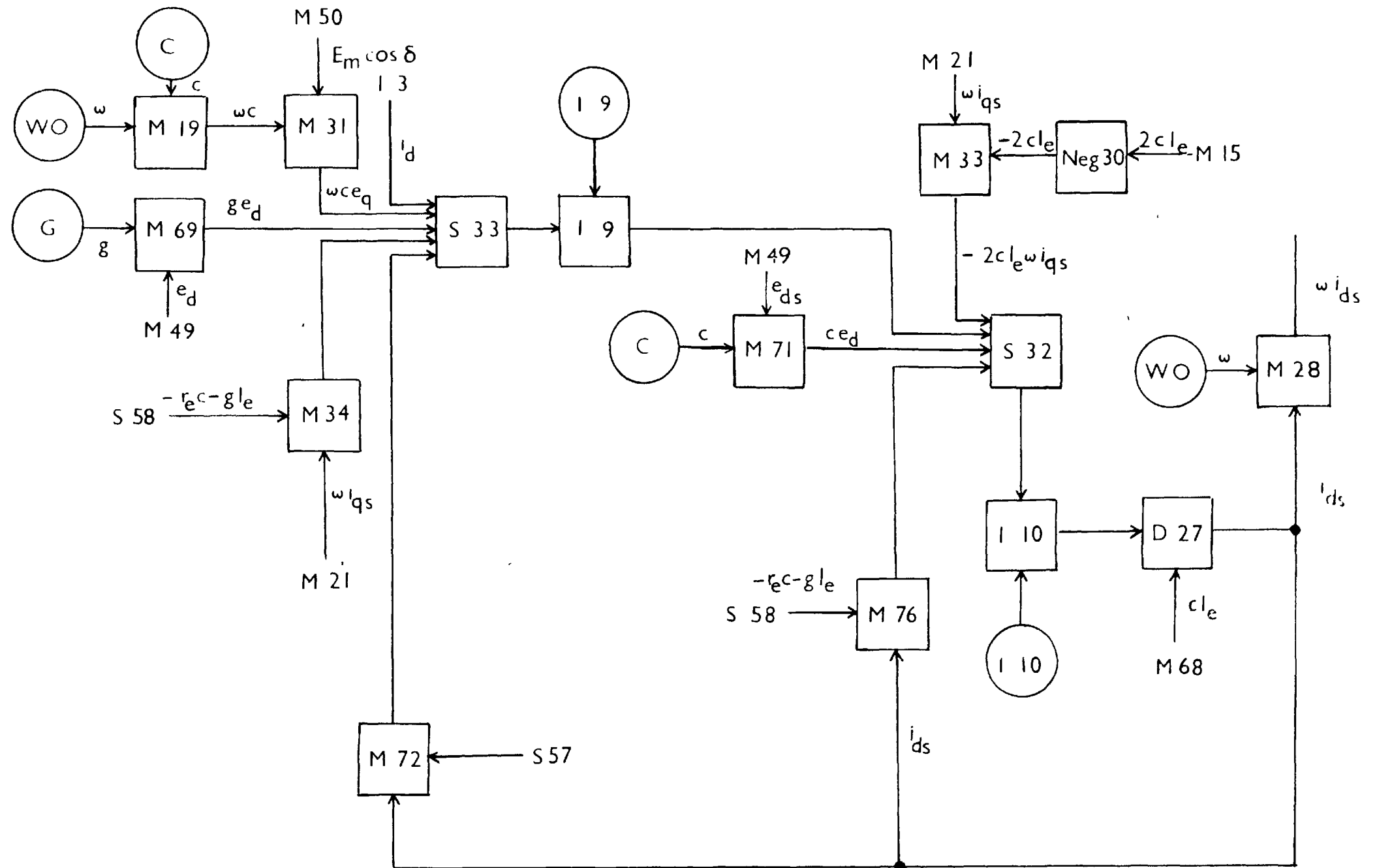


FIGURE 3.9 Long Transmission Line Equation for the Direct Component of Current Loss

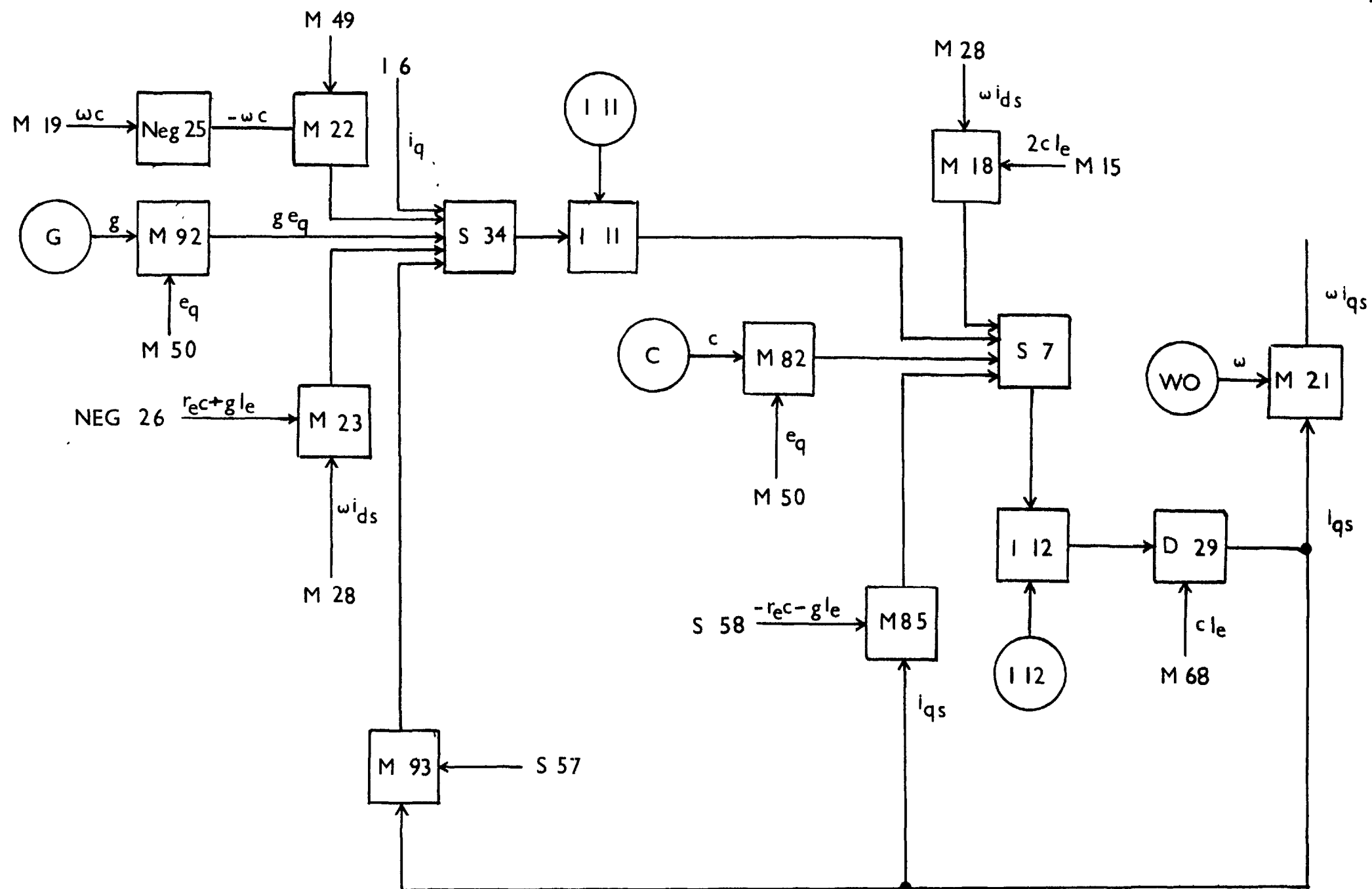


FIGURE 3.10 Long Transmission Line Equation for the Quadrature Component of Current Loss

3.2.7 Circulating Current Equation

To obtain the time domain equation for the circulating current, Equation (2.42) is multiplied by $(r_s + \ell p)$ to become

$$\begin{aligned} L r_s p I_n + L \ell p^2 I_n + (r_s^2 + 2 r_s \ell p + \ell^2 p^2) i_n + R r_s N i_n \\ + R \ell N p i_n + R L N p I_n - R \sum_{n=1}^N L p I_n = 0 \end{aligned} \quad (3.41)$$

dividing by p^2 and solving for i_n

$$\begin{aligned} i_n = - \frac{r_s^2}{\ell^2} \frac{i_n}{p^2} - \frac{NR}{\ell^2} r_s \frac{i_n}{p} + \frac{R}{\ell} \sum_{n=1}^N \frac{I_n}{p} - \frac{RN}{\ell} \frac{I_n}{p} - \frac{2r_s}{\ell} \frac{i_n}{p} \\ - \frac{NR}{\ell} \frac{i_n}{p} - \frac{r_s}{\ell} \frac{I_n}{p} - I_n \end{aligned} \quad (3.42)$$

For a CT with low leakage such as a through or bar type (33, 68, 71), $\ell \approx L$.

3.3 Transformation of Symmetrical Waveforms

3.3.1 Busbar Voltage

The voltage of phase a sinusoidally applied at a frequency of $\omega/2\pi$ can be expressed as

$$e_a = E_m \sin(\omega t + \lambda) \quad (3.43)$$

If λ is chosen so that $e_a = 0$ when $t = 0$ it is possible to transform all networks to the same instant in the time domain by relating them to the busbar voltage. From Equation (2.17)

$$\omega t + \lambda = \theta + \delta \quad (3.44)$$

where $\lambda = 0$. Substituting Equation (3.44) in Equation (3.43) gives

$$e_a = E_m \sin \delta \cos \theta + E_m \cos \delta \sin \theta \quad (3.45)$$

The inverse transformation of Equation (2.1) relates e_a to e_d and e_q as follows.

$$e_a = e_d \cos \theta + e_q \sin \theta \quad (3.46)$$

Therefore

$$e_d = E_m \sin \delta \quad (3.47)$$

$$e_q = E_m \cos \delta \quad (3.48)$$

The MIDAS circuit for symmetrical voltages is given in Figure 3.11. For normal operation $E_m = 1.4142$ as defined in Section 2.2. For a three phase fault $E_m = 0$.

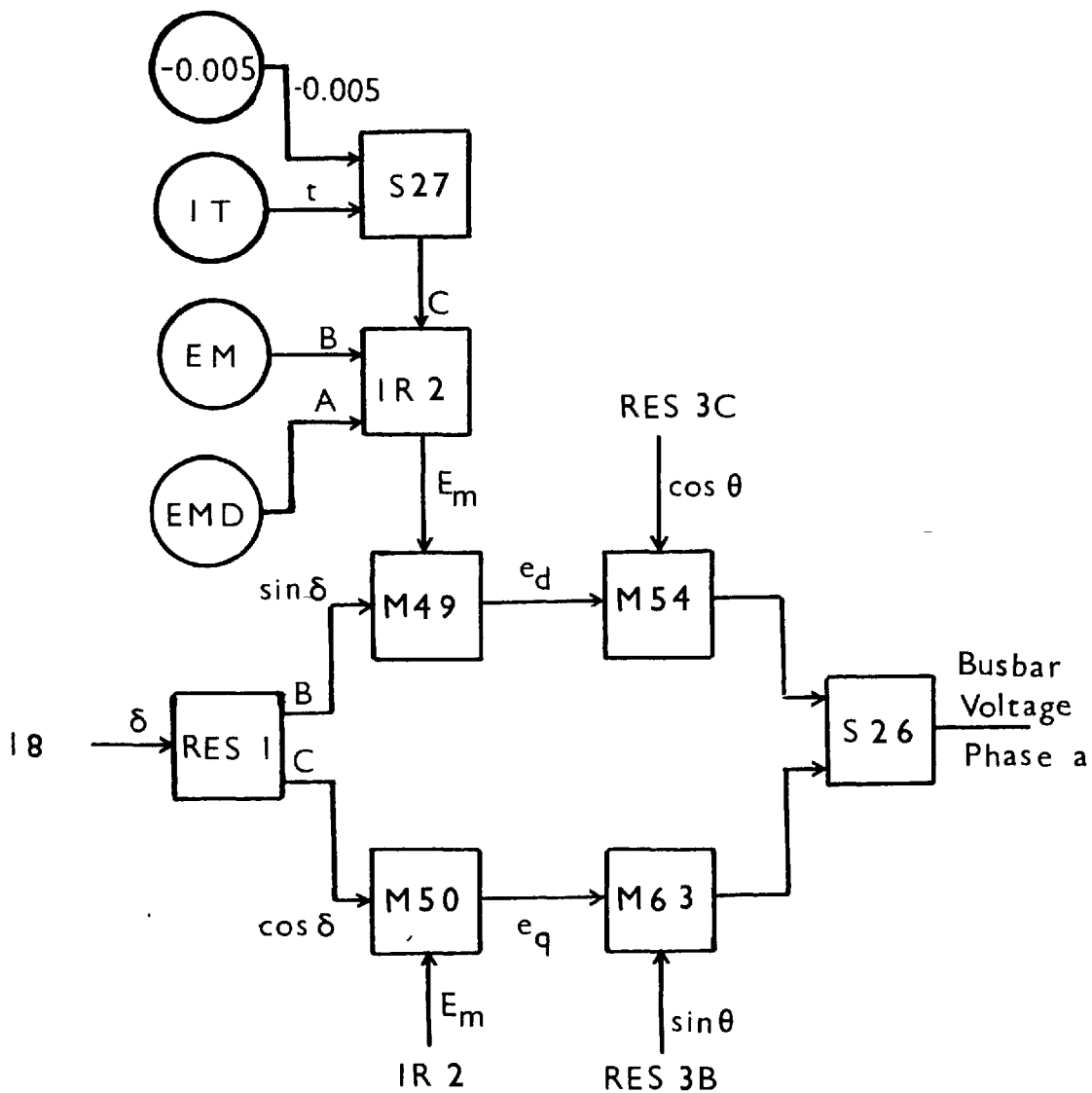


FIGURE 3.II Busbar Symmetrical Voltage Equation

3.3.2 Primary Circuit Currents

The current equivalent transform of Equation (3.46) is as follows.

$$i_a = i_d \cos \theta + i_q \sin \theta \quad (3.49)$$

The transform of currents is given in Figure 3.12.

3.3.3 Linear Coupler

The voltage on the secondary of a linear coupler is given by (44)

$$e_s = -L p i_t + ((L + \ell_s)p + r_s)i_s \quad (3.50)$$

$$e_s = -R i_s \quad (3.51)$$

Substituting Equation (3.51) in Equation (3.50) and expanding by Equation (2.1)

$$\begin{aligned} -R(i_{ds} \cos \theta + i_{qs} \sin \theta) &= -L \cos \theta p i_{dt} + L i_{dt} \omega \sin \theta \\ &- L \sin \theta p i_{qt} - \omega L i_{qt} \cos \theta + (L + \ell_s)p i_{ds} \cos \theta \\ &- (L + \ell_s)\omega i_{ds} \sin \theta + (L + \ell_s)p i_{qs} \sin \theta \\ &+ (L + \ell_s)\omega i_{qs} \cos \theta + r_s i_{ds} \cos \theta + r_s i_{qs} \sin \theta \end{aligned} \quad (3.52)$$

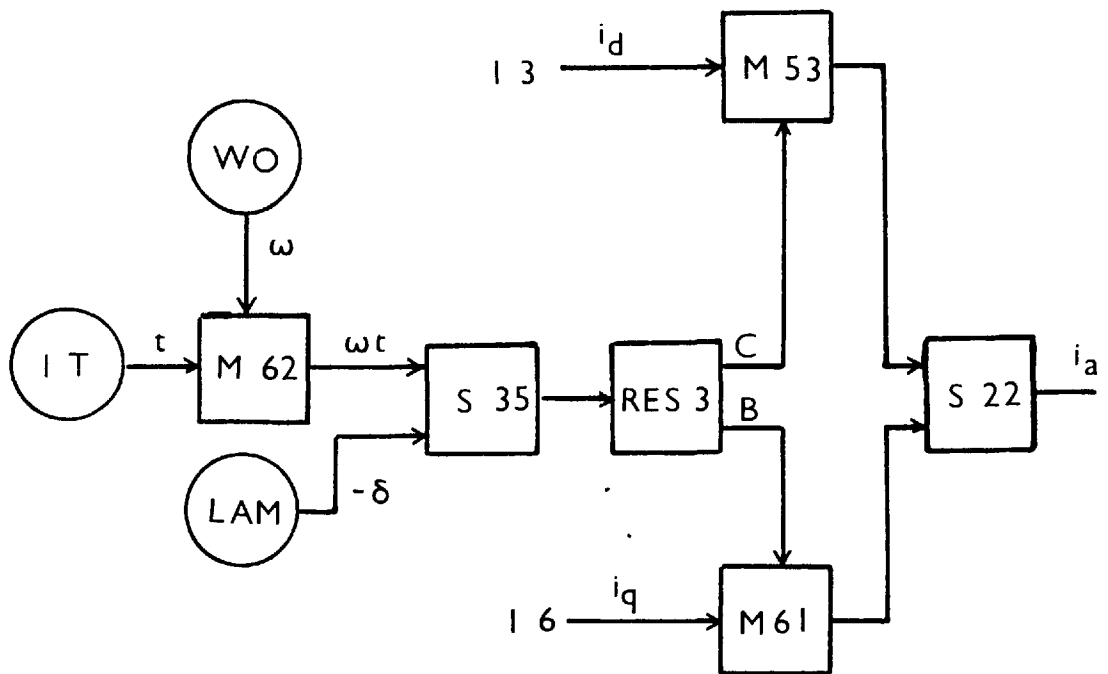


FIGURE 3.12 Transform Equation for Waveforms

Gathering terms and dividing by p the axis equations for the linear coupler become

$$i_{ds} = \frac{L}{(L + \ell_s)} i_{dt} + \frac{\omega L}{(L + \ell_s)} \frac{i_{qt}}{p} - \frac{(R + r_s)}{(L + \ell_s)} \frac{i_{ds}}{p} - \omega \frac{i_{qs}}{p} \quad (3.53)$$

$$i_{qs} = \frac{L}{(L + \ell_s)} i_{qt} - \frac{\omega L}{(L + \ell_s)} \frac{i_{dt}}{p} - \frac{(R + r_s)}{(L + \ell_s)} \frac{i_{qs}}{p} + \omega \frac{i_{ds}}{p} \quad (3.54)$$

The MIDAS representation for the linear coupler voltage is given in Figure 3.13.

The current equations which have the same waveform as the voltage equations are used to reduce scaling problems on the computer plotter.

3.4 Transformation Using α and β Components for Asymmetrical Waveforms

The following relationship between the two-axis field and α and β field for the reference axis is the inverse of that used by Concordia (14).

$$\begin{bmatrix} e_\alpha & i_\alpha \\ e_\beta & i_\beta \end{bmatrix} = \begin{bmatrix} \cos \theta & \sin \theta \\ -\sin \theta & \cos \theta \end{bmatrix} \begin{bmatrix} e_d & i_d \\ e_q & i_q \end{bmatrix} \quad (3.55)$$

Clarke (13) gives the relationship between phase values and α and β components for phasors from which the relation for instantaneous values is as follows.

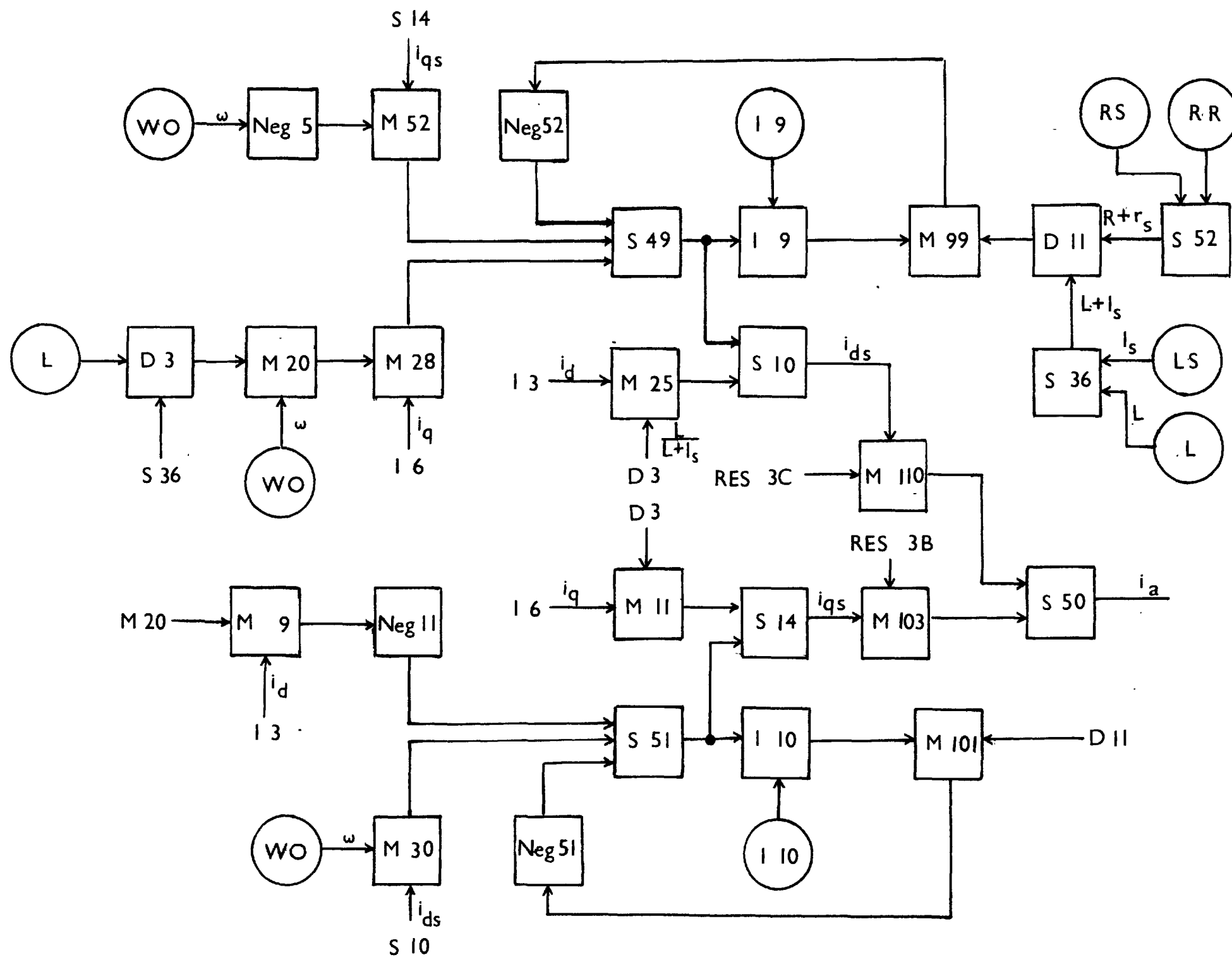


FIGURE 3.13 Linear Coupler Equation for Phase a

$$\begin{bmatrix} e_a, i_a \\ e_b, i_b \\ e_c, i_c \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ -\frac{1}{2} & -\frac{3}{2} & 1 \\ -\frac{1}{2} & \frac{3}{2} & 1 \end{bmatrix} \begin{bmatrix} e_\alpha, i_\alpha \\ e_\beta, i_\beta \\ e_o, i_o \end{bmatrix} \quad (3.56)$$

With these relationships the asymmetrical waveforms for faults can be developed.

3.4.1 Line - to - Line Faults

Phase quantities for a line - to - line fault on phases b and c are as follows.

a) Phase Currents

From Equations (3.55) and (3.56) currents in phase b and c are as follows.

$$i_b = - \left[\frac{1}{2} i_d + \frac{3}{2} i_q \right] \cos \theta + \left[-\frac{1}{2} i_q + \frac{3}{2} i_d \right] \sin \theta \quad (3.57)$$

$$i_c = \left[-\frac{1}{2} i_d + \frac{3}{2} i_q \right] \cos \theta - \left[\frac{1}{2} i_q + \frac{3}{2} i_d \right] \sin \theta \quad (3.58)$$

The MIDAS representation to determine i_b and i_c is shown in Figure 3.14. When $e_b = 0$ at $t = 0$ then by the argument of Section 3.3.2

$$\theta = \omega t - \delta + \frac{2\pi}{3} \quad (3.59)$$

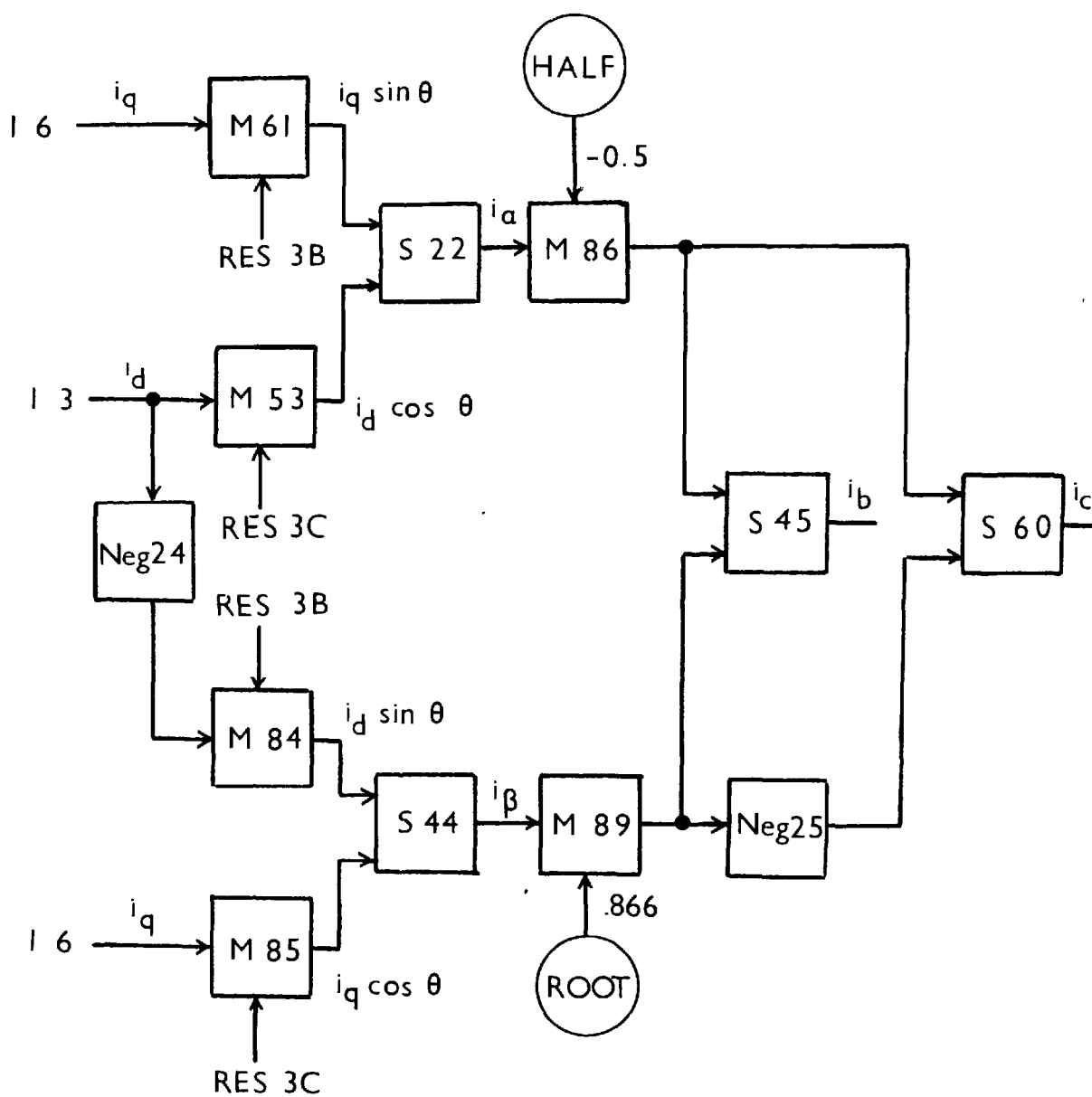


FIGURE 3.14 Line to Line Fault Current Transform

b) Faulted and Unfaulted Voltage

The busbar unfaulted voltage can be taken from Equations (3.46), (3.47) and (3.48).

$$e_a = E_m \sin \delta \cos \theta + E_m \cos \delta \sin \theta \quad (3.60)$$

Transform (3.55) gives the following relation.

$$e_d = e_\alpha \cos \theta - e_\beta \sin \theta \quad (3.61)$$

$$e_q = e_\alpha \sin \theta + e_\beta \cos \theta \quad (3.62)$$

Since $e_\alpha = e_a$ and $e_\beta = 0$ for a phase b-to-c fault

$$e_d = E_m \sin \delta \cos^2 \theta + E_m \cos \delta \sin \theta \cos \theta \quad (3.63)$$

$$e_q = E_m \cos \delta \sin^2 \theta + E_m \sin \delta \sin \theta \cos \theta \quad (3.64)$$

The circuit for the application of this fault is shown in Figure 3.15.

c) Protective Circuit Transformation

Combining the linear coupler equations, Equations (3.53) and (3.54), and the current equations, Equations (3.57) and (3.58), the coupler voltage waveforms for phase b on a line-to-line fault for the components of α

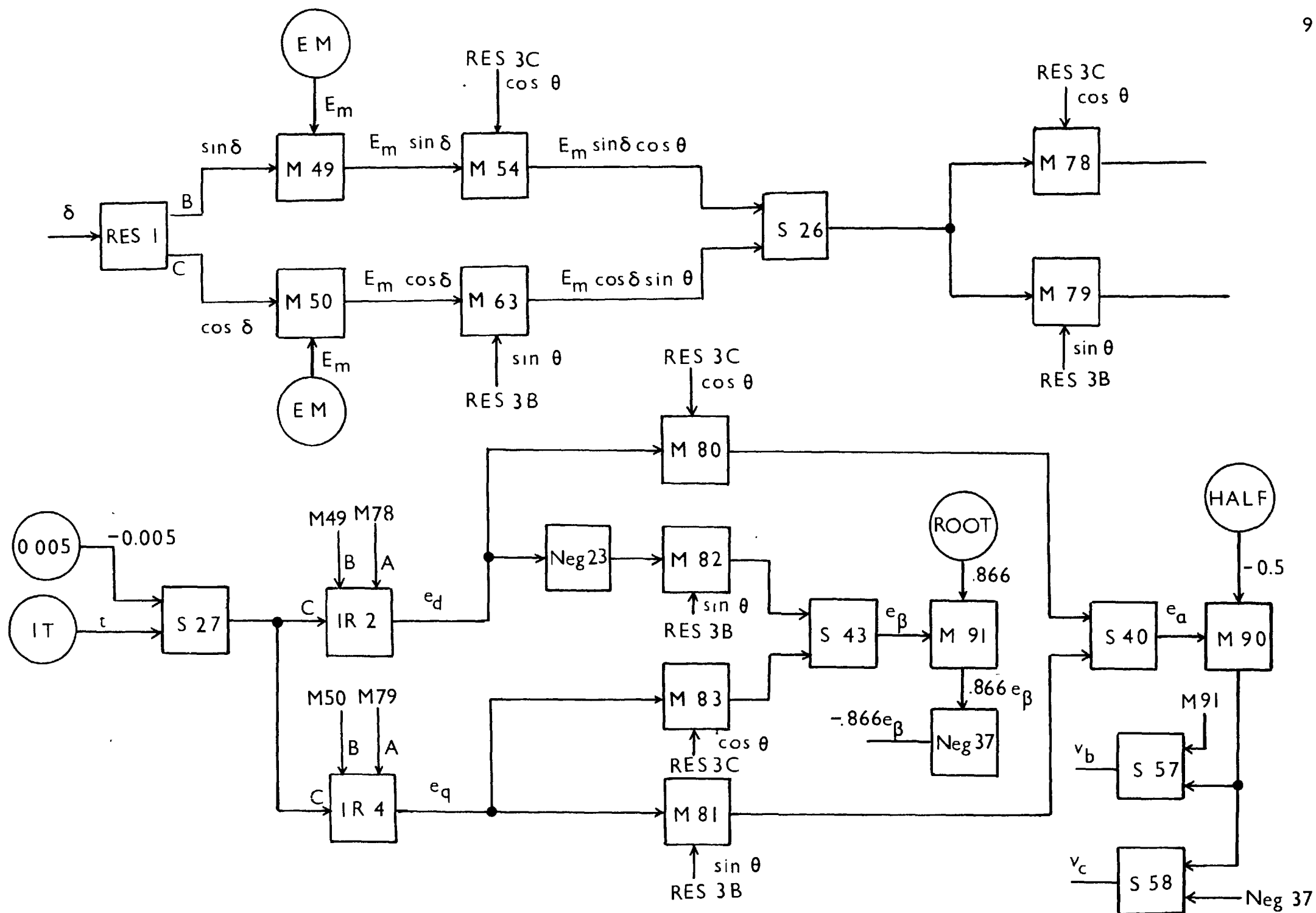


FIGURE 3.15 Line to Line Fault Voltage Transform Equation

and β along each axis is as follows.

$$i_{bds} = \frac{L}{(L + \ell_s)} \left(-\frac{1}{2} i_{dt} - \frac{3}{2} i_{qt} \right) + \frac{\omega L}{(L + \ell_s)} \frac{\left(-\frac{1}{2} i_{qt} + \frac{3}{2} i_{dt} \right)}{p} - \frac{(R + r_s)}{(L + \ell_s)} \frac{i_{bds}}{p} - \omega \frac{i_{bqs}}{p} \quad (3.65)$$

$$i_{bqs} = \frac{L}{(L + \ell_s)} \left(-\frac{1}{2} i_{qt} + \frac{3}{2} i_{dt} \right) - \frac{\omega L}{(L + \ell_s)} \frac{\left(-\frac{1}{2} i_{dt} - \frac{3}{2} i_{qt} \right)}{p} - \frac{(R + r_s)}{(L + \ell_s)} \frac{i_{bqs}}{p} + \omega \frac{i_{bds}}{p} \quad (3.66)$$

and similarly for phase c.

3.4.2 Line - to - Ground Faults

Phase quantities for a phase a - to - ground fault are as follows.

a) Phase a Current

The current in phase a for a line - to - ground fault is obtained from Equations (3.55) and (3.56) for the condition where (13)

$$i_\alpha = 2 i_o \quad (3.67)$$

and is as follows.

$$i_a = \frac{3}{2} (i_d \cos \theta + i_q \sin \theta) \quad (3.68)$$

b) Two - Axis Voltage

The busbar voltage for unfaulted conditions is given in Equation (3.45). Since $e_\alpha = -e_o$ for line - to - ground fault and $e_a = 0$ the axis equations are derived from Equations (3.45), (3.55) and (3.56).

$$e_d = E_m \sin \delta \sin \theta - E_m \cos \delta \cos \theta \sin \theta \quad (3.69)$$

$$e_q = -E_m \sin \delta \sin \theta + E_m \cos \delta \cos \theta \cos \theta \quad (3.70)$$

The simulator circuit for this fault is shown in Figure 3.16.

Equations (3.53), (3.54) and (3.68) give the waveforms of the linear coupler output voltage.

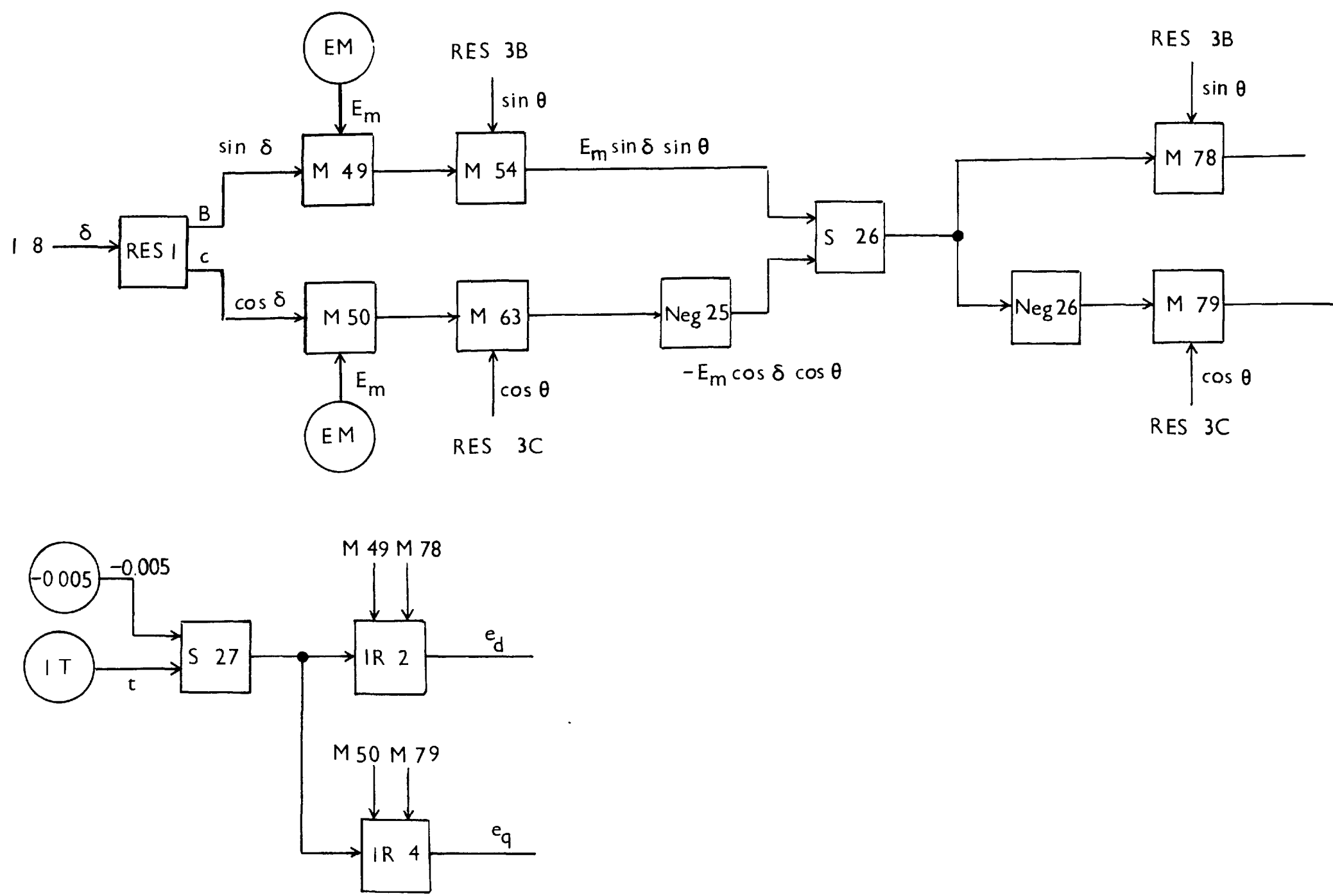


FIGURE 3.16 Line to Ground Fault Voltage Transform Equation

CHAPTER 4

SYSTEM BEHAVIOUR DURING FAULTS

4.1 Power and VAR Flow

During normal operation of an electrical network, infeed and output of both real and reactive power at the busbar are equal. In this network simulation each feeder is examined individually and the real and reactive power of the feeder is set to a predetermined value which is fixed by preliminary computer runs.

4.2 Method of Determination of the Primary Circuit Waveforms

To comply with the requirements outlined in Section 1.3.2 each feeder is represented by a machine connected through a transmission line to a substation busbar. The simulation is run for a number of network operating conditions. The real power at the busbar is given by Equation (3.29). T_t , shown in Figure 3.6, is varied to give this required value of power at the busbar. The busbar reactive power balance is regulated by varying the value of EF, shown in Figures 3.3 and 3.4, to the required output as given by Equation (3.31). This method is used to determine the simulator initial conditions which represents the network under its loaded or operational state. The simulation is run

for a number of network operating conditions.

All variables are obtained for unfaulted steady state conditions, and current and voltage waveforms are obtained for the three types of faults. The application of the short circuit is from a normal or loaded network condition at maximum instantaneous voltage and not from the unloaded network condition. Each feeder is simulated separately by changing the parameters and determining the required variables over a desired range of the independent variable. All primary waveforms are determined in the two-axis field and then transformed to the time domain.

4.3 Methods of Determination of the Busbar Protection Circuit Currents

When the secondary or busbar protection circuit has an impedance which is independent of primary current, the simulation of the secondary is included with the simulation of the primary in the two-axis field and then transformed. Since the secondary current of a circulating protection scheme is a function of the current in the primaries of all busbar protection CTs the effect of all lines are considered together. Because the simulation of each feeder is done individually, a separate program is used for the simulation of the circulating current protection scheme. The parameters of this simulation are the circuit values given in Equation (3.42) and the primary circuit currents obtained from the network simulation.

The reference axes chosen do not permit addition and subtraction of the two-axis quantities unless they are first transformed to a field with the same reference axis. The sinusoidal variation of the currents in the time domain, which makes calculation of instantaneous values impractical without transform methods, gives increased difficulty in the determination of initial values for this representation because of the short times possible between successive iterations. However the reduction in the number of parameters required in the input is considerable. Therefore the secondary currents are determined in the time domain but only for the circulating current scheme simulations.

4.4 Substation Parameters

The substation used in this analysis is based on the configuration and power flow of a substation in Southeastern England but it is intended as an illustrative example of a substation and not as an exact simulation. The network parameters and the parameters obtained from the solutions of Equations (3.14), (3.15), (3.16), (3.17) and (3.18) for each feeder are given in Appendix Sections A.1 and A.2. The network arrangement for this substation is shown in Figure 4.1. The feeders are numbered 7, 8, 9 and 10 simply for convenience in computer runs and general handling of data and have no practical significance.

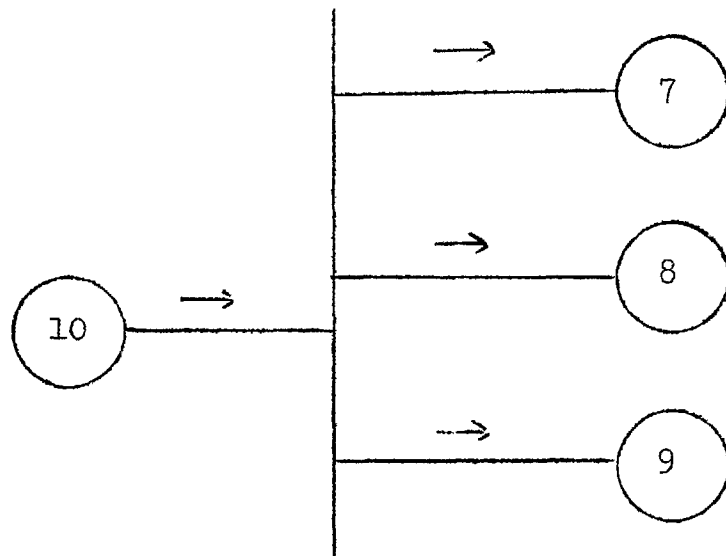


Figure 4.1 Substation Network

4.5 Normal Substation Operation

The instantaneous values of per unit current and voltage for phase a at the substation busbar are given in Figure 4.2. The real value of feeder current can be obtained from the per unit instantaneous current by the following equation.

$$I_t = 600 \times \text{MEG} \times i_a \quad (4.1)$$

The value of MEG for each substation feeder is given in Appendix Section A.3. Also included in this section are the values of real power in MW and reactive power in MVA for the desired operating condition. The per unit values used to simulate this condition are given as well as the values of torque and excitation required to obtain this balance. The computer constants of integration required are given in Appendix Section A.4.

4.6 Circulating Current Scheme Stability on External Faults

The general method of determining the value of stabilising resistance is given in Section 1.1.2. The solutions of Equations (1.1) and (1.2) give the stabilising and relay resistance (R_R) for an operating current of .2 per unit amperes. Since the phasor representation used in determining R_R is incorrect for functions not varying sinusoidally, the instantaneous values of relay current over the first 3/4 cycle after occurrence of a fault, are determined. For comparison

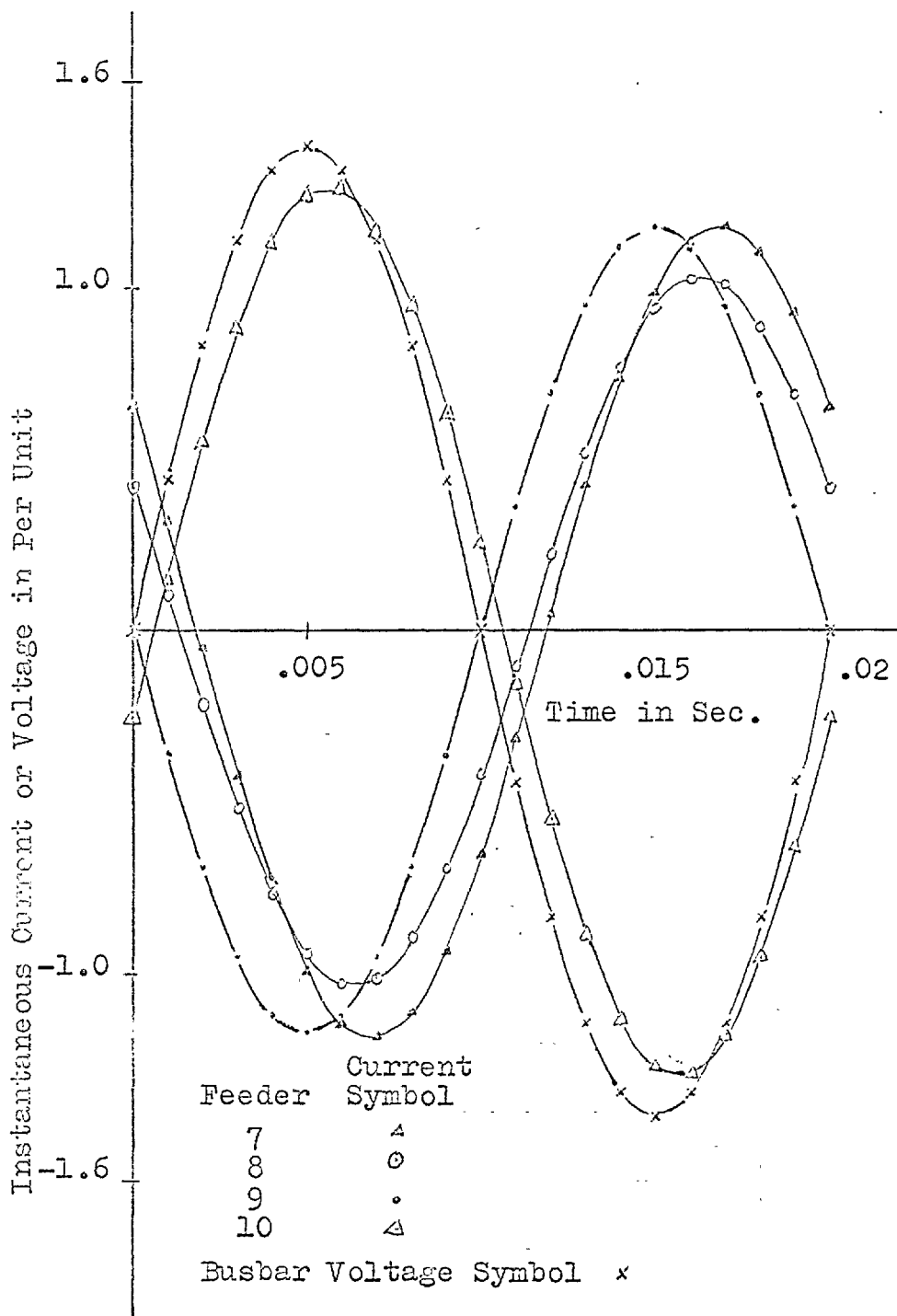


Figure 4.2 Normal Substation Operation

Figure 4.3 gives the fundamental relay currents for values of relay branch resistance of $R_R/14$, $R_R/2$ and R_R . These curves are for an external three phase fault which saturates the CT on feeder No. 10 and are obtained from the simulation of Equation (3.42).

4.7 Three Phase Fault Waveforms

The definitions of many terms used in this description are based on the phasor representation of current and voltage and these definitions become meaningless during a fault. However for purposes of discussion a cycle will be taken to mean the period of oscillation of the steady state, non-faulted system. Real and reactive power flows are not balanced on the busbar feeders during an internal fault.

Since fault studies are for one cycle only the speed governor and voltage regulator will not be considered.

4.7.1 Primary Network Waveforms

Figure 4.4 gives the primary circuit current for each network feeder for an internal three phase fault which occurs at maximum instantaneous voltage. This voltage waveform is included in the figure.

Figure 4.2 which is for the normal operating conditions shows that at all instants of time there

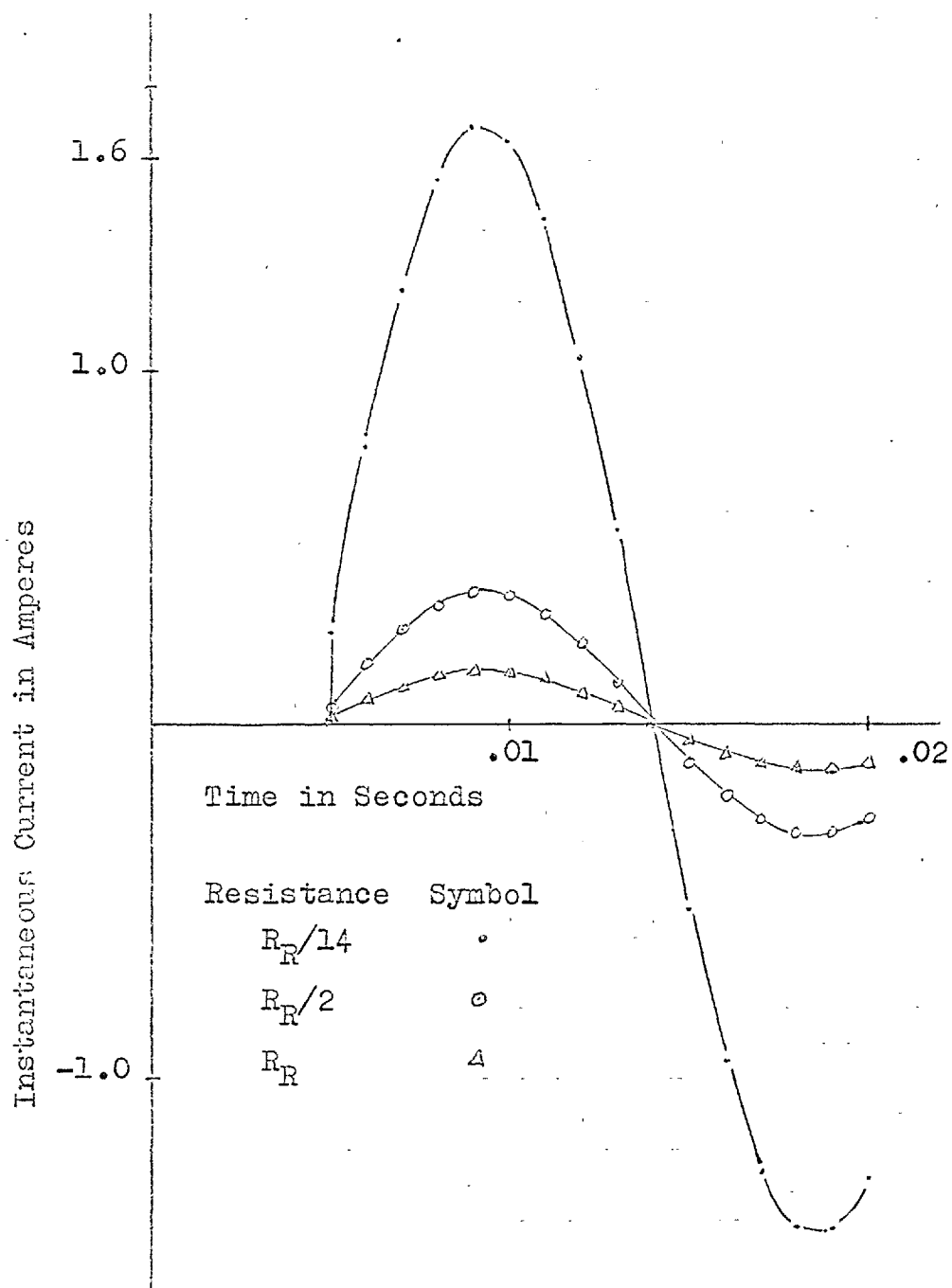


Figure 4.3 Relay Current During CT Saturation on External Fault

Fault Occurs at Time .005 Seconds

are feeders with instantaneous current of different polarity. However Figure 4.4 shows that on a three phase fault there are periods of time when the current in all feeders have the same polarity but that there is a region of polarity change in which both polarities exist.

4.7.2 Circulating Current Waveforms

The CT secondary instantaneous current values and protective relay instantaneous current for this fault occurring on the busbar is given in Figure 4.5 for a stabilising resistance of R_R . The relay current however is limited by a parallel connected non-linear resistor as outlined in Section 1.1.2, which may alter the waveforms of Figure 4.5. This voltage limitation is high enough to retain the resistor in the linear range on an external fault.

The protection scheme is dependent upon the saturation voltage of the CTs and the resistance of the relay circuit. If the ratio of CT inductance to relay resistance is too high saturation causes false operation on external faults. If this ratio is too low then a higher proportion of the current is required for CT magnetising current. A comparison of Figures 4.4 and 4.5 indicates that the pick-up current of .2 per unit amperes specified in Section 4.6 has put this ratio on the low side of the permitted range. Thus Figure 4.6, which gives the CT and protective relay instantaneous

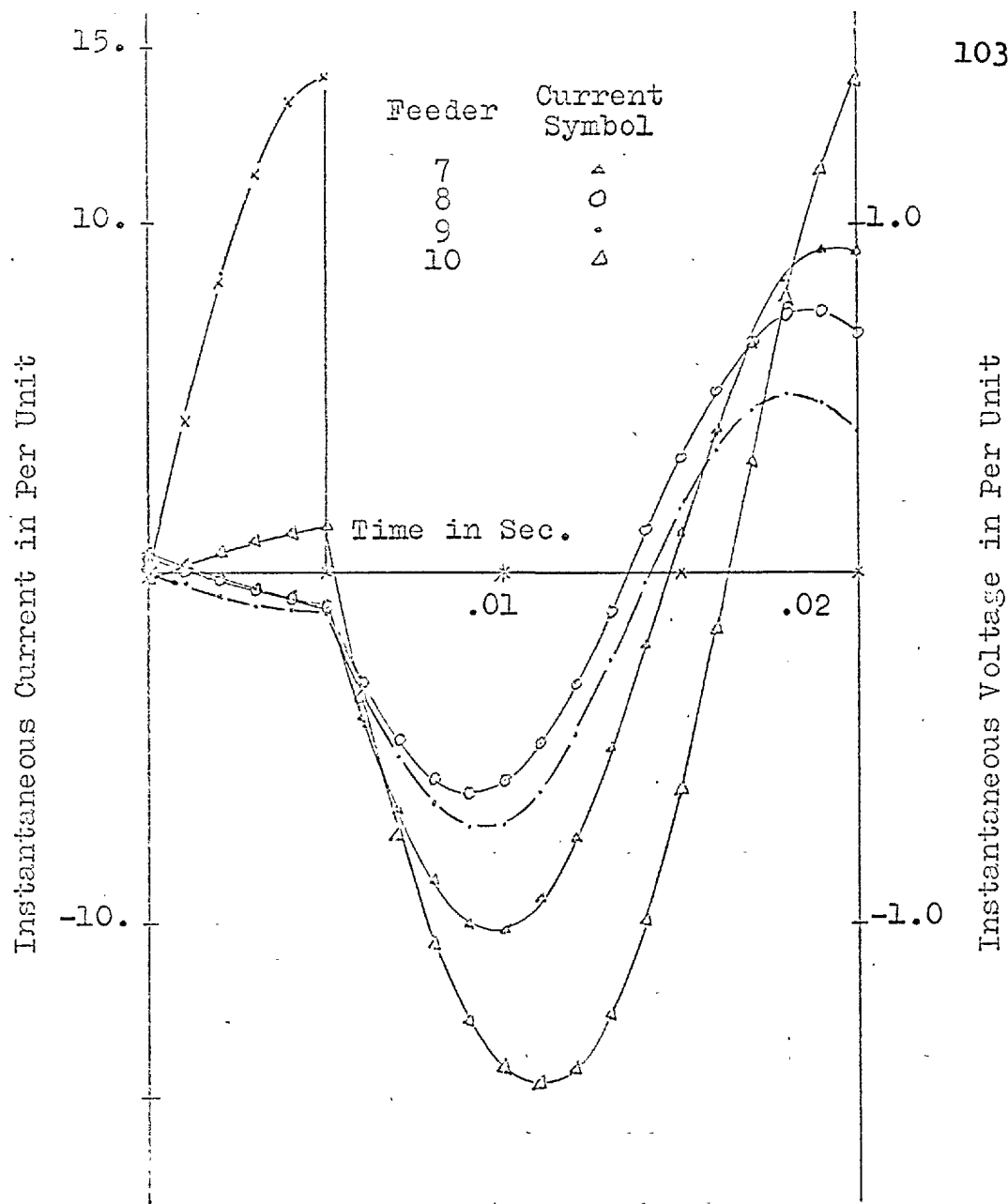


Figure 4.4 Waveforms for Three Phase Busbar Fault

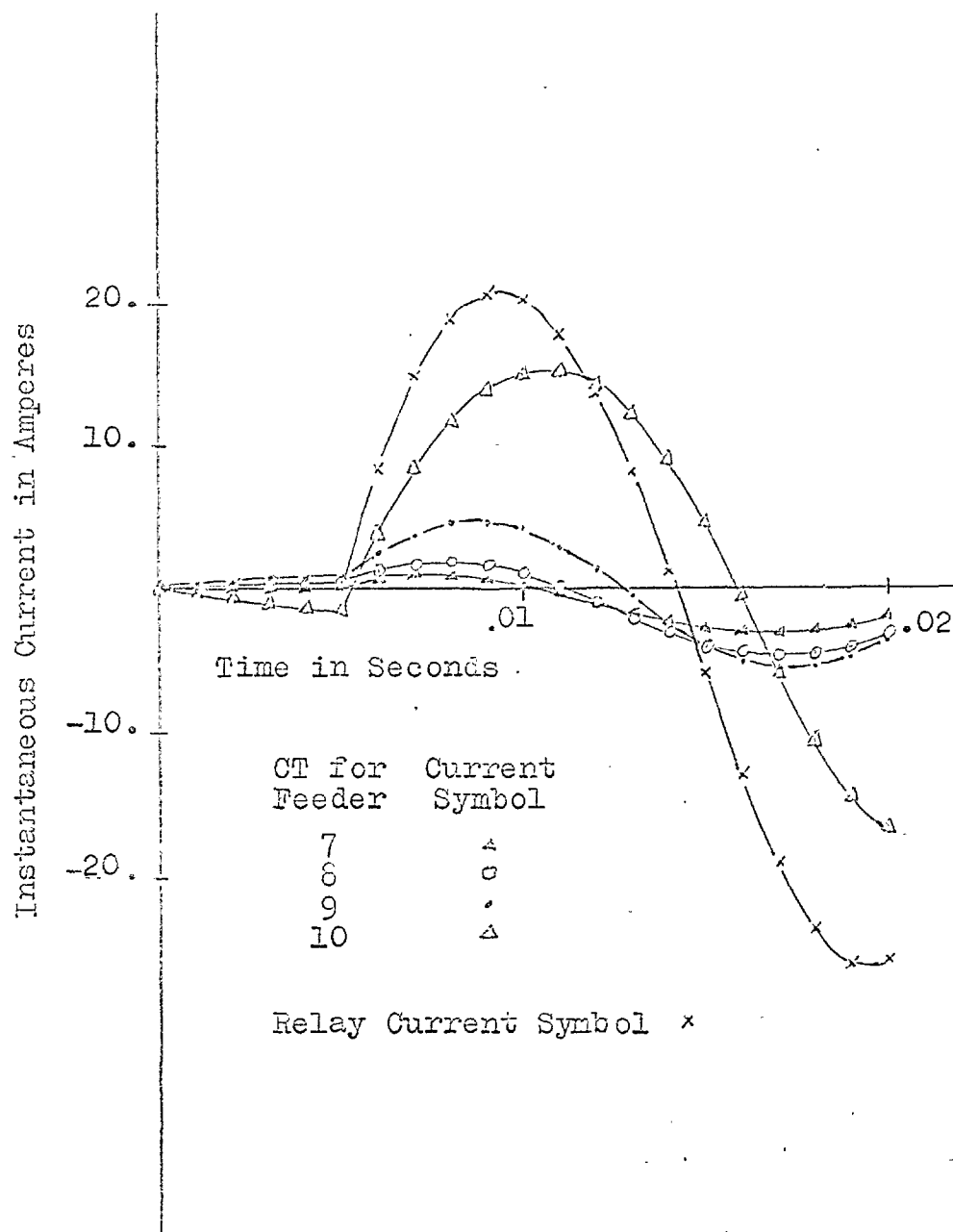


Figure 4.5 Current Transformer and Relay Waveforms for an Internal Three Phase Fault

Fault Occurs at Time .005 Seconds

current values for an external fault, shows a scheme with high stability.

4.7.3 Linear Coupler Waveforms

Figure 4.7 shows the linear coupler output for a three phase fault with the resistance of the coupler circuit equal to R_R . Figures 4.8 and 4.9 are also waveforms of linear coupler output for three phase faults but with coupler circuit resistances of $R_R/14$ and 1 megohm respectively. For convenience these values of linear coupler current are given on different per unit base values. Because the power output of a linear coupler is limited by the magnetic circuit Figure 4.8 is of interest for comparative purposes only. Figure 4.7 shows that there is no practical difference in linear coupler circuit waveforms for an increase in resistance to limit power output over this range. However Figure 4.9 shows the increase in phase shift as the circuit resistance increases which at infinite resistance or open circuit is 90 degrees ahead.

4.8 Line - to - Line Fault Waveforms

Figure 4.10 gives the primary instantaneous current for phase b of a line - to - line fault between b and c. Since the transform which gives the current in the time domain is 120 degrees ahead of the a phase transform the first quarter cycle of this figure is identical to Figure 4.4. For a three phase fault the

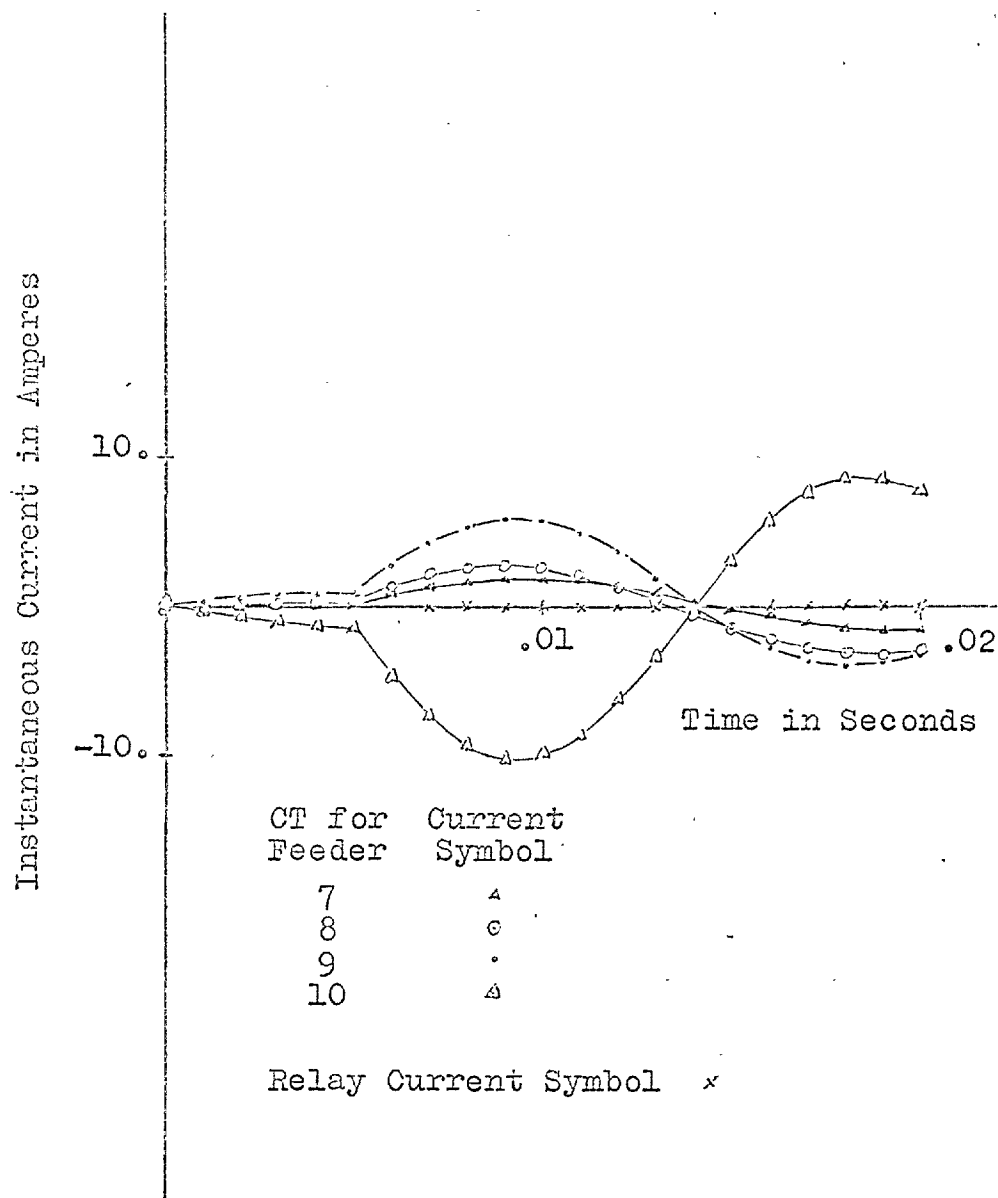


Figure 4.6 Current Transformer and Relay Waveforms for an External Fault

Fault Occurs at Time .005 Seconds

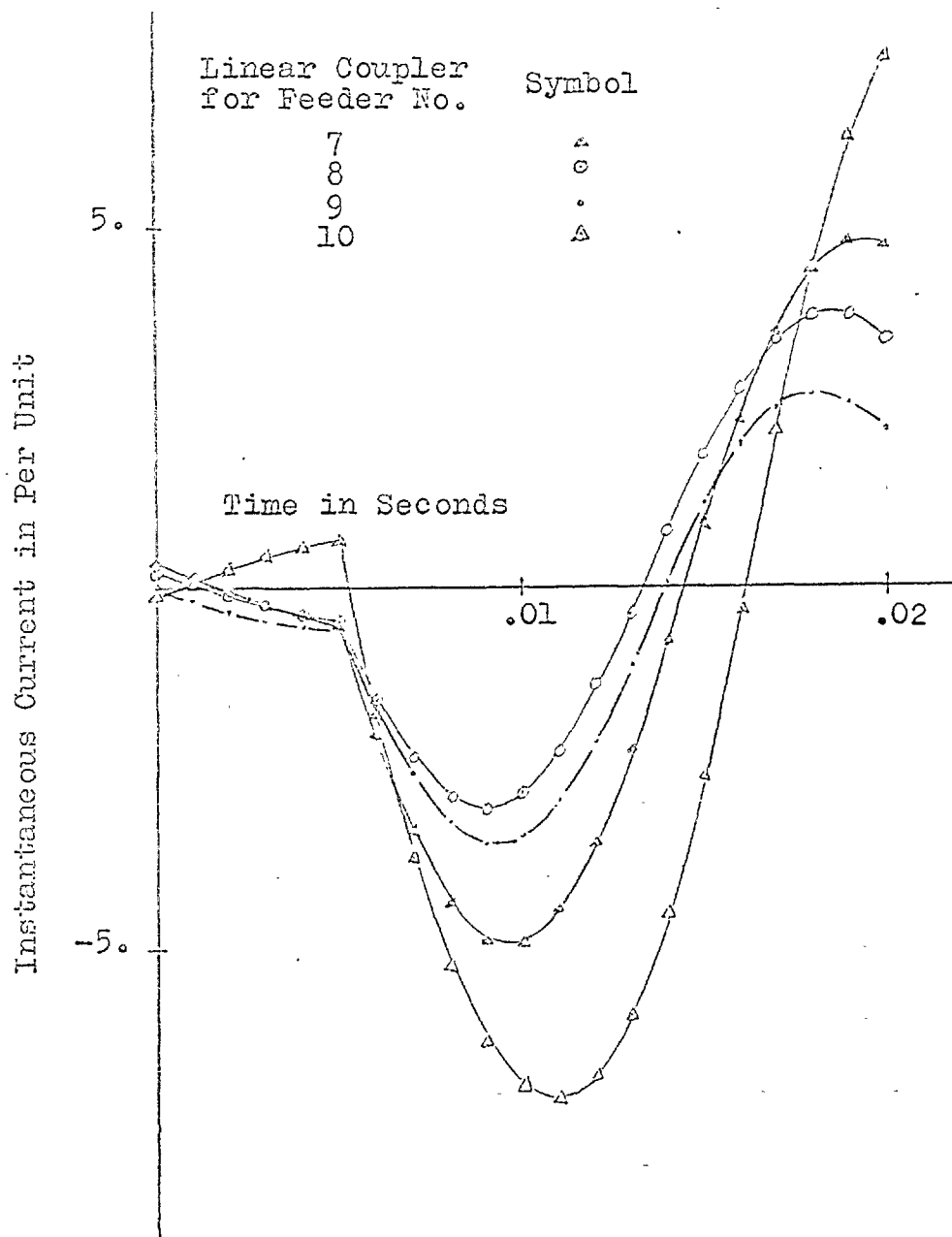


Figure 4.7 Linear Coupler Waveform for Output Resistance of R_R for a Three Phase Busbar Fault

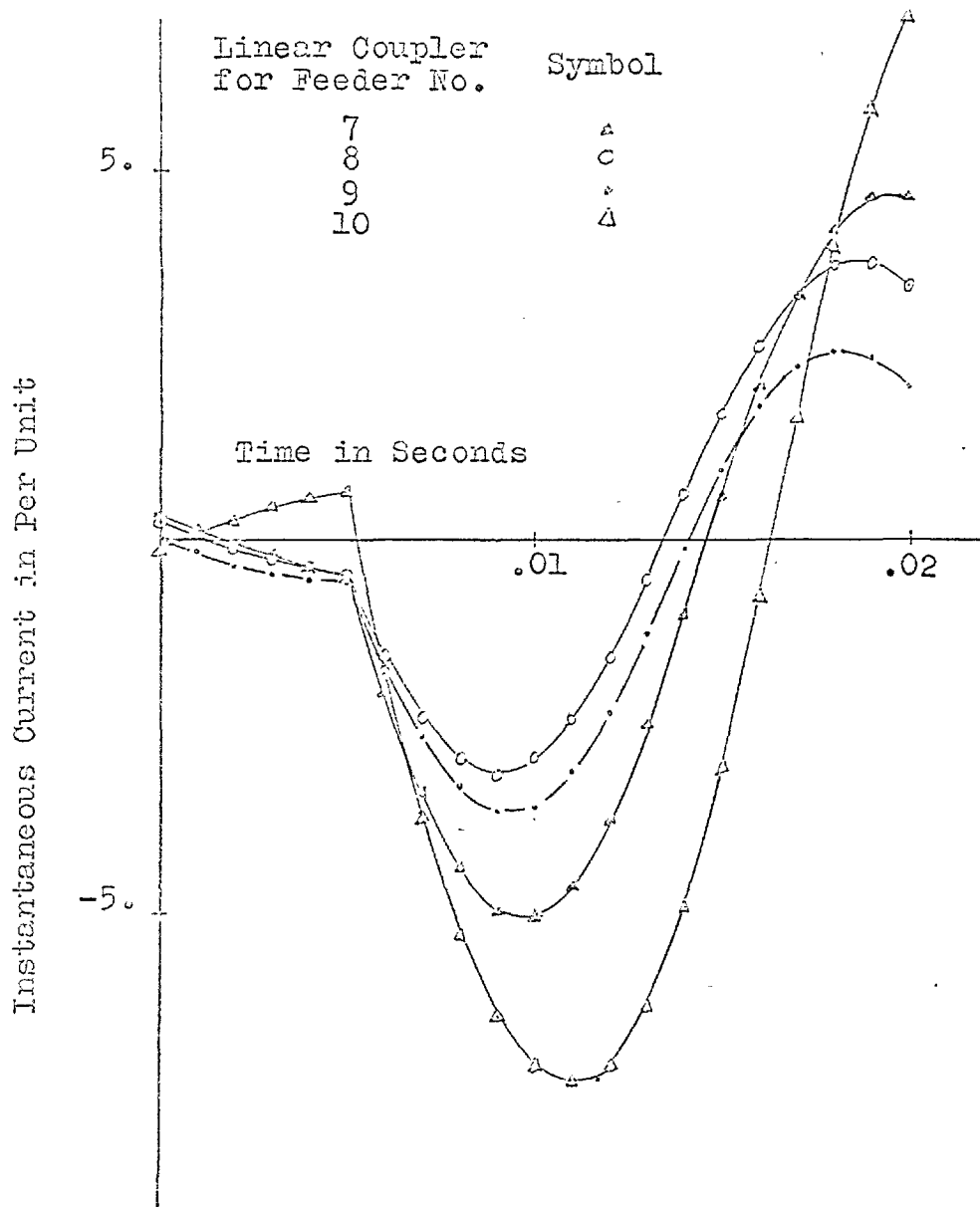


Figure 4.8 Linear Coupler Waveform for Output Resistance of $R_R/14$ for a Three Phase Busbar Fault

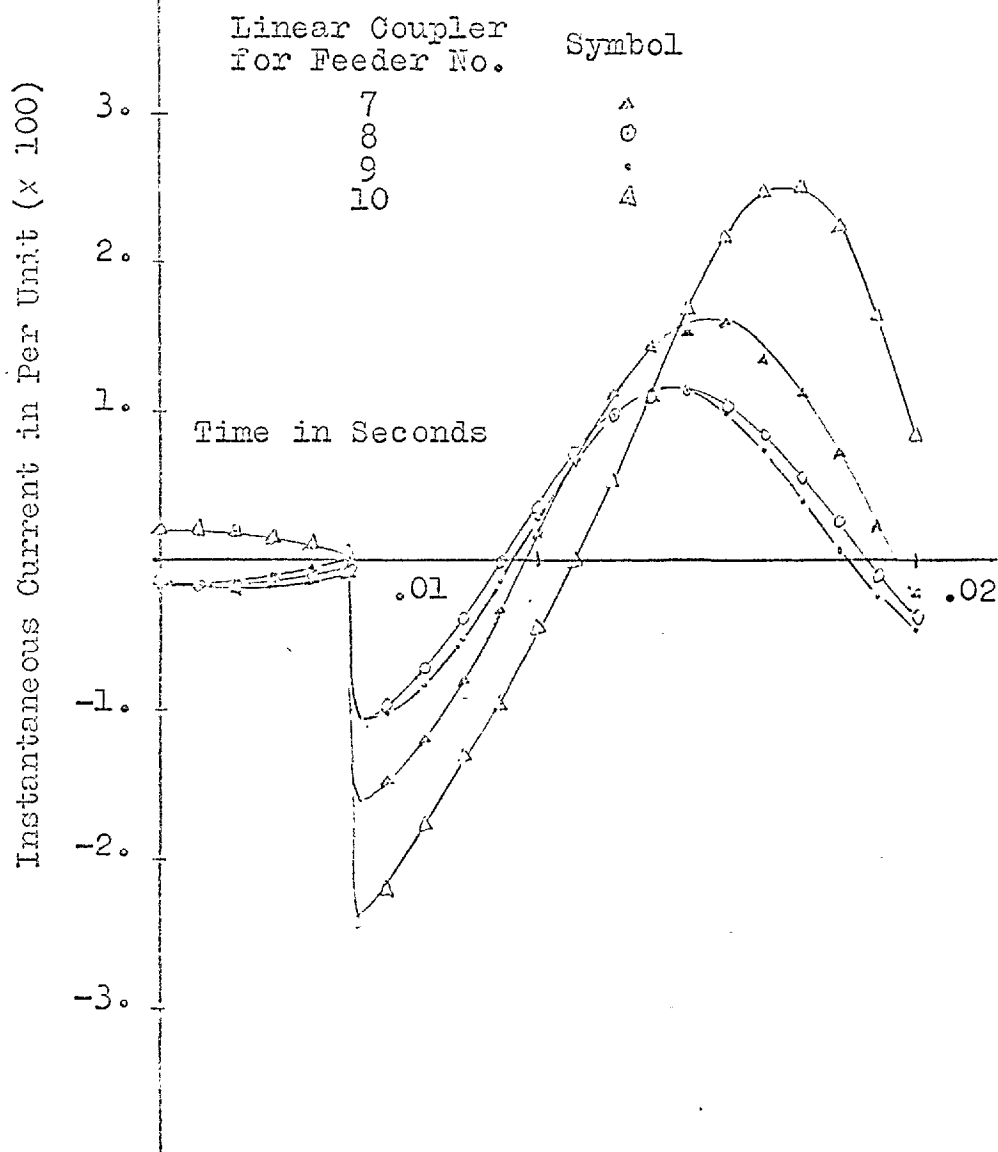


Figure 4.9 Linear Coupler Waveform for Output Resistance for 1 Megohm for a Three Phase Busbar Fault

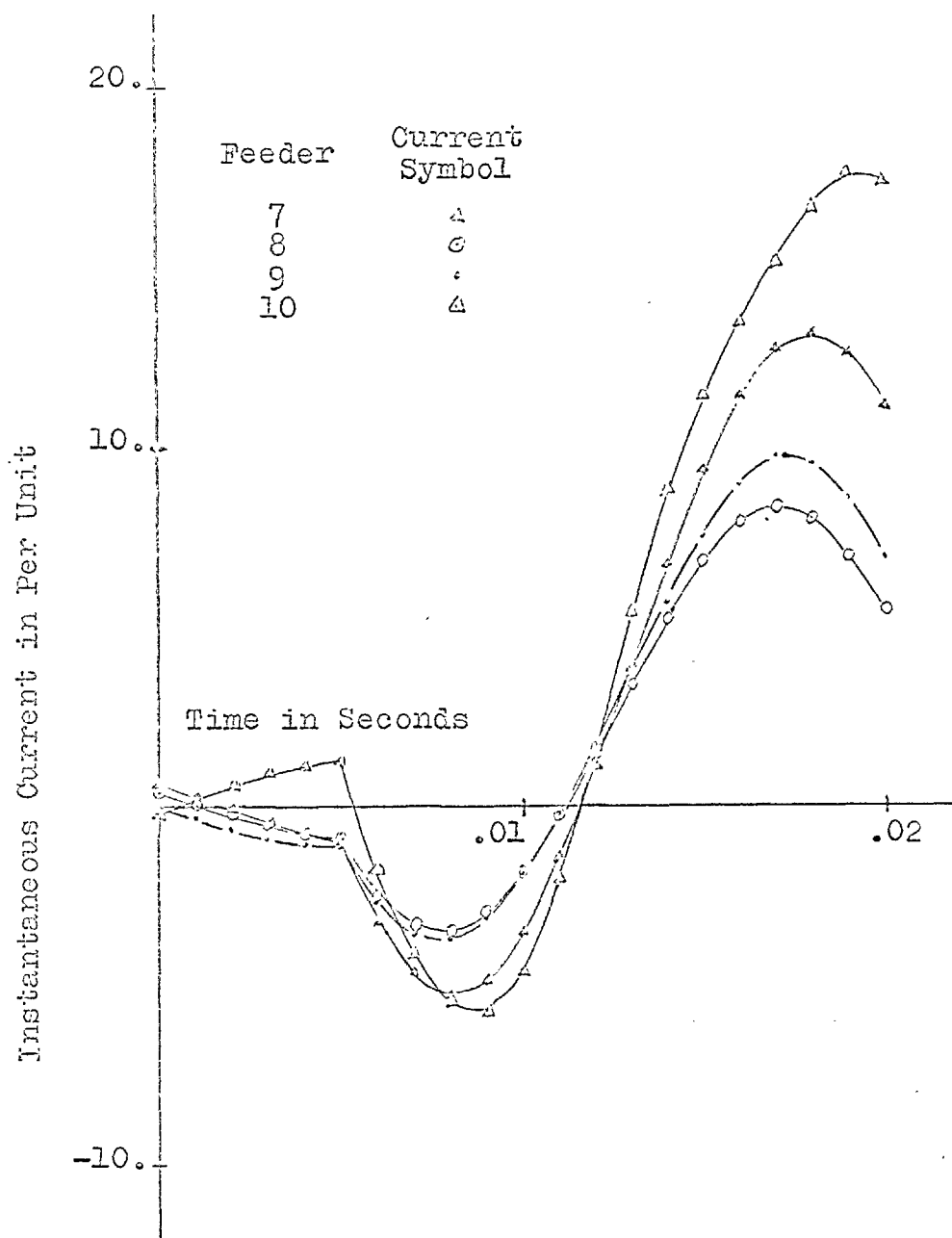


Figure 4.10 Phase b Primary Current for a Busbar Fault between Lines b - to - c

primary current is dependent upon the parameters of the power source and the impedance of the network to the fault location. However for a line - to - line fault, a busbar voltage remains and the primary current is influenced by it. The primary current in line c after the occurrence of this fault is approximately the mirror image of line b current. But some power flows on the faulted lines as well as on the unfaulted line associated with phase a. For a three phase fault the convention given in Section 2.2 for motoring and generating action is maintained for the instantaneous voltage and current of all phases. But for a line - to - line fault this convention is maintained for phase b and not maintained for phase c.

The current transformer and operational relay secondary waveform on phase b are given in Figure 4.11 for a circulating current scheme during a line - to - line fault.

Figure 4.12 shows the linear coupler output for phase b during a line - to - line fault.

4.9 Single Line - to - Ground Fault Waveforms

Figure 4.13 gives the primary current for a single line - to - ground fault at the busbar of the typical substation. The waveform of the faulted phase for a single line - to - ground fault resembles the waveform of phase a of the three phase fault of Figure

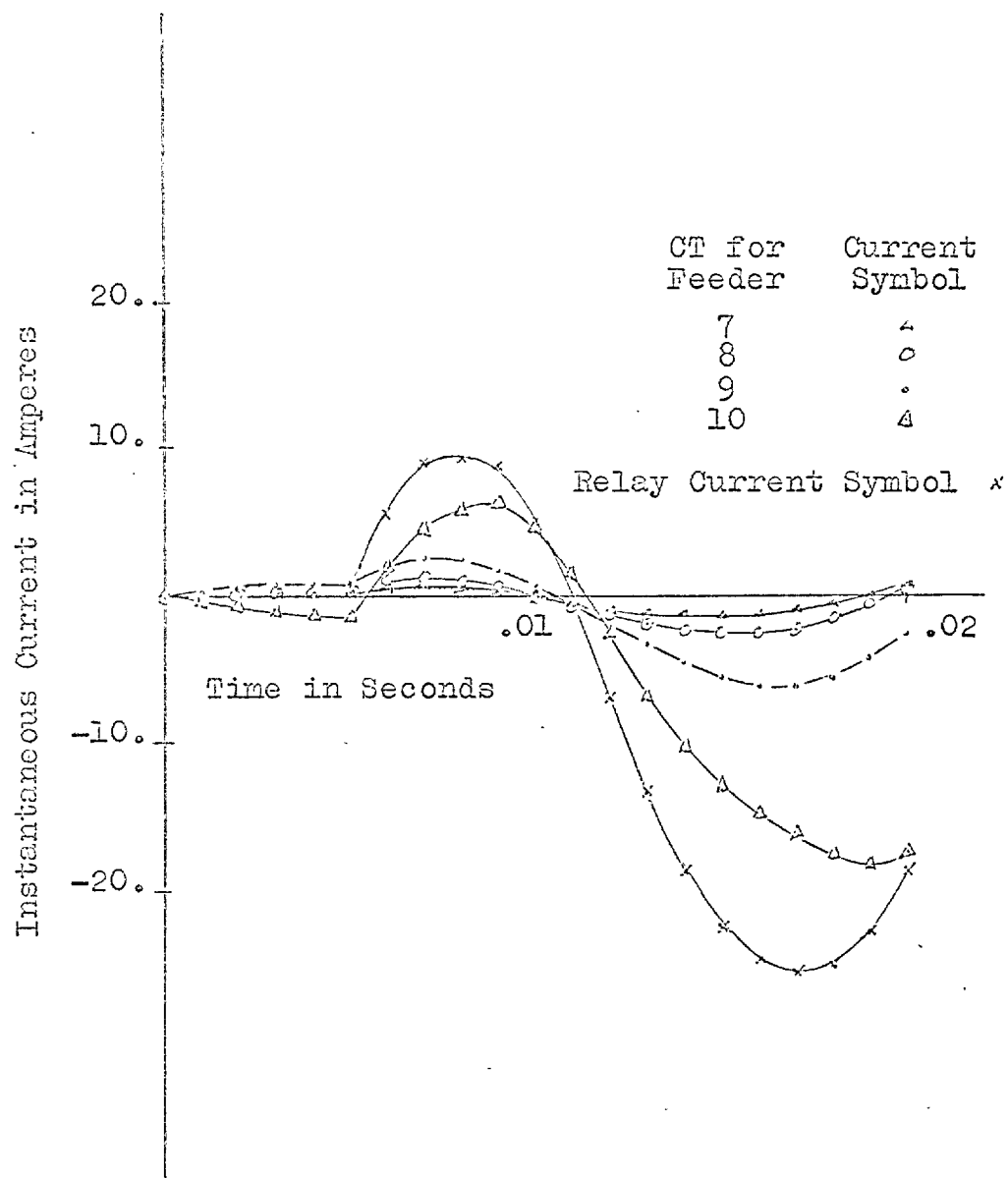


Figure 4.11 Current Transformer and Relay Waveforms for a Line - to - Line Busbar Fault

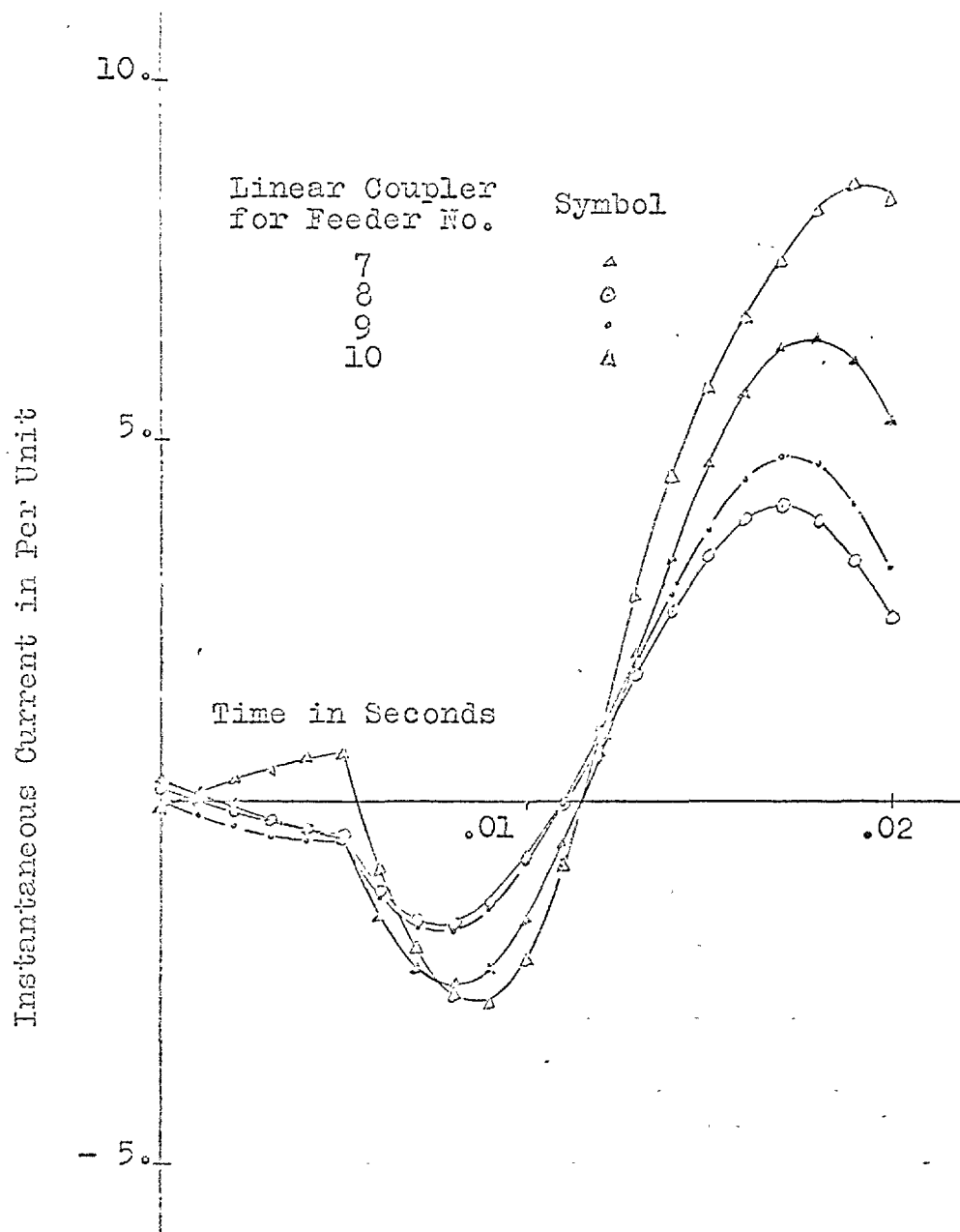


Figure 4.12 Linear Coupler Waveform for Output Resistance of R_R for a Line - to - Line Busbar Fault

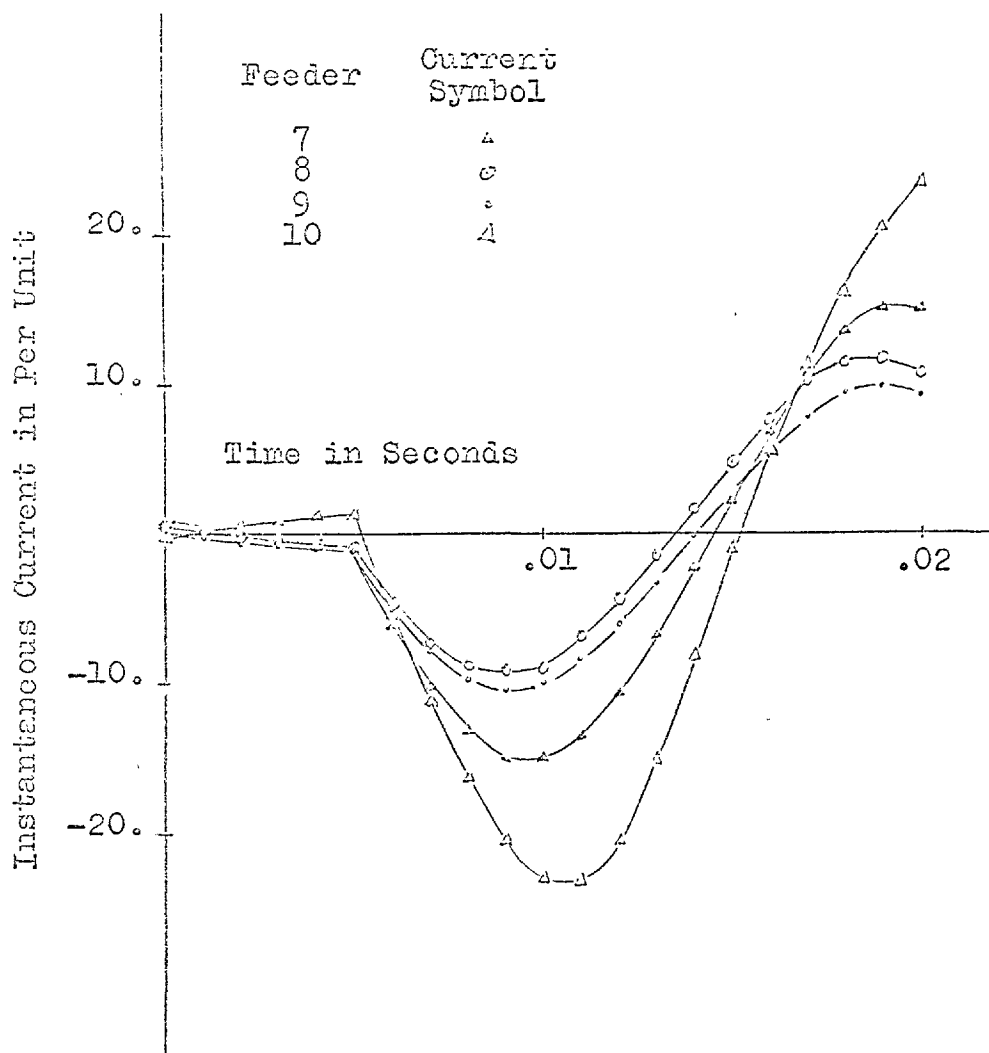


Figure 4.13 Primary Currents for Single Line - to - Ground Busbar Fault

4.4. The behaviour of the network is similar to a three phase fault since the single line - to - ground fault divides the network into four parts each operating independently.

The circulating current operational relay and current transformer waveforms for the faulted phase of a single line - to - ground fault are given in Figure 4.14. The linear coupler output waveform for this fault is given in Figure 4.15.

4.10 Sampling and Integration

If it is possible to obtain an accurate sample of instantaneous primary current from each feeder, busbar protection can be achieved as outlined in Section 1.1.1. Since the difficulties of accurate transducer operation occurs when it is attempted to provide power through the transducer for protective equipment operation a transducer which does not require maximum power transfer is investigated here. In order to have a minimum of power transfer by the transducer its output is sampled by a digital device. The sum of the values sampled for each phase from all feeders connected to the busbar is taken. To obtain a voltage sample proportional to current an output impedance from the transducer on which the voltage can be determined is required. If this impedance is very large the voltage across it is not proportional to primary current as shown in Figure 4.9.

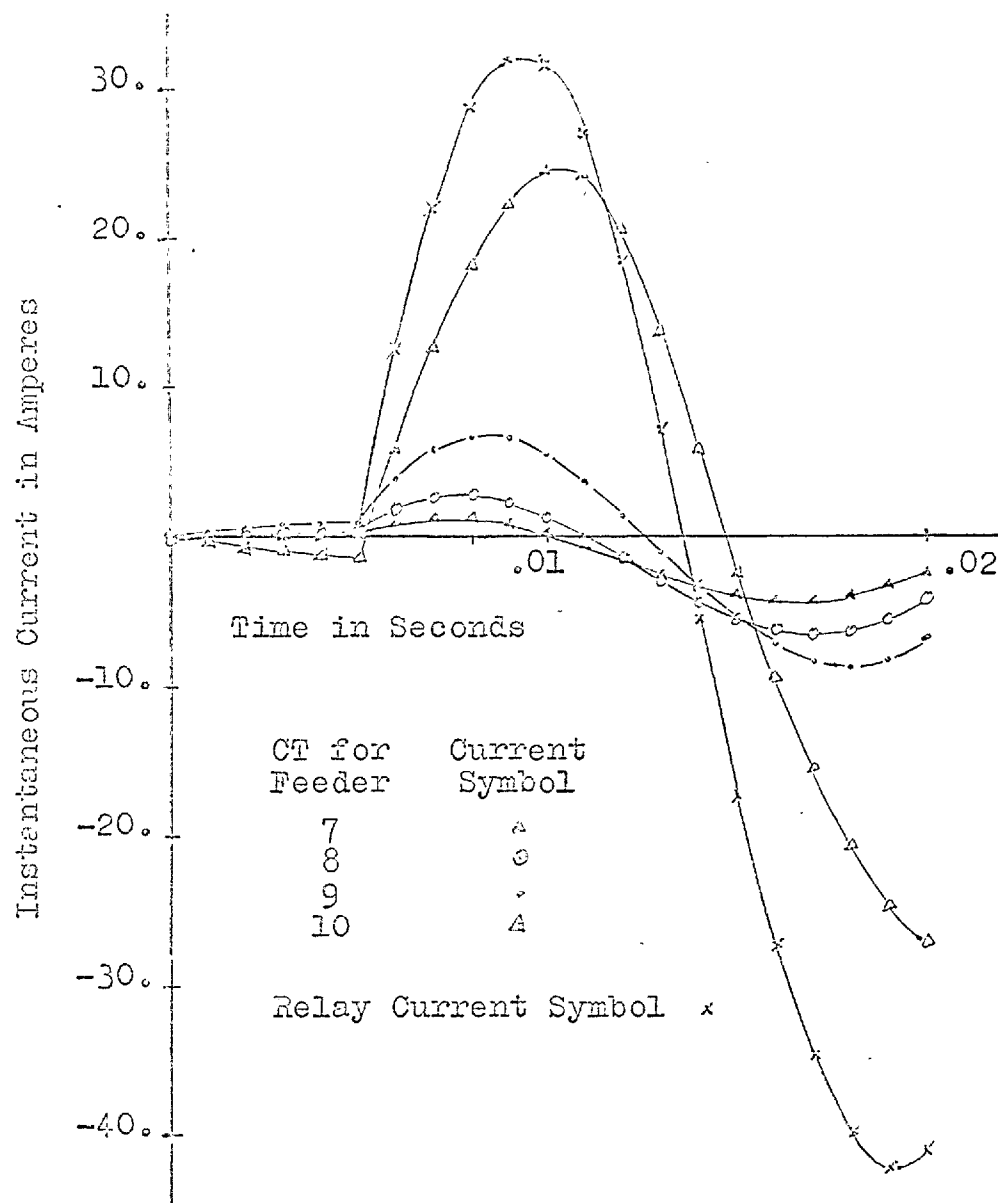


Figure 4.14 Current Transformer and Relay Waveforms for a Line-to-Ground Busbar Fault

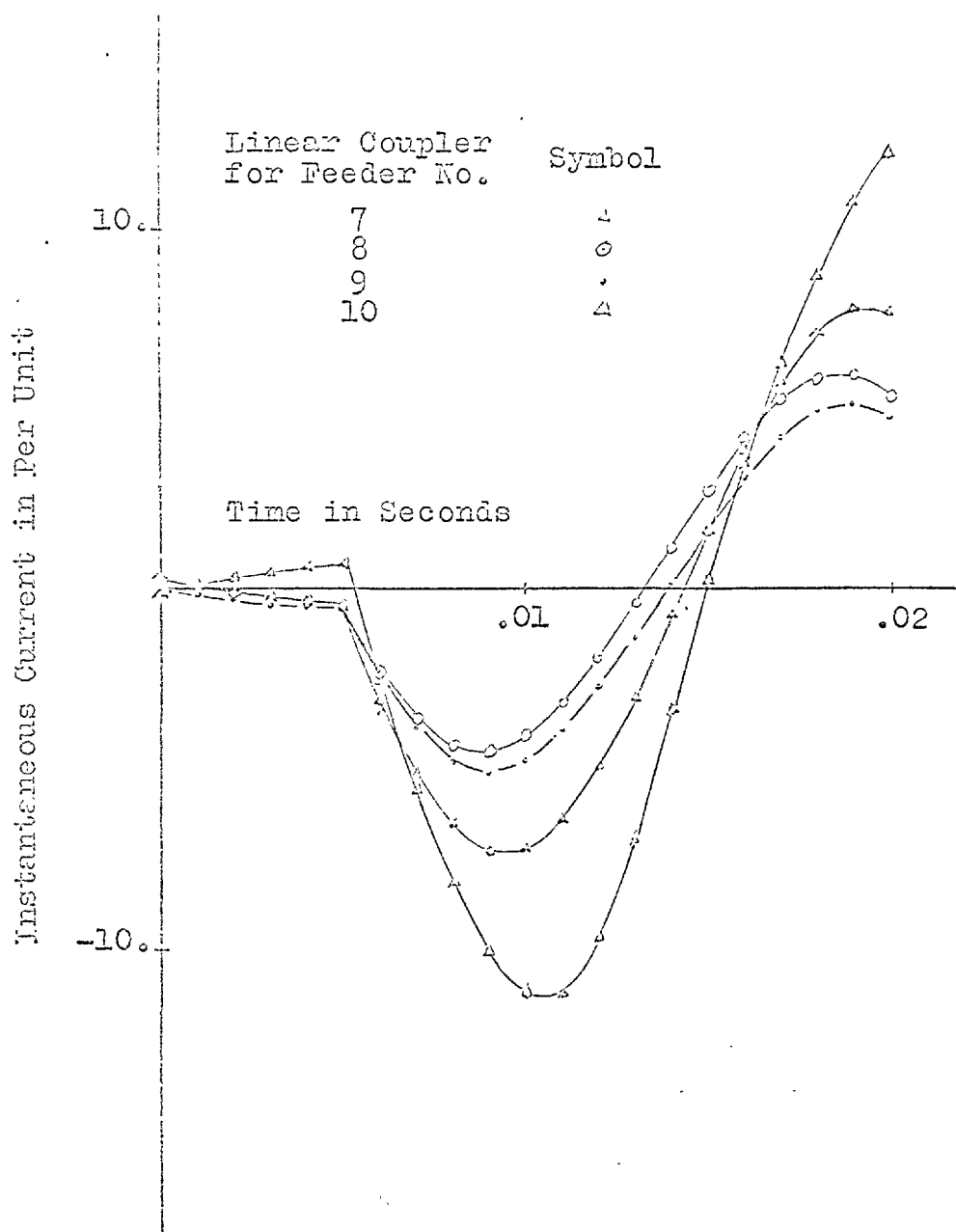


Figure 4.15 Linear Coupler Waveform for Output Resistance of R_R for a Single Line - to - Ground Busbar Fault

In order that the effect of propagation of surges between points might be investigated the long line representation developed in Sections 2.9 and 3.2.6 is used. Figure 4.16 gives the busbar fault waveforms for this representation. A sampling method which integrates linear coupler output over variable lengths of time is used to determine the value to be fed to an analogue to digital convertor. Values from the convertors are summed and this magnitude is used for protection according to Kirchhoff's second law.

The values used for line simulation are given in Appendix Section A.5. The simulation time constant T_1 is very large compared to one cycle over which the sampling is done. The increased calculation required by the more complex line simulation can be offset by greatly reducing T_1 without loss of accuracy. Thus other parameters are used for this simulation for ease in determining the network initial conditions. The primary parameters for this simulation are given in Appendix Section A.5, the calculated parameters and those determined from Equations (3.14), (3.15), (3.16), (3.17) and (3.18) are given in Appendix Section A.6. Parameters associating real and reactive power flow and the required initial conditions are given in Appendix Section A.7.

4.11 Methods of Current Summation

Busbar protection is now almost exclusively of the circulating current type because this method is

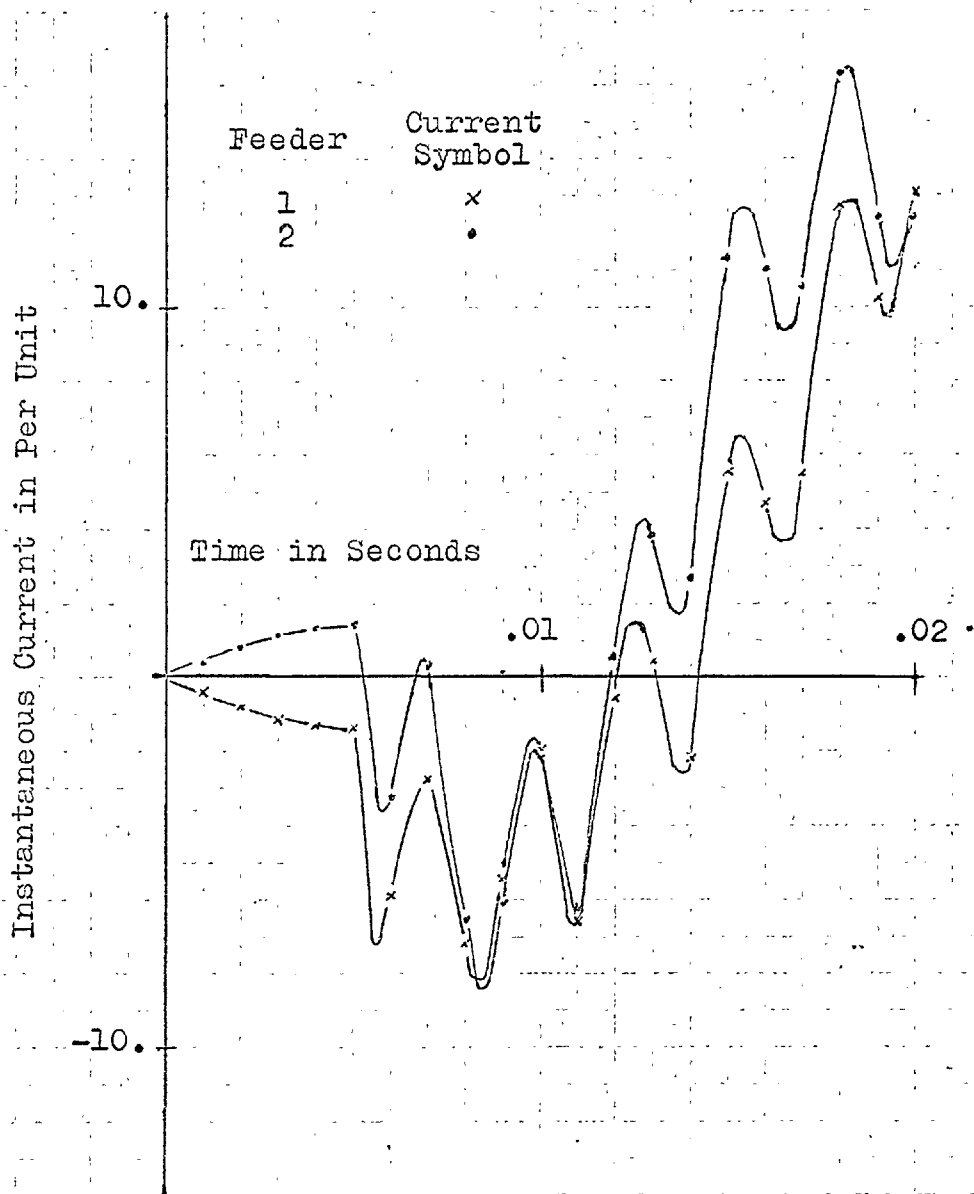


Figure 4.16 Primary Currents for Three Phase Busbar Fault with Long 275 kV Transmission Line Representation

well suited to the conventional type of CTs and relays. The development of this method is associated with the reliability of the equipment available, its sturdy construction, and use of components with which the operational and maintenance staff are familiar. As the system developed many of the features inherent in a circulating current scheme have become with time to be regarded as desirable features for busbar protection. With the advancement of technology, improved materials and components could lead to a better application of old techniques or the introduction of new methods.

It has been proposed (17) that the time for detection of busbar faults can be reduced by the introduction of a protection scheme using integrated samples of primary network currents and analogue to digital conversion with digital summation. The criterion for tripping of busbar breakers is based on Kirchhoff's second law. Using this method to detect busbar faults a technique is required to control substation reswitching operations automatically so that security of supply is maintained during busbar fault conditions. This technique is developed along with methods for supervising manual switching instructions in Chapters 5 and 6.

CHAPTER 5

LOGIC PROCEDURES

5.1 The Purpose of Logic

In order to control substation busbar switching it was stated in Chapter 1 that methods based on logic would be investigated. In this chapter the theory of some of the logic applied to substation control is outlined. In the subsequent chapters this theory (27) is applied to substation control.

5.2 The Logic Forms

To determine and store the information required by a substation controller so that it performs the desired operations safely and intelligently, it is necessary to develop a method of manipulating logic arguments and of storing the logic for these operations.

Logical arguments are not possible without a form of language of which there are two generally accepted forms. The calculus of propositions (20) deals with logical connectives linking propositional variables and, strictly speaking, should be formalised language sentences. This language is useful for switching problems because it can be used to transform expressions into their conjunctive and disjunctive forms (11). The algebra of classes, which is frequently referred to as

Boolean algebra, is the symbolical study of relations between classes. In Appendix B the definition of Boolean algebra is given.

Switches are like bounds of a Boolean algebra, that is, they can be 'on' or 'off'. Because of this analogy, problems in switching have been solved using some of the principles of Boolean algebra. The application to switching problems is generally attributed to Shannon (61), but it must be noted that he favoured the calculus of propositions rather than Boolean algebra. Since the elements used in switching are limited to two possible and exclusive values, 0 and 1, a switching algebra (38) will be constructed here in terms of 0 and 1.

Using the Boolean operator $\cdot$, two elements x and y will have an output table as follows.

x	y	output
0	0	0
0	1	0
1	0	0
1	1	1

Table 5.1

The distinction between a Boolean algebra (8) and a switching algebra must be kept clear. The definition of a Boolean algebra, given in Appendix B, shows that its elements are not restricted to two states, whereas

the elements of a switching algebra are. In a switching algebra the terms x and y are meaningless unless the accompanying table of values is given. In Table 5.1 these values are given in columns 1 and 2. Then column 3 must be added in order to describe a function. In Boolean algebra form the output of Table 5.1 can be written as $x \cdot y$.

The purpose of introducing switching algebra is to develop a simple way of representing functions of more involved combinations of Boolean operators (69).

5.2.1 Boolean Binary Operation

Figure 5.1 shows a double busbar substation with three changeover switches x_1 , x_2 and x_3 . Each switch can be in either of two states (x_1 or $\overline{x_1}$, x_2 or $\overline{x_2}$, x_3 or $\overline{x_3}$). For example, if f_1 represents the input to the substation and if switch x_1 is in the x_1 state power is supplied to busbar M, and if it is in the $\overline{x_1}$ state power is supplied to the busbar R. An expression in Boolean algebra form can be obtained for feeders f_2 and f_3 when the following conditions are satisfied.

$$f_2 = (x_1 \cdot x_2) \vee (\overline{x_1} \cdot \overline{x_2}) \quad (5.1)$$

$$f_3 = (x_1 \cdot x_3) \vee (\overline{x_1} \cdot \overline{x_3}) \quad (5.2)$$

In switching algebra these equations can be written in the form of the following table.

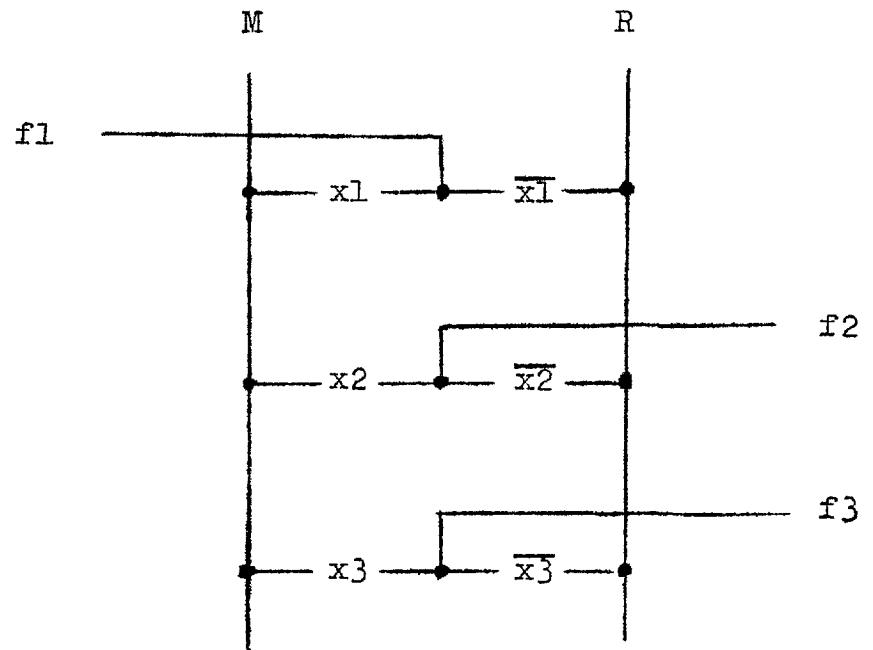


Figure 5.1 Switch Arrangement

x1	x2	x3	f2	f3
0	0	0	1	1
1	0	0	0	0
0	1	0	0	1
1	1	0	1	0
0	0	1	1	0
1	0	1	0	1
0	1	1	0	0
1	1	1	1	1

Table 5.2

In columns 1, 2 and 3 the values of elements x1, x2 and x3 are given and switching functions of these values are described for f2 and f3 in columns 4 and 5 respectively. Obviously this table will soon become too long and inconvenient to reproduce each time it is required. However the following notation will be used to denote columns 1, 2 and 3.

$$\begin{bmatrix} x1 & x2 & x3 \end{bmatrix}$$

With the introduction of this notation the order of the exclusive values becomes important. The method of assigning these values is to take a binary progression from row to row with the least significant digit in each row in the first column. Thus the first three columns of Table 5.2 become

$$\begin{bmatrix} x_1 & x_2 & x_3 \end{bmatrix}$$

0
1
2
3
4
5
6
7

The following tables give another method (20) of showing when f2 and f3 are energised.

	x1 x2				
x3	00	01	11	10	
0	1	0	1	0	f2
1	1	0	1	0	

Table 5.3

	x1 x2				
x3	00	01	11	10	
0	1	1	0	0	f3
1	0	0	1	1	

Table 5.4

In these tables the exclusive values of x1 and x2 are listed horizontally. By listing values of x3 vertically

the eight co-ordinates obtained can be used to represent the eight rows of Table 5.2 in a matrix. The elements of the matrices in Tables 5.3 and 5.4 are equivalent to columns 4 and 5 respectively of Table 5.2. With this notation the order of the exclusive values again becomes important.

The switching algebra representation of $f2 \cdot f3$ is

$$\begin{array}{c}
 \text{x1 x2} \\
 \text{x3} \quad 00 \ 01 \ 11 \ 10 \\
 0 \quad \begin{array}{|c|c|c|c|} \hline 1 & 0 & 1 & 0 \\ \hline 1 & 0 & 1 & 0 \\ \hline \end{array} \cdot \begin{array}{|c|c|c|c|} \hline 1 & 1 & 0 & 0 \\ \hline 0 & 0 & 1 & 1 \\ \hline \end{array} = \begin{array}{|c|c|c|c|} \hline 1 & 0 & 0 & 0 \\ \hline 0 & 0 & 1 & 0 \\ \hline \end{array} \quad (5.3)
 \end{array}$$

This represents the condition when both feeders $f2$ and $f3$ in Figure 5.1 are energised at the same time. In a similar fashion it can be shown that the solution of $f2 \vee f3$ is

$$\begin{array}{c}
 \text{x1 x2} \\
 \text{x3} \quad 00 \ 01 \ 11 \ 10 \\
 0 \quad \begin{array}{|c|c|c|c|} \hline 1 & 0 & 1 & 0 \\ \hline 1 & 0 & 1 & 0 \\ \hline \end{array} \vee \begin{array}{|c|c|c|c|} \hline 1 & 1 & 0 & 0 \\ \hline 0 & 0 & 1 & 1 \\ \hline \end{array} = \begin{array}{|c|c|c|c|} \hline 1 & 1 & 1 & 0 \\ \hline 1 & 0 & 1 & 1 \\ \hline \end{array} \quad (5.4)
 \end{array}$$

This represents the condition when either $f2$ or $f3$ in Figure 5.1 is energised.

Equations (5.3) and (5.4) show how the Boolean

operators can be applied to a switching matrix, however there now arises another distinction between a Boolean algebra and a switching algebra. The Boolean operators do not form groups whereas the elements of a switching algebra under a new operator shown below form an ordered group. The definition of a group is given by McCoy (39). The following section gives the use of this new operator.

5.2.2 Matrix Product Operation

If the values of f2 and f3 given in columns 4 and 5 of Table 5.2 are transposed to form rows, and the values of x1, x2 and x3 given in columns 1, 2 and 3 of Table 5.2 are considered to be an ordered progression Table 5.2 can be written as the following matrix equation using the new operator.

$$\begin{bmatrix} 1 & 0 & 0 & 1 & 1 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 & 0 & 1 & 0 & 1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} = \begin{bmatrix} f_2 \\ f_3 \end{bmatrix} \quad (5.5)$$

where

$$\begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix}$$

is the transpose of $[x_1 \ x_2 \ x_3]$ given in Section 5.2.1. In regular matrix form Equation (5.5) becomes

$$[B][x] = [f] \quad (5.6)$$

where $[B]$ is the matrix of coefficients given in Equation (5.5) and $[x]$ and $[f]$ are vectors representing the terms

$$\begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} \quad \text{and} \quad \begin{bmatrix} f_2 \\ f_3 \end{bmatrix} \quad \text{respectively.}$$

If the binary progression

$$\begin{bmatrix} 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 1 & 1 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 \end{bmatrix}$$

Table 5.5

is written in the form

$$\begin{bmatrix} \overline{x_1} & x_1 & \overline{x_1} & x_1 & \overline{x_1} & x_1 & \overline{x_1} & x_1 \\ \overline{x_2} & \overline{x_2} & x_2 & x_2 & \overline{x_2} & \overline{x_2} & x_2 & x_2 \\ \overline{x_3} & \overline{x_3} & \overline{x_3} & \overline{x_3} & x_3 & x_3 & x_3 & x_3 \end{bmatrix}$$

Table 5.6

it can be combined with each row of B ,

$$\begin{bmatrix} 1 & 0 & 0 & 1 & 1 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 & 0 & 1 & 0 & 1 \end{bmatrix},$$

to obtain the following Boolean expressions.

$$\begin{aligned}
& (1 \cdot \overline{x_1} \cdot \overline{x_2} \cdot \overline{x_3}) \vee (0 \cdot x_1 \cdot \overline{x_2} \cdot \overline{x_3}) \vee (0 \cdot \overline{x_1} \cdot x_2 \cdot \overline{x_3}) \\
& \vee (1 \cdot x_1 \cdot x_2 \cdot \overline{x_3}) \vee (1 \cdot \overline{x_1} \cdot \overline{x_2} \cdot x_3) \vee (0 \cdot x_1 \cdot \overline{x_2} \cdot x_3) \\
& \vee (0 \cdot \overline{x_1} \cdot x_2 \cdot x_3) \vee (1 \cdot x_1 \cdot x_2 \cdot x_3) = f_2
\end{aligned} \tag{5.7}$$

and

$$\begin{aligned}
& (1 \cdot \overline{x_1} \cdot \overline{x_2} \cdot \overline{x_3}) \vee (0 \cdot x_1 \cdot \overline{x_2} \cdot \overline{x_3}) \vee (1 \cdot \overline{x_1} \cdot x_2 \cdot \overline{x_3}) \\
& \vee (0 \cdot x_1 \cdot x_2 \cdot \overline{x_3}) \vee (0 \cdot \overline{x_1} \cdot \overline{x_2} \cdot x_3) \vee (1 \cdot x_1 \cdot \overline{x_2} \cdot x_3) \\
& \vee (0 \cdot \overline{x_1} \cdot x_2 \cdot x_3) \vee (1 \cdot x_1 \cdot x_2 \cdot x_3) = f_3
\end{aligned} \tag{5.8}$$

Each set of terms within brackets represents a row in Table 5.1 and is equivalent to the appropriate descriptive value (column 4 for f_2 , column 5 for f_3) and the first three columns. In this way Equations (5.7) and (5.8) are used to give the fully expanded Boolean algebra forms of the switching algebra of Equations (5.5) or (5.6). To interpret the meaning directly from Equations (5.7) and (5.8) in Boolean algebra form the definition in Appendix B is followed strictly. From the bound property for $\cdot$, given in Appendix Section B.3, the following substitutions can be made.

$$(1 \cdot \overline{x_1} \cdot \overline{x_2} \cdot \overline{x_3}) = (\overline{x_1} \cdot \overline{x_2} \cdot \overline{x_3}) \tag{5.9}$$

and

$$(0 \cdot x_1 \cdot \overline{x_2} \cdot \overline{x_3}) = 0 \tag{5.10}$$

Also, from the bound property for $\vee$, the following

substitution can be made.

$$(\overline{x_1} \cdot \overline{x_2} \cdot \overline{x_3}) \vee 0 = (\overline{x_1} \cdot \overline{x_2} \cdot \overline{x_3}) \quad (5.11)$$

Using the complementary law for $\vee$ given in Appendix Section B.4,

$$(\overline{x_3} \vee x_3) = 1, \quad (5.12)$$

and the bound property for $\cdot$ as illustrated above the following substitution can be made.

$$(\overline{x_1} \cdot \overline{x_2} \cdot \overline{x_3}) \vee (\overline{x_1} \cdot \overline{x_2} \cdot x_3) = (\overline{x_1} \cdot \overline{x_2} \cdot 1) = (\overline{x_1} \cdot \overline{x_2}) \quad (5.13)$$

By this method it can be shown that Equation (5.7) is equivalent to Equation (5.1) and similarly Equation (5.8) is equivalent to Equation (5.2).

Vector representation of a matrix leads to a further simplification in the use of this operator.

5.2.3 A Convenient Method of Matrix Representation

In order to specify the matrix representation of Equations (5.7) and (5.8) given in Equation (5.5) a method of vector representation is employed (26). Vector representation can be given to the Boolean matrix $[B]$ by regarding each column of the matrix as binary numbers. The decimal equivalent is obtained from the binary representation by taking the value in the top row as the

least significant digit. For example, from the matrix

$$[B] = \begin{bmatrix} 1 & 0 & 0 & 1 & 1 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 & 0 & 1 & 0 & 1 \end{bmatrix} \quad (5.14)$$

the vector

$$\vec{B} = [3 \ 0 \ 2 \ 1 \ 1 \ 2 \ 0 \ 3] \quad (5.15)$$

is obtained.

A vector $\vec{\lambda(3)}$ is equivalent to the binary progression of minimal polynomials in a Boolean algebra as illustrated by Table 5.6. Thus for a three element matrix

$$\vec{\lambda(3)} = [0 \ 1 \ 2 \ 3 \ 4 \ 5 \ 6 \ 7] \quad (5.16)$$

The equivalent Boolean matrix is

$$\lambda(3) = \begin{bmatrix} 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 1 & 1 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 \end{bmatrix} \quad (5.17)$$

Note the relationship between this Boolean matrix and the progression of x_1 , x_2 and x_3 in Table 5.2.

With the addition of the vector $\vec{\lambda(n)}$ Boolean matrix multiplication can be defined and the properties of identity and inverse can be

demonstrated. This is shown in Appendix C.

5.3 Karnaugh Map Method

The table, Table 5.3, of Section 5.2.1 can be called a map. This map was developed by Karnaugh (30) as a convenient method of representing switching functions.

In order to illustrate the use of a Karnaugh map four variables, which can be designated w, x, y, z , are used to form elements of a Boolean algebra. By the complementary law given in Appendix Section B.4, each variable must have two elements in the set. The variable w has elements w and $\bar{w}$, and similarly variables x, y and z have elements x and $\bar{x}$, y and $\bar{y}$, z and $\bar{z}$. Sixteen possible combinations of these four variables are determined by the Boolean algebra expression of the binary progression developed in Section 5.2.2. Each of these combinations is assigned a position in accordance with Figure 5.2.

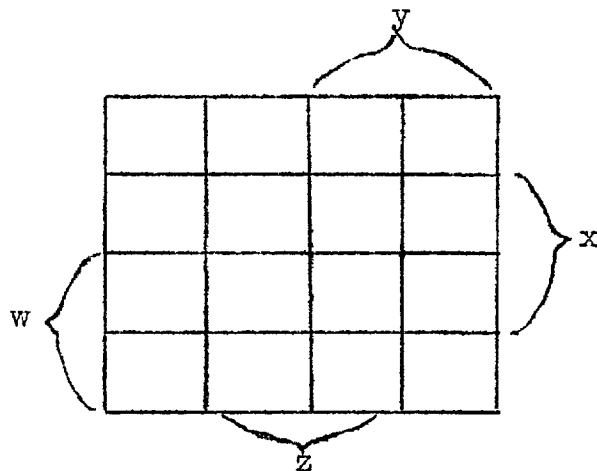


Figure 5.2 Element Assignment

In this figure rows 3 and 4 are assigned to the element w , therefore rows 1 and 2 are assigned to the element $\bar{w}$. The accompanying exclusive values of $wxyz$ (see Section 5.2) can be placed in the appropriate cells of Figure 5.2 to produce a switching algebra form as shown in Figure 5.3. The two rows indicated by w in Figure 5.3 denote the positions in which w has a value of '1'. In a similar manner these positions are indicated for x , y and z .

0000	0001	0011	0010
0100	0101	0111	0110
1100	1101	1111	1110
1000	1001	1011	1010

Figure 5.3 Cell Assignment

This map method can be used to illustrate a method of simplifying a function. By adopting the representation of Figure 5.3 given in Figure 5.4, switching functions of w , x , y , z can be described in the manner used in Equations (5.7) and (5.8). In Section 5.2.2 Equation (5.7) was simplified to the form of Equation (5.1). This process is much easier to follow when done by the Karnaugh map method. Simplification in this map depends upon the ease of observing adjacencies

	y z			
w x	00	01	11	10
00				
01				
11				
10				

Figure 5.4 Karnaugh Map

in the map. To make these adjacencies easier to see, '0' is usually dropped from the cells in which it occurs. The Karnaugh map of Equation (5.7) in this form can be obtained by modifying Table 5.3 and is given in Figure 5.5.

	x1 x2			
x3	00	01	11	10
0	(1)		(1)	
1	(1)		(1)	

f2

Figure 5.5 Function Representation

The cells are grouped into rectangles, squares, rows, columns and pairs. In the map there are two column groupings possible as shown by the enclosing loops in Figure 5.5. By inspection of the group in column 1 it can be seen that there is an entry for both states of x_3 . Therefore it can be omitted from the Boolean

algebra expression for that column. By this argument both states of x_3 can be omitted for column 3. The Boolean equation in x_1 and x_2 representing Figure 5.5 can by inspection be seen to be

$$f_2 = (\overline{x_1} \cdot \overline{x_2}) \vee (x_1 \cdot x_2) \quad (5.18)$$

which is the same as Equation (5.1), the simplified expression.

Using the principles described in the sections above switching maps can be developed.

5.4 Stability in Switching

One of the features of the switching controller, mentioned in Section 1.4.3, is that it utilises a memory. That is, time is an element and the outputs are functions of the present input and also of past switching arrangements. Inputs for circuit memory (55) are called primaries, and their states are represented by x 's. Outputs are represented by Z 's. The memory of these circuits are called secondaries and their states are represented by y 's. Since there is a time delay before secondaries change to a new state their next state is represented by Y 's.

When the next state of the secondary is the same as the present state the secondary is stable. When the next state of the secondary is not the same as the present state, the secondary is unstable. Stable

conditions are then obtained when

$$\begin{array}{l} y = 1 \quad \text{and} \quad Y = 1 \\ \text{or} \\ y = 0 \quad \text{and} \quad Y = 0 \end{array}$$

and unstable states are obtained when

$$\begin{array}{l} y = 1 \quad \text{and} \quad Y = 0 \\ \text{or} \\ y = 0 \quad \text{and} \quad Y = 1 \quad . \end{array}$$

5.5 The Formalised Procedure

The first four sections of this chapter outline some of the general considerations of logic manipulation. This section outlines the steps used in Chapter 6 in the development of the computer program for the switching controller (18).

5.5.1 Primitive Flow Table

The primitive flow table is constructed from the arrangement of substation feeder switches and constraints. The constraints determine the columns that occur in the map. A different state number is assigned to each stable switching state which is determined by the relevant information for each switch. Since this is a preliminary step in the assignment, the number is assigned by convenience. Distinction can be

made between different permitted orders of switch operation by assigning different numbers to them and undesirable orders of switching are avoided if they are not given state assignments. For example, a breaker and an isolator in the same feeder must be operated in the correct sequence. The primitive flow table for the switching of this feeder is shown in Figure 5.6 and is developed as follows. The inputs are called x_1 , which is assigned to the breaker, and x_2 , which is assigned to the isolator. Since there are no ~~re~~ constraints all elements in the switching algebra are permitted as inputs. The inputs are listed as column headings in Figure 5.6.

x1 x2				
00	01	11	10	Z
1s	2		3	0
	2s	4		0
	5	4s		1
1	5s			0
1			3s	1

Figure 5.6 Primitive Flow Table

The heading for column 1, which is 00, means that an input signal which requests that both switches be opened has been received. The heading for column ~~2~~²⁴, 01, means that a signal which requests that the isolator be closed and the breaker be opened has been received.

In the output column, headed Z, the signals to be used to control the breaker are listed. 0 means an output signal to open the breaker and 1 means to close the breaker. The output column for the isolator is not given.

Each stable state is assigned a separate row in the body of the table. The letter s is used to signify stable states. With both switches open the stable state 1s exists. From state 1 the next step is to close the isolator, x2, moving horizontally in the table from state 1s to state 2 when the input changes from 00 to 01, and then in the column to stable state 2s, and so on. Vacant positions indicate situations which cannot occur. Therefore from stable state 3s in which the breaker is closed and the isolator is open the only next possible state is 1 and the isolator cannot be closed.

5.5.2 Primary Flow Table

In the development of the primitive flow table it is possible to introduce more stable states than are needed. Two stable states become redundant if they have the same input and output states and if each input change causes the same or equivalent change in stable states. To produce the primary flow table all stable states which can be assigned the same secondary state are determined. This reduces the number of secondary state assignments required. The difference in state

with the same secondary assignment is determined by a difference in input. Stable states which can have the same secondary state assignment are those which have no conflicting state numbers for any change of input. A vacant position does not conflict with state assignment because this position can have any convenient assignment since it has no output (9). To illustrate this by the example in Figure 5.6, rows 1 and 2 can be combined to form the following row

00	01	11	10
1s	2s	4	3

because no conflicting states occur between rows in any one column. However rows 1 and 4 cannot be combined because state 2 and stable state 5s in column 2 have conflicting state numbers.

In a primary flow table with a large number of stable states, generally, there are a large number of ways in which this assignment of secondary states can be accomplished. The method adopted in Chapter 6 of this thesis is to consider the different possible ways of assigning stable states and to test for the assignment which allows the largest number of primitive flow table states to be given the same secondary state assignment.

A primary flow table can be formed from the primitive flow table of Figure 5.6 by combining rows 1

and 2 to form a new row and rows 3, 4 and 5 to form another new row. The resulting primary table is shown in Figure 5.7.

	x1 x2			
	00	01	11	10
a	1s	2s	4	3
b	1	5s	4s	3s

Figure 5.7 Primary Flow Table

An assignment for rows a and b in this table is now required.

5.5.3 Secondary State Assignment Table

To assign secondary states to the stable states in the primary flow table, the state - to - state transition must be examined. For a direct transition between stable states, it is desired to limit the number of transitions in the logic variables as much as possible. For example, if the secondary state assignment of a more complex table is to be accomplished by three logic variables, y_1 , y_2 , y_3 , a transition in these variables from 011 to 101 is to be avoided if the states 111 and 001, which are intermediate or transitional, represent other stable states. The assignment of states is accomplished by examining the flow table for states which are logically adjacent. The stable state number

can now be given more than one logic variable assignment when this does not increase the number of logic variables required. Only one of these assignments can be used as a stable condition but in this way the number of adjacencies (see Section 5.3) can be increased which permits a choice of transition routes to avoid this difficulty.

5.5.4 Secondary Maps

The secondary map is determined from the primary flow table and the secondary state assignment table by substitution. First the corresponding secondary state assignment is substituted for each stable state of the flow table and thus each stable state becomes the same as the present secondary state. Then each unstable state is given an assignment corresponding to the next secondary state. This entry should be the same as the corresponding stable state or may have a transition through an unstable state eventually terminating in the stable state. Assuming that rows a and b of Figure 5.7 have been given secondary state assignments 0 and 1 respectively, Figure 5.8 gives the initial substitution where stable states only are replaced by present states (see Section 5.4).

The map is completed by giving unstable states the assignment of their associated stable states. The completed map is shown in Figure 5.9.

	x1 x2			
y1	00	01	11	10
0	0	0		
1		1	1	1

Figure 5.8 Present State Assignment

	x1 x2			
y1	00	01	11	10
0	0	0	1	1
1	0	1	1	1

Y1

Figure 5.9 Secondary Map

5.5.5 The Output Map

The output map is obtained from the primitive flow table, the primary flow table and the secondary state assignment table. The output for each stable state is defined in the primitive flow table. To determine the output map the output for each stable state is substituted in the stable state location found in the primary flow table. Figure 5.10 shows the output map determined from Figures 5.6 and 5.7 for the y1 assignments of rows a and b.

	x1 x2				
y1	00	01	11	10	
0					Z
1			1	1	

Figure 5.10 Output Map

5.5.6 Boolean Expressions

By the method given in Section 5.3 the Boolean equation equivalent to Figures 5.9 and 5.10 can be written as follows.

$$Y1 = x1 \vee (\overline{x1} \cdot x2 \cdot y1) \quad (5.19)$$

$$Z = y1 \cdot x1 \quad (5.20)$$

This can be used to program the state of logic variable Y1 in the switching controller and the controller output Z.

To make the determination of this function much simpler the computer program of Chapter 6 has been developed.

CHAPTER 6

THE DEVELOPMENT OF THE SWITCHING PROGRAM

6.1 The Switching Controller

The purpose of the switching controller is to perform required network switching in a real-time system. It is intended that the controller should consist of a number of logic variables so that it can be programmed to control any desired network configuration. Since the controller circuitry would consist of only a small number of elements, the assumption is made that controller reliability can be provided by duplication or by error checking and correcting codes. In this way controller security would be improved (23).

The operation of the controller would be either by manual instruction by the substation operator or automatically by protection circuit input signals. All switching performed must be supervised by the controller. If the operator finds that he is unable to perform a desired operation, rather than bypass the controller, he can reprogram it with the aid of an off-line program. The program for the controller and the functions provided by it would be the responsibility of the substation operations staff.

The program which follows illustrates the type of off-line program required for controller programming.

6.2 Program Input

The input to this program is in the form of cards. Each card contains all the information concerning one switch. The name of the switch is entered in the first five columns of each card and all switches which cannot be closed in parallel with it are listed in columns 6 to 25, five columns for each switch. The remaining columns of the card provide space for the listing of switches which must be closed before this switch. There is no required sequence for presenting these cards to the program, but a card, denoted IXX in the first three columns, must follow the last switch card.

6.3 The Generation of Input States

Figure 6.1 gives the flow diagram for the determination of input states. Each switch card is read and the information concerning the network is stored. Each switch in the network is assigned a binary variable equivalent. With this assignment the switching algebra notation given in Section 5.2.2 can be used for denoting input states. For example, if a system consists of five switches the notation 5 represents the input (see Equation (5.17))

x1	x2	x3	x4	x5
1	0	1	0	0

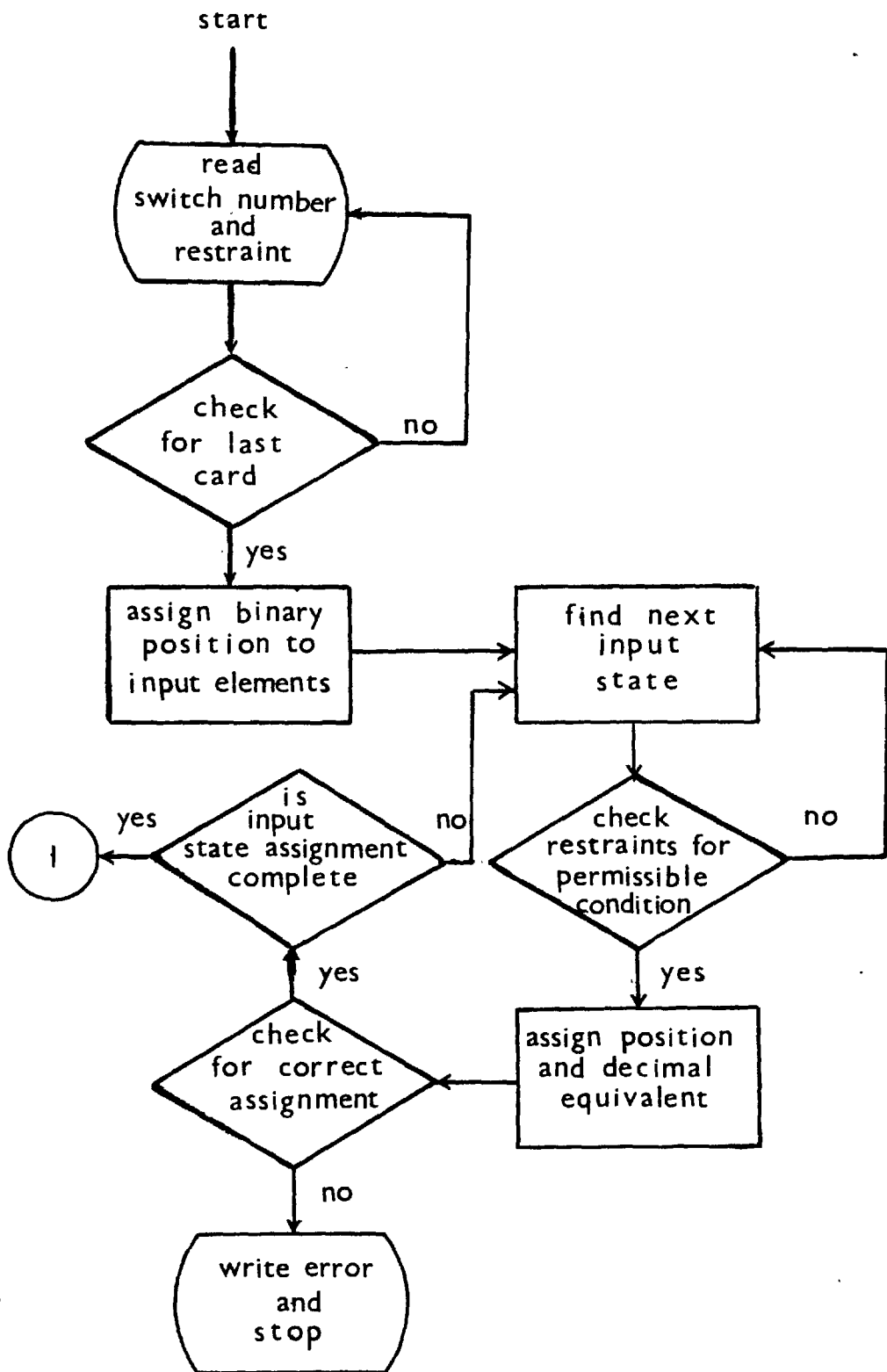


FIGURE 6.1 Input State Generation

Therefore it is important that the listed order of switches be referred to when interpreting the meaning of any switching algebra decimal integer. An initial input state is chosen by the computer program. Then the restraints for the network are checked against this input state by comparing the binary digits which form the input state number. For example, input state 5 represents switches x_1 and x_3 closed together. Input states which are not permitted must be omitted from the input state generation.

Once any one state is formed all input states can be determined. Each permitted input state is given a decimal integer equivalent to facilitate storage in the computer.

When the input state generation is completed the primitive flow table generation starts.

6.4 The Generation of the Primitive Flow Table

Figure 6.2 gives the program flow chart for generation of the primitive flow table. The theory followed in determining this chart is outlined in Section 5.5.1. In order to obtain a starting point a network switching arrangement is assumed. The input state columns of the flow table, which are described in Section 6.3, are scanned to find the input which is equivalent to this network switching arrangement. Since the input state is equivalent to the network arrangement

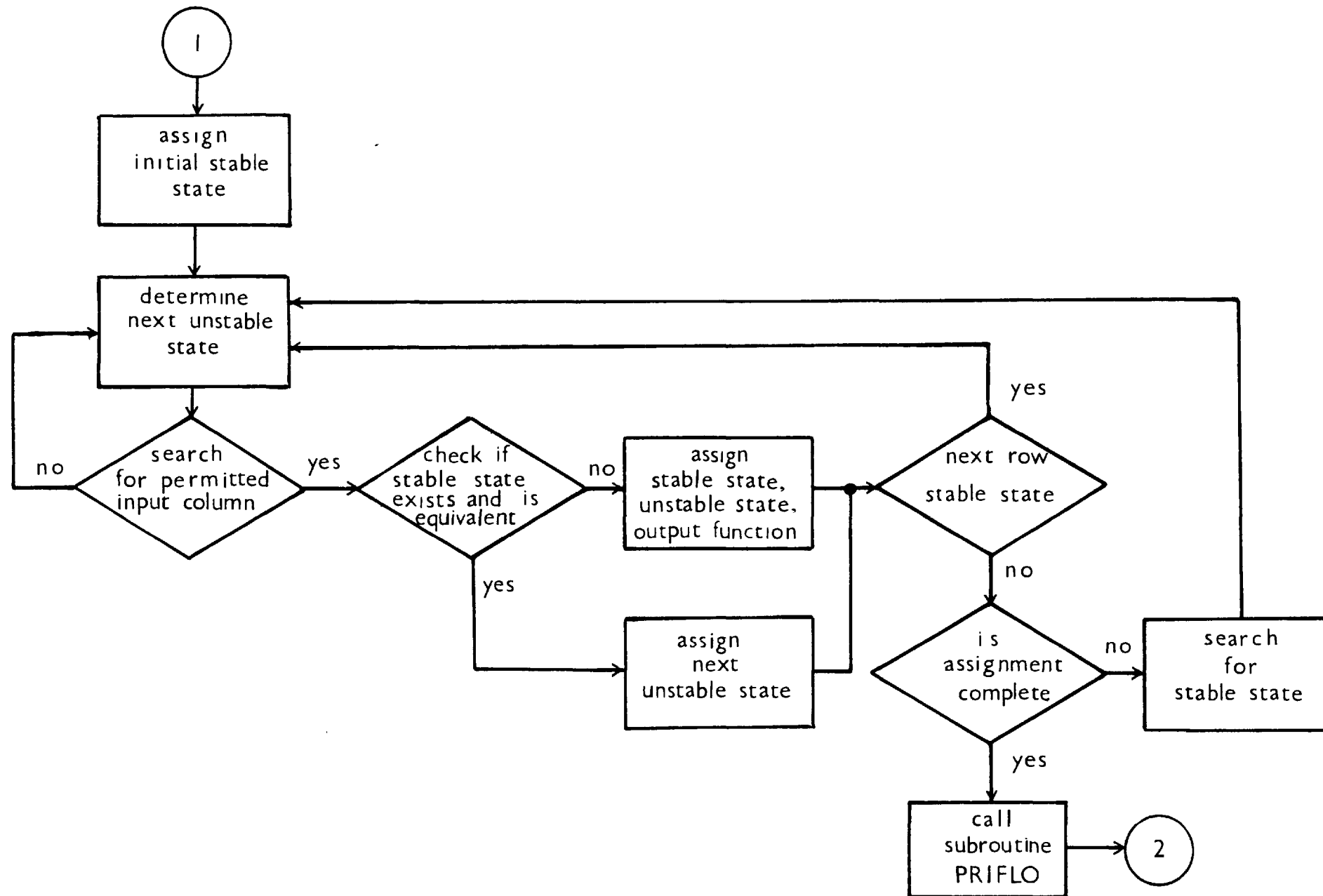


FIGURE 6.2 Primitive Flow Table Generation

this is a stable state. In the primitive flow table each stable state is assigned a row. The row number is used as a state assignment number in the body of the table. Therefore the row number is entered in the row under the input column which was located in the scan above. When the row number and the state number are the same in the primitive flow table the state number represents the present state (see Section 5.4) and is therefore the stable state.

Once a stable state is determined the network arrangement can be systematically tested to determine which switches in the system can be operated. This is done by determining the input which is required by each switching operation, and then the state input columns are searched to find the equivalent column. If no such input exists the switching arrangement tested is not permitted and cannot be given an assignment. If such a column does exist it is then possible for it to become a next state or unstable state (see Section 5.4). Such unstable states are given state assignment equivalent to their own stable state. A change of input causes a change from stable state to next state which in a flow table is a horizontal movement or change within a row. Then the next change is automatically from next state to its own stable state which in a flow table is a vertical movement or change within a column. This means that any states, which are stable or unstable, with the same assignment always occurs only in the same column. To determine if a stable state equivalent to the next state already exists in the primitive flow table a

search is required. Since the state input has already been determined this search can be limited to that column. In a primitive flow table a search for stable states is done by equating a state assignment number to a row number. However once a stable state is found it must be tested to determine if it is equivalent to the next state by comparing network changes. If both states represent the same network change they are equivalent. Therefore the network change associated with a stable state is recorded. If an equivalent stable state is found the next state must be given the stable state row assignment. If no equivalent stable state is found a new row must be taken for a stable state assignment. The next state must be given this assignment and the network change which involved this next state recorded.

The generation is tested to determine if all possible unstable states have been obtained. The process is continued until all unstable state generation is complete.

When the number of rows and the number of states are equivalent the flow table is complete. An incomplete primitive flow table can be finished by systematically searching for all stable states and continuing with the procedure outlined above.

A shift routine to print this table in an intelligible manner, called subroutine PRIFLO, is described in Section 6.9.

When this table is complete a routine is used to combine rows to reduce the number of assignment variables required.

6.5 Row Merging

Figure 6.3 gives the program flow chart for the process of combining rows in the primitive flow table to form the primary flow table. The theory for this is outlined in Section 5.5.2.

Since in the primary flow table there is no relationship between the row number and the stable state the primitive flow table is scanned and each stable state must be indexed for future reference.

When there are a large number of restraints associated with a switching network the number of rows with which any one row can be combined is greatly increased. Since this increases the working space required in the computer with no reduction in the number of variables required for assignment, the number of rows considered is limited to save space. As rows are combined the possible remaining combinations are reduced and therefore more rows must be considered in any subsequent merging operation. Rows in the primitive flow table are examined individually in a systematic manner and the number of each row with which it can be combined (see Section 5.5.2) is stored, until either the storage space is filled or no more possible combinations

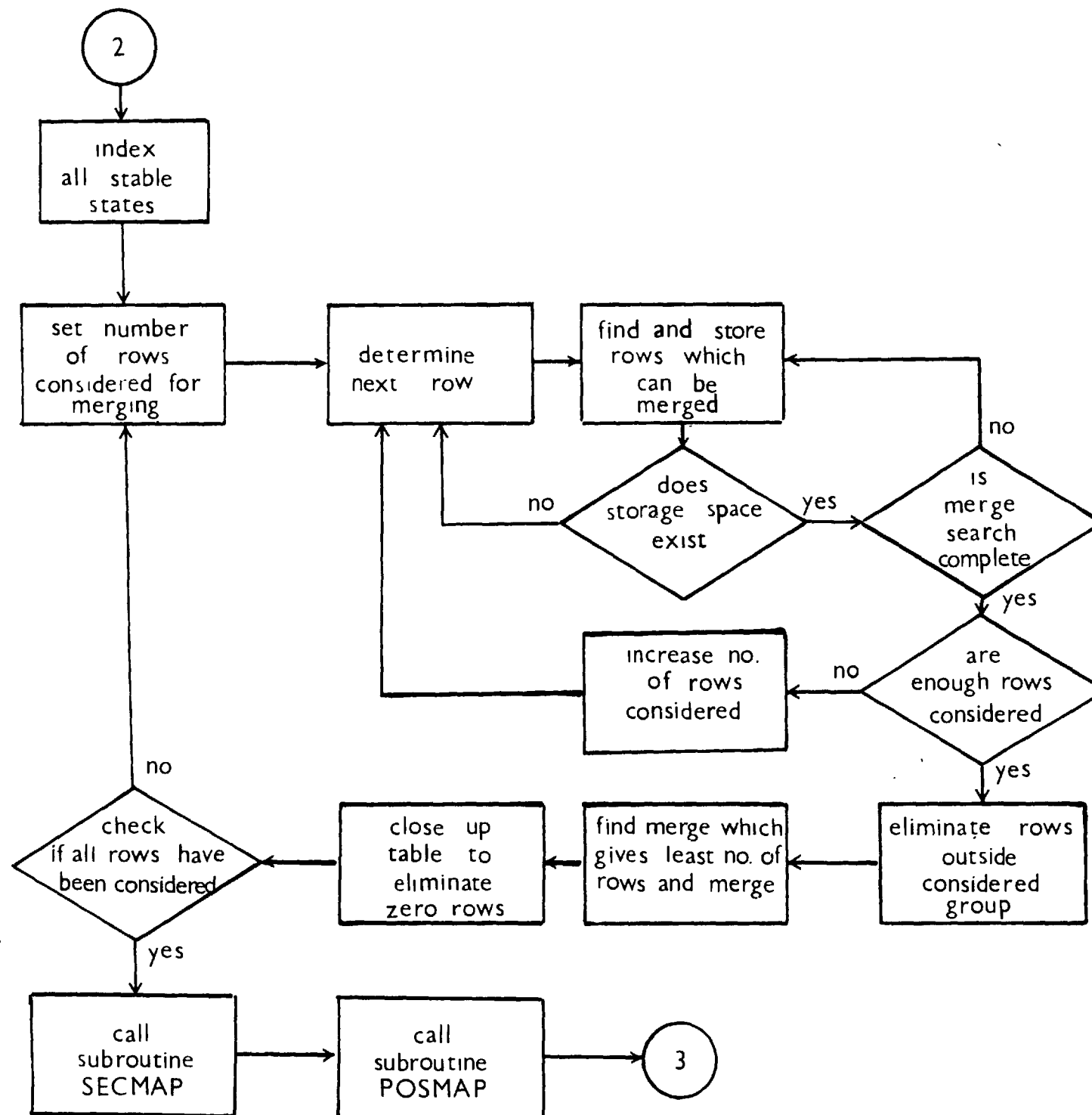


FIGURE 6.3 Row Merging

exist. When the working space is not filled the number of rows examined is increased until eventually all rows in the table are examined at one time.

In the initial stages of combination, examination of the rows in the manner chosen results in combinations of rows which are outside the group being recorded. Since this combination is not in the optimal group the row number thus recorded must be eliminated from it.

Rows are now combined by putting the states which occur in all the rows into only one row and replacing each state in the other rows with a zero. The table is closed up by eliminating all rows containing only zero elements.

As in Section 6.4 a subroutine, called SECMAP, is used to print the primary flow table. The subroutine is described in Section 6.9.

When the primary flow table is complete each row is given a secondary state assignment (see Section 5.5.3). To do this an assignment table is provided by the subroutine POSMAP which is described in Section 6.10.

With the assignment table, secondary state assignment can be given to the flow table to form a secondary map. This is described in Section 6.7. However, before describing this the process of optimum combination of rows is dealt with in greater detail in

the following section.

6.6 Optimum Row Combinations

Figure 6.4 gives the program flow chart for determining the optimum combination of rows which is referred to in a flow chart block of Figure 6.3 as 'find merge which gives least number of rows and merge'.

The general idea in this optimum row combination is based upon grouping (9). Starting with one row, call it the initial row, all the rows with which it can be combined are determined by the method given in Section 6.5. If the rows with which it can be combined can themselves be combined they are within a group. But, if one of the combinable rows has a further possible combination with a row with which the initial row cannot be combined this combination is not in the group and is indexed with a cut line. For example, if each row in a primitive flow table is represented by the circled numbers in Figure 6.5, the straight lines represent possible combinations. That is, row 1 can be combined with row 2 or row 3, row 2 can be combined with row 1 or row 3, row 3 can be combined with row 1 or row 2 or row 4, row 4 can be combined with row 3 or row 5 and row 5 can be combined with row 4 (19).

If row 1 is considered as the initial row one of the loops around rows 1, 2 and 3 indicates that this is a possible combination. This loop cuts the

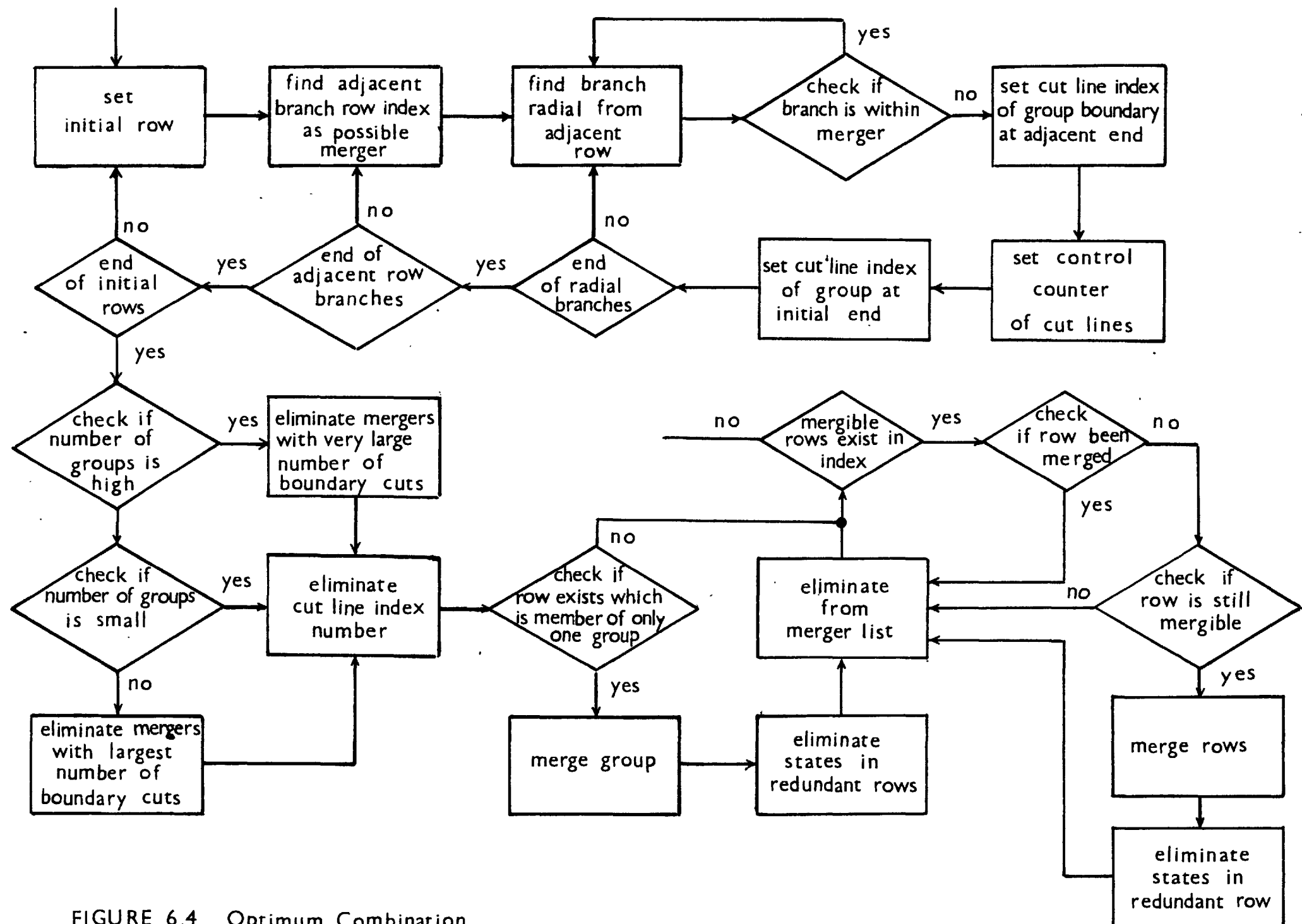


FIGURE 6.4 Optimum Combination

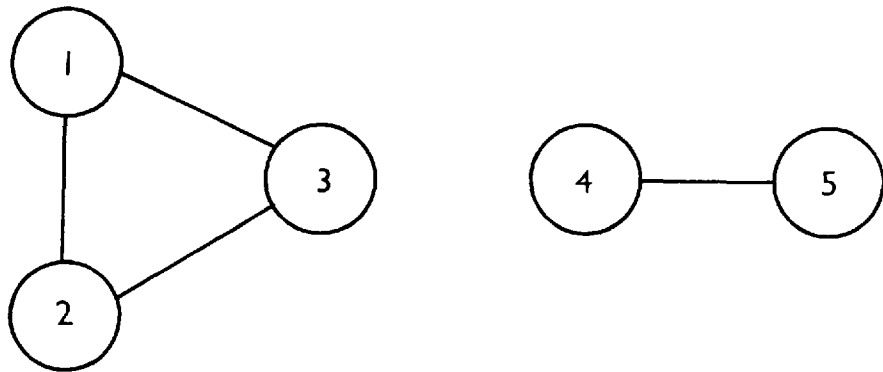
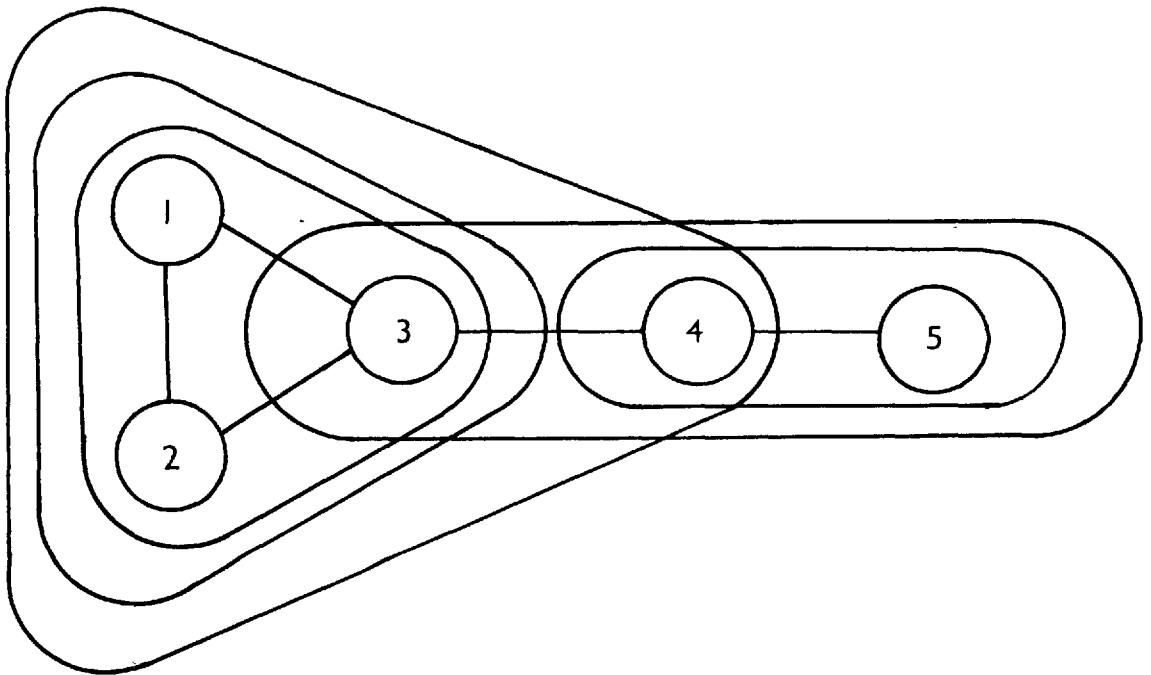


FIGURE 6.5 Cut Lines

straight line between rows 3 and 4. Therefore there will be a cut line recorded for that combination. Considering row 2 as the initial row another loop around rows 1, 2 and 3 results in another cut line between the combination of rows 3 and 4. When row 3 is considered as the initial row the loop will surround rows 1, 2, 3 and 4 resulting in a cut line between rows 4 and 5. If row 4 is the initial row the cut lines will occur between rows 1 and 3 and rows 2 and 3. The cut line for row 5 is between rows 3 and 4.

By counting the number of cut lines the following totals are obtained.

Number of Cut Lines	Straight Line Between Row and Row	
0	1	2
1	1	3
1	2	3
3	3	4
1	4	5

The combination of rows 3 and 4 has the greatest number of cut lines and therefore this combination of rows is eliminated. It can be seen by inspection of this example that if rows 3 and 4 were combined there would be three rows formed in the resulting grouping. But with this combination eliminated the rows can be combined to form only two new rows.

This procedure is followed in the program flow chart shown in Figure 6.4. The initial row is chosen and from it one of the possible combinable rows is selected as an adjacent row. Each row listed as combinable with the adjacent row is examined to determine if it in turn is combinable with the initial row. If not the cut line index number which is assigned to represent the branch from the adjacent row is increased by 1. Since the combination represented by the branch is listed in two storage locations, once for each row, the index is increased in both places. If there are a large number of loops, all combinations with more than 15 cut lines are eliminated. Below this number only one branch line is eliminated at each step and the cut line index is then reset to zero.

When one row has only one possible combination this must be done first and then any rows which form a group can be combined. The redundant rows which were used to form the new row are eliminated from the table and also removed from any list in which they appear. The optimum combination of rows is then complete for one cycle in the procedure described in Section 6.5 which continues until the primary flow table is complete.

When the table for secondary state assignment, which is developed by subroutine POSLAP, is complete state assignment begins.

6.7 Secondary State and Output Assignment

Figure 6.6 gives the program flow chart for the process of assigning secondary states to the cells in the primary flow table to form the secondary and output maps. The theory for this is outlined in Sections 5.5.4 and 5.5.5.

Before the rows were combined each stable state was indexed so that stable states can be found in the primary flow table by scanning for this index. When a stable state is found in the flow table the equivalent cell in the secondary map is examined to determine if the secondary assignment has been made. Where it has not been made the proper assignment is obtained by reference to the assignment table determined by subroutine POSMAP. By scanning the column in the primary flow table in which the stable state occurs associated unstable states are found. If there is no secondary map assignment for the unstable state the secondary state assignment for the row in which the unstable state occurs is compared with the secondary state assignment for the row in which the stable state occurs. If these assignments are logically adjacent (that is, if in a Karnaugh map these two assignments would appear in adjacent cells, see Section 5.3), the unstable state cell in the secondary map is given the assignment of the stable state row. If the assignments are not logically adjacent the unstable state is indexed. When all unstable states have been found a check is made to see if the unstable state assignment is complete. A

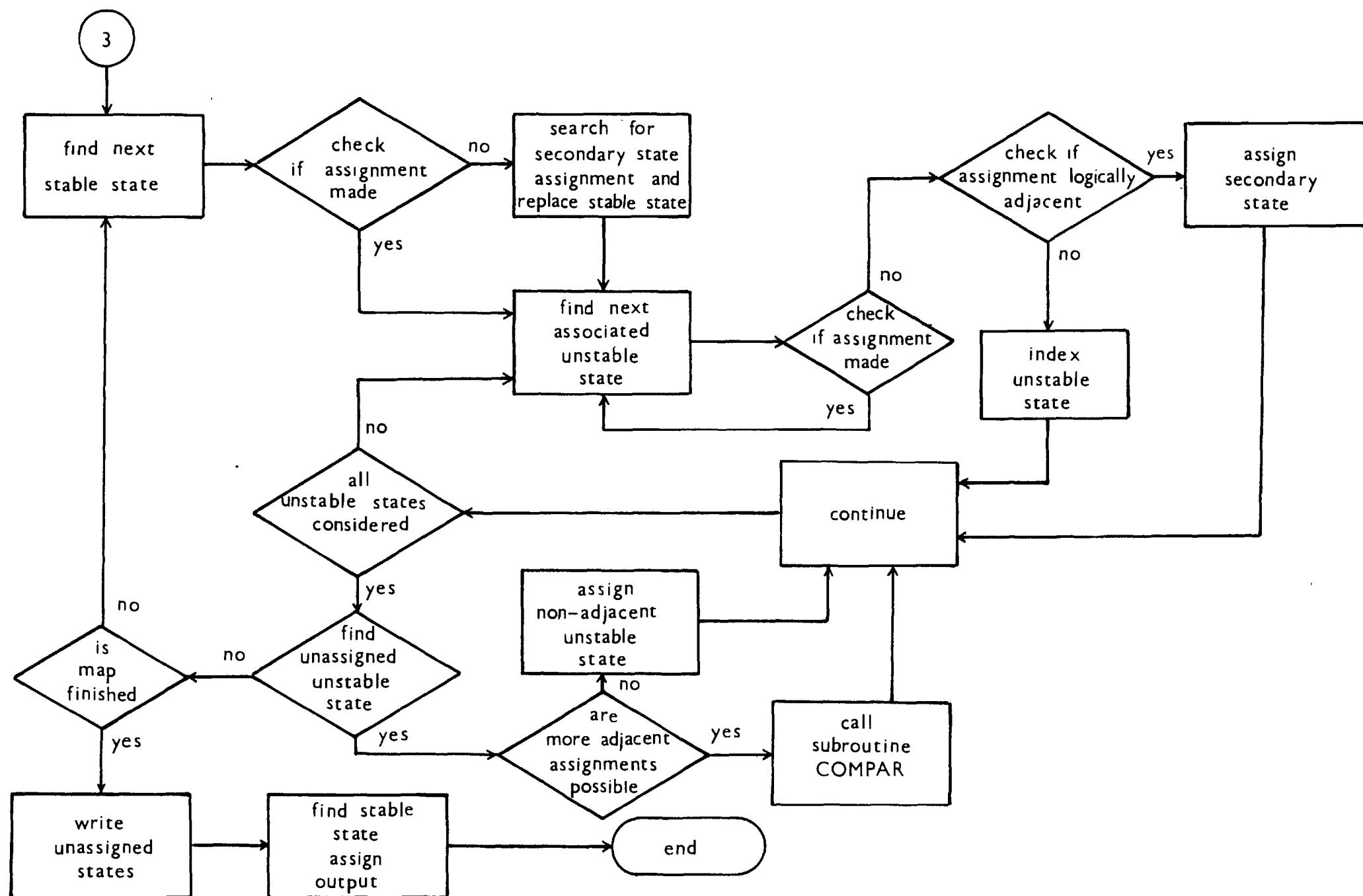


FIGURE 6.6 Secondary State and Output Assignment

subroutine COMPAR, described in Section 6.8, is used to determine the assignment for the unassigned unstable states. When the assignment is complete the output map assignment is made by replacing each stable state in the primary flow table with the output for the stable state which is determined from the primitive flow table. Each unstable state is replaced by zero.

Subroutine COMPAR which is used to assign secondary states to unstable states is described in the following section.

6.8 Subroutine COMPAR

Figure 6.7 gives the program flow chart for the process of comparing secondary assignments to determine the best assignment for unstable states in the secondary map.

Within the selected column each row is scanned in turn to determine its unstable state assignment in the primary flow table and whether it has been given an assignment in the secondary map. All such secondary map assignments are compared with the secondary map row assignments for unassigned unstable states in the primary flow table to determine if the two secondary map row assignments represent adjacent cells in a Karnaugh map. If they do the unassigned unstable state is given the assigned unstable state secondary state row assignment.

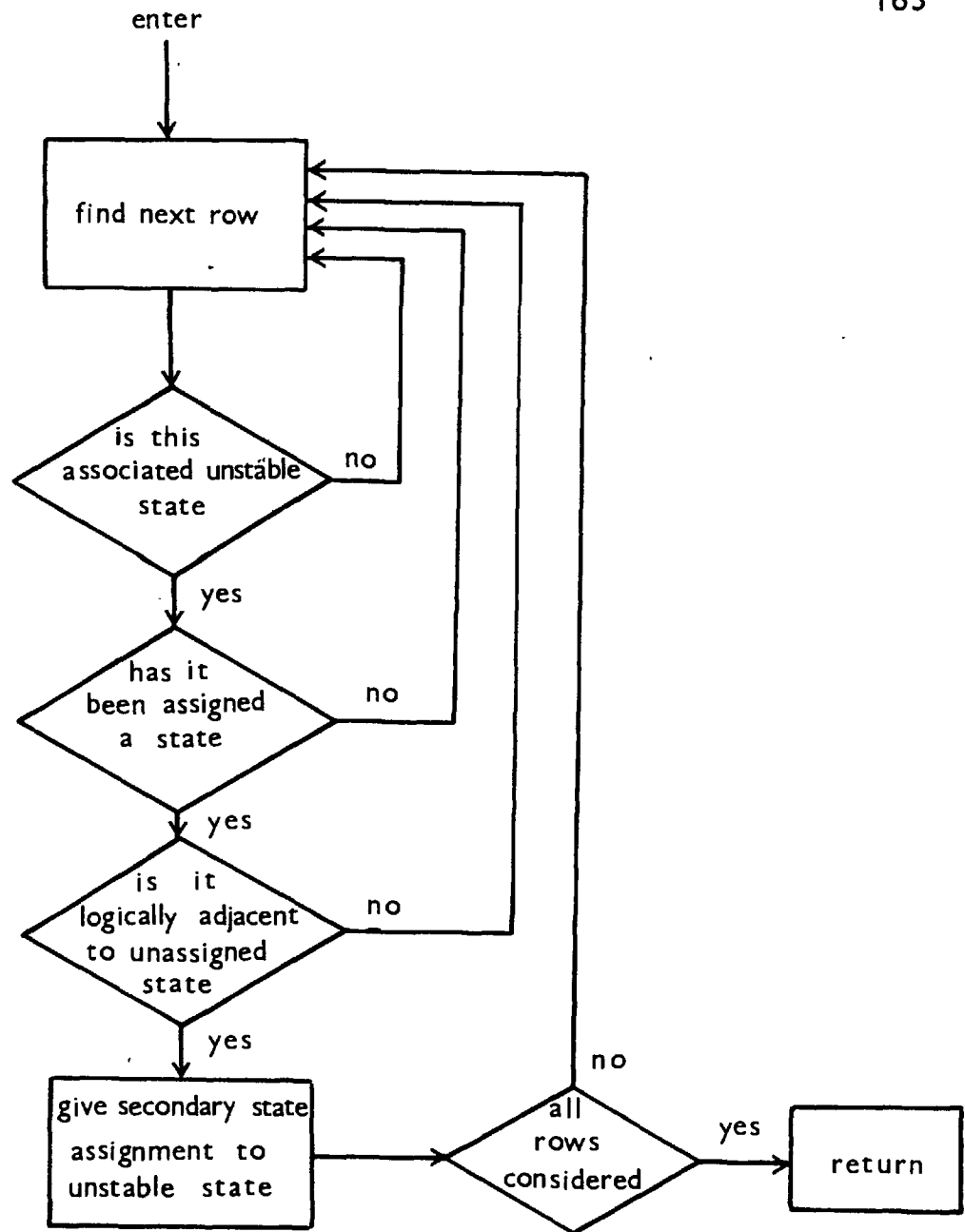


FIGURE 6.7 Subroutine COMPAR

When a flow table or map is printed, an A field is used to avoid printing meaningless O's which might lead to confusion. This is accomplished in the following way.

6.9 Map Printout

All calculations involved in the determination of the above maps are done in an integer field. That is, only integers and positive and negative signs are used. Since there are no blanks in this field, blanks in the flow table or map are represented as zeroes. In the development of this method a zero and a blank are quite different. Therefore a method of writing blanks when blanks are meant is described here.

Figure 6.8 gives the program flow chart for writing a single row of a flow table or map. Since writing subroutines vary slightly with the information required in different tables or maps three separate subroutines, called PRIFLO, SECMAP and KARNAU, are available. However the basic flow chart described is used in all three subroutines.

The general idea of this flow chart is to change from a writing code which permits only numerics to a new writing code which permits all required characters. In the Imperial College IBM 7090 digital computer a word for an integer field or an alpha-numeric field consists of 36 bits. Therefore an integer constant

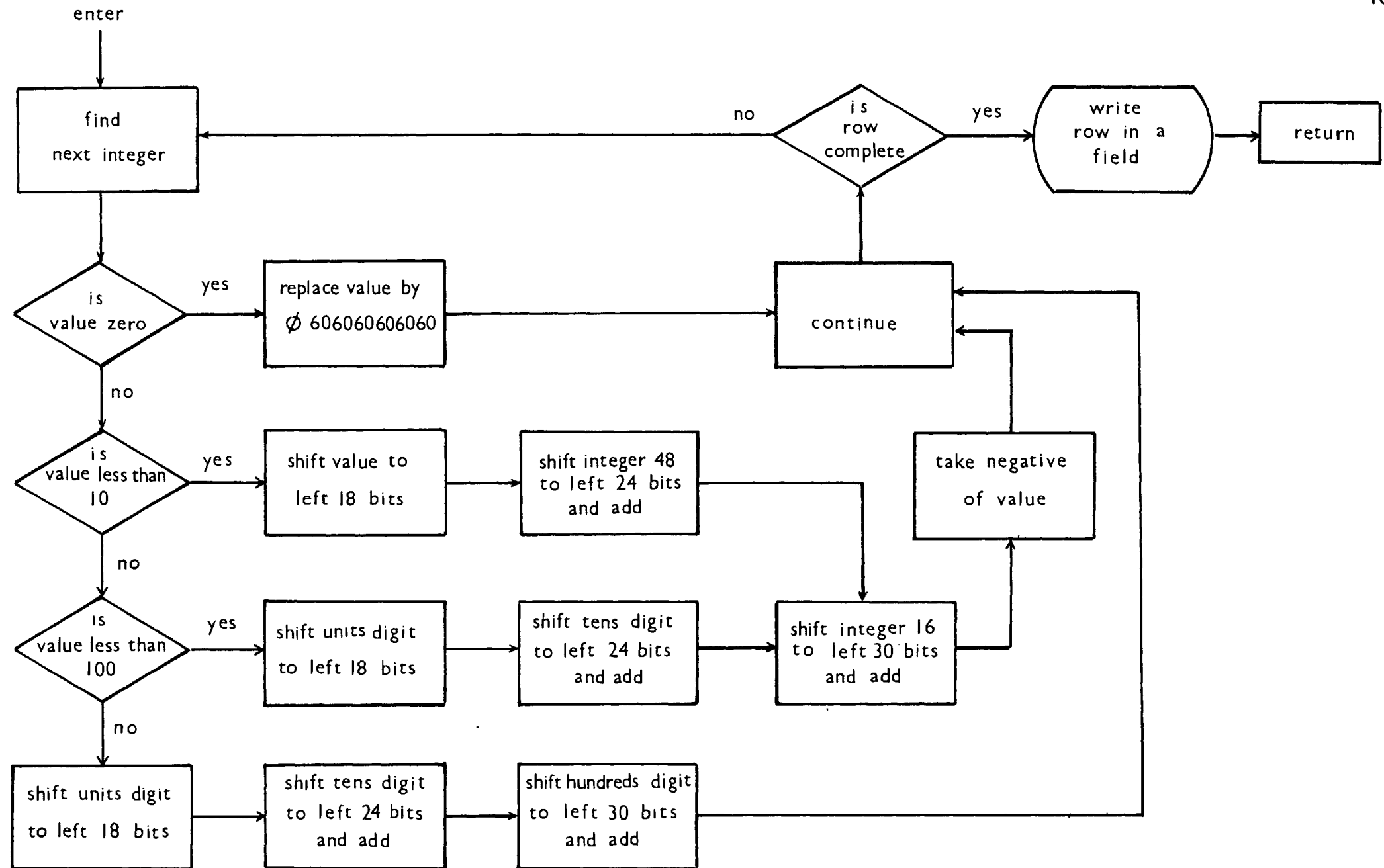


FIGURE 6 8 Program Flow Chart for Writing Subroutines PRIFLO, SECMAF and KARNAU

can consist of up to 11 decimal digits and be as large as $2^{35} - 1$ (28). This means that blanks cannot be written in this field. The bits in an integer field are 'filled' starting with the least significant digits and beginning at the right-hand end of the word.

In an A (alpha-numeric) field a source program exists which is capable of interpreting different binary decimal codes as numbers, letters, arithmetic and punctuation characters as well as blanks. To do this each word is divided into six characters of six bits each. (The integer field is divided into 11 decimal digits.) The word starts at the left and proceeds to the right. To transfer a number into the A field its code must be changed and the position of numbers must be moved from the right-hand end of the storage word to the left-hand end taking into account the difference in the number of bits occupied by a number. Blanks in the output must be represented by the code for a blank which in octal form is the six character word

60 60 60 60 60 60

In the flow table each integer is dealt with separately. First it is examined to see if its value is zero. If it is, the storage location in a new array equivalent to its location in the row is replaced by octal 606060606060. (Numbers which are true binary zeroes are represented in integer form by 2^n where n is the number of logic variables. Modulo 2 of this number repeated n times results in a string of n binary

zeroes.) If the number is not zero, and if it lies between zero and 10, the number is multiplied by 2^{18} which positions it three characters to the left. Each character to the left of this must be replaced by octal 60 to produce a blank character for this location. In integer form 48 represents octal 60, therefore 48×2^{24} will place a code for a blank in this location. Since the character at the extreme left of a word has a bit for a positive or negative sign, 48×2^{30} will place a 1 in this bit which will be interpreted by the print source program as a negative sign. Therefore the character at the extreme left is formed by octal 20 (integer 16) and then the negative is taken to produce the octal 60 or blank character in the location.

Integers from 10 to 99 inclusive must be considered in two stages. For example, the integer 48 cannot just be shifted since the resulting octal 60 would be interpreted as a blank character in the A field. For this integer, first the 8 must be multiplied by 2^{18} and then the 4 must be multiplied by 2^{24} to produce octal 10 and octal 04 respectively. The first character in the word is formed in the manner given above.

To form the code for a number greater than 99 the shift numbers are 2^{18} , 2^{24} and 2^{30} . No difficulty is incurred with the negative sign since the largest octal number which can occur is 11 which avoids the troublesome bit.

The secondary state assignment table subroutine referred to in Section 6.5 is described in the following section.

6.10 Subroutine POSMAP

Figure 6.9 gives the program flow chart for the subroutine POSMAP which describes the formation of the table used to assign states in the primary flow table. The theory for this secondary state assignment table is given in Section 5.5.3.

This table is set up in the computer as an array. The argument of the array is used as the secondary assignment and the value of the array gives the row with that assignment. The dimension of the array is determined by increasing the number of secondary variables used for assignment until the number of elements is equal to or greater than the number of rows in the primary flow table. The first row in the table is assigned the last array position. This is the decimal equivalent of row 1 in a binary progression (see Section 5.2.2). This assignment permits entry into the loop in the flow chart. Once a row with state assignment is chosen it is used as a reference throughout the loop. The row is checked to see if the number of stable states is larger than the mean number of stable state assignments per row. If it is and the dimension of the assignment array is greater than the number of rows and the array is not filled, the row can

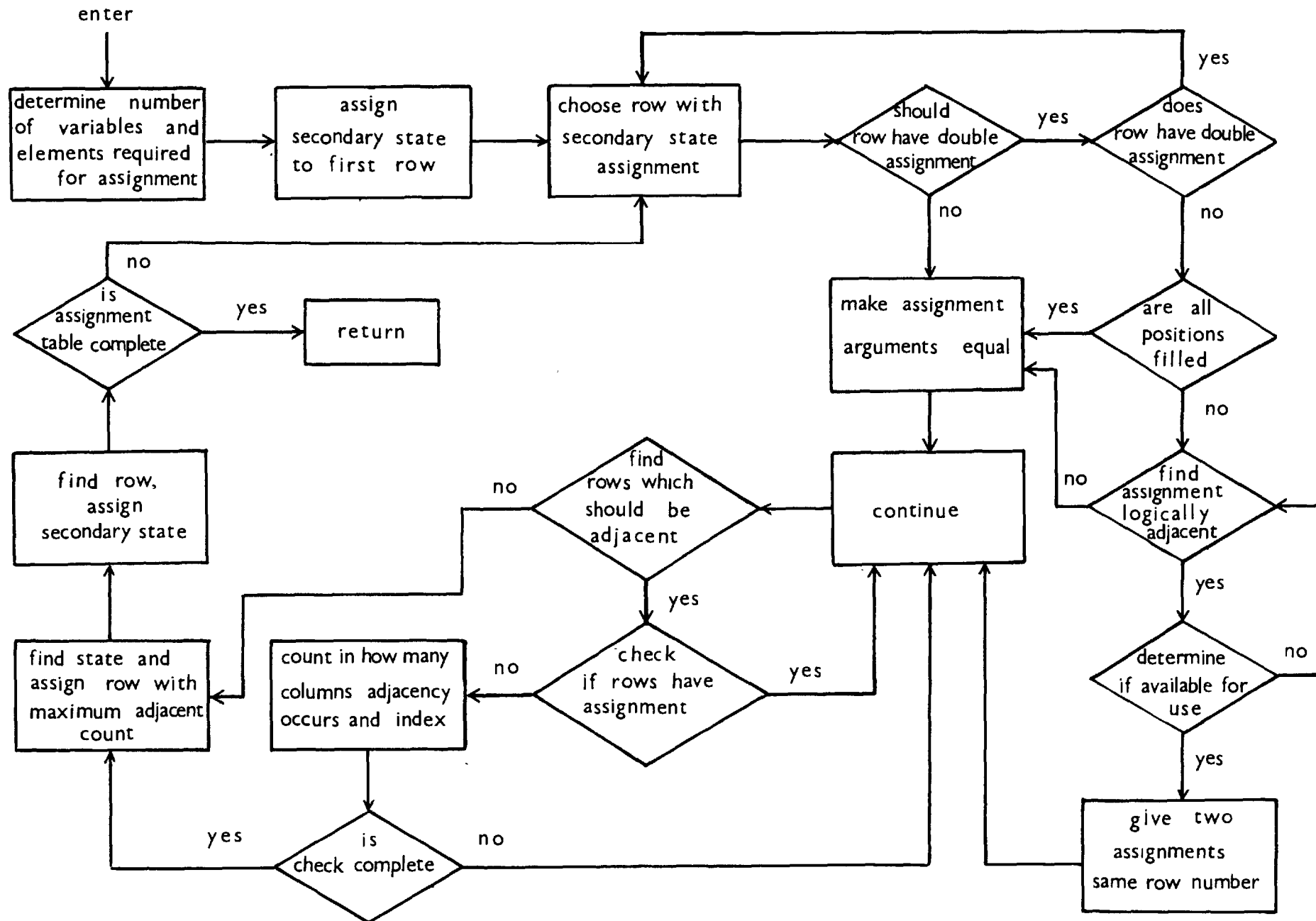


FIGURE 6.9 Subroutine POSMAP

be given a double assignment. However if an assignment which is equivalent to an adjacent cell in a Karnaugh map (see Section 5.3) is not available there is no advantage in this double assignment. Double assignments are made by giving two elements in the array the same row number. The arguments of these two elements are retained for subsequent use. Therefore if a double assignment is not made both constants used in the notation are given the same value.

After checking if the double assignment is made to the reference row, all unassigned rows which have unstable states equivalent to the stable states in the reference row are scanned. A count is kept and the row in which this equivalence occurs most often is given an adjacent assignment. With another row given assignment it can be established as a reference row and the loop continues until the procedure is complete.

To illustrate this procedure the formation of variable equations required for programming a substation switching controller is given below.

6.11 Substation Primary Flow Table

The example chosen here is for six feeders L24, L44, L25, L26, L46 and L45 and the restraints on the system prohibit closing the following switches in parallel.

L24 and L26

L44 and L46

Figure 6.10 gives the substation primary flow table.

The input states of this table are given in the first row below the listed order of switches which is required to interpret the decimal integer (see Section 5.2). Since the switches L24 and L26 cannot be closed together the integer 9 does not appear as an input state as can be seen by the following representation.

Binary Number						Integer
L24	L44	L25	L26	L46	L45	
1	0	0	1	0	0	[9]

Figure 6.10 gives the primary flow table for substation switching as developed by the off-line computer program. This table is the combined form of the primitive flow table which is not given here. In row 1 of Figure 6.9 stable states occur in columns 5, 12, 17, 22 and 34. In row 46 stable states occur in columns 1, 2 and 22. These stable states can be found in this map by a comparison with Figure 6.12, the secondary map. In this figure the first column which is headed 'Y' gives the row assignment in decimal integer form. Row 1 is assigned the decimal integer 64 and therefore the stable states in row 1 of Figure 6.12 have the number 64 as their state assignment. These

are in columns 5, 12, 17, 22 and 34 as given above. The same procedure can be used to find the stable states in any row. In row 46 the row assignment is decimal integer 41. The stable states (that is, columns in which the number 41 is used as a state assignment) occur in columns 1, 2 and 22 as given above.

Since there are 46 rows in the primary flow table, six variables are required to make the state assignment. Sixty-four is the maximum number of assignments possible with six variables. Figure 6.11 gives the expanded primary flow table which includes the column 'Y'. The Y column gives the way in which the 64 assignments are to be applied to the primary flow table. Row 1 is given assignment 64, row 2 is given assignment 12 and so on for the 46 rows with stable states. The 47th row is a duplication of the states in row 1 except that no stable state appears in this row (see Section 5.5.3). Also the 48th row is a duplication of the states in row 5 except that no stable state appears in row 48. In this way the table has been expanded to 64 rows.

A comparison of Figure 6.11, the expanded primary flow table, Figure 6.12, the secondary map, and the output map shown in Figure 6.13 can be used to explain the sequence of changes through the map. For example, in column 1 of Figure 6.11 stable states exist in rows 5, 7, 9, 10, 15 and 46. An input request to close switch L24 results in a change in input from column 1 to column 2 and an output to close switch L24.

The output map shows that in column 2 a signal '1' is given to close switch L24 in row 46. The secondary map shows that this location represents a stable state. That is, the row assignment 41 is equivalent to the state assignment in this location. Therefore the variables in the secondary map must change to this state.

If the initial stable state in column 1 of Figure 6.12 is state 3 the map location is row 5. The input signal causes a horizontal change in the map from stable state 3 to state 11. The secondary assignment for state 3 is as follows.

Binary Number						Integer
y1	y2	y3	y4	y5	y6	
1	1	0	0	0	0	$[3]$

A change to state 11 results in the following variable values

1	1	0	1	0	0	$[11]$
---	---	---	---	---	---	----------

which represents a change of state from 0 to 1 for variable y4.

Since the variable then changes to state 11 there is a vertical movement in column 2 of the secondary map from row 5 with assignment 3 to row 52 with assignment 11. In row 52, column 2, the next state given is 9. The change is as follows.

Binary Number						Integer
y1	y2	y3	y4	y5	y6	
1	1	0	1	0	0	[11]

to

1	0	0	1	0	0	[9]
---	---	---	---	---	---	-----

This is a change of state for variable y2. With the variables in state 9 a vertical change in column 2 to state 9 in row 10 results, which in turn changes the variables to state 41 as follows.

Binary Number						Integer
y1	y2	y3	y4	y5	y6	
1	0	0	1	0	0	[9]

to

1	0	0	1	0	1	[41]
---	---	---	---	---	---	------

This is a change of state for variable y6.

The vertical movement in column 2 to state 41 row 46 results in a state in which the present state 41 and the next state 41 are equal thus no further change occurs and the variables settle in a stable state. The output map of Figure 6.13 shows that at this state an output of 1 occurs. The binary representation of 1 is as follows.

Binary Number						Integer
L24	L44	L25	L26	L46	L45	
1	0	0	0	0	0	[1]

This output closes switch L24. In Figure 6.13 the output to a tripping coil is given a hundred series number to distinguish it in the table from a closing signal.

The example above is one of the more complex switching sequences. An example of a more direct sequence is shown by considering the change from stable state 9 to stable state 41. Stable state 9 occurs in row 10 column 1. With the same input as above the horizontal change in the secondary map is to column 2. This initiates a change in the secondary variables which is as follows.

Binary Number						Integer
y1	y2	y3	y4	y5	y6	
1	0	0	1	0	0	[9]
to						
1	0	0	1	0	1	[41]

The secondary map given in Figure 6.12 is in reality six maps combined into one. That is, it is composed of the binary states of six variables. The map for any single variable in binary form is determined by testing the integer form of representation for the

presence of the appropriate power of 2 in the binary progression (see Section 5.3).

The secondary map for variable y_1 is given in Figure 6.14 as an example of the representation of the Karnaugh map form of Section 5.3 from which the Boolean expressions can be seen more easily. This form representing the control for switch L24 is given in Figure 6.15. Signals to the tripping circuit of this switch are preceded by a 1 to distinguish them from closing circuit signals.

SUBSTATION MAP

FLOW TABLE

INPUT STATES

L24 L44 L25 L26 L46 L45

C	1	3	2	6	7	5	4	12	14	10	8	24	28	22	21	17	16	48	49	53	52	60	56	40	42	46	44	36	37	39	38	34	35	33	32
25	50108	59014	57				58	24	60	23005	26		148	49010	48145	51144	157146						27					147	137	61105066106					
31	45	64130	44009	43					63015	62	30		29	46	28006	32								65129			127	47126163128							
	1056	P	59018	57	9	58			60134						10	55								131065132			54	61133	53311	52					
13	40212	39	14	41117	79				15	95		78021	76		77		116	81					94027	91		92113081114		16	42115	93					
013	2	12303	14						164	15	5					6										162139161			163	16					
19	45		70	18	44017243	20					152		21	46		150								149165151	69		22	47	68016	66					
019	2		3	18156	17004	20			134	5					21		6								131162132			22154	126153133	155					
	1040	8		130		9	75024	71		72			74				10102332	96		97				98			129	75127	126061128			11	99		
025	2		3130	111	4						5		168109049110				6		121666149165							129167127	126082128								
031	2		2130								5		160				6		158112157							129	127159126068128								
38	56103	64111	357102	79					63023	62			78109	76		77	37	55	80					36	65		35	54124	34	53033052					
25	50108						86	24		23062	26			49121	48		51	85					27			84035	81107	82105042106	83						
31	103		101041102								95	30		29160	28088	32158119157							94036	91	92	159104									
25	103		101044102				24164	23089	26								100037	96		97				98	27162125161				104163						
038	2										5						6																		
	1045	8	70			9	79143						78029	76	10	77							80142		140	69139161141		68034	66	11	67				
31	56		124	117		122360123			30		29		28077	32	55116									125		113054114			53115	52					
19			18	17058	20				134	89030	87	21		121	88118158119									90131091132		22		133	120						
13		12059	14		80				15	89026	87			121	88118051119	85								90		84022	81	82	16	120	83				
13		1270	14		86137				15	135074136				121	118055119	85138										84127	81	82	16	120	83				
19		70	18		17073	20				152		21				150								149090151	69		22		68133	66					
19			16156	17079	20		134					21		121100118096119	97								98131069132		22154	107153133155120	99								
38			124156111		122071123						95		168109160110			37		12166142165	36				125167		35154114153	34155	33063								
		108										148				145		144085146	94131	91					92147		107	105053106	93						
14	56		18		17086	20			152		21			150	55								149094151		22	54			53120	52					
38	40108	39		41		137				135078136					37									138		36		35		34	42	33093			
25	40103	39		41117		24			23095	26168									116166146165	27						167113047114				42115					
38	45		44102	43137						135168136	46				37									138		36		35	47		34	33099			
31	56		59101	57		58143	60			30	29		28100	32	55								142	140		139167111	54		61	53106	52				
			70			79143						78148	76		77								80142	140		69139084141		68105	66						
25	50					24			23072	26168			49110	48		51			166138165	27						167									
45						44111	43		164				148	46		145			144080146							162129161147	47		163						
			103	64101156102	86137	63123			62135087136										85138					65		84113	81104	82							
38	40008	36		41		73020	71		72		74		160						37158116157					36		75	35159		34	42	33007				
45		64		44117	43143	63134	62					46		100150	96				97142	98140					65139092141	47									
38					73122	71			72		74					37								36		75	35		34	33067					
			59124	57111	58143	60								109076110100145	96112	97142	98140								139075141			61							
31	50		70		117						30		29	49028048	32	51116								69		113159114	68128	66115	67						
						79	164				152	78136	76		77150				80149098151162132161									163							
						73137	71		72		74		160						158144157							75	159107	105155106							
						59130	57117	58		95									116						94140	91		92113154114	61		115	93			
						124				86122164123	89135	87				88			85						90		125	84141	81		82				
						130				73143	71		72		74												129	75127	126153128						
13		12064	14		111	86				15	89152	87109046113	88						112	85				90		84147	81		82	16					
1050	8		124156	9		4						148	10		145				144097146	94151	91125				92147154104153		155	11	93						
001022	8	3									5		148	10		6145			144166146								147								

FIGURE 6.10 Substation Primary Flow Table

SUBSTATION MAP

SECONDARY MAP

INPUT STATES

L24 L44 L75 L76 L46 L45

Y	C	1	3	2	6	7	5	4	12	14	13	8	24	28	20	21	17	16	48	49	53	52	60	56	40	42	46	44	36	37	39	38	34	35	33	32
64	25	50108	59014	57	58	24	60	23005	26	148	49010	48145	51144	157146	27	65129	127	47126163128	54	61133	53011	52														
12	31	45	64130	44009	43	63015	62	30	29	46	28006	32	55																							
17	1056	8	57018	57	9	58	60134																													
6	13	40	12039	14	41117	79	15	95	78021	76	77	55	116	80	94027	91	9211301114	16	42115	93																
3013	2	12031	14	4	164	15	5																													
27	19	45	71	12	44017043	20	152	21	46	150																										
10019	2	3	12156	17004	20	134	5																													
19	1240	8	130	9	73024	71	72	74	1010032	96	97	98	131162132	22154126153133155	7																					
24025	2	3130	111	4	5	168109049110	6	112166149165	129167127	126082128	7																									
9031	2	3130	4	5	160	6	158112157	129	127159126068128	35	54104	34	53034052																							
20	38	56103	64101057102	79	63023	62	78109	76	77	37	55	80	36	65	27	84035	81107	82105042156	83																	
15	25	50108	64101057102	79	63023	62	78109	76	77	37	55	80	36	65	27	84035	81107	82105042156	83																	
58	31	133	101041102	86	24	23062	26	95	30	29160	28088	32158119157	94036	91	92	159104																				
29	25	103	101041102	24164	23089	26	5																													
33038	2	5	4																																	
5	1045	8	70	9	79143																															
60	31	56	124	117	122060123	30	29	28077	32	55116																										
30	19		18	17058	20	134	89030	87	21	121	88118158119	90131091132	22	113054114	133	120																				
45	13	12059	14	86	15	89026	87	121	88118051119	85	90	84022	81	82	16	120	83																			
57	13	12072	14	86137	15	135074136	121	118055119	85138																											
46	19	70	18	17073	20	152	21	150	149090151	69	22	68133	66	67																						
53	19		18156	17079	20	134	21	121100118096119	97	98131069132	22154107153133155120	99																								
63	38	124156111	122071123	95	148	145	144085146	94131	91	92147	107	105053106	93																							
51	19	56	18	17086	20	152	21	150	149090151	69	22	54	53120	52																						
23	38	40108	39	41	137	135078136	37	138	136	35	34	42	33093																							
50	25	40103	39	41117	24	23095	26168	116166146165	27	167113047114	42115																									
59	38	45	44102	43137		135168136	46	57	138	36	35	47	34	33099																						
54	31	56	59101	57	58143	60	30	29	28130	32	55	142	140	139167141	54	61	53106	52																		
49		70	79143	24	23072	26168	49110	48	51	166138165	27	167																								
26	35	50		44111	43	164	148	46	145	144080146	162129161147	47	163																							
39	45		103	64101156102	86137	63123	62135087136	85138	65	84113	81104	82	83																							
16			43	38	40108	39	41	73020	71	72	74	160	37158116157	36	75	35159	34	42	33007																	
48	46	64	44117	43143	63134	62	46	120150	96	97142	98140	65139092141	47	99																						
32	38			73122	71	72	74	37	36	75	35	34	33067																							
40		59124	57111	58143	60	30	29	109076110100145	96112	97142	98140	139075141	61	99																						
36	31	50	70	117		30	29	490280548	32	51116	69	113159114	68128	66115	67																					
38				79	164	152	78136	76	77150	80149098151162132161	163																									
37		126		73137	71	72	74	160	158144157	75	159107	105155106																								
52		59130	57117	58	60	95			116	85	94140	91	92113154114	61	115	93																				
42		124		86122164123	89135	87	88		90	125	84141	81	82																							
56		130		73143	71	72	74																													
35	13	12064	14	111	86	15	89152	87109046110	98	112	85	90	84147	81	82	16																				
34	1050	8	124156	9	122063123	95	148	10	145	144097146	94151	91125	92147154104153	155	11	93																				
41	01002	8	3	9	4	5	148	10	6145	144166146	147																									
1	25	50108	5914	57	58	24	60	23	5	26	148	49	10	48145	51144157146	27	162139161	163	16																	
2	13	2	12	14	4	164	15	5																												
4	1	45	8	70	9	79143																														
7	13	40	12	39	14	41117	79	15	95	78	29	76	10	77	80142	140	69139161141	68	34	66	11	67														
8	31	2	3130	4	5																															
11	19	2	3	10156	17	4	20	134	5	21	6																									
13	31	45	64130	44	9	43	63	15	62	30	29	46	28	6	32	51	85	27	84	35	81107	82105	42106	83												
14	25	50108	64101	57102	79	63	23	62	78109	76	77	37	55	80	36	65	35	54104	34	53	33	52														
21	38	56103	64101	57102	79	63	23	62	78109	76	77	37	55	80	36	65	35	54104	34	53	33	52														
22	38	40108	57	41	137	185	78136	37	138	36	35	47	34	33099																						
25	25	2	3130	111	4	5	168109	49110	6	112166149165	129167127	126082128	7																							
18	25	50		24	23	72	26168	49110	48	51	166138165	27	167																							
31	19	45	70	10	44	17	43	2																												

SUBSTATION MAP

OUTPUT (Z) MAP

INPUT STATES

L24 L44 L25 L26 L46 L45

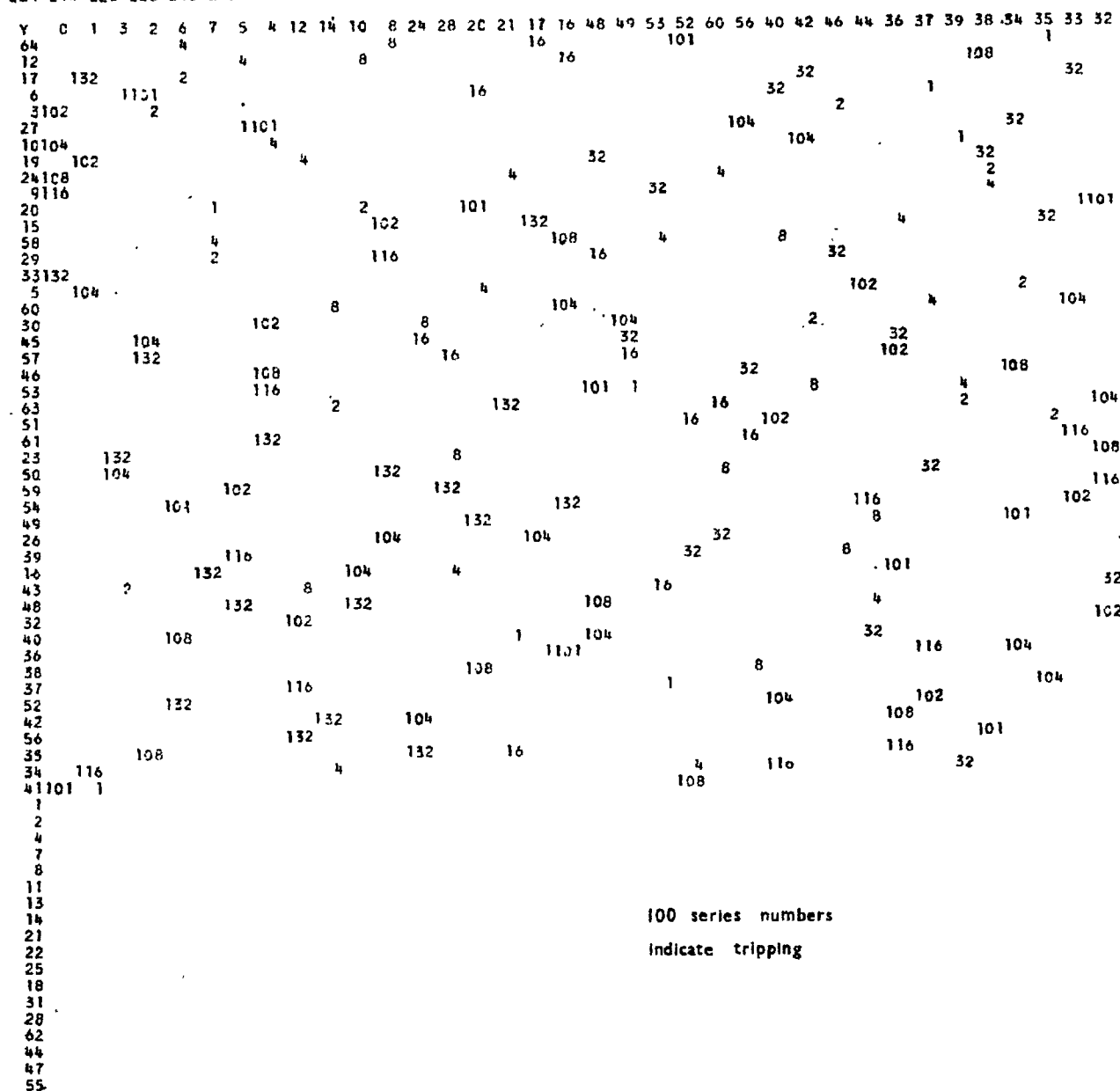


FIGURE 6.13 Substation Output Map

CHAPTER 7

A METHOD OF DEVELOPING LOGIC EQUATIONS FOR USE ON THE NETWORK SIMULATOR

7.1 General

In Section 1.4.2 it is suggested that the network simulator described in Chapter 3 can be used to test methods of busbar protection based on Casson - Last and the power flow principle. The method of developing equations which may be used for such systems is given in this chapter.

In the Casson - Last system described in Section 1.1.4 the equations are given in Boolean algebra form. However this system relies strictly on current direction flow, and although Equation (1.10) indicates correct operation for the three phase busbar fault given in Figure 4.4, difficulty is encountered in practical application particularly for sectioned busbars. This condition arises when a check feature (see Section 1.2.2) is provided. A busbar fault is detected when the positive protection bus (x) and the negative protection bus (y) in this system are energised alternately. This is shown in Equation (1.10). The following equation is a Boolean expression for the check loop protection buses for a sectioned busbar with a three phase fault on only one section.

$$f = (x \cdot y) \vee (\bar{x} \cdot \bar{y}) \quad (7.1)$$

This equation is developed by taking the waveforms of Figure 4.3 to represent the unfaulted section and the waveforms of Figure 4.4 to represent the section on which the fault occurs. Condition $(x \cdot y)$ represents both buses energised and condition $(\bar{x} \cdot \bar{y})$ represents both buses de-energised. Therefore Equation (7.1) shows that the protection buses are energised or de-energised together. This condition is identical to that for a healthy busbar or to that for an external fault as shown in Figure 1.5. Therefore the fault which is on only one section is not detected. No practical method which overcomes this difficulty has been developed. However the Casson-Last system represents an attempt to provide faster busbar protection by using instantaneous current relationships to overcome some of the difficulties in the circulating current scheme.

Figure 4.5 shows that during a busbar fault all the CTs of a circulating current scheme on the busbar push current through the relay operating coil. The accuracy of the circulating current scheme is affected by the magnetising currents of the CTs and the varying impedance of the system with different fault levels. For an external fault the CT secondary associated with the feeder (Feeder No. 10) supplying the fault will be of opposite polarity as shown in Figure 4.6. In effect this CT provides a shunt path for the relay and the voltage across the relay is reduced.

A comparison of Figures 4.2, 4.5 and 4.7 shows that current transformation with an independent non-varying burden gives a more accurate representation of the primary network currents. If this signal is coded, the accuracy can be retained and signal interference can be avoided. With a more accurate measurement a reduction in the time required to detect current unbalance can be made which should result in faster operation than the circulating current scheme.

For the reasons given above it is suggested that the linear binary digit coding system for detection of busbar faults proposed by Cory (17) be used. Because protection schemes using electronic circuitry generally are fast enough to be applied to instantaneous values and mechanical relays usually operate on phasor quantities electronic circuitry can have much shorter operating times.

A scheme which provides busbar protection by a centralised controller must have a number of peripheral units to monitor substation busbar feeder currents. These units would convert an analogue signal into digital form which is then fed to the arithmetic unit of a computer. The output signal from this unit has only two possible values which form a decision either to trip or not to trip. The method of protection outlined here investigates the possibility of eliminating the analogue to digital conversion equipment by utilising simple logic. Signals which are produced when specified threshold values are reached provide the input to the

protection system.

Since logic schemes are beginning to be used for protection in power networks (40), a method of examining logic techniques is useful. Although the particular example below is not immediately practical for protection of sectioned buses it illustrates the method.

7.2 Restraint Conditions

A simple scheme using logic circuitry components which compares the phases of the current at any one instant can be written using a function switch together with logic gates. Two inputs to a function switch consist of a setting value and a variable which in this case is instantaneous current. The output which has only two possible values depends upon a comparison of the magnitudes of the inputs. If the magnitude of the instantaneous current is less than or equal to the setting value the output has one value. The output has the other value when the magnitude of the instantaneous current is greater than the setting value. This switch acts as a logical equivalent of a square wave generator with a choice of setting values. It can be used to produce an output signal which gives the polarity of a current if the setting value is zero. If the function switches connected to phase 'a' of all feeders on a busbar are combined through an 'and' gate a signal will be produced when the instantaneous currents in phase 'a'

have positive polarity. Similarly, a signal can be produced from an 'and' gate when phase 'a' of all feeders have negative polarity. If the signals from these two 'and' gates are applied to an 'or' gate, an output is produced when the polarities of phase 'a' in all feeders are the same. This method produces a protection scheme using logic circuitry which is operationally equivalent to the Casson-Last system. Since this scheme has limitations (see Section 7.1) a system which provides restraint against false operation is developed here.

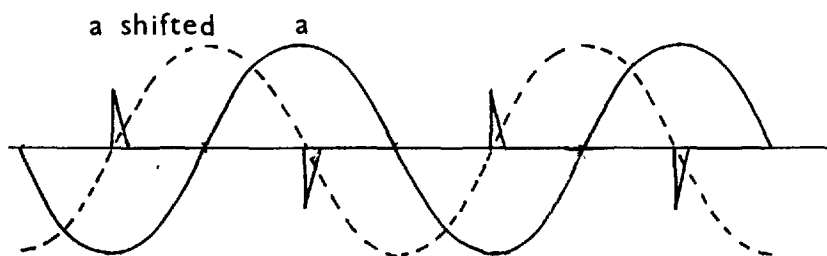
One method of busbar protection is described by Steel(64). This method uses a directional relay in each feeder of the busbar. The contacts on the relays are arranged to close when the voltage and current relationship indicates a fault flow into the busbar. When the contacts on all relays close together a busbar fault is indicated. The vector addition of voltage derived from current and line voltage work to trip the relay. Restraint is obtained from the line voltage. When current and voltage operate in the same direction they become larger than the restraining voltage and the relay operates. When the current flow is in the opposite direction the operating voltage becomes smaller than the restraint voltage holding the relay. This type of protection does not operate on a sectioned busbar. It is very slow and the large number of series contacts from relay to relay greatly increases the possibility of contact failure. Restraint on a directional relay is provided by the voltage signal but under short circuit conditions this relay may lose its

directional discriminating ability. When the ratio of the current to the voltage becomes sufficiently large, the voltage which operates the relay exceeds the restraint and the relay will release. Restraints derived from line voltage are ineffective when short circuits occur and it would seem better to use voltages which increase rather than decrease as restraint signals, if possible.

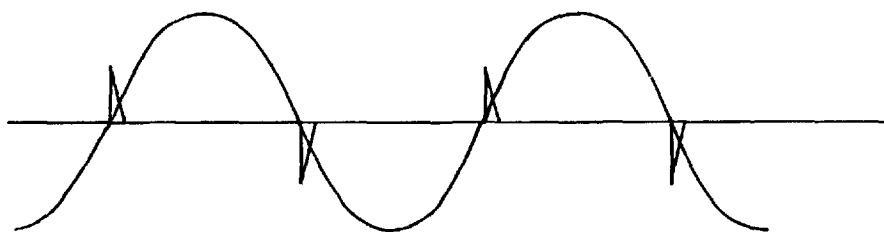
Wideroe (70) developed a number of relays using valves and, in fact, some of these circuits are logic 'and'/'or' gates. In the high speed directional relay which he proposed the current signal was shifted by 90 degrees and rectified. ^{This} The value is used as a tripping restraint (x3) except when it is very small. Under this condition the negative half cycle of current (x2) is added to the rectified voltage signal (x1). The tripping restraint equation for this relay can then be written as

$$\text{RESTRAINT} = x3 V (\overline{x3} \cdot x2 \cdot x1) \quad (7.2)$$

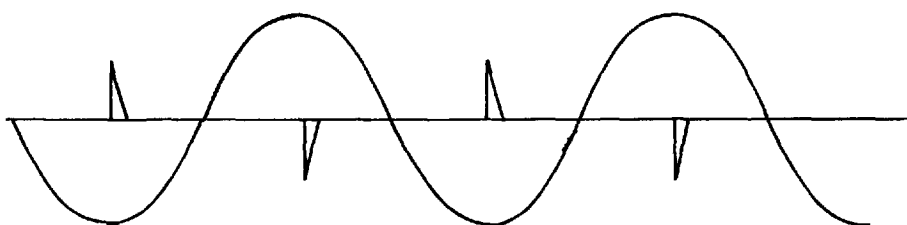
Later Loving (37) proposed a method of blocking and passing pulses based upon the phase sequence relationship of three phase currents. Basically in this method phase 'a' is shifted 90 degrees ahead and pulses are formed when this phase passes through zero (see Figure 7.1). The instantaneous currents in phases 'b' and 'c' are summed such that under normal operating conditions this waveform leads phase 'a' by 90 degrees. When the instantaneous value of this sum is negative a positive pulse from phase 'a' is passed.



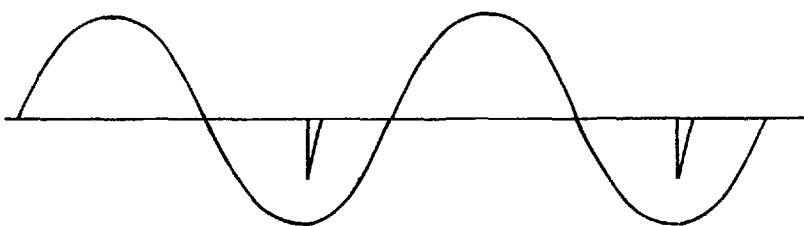
phase 'a' waveforms and pulses



sum of phase 'b' and 'c' currents for unfaulted condition



sum of phase 'b' and 'c' currents for line a-to-b fault



sum of phase 'b' and 'c' currents for line a-to-c fault

FIGURE 7.1 Fault Type Detection

If the instantaneous value is positive a positive pulse from phase 'a' is blocked. On a line-to-line fault involving phases 'a' and 'b' the instantaneous sum of phases 'b' and 'c' have the opposite polarity to the pulses and all positive pulses are passed. However on a line-to-line fault involving phases 'a' and 'c' the instantaneous sum of phases 'b' and 'c' have the same polarity as a phase 'a' pulse and all positive pulses are blocked. When Loving outlined the electronic relay development in 1949 the equipment available was expensive, unreliable, relatively bulky and not readily applicable to relaying application. It had no advantage over existing equipment. However with the development of reliable high speed logic circuitry some of his ideas are now applicable to logic relays (40). The basic principles illustrated by this method could be used to distinguish if a line-to-line fault is between lines a and c or a and b. This is important because, as shown in Chapter 4, the conventions for direction of voltamp flow given in Section 2.2 are maintained except for phase 'c' on a line b-to-line c fault. Since the method above can be used to determine when the convention is not maintained on line-to-line faults, a voltage signal is not required to determine if voltamps are flowing into the busbar. However the method gives no indication of the direction of power flow and also requires a summation of phase currents. It can be modified to use signals obtained from each phase individually to provide tripping restraint and also to provide a 'memory' circuit similar to the Casson-Last protection buses (x and y) shown in Figure 1.3.

Since the derivation of the restraint signal is more involved than the power flow direction signal, the flow diagram, the maps and an output table for the restraint are developed first. In this way the same flow diagram and maps can be used to produce an output table for the power flow direction signal.

The method of determining restraints depends basically on the presence of negative sequence components during a line-to-line fault (1). If α and β components (see Section 3.4) are used rather than symmetrical components, a method better suited to logic can be developed. For example, during a line b-to-line c fault with the reference axis on phase 'a', the maximum instantaneous fault current occurs on the β axis. Two methods of detecting this increase in the β component of current are possible. In one method the time interval between a pulse defining the β axis and a pulse defining the maximum current in line 'b' or 'c' can be used. On a line-to-line fault this time interval tends to zero. In the other method the instantaneous value of current in lines 'b' and 'c' under normal operation can be used to establish the approximate location of the β axis. Large differences in these locations indicate abnormal conditions. Actually, a reference system leading the α and β components by 90 degrees is more convenient since pulsing can be arranged to occur when the instantaneous value is zero. It is this second method which is used here as an illustration.

The pulsing conditions are maintained for other line-to-line faults by shifting the reference axis for each phase. This pulsing arrangement divides each cycle of current into twelve segments. It is the pulsing sequence which detects the presence of negative sequence components. Therefore a method of detecting this pulsing sequence is proposed. By a state assignment procedure similar to that used in Section 5.5.3 the segments in which the restraint condition may exist are indicated.

7.3 Basic Logic Signals

A formal procedure (41) shown in Figure 7.2 similar to that outlined in Chapter 5 is used as a method of developing the logic system for a busbar protection scheme. The pulsed signals provide the input to a logic controller which transforms the signals into an output suitable for busbar protection. Each input signal changes the state of the protection circuit so that the sequence is stepped along. This forms a type of 'memory' circuit.

The form of 'memory' used is a logic variable having two stable states, 0 and 1. The input to this variable is in pulse form. When the variable is pulsed on the set input, S, it changes from state 0 to state 1 or retains state 1 if the initial state is 1. Similarly, when pulsed on the reset input, R, the variable changes from state 1 to state 0 or retains state 0 if the initial

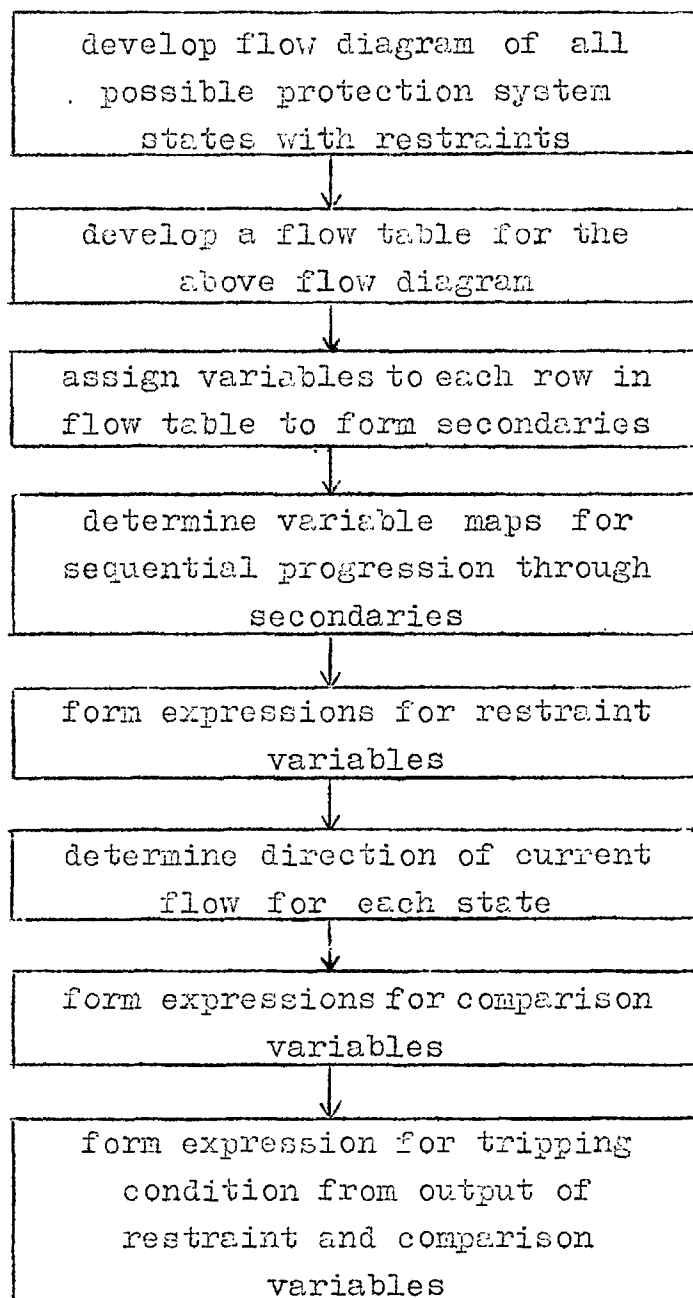


Figure 7.2 Procedure for the Development of the Logic System

state is 0. For convenience S1 and R1 are taken to represent the inputs to variable number 1, $\overline{y1}$ and y1 represent the two output states of variable number 1, 0 and 1 respectively. Similarly, S2, R2, $\overline{y2}$ and y2 refer to the inputs and outputs of variable number 2. For an input pulse from x this type of 'memory' has a set input S1 which is excited according to the following Boolean equation.

$$S1 = x \cdot \overline{y2} \quad (7.3)$$

That is, variable number 1 will be set on a pulse from x if variable number 2 has an output of $\overline{y2}$. Variables denoted by VS are secondaries which are used for state assignment. Variables denoted by VR are used to provide the tripping restraint conditions. Variables denoted by VC are used to give current flow direction and are called comparison variables.

The logic is developed from the figures of Chapter 4 to form a stable state flow diagram.

7.4 Protection Flow Diagrams

The principle of the protection method is that from all phases of a feeder pulses are obtained which determine the restraint and current flow directions in each phase. Although the state assignments of the secondaries are always the same the restraints and direction signals change for each phase.

The pulses required from each phase are as follows:

From phase 'a',

- x_1 when the instantaneous current becomes greater than 0.
- $\overline{x_1}$ when the instantaneous current becomes less than 0.
- x_a when the instantaneous current becomes greater than its normal value along the β axis with phase 'c' as reference.
- $\overline{x_a}$ when the instantaneous current becomes less than its normal value along the $-\beta$ axis with phase 'c' as reference.

In Figure 7.3 these pulses are shown for phase 'a' during normal operating conditions. For phase 'b' the corresponding pulses are denoted by x_2 , $\overline{x_2}$, x_b , $\overline{x_b}$ and for phase 'c' by x_3 , $\overline{x_3}$, x_c , $\overline{x_c}$.

A flow diagram consisting of all stable states is constructed. This flow diagram is shown in Figure 7.4. Large circled numbers represent stable states and small circled numbers represent restraint output. For an output of 0 tripping is permitted and for an output of 1 tripping is not permitted provided that the comparison circuit output given in Section 7.7 indicates that tripping is required.

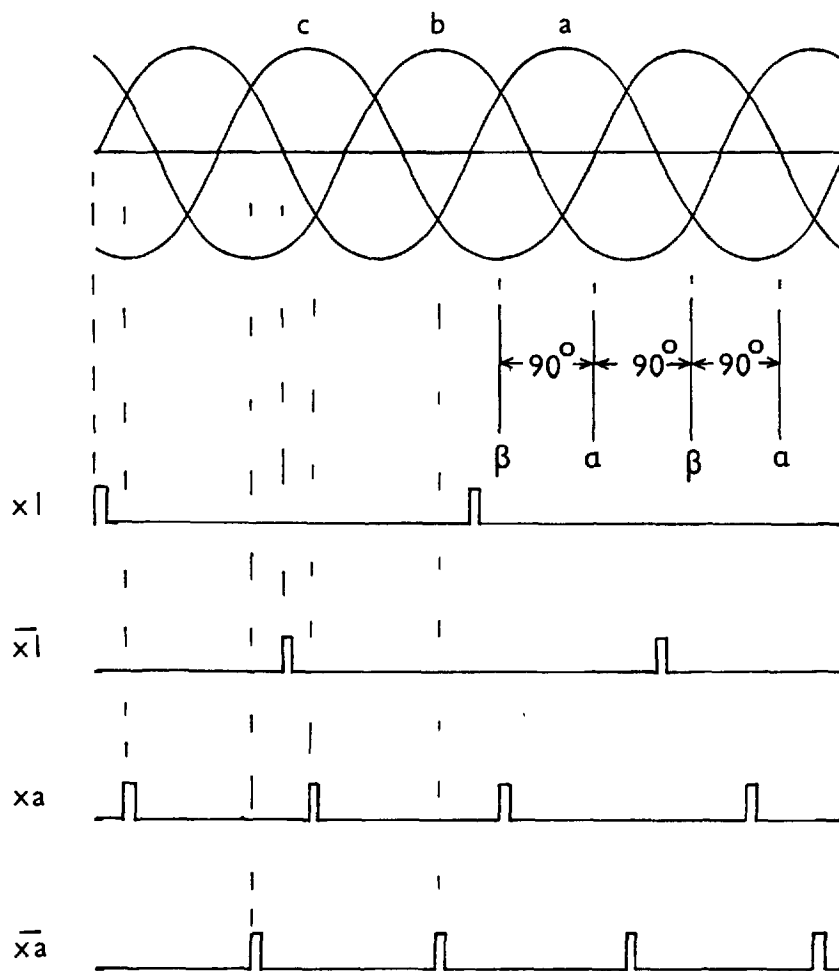


FIGURE 7.3 Phase 'a' Pulsing With Phase 'c' Reference

In Figure 7.4 possible combinations of input signals are given. Those combinations which result from a pulse sequence associated with a line b - to - line c fault are marked with a C inside the small circle. The combinations for the instantaneous value when phase 'a' is positive are shown to the right of the phase 'a' line.

In state 1 the instantaneous value of current in phase 'a' is negative. As the value decreases a pulse, $\overline{x_1}$, is received to indicate that one of the reference axes has been crossed and the circuit is stepped to state 2. Then, when the instantaneous current in phase 'a' becomes positive a change to state 3 occurs. When the next reference phase is crossed signals are received from both phase 'a' and phase 'c' and the paths through states 4 and 14 allow for either signal occurring first. When the instantaneous current in phase 'c' changes from positive to negative the state change is from 5 to 6. This figure is cyclic and can be followed through in this manner. When phase 'c' returns from negative to positive a change of state from 11 to 8 occurs. The arrowheads in this diagram are associated with the given changes so that a change from state 8 to state 11 indicated by the arrow and the pulse $\overline{x_3}$ also implies a change from state 11 to state 8 with the pulse signal x_3 .

The flow diagram gives all the possible conditions or states which the circuit is required to detect. It is then used to develop the flow table for the state assignment.

7.5 State Assignment Flow Table

The flow table contains the same information as the flow diagram but it is constructed so that secondary states can be assigned. The rows in the flow table represent the initial states and an element in a row represents a next state. If the output from a given state is 1, which is shown in the small circle of Figure 7.4, it is labelled with a Z.

To construct the flow table, Table 7.1, from the flow diagram, Figure 7.4, the following procedure is used. State 1 is positioned on row 1 and all the possible next states are entered in this row. That is, in Figure 7.4 there are two radial lines from state 1, therefore in row 1 of Table 7.1 there are two entries. These entries are for states 2 and 9, the two next possible states from state 1. Since they occur as a result of either pulse $\overline{x_a}$ or $\overline{x_b}$ they are entered in row 1 each under its appropriate pulse heading. Similarly, state 2 is assigned to row 2. It has three possible next states. Therefore there are three entries in Table 7.1, each in the column for the pulse which causes the entered state to occur. That is, pulse x_1 causes a change to state 3, pulse x_a causes a change to state 1 and pulse $\overline{x_b}$ causes a change to state 13. In the flow diagram, Figure 7.4, a small circled 1 appears beside state 3. This 1 represents an output and is entered in the flow table as a Z. Therefore in row 2 state 3 appears as state 3Z.

Stable State	Pulses												Logic Variable Assignment				
	x1	x2	x3	$\overline{x1}$	$\overline{x2}$	$\overline{x3}$	xa	xb	xc	$\overline{xa}$	$\overline{xb}$	$\overline{xc}$	y1	y2	y3	y4	y5
1										2	9		0	0	0	0	0
2	3 Z						1				13		0	0	0	0	1
3				2			4 Z					14 Z	0	0	0	1	1
4										3 Z		5 Z	0	0	0	1	0
5						6 Z			4 Z	14 Z			0	0	1	1	0
6			5 Z						19		24		0	0	1	1	1
7											10	8 Z	0	0	1	0	1
8						11 Z			7		12		0	0	1	0	0
9		10						1		13			0	1	1	0	0
10					9			7				12	0	1	1	0	1
11			8 Z						15 Z	17 Z			0	1	1	1	1
12								8	10				0	1	1	1	0
13							9	2					0	1	0	1	0
14							5 Z		3 Z				0	1	0	1	1
15										16 Z		11 Z	0	1	0	0	1
16	18						15 Z					17 Z	0	1	0	0	0
17							11 Z		16 Z				1	1	0	0	0
18				16 Z			20				23		1	1	0	0	1
19											21	6 Z	1	1	0	1	1
20										18	22		1	1	0	1	0
21					22			19				24	1	1	1	1	0
22		21						20		23			1	1	1	1	1
23							22	18					1	1	1	0	1
24								6 Z	21				1	1	1	0	0

Table 7.1 Flow Table Showing Restraint

This process of construction is continued until all rows are complete and then the variable assignments begin. In this example a binary progression was chosen as an assignment so that each entry in the flow table which is in decimal integer form represents its binary equivalent minus 1 as shown by Equations (5.16) and (5.17).

To assign states to the 24 rows of Table 7.1 five logic variables are required and their assignment states are shown in the last column. A variable map for each of these five variables for each of the twelve pulse inputs is necessary.

7.6 Variable Maps

The next step is the development of the variable maps for secondaries. In this case a variable map is developed for each input pulse together with each logic variable. This gives a total of sixty maps. However, only the maps for input pulses x_a , $\overline{x_a}$ and x_b are given as examples. These maps are formed for five possible entries I, $\emptyset$, 1, 0 and a blank which are defined below. The variable state map represents the response to an input pulse when the variable is in a defined initial state. The map entries are as follows:

- a) If the logic variable is at state 0 initially and the input pulse changes the state to 1, the map entry is an I.

- b) If the logic variable is at 1 and the pulse changes it to 0, the map entry is a $\emptyset$.
- c) If the logic variable is at 1 and the pulse retains it at 1, the map entry is 1.
- d) If the logic variable is at 0 and the pulse retains it at 0, the map entry is 0.
- e) An entry indicated by a blank means the pulse cannot occur generally or that the pulse causes no relevant change in logic variables.

These entries are made in the variable maps as above and Figures 7.5, 7.6 and 7.7 are given as examples. These maps for five variables VS1, VS2, VS3, VS4 and VS5 with outputs y1, y2, y3, y4 and y5 for an input pulse x2 are constructed from Table 7.1 as follows. First a Karnaugh map is constructed for the five output variables y1, y2, y3, y4 and y5 for each of the variables VS1, VS2, VS3, VS4 and VS5. This map has 32 cells. Each entry in the x_a column is then transferred to the maps for pulse x_a. In row 2 of the flow table, Table 7.1, there is an entry of 1. This is entered in the maps as follows. The logic variable assignment for row 2 is

y3 y4 y5			y1 y2				
			00	01	11	10	
000				0	$\emptyset$		
001			0		1		
011			0	0			
010				0			
110							VS1
111							
101					1		
100							

y3 y4 y5			y1 y2				
			00	01	11	10	
000				1	1		
001			0		1		
011			0	$\emptyset$			
010				1			
110							VS2
111							
101					1		
100							

y3 y4 y5			y1 y2				
			00	01	11	10	
000				0	I		
001			0		0		
011			0	I			
010				I			
110							VS3
111							
101					1		
100							

y3 y4 y5			y1 y2				
			00	01	11	10	
000				0	I		
001			0		I		
011			1	1			
010				$\emptyset$			
110							VS4
111							
101					I		
100							

y3 y4 y5			y1 y2				
			00	01	11	10	
000				I	I		
001			$\emptyset$		$\emptyset$		
011			$\emptyset$	$\emptyset$			
010				0			
110							VS5
111							
101					1		
100							

Figure 7.5 Variable Map for xa Pulse

y3 y4 y5				y1 y2	y3 y4 y5				y1 y2
				00 01 11 10					00 01 11 10
000	0				000	0			
001		0			001		1		
011					011				
010	0		1		010	0		1	
110	0			VS1	110	I			VS2
111		I	1		111		1	1	
101					101				
100		0			100		1		

y3 y4 y5				y1 y2	y3 y4 y5				y1 y2
				00 01 11 10					00 01 11 10
000	0				000	0			
001		0			001		0		
011					011				
010	0				010	1		$\emptyset$	
110	$\emptyset$		0	VS3	110	1			VS4
111		$\emptyset$			111		$\emptyset$	$\emptyset$	
101			1		101				
100		$\emptyset$			100		I		

y3 y4 y5				y1 y2	y3 y4 y5				y1 y2
				00 01 11 10					00 01 11 10
000	I								
001		$\emptyset$							
011									
010	I		I						
110	I			VS5					
111		$\emptyset$	1						
101									
100		0							

Figure 7.6 Variable Map for $\overline{x}a$ Pulse

y3 y4 y5	y1 y2			
	00	01	11	10
000				
001				
011				
010	0			
110	0	1		
111		1		
101	0	1		
100	0	∅		

VS1

y3 y4 y5	y1 y2			
	00	01	11	10
000				
001				
011				
010	∅			
110	∅	1		
111		1		
101	∅	1		
100	∅	∅		

VS2

y3 y4 y5	y1 y2			
	00	01	11	10
000				
001				
011				
010	0			
110	1	∅		
111		∅		
101	1	∅		
100	∅	1		

VS3

y3 y4 y5	y1 y2			
	00	01	11	10
000				
001				
011				
010	∅			
110	∅	1		
111		1		
101	0	0		
100	0	1		

VS4

y3 y4 y5	y1 y2			
	00	01	11	10
000				
001				
011				
010	I			
110	0	I		
111		∅		
101	1	1		
100	0	I		

VS5

Figure 7.7 Variable Map for xb Pulse

0 0 0 0 1

and from Table 7.1 the assignment for state 1 is

0 0 0 0 0 .

By the entry procedure above the maps

VS1 VS2 VS3 VS4 VS5

will each have assignments

0 0 0 0 $\emptyset$.

Thus in map VS1 the Karnaugh map cell representing row 2, that is cell

y1 y2 y3 y4 y5
0 0 0 0 1 ,

has an entry of 0 as has this cell in maps VS2, VS3 and VS4. However, this cell has an entry $\emptyset$ in the VS5 map (this particular entry is ringed in Figure 7.5 for identification).

Similarly the entries for row 17 and column xa is illustrated below. The logic variable assignment for row 17 which defines the map cell is

1 1 0 0 0

and in column xa state 11 has the variable assignment

0 1 1 1 1 .

The entry for each of the maps

VS1 VS2 VS3 VS4 VS5

from the procedure outlined is

Ø 1 I I I .

Thus locating the cell defined by

y1 y2 y3 y4 y5
1 1 0 0 0

the above entries in each map can be made.

By this procedure all the variable maps can be completed to give the map representation of the inputs to each logic variable.

Boolean expressions can be written for each logic variable input by examination of their maps. The expressions for the set inputs, S, are obtained by determining the Boolean function of all the I's, treating 1's and blanks as optional and the reset inputs, R, are obtained by determining the Boolean function of all the Ø's treating 0's and blanks as optional.

The Boolean equations for Figures 7.5, 7.6 and 7.7 are given below as an example. This example ignores the Boolean functions which are required for other pulses. However expressions from all the maps are determined in the following manner.

The Boolean expression for S1 is determined by examining map VS1 in Figures 7.5, 7.6 and 7.7. The Boolean expression for each cell in which 1 occurs is written. For variable VS1 the symbol 1 occurs only for the $\bar{x}a$ pulse in Figure 7.6. The expression for the cell in which it occurs is

$$\bar{y}1 \cdot y2 \cdot y3 \cdot y4 \cdot y5$$

By combining the expression for this cell with the pulse, $\bar{x}a$, the Boolean expression for S1 is as follows:

$$S1 = \bar{x}a \cdot \bar{y}1 \cdot y2 \cdot y3 \cdot y4 \cdot y5$$

The Boolean expression for R1 is determined by examining map VS1 in each figure to locate the cells in which $\emptyset$ occurs. $\emptyset$ occurs in Figure 7.5 for pulse xa in cell

$$y1 \cdot y2 \cdot \bar{y}3 \cdot \bar{y}4 \cdot \bar{y}5$$

and in Figure 7.7 for pulse xb in cell

$$y1 \cdot y2 \cdot y3 \cdot \bar{y}4 \cdot \bar{y}5$$

therefore by combining pulses and the cell notation the

Boolean expression for $S1$ is as follows:

$$S1 = (xa \cdot y1 \cdot y2 \cdot \overline{y3} \cdot \overline{y4} \cdot \overline{y5}) \vee (xb \cdot y1 \cdot y2 \cdot y3 \cdot \overline{y4} \cdot \overline{y5})$$

The Boolean expressions for $S2$ are obtained by finding 1's in map VS2 in each figure. An 1 occurs in Figure 7.6 for pulse $\overline{xa}$ in cell

$$\overline{y1} \cdot \overline{y2} \cdot y3 \cdot y4 \cdot \overline{y5} \quad .$$

Therefore the expression for $S2$ is

$$S2 = \overline{xa} \cdot \overline{y1} \cdot \overline{y2} \cdot y3 \cdot y4 \cdot \overline{y5} \quad .$$

0's occur in map VS2 in Figure 7.5 for pulse xc in cell

$$\overline{y1} \cdot y2 \cdot \overline{y3} \cdot y4 \cdot y5$$

and also in Figure 7.7 for pulse xb in the following 5 cells.

$$\overline{y1} \cdot y2 \cdot \overline{y3} \cdot y4 \cdot \overline{y5}$$

$$\overline{y1} \cdot y2 \cdot y3 \cdot y4 \cdot \overline{y5}$$

$$\overline{y1} \cdot y2 \cdot y3 \cdot \overline{y4} \cdot y5$$

$$\overline{y1} \cdot y2 \cdot y3 \cdot \overline{y4} \cdot \overline{y5}$$

$$y1 \cdot y2 \cdot y3 \cdot \overline{y4} \cdot \overline{y5}$$

This can be simplified (see Section 7.3) to

$$((\overline{y1} \cdot y2) \cdot ((y4 \cdot \overline{y5}) \vee (y3 \cdot \overline{y4}))) \vee (y3 \cdot \overline{y4} \cdot \overline{y5} \cdot y2)$$

Therefore the Boolean expression for R2 of map VS2 is

$$R2 = (x_a \cdot \overline{y1} \cdot y2 \cdot \overline{y3} \cdot y4 \cdot y5) \\ \vee ((x_b \cdot y4) \cdot (y1 \cdot (y4 \cdot \overline{y5} \vee y3 \cdot \overline{y4})) \vee (y3 \cdot \overline{y4} \cdot \overline{y5})) \quad .$$

Similarly, the expression for S3 can be developed from map VS3. I appears in map VS3 in Figure 7.5 for pulse x_a in three cells, namely

$$\overline{y1} \cdot y2 \cdot \overline{y3} \cdot y4 \cdot y5 \\ \overline{y1} \cdot y2 \cdot \overline{y3} \cdot y4 \cdot \overline{y5} \\ y1 \cdot y2 \cdot \overline{y3} \cdot \overline{y4} \cdot \overline{y5} \quad .$$

The simplified expression for S3 can be found by following the procedure given in Section 5.3. The Boolean expression for S3 is

$$S3 = (x_a \cdot y3 \cdot y2) \cdot ((y4 \cdot \overline{y1}) \vee (\overline{y4} \cdot \overline{y5} \cdot y1))$$

By this procedure the following expression is also obtained.

$$R3 = (\overline{x_a} \cdot y3 \cdot \overline{y1}) \cdot ((y4 \cdot \overline{y2} \cdot \overline{y5}) \vee (y2 \cdot y4 \cdot y5) \vee (y2 \cdot \overline{y4} \cdot \overline{y5}))$$

The expression obtained from I for map VS4 of Figure 7.5 for three cells is

$$x_a \cdot y1 \cdot y2 \cdot ((\overline{y3} \cdot \overline{y4}) \vee (y3 \cdot \overline{y4} \cdot y5))$$

For map VS4 of Figure 7.6 the expression for I is

$$\overline{a} \cdot \overline{y}_1 \cdot y_2 \cdot y_3 \cdot \overline{y}_4 \cdot \overline{y}_5$$

and of Figure 7.7 the expression for I is

$$x_b \cdot y_1 \cdot y_2 \cdot y_3 \cdot \overline{y}_4 \cdot \overline{y}_5 \quad .$$

Therefore the expression for S4 is obtained by combining the notation for these cells and is

$$\begin{aligned} S4 = & (\overline{a} \cdot \overline{y}_1 \cdot y_2 \cdot ((\overline{y}_3 \cdot \overline{y}_4) \vee (y_3 \cdot \overline{y}_4 \cdot y_5))) \\ & \vee (y_2 \cdot y_3 \cdot \overline{y}_4 \cdot \overline{y}_5 \cdot ((\overline{a} \cdot \overline{y}_1) \vee (x_b \cdot y_1))) \end{aligned}$$

Similarly, from Fig. V64 the expression for $\emptyset$ cells gives the Boolean equation for R4 which is

$$\begin{aligned} R4 = & (y_2 \cdot y_4 \cdot (((\overline{a} \cdot \overline{y}_3) \vee x_b) \cdot \overline{y}_1 \cdot \overline{y}_5)) \\ & \vee (\overline{a} \cdot (y_3 \cdot y_5) \vee (y_1 \cdot \overline{y}_3 \cdot \overline{y}_5))) \end{aligned}$$

Similarly, the procedure is repeated for S5 to obtain

$$\begin{aligned} S5 = & (\overline{a} \cdot \overline{y}_1 \cdot \overline{y}_2 \cdot \overline{y}_3 \cdot ((\overline{y}_3 \cdot \overline{y}_4) \vee y_4)) \\ & \vee (y_2 \cdot y_3 \cdot \overline{y}_5 \cdot ((\overline{a} \cdot \overline{y}_4) \vee (\overline{a} \cdot y_1 \cdot y_4))) \\ & \vee (\overline{a} \cdot y_2 \cdot \overline{y}_5 \cdot ((\overline{y}_1 \cdot \overline{y}_3 \cdot y_4) \vee (y_1 \cdot y_3))) \quad . \end{aligned}$$

Finally, the Boolean expression for R5 is

$$\begin{aligned} R5 = & (\overline{a} \cdot \overline{y}_3 \cdot y_5 \cdot ((\overline{y}_1 \cdot (\overline{y}_2 \vee y_4)) \vee (y_1 \cdot y_2 \cdot y_4))) \\ & \vee (\overline{a} \cdot \overline{y}_1 \cdot y_2 \cdot y_5 \cdot ((\overline{y}_3 \cdot \overline{y}_4) \vee (y_3 \cdot y_4))) \\ & \vee (x_b \cdot y_1 \cdot y_2 \cdot y_3 \cdot y_4 \cdot y_5) \quad . \end{aligned}$$

7.7 Restraint Outputs

The restraint output is formed from Table 7.1 by taking the coordinates of each cell in which a Z appears and writing the Boolean expression for it. There are no Z terms in the first row. The Boolean expression for row 2 is obtained from the coordinates of cell 3Z. The pulse input for this cell is x1 which is combined with the logic variable assignment to obtain the output term

$$x1 \cdot \bar{y}1 \cdot \bar{y}2 \cdot \bar{y}3 \cdot \bar{y}4 \cdot y5$$

There are two cells in row 3 occupied by Z terms. The Boolean expression for the coordinates of the cell occupied by 4Z is composed of the pulse input xa combined with the logic variable assignment. Thus the output term of 4Z is

$$xa \cdot \bar{y}1 \cdot \bar{y}2 \cdot \bar{y}3 \cdot y4 \cdot y5$$

This term can be expanded to include the coordinates of the cell occupied by 14Z. The pulse input to this cell is $\bar{x}c$ and it is combined with the other cell term above to obtain the full expression for the output of row 3 which is

$$(\bar{x}c \vee xa) \cdot \bar{y}1 \cdot \bar{y}2 \cdot \bar{y}3 \cdot y4 \cdot y5$$

The terms for the complete table can be obtained in this manner.

The terms in Table 7.1 which are denoted with a Z form the set inputs, S, for the phase 'a' restraint variable VRI and the terms without Z form the reset inputs, R. The output from VRI is $z1$ or $\bar{z1}$. Each phase in a feeder requires a logic variable to indicate when a tripping restraint exists.

7.8 Comparison Circuit Flow Table and Boolean Expressions

The development of the Boolean expressions for the set and reset inputs to the comparison variables, VC, is greatly simplified by using the state assignments given in Table 7.1. The flow diagram, Figure 7.4, and the flow table, Table 7.1, have many redundant states since only six states are required to define the different flow directions in a three phase line. However the states in Figure 7.1 can be combined into six groups which are then used to define flow directions. This is accomplished by introducing into Figure 7.1 a dividing line for each phase. On one side of the dividing line the instantaneous current is negative and on the other side it is positive. One line for each phase divides the states of Figure 7.1 into six groups. Since the variable assignment for secondaries has been made for these states and since all the variable maps have been completed, it is more convenient and economical to use the assignments already given.

In Figure 7.4 the phase 'a' line divides the states into two groups. The states on the positive side

of this line are associated with an output which indicates positive instantaneous current and the other states are associated with a negative instantaneous current. Therefore although the same state assignment and variable equations can be used, new output equations are required. This is accomplished by assigning new outputs to each state in the flow table.

The comparison circuit flow table for phase 'a' is given in Table 7.2. The only change between this table and Table 7.1 is in the output assignments. Each state is assigned an output P or N in accordance with its relationship to the phase 'a' dividing line of Figure 7.4. P indicates positive instantaneous current and N indicates negative instantaneous current. Therefore the two states 2 and 9 which occur in row 1 have an assigned output. Since they are both on the negative side of the phase 'a' line, the output assignments are N for both these states. In row 2 there are the three states 3, 1, 13. Since state 3 is on the positive side of the phase 'a' line state 3 is given an output assignment P. States 1 and 13 are on the negative side and are each given output assignments N. In this manner Table 7.2 is completed. Any given state must always have the same output assignment no matter where it occurs in the table.

Once a complete state diagram is developed and the logic variable assignment and variable maps have been completed, the same variable assignment and equation can be used for each phase. It is only the output assignments and the output equations which differ.

Stable State	Pulses											
	x_1	x_2	x_3	$\overline{x_1}$	$\overline{x_2}$	$\overline{x_3}$	x_a	x_b	x_c	$\overline{x_a}$	$\overline{x_b}$	$\overline{x_c}$
1										2N	9N	
2	3P						1N				13N	
3				2N			4P					14P
4										3P		5P
5						6P			4P	14P		
6			5P						19P		24P	
7											10N	8N
8						11N			7N		12N	
9		10N						1N		13N		
10					9N			7N				12N
11			8N						15N	17N		
12								8N	10N			
13							9N	2N				
14							5P		3P			
15										16N		11N
16	18P						15N					17N
17							11N		16N			
18				16N			20P				23P	
19											21P	6P
20										18P	22P	
21					22P			19P				24P
22		21P						20P		23P		
23							22P	18P				
24								6P	21P			

Table 7.2 Flow Table Showing Comparison

The equation for the set and reset inputs to comparison variable V_{C1} for Table 7.2 is developed as in the previous section. For example, states 2 and 9 in row 1 have output assignments H . For state 2 the pulse input is $\bar{x}_2$ which is combined with the logic variable assignment for row 1 to obtain the expression

$$\bar{x}_2 \cdot \bar{y}_1 \cdot \bar{y}_2 \cdot \bar{y}_3 \cdot \bar{y}_4 \cdot \bar{y}_5 \quad .$$

This can be combined with the pulse input for state 9 to obtain the complete H expression for row 1

$$(\bar{x}_2 \vee \bar{x}_9) \cdot \bar{y}_1 \cdot \bar{y}_2 \cdot \bar{y}_3 \cdot \bar{y}_4 \cdot \bar{y}_5 \quad .$$

State 3 in row 2 is part of the expression for variable P and is formed by taking the input signal x_1 and combining it with the row 2 logic variable assignment. It is

$$x_1 \cdot \bar{y}_1 \cdot \bar{y}_2 \cdot \bar{y}_3 \cdot \bar{y}_4 \cdot \bar{y}_5 \quad .$$

Similarly, for states 1 and 13 in this row the R variable expression is given as

$$(x_2 \vee \bar{x}_9) \cdot \bar{y}_1 \cdot \bar{y}_2 \cdot \bar{y}_3 \cdot \bar{y}_4 \cdot \bar{y}_5 \quad .$$

By this method the input expressions for the comparison variable, V_{C1} , can be completed. All terms from the expression for P are used as set inputs, F_1 , of variable V_{C1} and all terms from the expression for R are used as reset inputs, R_1 , of variable V_{C1} . The outputs, p_1 or $\bar{p}_1$, from variable V_{C1} give the current polarity.

When voltamps flow into a substation busbar on the same phase for all feeders, the output from all their comparison variables for this phase are the same at one instant in time. When all the restraint variables are not set the above condition indicates a busbar fault. Therefore this combination of signals can be used to indicate a trip of all busbar feeder breakers.

If for example the substation busbar has four feeders numbered 7, 8, 9 and 10 the comparison variable outputs for phase 'a' on these feeders can be numbered 1, 2, 3 and 4 respectively. The outputs are all the same when either

$$(p1 \cdot p2 \cdot p3 \cdot p4)$$

occurs or

$$(\bar{p1} \cdot \bar{p2} \cdot \bar{p3} \cdot \bar{p4})$$

occurs. When no restraint occurs the restraint variables such as V_{R1} and $M2$ have outputs $\bar{Z1}$ and $\bar{Z2}$ respectively. A substation busbar with four feeders has a restraint variable for each feeder on phase 'a' for which the outputs, when no restraint occurs, are $\bar{Z1}$, $\bar{Z2}$, $\bar{Z3}$ and $\bar{Z4}$ respectively. Since a restraint signal does not occur on any feeder under busbar fault conditions all these signals must be present to indicate tripping is required. The expression which gives the condition when restraint does not block the tripping signal is

$$(\bar{Z1} \cdot \bar{Z2} \cdot \bar{Z3} \cdot \bar{Z4})$$

Combining the comparison signals and the restraint signals the following expression gives the condition for phase 'a' which requires that the four network substation feeder breakers are to be tripped.

$$\text{TRIP} = (\overline{z1} \cdot \overline{z2} \cdot \overline{z3} \cdot \overline{z4}) \cdot ((p1 \cdot p2 \cdot p3 \cdot p4) \vee (\overline{p1} \cdot \overline{p2} \cdot \overline{p3} \cdot \overline{p4}))$$

7.9 Computer Applications

This method of busbar protection is developed for use with high speed digital computers. Since the variables, VS, VR, VC, are flip-flop devices they are the same as storage units in a computer. The 'and'/'or' logic is similar to the arithmetic unit. Thus with a program based on the method developed above a standard arithmetic unit and core store can be used with suitable peripheral equipment to protect high voltage substation busbars.

The Boolean expressions developed for the secondaries, VS, the restraints, VR, and the comparison variables, VC, enter the computer in the form of software. Since these operations are performed by the computer arithmetic unit there is little need to limit their number.

The advantages that this method is likely to have over other methods of busbar protection by computer are in the simplicity of peripheral equipment required and in the savings in core store. It is for these

reasons that further study of this method is recommended.

The disadvantage is in the difficulty of establishing a state flow diagram (see Figure 7.3) which gives a completely adequate description of all possible conditions for healthy and unhealthy busbars.

CHAPTER 8

CONCLUSIONS

8.1 Use of the Substation Simulation Equations

The development of the network simulator in Chapter 3 follows the MIDAS (51) programming methods. However for the solution of problems, generally, the programs are converted to MINIC (52). The MIDAS type of flow diagram is useful during the development stage but there are disadvantages in the language due to the speed of convergence and in the organisation of the operational blocks because of the great number of cards which must be handled. The convergence is a problem because the stop routine does not work satisfactorily with the result that non-converging programs are unnecessarily wasteful of computer time. The MINIC program converges faster than MIDAS and is more convenient since equations are written in a form similar to Fortran IV.

The establishment of the initial network conditions for the simulator integrators to represent load conditions is time consuming. However, using the values given in Appendix A, established by trial and error, much of the difficulty can be reduced. Simulator setting is dependent upon establishing the value of EP of Figures 3.3 and 3.4 and the value of TT of Figure 3.6. TT is varied to change the input power to the network to maintain the required output power balance at the

substation busbar. The two values differ by the amount of the power loss in the network. As the representation of the network becomes more complex the difficulty of establishing the value of T_1 is increased. Changes in EP affect the VAR flow and determining this value is more difficult because the magnitude of the ratio of output to input can vary between 20 and 100. For future work it is recommended that a feedback loop to automatically set these values be developed.

With the transforms of Equations (2.1) and (3.55) the network simulation program developed in Chapters 2 and 3 is an excellent way of determining instantaneous quantities. This method can be extended to study other network problems where instantaneous values of current and voltage are required.

The transform which is given in Equation (2.1) was not applied to the simulation of the circulating current scheme for reasons explained in Chapter 3. From experience obtained in working with transformed and time domain values the superiority of transformation techniques became evident. A practical method of using two-axis transforms for systems based on different reference axes is therefore proposed.

8.2 Rotational Reference Frames

Kron (34) has outlined a method of tensors using the connection matrix, K , to formalise the

transformation of networks. The transform of Equation (2.1) is not a tensor since pK is not zero. None the less, a law of transformation does exist and the formalised approach can be used.

A rotational frame has a connection matrix K ,

$$K = \begin{bmatrix} \cos \theta_1 & \sin \theta_1 \\ -\sin \theta_1 & \cos \theta_1 \end{bmatrix}, \quad (8.1)$$

and again

$$pK \neq 0 \quad . \quad (8.2)$$

In the balanced case

$$K = e^{-j\theta_1} \quad . \quad (8.3)$$

The law of transform with a time dependent connection matrix is given by (34)

$$Z = K_t^* Z_0 K + K_t^* \epsilon \frac{K}{\theta_1} p \theta_1 \quad . \quad (8.4)$$

With this technique all currents at a substation busbar could be determined in a two-axis field with the same reference axis. This technique also provides a powerful method of using Park's transform for complex busbar equations, for example Equation (3.41).

8.3 Improved Power Network Differential Equation Representation

The problem which still remains is to establish a technique for ordering the simulator equations so that the arrangement of the program does not limit the simulation to one feeder at a time as is now the case. Another problem, entirely different, but which should be considered in the solution concerns the transmission line simulation. Transmission line equations are functions of two independent variables, time and distance. The solution of the differential equation for one variable in the LIBIC program is by the Runge Kutta method. Numerical methods for the solution of second order partial differential equations (10) would give a more accurate simulation of long transmission lines.

The arrangement of the LIBIC program is for a more general solution of a differential equation. If a program of the LIBIC type is to be used entirely for power network simulation a more powerful program would be achieved by writing subroutines for machines, transmission lines, transformers, etc. This has to some degree now been done in this thesis. However, if the operators of the program such as multiplication, division, integration, etc., were to be replaced by operators representing the above subroutines, that is, machine, transmission line, etc., power networks could be 'patched' up. This rearrangement or development into a new basic program could be written for the solution of partial differential equations and for multiple networks.

This would give a program which would be more effective for power network analysis.

8.4 Controller Programs

In Chapters 5 and 6 a method of utilising memory and logic is applied to switching. These chapters show the feasibility of the application. The method in Chapter 5 has a limitation in the computer development because of the number of empty spaces required in each table. If the disadvantage of non-economy of variables in logic functions can be overcome the method of Chapter 7 would appear more attractive. However, this disadvantage is not really very important in a controller application and it is recommended that future development be along the lines outlined in Chapter 7. The advantage of this method is the economy of working space in the computer development of logic variable equations.

8.5 Controller Coordination and Features

The controller functions dealt with in this thesis are those of busbar fault detection and substation switching. A logic controller could be programmed to provide these functions in conjunction with each other. The controller as proposed here has the independent job of supervising switching to guard against incorrect operation. In the event of a busbar fault the controller detects the fault, clears the faulted zone and reswitches

the substation to maintain transmission capability. Since it contains the switching arrangement of the substation the controller can be used to select the feeders from which protection signals are required. Thus it would eliminate supervisory and protection circuit switching and interlocking as it exists at present.

Problems in interlocking associated with rearrangements and extensions to the substation can be greatly reduced by the controller. A new program with a different set of restraints and operating sequences can be determined for any temporary condition of substation operation thus simplifying the procedures in providing safe conditions during alteration.

In a substation, functions such as feeder protection, busbar protection, interlocking, alarm annunciation, checking for faulty equipment and data recording are at present carried out by separate items of equipment, each developed for reliability, low cost and easy maintenance. However, the integration of this equipment into a single control system often leads to problems of incompatibility, inflexibility and specialised components. Considerable valuable space and the continuous attention and time of the operators are required.

A centralised system of substation control would be a desirable development wherein all the functions at present performed separately by individual components

could be grouped together in a central controller. This would enable equipment to be time shared and automatically checked and maintained. The controller would have high speed logic units, memory units, calculating facilities and the necessary peripheral equipment.

A method of programming the controller would provide a system with the desirable feature of flexibility.

One of the functions of this controller would be the automatic recording and checking of power and VAR flow voltage level and other operating conditions. The control of transformer tap changes would be programmed and the control of load shedding by voltage reduction can be incorporated. Discrete operations such as circuit breaker and lightning arrester operations would be counted.

It is essential that the controller can communicate information to the control engineer. Printed information would provide a permanent record of operation. The time, type and sequence of alarm signals would be recorded. However, in addition, alarms can be indicated both audibly by horn and visibly by picture display. It is possible that the printout be arranged not only to indicate the basic cause, but also the corrective action to be taken.

A dummy signal from the controller can be used to check peripheral and substation equipment. One arrangement can be to make equipment which is seldom

used polarity sensitive. A dummy signal of the opposite polarity would be used to check continuity of wiring.

8.6 Network Control

This thesis is intended to form part of an overall plan proposed by the Central Electricity Generating Board (35) for an integrated network controller. As the national grid increases its capacity for energy transmission, more and more control functions will be performed at the transmission high voltage substation. The substation operator will be required to perform some novel and more sophisticated duties, as well as his conventional ones. This substation controller is intended as an aid so that the operator will not find that more of his time is devoted to switching functions. With more work to do, the operator must be provided with every possible means of increasing his productivity.

8.7 Future Busbar Fault Studies

The network simulation equations of Chapter 3 provide an excellent method of producing the instantaneous waveforms of a network required for the study of system disturbances. It is proposed that the simulation be extended to include the features outlined in Sections 8.1, 8.2 and 8.3. It is also proposed that the equations in Chapter 7 be included in the network simulation by use of the logic functions 'and', 'or' and 'function switch' (see Section 7.1) and the hybrid

function of 'flip-flop' which are available in the MILIC program. The inclusion of these protection system equations in the simulation provides a method of testing and developing the pulsing sequence (see Section 7.4).

The method of sampling proposed by Cory (17) should be an improvement in the application of Kirchoff's second law for busbar fault detection. It is recommended that an investigation into the available equipment and problems of a practicable installation be undertaken.

8.8 New Developments Considered in this Thesis

The purpose of the network simulation of Chapter 3 is to provide a convenient method of modeling the widest possible range of equipment involved in an electrical network. The program used is applicable to any system which can be described in differential equation or logic equation form.

The equations which are generally used to simulate networks are applicable to the analogue simulation of steady state conditions. The digital computer simulation used here is for transient conditions. In previous simulations neglecting transient terms has led to great simplifications. These terms produce closed loops in the simulation which are not permitted in the digital simulation programs. Therefore all

machine equations in Chapter 3 which involve transient terms are developed in a new form. This also applies to the simulation of short transmission lines. The equations for long transmission lines and protective circuits are an original development of this thesis. All asymmetrical waveform equations using α and β components are new developments.

In this thesis the use of transforms is extended to include network equipment other than machines to provide a representation suitable for application to iterative techniques.

The introduction of the use of switching algebra for solving problems in substation switching is a new development in this thesis. In Chapter 5 a method of obtaining Boolean expressions from a switching algebra is given for application to automatic switching of substations. A digital computer program based on this method is developed. Properties of group theory applied to determine the optimum combination of rows is a new development used in this program. The way in which substation operators can use this program is illustrated. A proposal is given in Chapter 7 outlining the way of applying switching algebra to substation busbar protection.

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APPENDIX ASUBSTATION NETWORK PARAMETERSA.1 Primary Parameters for Substation Representation

	Feeder Number			
	7	8	9	10
x_d	1.409	1.6	1.85	0.7958
x_q	1.35	1.72	1.57	0.68
x_d'	0.235	0.203	0.245	0.0763
x_d''	0.138	0.14	0.19	0.0572
x_a	0.12	0.09	0.16	0.0392
r_a	0.00219	0.00118	0.00207	0.00057
T_d'	1.42	1.46	0.81	0.8
T_d''	0.05	0.05	0.02	0.019
T_q''	0.06	0.06	0.021	0.0205
H	3.375	4.83	5.055	3.28
Rating	50	120	222	333
x_q''	0.141	0.1548	0.2051	0.0709
x_e	0.00568	0.0579	0.	0.0204
r_e	0.00163	0.	0.	0.003

A.2 Calculated Values for Substation Representation

	Feeder Number			
	7	8	9	10
x_{md}	1.289	1.71	1.69	0.7566
x_f	0.126	0.219	0.0895	0.0391
x_{kd}	0.0214	0.0673	0.0465	0.0334
L_{md}	0.00411	0.00544	0.00538	0.00241
r_f	0.000529	0.000663	0.000923	0.000303
r_{kd}	0.00509	0.00819	0.0163	0.00896
T_1	8.53	9.23	6.14	8.37
T_2	0.82	0.692	0.34	0.281
T_3	0.0846	0.1015	0.0258	0.0251
T_{kd}	0.0134	0.0257	0.00909	0.012
x_{mq}	1.23	1.63	1.41	0.6408
x_{kq}	0.0214	0.0673	0.0465	0.0334
r_{kq}	0.00692	0.00809	0.0288	0.0109
T''_{qo}	0.577	0.668	0.161	0.197
B_{d1}	1742.8	1442.7	959.94	3105.0
B_{d2}	-12.118	-10.254	-2.3787	-4.5066
A_{d1}	-0.8443	-0.85731	-0.87146	-0.90557
A_{d2}	-0.057759	-0.064912	-0.025836	-0.022555
α_{d1}	0.10777	0.10179	0.160132	0.11732
α_{d2}	12.849	10.489	40.746	41.061

A.3 Power and VAR Flow for Substation Representation

	Feeder Number			
	7	8	9	10
Power	-35	-80	-185	300
VARs	-23.2	-35.4	0.	58.6
T_t	0.70283	0.694555	0.834771	-0.897001
EF	0.00111814	0.00109675	0.0014641	0.0006428
pu Power	-0.700005	-0.666624	-0.833333	0.899947
pu VARs	-0.461576	-0.295159	0.0008202	0.176098
MEG	0.175	0.42	0.778	1.165

A.4 Simulator Initial Conditions for Substation Representation

	Feeder Number			
	7	8	9	10
I1	0.00391726	0.00385152	0.00274348	0.00367325
I2	0.00226711	0.00275821	0.00357869	-0.00254999
I3	-1.06197	-0.899548	-0.936009	-0.542381
I4	-13.5132	-8.50812	-24.0229	-61.7628
I6	0.527599	0.503832	0.716101	-1.17808
I7*	-3.59296	-11.6695	-0.0093904	-4.33569
I8	-3.66835	-3.78501	-4.05834	3.76627

* $\times 10^{-5}$

A.5 Primary Parameters for Long Line Representation

x_d	0.9403
x_q	0.568
x_d'	0.237
x_d''	0.1451
x_a	0.0996
r_a	0.007
T_d'	0.204
T_d''	0.022
H	3.64
x_q''	0.1425
x_e	0.045
r_e	-0.00483
c	0.00172
g	0.
ℓ or l_e	0.000143

A.6 Calculated Values for Long Line Representation

x_{md}	0.8427
x_f	0.2124
x_{kd}	0.0383
L_{md}	0.000268
r_f	0.00446
r_{kd}	0.01465
T_1	0.885
T_2	0.2095
T_3	0.046
T_{kd}	0.00832
x_{mq}	0.4684
x_{kq}	0.0383
r_{kq}	0.01465
T''_{qo}	0.094
B_{d1}	136.07
B_{d2}	-7.381
A_{d1}	-0.6982
A_{d2}	-0.14278
α_{d1}	1.651
α_{d2}	25.922

A.7 Simulator Initial Conditions for Long Line Representation

	Feeder Number	
	1	2
T_t	1.01181	-0.98822
EF	0.015691	0.015495
I1	3.97164×10^{-3}	0.00385711
I2	2.22955×10^{-3}	-0.00221609
I3	-0.692333	-0.705405
I4	-42.4612	-41.5334
I6	1.23317	-1.22575
I7	-1.44377×10^{-4}	0.002127
I8	-3.65312	3.66309
I9	-1.19642×10^{-3}	1.20597×10^{-3}
I10	-9.90038×10^{-5}	-1.00874×10^{-4}
I11	2.13125×10^{-3}	2.09897×10^{-3}
I12	1.76344×10^{-4}	-1.75282×10^{-4}
I13	-9.32610×10^{-5}	-1.06663×10^{-4}
I14	1.71087×10^{-7}	-1.72453×10^{-7}
I15	1.66114×10^{-4}	-1.85357×10^{-4}
I16	-3.04769×10^{-7}	-3.00153×10^{-7}

APPENDIX BDEFINITION OF A BOOLEAN ALGEBRA

A Boolean algebra B is a set of elements x , y , z , ... with the following properties.

- B.1 B has two binary operations, $\vee$ and $\cdot$, which satisfy the idempotent, commutative, associative and distributive laws.
- B.2 B has a binary relation denoted by $\leq$ which is reflexive, antisymmetric, and transitive and satisfies the consistency principle.
- B.3 B contains two elements 0 and 1 which are universal bounds and satisfy the intersection and union laws.
- B.4 B has a unary operation of complementation, $\bar{}$, which obeys the complementary, dualization and involution laws.

It is convenient to read the Boolean operators and relations as follows:

$\vee$	or
$\cdot$	and
$\leq$	implies
$\bar{}$	not

A symbolic representation of the properties of a Boolean algebra are as follows:

Idempotent	$x \cdot x = x$ and $x \vee x = x$
Commutative	$x \cdot y = y \cdot x$ and $x \vee y = y \vee x$
Associative	$x \cdot (y \cdot z) = (x \cdot y) \cdot z$ and $x \vee (y \vee z) = (x \vee y) \vee z$
Distributive	$x \cdot (y \vee z) = (x \cdot y) \vee (x \cdot z)$ and $x \vee (y \cdot z) = (x \vee y) \cdot (x \vee z)$
Reflexive	$x \leq x$, for all x
Antisymmetric	$x \leq y$ and $y \leq x$ then $x = y$
Transitive	$x \leq y$ and $y \leq z$ then $x \leq z$
Consistency	$x \leq y$, $x \cdot y = x$, $x \vee y = y$ are mutually equivalent
Universal bounds	$0 \leq x \leq 1$ for all x
Intersection	$0 \cdot x = 0$ and $1 \cdot x = x$
Union	$0 \vee x = x$ and $1 \vee x = 1$
Complementary	$x \cdot \bar{x} = 0$ and $x \vee \bar{x} = 1$
Dualization	$\overline{(x \cdot y)} = \bar{x} \vee \bar{y}$ and $\overline{(x \vee y)} = \bar{x} \cdot \bar{y}$
Involution	$\overline{\bar{x}} = x$

APPENDIX CSOME PROPERTIES OF BOOLEAN MATRIX MULTIPLICATION

Boolean matrix multiplication should not be confused with arithmetic and matrix multiplication. Boolean matrix multiplication is defined as follows.

$$[B] [C] = [D]$$

where each column of matrix $[D]$ is obtained by comparing the corresponding column of matrix $[C]$ with those in matrix $[\lambda(n)]$ (see Section 5.2.3) and taking that column of matrix $[B]$ which is in the same relative position as the column in $[\lambda(n)]$ equivalent to that of $[C]$. That is,

$$\text{column } m \text{ of } [D] = \text{column } s \text{ of } [B]$$

where column s of $[\lambda(n)]$ is equivalent to column m of $[C]$.

To illustrate Boolean matrix multiplication consider the following example.

$$[B] [C] = [D]$$

where

$$[B] = \begin{bmatrix} 0 & 1 & 1 & 0 \\ 1 & 1 & 0 & 1 \end{bmatrix}$$

$$[C] = \begin{bmatrix} 1 & 1 & 0 & 0 \\ 0 & 1 & 0 & 1 \end{bmatrix}$$

and

$$[\lambda(n)] = \begin{bmatrix} 0 & 1 & 0 & 1 \\ 0 & 0 & 1 & 1 \end{bmatrix}$$

To obtain column 1 of $[D]$, note that column 1 of $[C]$,

$$\begin{bmatrix} 1 \\ 0 \end{bmatrix},$$

is equivalent to column 2 of $[\lambda(n)]$ and then that column 2 of $[B]$ is

$$\begin{bmatrix} 1 \\ 1 \end{bmatrix}$$

This then is column 1 of $[D]$. Similarly,

$$\text{column 2 of } [D] = \text{column 4 of } [B]$$

$$\text{column 3 of } [D] = \text{column 1 of } [B]$$

$$\text{column 4 of } [D] = \text{column 3 of } [B]$$

Hence

$$[D] = \begin{bmatrix} 1 & 0 & 0 & 1 \\ 1 & 1 & 1 & 0 \end{bmatrix}$$

Taking the decimal vector equivalents of the binary matrices given above the illustration of Boolean matrix multiplication is more easily understood. The decimal vector equivalents of the binary matrices $[B]$, $[C]$ and $[\lambda(n)]$ are

$$\begin{aligned} \vec{B} &= [2 \quad 3 \quad 1 \quad 2] \\ \vec{C} &= [1 \quad 3 \quad 0 \quad 2] \\ \text{and} \quad \vec{\lambda(n)} &= [0 \quad 1 \quad 2 \quad 3] \end{aligned}$$

respectively. Then, following the Boolean matrix multiplication procedure,

$$\begin{aligned} \vec{D} &= \vec{B} \vec{C} \\ &= [2 \quad 3 \quad 1 \quad 2][1 \quad 3 \quad 0 \quad 2] \\ &= [3 \quad 2 \quad 2 \quad 1] \end{aligned}$$

which is the decimal vector equivalent to the binary matrix $[D]$.

Since

$$\begin{aligned} \vec{C} \vec{B} &= [1 \quad 3 \quad 0 \quad 2][2 \quad 3 \quad 1 \quad 2] \\ &= [0 \quad 2 \quad 3 \quad 0] \end{aligned}$$

is not equal to $\vec{D}$,

$$\vec{B} \vec{C} \neq \vec{C} \vec{B}$$

and Boolean matrix multiplication is not commutative. Also, as

$$\begin{aligned}\vec{C} \vec{C} &= \begin{bmatrix} 1 & 3 & 0 & 2 \end{bmatrix} \begin{bmatrix} 1 & 3 & 0 & 2 \end{bmatrix} \\ &= \begin{bmatrix} 3 & 2 & 1 & 0 \end{bmatrix}\end{aligned}$$

is not equal to $\vec{C}$, $\vec{C} \vec{C} \neq \vec{C}$, the idempotent law does not hold.

The inverse of a matrix $[A]$ with respect to Boolean matrix multiplication, $[A]^{-1}$, is defined as the matrix for which

$$[A][A]^{-1} = [\lambda(n)]$$

where $[\lambda(n)]$ (see Section 5.2.3) is the identity matrix. Using vector notation,

$$\vec{A}^{-1}$$

is the inverse of $\vec{A}$ if

$$\vec{A} \vec{A}^{-1} = \vec{\lambda(n)}$$

Since one of the columns of $[\lambda(n)]$ does not appear in $[B]$ in the above example, the inverse of $[E]$ does not exist. However, the inverse of matrix $[C]$ does exist and can be found from

$$[C][C]^{-1} = [\lambda(n)]$$

Using the equivalent decimal vectors, the inverse of $\overrightarrow{C}$,
 $[1 \ 3 \ 0 \ 2]$, is

$$\overrightarrow{C^{-1}} = [2 \ 0 \ 3 \ 1]$$

since

$$\begin{aligned} \overrightarrow{C} \ \overrightarrow{C^{-1}} &= [1 \ 3 \ 0 \ 2] [2 \ 0 \ 3 \ 1] \\ &= [0 \ 1 \ 2 \ 3] \\ &= \overrightarrow{\lambda(n)} \end{aligned}$$

and $\overrightarrow{\lambda(n)}$ is the decimal vector equivalent to the binary identity matrix $[\lambda(n)]$.

AUTOMATIC SWITCHING

By B.J. Cory and G.S. Hope

List of Symbols

- f function of a Switching algebra
- and (Binary operation of algebra)
- V or (Binary operation of algebra)
- not (Unary operation of algebra)

1. Introduction To achieve a reduction in the cost of electricity supply the present trend is toward the installation of large generating units which require automated controls to achieve maximum efficiency of operation. A start has been made in many countries to apply some measure of automatic control to the transmission and distribution systems so that they are compatible with the large generating units and the reliability and flexibility demanded by electricity consumers. So far system control has consisted largely of automatic load forecasting, plant ordering and frequency control. As automatic control methods become established their extension to other aspects of system control will follow. It is the purpose of this paper to record the progress being made on a method of switching control which has application to areas of the transmission network as well as a H.V. substation.

One method of using mathematical logic to describe the switching and interlocking of power system networks and equipment has already been described (1). By the use of set theory as well as mathematical logic it is possible to use a suitable controller to switch automatically the circuit breakers and power operated isolators in a network or substation. For the purpose of this paper all circuit breakers and isolators required to be operated by an automatic controller will be referred to as switches and the theory will be developed in terms of a single substation. Extension of the method to networks is possible provided adequate telemetering facilities are available. Since automatic switching will be only one of the functions required of a system or station controller, the method developed using set theory here is applicable to digital programming of a central control computer with peripheral input - output equipment.

2. Application of Set Theory Set theory is applied in the development of the method of control and the switches of a substation are considered as elements of a set. The elements connected to any one busbar form a subset and the set of all possible switching combinations of this subset forms a Boolean algebra.

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Switching states are presented in Karnaugh Map form (2) with all feasible switching combinations represented in columns. An example of a Karnaugh Map representation for four switches (w, x, y, z) is as follows

				y	
				┌───────────┐	
w	{	0000	0001	0011	0010
		0100	0101	0111	0110
		1100	1101	1111	1110
		1000	1001	1011	1010
		└───────────┘			
		z			

Figure 1. Karnaugh Map for four switches

In this map the sixteen possible ways the four switches can be switched are shown. Using '1' to denote closed and '0' to denote open, position 0000 represents all switches open, position 0111 represents switches w open and x, y, z closed, position 1010 represents switches x and z open and w and y closed. The two rows indicated by w denote the positions in which w has a value of '1'. These positions are similarly indicated for x, y and z. A more convenient representation in Karnaugh Map form is as follows

		y z				
		00	01	11	10	
wx	00	1				$= (\bar{w} \cdot \bar{x} \cdot \bar{y} \cdot \bar{z}) \vee (\bar{w} \cdot x \cdot y \cdot z)$ $\vee (w \cdot \bar{x} \cdot y \cdot \bar{z}) = f$
	01			1		
	11					
	10				1	

Figure 2. Karnaugh Map representation of a function

This representation gives a function. Of all the switching possibilities presented by the map the three given above are chosen. The Karnaugh Map form that is used to develop the mathematical model for the controller is shown in Figure 3. In this representation elements x1 x2 form a subset as mentioned in the first paragraph of this section. The inputs, which are the switching combinations of these two elements, form a Boolean algebra. The switching combinations are columns in this map. Switching states are given by each position in the map. For example, switching combination 10 given as a column of x1 x2 has

		x1 x2			
		Input			
		00	01	11	10
Secondary State y1 y2	00	1			
	01			1	
	11				
	10				1

Figure 3. Karnaugh Map representation of switching states

four possible switching states of which 10 of y1 y2 is the term given. A switching state is different from a switching combination in the following way. A switching combination is a representation of a given number of switches each either opened or closed and this combination changes with the opening or closing of one of the elements. Each switching combination may be represented by several switching states dependent upon whether each switch has been opened or closed to form the switching combination being considered. Representation of the switching states enables the controller to operate switches in sequence. The switches y1 and y2 form four secondary assignments used to determine switching states.

The mathematical map of switching states is stored in Boolean matrix form in the switching controller. The mathematical map will be in a form similar to a Switching algebra (3) as distinct from a Boolean algebra. Although a Boolean algebra (4) may be represented in matrix form, in this paper a Switching algebra on which a Boolean matrix multiplication is defined will be used. Basically a Switching algebra has 'group' properties whereas a Boolean algebra does not. Since it is unnecessary to understand the full implication of this to follow the paper the definitions of both algebras will be omitted here but they can be obtained from references 3 and 4.

Each position of a Karnaugh Map gives one possible switching state and it is possible to represent each position as a term in a polynomial. By assuming a rank order of all polynomial terms and then giving a position in a binary word to each polynomial, a prefix 1 or 0 may be used to indicate if the term exists in an equation of a function. The order of terms in a polynomial is different from the order in a Karnaugh Map for convenience in presentation.

As an illustration of this method refer to the switching function given above. In polynomial form this can be written

$$(1 \cdot \bar{w} \cdot \bar{x} \cdot \bar{y} \cdot \bar{z}) \vee (0 \cdot w \cdot \bar{x} \cdot \bar{y} \cdot \bar{z}) \vee (0 \cdot \bar{w} \cdot x \cdot \bar{y} \cdot \bar{z}) \\ \vee (0 \cdot w \cdot x \cdot \bar{y} \cdot \bar{z}) \vee (0 \cdot \bar{w} \cdot \bar{x} \cdot y \cdot z) \vee (\text{etc.}) = f$$

or (1 000 010 000 000 010) (wxyz) = f.

The octal equivalent of this binary representation is

(1 0 2 0 0 2) (wxyz) = f.

Each polynomial is represented as a word or group of words and the process of Boolean matrix multiplication basically gives access to the polynomial required when a change of input occurs.

3. Off Line Calculations and Logic Decisions The mathematical model of the system to be used in the controller must be complete both in the input considered and in the number of switching states possible. Also all constraints, sequences and preferences must be complete. To guarantee this the model is developed by a large off line computer.

Information on each element of the subset is punched on a card. For example, each switch connected to the busbar can have a card. On this card is punched the switch name, say L26, and the constraints relating to it, such as switches which cannot be closed when L26 is closed, as well as switches which must be closed before or after it, etc. Such cards form the input data of the programme.

4. Development of the Mathematical Model The first step in the development of the mathematical model is to form the set of all possible switching combinations of the elements of the subset to be controlled. By the proper selection of elements of the set of switching combinations dangerous and undesirable switching combinations can be avoided. That is, constraint can be built into the model by the elimination of elements of the set. It is impossible for these switching combinations to occur in the substation because they no longer exist in the mathematical model.

The next step is to form a primitive flow table. This consists of forming all the different switching states which give all possible operations of the switches to arrive at a switching combination. Outputs can be assigned to these switching states. It is possible to have different outputs from the same input depending upon different states. In this way it is possible for the controller to perform a switching operation to change from an existing circuit arrangement to a required arrangement and to initiate only the outputs required for this change.

Switching states are considered to be either stable or unstable depending upon the agreement of the input condition with the output performed. If the existing switching state is different from the required switching state, the existing switching state is unstable, but if the existing and required states are the same the existing switching state is stable. Care must be taken that the programme does not introduce redundant stable states.

The next step is to form the flow table. This is done by modifying the primitive flow table. Rows in the primitive flow table may be merged together if the states in each column are not unequal.

For example, the following rows of states can be merged

00	01	11	10
1	2		3
1	2	4	

but

1	2		3
5	2		3

cannot be merged since the two states in column one are unequal. To recognise rows that can be merged the lattice theory of sets is used (6) by considering the switching states to be elements of a set and each row to form a subset which has an ordered association. If each state is considered a least upper bound and if the other elements of the set are considered greatest lower bounds, subsets can be merged to form a lattice between relative elements of each subset under the inequality relation as a group or as a Boolean algebra.

Once all possible mergible rows are found merging can begin. Since the number of choices available to form merged rows is very large a method in which the merging is optimal is required.

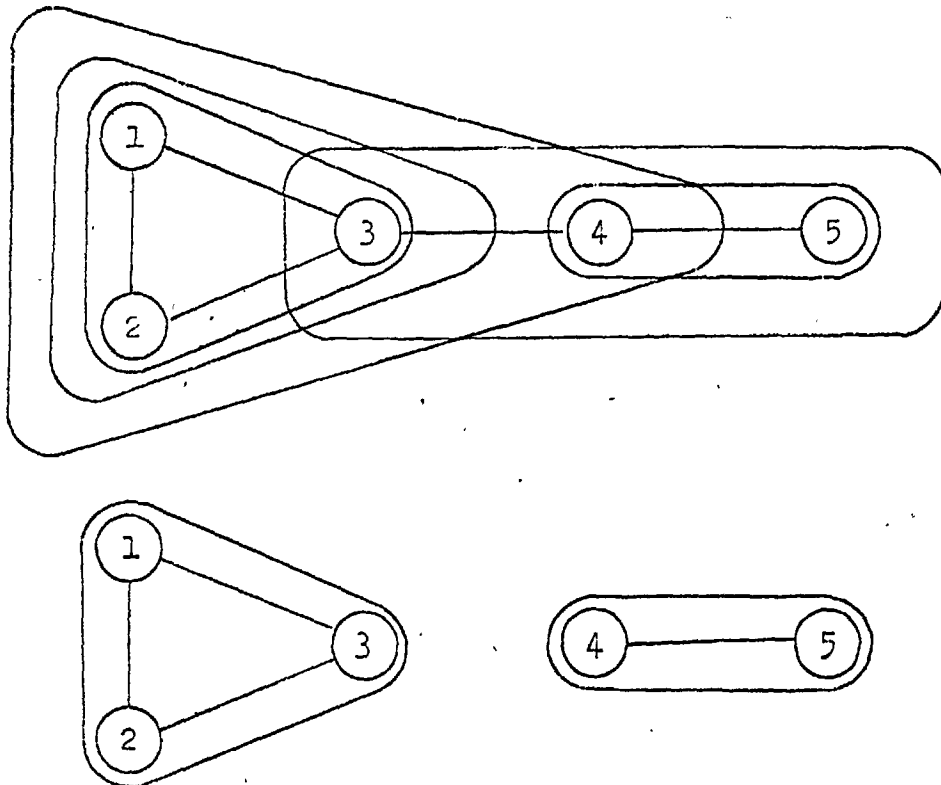


Figure 4. Optimal merging of rows

For this purpose the following method is adopted. Consider each row to form an element of a set and consider each element in all the possible ways it can form a member of a group. The element that is most often the greatest lower bound must repeatedly be eliminated from the elements which least often form the lowest upper bound until the greatest lower bound is empty. The merging is then completed and by this procedure a new set with new elements is formed. Figure 4 is an example of the merging of 5 elements into 2 where elements of the set are rows 1, 2, 3, 4 and 5 and lines joining elements form a group. The loops form least upper bounds which are the elements to be considered for combination to form elements of a new set. The intersection of the loops form the greatest lower bounds. In this example element 3 is most often the greatest lower bound since it occurs most often in the intersection of loops. It must be eliminated from group 3 - 4 which is least often the lowest upper bound. That is, group 3 - 4 is cut by loops three times which is the maximum number of times any group is cut.

The next step is to assign secondary states by giving to all stable states within a row the same secondary state assignment. All unstable states are given the same assignment as their equivalent stable states or as other equivalent unstable states. Figure 5 shows an example of a flow table with letters assigned to each row as the initial stage in the assignment of secondary states. In all the following figures δ signifies that the switching state is stable.

		Input			
		00	01	11	10
Secondary State Assignment	a	1s	2s	4	3
	b	5s	2	9	3s
	c	8	6	4s	7
	d	1	6s	4	
	e	5	6	9s	7
	f	8s	2	10	3
	g	8	6	10s	7

Figure 5. Flow table with initial secondary state assignment

Although it is not always necessary, it is convenient to have the secondary state representation such that all unstable states are adjacent in their binary assignment form to the next desired secondary state. It is undesirable to change secondary states through another stable secondary state since this may result in settling. With the proper choice of secondary state assignment any tendency to settle is avoided. The secondary state assignment

For the example above is shown in Figure 6, which assigns a binary number to each letter representing a row. Shown in Figure 7 is the secondary map, obtained by placing the secondary state assignment in the flow table of Figure 5 as outlined above.

	00	01	11	10
0	a1	a2	d	c
1	f	b	e	g

Figure 6. Karnaugh Map of secondary state assignment

Figure 5 indicates that rows b-c-d-f should be adjacent to row a. This is achieved by allowing row a to have two assignments, as shown in Figure 6, only one of which is stable.

		Input			
		00	01	11	10
a1	000	000	000	010	100
a2	001	000		011	
d	011	001	011	010	
c	010	110	011	010	
g	110	100	010	110	111
e	111	101	011	111	111
b	101	101	100	111	101
f	100	100	000	110	101

Figure 7. Secondary map

An output map is now formed by substituting the desired output in the position where stable states occur in the flow table. Each stable state has a corresponding output which is indicated by the primitive flow table and this is illustrated in Figure 8. The output values shown in each stable state represent some desired output. For example, the value 000 in row 1 column 1 might represent a signal to open 3 switches. Unstable positions in this map are assigned for convenience. An individual binary bit in an intermediate unstable state must not change in the transition between stable states if it is the same in both the stable states. However if the binary bit changes between stable states either representation may be chosen for the intermediate unstable state.

	Input			
	00	01	11	10
000	000	000		
001				
011		010		
010			011	
110			111	
111			001	000
101	010			011
100	110			

Figure 8. Output map for stable states

If switching combinations are called x and secondary states are called y the complete output map is shown in Figure 9.

	Input			
	x1 x2			
y1 y2 y3	00	01	11	10
000	000	000	0--	0--
001	0-0		0--	
011	0-0	010	01-	
010	-1-	01-	011	
110	11-	-1-	111	---
111	0-0	0--	001	000
101	010	0-0	0-1	011
100	110	--0	11-	---

Figure 9. Output map completed

5. Boolean Expressions Boolean expressions may now be formulated for each of the binary bits in the secondary state representation and for each of the output bits in the output map representation. Output maps can also be called Z maps since the Boolean expression of the switching function of the map is often called Z. The secondary and output maps shown above are each a contraction of

three maps Y1, Y2 and Y3 for the secondary map and Z1, Z2 and Z3 for the output map.

The Boolean expressions from the above maps are

$$Y1 = (x1 \cdot \bar{x2}) \vee (x1 \cdot x2 \cdot y1) \vee (y1 \cdot \bar{y2} \cdot y3) \vee (\bar{x1} \cdot \bar{x2} \cdot y1) \\ \vee (\bar{x1} \cdot \bar{x2} \cdot \bar{y1} \cdot y2 \cdot \bar{y3})$$

$$Y2 = (\bar{y1} \cdot y2 \cdot \bar{y3}) \vee (x2 \cdot y2) \vee (x1 \cdot x2) \vee (x1 \cdot y1 \cdot y2)$$

$$Y3 = (y1 \cdot y2 \cdot y3) \vee (\bar{x1} \cdot \bar{x2} \cdot y1 \cdot y3) \vee (\bar{x1} \cdot \bar{y1} \cdot y2 \cdot y3) \\ \vee (\bar{x1} \cdot x2 \cdot \bar{y1} \cdot y2) \vee (x1 \cdot x2 \cdot \bar{y2} \cdot y3) \vee (x1 \cdot \bar{x2} \cdot y1)$$

$$Z1 = (y1 \cdot \bar{y3})$$

$$Z2 = (\bar{x1} \cdot y2) \vee (\bar{x1} \cdot y1) \vee (x2 \cdot \bar{y1} \cdot y2) \vee (x2 \cdot y2 \cdot \bar{y3})$$

$$Z3 = (x1 \cdot x2) \vee (x1 \cdot y1 \cdot \bar{y2} \cdot y3)$$

With each position represented in Karnaugh Map form the prefixes '0' or '1' of each term in the polynomial are determined. The octal form of these polynomials from the above maps is as follows

$$(11533242517) \quad (x1 \ x2 \ y1 \ y2 \ y3) = Y1$$

$$(02175610467) \quad (x1 \ x2 \ y1 \ y2 \ y3) = Y2$$

$$(00411016657) \quad (x1 \ x2 \ y1 \ y2 \ y3) = Y3$$

$$(01703600000) \quad (x1 \ x2 \ y1 \ y2 \ y3) = Z1$$

$$(01256605474) \quad (x1 \ x2 \ y1 \ y2 \ y3) = Z2$$

$$(02104212421) \quad (x1 \ x2 \ y1 \ y2 \ y3) = Z3$$

These solutions can be stored in the controller which would be able to change switch positions when an input signal is received.

6. Characteristics of the Controller The purpose of the stored mathematical model is to enable an appropriate reconnection to be made upon the application of an input signal. This signal may originate from a protective device, a manual operation or another system controller. Its immediate effect on the switching control programme would be to indicate that an unstable state of switching exists and to proceed to the next permissible stable state. This next state is then made to operate the appropriate output device to alter the switching configuration of the substation. In most cases this will involve the operation of one switch, but in the case of a busbar fault, for example, it could involve many switch operations to achieve a satisfactory new switching configuration. It is the purpose of the method which has been outlined to determine acceptable rerouting of essential supplies so that system security is enhanced. It is hoped that this can be achieved by entering such rerouting constraints for each switch on the appropriate card.

Changes in the desired switching of all substations can be made without any change in the physical arrangement of the controller. It is simply reprogrammed. More important, redesign or extension of a substation requires no modification to the controller. Connections between the local controller and equipment for operating switches will be required. Interlocks and interlock relays should not be required since the switches are protected against mal-operation by the mathematical model of the system. All general switching, such as that required for access or maintenance, could be done through the controller. If a switch is open or refuses to close the controller could be made to reroute the supply.

The operating time required depends to a large extent on the speed and size of the controller together with the speed at which the switches can be signalled to operate. Using present supervisory techniques and on-line control computers it should be possible to match the time scales associated with the transients on the power network which limit the speed at which switches can be operated to re-route supplies.

It is hoped that by the development of switching theory as outlined in this paper, the security of power networks can be kept as high as possible by purely automatic means.

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8. References

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