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Citation: Applied Physics Letters **108**, 023302 (2016); doi: 10.1063/1.4939045
View online: http://dx.doi.org/10.1063/1.4939045
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Self-aligned organic field-effect transistors on plastic with picofarad overlap capacitances and megahertz operating frequencies

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(Received 6 August 2015; accepted 15 December 2015; published online 12 January 2016)

Using a combination of nanoimprint lithography, gate-source/drain self-alignment, and gravure and inkjet printing, we fabricate organic field-effect transistors on flexible plastic substrates with gate-source and gate-drain electrode overlap capacitances of $C_{OL} < 1$ pF, equivalent to channel-width normalised capacitances of $C^*_{OL} = 0.15$–$0.23\,\mathrm{pF\,mm^{-1}}$. We compare photopatterned and nanoimprint lithography patterned channels of $L \approx 3.8\,\mu$m and $L \approx 800$ nm, respectively. The reduction in L was found on average to result in order of magnitude greater switching frequencies. Gravure printing the dielectric (versus photo-patterning) was found to yield an order of magnitude lower overlap capacitance $C^*_{OL} = 0.03\,\mathrm{pF\,mm^{-1}}$, at the expense of greater processing variation. Inkjet printed p- and n-type polymeric organic semiconductors were used to fabricate organic-field effect transistors with a peak cutoff frequencies of $f_S = 9.0 \pm 0.3$ MHz at $V_{GS} = 30$ V, and transition frequencies of $f_T = 3.3 \pm 0.2$ MHz at $V_{GS} = 30$ V. © *2016 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution 3.0 Unported License.*
[http://dx.doi.org/10.1063/1.4939045]

Understanding and characterising the switching frequency of organic field-effect transistors (OFETs) is critical for furthering the adoption of printed electronics into practical circuit applications. While high field-effect mobilities are an important figure-of-merit for assessing the performance of OFETs, equally important are the dynamic characteristics of devices. These are a function not only of mobility but also of intrinsic capacitances.[1,2] High capacitances reduce the maximum switching speed that can be achieved in OFETs, limiting their application to low-frequency operation such as display switching (e.g., on the order of 100 Hz). High-frequency radio-frequency identification (HF RFID) is a clear target market for organic electronics, thanks to the potential of printed processes to undercut the high cost of attaching silicon chips to RFID antennas.[3] However, the industry-standard operating frequency of 13.56 MHz far exceeds the switching properties of the majority of reported devices.[4,5] This is in part due to a lack of focus on AC performance—most devices are not characterised in the AC domain—and as a result fabrication techniques such as large-area shadow-masked contacts are used that yield devices with inherently large overlap capacitances. Hence, it is highly important and relevant that alternative fabrication pathways and characterisation techniques are developed that contribute to this missing narrative. Here, we demonstrate the advantages of designing and fabricating OFETs from the ground-up with an explicit focus on switching performance.

In our approach, we focus on combining the best aspects of multiple fabrication technologies. We have previously reported on how ultraviolet nanoimprint lithography (UV-NIL) can be used to pattern sub-micron channel length devices on plastic substrates.[6] Smaller channel lengths reduce the transit time for carriers and hence increase the switching frequency.[7,8] We utilise a self-aligned process, whereby the patterned gate defines the spacing of the source-drain electrodes.[9,10] This minimises the overlap of gate-source and gate-drain electrodes that ultimately limit the device performance. The bottom-gate bottom-contact OFET architecture used here is summarised in Figure 1, indicating the relevant overlap and channel length dimensions.

The ultimate target for organic electronics is a roll-to-roll manufacturing paradigm, yielding low-cost, high throughput manufacturing of circuits, which cannot be achieved with existing silicon-based electronics.[11] Hence, we attempt to use roll-to-roll compatible processing wherever possible. Here, we use gravure printing as an alternative to photolithography to pattern the OFET dielectric layer. We have previously demonstrated how gravure printing allows the high-speed patterning of arrays of dielectric pads on plastic substrates over a large area.[12,13] In this study, a gravure printer (Labratester, Norbert Schläfli Maschinen) was used to pattern a proprietary dielectric formulation (GSID 938109–1, BASF),[14,15] and compared to equivalent photolithographically patterned (MJB3, Süss) layers.

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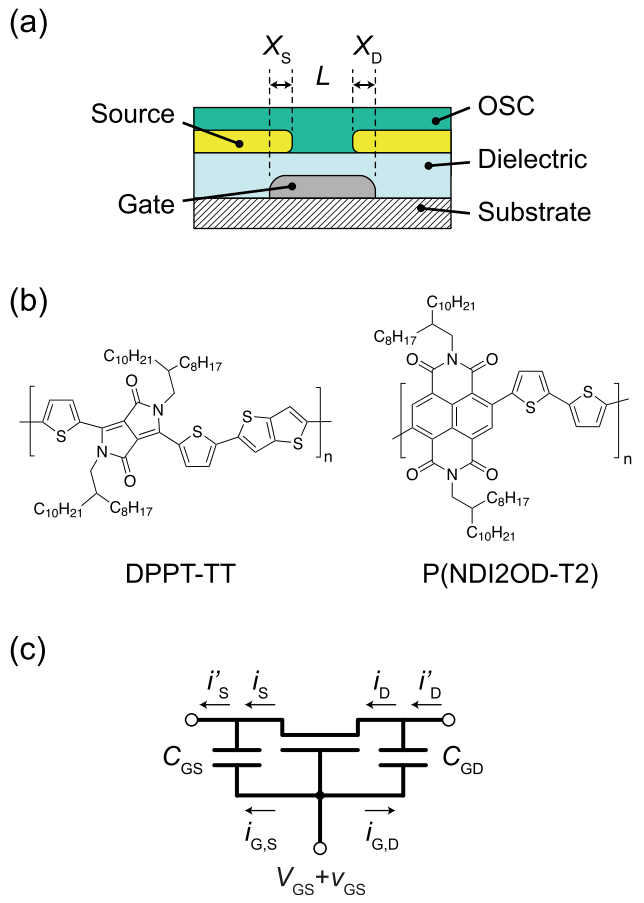


FIG. 1. (a) Illustration of self-aligned OFET architecture, indicating gate-drain overlap X_D, gate-source overlap X_S and effective channel length L. (b) Chemical structures of DPPT-TT and P(NDI2OD-T2). (c) Small signal AC OFET model illustrating gate-drain (C_{GD}) and gate-source (C_{GS}) overlap capacitances and corresponding current flows.

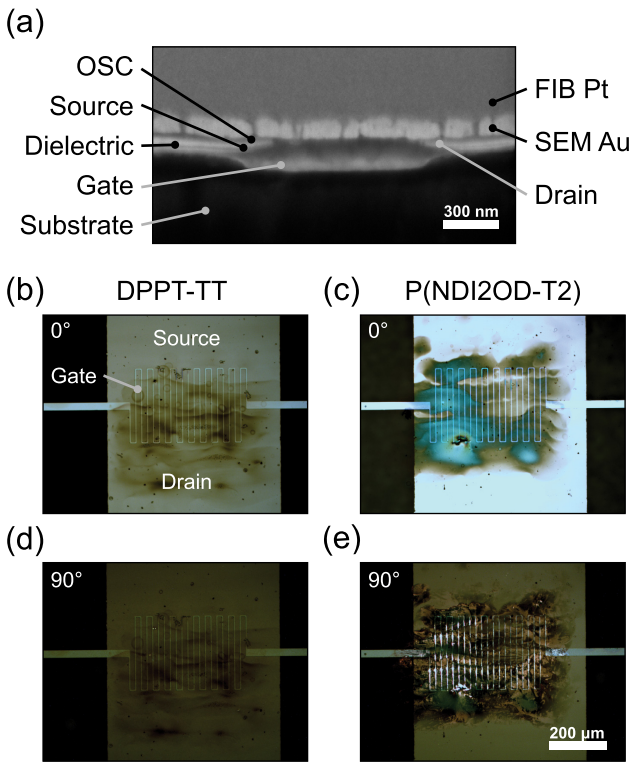


FIG. 2. (a) FIB-SEM micrograph showing cross-section through device with NIL patterned gate and photo-patterned dielectric. (b)–(e) Cross-polarised micrographs of inkjet printed DPPT-TT and P(NDI2OD-T2) on top of devices with PL patterned gate and PL patterned dielectric, with polarisers oriented at 0° and 90°.

Finally, we use inkjet-printing (Dimatix DMP2800, Fujifilm) to deposit two high-performance organic semiconductors,[16] the donor-acceptor copolymers diketopyrrolopyrrole-thieno[3,2-b]thiophene (DPPT-TT),[17] and poly([*N*,*N*′-bis (2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,5′–(2,2′-bithiophene)) (P(NDI2OD-T2)).[18] The chemical structures of both are shown in Figure 1. While both exhibit some ambipolar character, our devices were biased to favour the predominant p-type (DPPT-TT) and n-type (P(NDI2OD-T2)) behaviour of these materials. After printing, the substrates were annealed overnight on a hotplate at 120 °C in a nitrogen glovebox.

Three architecture variants were fabricated in this work: (1) photolithographically (PL) patterned gates, PL patterned dielectric; (2) nanoimprint (NIL) patterned gates, PL patterned dielectric; and (3) NIL patterned gates, gravure printed dielectric. For each architecture, DPPT-TT and P(NDI2OD-T2) OFETs were inkjet printed on adjacent devices on the same substrate, to minimise device-device variation and consistent with the ultimate aim to use these devices in complementary circuits.

Figure 2 shows micrographs of the fabricated devices. The self-aligned architecture was verified using focussed ion-beam scanning electron microscopy (FIB-SEM) (Helios Nanolab, FEI), whereby a cross-section through the substrate is milled by irradiation with gallium ions. Note in order to achieve this, sputtered gold and platinum are deposited onto the region of interest pre-milling, and these layers are also visible in the micrograph. Sub-micron NIL patterned channel lengths of $L \approx 0.7$–$0.8\ \mu$m and PL patterned channel lengths of $L \approx 3.8\ \mu$m were measured. Optical microscopy was used to determine channel widths of $W = 5.4 \pm 0.01\ \mu$m for PL and $W = 5.0 \pm 0.01\ \mu$m for NIL patterned gates (full details shown in Table SI in the supplementary material).[19] Self-aligned overlaps of less than $X_{OL} \leq 210$ nm were measured across all substrates.

Cross-polarised microscopy of inkjet printed semiconductors revealed no evidence of birefringence, suggesting a predominantly amorphous layer of DPPT-TT. This is consistent with previous reports,[17] where significant crystallinity was observed after annealing at 320 °C—much higher than the 120 °C we use to avoid irreversible deformation of our plastic substrate. Interestingly, we did observe evidence of birefringence (and hence possibly preferential crystallinity) in P(NDI2OD-T2), which was correlated with print direction. During printing, the inkjet nozzle was rastered from left-right, top-bottom, as looking at the optical micrographs in Figure 2. This is consistent with previous reports of the influence of long range order on charge transport,[20] and semicrystalline face-on π-stacking in P(NDI2OD-T2).[21,22]

OFETs were biased in the transdiode regime ($V_{DS} = V_{GS}$) and a frequency modulated voltage $v_{GS}(f)$ superimposed on the DC gate bias.[6] By measuring the decoupled AC component of the current at both source and drain electrodes (i'_S, i'_D), we determine the admittance of the OFET in response to an AC signal, as shown in Figure 3. For this, we

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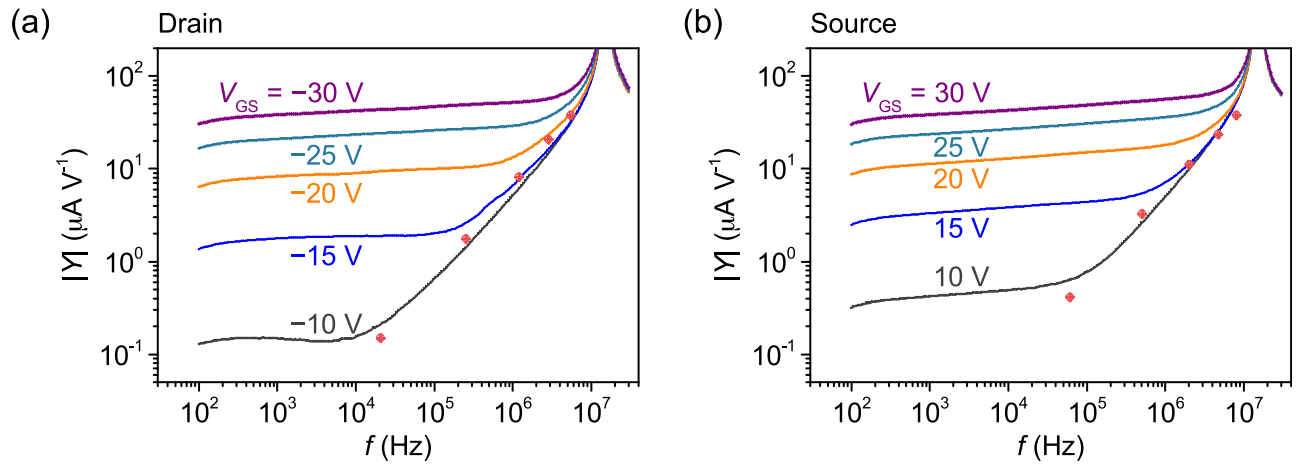


FIG. 3. Admittance measurements of a P(NDI2OD-T2) OFET with NIL patterned gate, and gravure printed dielectric for a range of operating biases $10\,V \le |V_{GS}| \le 30\,V$, where the device is biased in the transdiode regime ($V_{GS} = V_{DS}$). Admittance is measured at the (a) drain and (b) source electrodes. Red circles (•) indicate the extracted cutoff frequencies, f_D and f_S, respectively.

used a network analyser (Agilent 5061B) and a high bandwidth transimpedance amplifier (Femto DHCPA-100) with a gain of $2 \times 10^3\,V\,A^{-1}$ (see Figure S2 in the supplementary material for a schematic of this setup).[19] The transconductance region was fitted between $0.5\,kHz < f < 7.3\,kHz$; the capacitance limited region was fitted between $3.5\,MHz < f < 6.6\,MHz$ (details of these regions are discussed below). Deviations at $f < 500\,Hz$ and $f > 7\,MHz$ are artefacts of the measurement setup.

Figure 3 shows an example of the admittance measurements performed to determine the limit of switching behaviour in our OFETs. In order to interpret these plots, we consider first how the gate-drain (X_D) and gate-source (X_S) overlaps effectively form parallel plate capacitors with the gate dielectric layer. This capacitance is proportional to the length of the overlap, $C_{OL} \propto X_{OL}$. Figure 1(c) illustrates the impact of these capacitors on the small signal AC behaviour of the OFET. As shown in Figure 1(c) we note that the effective drain and source currents (i'_D, i'_S, respectively) comprise both channel and capacitive current contributions. It can be shown that these additional current pathways yield two operating regimes in the OFET, as described by Equation 1 (shown for the drain electrode case and where $j = (-1)^{-0.5}$).[1,6]

$$i'_D = i_D - i_{G,D}, \tag{1a}$$

$$= g_M v_{GS} - j2\pi f C_{GD} v_{GS}, \tag{1b}$$

$$= \begin{cases} g_M v_{GS} & \text{in the limit of small } f \\ j2\pi f C_{GD} v_{GS} & \text{in the limit of large } f. \end{cases} \tag{1c}$$

For low frequency modulation of the gate bias, the effective drain current i'_D is dictated by the channel transconductance g_M. However, at high frequencies, the capacitive current contribution through the gate dielectric increases, ultimately dominating the output. In this regime, the gate modulation of the channel transconductance is dwarfed by parasitic capacitive current flow, and the transistor no longer acts as a current amplifier for the input signal.

Figure 4 summarises the measurements of different architecture and semiconductor variants. Devices show exceptionally low overlap capacitances in the range $C_{OL} < 1.2\,pF$. This equates to channel-width normalised overlap capacitances in the range $(0.15 \pm 0.01)\,pF\,mm^{-1} < C^*_{OL} < (0.23 \pm 0.01)\,pF\,mm^{-1}$, consistent with previous reports for self-aligned inkjet printed

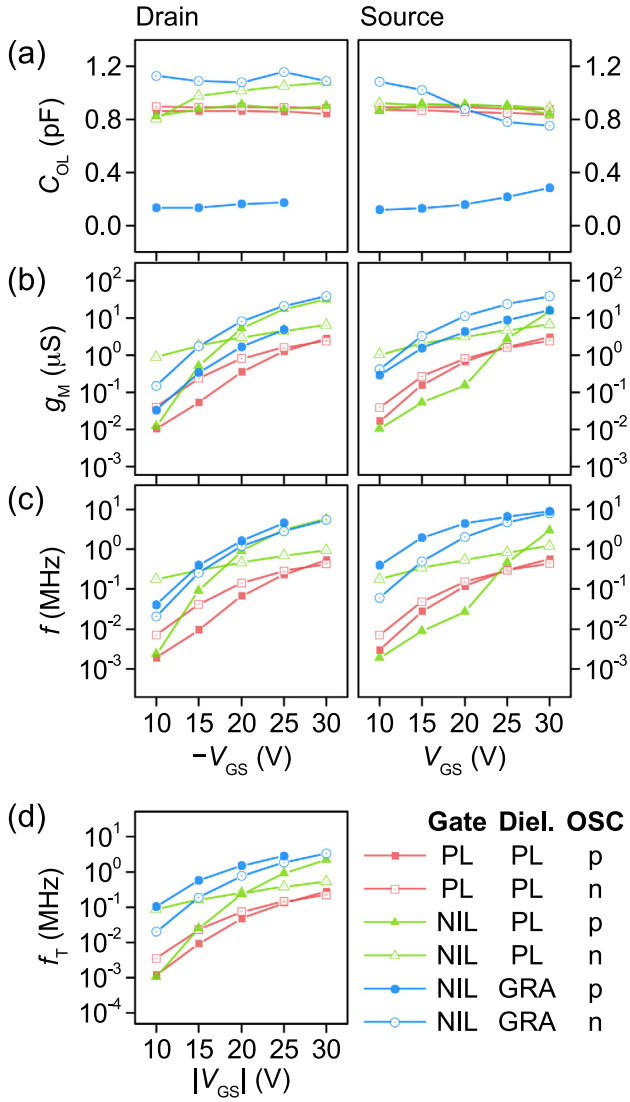


FIG. 4. Summary of AC admittance measurements. Extracted (a) capacitances and (b) transconductances. (c) Calculated cut-off frequencies and (d) transition frequencies.

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architectures.[23] This is achieved irrespective of having a more complex, interdigitated channel design, demonstrating the benefits of our processing approach.

We note that in the case of gravure printed dielectric with p-type semiconductor $C_{OL} < 0.3$ pF was measured, but this was not reflected in the n-type device. In order to determine whether this low value can be expected, we consider how theoretically the total capacitance appearing at either electrode is a combination of both the geometric overlap capacitance and also a charge-induced channel capacitance ($C_{GS} = C_{OL} + C_{CH}$). The latter arises from the accumulation of charge in the channel while the device is on, forming an additional capacitance across the dielectric. The overlap capacitance can be estimated as $C_{OL} \approx WX_{OL}C_i$ yielding $C_{OL\text{-}GRA} \approx 0.24$ pF for the gravure printed dielectric (and $C_{OL\text{-}PL} \approx 0.16$ pF for PL-patterned dielectric). Similarly, in the transdiode regime, the channel contribution at the source can be estimated as $C_{CH\text{-}S} \approx 2/3WLC_i$ as a result of charge accumulation at that electrode. Conversely, the channel contribution at the drain is approximately zero, $C_{CH\text{-}D} \approx 0$, as a result of depletion of the semiconductor in this region.[1] In the case of gravure printed dielectric, and NIL patterned gate, this yields a channel contribution of $C_{CH\text{-}S\text{-}NIL} \approx 0.8$ pF, and hence total theoretical capacitances of $C_{GD} \approx 0.2$ pF and $C_{GS} \approx 1.0$ pF. These approximations suggest that a measurement of 0.3 pF is reasonable. It is most likely that localised modulation of the printed dielectric film thickness is responsible for the variation seen.

Interestingly, however, if we consider the remaining architecture permutations, we would still expect gate-source and gate-drain capacitances to be different, $C_{GS} \neq C_{GD}$. Considering that devices may not be fully operating in the transdiode regime (for example, due to high threshold voltages), the channel capacitance may be better modeled assuming a linear regime contribution $C_{CH} \approx 1/2WLC_i$ appearing at both electrodes.[1] This yields estimates of $C_{GS} = C_{GD} \approx 2.1$ pF (PL gate, PL dielectric), 0.6 pF (NIL gate, PL dielectric), and 1.1 pF (NIL gate, gravure dielectric), which still deviate slightly from the observed values. We conclude that either the channel contribution is more complex than the model used here, or that other sources of variation are present. This is interesting, as we have previously observed the expected $C_{GS} > C_{GD}$ behaviour in our self-aligned architecture, but with a much shorter channel width ($W \approx 120\,\mu$m), different semiconductor, semiconductor film thickness and non-interdigitated electrodes.[6] This suggests the overlap and channel contributions may not scale linearly with W as predicted, or again that other factors are influencing the capacitance.

Despite slight device-device variation in the extracted transconductances in Figure 4(b), a clear systematic shift is observed with the downscaling of the channel length. At $V_{GS} = 25$ V this corresponds to an average order of magnitude increase from $g_{PLG} \approx 1\,\mu$S to $g_{NIL} \approx 10\,\mu$S for both DPPT-TT and P(NDI2OD-T2) devices, consistent with the downscaling of channel length. This also concurs with observed shift in transconductance from the DC characteristics of these devices (see Figure S1 and Tables SII and SIII in the supplementary material).[19]

We also observed that the gate-drain and gate-source capacitances are voltage independent. The voltage-dependency observed in the NIL gate, gravure printed dielectric devices in Figure 4(a) cannot be deemed significant, as it becomes increasingly difficult to fit the capacitive regime in devices approaching 10 MHz (as limited by the coaxial probing used in the measurement setup).

The combination of the measurements in Figures 4(a) and 4(b) yields the drain and source cutoff frequencies shown in Figure 4(c). Equations (2) and (3) show the expressions used, where f_D, f_S, are the drain and source cutoff frequencies, respectively, and g_D and g_S are the transconductance values recorded during each measurement

$$f_D = \frac{g_D}{2\pi C_{GD}}, \tag{2}$$

$$f_S = \frac{g_S}{2\pi C_{GS}}. \tag{3}$$

For high cutoff frequencies, a combination of both high transconductance and low capacitance is desired. Peak performance was measured in devices with NIL-patterned gate, gravure printed dielectric and DPPT-TT and P(NDI2OD-T2) semiconductors, with $f_D = 5.5 \pm 0.2$ MHz, and $f_S = 9.0 \pm 0.3$ MHz at $V_{GS} = 30$ V, respectively (we note that the DPPT-TT device failed under bias during the 30 V drain measurement, hence 25 V is the highest recorded drain value).

While drain and source cutoff frequencies are useful indicators of device performance, the transition frequency (Equation 4) is a more complete and conservative figure of merit for assessing device performance, taking into account both C_{GD} and C_{GS} and giving a better indication of the actual performance achievable in a circuit application

$$f_T = \frac{g_M}{2\pi(C_{GD} + C_{GS})}. \tag{4}$$

Figure 4(d) shows the calculated transition frequencies with a peak value of $f_T = 3.3 \pm 0.2$ MHz at $V_{GS} = 30$ V measured for NIL-patterned gate, gravure printed dielectric and P(NDI2OD-T2) semiconductor. A summary of these results is shown in Table I. For transition frequency estimates an average of g_D and g_S is used to minimise any uncertainty in the two drain and source measurements. A comparison between the directly extracted transconductance compared to estimates derived from DC measurements is shown in Table SIII in the supplementary material.[19] We note that using the

TABLE I. Summary of drain cutoff-, source cutoff-, and transition frequencies for architecture variants. Extracted at $V_{GS} = 30$ V unless otherwise indicated.

Gate	Dielectric	OSC	f_D (MHz)	f_S (MHz)	f_T (MHz)
PL	PL	p	0.5 ± 0.1	0.6 ± 0.1	0.3 ± 0.1
PL	PL	n	0.4 ± 0.1	0.5 ± 0.1	0.2 ± 0.1
NIL	PL	p	5.6 ± 0.2	2.9 ± 0.1	2.2 ± 0.1
NIL	PL	n	0.9 ± 0.1	1.2 ± 0.1	0.5 ± 0.1
NIL	GRA	p	4.6 ± 0.2[a]	9.0 ± 0.3	2.8 ± 0.2[a]
NIL	GRA	n	5.5 ± 0.2	8.0 ± 0.2	3.3 ± 0.2

[a]$V_{GS} = 25$ V.

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value of g_M derived from the transfer characteristics in general underestimates f_T. We attribute this to the relatively low stability of the un-encapsulated devices, which were stored for a period of one day between DC and AC testing, as well as the additional uncertainty introduced by using two independent setups measurements to determine f_T instead of our simpler approach.

We have shown the benefits of combining multiple fabrication technologies to yield multi-megahertz switching OFETs, as well as the importance of considering the AC frequency response of devices. The switching speed of our devices exceeds many state-of-the-art reports for OFETs on plastic.[24,25] Self-alignment yielded very low geometric overlap between gate-drain and gate-source electrodes, as confirmed via FIB-SEM. This was verified by admittance measurements, revealing sub-pF capacitances. These gave exceptionally low channel-width normalised overlap capacitances, despite the fabrication challenge of fabricating large *W/L* ratio devices. Gravure printing (versus photo-patterning) the dielectric yields thinner layers at expense of some device-device variation, yielding an order of magnitude reduction in the overlap capacitance. Deviations from the predicted capacitances at both electrodes suggest that further refinement of the model of overlap and channel capacitance contributions may be required for these devices.

Finally, we note that measured capacitances were invariant with channel length, an indicator of reliable self-aligned processing, and that nanoimprint lithography patterned submicron gates yielded an order of magnitude boost in the observed channel transconductance, directly resulting in higher frequency cutoffs for these devices. Even when considering the more conservative transition frequency, megahertz operating frequencies are obtained.

S.G. Higgins was supported by the Engineering and Physical Sciences Research Council (EPSRC) under Grant No. EP/P505550/1. Parts of this work have also been supported by the European Commission's 7th Framework Programme (FP7/2007-2013) under Grant Agreement No. 247978 (POLARIC). Work performed at IIT has been in part financially supported by the European Research Council (ERC) under the European Union's Horizon 2020 research and innovation programme "HEROIC", grant agreement 638059.

Open data statement: the underlying data supporting this publication is available at: http://dx.doi.org/10.5281/zenodo.35592.

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