

Solution Processed Polymer-Sorted Single Walled Carbon Nanotubes for Plastic Electronics

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Declaration of Originality

I hereby declare that this thesis describes the work carried out within the Department of Physics at Imperial College London between September 2013 and August 2016. Except where specific reference is made to the involvement of others, the work presented here is a product of my own work. The material in this thesis has not been submitted in whole or in part for the award of a degree at this, or any other Institution.

Francesca Bottacchi
August 2016

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Abstract

Single walled carbon nanotubes (SWNTs) have been successfully employed in a wide range of large-area and low-cost optoelectronic devices, such as field-effect transistors (FETs), light emitting diodes, solar cells, and logic circuits. Most common synthesis methods produce a mixture of nanotube diameters that typically results in one-third of the as-synthesized nanotubes being metallic and the remaining two-thirds being semiconducting. These synthesis procedures have a big impact on many optoelectronic applications, where the presence of metallic SWNTs could dramatically degrade device performances. To overcome this problem and sort semiconducting nanotubes from metallic ones, a post-synthetic process called polymer sorting method has been recently developed. If, on the one hand, significant progress has been made to optimize sorting techniques, on the other hand the ability to accurately characterize the residual metallic content in highly pure semiconducting samples remains a major challenge. The primary aim of this thesis is the study of electronic transport processes occurring in polymer-sorted semiconducting SWNT networks. This is achieved with a detailed surface and material characterization, and with the design, fabrication and electrical characterization of field-effect transistors. In the first part of the thesis, the theoretical background of all materials and devices used is given, followed by the description of all procedures, methods, as well as of the fabrication and characterization techniques. In the second part of the thesis, experimental results on SWNT charge transport percolation, flexible field-effect transistors, flexible logic circuits, and alternative processing techniques are discussed. Best achievements include the quantification of residual metallic nanotubes through the application of the percolation model to FETs, the realization of flexible low-voltage SWNT FETs with a mobility of $8.1\text{cm}^2\text{V}^{-1}\text{s}^{-1}$, and the fabrication of flexible low-voltage SWNT complementary inverters with a gain higher than 85V/V . These results clearly demonstrate the potential of solution processed polymer-sorted semiconducting SWNTs for plastic electronics.

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1 Introduction

Single walled carbon nanotubes (SWNTs) have drawn a lot of attention in the last years, owing to their exceptional thermal, mechanical and optoelectronic properties¹ such as bandgap tunability,² high current density,³ excellent thermal conductivity,⁴ ballistic transport,⁵⁻⁸ high infrared absorption,⁹ high mechanical flexibility with an extremely high Young's modulus,¹⁰ and a transmission in the visible range that can be higher than 90%.^{11,12} Moreover, the ability to disperse SWNTs in organic solvents and in water makes solution-based fabrication processes very promising for the realization of large-area and low-cost devices. Because of these remarkable properties, SWNTs have been employed as wiring and interconnect material,¹³ as well as in a wide range of optoelectronic devices, including organic photodetectors,¹⁴ radio frequency antennas (RFID),¹⁵ organic field-effect transistors (OFET),¹⁶⁻²¹ organic solar cells,²² and integrated circuits.²³⁻²⁵ Furthermore, SWNTs show either metallic or semiconducting properties depending on their diameter and chirality, a property with a fundamental importance. However, the drawback of their tremendous potential is that the separation procedure of the semiconducting nanotubes from the metallic ones in an efficient way remains a major challenge.

Most common synthesis methods such as laser ablation,²⁶ arc-discharge,²⁷ chemical vapour deposition (CVD),²⁸⁻³¹ high-pressure carbon monoxide disproportionation (HiPco),³² and plasma torch,³³ produce a mixture of nanotube diameters that typically results in one-third of the as-synthesized SWNTs being metallic and the remaining two-thirds being semiconducting.^{34,35} To overcome this issue, various post-synthetic processing methods have been recently developed, including density gradient ultracentrifugation,³⁶ gel chromatography,³⁷ and polymer sorting,³⁸⁻⁴¹ which make it possible to obtain semiconducting-enriched SWNT dispersions. Among these various processing methods, polymer sorting with polyfluorene-based derivatives is the most effective way of dispersing and sorting semiconducting SWNTs with specific diameters from nanotube bundles, aggregates and any residual metallic nanoparticle. The efficiency of this sorting process is of

crucial importance for all optoelectronic applications in general, and especially for microelectronics, where the presence of metallic nanoparticles in a device, even at concentrations of few parts per thousand, could dramatically degrade its performance.^{17,42} Even though on the one hand significant progress has been made to optimize sorting and enrichment techniques, on the other hand the ability to accurately characterize the residual metallic content in highly pure semiconducting SWNTs samples still remains a major challenge. Raman spectroscopy is one of the more common method to assess metallic content.^{43,44} However, the metallic content can be also accurately determined by electrical characterization of OFETs,⁴⁵ without having to use a sophisticated Raman spectroscopy setup.

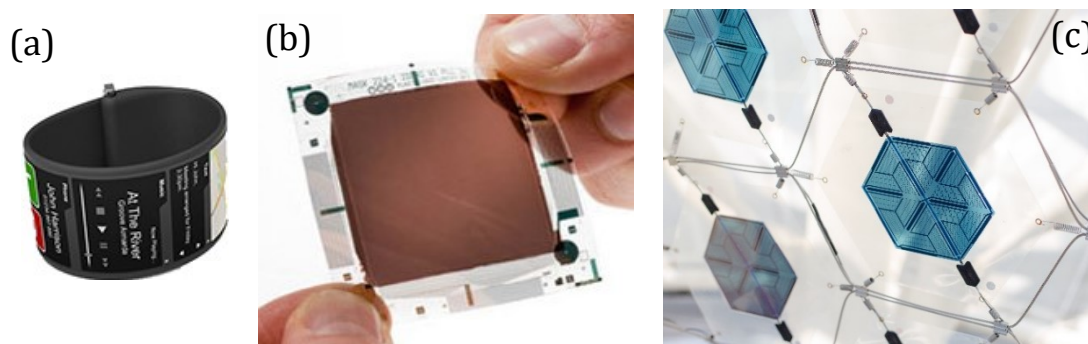


Figure 1: (a) Flexible active matrix LED display based on organic transistors (Photography courtesy of Flexenable Ltd).⁴⁶ (b) Flexible X-ray image sensor (Photography courtesy of Flexenable Ltd).⁴⁷ (c) Flexible organic solar cell module (Photography courtesy of Belectric OPV GmbH).⁴⁸

Using such solution-based approach, several deposition techniques, such as drop casting,¹⁶ spin-coating,^{21,23,45} dip coating,²⁵ inkjet printing,⁴⁹ blade coating,¹⁸ self-assembly,¹⁷ and gravure printing,⁵⁰ have proven suitable for cost efficient, room temperature deposition of SWNT thin-films into microelectronic devices. Moreover, the high mechanical flexibility combined with high charge carrier mobility and cost efficient solution-based manufacturing processes at room temperature, pave the way for flexible and wearable displays and electronics, emerging fields in which silicon-based devices cannot be used due to their very poor mechanical properties. Today, flexible displays^{46,47} and solar cells⁴⁸ based on organic semiconducting materials are already commercially available, as shown in Figure 1.

The main figure of merit in transistor operation is the charge carrier mobility. The minimum requirement for a transistor to drive an organic light-emitting diode (OLED) in an active matrix display is $\mu > 5\text{cm}^2/\text{Vs}$.⁵¹ Often used benchmark for organic materials are amorphous silicon, with a mobility of $0.5\text{-}1\text{cm}^2/\text{Vs}$, polycrystalline silicon, with a mobility around $100\text{cm}^2/\text{Vs}$, and semiconducting metal oxides, for which an electron mobility well above $10\text{cm}^2/\text{Vs}$ is commonly reported nowadays.⁵²⁻⁵⁵

Table 1: Key parameters of thin-film deposition techniques for emerging electronic materials.^{17,20,51-55}

Material	Deposition Technique	Mobility (cm^2/Vs)	Spatial Uniformity	Cost
α -Si	Chemical Vapour Deposition	< 1	High	Low
Poly-Si	Excimer Laser	100	Low	High
Semiconducting Metal Oxides	Sputtering, spray-coating or solution deposition	10-100	High	Medium
Organic Semiconductors	Printing, solution deposition or vacuum evaporation	1-10	Low	Low
Carbon Nanotubes	Printing, spray-coating or solution deposition	< 50	Low	Low

Table 1 summarizes the key parameters of several thin-film deposition techniques for emerging electronic materials.

1.1 Thesis Aim and Outline

This project is part of the Marie Curie Network called POCAONTAS (“Polymer – Carbon Nanotubes Active Systems for Photovoltaics”), whose aim is to implement solution-processed single walled carbon nanotubes inside photovoltaic devices. The primary aim of this thesis is to study the electronic transport processes that occur in polymer-sorted single walled carbon nanotube network thin-films. This is achieved with a detailed surface and material characterization, and with the design, fabrication and electrical characterization of field-effect transistors as well as logic circuits. Furthermore, additional purpose of this thesis is to demonstrate that single walled carbon nanotubes can be a valid new material for microelectronics, even though a lot of work in material processing still needs to be done for real commercial applications.

This work is organized in four main chapters, followed by Bibliography and Appendix. In the Theoretical Background chapter, structural and electronic properties of single walled carbon nanotubes, conjugated polymers, small molecules, and semiconducting metal oxides are explained. The organic field-effect transistor (OFET), the ambipolar OFET and logic circuits are also fully described from an electrical and device physics perspective. Then, the procedures, the fabrication and characterization techniques, as well as any other experimental method involved in this project, are explained in the Experimental Method chapter. Afterwards, all the experimental results obtained during the PhD are presented and discussed in the Experimental Results and Discussion chapter. This chapter comprises of four sections, where results on SWNT network charge transport percolation, SWNT flexible field-effect transistors, SWNT flexible logic circuits, as well as alternative processing techniques are discussed. Finally, the Conclusions and Outlook of the thesis are drawn.

2 Theoretical Background

In this chapter, some fundamental theoretical aspects related to materials and devices used for the results are introduced. Initially, structural and electronic properties of single walled carbon nanotubes, conjugated polymers, small molecules, and metal oxides are described. Later, the operating principles of devices such as the organic field-effect transistor (OFET), the ambipolar OFET and logic circuits are explained.

2.1 Single Walled Carbon Nanotubes

2.1.1 Carbon Allotropes

A free carbon atom has the electronic structure $1s^2 2s^2 2p^2$ and, in order to form covalent bonds, one of the 2s electrons needs to be promoted to the 2p orbital, and the orbitals can then hybridize in one of these three possible ways: sp^3 , sp^2 , sp . The sp^3 electronic configuration is characteristic of the diamond structure, where the carbon atoms form bonds with all four nearest neighbours in a tetrahedral lattice. The sp^2 electronic configuration results instead in the formation of graphite, where the carbon atoms form planar bonds in a hexagonal honeycomb lattice with three nearest neighbours' orbitals at 120° to each other, with the remaining orbital having a p_z configuration at 90° to this plane. In this structure, the sp^2 orbitals form the strong σ bonds between carbon atoms in the graphitic plane, while the p_z or π orbital provides the weak van der Waals bond between the planes. Because of the strong in-plane bonds and the very weak out-of-plane bonds, graphite can be considered as a layered structure, in which the basic unit is one layer, also called graphene. A third form of carbon is fullerene C_{60} , a molecular cage made of 60 identical carbon atoms bonded in an icosahedral structure based on twelve pentagons and twenty hexagons. Other fullerenes with a bigger cage also exist, e.g. C_{70} , where the molecular cage is made up of 70 identical carbon atoms. Because each of the carbon atoms in the fullerene are joined to three neighbours, the bonding is essentially sp^2 , although there is a small amount of sp^3 character due to the curvature of the structure. Finally, an example of sp hybridization is acetylene, a hydrocarbon in which each carbon

atom in the 2s orbital hybridizes with one carbon atom in the 2p orbital, thus forming a sp hybrid, while the other two 2p orbitals do not hybridize. The two ends of both the sp hybrid orbitals overlap to form strong σ bond, while the two 2p orbitals form a pair of weaker π bonds. Bonds in carbon nanoparticles and carbon nanotubes are also primarily sp², although there may be some sp³ character in regions of high curvature. Figure 2 shows eight possible molecular configurations of carbon allotropes.

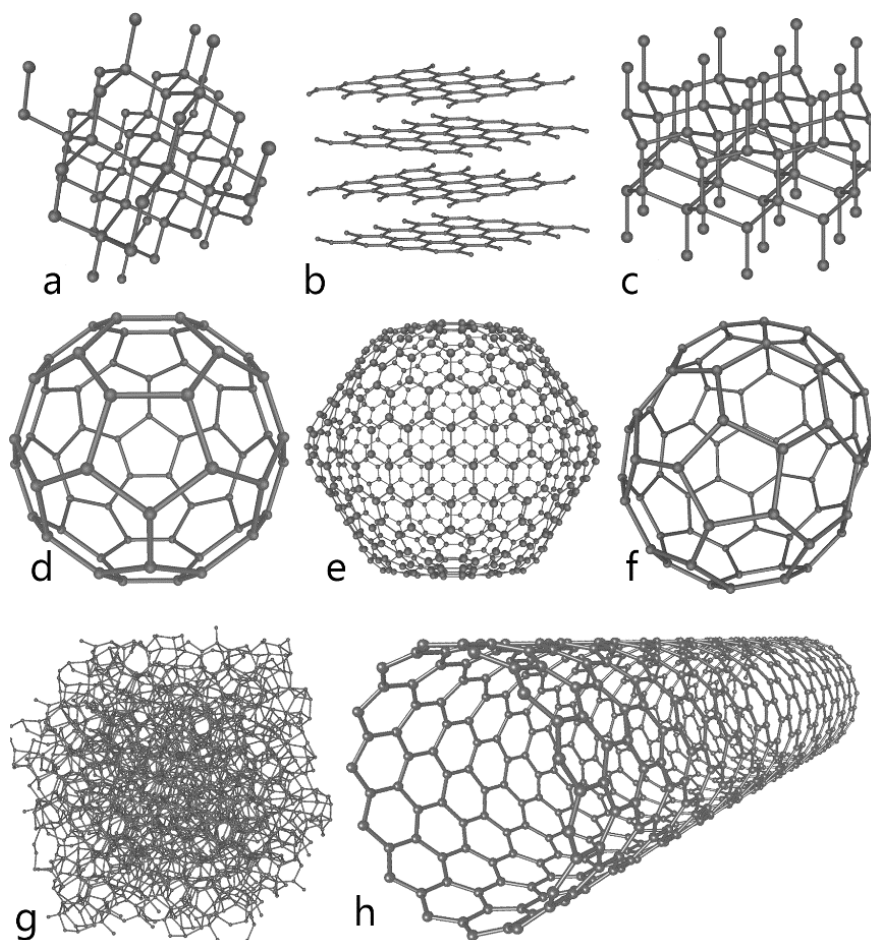


Figure 2: Eight molecular configurations of carbon allotropes: (a) Diamond, (b) Graphite, (c) Lonsdaleite, (d) Fullerene C₆₀, (e) Fullerene C₅₄₀, (f) Fullerene C₇₀, (g) Amorphous Carbon, (h) Single Walled Carbon Nanotube.⁵⁶

In 1991 multi walled carbon nanotubes (MWNTs) were discovered,⁵⁷ which are quasi-1D structures with the nested carbon tubes only weakly coupled. A few years later, single walled carbon nanotubes (SWNTs) were also discovered,⁵⁸ and since then carbon nanotubes have been dedicated a lot of attention.

2.1.2 Crystalline Structure

Single walled carbon nanotubes are best described as a seamless cylindrical hollow fiber made of a single sheet of pure graphite, where each carbon atom is bonded to its three nearest neighbours in such a way that a certain curvature is achieved. The physical properties of SWNTs can therefore be derived from the structure of graphene rolled up into a seamless cylinder with a specific rolling angle θ . The atomic structure of a SWNT is specified by the chiral vector $\mathbf{C}_h$, which is defined by the two indices (n, m) . The chiral vector $\mathbf{C}_h$ is defined as:

$$\mathbf{C}_h = n\mathbf{a}_1 + m\mathbf{a}_2 \quad (1)$$

where $\mathbf{a}_1$ and $\mathbf{a}_2$ are the unit vectors of the hexagonal honeycomb lattice, with $|\mathbf{a}_1| = |\mathbf{a}_2| = 0.246\text{nm}$. The vector $\mathbf{C}_h$ connects two equivalent sites on the graphene sheet, where carbon atoms are located at each vertex of the honeycomb lattice.

The chirality of a carbon nanotube plays a significant role on its physical properties because, depending on the chiral index (n, m) , a carbon nanotube can have semiconducting or metallic properties.

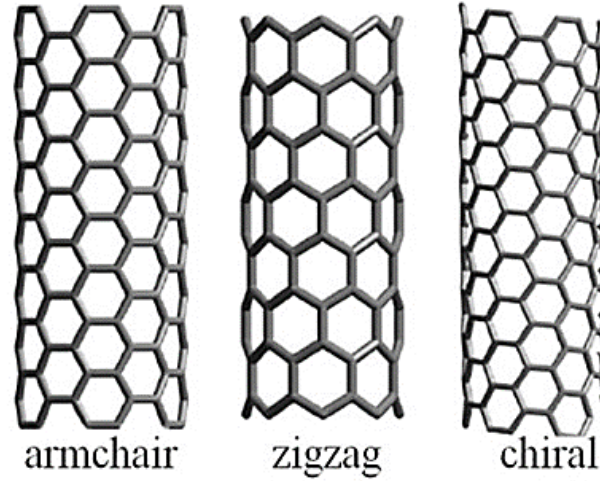


Figure 3: Armchair, zigzag and chiral nanotube structures.⁵⁹

There are only two species of SWNTs that have mirror symmetry, and these are called: zigzag nanotubes if $(n, 0)$ and armchair nanotubes if (n, n) . All the other nanotubes are called chiral nanotubes, denoted by the rolling angle θ (also called

chiral angle), and they have axial chiral symmetry with the chemical bonds not parallel to the nanotube axis. The zigzag ($\theta = 0^\circ$), armchair ($\theta = 30^\circ$) and chiral ($0^\circ \leq |\theta| \leq 30^\circ$) nanotubes are shown in Figure 3. The chiral angle θ is given by

$$\theta = \tan^{-1} \left[\frac{\sqrt{3}m}{(m+2n)} \right], \quad (2)$$

while the diameter d of a (n, m) nanotube is defined as

$$d = \frac{|\mathbf{C}_h|}{\pi} = \frac{\sqrt{3}a_{C-C}\sqrt{(n^2 + mn + m^2)}}{\pi}, \quad (3)$$

where $\sqrt{3}a_{C-C} = |\mathbf{a}_1| = |\mathbf{a}_2| = 0.246\text{nm}$, with $a_{C-C} = 0.142\text{nm}$ the nearest-neighbour C-C distance in graphite. According to equation (3), for a (7,5) tubes $d = 0.817\text{nm}$.

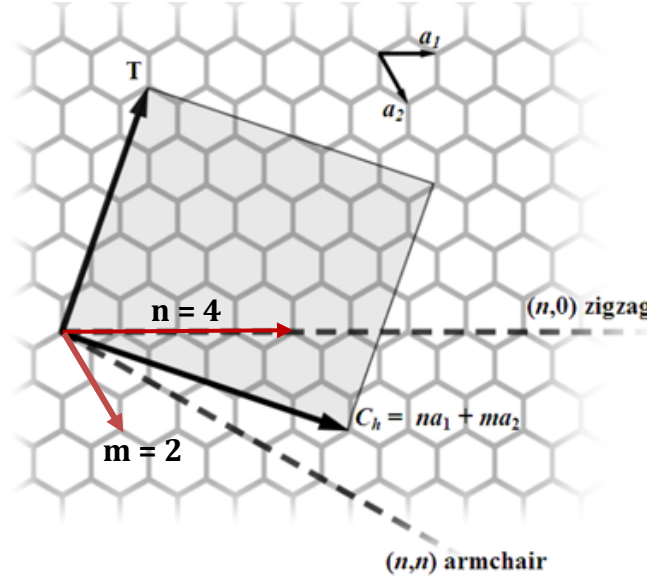


Figure 4: The unrolled honeycomb lattice of a nanotube. $\mathbf{C}_h$ is the chiral vector, $\mathbf{T}$ is the translational vector, and $\mathbf{a}_1$ and $\mathbf{a}_2$ are the unit vectors of the hexagonal honeycomb lattice.

Figure 4 shows the unrolled honeycomb lattice with all the related vectors. $\mathbf{T}$ is the translational vector, which is the length of the real space unit cell along the nanotube axis direction and $|\mathbf{T}| = a$ for the armchair tube, $|\mathbf{T}| = \sqrt{3}a$ for the zigzag tube, and $|\mathbf{T}| = \frac{\sqrt{3}|\mathbf{C}_h|}{d_R} = \frac{\sqrt{3}d_t\pi}{d_R}$ for any general (n, m) chiral tube, where d_R is the greatest common divisor between $(2n + m)$ and $(2m + n)$.⁶⁰

2.1.3 Electronic Structure and Density of States

The 1D electronic density of states (DOS) is obtained from the energy dispersion relations of SWNTs, which are obtained by zone-folding of the 2D graphene energy dispersion relations. Curvature-induced strains in the sp^2 structure of SWNTs with diameters above 1nm do not affect much the electronic properties but, of course the approximation improves at larger diameters. Hereafter, π and π^* are the valence and the conduction energy bands respectively, while σ and σ^* are deep energy states, as they are away from the Fermi energy E_F by more than 10eV. Figure 5 shows the electronic energy dispersion relations of graphene, plotted as a function of the two-dimensional wave vector $\mathbf{k}$ in the hexagonal Brillouin zone.

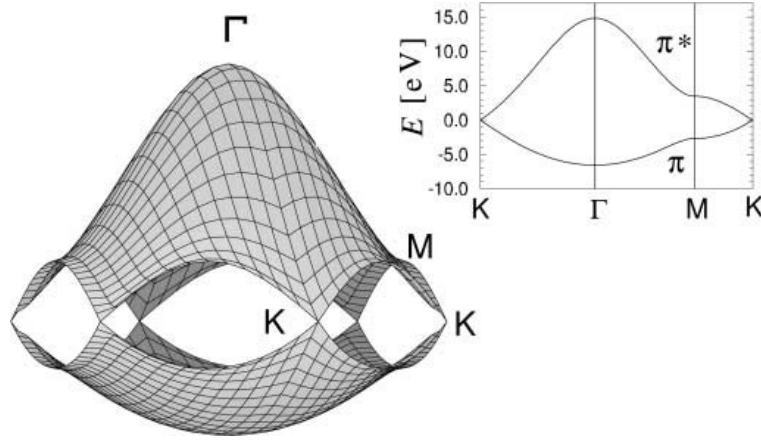


Figure 5: Energy dispersion relations for the π and π^* bands in graphene. The inset shows the energy dispersion along the high symmetry line passing through Γ , M, and K points, where π and π^* bands are degenerate. (Reproduced with permission from Saito et al., *Phys. Rev. B* **61**, 2981–2990 (2000). Copyright © 2000 by the American Physical Society).⁶¹

At the K points in the hexagonal Brillouin zone, which correspond to the Fermi energy, the valence π and conduction π^* bands are degenerate and the energy dispersion has a linear dependence on k . If we assume a linear k approximation, the linear dispersion relations of graphene become the following:^{60,61}

$$E_{2D}^{\pm}(k) = \pm \frac{\sqrt{3}}{2} \beta k a = \pm \frac{3}{2} \beta k a_{C-C}, \quad (4)$$

where $\beta > 0$ is the nearest-neighbour transfer integral. From equation (4), the 1D energy dispersion relations of SWNTs can be expressed as:

$$E_{\mu}^{\pm} = E_{2D}^{\pm} \left(k \frac{\mathbf{K}_2}{|\mathbf{K}_2|} + \mu \mathbf{K}_1 \right), \quad \left(-\frac{\pi}{|\mathbf{T}|} < k < \frac{\pi}{|\mathbf{T}|}, \quad \mu = 1, \dots, N \right), \quad (5)$$

where k is a 1D wave vector along the nanotube axis, N indicates the number of hexagons in the graphene honeycomb lattice that lie within the carbon nanotube unit cell, $\mathbf{K}_1$ represents a discrete unit wave vector along the nanotube circumferential direction, and $\mathbf{K}_2$ represents a reciprocal lattice vector along the nanotube axis direction. $\mathbf{K}_1$ and $\mathbf{K}_2$ also define the separation between two of these adjacent lines and their length. The N pairs of energy dispersion curves $E_{\mu}^{\pm}$ obtained from Equation (5) correspond to the cross sections of the energy dispersion surface shown in Figure 5.

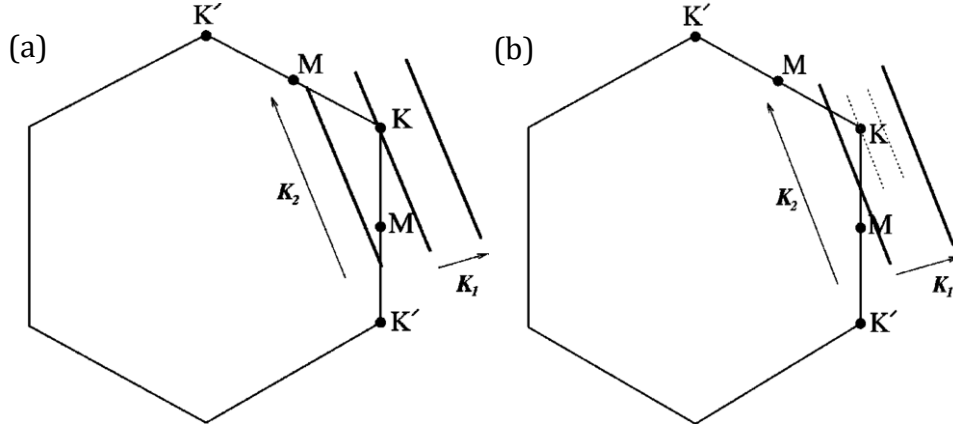


Figure 6: The wave vector k for carbon nanotubes is shown in the 2D Brillouin zone of graphene as bold cutting lines for (a) metallic and (b) semiconducting carbon nanotubes. For metallic nanotubes, the cutting line always intersects a K point at the Fermi energy of graphene, while for semiconducting nanotubes, the K point always remains one-third of the distance between two cutting lines. (Reproduced with permission from Saito et al., *Phys. Rev. B* **61**, 2981–2990 (2000). Copyright © 2000 by the American Physical Society).⁶¹

Figure 6 shows several cutting lines near one of the K points for a metallic and a semiconducting nanotube. If one of these cutting lines passes through a K point (Figure 6(a)), the valence and conduction energy bands are degenerate at the Fermi energy (inset in Figure 5), consequently the 1D energy bands have a zero energy gap, and thus the nanotube is metallic. However, when the K point is located between two cutting lines (Figure 6(b)), the nanotube is a semiconductor with a finite energy gap.⁶⁰ A specific rule states that the nanotube is metallic when $n - m =$

$3q$, and is semiconducting when $n - m \neq 3q$, with q an integer. From this rule it follows that all armchair tubes are metallic, while approximately one-third of chiral and zigzag nanotubes are metallic, and the remaining two-thirds are semiconductors.^{34,35}

The 1D density of states (DOS) of SWNTs has the following energy dependence:

$$\text{DOS}(E) \propto \left| \frac{dE_{\mu}^{\pm}(k)}{dk} \right|^{-1}. \quad (6)$$

When the energy dispersion relations $E_{\mu}^{\pm}(k)$ are linear near the Fermi energy, the DOS is constant; instead, when $E_{\mu}^{\pm}(k)$ become flat, the DOS becomes large and van Hove singularities (vHs) appear, as shown in Figure 7, which are extremely important for the determination of many optical properties of carbon nanotubes.

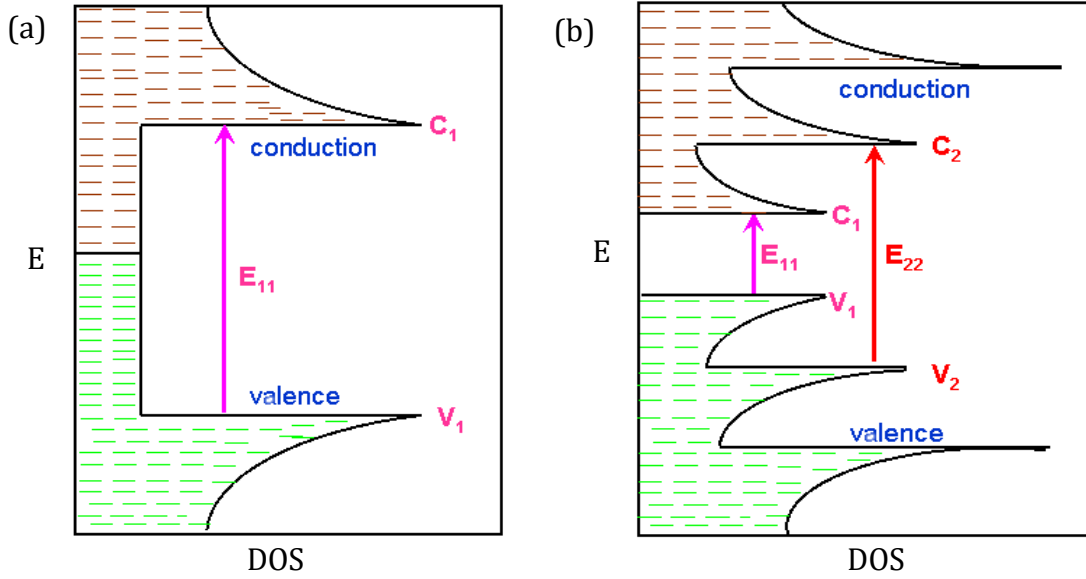


Figure 7: Density of states for (a) metallic and (b) semiconducting nanotubes.⁶²

For nanotubes with a very small diameter $d < 2\text{nm}$, the linear approximation can no longer be applied, and the equi-energy lines near the K points become a triangle for large k values. This distortion is known as the trigonal warping effect, and it produces a characteristic splitting of the DOS peaks for the metallic nanotubes. In general, this effect can be considered only for metallic zigzag nanotubes with diameters $d < 2\text{nm}$.^{60,61}

2.1.4 Ballistic Conduction

SWNTs can support ballistic conduction when electrical resistivity, caused by scattering, is negligible. In general, resistivity exists because an electron moving inside a medium is scattered by impurities, boundaries, defects, and phonons. For a given medium, each moving electron is associated with a mean free path (λ_{MFP}), which is the average length that an electron can freely travel before clashing in a collision that changes its momentum. The mean free path can be increased by lowering the temperature of a crystal or by reducing the number of impurities. Ballistic transport is a coherent motion of electrons that is observed when the electron's mean free path is much longer than the path (L) in the medium through which the electron is travelling ($\lambda_{\text{MFP}} \geq L$). In terms of scattering mechanisms, optical phonons emission normally dominates in SWNTs but, for a low scattering rate, λ_{MFP} as high as $1 \mu\text{m}$ can be achieved.⁷

Due to their 1D nature, electrical conduction in SWNTs is quantized and the number of allowed electronic states is limited. The nanotube thus behaves as a quantum wire and charge carriers are transmitted through discrete conduction channels. As a result, the electrons do not encounter any resistance and no energy is dissipated during conduction. Assuming no scattering events, the conductance of a 1D system is given by $G = G_0 NT$, where T is the probability that an electron is transmitted along the channel, N is the number of modes in the transmission channel with spin included, and G_0 is the quantum conductance defined as:

$$G_0 = 2e^2/h = (12.9 k\Omega)^{-1}. \quad (7)$$

Perfect contacts with no back-scattering along the channel result in a transmission probability $T = 1$, thus the ballistic conductance for a SWNT becomes $G = 2G_0 = (6.45 k\Omega)^{-1}$.^{5,6,8} In the non-ideal situation where contact resistance is present, T must be replaced by the sum of the transmission probabilities for each conduction channel. Hence, low contact resistance is a prerequisite for investigating ballistic conduction in SWNTs. If the contacts are ideal however, T can still be reduced by back-scattering events along the carbon nanotube. Contact resistance and scattering events are the two major mechanisms ruining ballistic conduction.

2.1.5 Synthesis and Processing Methods

Various techniques have been developed to produce single walled carbon nanotubes in substantial quantities, including arc-discharge, laser ablation, plasma torch, chemical vapour deposition (CVD), and high-pressure carbon monoxide disproportionation (HiPco). Most of these techniques take place in vacuum or with a process gas.

During the process of arc-discharge,²⁷ the carbon contained in the negative electrode sublimates because of the high-discharge temperatures. The yield for this technique is up to 30% by weight, and it produces up to 50 μm long single and multi-walled carbon nanotubes with only few structural defects. In laser ablation,²⁶ a graphite target is vaporized by a pulsed laser in a high-temperature reactor while an inert gas is drained into the chamber. As the vaporized carbon condenses, carbon nanotubes grow on the cold surfaces of the reactor. The laser ablation technique yields around 70% and it produces primarily single walled carbon nanotubes whose diameter is determined by the reaction temperature. However, this technique is more expensive than other available methods. Another method is plasma torch,³³ whose aim is to reproduce the arc-discharge and laser ablation approaches but instead of graphite vapours, a gas containing carbon is used to supply the carbon necessary for the production of SWNTs. By doing so, the growth of SWNT is more efficient, continuous and cost-effective. The fumes created by the flame contain SWNTs, metallic residues, carbon nanoparticles, and amorphous carbon.

The most common synthesis method of carbon nanotubes is CVD,³⁰ during which a substrate is covered with a layer of metal catalyst nanoparticles, most commonly nickel, cobalt or iron. The nanotubes diameter is related to the size of the metal nanoparticles, which can be controlled by patterning the surface. To start the growth, the substrate is heated to about 700 °C and two gases are mixed into the reactor: a process gas and a carbon-containing gas. The carbon-containing gas is decomposed at the catalyst nanoparticle surface, and the carbon is then transported to the edges of the nanoparticles, where it forms the nanotubes with a random orientation. One issue in this synthesis is the removal of the metal catalyst, usually done with an acid treatment, which sometimes could damage the original of the

carbon nanotube structure, inducing structural defects. If a plasma is generated during the growth (plasma-enhanced chemical vapour deposition),²⁸ carbon nanotubes will follow the direction of the electric field and vertically-aligned carbon nanotubes can be synthesized.

Finally, in the HiPco process³², the disproportionation of CO into CO₂ and carbon nanotubes growth ($\text{CO} + \text{CO} \rightarrow \text{C}_{(\text{s})} + \text{CO}_2$) occurs on unsupported iron catalyst nanoparticles formed in situ by the gas-phase decomposition of iron pentacarbonyl precursor. Depending on the conditions and geometry of the reactor, both the yield of SWNT material and the diameter can vary over a wide range, but SWNTs with diameters ranging from 0.7 nm to 1.2 nm are usually obtained with this technique.

The main problem of these synthesis processes is that the diameter of the nanotube, and consequently its electronic properties, strongly depends on the size of the metal nanoparticle catalyst. By exploiting CO disproportionation occurring at 750 °C with only cobalt and molybdenum nanoparticles in a precise ratio, a unique catalytic method called CoMoCat has been developed.^{29,31} This synthesis technique produces SWNTs of high quality with a remarkably narrow distribution of diameters, dominated by the two semiconducting nanotube species with chirality (6,5) and (7,5).

Once carbon nanotubes are synthesised, in order to be efficiently used in transistors, solar cells, and other optoelectronic devices, they need to go through a post-synthetic process, in order to remove the metallic catalyst residues and separate metallic tubes from the semiconducting ones. This can be done with techniques such as density gradient ultracentrifugation, gel chromatography, and polymer sorting, which make it possible to obtain semiconducting-enriched SWNT dispersions.

Density gradient ultracentrifugation³⁶ is a scalable and effective technique that exploits differences in the buoyant densities (mass per volume) among SWNTs with different diameters. In response to the centripetal force applied during ultracentrifugation, carbon nanotubes sediment toward their respective buoyant densities and spatially separate by diameter, as shown in Figure 8.

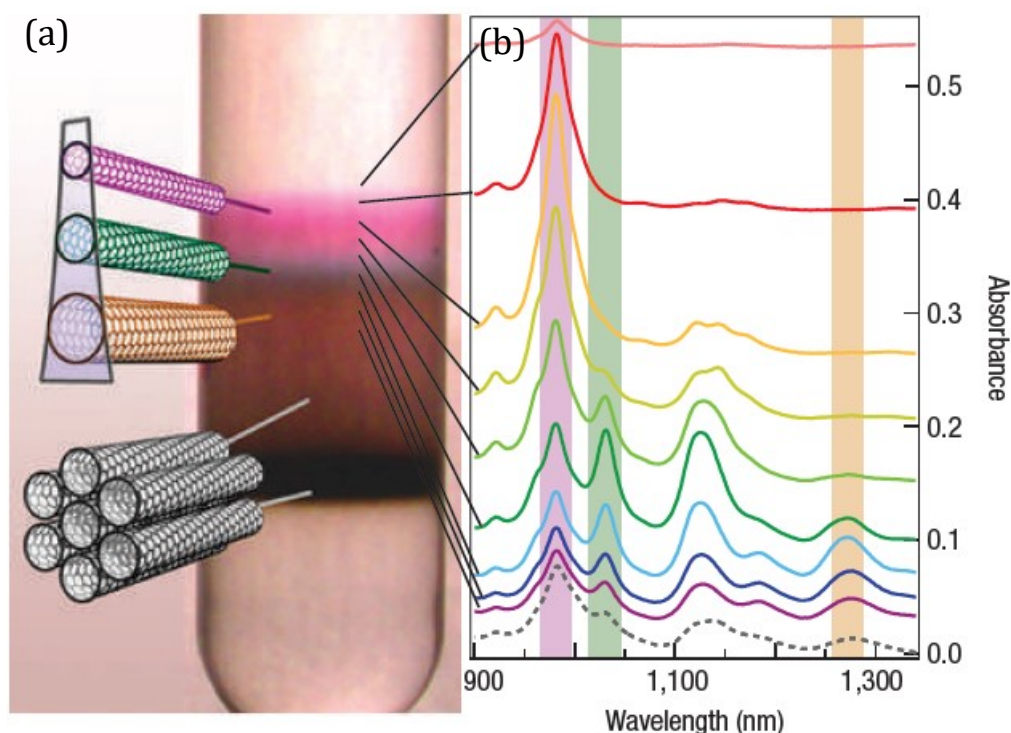


Figure 8: (a) Photograph and (b) optical absorbance spectra after density gradient ultracentrifugation. The separation is clear from the formation of coloured bands of isolated nanotubes sorted by diameter and bandgap. Bundles, aggregates and insoluble material sediment down in the gradient. (Reprinted by permission from Macmillan Publishers Ltd: Nature Nanotechnology,³⁶ Copyright © 2006).

During gel chromatography,³⁷ a gel is used as the medium and several gel columns are connected vertically in series to achieve large-scale diameter separation. By overloading a SWNT dispersion in a sodium dodecyl sulphate (SDS) aqueous solution onto the top column, the selective adsorption of carbon nanotubes with different diameters in the various columns, based on the interaction strengths with the gel, is achieved. Metallic nanotubes exhibit the lowest interaction with the gel and so they are collected as unbound nanotubes and separated from the semiconducting ones.

Another sorting technique is the so-called polymer sorting method.^{38–41} Certain polymers, especially polyfluorene-based derivatives (PFO), are extremely effective in sorting and dispersing SWNTs with specific diameters, thanks to the interaction between the nanotube and the side-chains attached to the polymer backbone. Although the exact selection mechanism is still debated, the type and number of side-chains, the molecular weight of the dispersing polymer, the concentration as

well as the viscosity of the solvent all affect the polymers selectivity toward semiconducting SWNTs.⁶³ A drawback of this method is that the removal of the polymer afterwards, which is essential to achieve good device performance, is very challenging, and very frequently the final dispersion is used for device fabrication without a proper polymer filtration.

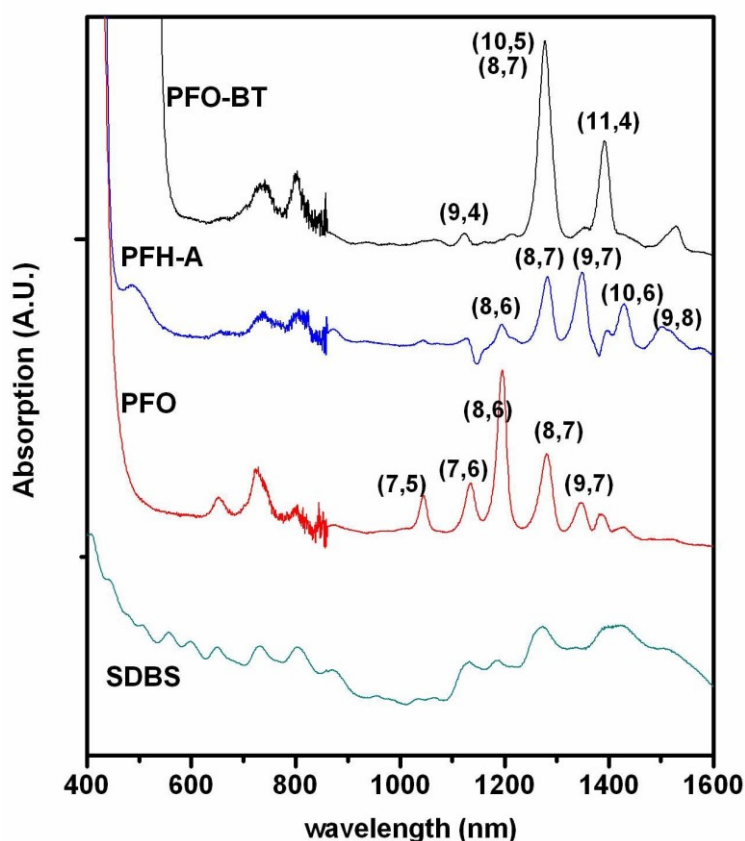


Figure 9: Optical absorption spectra for HiPco nanotubes dispersed in: SDBS/H₂O, PFO/toluene, PFH-A/toluene and PFO-BT/toluene dispersions. (Reproduced with permission from Chen, F. et al., *Nano Lett.* **7**, 3013–3017 (2007). Copyright © 2007 American Chemical Society).⁶⁴

Figure 9 summarizes some of the different chirality that can be sorted and dispersed from a HiPco carbon nanotube mixture with the appropriate choice of the polymer in a toluene dispersion, compared to the reduced selectivity of surfactant SDBS in water. Among the category of polyfluorene-based derivatives, PFO [poly(9,9-di-n-octylfluorenyl-2,7-diyl)] and PFO-BPy poly[(9,9-dioctylfluorenyl-2,7-diyl)-alt-co-(6,6'-{2,2'-bipyridine})] are particularly effective in sorting and dispersing (7,5) SWNTs and (6,5) SWNTs, respectively.

2.2 Conjugated Polymers and Molecules

Traditional polymers such as polyethylenes are characterized by sp^3 hybridization, in which the four valence electrons are bound in a linear chain of covalent σ bonds with carbon and hydrogen atoms. Such σ electrons have low mobility and do not take part in the conduction processes of the material. However, in conjugated material systems the situation is completely different because polymers become conductive through the continuous backbone of sp^2 hybridized carbon atoms forming three σ bonds at 120° to each other. The remaining valence electrons reside in p_z orbitals, which overlap to form a delocalized set of orbitals with π bonds. In this situation, a conjugated polymer is defined by the alternation of single/double or single/triple carbon bonds. However, it is not very easy to locate the π bonds. Sometimes an intermediate state is adopted, where π electrons are totally delocalized so that it is impossible to assign double or triple bonds. In conjugated molecules, π electrons delocalize throughout the entire molecule, sometimes far away from their original carbon, and are relatively loosely bound, so that a very high mobility can be achieved when the material is doped by oxidation. Thus, the conjugated π -orbitals form a 1D electronic band, and the electrons within this band become mobile when it is partially emptied by oxidation, making the material a p-type conductor.⁶⁵

Equivalent to the valence/conduction band description of inorganic semiconductors, in an organic semiconductor the HOMO (Highest Occupied Molecular Orbital) is defined as the molecular orbital filled with the last pair of electrons and the LUMO (Lowest Unoccupied Molecular Orbital) is defined as the next molecular orbital beyond the HOMO. The HOMO and LUMO orbitals take therefore the same meaning of valence and conduction bands in inorganic semiconductors. They are also known as frontier orbitals and the energy difference between them is called the bandgap. The bandgap of conjugated polymers can be tuned rather widely by the attachment of side chains, which are also essential to improve the polymer solubility. Side chains lead to twisting of the backbone out of the coplanar conformation. The twist angle depends on the length, type and bulkiness of the side chains. The larger the twist, the poorer the overlap between

the delocalized orbitals, thus a blue-shift occurs and the bandgap increases.⁶⁵ When an electron is removed from the HOMO or added to the LUMO, the resulting molecule is called a radical cation for positive charge, and radical anion for negative charge, where the word radical refers to the net spin the molecule due to the unpaired remaining/added electron. Radical ions are also called polarons, and they are not delocalized. Due to the localized character of the polaron, its charge strongly couples to the molecular geometry. Bond distances and angles result distorted compared to the neutral molecule. After removal or addition of the electron, molecular orbitals and the positions of nuclei within the backbone chain respond with a structural relaxation to a new position of minimum energy. This distortion always reduces the energetic cost of forming a polaron. The energy required to form a positive polaron is called the ionization potential I_p , while to form a negative polaron is called electron affinity E_a .⁶⁵

Charge carrier mobility is one of the most important parameters of organic semiconductors. It can range between 10^{-7} cm²/Vs and 10^{-1} cm²/Vs within the regime of hopping transport, which characterises low-temperature conduction in strongly disordered systems with localized charge carrier states, and it can go up to 10 cm²/Vs or more for coherent motion typical of organic single crystals. This difference can be understood with the concept of the effectively conjugated segment. In this description, a conjugated polymer consists of a string of effectively conjugated segments, at the end of which one unit ends and another begins. Hence, the presence of conformational degree of freedom in a polymer chain may limit the coherence of the π electron cloud and thus reduce the effective conjugation length. The longer the conjugation length, the more extensive the π electron coherence is, and the smaller the bandgap becomes (red-shift). Concerning charge carrier transport and mobility, molecular packing and the orientation of neighbouring polymer chains play a fundamental role, thus morphology and material processing have a strong impact on device performance. Generally, a high degree of molecular order, called regio-regularity, is the key to enhance mobility. However, crystallization is usually undesirable because, although organic single crystals may display very high mobility and coherent transport, for realistic processing techniques, materials usually result in a polycrystalline morphology characterized

by grain boundaries and interfaces between crystalline and amorphous regions, which typically represent deep traps with undesirable effects.⁶⁶

2.3 Semiconducting Metal Oxides

A semiconducting metal oxide is a chemical compound that contains at least one metal and one oxygen atom in the oxidation state -2 . Like other solids, the electronic properties of semiconducting metal oxides are best described by their band structures, even though the interaction between the oxygen orbitals and the metal leads to more complex electronic structures and to a significant disparity between hole and electron conduction. They are valence compounds with a high degree of ionicity within their chemical bonding that creates an electronic structure that differs from standard covalent semiconductors like silicon. Generally, the metal s and oxygen $2p$ orbitals contribute to the formation of a highly-dispersed conduction band minimum (CBM) and a localised valence band maximum (VBM), respectively. This leads to a smaller effective mass for electrons, and consequently a better electron transport in comparison to hole conduction, even in an amorphous state. As a matter of fact, the large metal s orbitals remain close to one another in both ordered and disordered states of some oxide systems, hence allowing efficient electron transport and high electron mobility in non-crystalline materials.⁵³

Semiconducting metal oxides are often characterized by a large bandgap, thus preventing thermal generation of carriers and leading to low intrinsic carrier densities. A possible explanation for electron conduction focuses on the non-stoichiometry of metal oxide systems. Metal interstitials and oxygen vacancies are thus possible candidates for electron donors in these conductive systems. Finally, many semiconducting metal oxides exhibit either band-like or hopping-like charge transport behaviour. At lower temperatures, impurities dominate transport, and hopping between localised states caused by defects and impurities occurs. At room temperature instead, charge transport becomes more band-like. In addition to these mechanisms, charge transport is also highly affected by the material morphology and processing conditions, and the electron mobility can consequently vary over a wide range, from $1 \text{ cm}^2/\text{Vs}$ to $160 \text{ cm}^2/\text{Vs}$.^{52,53,55}

2.4 The Field-Effect Transistor

An organic field-effect transistor (OFET) is a field-effect transistor in which an organic semiconductor constitutes the channel. OFET have been developed to realize low-cost and large-area electronic products. The organic layer can be deposited by vacuum evaporation of small molecules, by solution casting of polymers, small molecules or carbon nanotubes, or by mechanical transfer onto a substrate. Originally, the field-effect transistor (FET) was first invented by J.E. Lilienfeld in 1930.⁶⁷ The three main components of field-effect transistors are the source, the drain and the gate, which controls the carriers' movement in the channel from the source to the drain. In the conventional Metal Oxide Semiconductor Field-Effect Transistor (MOSFET), the channel is the inversion layer modulated by the gate field between two heavily doped silicon regions (source and drain), and the semiconductor material typically is the substrate itself (silicon) with the doping opposite to source and drain regions. The choice of the gate material, the position of the gate with respect to the channel, and the choice of the gate dielectric material all have a big impact on device operation. Nowadays, many OFETs are designed based on the thin-film transistor (TFT) model, which allows devices to be thinner and to use less conductive materials.

2.4.1 Device Architectures

A thin-film transistor is a type of field-effect transistor characterized by a thin semiconducting layer, a dielectric layer, three metallic contacts, and a substrate. Figure 10 shows the four possible TFT architectures, two with top-gate and two with bottom-gate geometry. These structures are also referred to as staggered and coplanar, depending on the relative position of the gate and the source/drain contacts. If the gate and the contacts are on the same side, i.e. BG-BC and TG-TC, the device is in the coplanar configuration, with the conducting channel in contact with the source/drain contacts, and the current simply flows along the channel plane. On the other hand, if the gate and the contacts are on opposite sides with respect to the semiconducting layer (BG-TC and TG-BC) the device is in the staggered configuration. In this case, the current flows vertically in the semiconducting layer,

from the contacts towards the channel area, and then it flows along the channel plane. Because of this, the bulk resistance of the semiconductor may have a negative impact on device performance, even though the contact resistance is significantly reduced and charge injection is improved due to the larger contact area.^{68,69} For these reasons, the staggered architecture is usually preferred over the coplanar one.

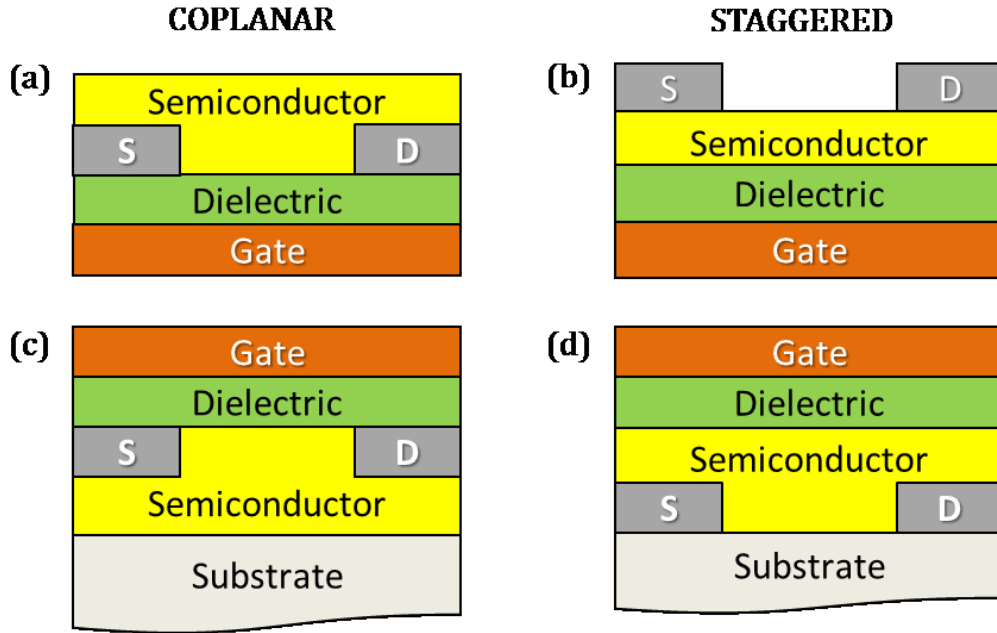


Figure 10: Possible four thin-film transistor architectures: (a) coplanar bottom-gate bottom-contact (BG-BG), (b) staggered bottom-gate top-contact (BG-TC), (c) coplanar top-gate top-contact (TG-TC), and (d) staggered top-gate bottom-contact (TG-BC).

In the top-gate architecture, common substrates are glass or plastic, while for the dielectric, solution-processable polymer dielectrics are often used. The gate electrode is then deposited on top of the dielectric, and usually it is patterned in order to cover only the channel area and avoid any overlap with the source/drain contacts that can generate stray capacitances and increase leakage currents. In the bottom-gate architecture instead, the semiconductor is deposited on top of the dielectric, which can be the native oxide SiO_2 of the silicon substrate or other oxides, such as Al_2O_3 or ZrO_x , deposited onto a silicon substrate. In this case, the silicon substrate usually is heavily doped and it can be used as a common unstructured bottom-gate electrode.

2.4.2 Operating Principles

The operation of the TFT can be described by the following three parameters: the drain current (I_D), the gate-source voltage (V_{GS}), and the drain-source voltage (V_{DS}). Since the source contact is usually grounded ($V_S = 0$), V_{GS} and V_{DS} can be referred to as V_G and V_D . The application of a gate voltage V_G induces the accumulation of charges at the interface between the semiconducting layer and the dielectric. The region of semiconductor in contact with the dielectric and included between the drain and source electrodes constitutes the channel. Once charges have been accumulated in the channel, by applying the appropriate bias to the drain electrode a current flow is generated between the source and the drain electrodes. Ideally, when no gate voltage is applied, the intrinsic conductance of the channel is so low that no current flows and the device is in the OFF state. When the appropriate gate voltage is applied, free carriers are induced in the channel and the transistor turns in the ON state. The gate voltage is therefore used to turn the device ON and OFF, and the voltage required to do so is called the turn-on voltage (V_{ON}). An important observation is that while the conventional MOSFET works in the depletion mode, with the minority carriers flowing in the inversion layer, the TFT instead works in the accumulation mode, with free carriers induced directly in the channel.

Figure 11 shows the mechanism of charge accumulation in the channel. By applying a positive bias to the gate electrode, negative charges are induced in the semiconductor and accumulate in the channel region. Once a positive bias is also applied to the drain electrode, electrons are then injected from the source and collected by the drain, thus producing a drain-source current I_{DS} . In the case of a negative gate bias and negative drain bias, the mechanism is the same but positive charges are induced in the semiconductor and accumulate in the channel, thus producing a hole current between source and drain electrodes. When negative charges (electrons) are induced in the channel, the TFT is called n-type while, when positive charges (holes) are induced, the TFT is called p-type. Usually organic semiconductors are p-type, even though n-type polymers and small molecules have been recently demonstrated.⁶⁶

The dielectric layer also plays a very important role in TFT operation. The choice of the dielectric material and the dielectric thickness play a major role on device performance because they determine the capacitive coupling between the gate and the semiconductor, affecting the amount and the type of charge carriers (electrons/holes) induced in the channel region.

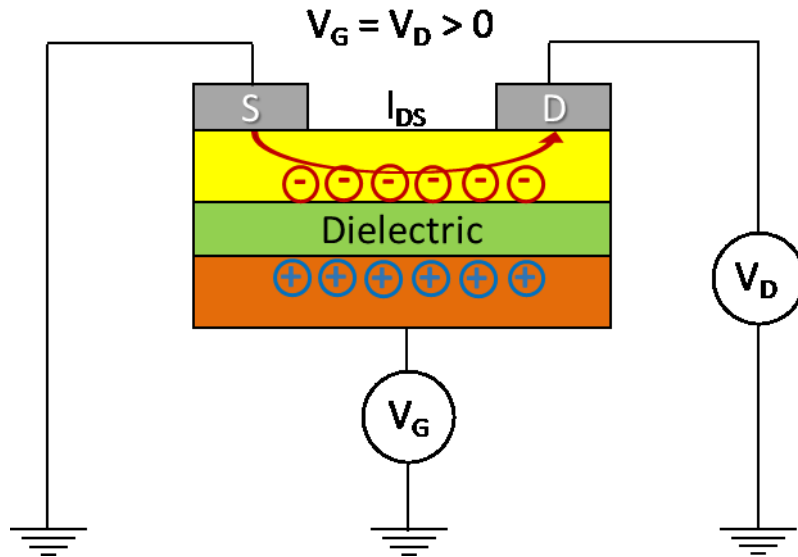


Figure 11: Schematic of a bottom-gate top-contact TFT with $V_G > 0$, $V_D > 0$ and $V_S = 0$. By applying a positive bias to the gate electrode, negative charges are induced in the semiconductor and accumulate in the channel region. Once a positive bias is also applied to the drain electrode, electrons are then injected from the source and collected by the drain, thus producing a drain-source current I_{DS} . In the case of a negative gate bias and negative drain bias, the mechanism is the same but positive charges are induced and accumulate in the channel, thus producing a hole current between source and drain electrodes.

If we consider a TFT where an n-type semiconductor is deposited in the channel region, upon the application of a positive gate and drain bias, negative charge carriers are accumulated and the channel becomes highly conductive (ON state). On the other hand, if the gate is negatively biased, the channel is depleted from electrons and it behaves as an insulator, thus no current can flow (OFF state). The ratio between the current in the ON state and the current in the OFF state is called the current ON/OFF ratio, and it is a very important figure of merit for TFTs. Figure 12 summarizes all the possible operation regimes for n-type and p-type TFTs.

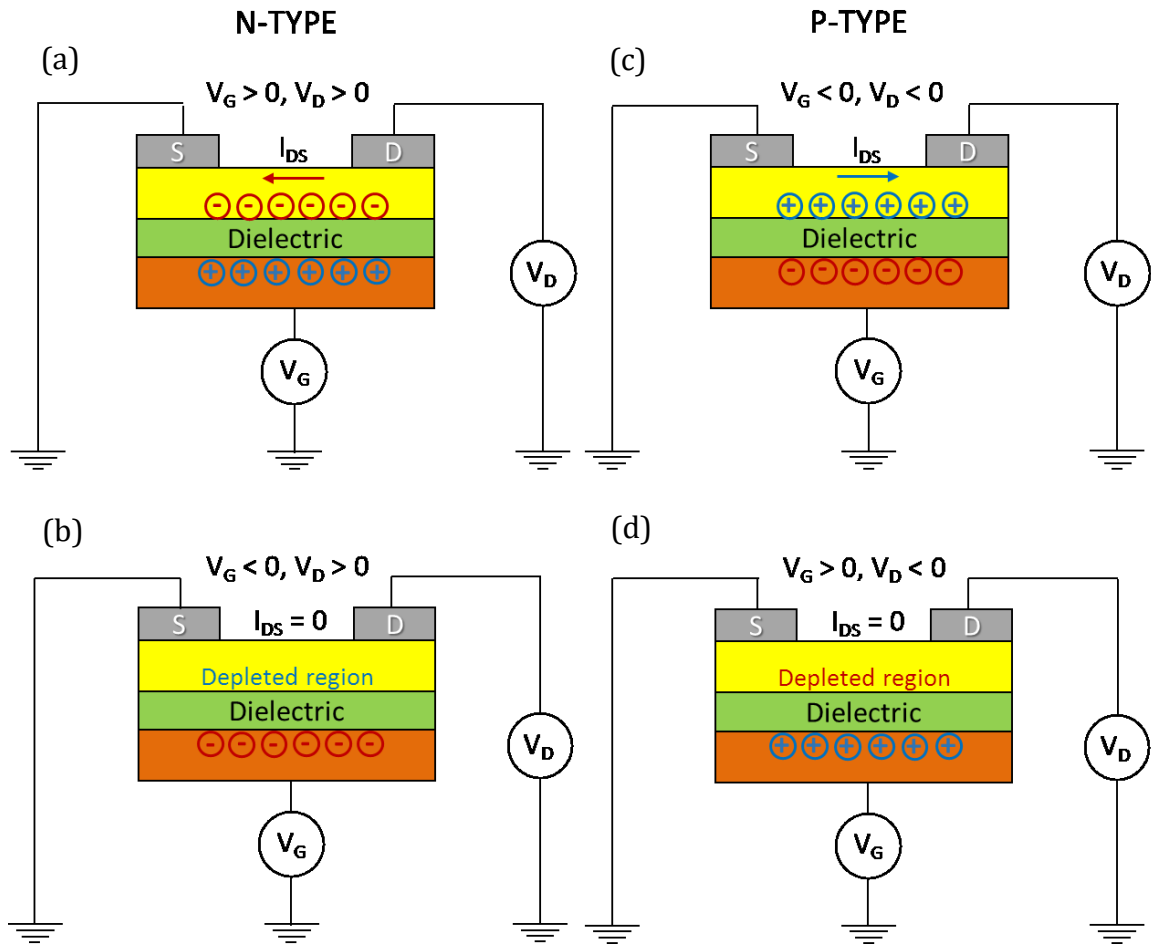


Figure 12: Schematics of the accumulation (ON state) and depletion (OFF state) regimes for n-type and p-type TFTs. In an n-type TFT, (a) current can flow when $V_G > 0$ and $V_D > 0$ while (b) for $V_G < 0$ and $V_D > 0$ the channel is depleted from electrons and no current can flow. In a p-type TFT, (c) current can flow when $V_G < 0$ and $V_D < 0$ while (d) for $V_G > 0$ and $V_D < 0$ the channel is depleted from holes and no current can flow.

In the Experimental Results chapter, SWNT transistors are referred to as FETs and not TFTs because the semiconducting layer does not form a uniform thin-film, which is a requirement for a TFT, but it forms a 2D random network due to processing and deposition conditions which affect carbon nanotube morphology. However, this is only a terminology refinement, as there are no changes in terms of device operation and electrical characteristics.

2.4.3 Electrical Characteristics

A well-accepted approximation to describe the behaviour of a TFT is the square-law model. In addition to the three electrical parameters I_D , V_G and V_D , this model also uses the geometric capacitance of the dielectric (C_i), the channel length (L_c) and channel width (W_c), as well as the field-effect mobility μ and the threshold voltage (V_{TH}).

After few calculations, the following drain-current equation is derived:⁷⁰

$$I_D = \frac{W_c}{L_c} \mu C_i \left[(V_G - V_{TH}) V_D - \frac{(V_D^2)}{2} \right]. \quad (8)$$

Figure 13 shows the output (a) and transfer (b) curves of a typical p-channel TFT.

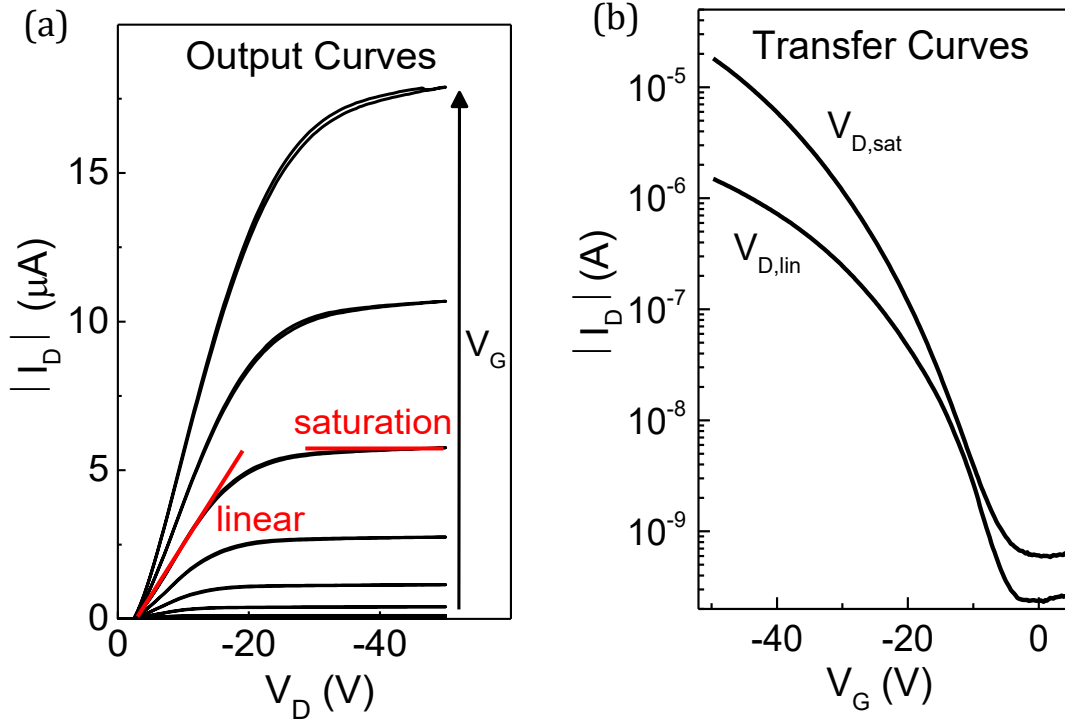


Figure 13: Output (a) and transfer (b) characteristics of a typical p-type TFT. The transfer curves are in logarithmic scale.

Two regions of operation are depicted in the output curve, namely the linear region and the saturation region. The voltage that defines the boundary between these two regimes is $V_G - V_{TH}$. Starting from the linear regime, in which the charge distribution in the channel is uniform, the device initially acts as a resistor and I_D increases linearly with V_D . Their relationship becomes sub-linear as V_D increases

further, creating a depletion layer near the channel/drain contact interface, and finally I_D saturates when $V_D \geq V_G - V_{TH} = V_{D,sat}$. When the slope of each I_D curve is zero in the saturation regime, the device exhibits a hard saturation, which indicates that the entire thickness of the channel is depleted of free carriers. Hard saturation is highly desirable for circuit applications, because a large output impedance characterizes a TFT operating in this regime.

For the specific cases of the linear and saturation regimes, equation (8) can be simplified. In the linear regime, V_D is small and hence I_D becomes:

$$I_{D,lin} = \frac{W_C}{L_C} \mu_{lin} C_i [(V_G - V_{TH}) V_D]. \quad (9)$$

When the transistor enters the saturation regime, $V_D \geq V_{D,sat}$ and I_D becomes independent from V_D , as shown in Figure 13(a), leading to the following equation:

$$I_{D,sat} = \frac{1}{2} \frac{W_C}{L_C} \mu_{sat} C_i (V_G - V_{TH})^2. \quad (10)$$

Several assumptions are made to derive the equations of the square-law model:

1. The gradual channel approximation, which assumes that in the channel the electric field perpendicular to the channel, is much greater than the electric field parallel to the channel. This assumption allows the two electric fields to be considered separately.⁷¹
2. The charge in the channel varies linearly with respect to the applied gate voltage.
3. All charge carriers induced in the channel are due to the gate field and are free carriers with a uniform mobility.

In order to consider a more realistic model, several non-idealities must be accounted. First, the series resistances at the source and/or drain contacts lead to a reduction of the intrinsic voltage drop in the channel, decreasing the drain current respect the ideal square-law model. Secondly, if a high bulk carrier concentration is present in the channel, the induced charge density does not vary linearly with respect to the applied gate voltage, as assumed in the ideal square-law model.

Thirdly, charge carrier traps reduce further the drain current respect the ideal TFT operation.⁷⁰

2.4.4 Electrical Parameters

From equations (9) and (10) it is possible to extract all the fundamental parameters of a TFT.

1. The threshold voltage V_{TH} can be extracted from the $\sqrt{I_{D,sat}}$ vs. V_G , as the x -intercept of the interpolated line in the linear region. It represents the minimum gate voltage that is needed to create a conducting path between the source and drain contacts.
2. Mobility is defined in the linear and saturation regimes, depending on the TFT operation. Linear mobility can be extracted from equation (9):

$$\mu_{lin} = \frac{L_C}{C_i V_D W_C} \frac{\partial I_{D,lin}}{\partial V_G}. \quad (11)$$

Saturation mobility can be extracted from equation (10):

$$\mu_{sat} = \frac{2L_C}{C_i W_C} \left(\frac{\partial \sqrt{I_{D,sat}}}{\partial V_G} \right)^2. \quad (12)$$

3. The current ON/OFF ratio is defined as $\frac{I_{D,ON}}{I_{D,OFF}}$.
4. The turn on voltage (V_{ON}) corresponds to the initial onset of appreciable drain current. It can be extracted from the steepest point of the $\log(I_D)$ vs V_G transfer curve. This onset occurs when I_D is larger than the gate leakage and/or the noise level of the measurement instrumentation.
5. The subthreshold swing (S) is a measure of how quickly the transistor changes between the OFF and ON state. It can be extracted from the maximum slope in the logarithmic plot of the transfer curve:

$$S = \left(\frac{\partial \log(I_D)}{\partial V_G} \right)^{-1}. \quad (13)$$

The minimum theoretical S of a conventional device is 60 mV/dec at room temperature. A typical experimental value for a MOSFET is 70 mV/dec.

2.4.5 Dielectric-Semiconductor Interface

The performance of a TFT are highly dependent on the properties of the gate dielectric. The choice of the dielectric material can affect the morphology of the semiconductor film, the roughness of the dielectric-semiconductor interface, and the dielectric constant (k). Charge carrier trap states at the semiconductor-dielectric interface are known to significantly affect the threshold voltage, as traps must be filled before current can start flowing in the channel. As an insulator, the dielectric should have a high resistivity to keep parasitic gate leakage currents (I_G) low. Moreover, it is also desirable for the dielectric to have a high breakdown electric field, in order to sustain high voltages when needed. The capacitance per unit area [nF/cm^2] is given by:

$$C_i = \frac{\varepsilon_0 k}{t}, \quad (14)$$

where $\varepsilon_0 = 8.854 \times 10^{-5} \text{ nF}/\text{cm}$ is the vacuum permittivity, k is the relative dielectric constant and t is the dielectric thickness expressed in cm.

There are three main types of gate dielectrics typically employed within a TFT: polymeric, inorganic and self-assembled monolayers (SAMs).⁷² Polymer dielectrics are often deposited on top of the semiconducting layer in top-gate device configurations. On one hand, they have the advantage of being solution processable and hence are compatible with low cost fabrication techniques. On the other hand, they have a low dielectric constant and thus they need to be deposited in very thin layers in order to be effective. Most commonly used polymer dielectrics include the fluoropolymer CYTOPTM⁷³ and PMMA (poly(methyl-methacrylate)).⁷²

Bottom-gate devices instead often employ an inorganic oxide layer directly grown on the gate surface. The surface of oxide dielectrics is strongly affected by processing techniques and can lead to shifts in threshold voltage and hysteresis. As an example, SiO_2 surface is known to have many electron trap states; hence passivation with self-assembled monolayers such as hexamethyldisilazene (HMDS)

or octadecyltrichlorosilane (OTS) is often necessary to avoid performance degradation. High- k inorganic dielectrics, such as barium strontium titanate (BST, $k = 16$) and barium zirconium titanate (BZT, $k = 17.3$), have also been used to fabricate TFTs with low operating voltages $\leq 5\text{V}$.^{72,74}

Self-assembled monolayers (SAMs) were first used as dielectrics to improve the insulating quality of native oxides and hence reduce leakage currents in inorganic devices. Three molecular structures of the most commonly used SAM for organic TFT dielectrics are shown in Figure 14. They are octadecylphosphonic acid (ODPA), phosphonohexadecanoic acid (PHDA), and (3-aminopropyl)triethoxysilane (APTES).

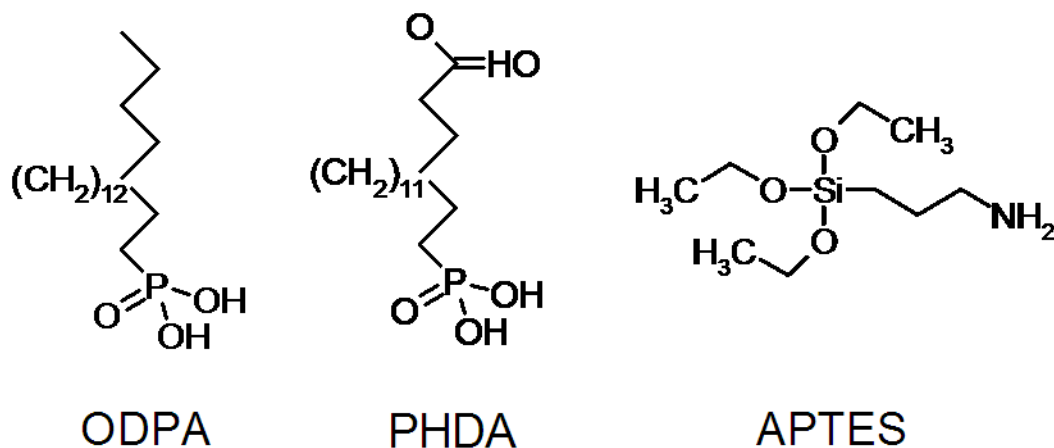


Figure 14: Molecular structure of SAMs commonly used in organic TFTs as dielectrics. The example molecules are octadecylphosphonic acid (ODPA), phosphonohexadecanoic acid (PHDA) and (3-aminopropyl)triethoxysilane (APTES).

In addition to their application for low-voltage TFTs with $|V_G| \leq 2\text{V}$, SAMs are also commonly used to passivate inorganic dielectric surfaces and to modify the dielectric surface energy and the threshold voltage of devices.^{75,76}

2.4.6 The Ambipolar OFET

The ambipolar OFET is a transistor that, under appropriate biasing conditions, can show both p-type and n-type behaviour. For ambipolar operation to occur, the semiconductor LUMO and HOMO must be aligned with the work functions of the injecting source/drain electrodes. Due to difference in offset between the injecting electrodes work function and the HOMO and LUMO of the semiconductor, the energetic barriers for hole and electron injection are not necessarily the same. In addition, the density of trap states is not likely to affect in the same way the two carrier pathways. For these reasons, the threshold voltage for holes and electrons is usually different. Within an ambipolar OFET, the current flow in the channel can be due to holes, electrons or both carriers simultaneously, depending on the bias applied to the gate and drain electrodes.

Figure 15 shows all possible operating regimes for the ambipolar OFET as a function of gate and drain biasing. When $V_G > 0$ and $V_D > 0$ (regime 1), the device operates in the standard unipolar n-type regime, while when $V_G < 0$ and $V_D < 0$ (regime 4), the device operates in the standard unipolar p-type regime. In an ambipolar OFET, electrons can still be injected when there is a hole depleted region in the channel ($V_G > 0$ and $V_D < 0$) (regime 6), and vice versa for holes when there is an electron depleted region ($V_G < 0$ and $V_D > 0$) (regime 3). Simultaneous injection of electrons from the source and holes from the drain occurs when $V_D > V_G - V_{TH} > 0$ (regime 2) and when $V_D < V_G - V_{TH} < 0$ (regime 5). Under those biasing conditions, a conventional OFET operates in saturation; the channel is pinched-off and charges cannot accumulate in the channel. In an ambipolar OFET however, those biasing conditions produce a change in the sign of the effective gate potential at a certain position in the channel.⁷⁷ Holes and electrons accumulate at opposite sides until a narrow transition region is formed, which acts as a *pn*-junction and where recombination takes place. As expected from electron-hole recombination, if the semiconductor is optically active, light emission often takes place, allowing these devices to be used as light-emitting organic field-effect transistors (LE-OFETs).⁷⁸

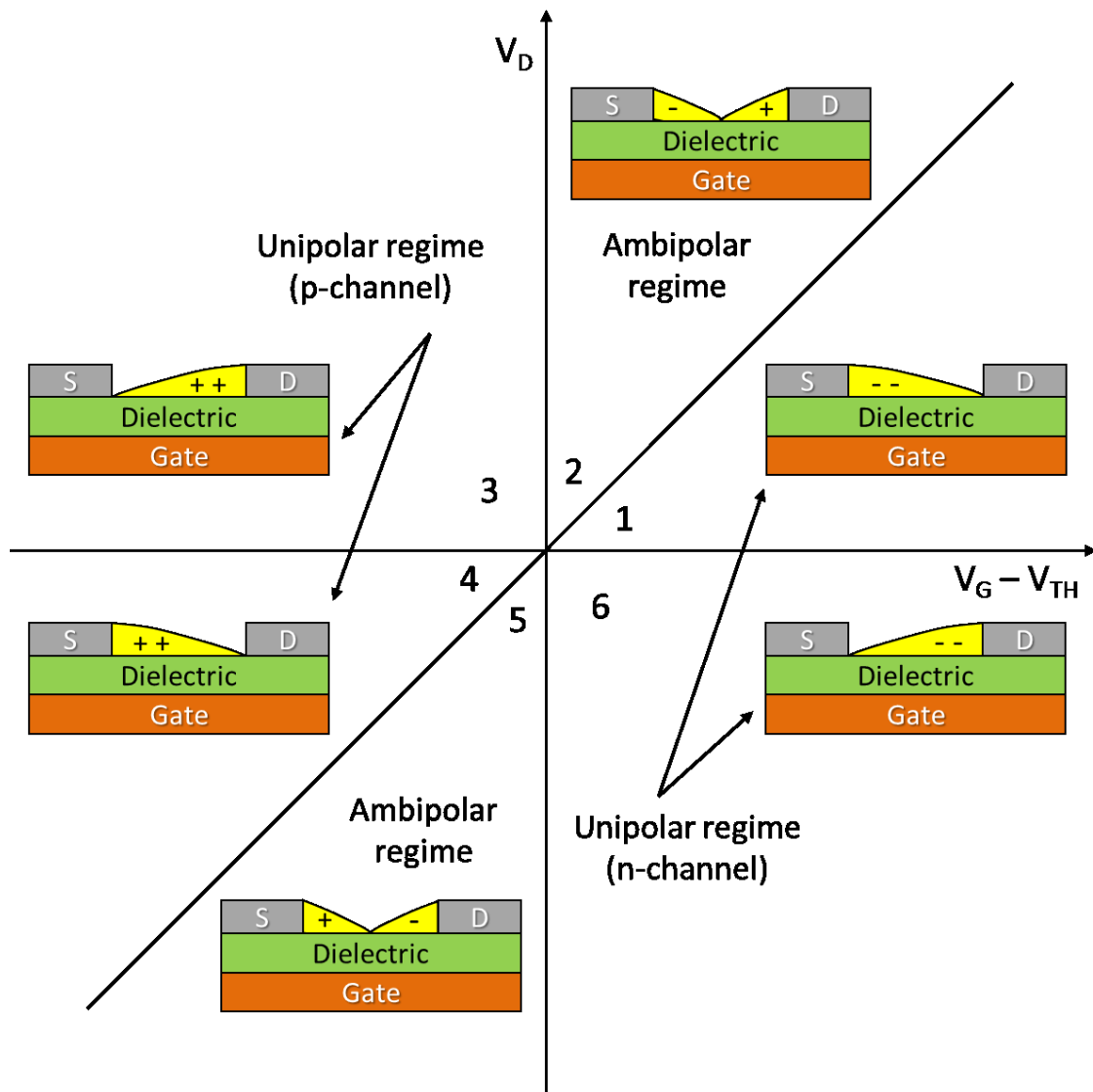


Figure 15: Schematic representation of all the possible operating regimes for an ambipolar OFET as a function of drain and gate biasing. Regimes 1 and 6 represent the standard unipolar regime for an n-type device, regimes 3 and 4 represent the standard unipolar regime for a p-type device, while regimes 2 and 5 represent the ambipolar regime where electrons and holes are simultaneously injected in the channel and recombination occurs.

2.4.7 The 2D Homogeneous Random-Network Stick Percolation Model

Percolation theory describes the behaviour of connected clusters in an inhomogeneous random system, and was originally developed to study the movements of fluids through porous materials. By using a slightly different mathematical model called site percolation, a site is "occupied" by a metallic nanotube with probability p or "empty" with probability $1-p$. Moreover, the percolation threshold is defined as the critical value of the occupation probability p such that infinite connectivity (percolation) occurs. In this case the question is: for a given p that a site is occupied by a metallic nanotube, what is the probability that a continuous metallic path exists between source and drain? To answer this question, the stick percolation model for an ideal 2D homogeneous random-network^{79,80} is applied to SWNT FET. The constant conductivity approximation is used, in which FETs are characterized in the linear regime (low-bias) and a constant charge density is assumed along the channel. With these assumptions, the universal current-scaling equation for I_D in the low-bias regime can be obtained:

$$I_D \approx \frac{k}{L_s} \left(\frac{L_s}{L_c} \right)^m, \quad (15)$$

where k [A·cm] is a parameter that depends on the stick-to-stick interaction ($C_{i,j}$), the nanotube diameter (d), the dielectric capacitance (C_i), the channel width (W_c) and biasing conditions.^{80,81} The exponent m instead depends on the anisotropy of the nanotubes and on the normalized coverage (ρL_s^2). In this model, the percolation threshold for a random network has the following expression:

$$\rho_{th} = \frac{4.236^2}{\pi L_s^2}. \quad (16)$$

In the case of a random network with a normalized coverage much higher than the percolation threshold ($\rho L_s^2 \gg 4.236^2 / \pi$), most of the nanotubes are connected together forming several conductive paths and therefore the network behaves as a 2D conductor, with $m \sim 1$. Thus, in the limit of the 2D conductor, corresponding to

the network formed by the majority semiconducting nanotubes, the universal current-scaling equation (15) reduces to Ohm's law where $I_D \propto k / L_C$. Vice versa, if the normalized coverage is below the percolation threshold, most of the nanotubes are not interconnected and the presence of conducting paths between the drain and source electrodes strongly depends on L_C as compared to L_S . This situation corresponds to that small part of the network formed by the minority metallic nanotubes, where the percolation regime dominates the channel conduction mechanism, and the exponent $m > 1$ can be found experimentally from the OFF current (I_{OFF} vs L_C). Once the exponent for metallic nanotubes is known, for a random network $m = f(\rho L_S^2)$, and hence the surface density ρ_{met} of the residual metallic nanotubes in the FET channel is obtained, and therefore also their concentration.⁴⁵

In addition to the residual amount of metallic nanotubes, other key factors that influence the performance of SWNT FETs are the channel length (L_C) as compared to the nanotubes length (L_S), the surface density (ρ) of the entire SWNTs population, and their degree of alignment.^{42,79} More specifically, for longer channel devices, where $L_C > L_S$, high current ON/OFF ratio can still be reached even with a small percentage of residual metallic carbon nanotubes, as long as they do not constitute percolating pathways across the channel, resulting in electrical shorts between the source and drain electrodes. This can be achieved by keeping the surface density of residual metallic nanotubes as low as possible and definitely below the percolation threshold. This is the case where percolation theory can be applied to characterize the SWNT network and quantify the metallic nanotubes content.⁴⁵ For short channel devices, where $L_C \leq L_S$, the situation is quite different because the presence of even a single metallic nanotube could in principle electrically short the source and drain electrodes and drastically reduce the transistor's current ON/OFF ratio. This case is known as the direct conduction regime. Lowering the density of the SWNT network can help to minimize the impact of metallic nanotubes but it has a negative effect on channel transconductance and charge carrier mobility. Therefore, achieving simultaneously high current ON/OFF ratio and high conductance in the ON state

remains a major challenge even for the purest solution-processed semiconducting SWNT networks.^{45,80,82}

Another important parameter affecting the SWNT FET performance is the degree of alignment between SWNTs in the network. It has been demonstrated⁸³ that, for long channel devices, I_D is maximized, with a 20% to 40% increase respect the random network, by an optimum angle ($0^\circ < \theta_{opt} < 45^\circ$) between the random ($\theta = 45^\circ$) and aligned networks ($\theta = 0^\circ$), while it rapidly degrades as perfect alignment ($\theta \rightarrow 0^\circ$) is reached. This happens because the percolation threshold density depends on the angle, and it is $\rho_{th,45^\circ} = 4.236^2/\pi L_S^2$ (equation (16)) for the random network, and $\rho_{th,0^\circ} \rightarrow \infty$ for the fully-aligned network, because increasing alignment reduces the probability of nanotube crossing each other when $L_C > L_S$. Thus, even though alignment reduces the number of nanotubes required to bridge the electrodes, the probability of formation of such connections (given by $\rho_{th,0^\circ}$) reduces as well and consequently $I_D \rightarrow 0$. Hence, for long channel devices, the benefit of alignment is small and a random network is unexpectedly close to being optimal.

Opposite is the case of short channel devices, where many nanotubes can directly bridge source and drain electrodes ($\rho_{th} \rightarrow 0$) for random as well as aligned networks, and $I_D \neq 0$ even for $\theta \rightarrow 0^\circ$. In general, nanotubes not bridging source and drain electrodes directly also contribute to I_D by creating percolating pathways, and this shifts the optimal alignment away from zero ($\theta_{opt} > 0^\circ$). However, since a higher fraction of nanotubes directly bridge the source and drain electrodes at shorter L_C , contribution from nanotube percolation reduces quickly and $\theta_{opt} \rightarrow 0^\circ$ is needed to optimize smaller L_C transistors and achieve an I_D increase of up to 100%.^{42,83}

2.5 Logic Circuits

A logic gate is the building block of logic circuits and it is a physical device implementing a Boolean function, which is a logical operation on one or more logical inputs generating a single logical output. Logic gates are primarily realised using transistors acting as electronic switches and they can be cascaded in the same way in which Boolean functions can be composed, allowing the creation of a physical model of all the algorithms and mathematics that can be described with Boolean logic. In practice, most logic gates are made from FETs, particularly MOSFETs. Figure 16 shows the three most common logic gates with their corresponding symbol and truth table.

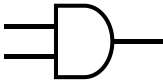
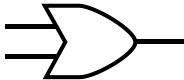
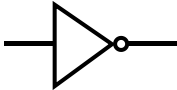
AND			OR			NOT	
							
INPUT		OUTPUT	INPUT		OUTPUT	INPUT	OUTPUT
A	B	A AND B	A	B	A OR B	A	NOT A
0	0	0	0	0	0	0	1
0	1	0	0	1	1	1	0
1	0	0	1	0	1		
1	1	1	1	1	1		

Figure 16: AND, OR and NOT logic gates with corresponding symbol and input/output truth table.

The elementary building block of digital logic is the NOT gate shown in Figure 16, which is also known as inverter because it inverts an input signal. Logic circuits are called unipolar if they are made of FETs with only one type of carrier (p- or n-type). If the FETs used in the circuit are both p- and n-type, the logic gate is called complementary. Complementary logic gates must always be preferred over unipolar gates because they can achieve higher operating speed and lower power dissipation.

2.5.1 The Unipolar Inverter

Among all unipolar logic circuits, the inverter (NOT gate) is the building block of digital logic. The unipolar inverter consists of a driving transistor (T_D) in series with a linear load (L) or another transistor acting as a load (T_L). The inverter is connected to power (V_{DD}) and ground (GND) for operation. It can be implemented either with a p-channel transistor or with an n-channel transistor, as shown in the Figure 17. When the appropriate voltage at the input (V_{IN}) is set low, the channel does not conduct any current (OFF state) and the output voltage (V_{OUT}) is tied to V_{DD} . Vice versa, when V_{IN} is set high, the channel is in the ON state and V_{OUT} is tied to GND. This gives rise to the Boolean logic function of inversion.

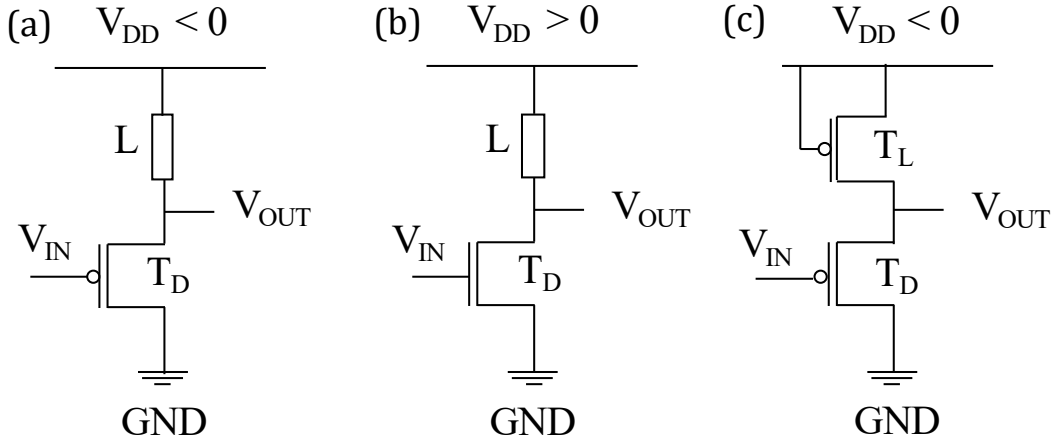


Figure 17: Electrical equivalent of (a) unipolar inverter with p-channel transistor and resistive load L , (b) unipolar inverter with n-channel transistor and resistive load L , (c) unipolar inverter with p-channel transistor and diode load T_L .

Digital inverter performance is often measured using the voltage transfer curve (VTC), which is a plot of V_{OUT} vs. V_{IN} . From such a graph, device parameters including gain, noise margin, and operating logic levels can be obtained. Ideally, the VTC appears as an inverted step function, but in real devices, there is a gradual transition

region. The slope of this transition region corresponds to the gain $G = \frac{\partial V_{OUT}}{\partial V_{IN}}$, and

it is a measure of quality, i.e. steeper slopes yield more precise switching. The noise margin (NM) is the amount by which the signal exceeds the threshold for a proper '0' or '1', which corresponds to the amount of noise that a circuit can withstand.

Ideally, an inverter VTC should have the maximum slope centred at the midpoint voltage $\left(V_M = \frac{V_{IN}}{2}\right)$ and the '0' and '1' logic states equal to GND and V_{DD} . For an integrated digital circuit to operate, the output of an inverter has to serve as input for a subsequent inverter stage. A minimum condition for this is that the inverter stage has a $G > 1$ and a NM as high as possible, ideally $NM = \frac{V_{IN}}{2}$, which is the maximum possible value. Figure 18 shows an ideal and a non-ideal VTC for a p-channel OFET with the corresponding gain and noise margin.

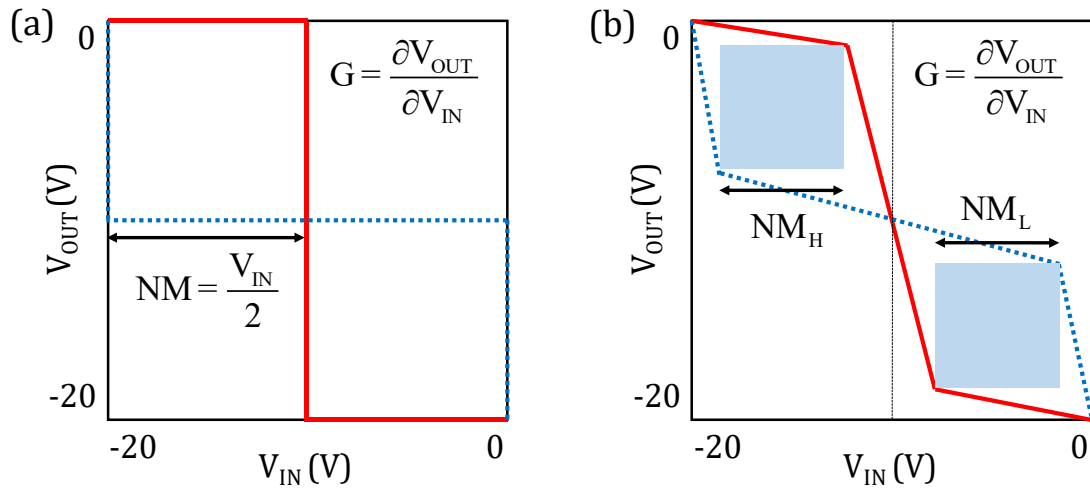


Figure 18: Schematic representation of (a) an ideal VTC with infinite gain and maximum noise margin, and (b) a non-ideal VTC typical of unipolar inverters, with finite gain and asymmetric noise margins high (NM_H) and low (NM_L) lower than $V_{IN}/2$. In both graphs $V_{DD} = -20V$ and $V_M = -10V$.

Unipolar logic circuits are characterised by a simple fabrication process, as they comprise of a single semiconducting material and a single contact material, but they are typically associated with low noise margin, low gain, and low yield. Moreover, unipolar inverters dissipate power while maintained in one logic state, i.e. high or low, because the load is a passive component and it cannot be turned off, hence current constantly flows in the circuit. This is called static power dissipation and it is a significant disadvantage since 50% of the inverters in the circuit consume power continuously.

2.5.2 The Complementary Inverter

The complementary inverter, also called CMOS inverter, consists of two driving transistors that actively pull up and down the output node. The pull-up transistor (T_{PU}) is the p-type transistor, which pulls V_{OUT} to V_{DD} when V_{IN} is low, while at the same time the n-type transistor is switched off; the pull-down transistor (T_{PD}) is the n-type transistor, which pulls V_{OUT} to GND when V_{IN} is high, while at the same time the p-type transistor is switched off. The current flowing in both transistors and their threshold voltages should be matched for an optimized operation. Despite differences in charge carrier mobility, this can be done by optimizing the W_C/L_C ratio of both transistors. Ideally, the drain current in each transistor should be equal at the midpoint voltage, which can be expressed by:

$$V_M = \frac{\sqrt{\frac{\beta_n}{\beta_p}} \cdot V_{TH,n} + (V_{DD} - V_{TH,p})}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}, \quad (17)$$

$$\beta = \frac{W_C}{L_C} \mu C_i, \quad (18)$$

where β is a design factor used to adjust the p- and n-channel drain currents. If the p- and n-type transistors are equivalent, from equation (17) it follows that $V_M = V_{DD}/2$. Otherwise, if the two transistors have different mobility and threshold voltages, the β factor must be properly adjusted in order to obtain identical drain currents. Therefore, a proper selection of p- and n-type semiconducting materials with balanced μ and V_{TH} is of crucial importance and it should be done as the first step before adjusting the β factor for a comprehensive device optimization.⁸⁴

Figure 19 shows the electrical equivalent of (a) a complementary inverter made with p- and n-type OFETs from different semiconducting materials, and of (b) a complementary-like inverter made with two ambipolar OFETs.

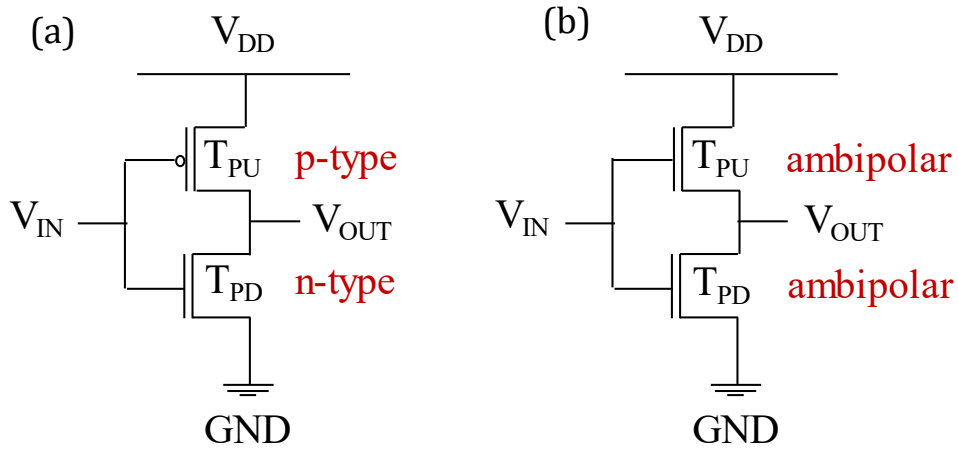


Figure 19: Electrical equivalent of (a) a typical complementary inverter with p- and n-channel transistors acting as pull-up and pull-down OFETs, and (b) a complementary-like inverter with identical ambipolar transistors acting as pull-up and pull-down OFETs.

Complementary inverters are typically associated with better performance than unipolar inverters. More specifically, the gain and noise margins are higher because the output voltage swing is “rail-to-rail” from V_{DD} to GND . Moreover, they dissipate power only during the transition between logic states. This is a significant advantage since the static power dissipation is extremely low and typically determined by the gate leakage currents of the individual OFETs. The only drawback of complementary logic is that different electrode materials and solution-processable semiconducting materials with high electron and hole mobility must be integrated on the same substrate for p- and n-type OFETs, thus increasing the complexity of fabrication.

3 Experimental Methods

In this chapter, all material processing methods, fabrication and characterization techniques that have been used in this thesis are explained. First, SWNT processing method is described, followed by the description of device fabrication procedures. Then, electrical and material characterization techniques are explained.

3.1 Material Processing

The majority of the SWNT solutions used to obtain the experimental results described in the next chapter have been dispersed using the polymer sorting method described in the works of Bottacchi F. *et al.* (2015)²¹ and (2016).⁴⁵ Both PFO/(7,5) SWNTs and PFO-BPy/(6,5) SWNTs have been used. In order to obtain the final dispersion, 100 mg of CoMoCat SWNTs with a diameter ranging from 0.7 nm to 0.9 nm (Sigma-Aldrich, SWNT content $\geq 77\%$) were first dispersed in 200 ml of toluene, together with 360 mg of PFO (Sigma-Aldrich, Mw ≥ 20000) or 200 mg of PFO-BPy (American Dye Source), depending if the final solution was based on (7,5) or (6,5) SWNTs. The mixture was then ultra-sonicated with a horn sonicator for 14 consecutive hours. Later, the dispersion was centrifuged for 30 minutes at 4000 rpm, and the supernatant was carefully selected. The excess polymer was then removed via vacuum filtration with a cellulose membrane acting as a filter to collect the SWNTs. Afterwards, the membrane was dissolved in acetone and the resulting SWNTs, floating on the acetone surface, were carefully selected and re-dispersed in chlorobenzene with the desired concentration, through 20 minutes ultrasonication and 1-hour cup sonication. Once the final SWNT solution was obtained, the absorption spectrum was taken to check its quality and concentration. A second round of centrifugation, vacuum filtration and cup sonication was repeated, if necessary, to improve the quality of the solution and to reduce as much as possible the polymer content. Finally, the SWNT dispersion was ultra-sonicated for 30 minutes prior to deposition to ensure that the nanotubes were well-dispersed and bundle-free.^{21,45}

The carbon nanotube/polymer blends described in section 4.4.3 have been instead obtained by blending together the carbon nanotubes (Sigma-Aldrich, SWNT content $\geq 77\%$) with polymer P3HT (Poly(3-hexylthiophene-2,5-diyl), Sigma-Aldrich, $M_n = 45000$ -65000, head-to-tail regioregularity $> 98\%$ $^1\text{H-NMR}$) and with polymer PTB7 (Poly({4,8-bis[(2-ethylhexyl)oxy]benzo[1,2-b:4,5-b']dithiophene-2,6-diyl}{3-fluoro-2-[(2-ethylhexyl)carbonyl]thieno[3,4-b]thiophenediyl}), Sigma-Aldrich, $M_w = 80000$ -200000).

Figure 20 shows some pictures taken during the different steps of the polymer sorting procedure.

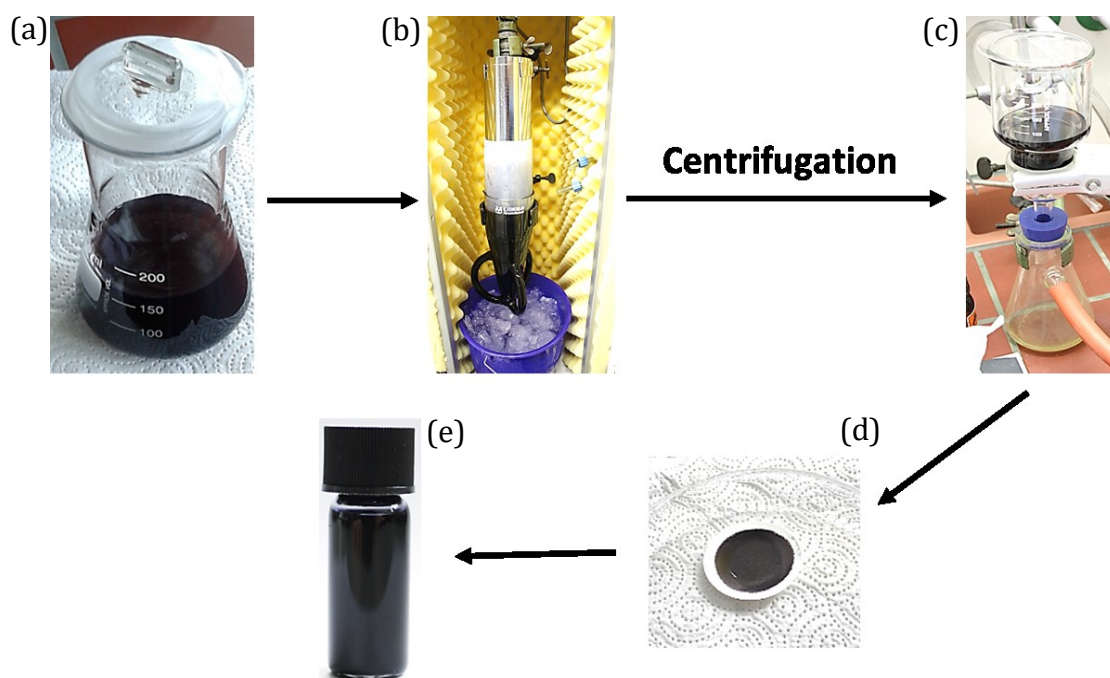


Figure 20: Pictures taken during the various steps of the polymer sorting procedure. (a) SWNTs and the polymer are dispersed in toluene and (b) subjected to 14 hours of horn sonication. After centrifugation, the supernatant is selected, (c) the solution is vacuum filtered to remove the excess polymer, and (d) the remaining cellulose membrane is dissolved in acetone. Finally, SWNTs are collected and (e) re-dispersed in chlorobenzene with the desired concentration. These pictures were taken by Miss Imge Namal at Würzburg University.

All the SWNT solutions dispersed with the polymer sorting method and used for the experimental results have been processed by Dr Florian Späth and Miss Imge Namal at Würzburg University, under the supervision of Prof Tobias Hertel, as part of a collaboration within the EU-FP7 project POCAONTAS.

3.2 Device Fabrication

This section introduces the various methods and techniques that were used for the fabrication of rigid as well as flexible TFTs, unipolar and complementary inverters based on SWNT films.

3.2.1 Spin-Coating

Spin-coating is a technique used to deposit uniform thin-films onto flat substrates. A small amount of material is usually poured with a pipette on the centre of the substrate, which can be either slowly spinning or not. The substrate is then rotated at high speed so that the material can be spread out by centrifugal force. Rotation continues until the desired film thickness is achieved. The solvent in which the material is dissolved is usually volatile and simultaneously evaporates so the higher the spinning speed, the thinner the film is. In addition to spinning speed, the thickness of the film also depends on the spinning time, the ramp time (acceleration), and on the viscosity and concentration of the solution and the solvent. The surface energy of the substrate and the hydrophobicity of the solution determine how good the sample is wet by the solution, which also greatly influences the resulting film thickness and uniformity. Drawbacks of this technique are a huge waste of material and the lack of scalability. SWNTs were spin-coated at 1000 rpm for 30 seconds inside a nitrogen glovebox, followed by 15 minutes of thermal annealing at 90 °C.

3.2.2 Thermal Evaporation of Metal Electrodes

Thermal evaporation from an electrically heated boat is a well-established method for thin-film deposition. The source material is evaporated in a high-vacuum chamber (10^{-6} mbar) in which vapour particles can travel directly to the substrate, placed in a holder above the boat, where they condense back to a solid state. Because the evaporated material arrives on the substrate mostly from one direction only, protruding features like the mask used to pattern the electrodes can prevent the evaporated material to reach some areas. This effect is called "shadowing" and to avoid it the substrate's holder is usually put in rotation for the entire evaporation.

3.2.3 TFT and Inverter Fabrication

In order to fabricate TFTs and inverters, a number of different substrate and dielectric material combinations can be employed. The most commonly used substrates are based on heavily doped Si^{++} wafers with a thermally grown 400 nm, 200 nm or 100 nm native oxide layer of SiO_2 as the gate dielectric. The semiconducting material, in this case SWNTs, was deposited from solution on top of the SiO_2 , followed by thermal evaporation of 5 nm of aluminium (Al) as adhesion layer and of 30 nm of gold (Au) source and drain electrodes. This yields to the staggered bottom-gate structure shown in Figure 10(b). Coplanar bottom-gate architecture devices were fabricated using pre-patterned substrates with photolithographically defined titanium/gold (Ti/Au) source and drain electrodes on top of a thermally grown 200 nm SiO_2 dielectric. Alternatively, a 50 nm layer of Al_2O_3 dielectric was deposited via atomic layer deposition (ALD) on top of a patterned bottom-gate chromium (Cr) electrode. With this device architecture, the last layer to be added is the semiconducting material, thus making this structure very convenient for complicated deposition techniques and for situations where nothing else can be deposited on top of the semiconductor. Even though pre-patterned substrates with a coplanar device architecture are not the best choice due to a reduced contact area for channel injection (see 2.4.1), they allow for a quick and easy assessment of material properties and device characteristics, which is the primary reason for their use. Similarly, pre-patterned substrates with a coplanar bottom-gate device architecture were used also for the fabrication of unipolar and complementary inverters.

Common to all different device configurations is the substrate cleaning process. Both silicon and glass substrates were cleaned with ultra-sonication in acetone and isopropyl alcohol (IPA) baths for 5 minutes each. Then, depending on the device architecture, different material layers were deposited on top. For the pre-patterned coplanar bottom-gate substrates on SiO_2 , provided by Philips, the semiconducting material was the only layer to be deposited. The staggered bottom-gate substrates on SiO_2 instead required first the deposition of the semiconductor layer, and later the evaporation of 5 nm/30 nm of Al/Au source and drain electrodes. For the

staggered top-gate substrates on glass, 5 nm/30 nm of Al/Au source and drain electrodes were evaporated first, then the semiconducting SWNTs and the dielectric, usually CYTOP, were spin-coated sequentially, and finally the Al gate electrode was evaporated (40 nm). CYTOP dielectric was spin-coated at 2000 rpm for 1 minute, followed by 20 minutes of thermal annealing at 100 °C. All these process steps have been performed inside a nitrogen glovebox, in order to avoid any contamination with oxygen and moisture. Figure 21 shows a schematic representation of the different architectures used, with all the specific layers of material deposited.

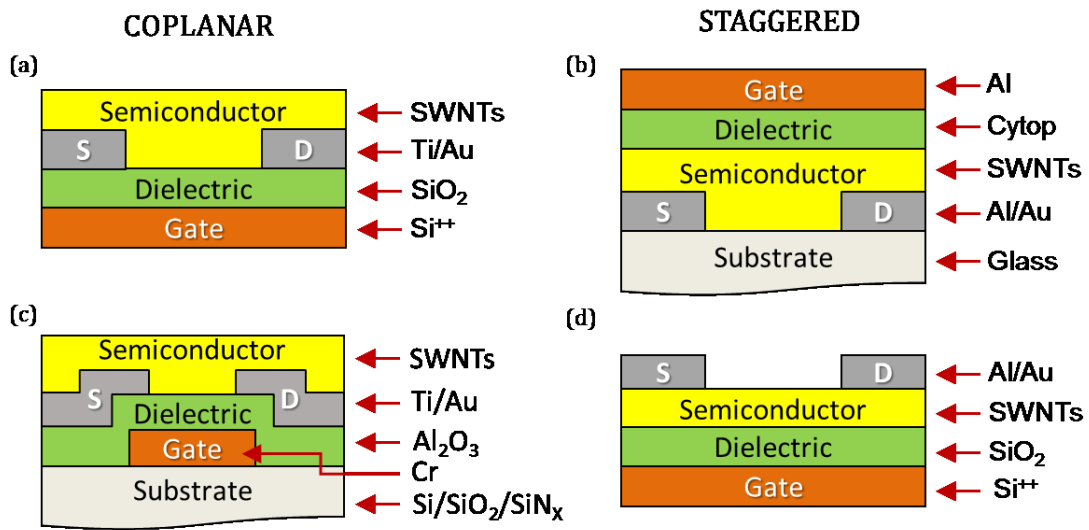


Figure 21: Schematic representation of the different device architectures and materials used. (a) Bottom-gate coplanar pre-patterned substrate with SiO₂ dielectric and Ti/Au source and drain contacts is shown. (b) Structure of staggered top-gate device with CYTOP dielectric, Al/Au source and drain contacts and Al gate electrode. (c) Coplanar bottom-gate pre-patterned substrate with Al₂O₃ dielectric, Ti/Au source and drain contacts and Cr gate electrode is shown. This device has been fabricated by Dr Luisa Petti at ETH Zurich. (d) Structure of staggered bottom-gate device with SiO₂ dielectric and Al/Au source and drain contacts.

Devices shown in Figure 21(a), (b) and (d) have been fabricated at Imperial College London. Slightly different is the case of TFT shown in Figure 21(c) and of unipolar and complementary inverters, where ALD deposited Al₂O₃ dielectric was used. These coplanar bottom-gate pre-patterned devices have been fabricated by Dr Luisa Petti at ETH Zurich, under the supervision of Prof. Gerhard Troëster. These bottom-gate coplanar TFTs and inverters were fabricated on a 4" silicon substrate

with 1 μm thermally grown SiO_2 acting as isolation layer and 500 nm SiN_x acting as adhesion layer, deposited by plasma-enhanced chemical vapour deposition (PECVD). Next, a 30 nm-thick Cr layer was e-beam evaporated and later patterned to form the bottom-gate electrodes via standard photolithography. Then, the Al_2O_3 gate dielectric ($t = 50$ nm, $C_i = 168$ nF/cm²) was deposited by ALD at 150 °C. Source and drain electrodes consisting of 10 nm/50 nm of Ti/Au were e-beam evaporated and patterned using a lift-off process.²¹ For logic circuits, the Cr gate itself was used to form the load resistor, therefore eliminating the requirement for further process steps. Flexible devices were fabricated using the same process steps but on free-standing polyimide foils instead of silicon substrates, and they were attached to a carrier glass in order to facilitate the deposition of SWNTs and later detached for mechanical and electrical characterization.²¹ More complex was the fabrication of complementary inverters, where SWNTs were integrated on the same coplanar bottom-gate substrate with n-type metal oxides such as indium-oxide (InO_x) and indium-gallium-zinc-oxide (IGZO). In order to deposit both semiconductors side by side and avoid any contamination between them, the metal oxide was first deposited. Later, it was patterned only in the n-channel and covered with an encapsulation layer acting as a protective layer from SWNTs.²³ Prior to semiconductor deposition, the substrates were diced into chips of 1.5×1.5 cm², cleaned by ultra-sonication in acetone and in IPA baths for 5 minutes each, and finally exposed to UV-ozone for 20 minutes.

3.3 Material and Electrical Characterization

In this section, the various characterization techniques used for the analysis of SWNT films and devices are described. The methods can be divided into two primary areas consisting of material characterization techniques including UV-Vis optical absorption spectroscopy, atomic force microscopy (AFM), and conductive atomic force microscopy (C-AFM), and electrical characterization methods such as current-voltage measurements.

3.3.1 UV-Vis Optical Absorption Spectroscopy

The first characterization technique to be performed on the SWNT dispersions has been the UV-Vis optical absorption spectroscopy. In absorption spectroscopy, a beam in the UV-Vis-NIR spectral range scans the sample. Some wavelengths of the source spectrum are transmitted through the sample and detected by the instrument, while other wavelengths are absorbed by the sample, and do not produce any detection signal. The sample transmittance (T) is defined as $T = P/P_0$, where P is the output power and P_0 is the incident power, as shown in Figure 22.

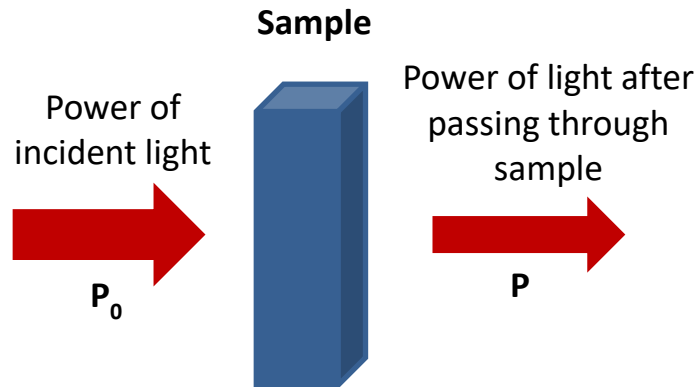


Figure 22: Schematic of light absorption through a sample, where P_0 is the incident power and P is the output power.

The sample absorbance (A) is defined as the logarithm of the reciprocal of the transmittance:

$$A = -\log\left(\frac{P}{P_0}\right). \quad (19)$$

An absorbance spectrum is usually plotted in absorbance unit [Abs], often called optical density [OD], and it depicts which wavelengths are absorbed by the sample (peaks) and which are transmitted (valleys) and therefore detected by the instrument. Optical density is related to the material concentration in the solution by the Lambert-Beer law:

$$A = \epsilon lc, \quad (20)$$

where A [OD] is the absorbance, ϵ [$\text{L}\cdot\text{mol}^{-1}\cdot\text{cm}^{-1}$] is the molar absorptivity, l [cm] is the light path, and c [$\text{mol}\cdot\text{L}^{-1}$] is the concentration of the material in the solution. By using equation (20), once the absorbance is measured and the molar absorptivity and light path are known, the concentration of the material in the solution can be obtained.⁸⁵ UV-Vis spectroscopy is commonly used in analytical chemistry to quantify the concentration of different materials. However, this technique is not suitable to determine the minority concentration in a sample with a single majority species at a high concentration, because absorption peaks become impossible to distinguish.

The basic parts of a spectrophotometer include a light source, a holder for the sample, a diffraction grating in a monochromator to separate the different wavelengths of light, and a detector. The Shimadzu UV-2600 spectrophotometer was used, equipped with an integrating sphere unit and a deuterium/halogen lamp with wavelength range between 220 nm and 1400 nm. Light path inside the UV-Vis spectrophotometer starts from the lamp and is then directed onto the monochromator, the sample and finally towards the detector. Both films and solutions can be analysed, and the operation mode can be set to absorption, transmittance and reflectance. This spectrophotometer was used to check the quality and the concentration of the SWNT dispersions used to fabricate devices.

Some of the spectra shown in the Experimental Results chapter have been measured at Imperial College London, while some others have been measured by Dr Florian Späth and Miss Imge Namal at Würzburg University, under the supervision of Prof Tobias Hertel, as part of a collaboration within the EU-FP7 project POCAONTAS.

3.3.2 Atomic Force Microscopy

Atomic force microscopy (AFM) is a high resolution scanning probe microscopy technique with demonstrated atomic resolution.^{86,87} The AFM consists of a cantilever with a sharp tip at its apex, also called the probe, which is raster scanned over the sample surface. By monitoring the movement of the probe, a 3D image of the surface can be reconstructed. The cantilever is typically made of silicon or silicon nitride and the probe has a radius of curvature of few nanometres. When the tip is brought close to the sample surface, a number of different forces may operate. Typically, the forces contributing most to the deflection of the cantilever are the Coulomb and van der Waals interactions. The Coulomb interaction is a strong, short-range repulsive force that arises from the electrostatic repulsion between the electron cloud of the tip and sample. The van der Waals interactions are instead longer-range attractive forces that arise from temporary fluctuating dipoles. As the tip is brought towards the sample, van der Waals forces cause attraction. However, as the tip-sample separation is further reduced, the repulsive Coulombic forces become dominant and the cantilever is deflected. Figure 23 shows the force-distance curve resulted from the combination of Coulombic and van der Waals forces.

The deflection of the cantilever is detected using a laser beam. A laser diode is focused onto the back reflective surface of the cantilever, and is reflected onto a photodetector, which is position sensitive and usually has four sectors. The vertical deflection of the cantilever is given by the difference in light intensity measured in the upper and lower sectors, while the lateral deflection of the cantilever is measured by the difference between the left and right sectors of the photodetector, as shown in Figure 24.

AFM has several different modes of operation depending on the application and the sample, but the most common ones are contact-mode and tapping-mode. In contact-mode, the tip is brought into contact with the surface and the detector monitors the changing cantilever deflection. The force in this mode of operation is calculated using Hooke's law:

$$F = -kx, \quad (21)$$

where x is the cantilever deflection and k is its spring constant. The feedback circuit adjusts the probe height in order to maintain a constant force, and hence a constant cantilever deflection, known as the deflection setpoint.

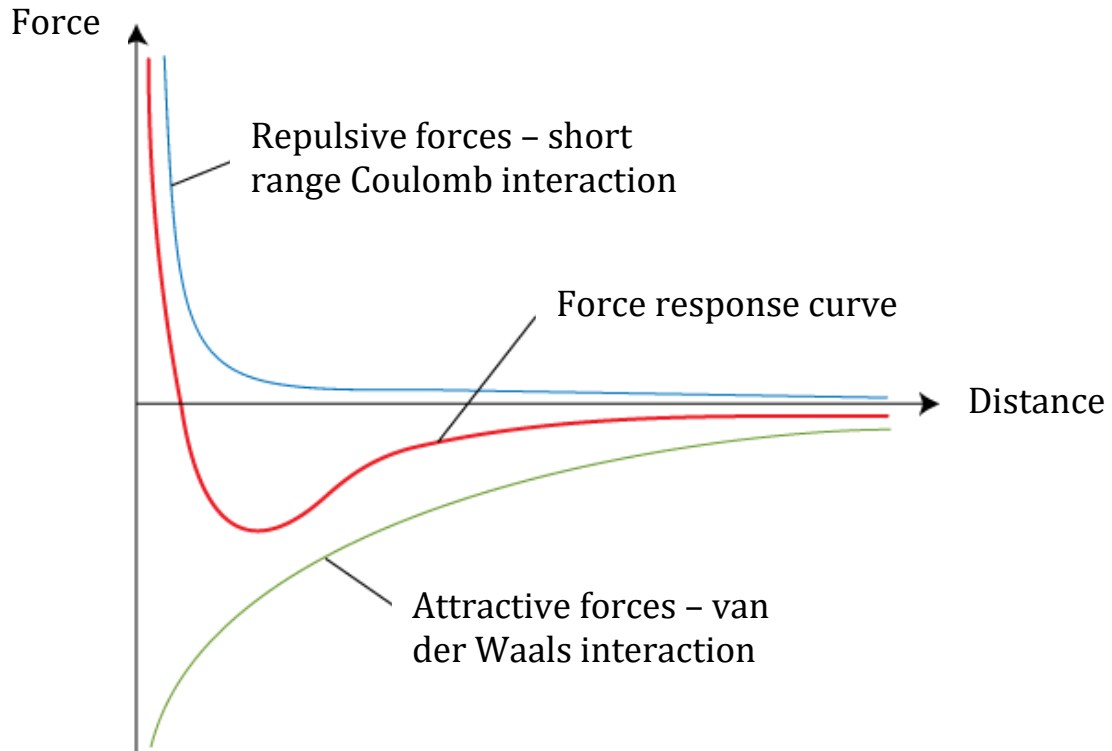


Figure 23: Schematic representation of the force-distance curve given by the combination of Coulomb and van der Waals interactions.⁸⁸

In tapping-mode (AC mode), the cantilever oscillates slightly below its resonant frequency. When the tip approaches the surface, the oscillation is damped by the interacting forces, and hence changes in the oscillation amplitude can be used to measure the distance between the tip and the surface. The feedback circuit in this case adjusts the probe height in order to keep constant the amplitude of oscillation, known as the amplitude setpoint.

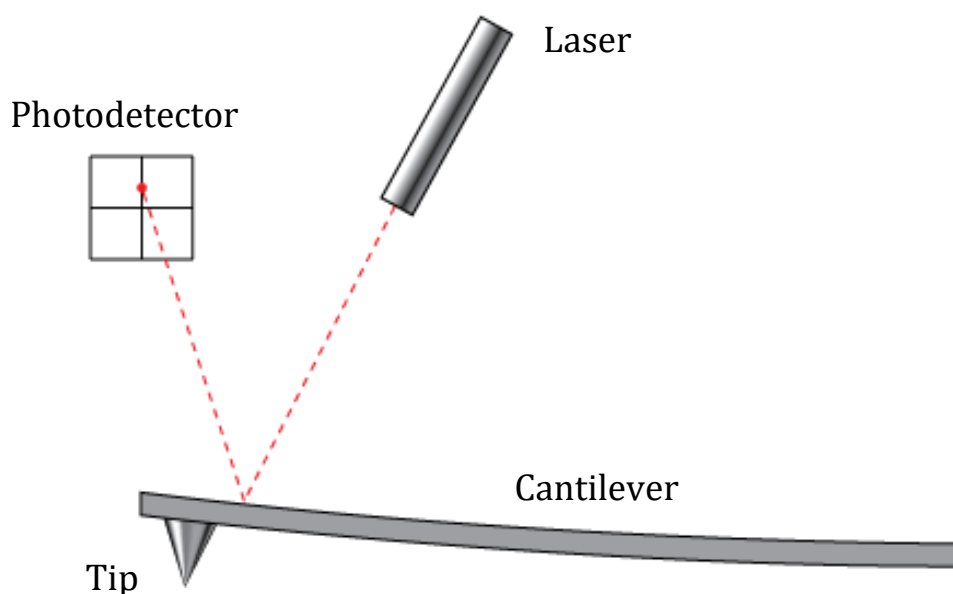


Figure 24: Schematic representation of the laser beam reflected from the cantilever onto the four-sector photodetector.⁸⁹

The Agilent 5500 scanning probe microscope was used, with a 980 nm IR diode laser, piezo scanner with 10 μm^2 scanning area, and nose assembly for AC and contact modes of operation. Budget Sensors Tap300Al-G silicon probes were used, with a spring constant of 40 Nm^{-1} and a probe-radius < 10 nm. This AFM was used to characterize the surface of SWNTs films and obtain parameters such as nanotube length, surface coverage, surface density, and surface roughness.

All the AFM images shown in the Experimental Results chapter have been obtained at Imperial College London.

3.3.2.1 Surface Coverage Analysis of Cylindrical Nanoparticles with AFM¹

Quantitative nanoscale evaluation of surface coverage of a certain material deposited over a substrate is a fundamental requirement for many modern surface science applications. Typically, such characterization is performed by scanning electron microscopy (SEM) or transmission electron microscopy (TEM).⁴² However, these techniques are destructive towards some soft samples, they need high vacuum, they are very expensive and, especially SEM, it suffers from surface

¹ Text and figures within this section have been partially reprinted from Bottacchi F. *et al.*, *Rev. Sci. Instrum.*, submitted (2016).¹¹⁵

charging and it provides at best semi-quantitative information about material surface coverage. Recently, optical methods such as sum frequency generation,⁹⁰ infrared spectroscopy,^{91,92} second harmonic generation^{93–95} or fluorescence-based techniques^{96,97} have introduced significant advantages over conventional particle-beam and X-ray diffraction spectroscopy, due to their surface sensitivity, spatial resolution, non-destructive interaction with soft samples and ambient operating conditions under atmospheric pressure. Another class of techniques that possess precisely these desired characteristics is the one of scanning probe techniques (SPM), comprised of atomic force microscopy (AFM),^{86,87} magnetic force microscopy (MFM),^{98–101} scanning tunnelling microscopy (STM),^{102–105} kelvin force microscopy (KFM),^{106–110} and scanning near-field optical microscopy (SNOM).^{111–114} These SPM techniques have so far been used for morphological, magnetic, electrical, and optical characterization of the sample surface with nanoscale spatial accuracy. However, none of these has been used to quantify and spatially map the surface coverage.

In this section, a novel method used to quantify the surface coverage of cylindrical nanostructures is presented. Material systems like carbon nanotubes (SWNTs) and silver nanowires (Ag NWs), deposited from solution onto different substrates, have been analysed by exploiting topographic information acquired via standard tapping-mode AFM. A statistical model of the cylindrical nanostructure's height density has been developed as a function of its diameter distribution and used to extract the coverage coefficients of all measured height configurations of the material deposited with a random distribution over the substrate.¹¹⁵

Statistical Height Models²

The statistical model of the height variable (y) of the cylinder with a random diameter requires the derivation of the joint probability density function¹¹⁶ between the horizontal position x of the AFM probe and the random diameter (y). To this end, the following assumptions have been formulated:

² The statistical model has been developed by Mr Stefano Bottacchi as part of a collaboration.

-
1. The random variable $\underline{x}$ is uniformly distributed in the interval $|x| \leq y/2$ with the following conditional probability density $f_{\underline{x}|\underline{y}}(x) = \begin{cases} 1/y, & |x| \leq y/2 \\ 0, & \text{elsewhere} \end{cases}$.
 2. The joint density $f_{\underline{xy}}(x, y)$ is given by the product of the conditioned density $f_{\underline{x}|\underline{y}}(x)$ with the probability density $f_{\underline{y}}(y)$ of the diameter $\underline{y}$.¹¹⁶
 3. The height density function $f_{\underline{z}}(z)$ of the cylindrical cross-section with random diameter $\underline{y}$ is then obtained integrating the diameter density $f_{\underline{y}}(y)$ with the proper surface weight function:

$$f_{\underline{z}}(z) = \int_{I_y(z)} \frac{2z-y}{y\sqrt{yz-z^2}} f_{\underline{y}}(y) dy, \quad z \in I_z. \quad (22)$$

It is important to remark that for every diameter density, the height density function in equation (22) is normalized. The general equation (22) of the height density function of cylindrical structures is now applied to the deterministic, uniform and Gaussian-Harmonic random diameter distributions.

The deterministic diameter is modelled with an impulsive density located at the diameter value d . From the general height density function equation (22), the height density of a cylinder with the deterministic diameter is given by:

$$f_{\underline{y}}(y) = \delta(y-d) \Rightarrow f_{\underline{z}}(z) = \begin{cases} \frac{1}{d} \frac{2z-d}{\sqrt{dz-z^2}}, & \frac{d}{2} \leq z \leq d \\ 0, & z \leq \frac{d}{2} \cup z \geq d \end{cases}. \quad (23)$$

Figure 25 shows the computed height density (equation (23)) of the cylindrical nanoparticle with a deterministic diameter of 80 nm. Due to the singularity at the diameter's height, the density function of the deterministic diameter can be approximated by the Delta distribution.

The uniform diameter is modelled with a constant density function centred on the nominal value d , with the full-width specified by the tolerance Δ , as indicated in the following equation:

$$f_y(y) = \begin{cases} 1/\Delta, & |y-d| < \Delta/2 \\ 0, & \text{elsewhere} \end{cases}. \quad (24)$$

The height density of the cylinder with a uniform diameter with nominal value d , and tolerance Δ is obtained by substituting equation (24) into the general equation (22).

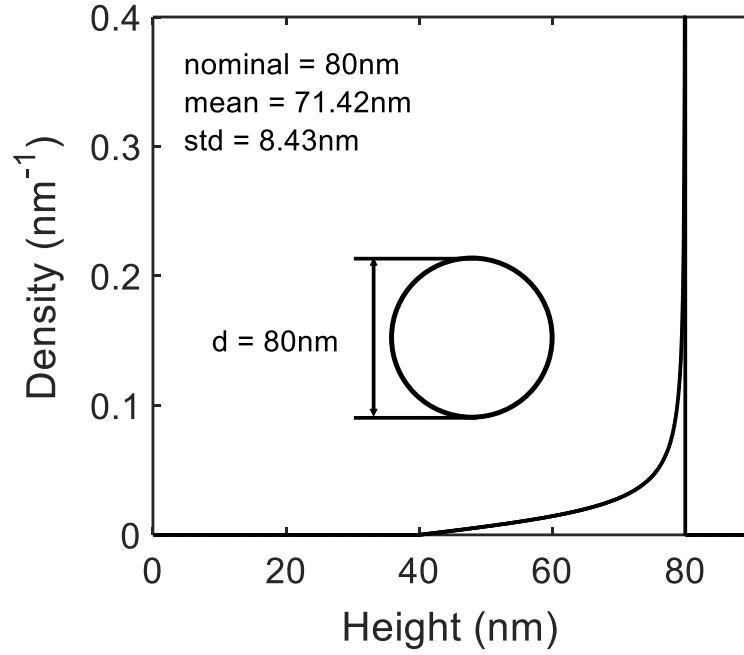


Figure 25: Simulation of the height density function of a cylinder with a deterministic diameter of 80nm. The density is identically zero for any height below half-diameter.

Figure 26 shows the simulated plot of the height density function of several cylindrical nanostructures with the same nominal diameter and uniform distribution but with different tolerances. By reducing the tolerance, the height density approaches the case of the deterministic diameter shown in Figure 25.

The Gaussian-Harmonic probability density function is a generalization of the Rayleigh probability density.

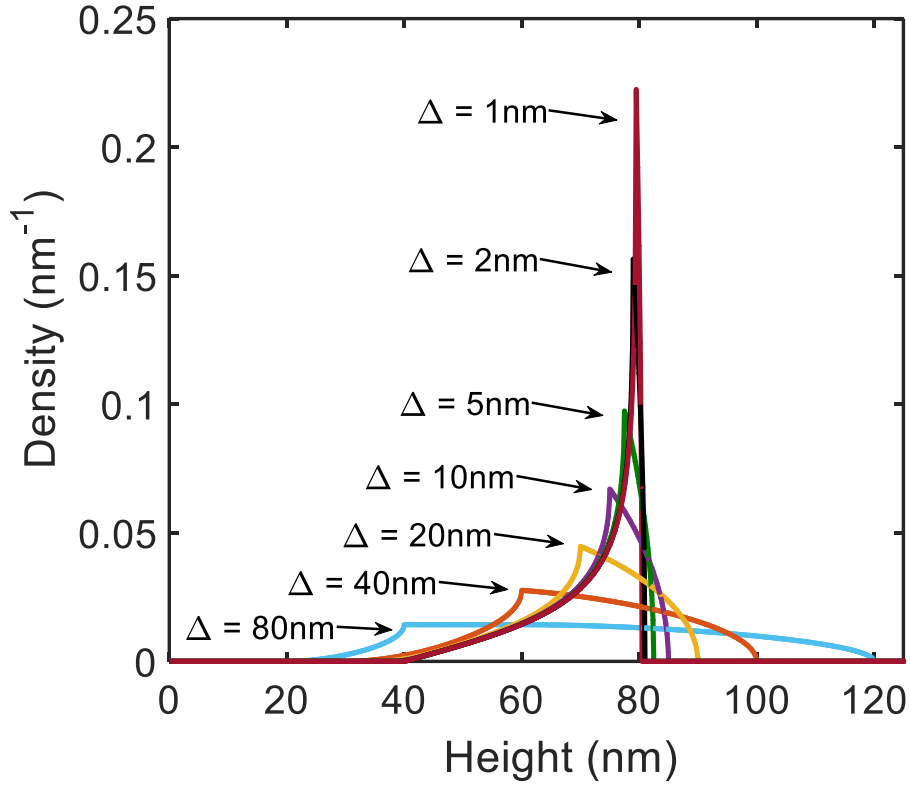


Figure 26: Simulation of the height densities of cylinders with uniform diameters. All curves refer to the same nominal diameter $d = 80\text{nm}$ but with different tolerances Δ .

With some calculations, the following density function of the Gaussian-Harmonic diameter can be found:

$$f_{\underline{y}}(y) = \frac{1}{4\sigma^2} y e^{-\frac{y^2 + d^2}{8\sigma^2}} I_0\left(\frac{yd}{4\sigma^2}\right) \quad , \quad y \geq 0, \quad (25)$$

where σ is the standard deviation, d is the diameter, and I_0 is the modified Bessel function of first kind and zero order. The mean value is always larger than the peak position and it approaches the peak for very large ratios d/σ . The simulation of the height densities with the Gaussian-Harmonic diameter distribution are shown in Figure 27. Several height density profiles with a fixed nominal diameter of 80nm have been plotted versus different tolerances, characterized by the parameter σ_d . When the ratio d/σ_d becomes relatively large, the density profile approaches the same highly peaked shape as the height density obtained from the deterministic diameter shown in Figure 25. At infinitesimal values of the standard deviation, the Gaussian-Harmonic density approaches the case limit of the Delta distribution.

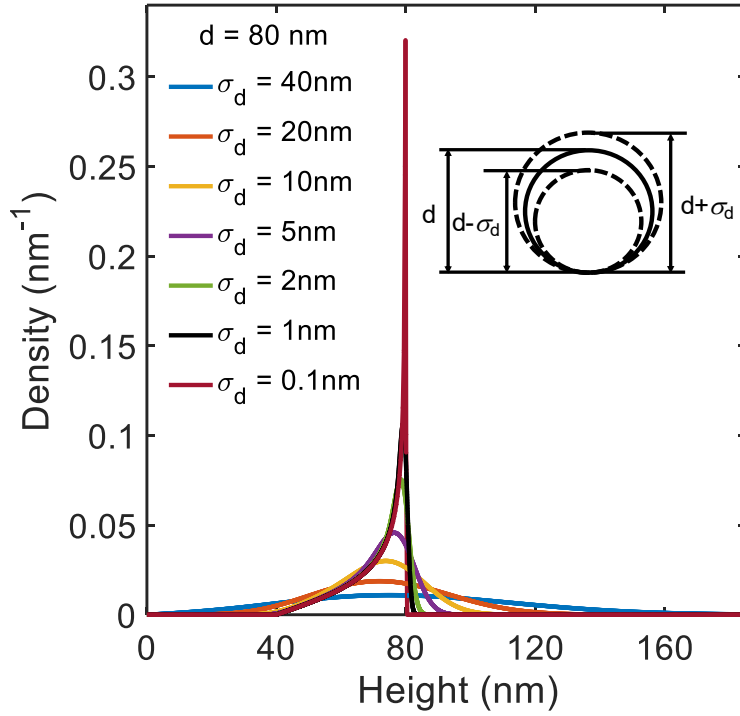


Figure 27: Simulation of the height density for the Gaussian-Harmonic diameter density function at decreasing values of the standard deviation σ_d . The height density at relatively large tolerance becomes almost symmetric and it is well approximated by a Gaussian profile. Decreasing the standard deviation, the height density begins peaking, losing gradually the symmetry and approaching the highly-peaked profile obtained by the Delta distribution of the diameter density.

Coverage Master Equation³

It is assumed that all cylindrical elements have the diameter distributed with the same known density function $f_y(y)$ that can be deterministic, uniform, or Gaussian-Harmonic, and the height density $f_z(z)$ of the single circular cross-section is a known function of the diameter statistic, as shown in equation (22). The events $\{j\text{-stacked cylinders}\}$ and $\{k\text{-stacked cylinders}\}$ are statistically independent, with probabilities of occurrence respectively c_j and c_k , known as partial coverage. The total height $\hat{z}^{(k)}$ of k -stacked cylinders, without the substrate contribution, is a random variable given by the sum of the height z_i , $i = 1 \dots k$ of each element of the cylinders' aggregate, while the heights z_i are mutually statistically independent random variables, distributed

³ The mathematical formulation of the coverage master equation has been developed by Mr Stefano Bottacchi as part of a collaboration.

with the same density function $f_v(z)$. The conditioned density function $f_{v|k}(z)$ of the height variable $\hat{z}^{(k)}$ of k -stacked cylinders is given by $k - 1$ times the self-convolution of the individual density $f_v(z)$. The total height $\underline{z}^{(k)}$ of k -stacked cylinders placed upon the substrate is given by the sum of the height $\hat{z}^{(k)}$ of the k -stacked cylinders with the substrate height $\underline{z}_s$. The height $\underline{z}_s$ of the substrate and the height $\underline{z}_i$ of each cylinder in the stacking aggregate form a set of mutually statistically independent random variables. The conditioned density function $f_{\underline{z}|k}(z)$ of the total height $\underline{z}^{(k)}$ of k -stacked cylinders placed upon the substrate is given by the convolution of the height density $g(z)$ of the substrate with the conditioned density $f_{v|k}(z)$. The total height density $f_{\underline{z}}(z)$ of the entire cylinders' population stacked in N different configurations and placed upon the substrate, is given by the linear combination of $N + 1$ conditioned probability density functions, each weighted by the probability of the corresponding stacked configuration:

$$f_{\underline{z}}(z) = \sum_{k=0}^N c_k g(z) * f_{v|k}(z) \quad (26)$$

The probability c_k of the event $\{k\text{-stacked cylinders}\}$ is the coverage coefficient for that event, i.e. how many k -stacked cylinders are present over the entire cylinders' population. The coverage coefficients c_k must satisfy the normalization condition for the total probability. In particular, the coverage coefficient c_0 assumes the meaning of the *uncovered* substrate percentage. Accordingly, the sum of all coverage coefficients between the single layer and the N -stacked layer configurations represents the total coverage C of the cylindrical nanoparticles placed over the given substrate, as shown in the following equation:

$$C = \sum_{k=1}^N c_k = 1 - c_0. \quad (27)$$

From the coverage master equation (26), the total height density $f_{\underline{z}}(z)$ is given by the inverse Fourier transform of the linear combination, through the coverage coefficients c_k , of the products between the Fourier transform of the height density of the Gaussian substrate with the $k - th$ power of the Fourier transform of the

height density of the circular cross-section, corresponding to the selected diameter statistic:

$$\left. \begin{array}{l} g_u(z) \xleftrightarrow{\mathfrak{F}} G_u(\xi) \\ f_z(z) \xleftrightarrow{\mathfrak{F}} F_z(\xi) \end{array} \right\} F_z(\xi) = G_u(\xi) \sum_{k=0}^N c_k F_v^k(\xi) \quad (28)$$

The unknown coefficients $c_0, c_1 \dots c_N$ of the coverage master equations (26) or (28) are the solution of the system of $N + 1$ independent linear equations obtained sampling the measured height density B_j at specified height positions. The positions of the height samples can be chosen arbitrarily; however, a possible choice is to sample at integer multiples of the nominal diameter. In order to solve the system and find the coverage coefficients c_k , the following system matrix must be solved:

$$\sum_{k=0}^N a_{jk} c_k = B_j, \quad j = 0, 1 \dots N \quad \rightarrow \quad \mathbf{A} \mathbf{c} = \mathbf{B}$$

$$\mathbf{A} = \begin{bmatrix} a_{00} & a_{01} & a_{0k} & a_{0N} \\ a_{10} & a_{11} & a_{1k} & a_{1N} \\ a_{j0} & a_{j1} & a_{jk} & a_{jN} \\ a_{N0} & a_{N1} & a_{Nk} & a_{NN} \end{bmatrix}, \quad \mathbf{c} = \begin{bmatrix} c_0 \\ c_1 \\ c_2 \\ c_3 \\ c_k \\ c_N \end{bmatrix}, \quad \mathbf{B} = \begin{bmatrix} B_0 \\ B_1 \\ B_2 \\ B_3 \\ B_k \\ B_N \end{bmatrix}, \quad (29)$$

where $a_{jk} = f_{z|k}(z_s + jd) = \left[g_u(z) * f_{v|k}(z) \right]_{z=\bar{z}_s + jd}$, $a_{j0} = g_u(z_s + jd)$, $j, k = 0, \dots, N$,

represents the convolution between the Gaussian substrate and the conditioned density function sampled at integer multiples of the diameter d .

Experimental Verification

This method has been carefully verified experimentally on SWNTs and Ag NWs deposited from solution on SiO₂ and glass. Figure 28 shows (a) the topography image of a PFO/(7,5) SWNT network obtained with AFM in tapping-mode and (b) the corresponding measured (red line, directly with AFM) and extracted (blue line) normalized height densities, together with all the extracted coverage coefficients. It

is important to observe how well the extracted density with the uniform diameter model matches the measured density profile.

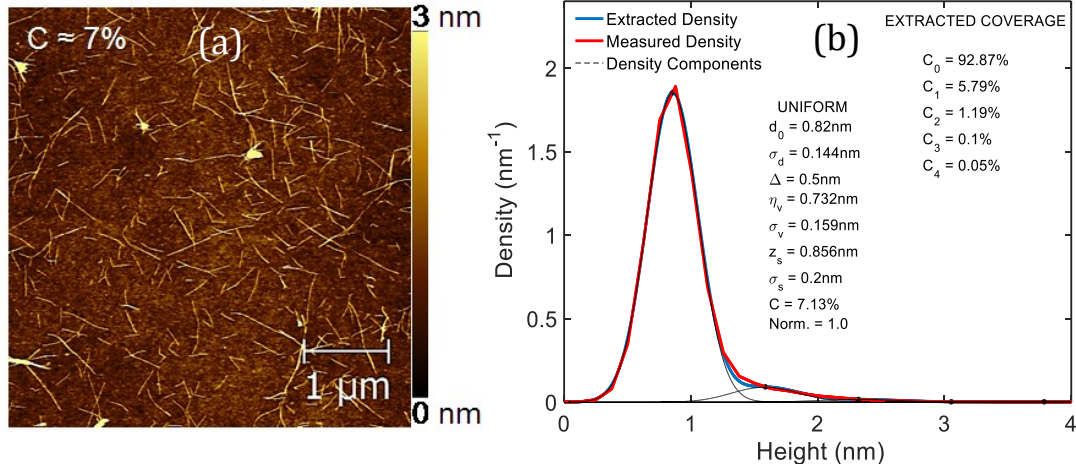


Figure 28: (a) Topography and (b) height density profile obtained with the AFM in tapping-mode on the solution-processed PFO/(7,5) SWNT network, randomly distributed over an SiO₂ substrate. The coverage spectroscopy solution assumes the uniform diameter statistic. The total coverage results $C = 7.13\%$, with dominant single-layer SWNT configurations with a corresponding coverage coefficient $c_1 = 5.79\%$.

The choice of the uniform diameter model is justified to account for additional polymer partially wrapped around some nanotubes, making their effective diameter a statistical variable with uniform distribution. The choice of the diameter statistical model, i.e. deterministic, uniform or Gaussian-Harmonic, depends on the result of the fitting procedure. Some measurements fit better assuming the simpler diameter deterministic model, assuming that the SWNT population is almost free from any residual polymer or aggregates. Both uniform and Gaussian-Harmonic diameter distributions represent either residual polymer contamination or heterogeneous SWNT population with multiple diameters.

Another example is shown in Figure 29, where the same coverage analysis has been performed on a single Ag NW deposited from solution on a glass substrate. In this case, the simulations of the density function of the Gaussian-Harmonic diameter (black line), the Gaussian substrate height (red line), the stand-alone Ag NW height (blue line) and the total height of the Ag NW placed onto the glass substrate (purple line) have been plotted together in Figure 29(a), whose inset shows the AFM topography image of the single Ag NW obtained with the AFM in tapping-mode. Figure 29(b) instead shows the corresponding measured (red line, directly with

AFM) and extracted (blue line) normalized height densities, together with the extracted coverage coefficients. Also for this case, the extracted height density perfectly follows the measured density both of the glass substrate and of the nanowire with a diameter $d \approx 75.7$ nm.

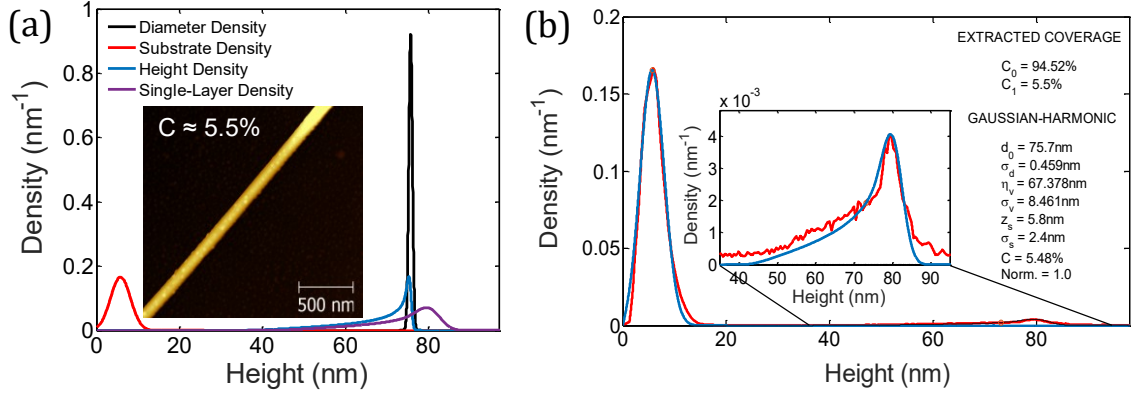


Figure 29: (a) Simulation of the density function of the Gaussian-Harmonic diameter (black line), the Gaussian substrate height (red line), the stand-alone Ag NW height (blue line) and the total height of the Ag NW placed onto the glass substrate (purple line). The inset shows the AFM topography obtained with the AFM in tapping-mode. (b) Measured (red line) and extracted (blue line) height density profiles with the Gaussian-Harmonic diameter model. The total coverage is $C = c_1 = 5.5\%$ and corresponds to the coverage of the Ag NW deposited in the scanned area.

Finally, it is important to remark that all scanning probe techniques present some native distortion when measuring highly-resolved vertical profiles of isolated nanoparticles, such as cylindrical nanoparticles with large diameters placed upon very low roughness surfaces, like SiO₂, or when measuring very small structures such as SWNTs, in which case the lateral shape of the probe contributes equally to the measurement as well as the very end of the probe. This is due to different probe resolutions available along vertical and lateral axes, which distort the profile image and could generate coverage coefficients larger than expected. Unless the shape of the probe is known and properly de-convolved from the acquired data, the measured height profile will result distorted, mainly in the transversal direction, showing an artificial elliptical cross-section instead of the expected circular one.

This method has been used to fully characterize the surface properties of many SWNTs samples, and it will be mentioned later in the Experimental Section.

3.3.3 Conductive Atomic Force Microscopy

Another imaging technique is the conductive atomic force microscopy (C-AFM), in which a conductive tip is brought into contact with the sample surface, and topographic and electrical signals are simultaneously acquired. In C-AFM, the sample must be biased with respect to the conductive tip and the current flows from the electrode to the tip (or vice versa) through the sample, either laterally on its surface or vertically in the semiconductor, depending whether the electrode is deposited on the sample surface or below it. By applying a fixed bias between the C-AFM probe and the metal electrode in contact with the sample, the simultaneous acquisition of both topography and surface current is possible. In the simplest case, the applied electric field is expected to be inversely proportional to the distance between the scanning C-AFM probe and the remote electrode. In lateral C-AFM, a semiconducting material is deposited over an insulating substrate and scanned with a metal-coated probe in contact-mode.¹¹⁷ This technique is particularly useful to characterize lateral current pathways in OFET channels between source and drain contacts. In vertical C-AFM instead, a semiconducting material is deposited over a conducting substrate and scanned with a metal-coated probe in contact-mode.¹¹⁸ This other version of the C-AFM is more useful to characterize bulk currents flowing vertically from the anode to the cathode of organic solar cells.

The Agilent 5500 scanning probe microscope was used, with a 980 nm IR diode laser, piezo scanner with 10 μm^2 scanning area, and nose assembly for current-sensing operation with 1 nA/V sensitivity. Platinum-coated Mikromasch CSC17/Pt probes were used in this case, with a spring constant in the range of 0.06 Nm^{-1} – 0.4 Nm^{-1} and a coated probe-radius < 30 nm. A bias of -5 V was applied to the sample electrode, while the conductive probe was held at ground, enabling hole injection from the probe and extraction through the negative biased electrode. The lateral C-AFM was used to electrically characterize the surface of SWNTs films and obtain intrinsic parameters of the SWNT network such as current, resistance, resistivity, and degree of alignment.

All the C-AFM images shown in the Experimental Results chapter have been obtained at Imperial College London.

3.3.4 Current-Voltage Measurements

Typically, FET performance is evaluated by the analysis of the experimentally acquired current-voltage characteristic (Figure 13) and the extraction of electrical parameters, as it is described in section 2.4.4. For the required measurements to be taken, a semiconductor parameter analyser (SPA) was used, in combination with a mechanical probe station. The probe station utilizes micromanipulators that allow the precise positioning of thin needles on the surface of a device electrode. It was placed either under vacuum, in an inert environment or in ambient environment, depending on the requirements of the device/material being tested. Moreover, either room temperature and low-temperature measurements with liquid nitrogen were possible with this setup. The device under test was placed on a chuck in the probe station and contacts were made using fine metal needles, in order to allow for an accurate and good quality contact. Current-voltage measurements at each of the terminals (source, drain, and gate) were recorded and saved into a spreadsheet file. For the measurement of logic circuits, the same system was used, but more source-measurement units (SMUs) were added, depending on the circuit design. For the characterization of a unipolar or complementary inverter, four SMUs were used for V_{DD} , V_{IN} , V_{OUT} , and GND.

In some cases, electrical characterization was performed while devices were subjected to tensile strain, in order to test their robustness to mechanical stress. During such bending tests, flexible devices on polyimide foils were attached onto a double-side adhesive tape and wound around metal rods of different radius, in order to apply tensile strain only parallel to the transistor channel.

For the characterization of SWNT FETs, an Agilent B2902A SPA was used, while for the characterization of unipolar and complementary inverters, a Keithley 4200-SCS SPA was used. These measurements were performed at room temperature, and the probe station was placed inside a nitrogen glovebox in order to avoid the interaction of carbon nanotubes with oxygen and moisture. All the devices shown in the Experimental Results chapter have been characterized and analysed at Imperial College London.

4 Experimental Results and Discussion

This chapter comprises of four sections, each describing an experimental result obtained during the PhD. More specifically, results on SWNT network charge transport percolation have been partially adapted with permission from Bottacchi F. *et al.*, *Small* **12**, 4211-4221 (2016),⁴⁵ results on SWNT low-voltage FETs from Bottacchi F. *et al.*, *Appl. Phys. Lett.* **106**, 193302 (2015),²¹ and results on SWNT logic circuits from Petti L. *et al.*, *IEEE International Electron Devices Meeting* (2014).²³

4.1 Percolation Study of PFO/(7,5) SWNT Networks⁴

4.1.1 Introduction

The main purpose of the percolation study of PFO/(7,5) SWNT networks is to assess and quantify the residual metallic content present in the polymer-sorted (7,5) SWNT dispersion. The SWNT current percolation is investigated using a combination of electrical field-effect measurements and scanning probe techniques, which enables the quantification of additional key network parameters such as resistivity, surface density, surface coverage and degree of alignment. Field-effect transistors based on a dense random network of polymer-sorted (7,5) SWNTs deposited from solution at room temperature have been fabricated with different gate dielectrics and device geometry. By using the 2D homogeneous random-network stick percolation model,^{81,119} the drain current scaling behaviour in the linear operating regime (low V_G) of the transistors as a function of the channel length L_C is analyzed and the residual metallic nanotubes are quantified. The surface topography of the as-processed networks is studied via atomic force microscope (AFM), and the current percolation in the networks is investigated with nanoscale spatial accuracy using the lateral conductive atomic force microscope (C-AFM).^{117,118,120}

It has been previously mentioned that, although on one hand substantial progress has been made to optimize SWNT sorting and enrichment techniques, on the other

⁴ Text and figures within this chapter have been partially reprinted from Bottacchi F. *et al.* *Small* **12**, 4211-4221 (2016), with the permission of John Wiley and Sons (see Appendix 7.1).⁴⁵

hand the ability to accurately characterize the residual metallic nanotube content in highly pure semiconducting samples remains a major challenge. A sensitive detection of metallic SWNTs is not possible by photoluminescence spectroscopy, and absorption spectroscopy is not suitable to determine the minority concentration in a sample with a single majority species at a high concentration, because absorption peaks become impossible to distinguish. The only spectroscopic technique that enables a sensitive metallic nanotubes quantification is Raman spectroscopy. However, there are many limitations and complications associated with this technique:

1. In order to resonantly excite the nanotubes, their diameter distribution must be known in order to choose the appropriate excitation wavelength. Hence, the nanotube diameter must be known *a priori*, and this can be a significant disadvantage because it does not allow the quantification of metallic content in a network of unknown carbon nanotubes chirality.
2. In order to produce maps of the radial breathing mode (RBM) region in both semiconductor and metal branches, a tunable source with many wavelengths must be used, but this setup is very sophisticated and most Raman setups have a limited number of wavelengths available.
3. The background from SWNT aggregates may be significant and this complicates the analysis.
4. Another complication regards the assessment of the G band line shape due to doping.
5. Some nanotube chirality, like the armchair tubes, may have no G⁻ band, so not all chiralities can be equally assessed with Raman spectroscopy.
6. Most importantly, Raman spectroscopy cannot be used to characterize metallic content in a sample with small diameters ($d < 0.8$ nm) or in a sample with a broad diameter distribution because peaks cannot be distinguished.

In conclusion, Raman spectroscopy is a useful technique to assess the metallic nanotube content in films and dispersions. However, it can be applied only on a limited range of nanotube samples with a known diameter distribution, and it requires a sophisticated Raman setup with a tunable source.^{43,44}

Here, optical and morphological characterization of PFO/(7,5) SWNT dispersions and films are discussed, followed by the electrical characterization of PFO/(7,5) SWNT FETs with several device architectures, the analysis of PFO/(7,5) SWNTs charge carriers' percolation using the 2D homogeneous random-network stick percolation model, and the investigation of PFO/(7,5) SWNTs conductivity pathways via C-AFM with nanoscale spatial accuracy.

4.1.2 Optical and Morphological Characterization

The PFO/(7,5) SWNT dispersion has first been optically characterized by absorption spectroscopy, as shown in Figure 30. The chemical structure of the polymer PFO is shown in the inset. The presence of two sharp absorption peaks at $\lambda = 1050$ nm and $\lambda = 655$ nm, corresponding respectively to the first (E_{11}) and second (E_{22}) excitonic sub-band transitions of the (7,5) single nanotube, is a strong evidence that nearly single chirality (7,5) SWNTs are present in the dispersion.⁴⁰

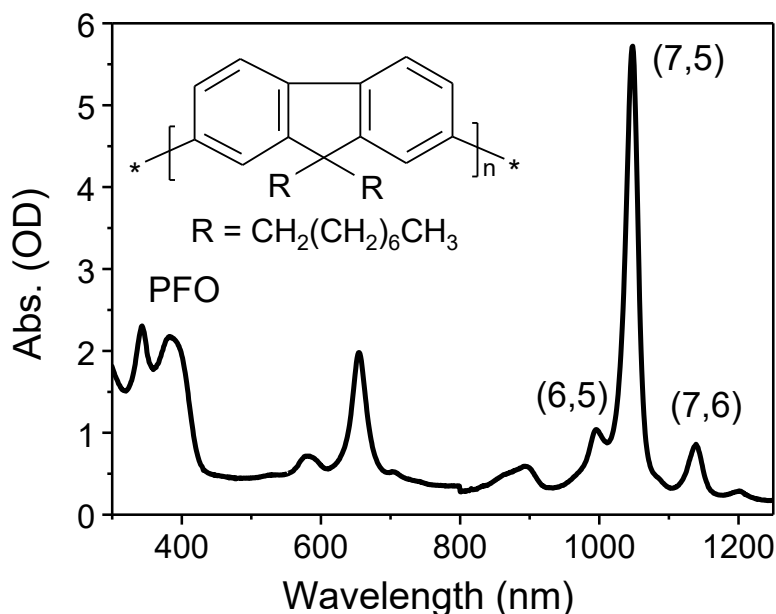


Figure 30: Absorption spectrum of the PFO/(7,5) SWNT dispersion in chlorobenzene. The two sharp peaks at $\lambda = 1050$ nm and $\lambda = 655$ nm respectively, correspond to the first and second excitonic sub-band transitions of the (7,5) nanotube chirality. The absorption between $340 \text{ nm} < \lambda < 380 \text{ nm}$ corresponds to the polymer PFO, whose chemical structure is shown in the inset. Two additional minor peaks are visible at $\lambda = 995$ nm and $\lambda = 1140$ nm, which are due to residual amounts of (6,5) and (7,6) nanotube chiralities, respectively. Most importantly, no absorption is visible in the metallic nanotubes range (450 nm – 550 nm).⁴⁵

Two additional smaller peaks are visible at $\lambda = 995$ nm and $\lambda = 1140$ nm, which are due to residual amounts of (6,5) and (7,6) semiconducting nanotube chirality, respectively,^{16,38} while the spectrum profile in the range of 340 nm – 380 nm corresponds to the absorption of the PFO. Moreover, there is no visible absorption in the range of 450 nm – 550 nm, which is where absorption from metallic nanotubes in the (7,5) diameter range would appear,^{38,40,41,121} clearly demonstrating the efficiency of using PFO as the dispersing polymer. However, as already mentioned, an exact quantification of the residual number of metallic nanotubes is not possible from the absorption spectrum and a more detailed analysis is needed.

The optical densities [OD] of the different nanotube chirality can be used to calculate the relative fractions present in the dispersion. In order to do so, Voigt line shapes must be fitted to the absorption peaks of (7,5), (6,5) and (7,6) nanotube chirality, the integral of the curves must be calculated, and finally the relative SWNTs concentration can be obtained using the integrated carbon nanotube optical cross-section and the following equation:

$$C_c = B \cdot \frac{(\Delta_{fwhm} \cdot OD)}{fd}, \quad (30)$$

where d is the thickness of the optical cell (1 cm), f is the C-atom oscillator strength specific for each chirality, $B = 5.1 \cdot 10^{-8}$ [mol cm/L nm] is a constant, and Δ_{fwhm} and OD are experimental values taken from the absorption spectrum of Figure 30. The relative nanotube concentrations obtained with equation (30) are: (7,5) SWNT $\approx$ 82%, (6,5) SWNT $\approx$ 8.9%, and (7,6) SWNT $\approx$ 9.1%.^{9,85}

Surface morphology of the spin-coated PFO/(7,5) SWNT networks has been studied by tapping-mode AFM. An exhaustive length characterization of the carbon nanotubes has been performed on an atomically-flat SiO₂ substrate with AFM in tapping-mode. In order to clearly distinguish and count single nanotubes, a diluted dispersion with an OD = 1 has been used to measure the nanotube lengths. Figure 31 shows the topography image of the PFO/(7,5) SWNT diluted network, where single carbon nanotubes are clearly distinguishable on the SiO₂ surface. From this AFM topography image 239 single nanotubes have been manually counted and their

length measured, obtaining an average nanotube length of 410 nm. Figure 32 shows the correspondent normalized histogram of the length distribution.

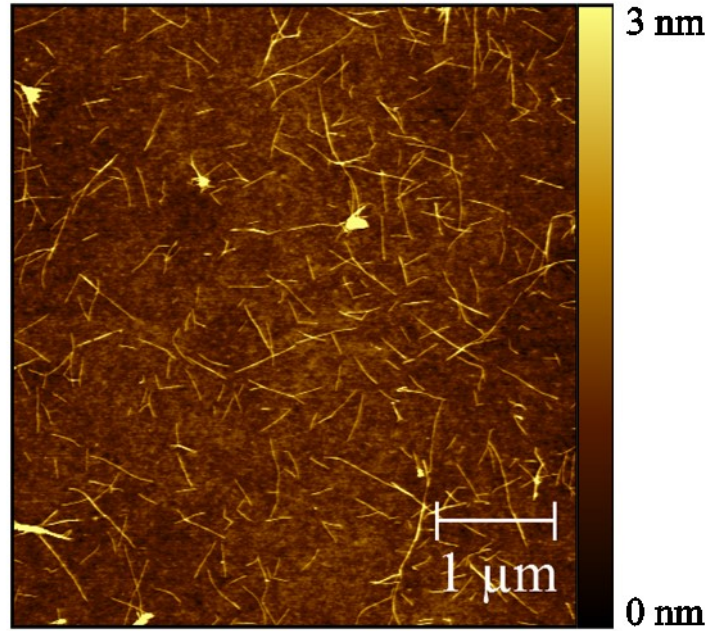


Figure 31: AFM topography image of a PF0/(7,5) SWNT diluted network spin-coated on a SiO₂ substrate. From this image 239 SWNTs have been counted and their length measured.⁴⁵

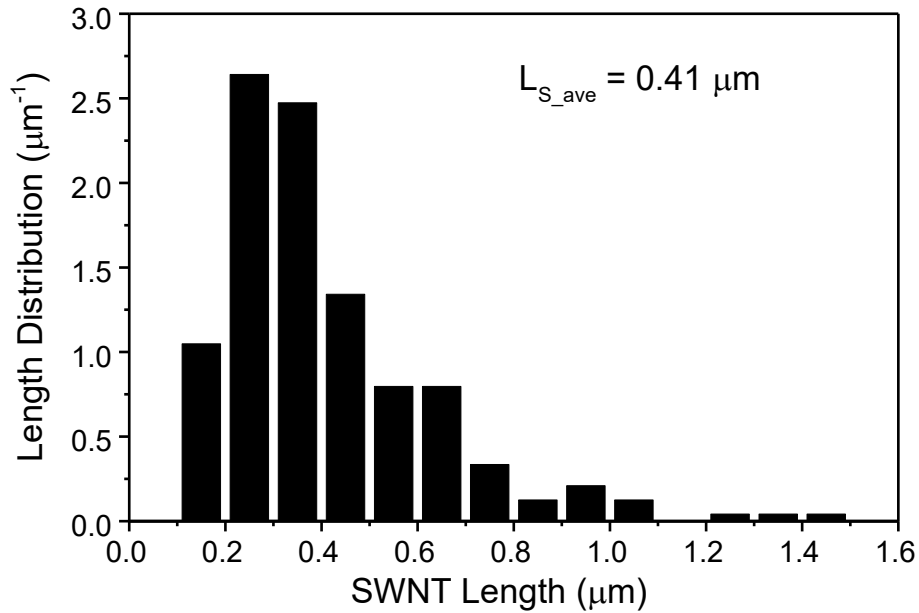


Figure 32: Histogram showing the normalized length distribution of the (7,5) SWNTs with the correspondent average value, taken from the topography image shown in Figure 30.⁴⁵

It is important to observe that the nanotube lengths are very broadly distributed between 100 nm and 1500 nm, thus making it very difficult to choose the most

representative length to be used in the analysis. Moreover, the presence of very short nanotubes can be attributed to the long sonication time essential to achieve a high level of nanotube dispersion, which is known to damage and break nanotubes. For the purpose of this percolation study, the longest nanotubes certainly dominate the transport in the FET channel over the shortest ones. Nonetheless, the average nanotube length of 410 nm has been used as the representative length for the percolation analysis, and the impact of different nanotube lengths has been examined by changing their value within the experimentally determined distribution shown in the histogram of Figure 32.

Figure 33(a) shows the AFM image of the surface topography of the PFO/(7,5) SWNT network deposited onto the SiO₂ gate dielectric surface in the bottom-gate FET, while Figure 33(b) shows a zoomed-in area of the same network where some larger bundles/nanotube aggregates are also visible.

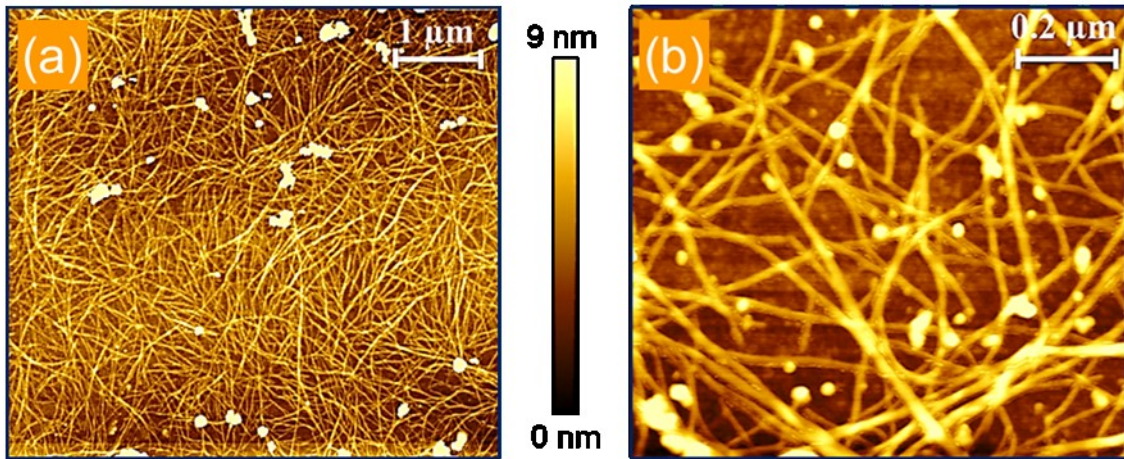


Figure 33: (a) AFM tapping-mode topography image of the spin-coated PFO/(7,5) SWNT network onto the SiO₂ gate dielectric surface. (b) Zoomed-in area of the image in (a), where bundles and SWNT aggregates are also visible.⁴⁵

In general, SWNTs appear to be randomly distributed over the entire SiO₂ surface without a preferential orientation. Finally, it is important to observe that the surface density of carbon nanotubes in Figure 33 is visibly well-above the percolation threshold of 34 SWNT μm⁻² ($\rho_{th} = 4.236^2/\pi L_s^2$, $L_s = 410$ nm),⁸⁰ and thus charge carrier mobility can be extracted using equations (11) and (12) within the gradual channel approximation.⁷¹

Further information on the SWNT network morphology is provided by the height counts distribution and the height cumulative distribution shown in Figure 34. Because SWNTs are deposited onto SiO₂, the total height counts distribution (black line) corresponds to the convolution of the independent height counts distributions of SiO₂ (red line) and of PFO/(7,5) SWNTs, respectively. Based on this assumption, and setting the (7,5) SWNT diameter to 0.82 nm,^{38,40} the height cumulative distribution (blue line) has been used in a simplified version of the coverage model explained in Section 3.3.2.1, obtaining the following surface coverage percentages: PFO/(7,5) SWNTs cover $\approx 58\%$ of the total surface area scanned, and SiO₂ covers $\approx 42\%$.

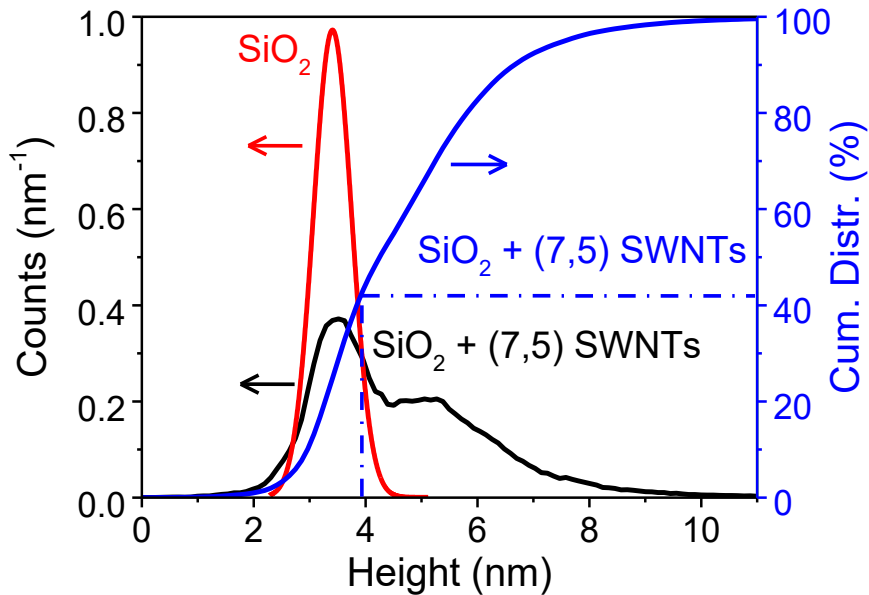


Figure 34: Normalized height counts distributions of bare SiO₂ (red line) and of PFO/(7,5) SWNTs on SiO₂ substrate (black line). Corresponding height cumulative distribution of PFO/(7,5) SWNTs on SiO₂ substrate (blue line) from which the relative coverages of PFO/(7,5) SWNTs and of SiO₂ have been determined.⁴⁵

We remark however that these values are only indicative of the upper limit for the total SWNTs coverage due to the following reasons:

1. The AFM probe has an atomic-scale vertical resolution and a lateral resolution comparable to the probe-radius so, the higher the resolution of the scan, the more accurate the extracted coverage value is.
2. The residual PFO present in the network most likely surrounds the nanotubes, potentially increasing their apparent diameter.

-
3. Small residual amounts of (6,5) and (7,6) carbon nanotubes with different diameters from the (7,5) nanotube are also present in our samples, providing some perturbation in the estimation of the single chirality SWNT surface coverage.
 4. The coverage value of 58% refers to the total amount of material deposited onto the SiO₂ substrate, and thus it includes carbon nanotubes, carbon bundles, carbon aggregates, and polymers.

Further information about the surface coverage evaluation through AFM topographic data is provided in Section 3.3.2.1, where an extensive description of this novel method is given.¹¹⁵

4.1.3 FET Architectures

PFO/(7,5) SWNT field-effect transistors have been fabricated both with top-gate bottom-contact and bottom-gate bottom-contact device architectures. Figure 35 shows the transfer and output characteristics of a top-gate FET with L_c/W_c of 50 $\mu\text{m}/1000 \mu\text{m}$ fabricated on glass with 900 nm of CYTOP as the gate dielectric, whose structure is shown in Figure 21(b).

The device exhibits strong ambipolar charge transport characteristics with balanced electron and hole currents and a channel current ON/OFF ratio about 10^4 . Gate leakage current results to be always at least two orders of magnitude lower than the ON current, while the small current hysteresis is attributed to atmospheric oxidants/adsorbates that are present within the nitrogen glovebox, even though at very small concentrations (ppm), and to contaminants in the carbon nanotube dispersion. Moreover, the high-voltage operation is attributed to the small capacitance produced by the CYTOP due to its film thickness and low k value, according to equation (14). Finally, electron and hole linear mobility have been extracted using equation (11) due to the lack of current saturation, and they are $\mu_e \sim 0.03 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and $\mu_h \sim 0.02 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, respectively.

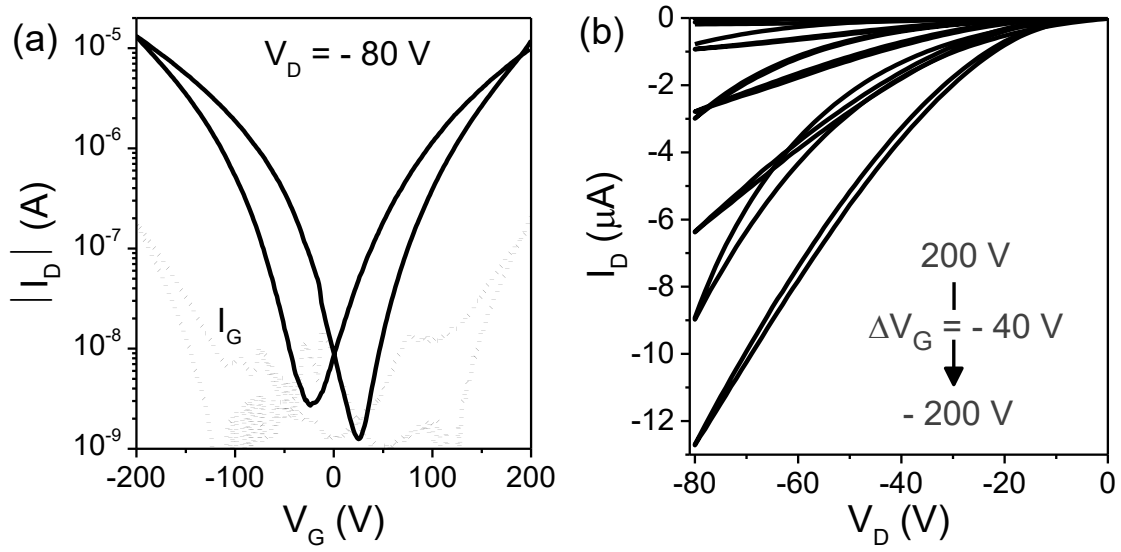


Figure 35: (a) Transfer characteristic of a PFO/(7,5) SWNT top-gate transistor with L_C/W_C of $50\mu\text{m}/1000\mu\text{m}$. The device shows ambipolar behaviour with balanced hole and electron currents. (b) Corresponding transistor output characteristics.⁴⁵

Similarly, transfer and output characteristics of a bottom-gate FET with L_C/W_C of $20\mu\text{m}/10000\mu\text{m}$ fabricated on 200 nm SiO_2 are shown in Figure 36.

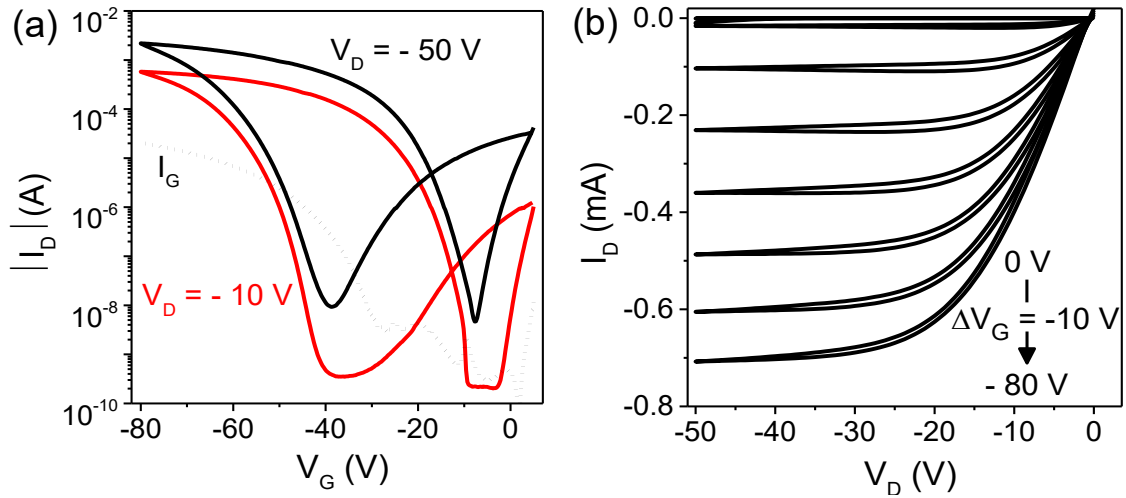


Figure 36: (a) Transfer characteristic of a PFO/(7,5) SWNTs bottom-gate transistor with L_C/W_C of $20\mu\text{m}/10000\mu\text{m}$. The device shows a predominant p-type behaviour with noticeable current hysteresis. (b) Corresponding transistor output characteristic.⁴⁵

Unlike the top-gate transistor of Figure 35, this device exhibits a predominant p-type behaviour, which can be explained by the existence of electron traps at the interface between SiO_2 and SWNT. Moreover, hole injection from both source and drain electrodes is very efficient due to their high work function ($\text{Au} \sim 5\text{ eV}$). It has

already been reported¹²²⁻¹²⁴ that n-type conduction is suppressed in most organic transistors due to charge traps formed at the SiO₂ interface and particularly due to charge transfer to the oxygen/water layer strongly bound to the SiO₂ surface, where the redox couple H₂O/O₂ occurs. This is particularly important for (7,5) SWNT since its valence band position ($E_v \approx -5.2$ eV) is very close to the redox potential of oxygen ($E_{\text{REDOX}} \approx -5.3$ eV) when is dissolved in the slightly acidic water (pH 6) adsorbed on the SiO₂ surface and, for this reason, electrons are efficiently transferred from the (7,5) SWNTs to the oxygen/water layer.¹²² Moreover, charge acceptor states are likely generated on the surface by negative chemical intermediates that have been in turn created by this electrochemical charge transfer process.¹²² These surface states may be the cause for the current hysteresis that is often measured in bottom-gate SWNT transistors made on bare SiO₂. Surface treatments with specific SAMs, like HMDS and OTS, are commonly used to passivate the SiO₂ surface from these surface trap states. However, this treatment has not been investigated here as preliminary results showed only minor improvements and because it was not the main scope of this study. In addition to this, the presence of cellulose membrane residues used to filter the nanotubes from the polymer during the polymer sorting procedure could be another possible cause for the current hysteresis. Regardless of these non-idealities, the device exhibits good performance with gate leakage two orders of magnitude lower than the ON current, current ON/OFF ratio higher than 10⁶, hole saturation mobility, obtained with equation (12), of $\mu_h \sim 0.24 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, and a clear current saturation.

Finally, it is important to remark that both the top-gate and bottom-gate transistors shown in Figure 35 and Figure 36 have not been optimized to achieve high carrier mobility and low-voltage operation, but they have been used to study the impact of the device architecture on charge transport properties. Moreover, due to the non-uniform surface coverage provided by the PFO/(7,5) SWNT network, the channel width that effectively takes part in the transport processes is smaller than the geometrical width used in equations (11) and (12) to calculate the charge carrier linear and saturation mobility, leading to an underestimated value for both transistor architectures.

4.1.4 Analysis of Charge Carriers Percolation

In order to assess the metallic amount still present in the PFO/(7,5) SWNT network after the polymer sorting procedure, ON and OFF currents of various FETs have been analysed as a function of the channel length L_C . Figure 37 shows some preliminary results where the transfer characteristics of PFO/(7,5) SWNT bottom-gate FETs with $W_C = 10000 \mu\text{m}$ and L_C of $2 \mu\text{m}$, $10 \mu\text{m}$ and $40 \mu\text{m}$ have been plotted together.

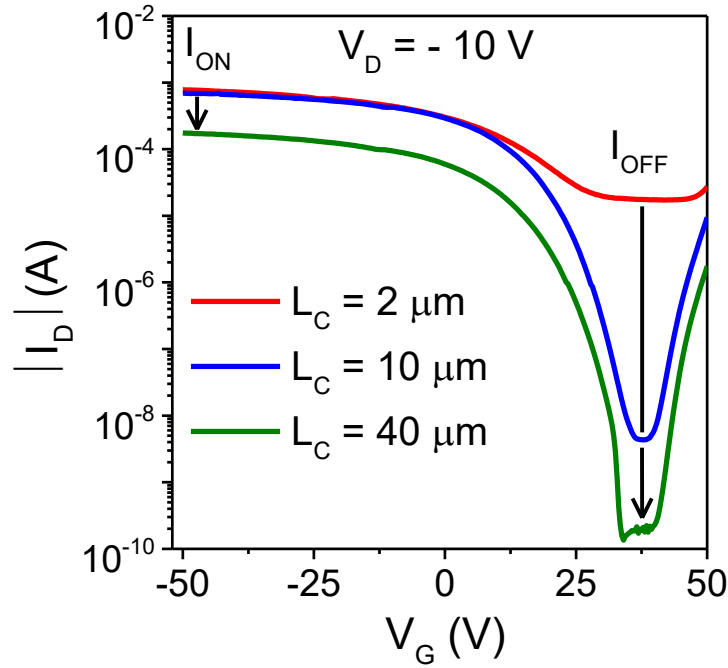


Figure 37: Transfer characteristics of three PFO/(7,5) SWNTs bottom-gate FETs with $W_C = 10000 \mu\text{m}$ and $L_C = 2 \mu\text{m}$, $10 \mu\text{m}$ and $40 \mu\text{m}$. All devices show predominant p-type behaviour with ON currents following Ohm's law and OFF currents following a percolation regime.⁴⁵

From Figure 37 is clearly visible that on one hand, the ON currents in all devices follow Ohm's law and decrease inversely proportional with increasing L_C , due to the corresponding reduction of the electric field along the channel. On the other hand, the OFF currents increase dramatically with decreasing L_C , and this behaviour suggests that charge transport in the transistor OFF state is dominated by the percolation of metallic SWNTs and is particularly pronounced in short L_C devices.

It is also important to observe that the presence of device-to-device variability, which can be appreciated from the slightly deviation of the ON currents from the

ideal ohmic behaviour, is due to multiple reasons. The presence of excess polymer and residues of the cellulose membrane in the PFO/(7,5) SWNT dispersion are known to degrade device performance and reduce the ON current. Fluctuations in the oxygen concentration inside the glovebox, which is known to p-dope SWNTs, are responsible for an unexpected increase of the ON current. The fact that the semiconducting layer is not uniform but is a random network of carbon nanotubes implies that devices are slightly different one from each other. Finally, the PFO/(7,5) SWNT FETs shown in Figure 37 come from different substrate batches, thus batch-to-batch variations are also responsible to affect device performance.

In order to study the charge transport properties of the PFO/(7,5) SWNT networks in the percolation regime and estimate their residual metallic content, the 2D homogenous random-network stick percolation model^{79,80} described by equation (15) is applied. The channel ON and OFF currents of many PFO/(7,5) SWNT transistors are measured to estimate the current exponent m in the ON and OFF states. By combining equation (15) with the experimentally determined ON currents, the current exponent m_{on} , corresponding to the contribution of the whole SWNT network, is extrapolated. On the other hand, from the OFF currents and equation (15), the current exponent m_{off} , corresponding to the percolation of only the metallic nanotubes (m-SWNTs), is obtained. Based on previous considerations from Figure 37, $m_{off} > m_{on}$ and $m_{on} \simeq 1$ are expected. Moreover, once m_{on} and m_{off} are known, the total surface density of the metallic SWNTs (ρ_{met} in m-SWNT μm^{-2}) and their percentage in the network can be easily obtained.

The schematics of the SWNT random networks deposited between two metal electrodes with different relative spacing are shown in Figure 38, where red sticks represent the m-SWNT while grey sticks represent the semiconducting (7,5) SWNTs. For simplicity, the polymer PFO has not been included in the schematics.

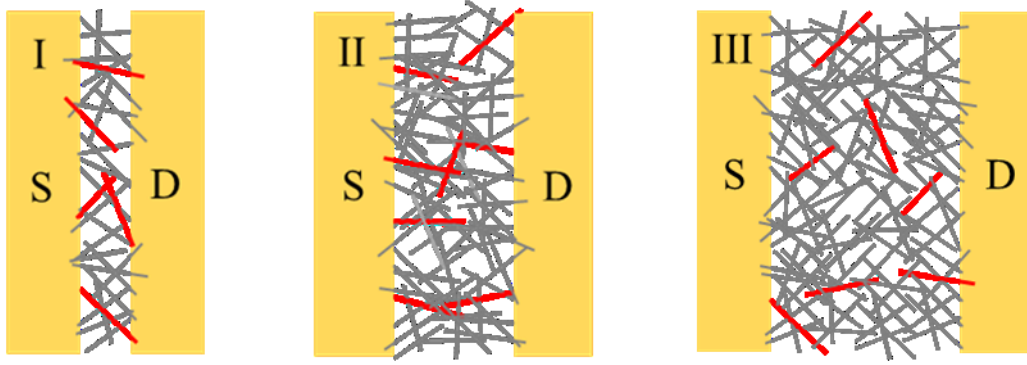


Figure 38: Schematics of the SWNT network in the direct conduction regime (I), percolation regime (II), and thermally-excited carriers' regime (III). Grey sticks correspond to the majority of semiconducting nanotubes, while red sticks correspond to the few m-SWNTs.⁴⁵

Regime I corresponds to the direct conduction regime, which is achieved when the channel length is shorter than the length of the nanotubes, $L_c \leq L_s$. If m-SWNTs are also present in this network, they could form electrical shorts across the channel independently from any applied gate voltage, drastically increasing the OFF current and degrading the device performance. In regime II, the channel length is longer than the nanotube length ($L_c > L_s$) and the conduction in the OFF state is dominated by the percolation of the m-SWNTs. In this regime, even if m-SWNTs cannot directly connect the source and drain electrodes, they could however form metallic percolating paths in parallel with the semiconducting percolation paths, thus increasing the OFF current and again degrading the device performance. From this regime, m_{on} , m_{off} and ρ_{met} are obtained. Finally, in regime III the charge transport in the OFF state is dominated by thermally-excited carriers at room temperature and by measurement limitations associated with the SPA experimental setup.

Figure 39 shows the dependence of the channel ON and OFF currents and current ON/OFF ratio from L_c ranging from $0.75 \mu\text{m}$ to $40 \mu\text{m}$. In order to account for device variability and also to provide a more reliable analysis, four FETs from the same substrate batch have been characterized per each L_c under the same conditions ($V_D = -10 \text{ V}$, $V_G = -50 \text{ V}$) and their ON and OFF currents have been averaged and fitted. The ON current (Figure 39(a), black line), when plotted versus the logarithm of the channel length, exhibits an inversely proportional dependence on L_c , which is attributed to the high surface density of the PFO/(7,5) SWNT network whose conductive behaviour is well approximated by the 2D ohmic conductor limit ($m_{on} =$

1.02 $\sim$ 1). On the contrary, the OFF current (Figure 39(a), red line) reduces by seven orders of magnitude, from $\sim$ 3 mA to $\sim$ 0.3 nA, going from $L_C = 2 \mu\text{m}$ to $L_C = 5 \mu\text{m}$. This L_C range (2-5 μm) corresponds to the regime II, where percolation of metallic nanotubes is responsible for the appreciable OFF current. Moreover, the fact that $m_{off} = 16.3 \gg 1$ is indicative that an almost ideal condition, corresponding to a very low surface density of metallic nanotubes in the channel, is reached. The L_C dependence of the current ON/OFF ratio, ranging from 10^0 to 3.5×10^6 , is also shown in Figure 39(b).

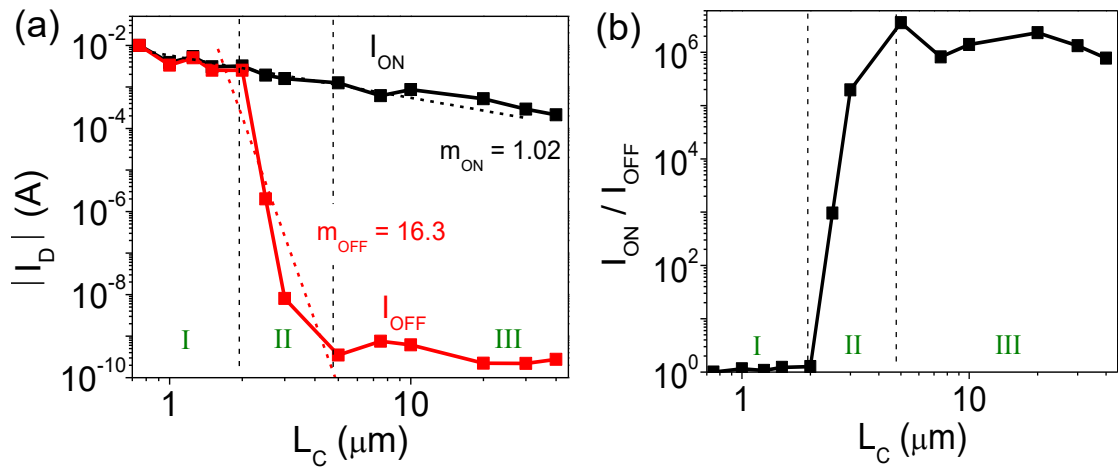


Figure 39: (a) Channel ON (I_{ON}) and OFF (I_{OFF}) currents as a function of L_C , measured at $V_D = -10\text{V}$ and $V_G = -50\text{V}$. m_{off} has been obtained from the fitting line (red dash line) of the percolation region II, while m_{on} from the fitting line (black dash line) of the full range. (b) Corresponding current ON/OFF ratio as a function of L_C .⁴⁵

Previously published experimental results obtained with CVD-grown carbon nanotubes^{80,82} have been used to reproduce the curve of the universal current exponent $m = f(\rho L_S^2)$ by fitting their experimental data, as shown in Figure 40. By using $m_{on} = 1.02$, $m_{off} = 16.3$ and $L_S = 410 \text{ nm}$, the total surface density is found to be approximately 504 SWNT μm^{-2} and the surface density of metallic nanotubes to be approximately 12 m-SWNT μm^{-2} , with a corresponding metallic nanotube percentage of 2.3%. Choosing different values for L_S , within the experimentally determined distribution shown in Figure 32, yields $\rho = 2125 \text{ SWNT } \mu\text{m}^{-2}$ and $\rho_{met} = 50 \text{ SWNT } \mu\text{m}^{-2}$ for $L_S = 200 \text{ nm}$, and $\rho = 85 \text{ SWNT } \mu\text{m}^{-2}$ and $\rho_{met} = 2 \text{ SWNT } \mu\text{m}^{-2}$ for $L_S = 1000 \text{ nm}$. An important observation is that while the surface density of carbon nanotubes strongly depends on the actual length considered for the calculations, the

percentage of metallic nanotubes is independent from L_s , and it depends only on m_{on} and m_{off} values obtained through FET characterization. Finally, it is possible to conclude that the metallic percentage of the PFO/(7,5) SWNT dispersion characterized in this work is approximately 2.3%, even if the nanotubes are broadly distributed in length.

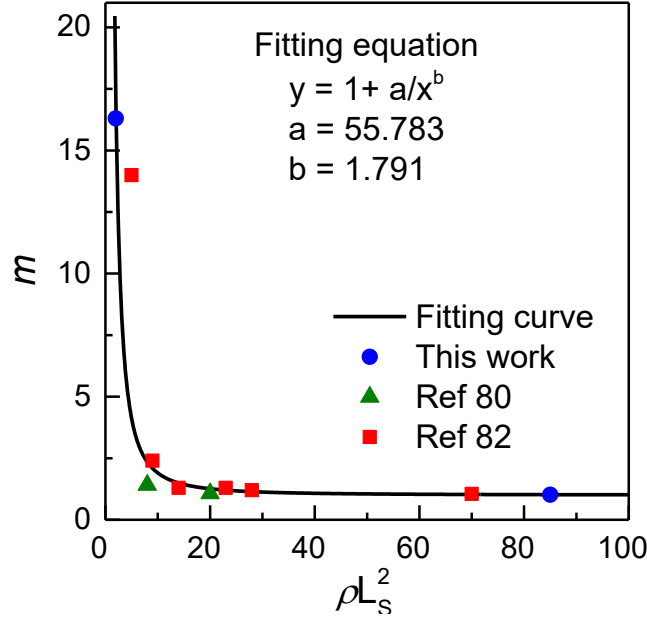


Figure 40: Experimental curve of $m = f(\rho L_s^2)$ obtained by fitting the data from previous published works.⁴⁵

Nevertheless, the presence of the polymer PFO in the network certainly affects the value of the parameter k in the current-scaling equation (15). Moreover, these solution-based nanotubes are not rigid sticks but they are flexible, with defects, they interact with each other and with the substrate, forming bundles and aggregates, and L_s is not precisely known. In any case, it is possible to conclude that even if ρ_{met} is much smaller than the surface density of the whole network, such tiny amount of metallic nanotubes, over a channel width of 10000 μm , is still able to completely shunt the drain-to-source path and degrade the performance of almost all devices with $L_c \leq 2 \mu\text{m}$. The small amount of m-SWNTs also validates the absence of any visible peak in the absorption spectrum of Figure 30. A possible explanation is that the actual surface density of m-SWNTs can be lower than the value calculated with the percolation theory because the presence of semiconducting nanotubes bundled

together in the FET channel may contribute to enhance the OFF current.^{17,82} However, further work is required to prove or refute this hypothesis.

4.1.5 Lateral Conductivity Measurements using C-AFM

In order to further characterize the percolation behaviour of the PFO/(7,5) SWNT network at the nanoscale, conductive atomic force microscope (C-AFM) in the lateral conductivity mode was performed.¹¹⁷ In this technique, a scanning electrode made of a platinum-coated (Pt) conductive AFM probe is scanned in contact with the active layer's surface, deposited over an insulating substrate, at a known lateral distance from a second fixed electrode, usually gold (Au). By applying a fixed bias between the C-AFM probe and the Au electrode, both the topography and the lateral current of the PFO/(7,5) SWNT network are simultaneously acquired. In the simplest case of a uniform film, the applied electric field is inversely proportional to the distance between the scanning C-AFM probe and the remote Au electrode. However, since the current flow between any two points along the SWNT network strongly depends on its morphology and on the various resistive paths (CNT-CNT junctions, intra/inter-CNT transport, etc....), the effective electric field may deviate from its theoretical value. These transport paths are made from a random combination of many semiconducting SWNTs and few metallic ones, which are randomly distributed within the semiconducting population and unfortunately are also completely hidden from any direct C-AFM visualization. Figure 41 shows a schematic representation of the lateral C-AFM setup used in this analysis.

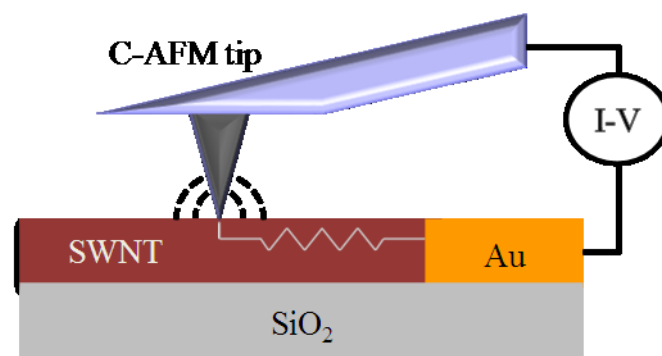


Figure 41: Schematic representation of the lateral C-AFM setup operating in contact-mode.⁴⁵

Figure 42(a) shows the topographic image of the PFO/(7,5) SWNT network deposited onto a SiO₂ substrate, while Figure 42(b) shows the corresponding

resistance map (R), where R has been calculated for each sampled point (x,y) from the measured current map $I(x,y)$ by using a constant voltage applied between the C-AFM probe and the Au electrode. As can be seen in Figure 42(b), only certain nanotubes close to the Au electrode (schematically depicted at the top of the image), are well visible in the network (darker regions). The resistance (current) increases (decreases) as the C-AFM probe moves away perpendicularly from the Au electrode in the y -direction, thus showing a preferred current transport direction perpendicularly to the Au electrode, almost independent from the x position. This is not surprising since the absolute value of the electric field reduces proportionally to the distance between the C-AFM probe and the Au electrode, for the applied constant voltage. This is not the case when the C-AFM probe moves in the x -direction (parallel to the electrode), where the electric field remains almost constant, as well as the current. However, this simplified description is valid only in the central region of the substrate, away from the edges of the Au electrode, where the geometry of the electrode determines a non-uniform electric field distribution and border effects take place.

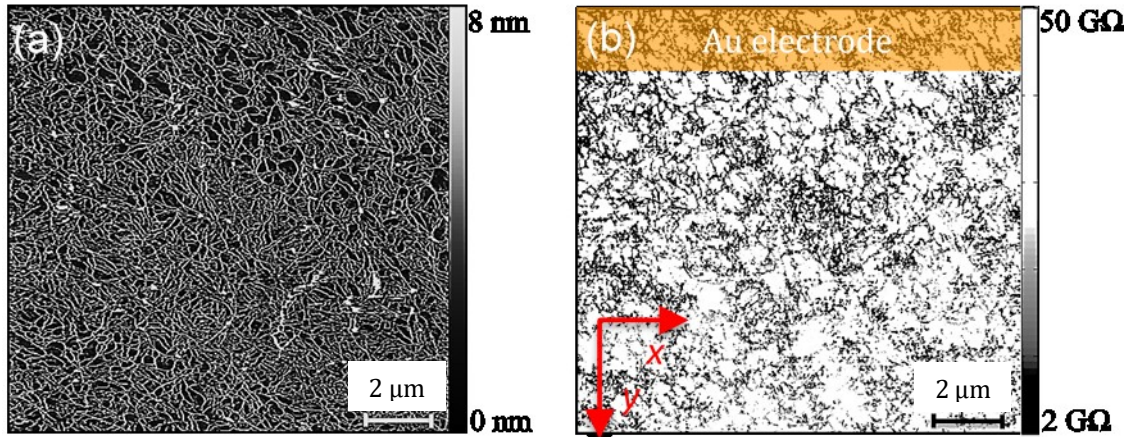


Figure 42: (a) Lateral C-AFM topography map obtained in contact-mode for a PFO/(7,5) SWNT network deposited on SiO₂. (b) Corresponding resistance map $R(x,y)$.⁴⁵

Figure 43(a) shows the resistance distribution of the whole nanotube population, taken from $R(x,y)$, where R_{AV} is the average value ($R_{AV} \sim 18 \text{ G}\Omega$) and R_{STD} is the standard deviation ($R_{STD} \sim 15 \text{ G}\Omega$). It is important to remark that the resistance map $R(x,y)$, shown in Figure 42(b), strongly depends from the shape of the Au electrode and the relative position between the scanning C-AFM probe and the Au electrode.

For these reasons, both the current and the resistance are not representative of the PFO/(7,5) SWNT network. In order to evaluate the intrinsic electrical properties of the PFO/(7,5) SWNT network, the network resistivity ρ_x and ρ_y have been calculated, defined respectively along x and y directions. Figure 43(b) shows the resistivity distributions together with the corresponding mean and standard deviation values.

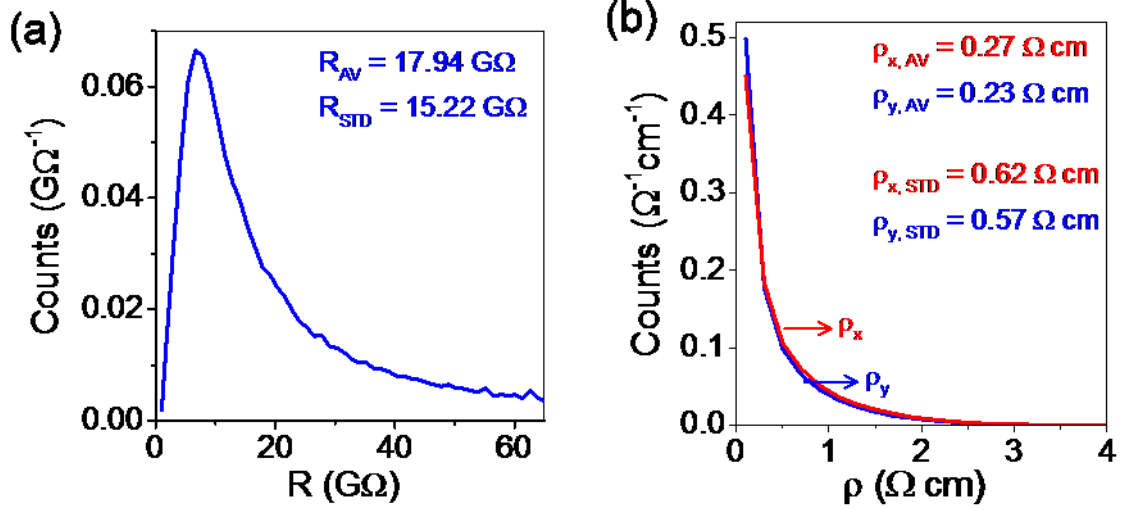


Figure 43: (a) PFO/(7,5) SWNT network resistance distribution with average and standard deviation values. (b) Corresponding PFO/(7,5) SWNT network resistivity distributions along x and y directions with average and standard deviation values.⁴⁵

The resistivity ρ_x and ρ_y have been obtained from the following expressions:

$$\rho_x(x, y) = \frac{|\Delta R(x, y)_x|}{\Delta x} t(x, y) \Delta y \quad (31)$$

$$\rho_y(x, y) = \frac{|\Delta R(x, y)_y|}{\Delta y} t(x, y) \Delta x. \quad (32)$$

In equations (31) and (32) $R(x, y)$ is the resistance value at each sampled position, Δx and Δy are the x and y measurement steps of the C-AFM probe, and $t(x, y)$ is the topographic height at the sampled position, which is acquired by the C-AFM simultaneously with the current. The main advantage of using the x and y resistivity is that they are intrinsic parameters of the network, as they do not depend from the electrode shape but only on carbon nanotube electrical properties and network distribution. In the ideal situation where SWNTs are fully-aligned along a certain

direction, two different transport mechanisms occur: ballistic-type along the nanotube axis and hopping-type transverse to the nanotube axis. The resistivity measured along the nanotube axis in the ballistic transport is characterized by a very narrow distribution, with low average and standard deviation values. On the other hand, the resistivity measured transverse to the nanotube axis in the hopping-limited transport is characterized by a broader distribution, with higher average and standard deviation values. As shown in Figure 43(b), ρ_x and ρ_y exhibit a very similar average ($\rho_{x,av} = 0.27 \text{ } \Omega\cdot\text{cm}$, $\rho_{y,av} = 0.23 \text{ } \Omega\cdot\text{cm}$) and standard deviation ($\rho_{x,std} = 0.62 \text{ } \Omega\cdot\text{cm}$, $\rho_{y,std} = 0.57 \text{ } \Omega\cdot\text{cm}$), accordingly it can be concluded that the measured PFO/(7,5) SWNT network is characterized by an isotropic distribution, with no preferential orientation (no alignment). Even though it is likely predictable for a spin-coated network to distribute randomly on the surface, it validates the applicability of the 2D random-network model used for the analysis of charge percolation behaviour. To further support this theory, a blade-coated PFO/(7,5) SWNT network partially-aligned along y direction has been scanned with C-AFM in contact-mode and its topography and resistance map have been acquired. Figure 44 shows the topography and resistivity distributions.

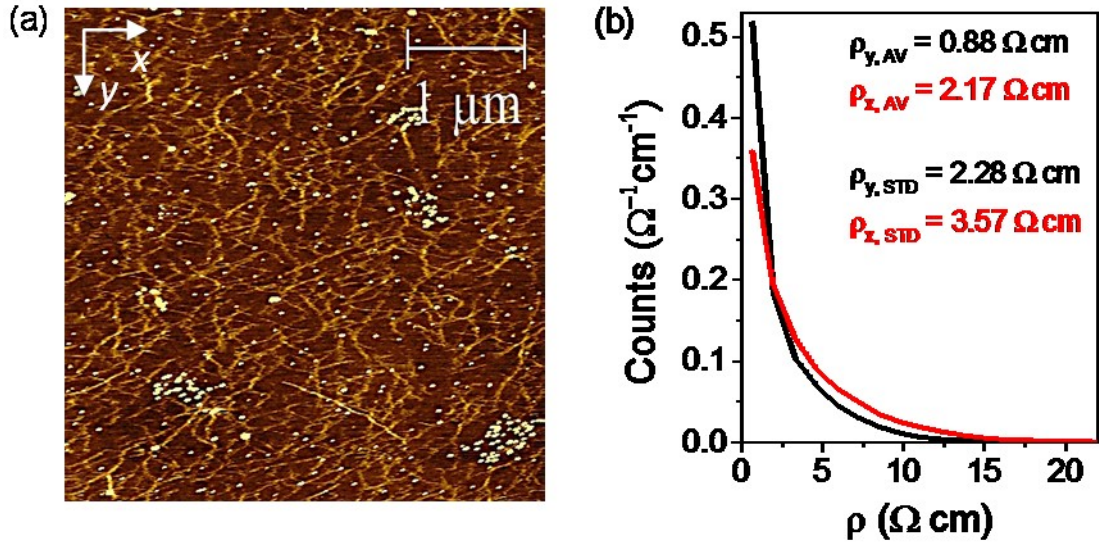


Figure 44: (a) C-AFM topography map obtained in contact-mode for a partially-aligned PFO/(7,5) SWNT network blade-coated along y direction on a SiO₂ substrate. (b) Corresponding network resistivity distributions along x and y directions, with average and standard deviation values.⁴⁵

The fact that the average and standard deviation values of the resistivity along y are smaller than those along x suggests that a partial alignment along y direction is achieved. Hence, from the analysis of the C-AFM resistivity map along x and y directions it is possible to assess if the carbon nanotube network is isotropic or if nanotubes are orientated along a certain preferential direction.

4.1.6 Conclusions

In conclusion, a novel approach for studying the current percolation behaviour in solution-deposited semiconducting 2D-networks made of PFO/(7,5) SWNTs has been reported. The method relies on the combination of AFM topography, electrical field-effect transistors and lateral C-AFM measurements. AFM analysis of spin-coated networks has been used to fully characterize the surface morphology in terms of length, surface density, and surface coverage. By combining electrical field-effect measurements with the 2D homogeneous random-network stick percolation model, the surface density of metallic nanotubes in the network has been calculated. The electrical measurements also revealed the presence of three conduction regimes depending on L_c . Regime I was identified as the direct conduction regime and was observed for devices with $L_c < 2 \mu\text{m}$. Regime II was identified as the percolation conduction regime and was found to dominate charge transport in transistors with $2 \mu\text{m} < L_c < 5 \mu\text{m}$. Finally, regime III was attributed to the transport of thermally-excited carriers and was observed only in transistors with $L_c > 5 \mu\text{m}$. By using the lateral C-AFM, the current percolation pathways in the SWNT network were mapped with nanoscale spatial accuracy. These measurements allowed calculation of the resistivity distributions in the PFO/(7,5) SWNT network as a function of (x,y) position, while validating its isotropic distribution. Most importantly, the proposed approach is simple and it could potentially allow quantification of the metallic content and the degree of alignment of any semiconducting material disposed in a 2D random network.

4.2 PFO-BPy/(6,5) SWNT Flexible Low-Voltage FETs⁵

4.2.1 Introduction

In addition to the excellent electrical properties, carbon nanotubes are remarkable also for their extraordinary mechanical properties. In the work of Lau *et al.*,⁵⁰ SWNTs have been deposited onto flexible substrates by gravure printing and TFTs have been characterised while bent down to 1 mm radius. Moreover, carbon nanotubes also proved to be a suitable material for active matrix X-ray backplanes on flexible substrates.¹²⁵ By exploring the low-temperature processing advantages offered by the solution-based deposition of the SWNT dispersion, PFO-BPy/(6,5) SWNT bottom-gate bottom-contact FETs have been fabricated on free-standing polyimide foils and characterized under variable tensile strain. Moreover, high charge carrier mobility ($8.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) and low-voltage operation with $|V_G| < 10 \text{ V}$ has been made possible by implementing a more advanced device design and a fabrication process comprising 50 nm of Al_2O_3 as the bottom-gate dielectric deposited by ALD on polyimide foils. Nonetheless, these low-voltage PFO-BPy/(6,5) SWNT FETs still cannot reach the performance of SWNT transistors that employ SAMs or polymer/metal oxide hybrid gate dielectrics, for which a low-voltage operation with $|V_G| < 3 \text{ V}$ has been demonstrated.^{20,126}

4.2.2 Optical and Morphological Characterization

Figure 45 shows the absorption spectrum of the PFO-BPy/(6,5) SWNT dispersion in chlorobenzene. Indication of nearly single chirality (6,5) SWNTs arises from the presence of the two sharp absorption peaks at $\lambda = 1000 \text{ nm}$ and $\lambda = 575 \text{ nm}$, which correspond to E_{11} and E_{22} sub-band excitonic transitions of the (6,5) SWNT respectively. However, other minor peaks are also visible at $\lambda = 1038 \text{ nm}$ and $\lambda = 1135 \text{ nm}$, corresponding to the absorption of minority species (7,5) and (7,6) nanotube chirality, while the peak at $\lambda = 355 \text{ nm}$ corresponds to the absorption of the polymer PFO-BPy.

⁵ Text and figures within this chapter have been partially reprinted from Bottacchi F. *et al. Appl. Phys. Lett.* **106**, 193302 (2015),²¹ with the permission of AIP Publishing (see Appendix 7.1).

The surface morphology of the PFO-BPy/(6,5) SWNT network has been studied by tapping-mode AFM. Figure 46(a) shows the surface topography of the PFO-BPy/(6,5) SWNT network deposited onto Al₂O₃, while Figure 46(b) shows the rough topography of the bare Al₂O₃ surface deposited on SiN_x by ALD, as described in Section 3.2.3.

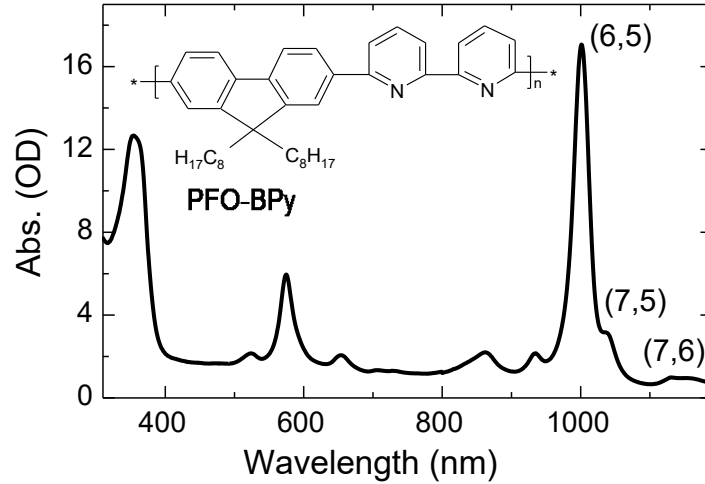


Figure 45: Absorption spectrum of the PFO-BPy/(6,5) SWNT dispersion in chlorobenzene. The peaks at $\lambda = 1000\text{nm}$ and $\lambda = 575\text{nm}$ respectively, correspond to the first and second excitonic transitions of the (6,5) nanotube, while the minor peaks at $\lambda = 1038\text{nm}$ and $\lambda = 1135\text{nm}$, corresponding to the absorption of (7,5) and (7,6) nanotube chiralities. The peak at $\lambda = 355\text{nm}$ corresponds to the absorption of the polymer PFO-BPy, whose chemical structure is shown in the inset.²¹

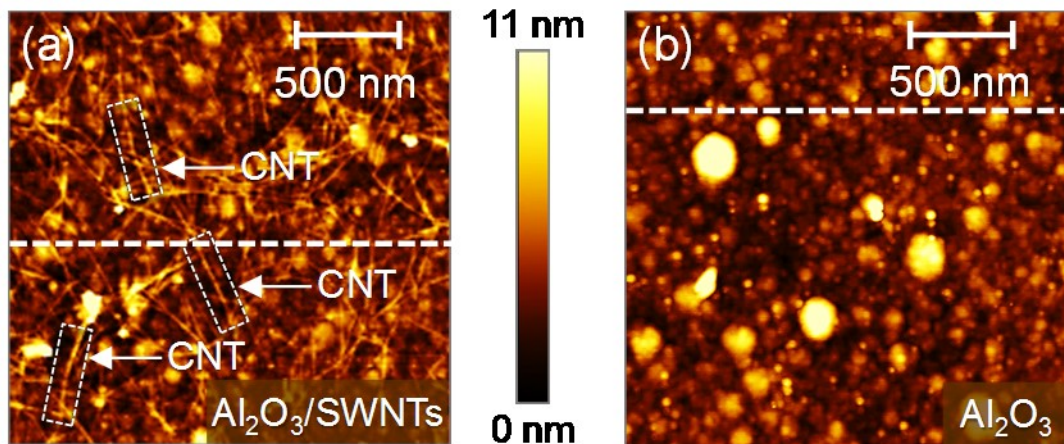


Figure 46: (a) AFM topography image of the PFO-BPy/(6,5) SWNT network on Al₂O₃ gate dielectric surface, and (b) AFM topography image of the rough Al₂O₃ gate dielectric surface prior to the semiconductor deposition. Surface line scans have been taken along the white dashed lines. In this case Al₂O₃ was deposited onto a rigid SiN_x substrate.²¹

In order to fully characterize the semiconductor and dielectric topography, height distributions and surface line scans (stacked), taken along the white dashed lines in Figure 46, have been plotted in Figure 47. The root mean square value in the height distribution of Figure 47(b) increases due to the presence of carbon nanotubes onto the Al_2O_3 dielectric surface.

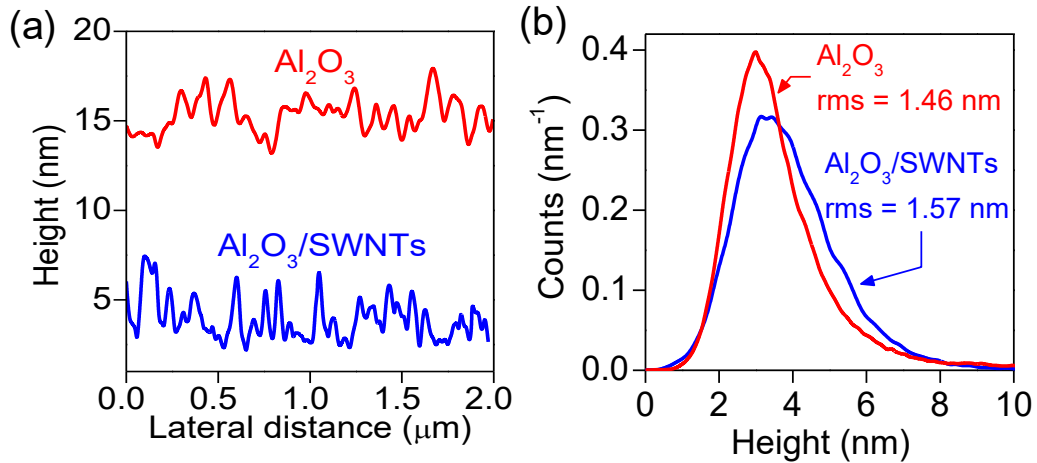


Figure 47: (a) Stacked surface line scans taken along the white dashed lines from Figure 45. (b) Corresponding height distributions. The root mean square (rms) value increases due to the presence of carbon nanotubes onto the Al_2O_3 dielectric surface.²¹

A detailed morphological characterization of the PFO-BPy/(6,5) SWNT network has been performed on an atomically-flat SiO_2 substrate with AFM in tapping-mode. Figure 48 shows the topography image of the PFO-BPy/(6,5) SWNTs, where carbon nanotubes are clearly visible on SiO_2 surface.

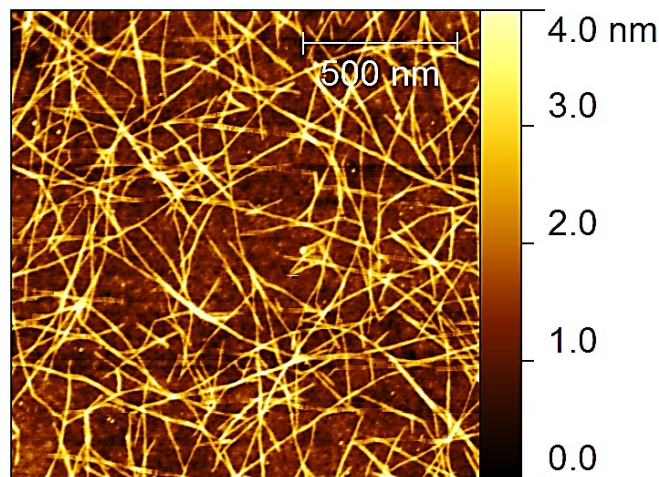


Figure 48: AFM topography image of the PFO-BPy/(6,5) SWNTs deposited on SiO_2 surface.²¹

From this AFM topography image, the surface density of the SWNTs has been estimated to be higher than $100 \text{ SWNT } \mu\text{m}^{-2}$, with an average nanotube length approximately of 400 nm. By applying equation (16) from the percolation model (Section 2.4.7) and by using $L_s = 400 \text{ nm}$, a percolation threshold of $36 \text{ SWNT } \mu\text{m}^{-2}$ is obtained, which is well below the experimentally-determined lower limit of $100 \text{ SWNT } \mu\text{m}^{-2}$. Therefore, it can be concluded that the SWNT density is well above the percolation limit, hence charge carrier mobility can be extracted using equation (11) and (12) within the gradual channel approximation.⁷¹

Through careful analysis of the AFM image in Figure 48, the relative surface coverage of SiO_2 and (6,5) SWNTs have been calculated based on the coverage model described in Section 3.3.2.1. The following percentages have been obtained: SiO_2 covers $\sim 61\%$ of the total surface area scanned while (6,5) SWNTs cover the $\sim 39\%$. Figure 49(a) shows the height distributions of bare SiO_2 (red line) and of PFO-BPy/(6,5) SWNTs onto SiO_2 (blue line), while Figure 49(b) shows the correspondent cumulative distribution.

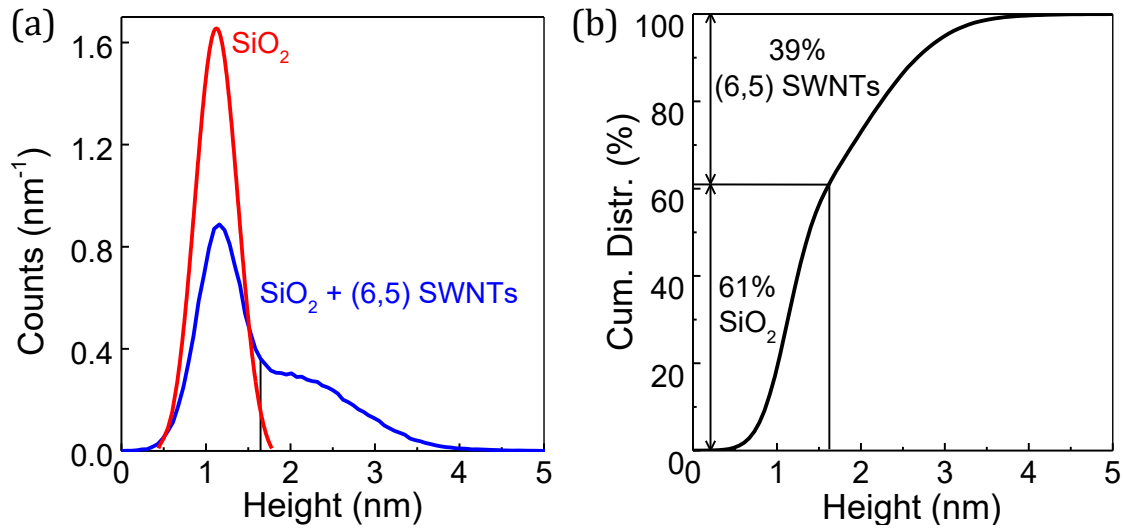


Figure 49: (a) Height distributions of bare SiO_2 (red line) and of PFO-BPy/(6,5) SWNTs onto SiO_2 (blue line). (b) Correspondent cumulative distribution of PFO-BPy/(6,5) SWNTs onto SiO_2 .²¹

Because SWNTs do not entirely cover the FET channel surface but they only occupy 39% of it, the effective FET channel width is much smaller than the geometrical width used to extract the charge carrier mobility. Hence, the mobility values calculated and reported below are underestimated.

Finally, because FETs have been fabricated onto flexible substrates, surface topography of polyimide foils have also been characterized, as shown in Figure 50.

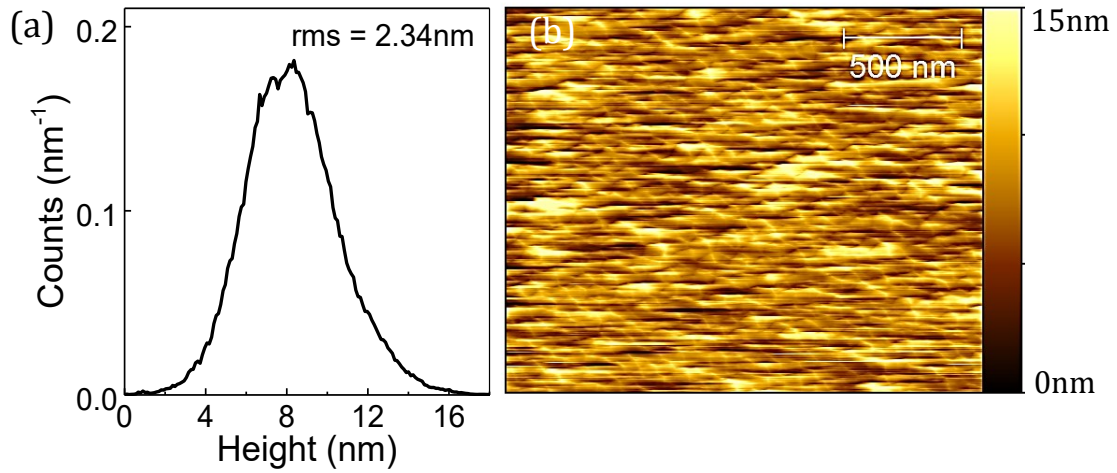


Figure 50: (a) Height distribution of polyimide with a root mean square (RMS) value of 2.34nm. (b) AFM topography image of a bare polyimide foil.²¹

An important observation is that the Al₂O₃ dielectric layer is always deposited on top of the polyimide, thus it is its surface that defines the channel interface in the bottom-gate bottom-contact FET configuration used. Thus, the surface onto which SWNTs are deposited is always Al₂O₃, regardless the polyimide or SiN_x substrate. Therefore, the only relevant surface morphology and roughness is that of Al₂O₃.

4.2.3 Low-Voltage FETs

The charge transporting characteristics of the PFO-BPy/(6,5) SWNT networks were studied using a bottom-gate coplanar transistor architecture, as the one shown in Figure 21(c). Figure 51 displays a representative set of the transfer and output characteristics of a transistor fabricated on a rigid SiN_x substrate, with L_C/W_C of 10 μm/500 μm and 50 nm of Al₂O₃ bottom-gate dielectric. The device exhibits low operating voltage and a strong p-type behaviour, which can be attributed to the electron trapping nature of the SWNT/Al₂O₃ interface, to the use of high work function S/D electrodes (Au → 5 eV), and to the presence of residual atmospheric oxidants in the glovebox that are known to p-dope SWNTs. All transistors exhibit a visible operating hysteresis (3.4 V) attributable to the presence of surface

adsorbates and water on the Al_2O_3 surface, similarly to the situation with SiO_2 described in Section 4.1.3.

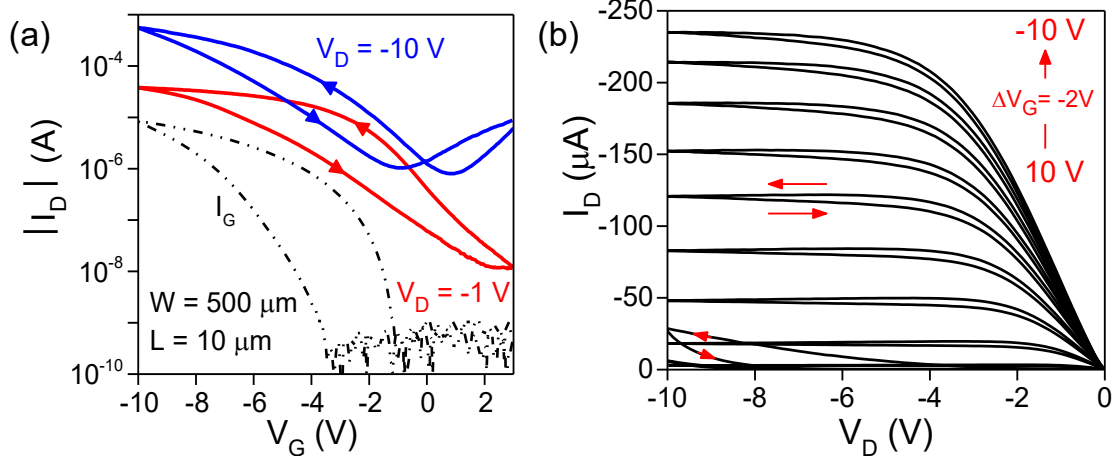


Figure 51: (a) Transfer characteristic of a PFO-BPy/(6,5) SWNT low-voltage transistor fabricated on a rigid SiN_x substrate, with L_c/W_c of 10/500 μm and 50nm of Al_2O_3 bottom-gate dielectric. The device shows a predominant p-type conduction and visible hysteresis. (b) Corresponding output characteristic.²¹

Nonetheless, all devices exhibit low operating voltage ($|V_G| < 10$ V), clear current saturation, an appreciable channel current ON/OFF ratio $> 10^3$, low threshold voltage ($V_{\text{TH}} \sim -1.1$ V), a sub-threshold swing (SS) of ~ 1.73 V/dec, and linear and saturation hole mobility of $0.7 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and $2.3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, respectively. Finally, it is interesting to observe the impact of the gate dielectric on the device performance. Devices described in Section 4.1 with 200 nm bottom-gate SiO_2 and 900 nm top-gate CYTOP show a much higher operating voltage and a much lower mobility. This dramatic change in performance is attributed to the different dielectric constant and dielectric thickness, which both strongly affect the capacitance induced in the FET channel.

4.2.4 Mechanical Bendability of Flexible Low-Voltage FETs

Once device performance have been assessed on a rigid SiN_x substrate, PFO-BPy/(6,5) SWNTs FETs have been fabricated directly on free-standing flexible polyimide foils in order to assess also their mechanical properties. A schematic representation of the device structure is shown in Figure 52.

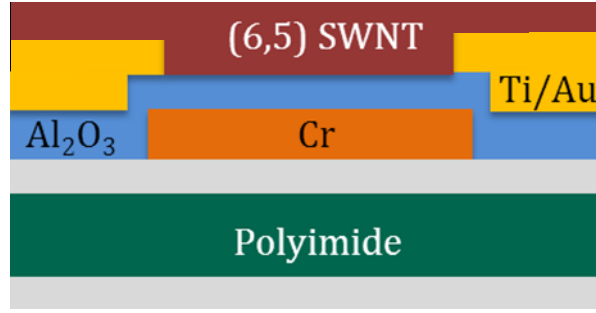


Figure 52: Schematic representation of the bottom-gate coplanar PFO-BPy/(6,5) SWNT FET fabricated on flexible polyimide.

Figure 53 shows a representative set of transfer and output characteristics obtained from a low-voltage PFO-BPy/(6,5) SWNT FET fabricated on a flexible polyimide foil and characterized flat while attached onto a carrier glass.

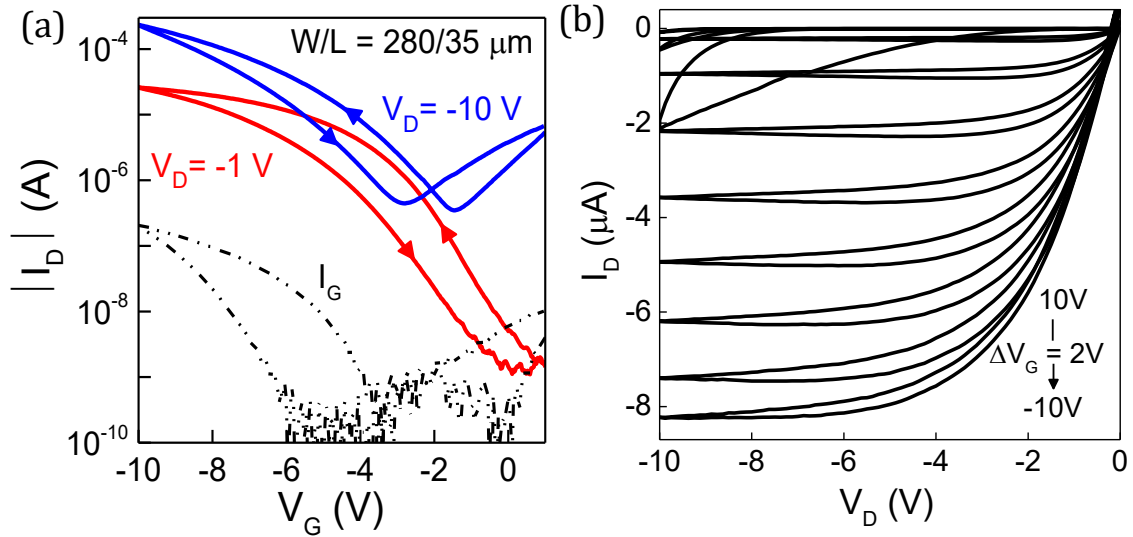


Figure 53: (a) Transfer characteristic of a PFO-BPy/(6,5) SWNT transistor with L_c/W_c of 35/280 μm , fabricated on a free-standing flexible polyimide foil. The device shows a predominant p-type behaviour and a saturation hole mobility of $8.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. (b) Corresponding output characteristic.²¹

The device exhibits strong p-type behaviour with clear current saturation and visible current hysteresis, as in the previous case. Key device parameters include a current ON/OFF ratio $> 10^4$, $V_{\text{TH}} = -3.1 \text{ V}$, $\text{SS} = 1.09 \text{ V/dec}$, $\mu_{\text{lin}} = 3.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and $\mu_{\text{sat}} = 8.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. The significantly higher hole mobility, as compared to devices fabricated on rigid substrates, is most likely attributed to an improved surface interaction between the nanotubes and the Al_2O_3 dielectric, due to the different morphology of the polyimide substrate (Figure 50).

To assess the mechanical flexibility of FETs, bending tests with a radius of 5 mm and 4 mm have been performed by attaching the transistors onto a double-sided adhesive tape and winding them around metal rods of different radius in such a way that tensile strain is applied only parallel to the transistor channel. Figure 54(a) shows the transfer characteristic of a flexible PFO-BPy/((6,5) SWNT transistor measured while flat and bent to rods with tensile radii (R_T) of 5 mm and 4 mm. Figure 54(b) shows a photograph of actual devices during testing. The transistors remain fully functional even when strained down to a 4 mm radius with only minor variations in the device performance (V_{TH} shift of -50 mV).

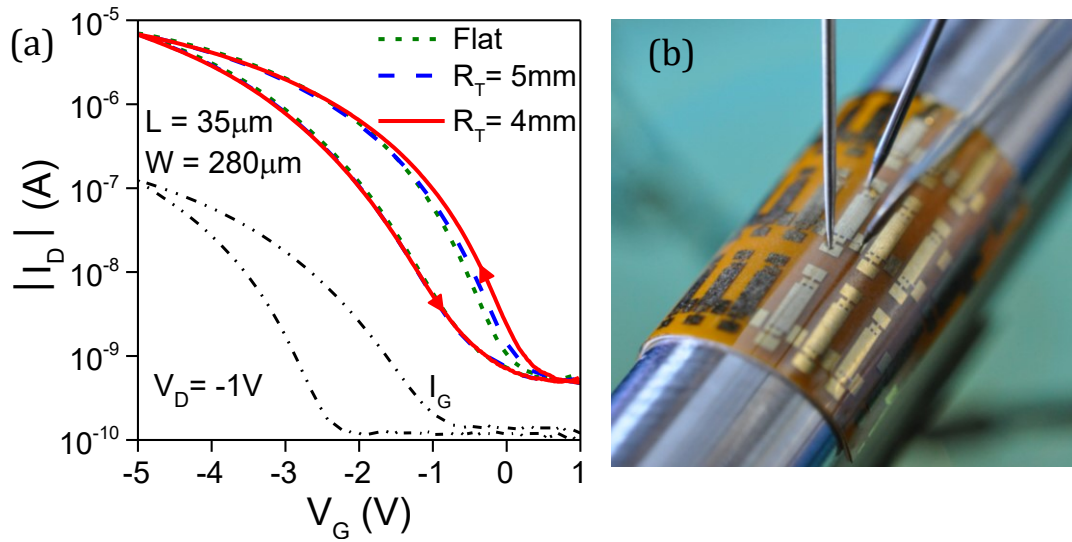


Figure 54: (a) Transfer characteristic of a flexible PFO-BPy/((6,5) SWNT transistor with L_c/W_c of 35/280 μm , measured while flat and bent to tensile radii of 5mm and 4mm. (b) Photograph of the actual transistor during testing, while bent to a tensile radius of 4mm.²¹

Due to their high mechanical flexibility, SWNTs could in principle be bent to much smaller radii, however such test has not been carried out due to the formation of cracks in the brittle Cr gate.¹²⁷

4.2.5 Conclusions

In conclusion, PFO-BPy/((6,5) SWNT FETs have been fabricated onto free-standing flexible polyimide foils and characterized under variable tensile strains to assess the mechanical bendability of SWNTs. Devices were fully operational down to 4 mm tensile radius and a charge carrier mobility of $8.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ was achieved with a low-voltage operation.

4.3 Polymer-sorted SWNT Flexible Logic Circuits⁶

4.3.1 Introduction

Complementary technology, combining n- and p-type integrated transistors, enables simplification of circuit design while minimizing noise and lowering power consumption. Unlike logic devices based on complementary semiconductors, like silicon, gallium-arsenide, indium-phosphide..., the lack of complementary organic or inorganic solution-processable semiconductors with similar n- and p-channel performance is a major challenge towards the realization of solution-processed CMOS logic circuits. While n-type semiconducting metal oxides, especially IGZO (indium gallium zinc oxide) and InO_x (indium oxide), have high electron mobility > 10 cm²V⁻¹s⁻¹ and ambient stability, organic and inorganic p-type materials with matching performance are difficult to obtain. To date, circuits based on n-type semiconducting metal oxides and organic or inorganic p-type semiconductors have been reported by several groups.⁵² More specifically, unipolar inverters^{25,128,129} as well as complementary inverters,^{24,130} complementary-like²⁰ inverters and more complex digital and analogue circuits²⁴ based on solution-processed SWNTs have been demonstrated. In particular, Kim *et al.*^{131–133} extensively worked on the integration of inkjet-printed carbon nanotubes with zinc tin oxide (ZTO) for the realization of high-speed hybrid complementary ring oscillators^{132,133} and D flip-flops.¹³¹

The promising operating characteristics and mechanical properties of the polymer-sorted (6,5) and (7,5) SWNT transistors have been further exploited for the fabrication of high performing unipolar and complementary logic circuits on rigid as well as flexible substrates. CMOS devices have been fabricated on free-standing polyimide foils by integrating spin-coated polymer-sorted SWNTs with sputtered and spray-coated n-type semiconducting metal oxides, offering a route towards solution-processed and bendable logic circuits with high performance.

⁶ Text and figures within this chapter have been partially reprinted from Bottacchi F. *et al. Appl. Phys. Lett.* **106**, 193302 (2015),²¹ with the permission of AIP Publishing, and from Petti L. *et al. IEEE International Electron Devices Meeting*, Copyright © 2014, IEEE (see Appendix 7.1).²³

4.3.2 Low-Voltage Unipolar Inverter

Unipolar PFO-BPy/(6,5) SWNT logic circuits with bottom-gate bottom-contact device architecture have been fabricated on rigid SiN_x substrates with 50 nm Al₂O₃ gate dielectric, and characterized inside a nitrogen glovebox. Figure 55(a) shows the circuit design of the p-type inverter used, which consists of a driving PFO-BPy/(6,5) SWNT transistor with $L_c = 20 \mu\text{m}$ and $W_c = 1.4 \text{ mm}$, and one passive load with resistance $R_L = 160 \text{ k}\Omega$, made from the same metal used for the gate electrode, and therefore eliminating the requirement for further process steps. The VTC and corresponding static gain are shown in Figure 55(b). The inverter exhibits a low-voltage operation with a gain of 5.3 V/V almost centred at the midpoint voltage ($V_M = -1 \text{ V}$), nearly rail-to-rail output swing with the output high voltage approaching zero ($V_{OH} = -0.02 \text{ V}$) and the output low voltage close to V_{DD} ($V_{OL} = -1.81 \text{ V}$), and noise margins of $NM_H = 0.4 \text{ V}$ and $NM_L = 0.6 \text{ V}$.

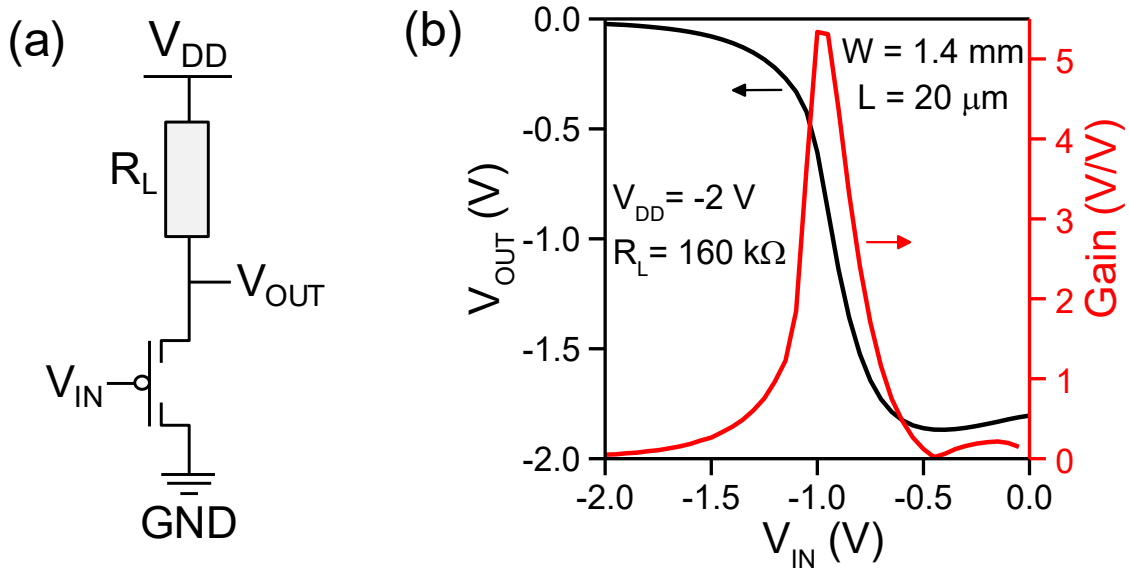


Figure 55: (a) Circuit schematic of the unipolar p-type inverter. (b) VTC and corresponding static gain of a PFO-BPy/(6,5) SWNT unipolar inverter fabricated on a SiN_x substrate. The p-type unipolar inverter exhibits a gain of 5.3V/V while measured at a supply voltage of -2V, and it consists of a driving PFO-BPy/(6,5) SWNT transistor with L_c/W_c of 20/1400 μm and one passive load with a resistance of 160k Ω .²¹

4.3.3 Bendable CMOS Inverter Integrated with IGZO

CMOS inverters have been realized by integrating one p-channel SWNT TFT and one n-channel metal oxide TFT on the same SiN_x substrate. Bottom-gate coplanar

device architecture with 50 nm Al_2O_3 gate dielectric was used. The IGZO was vacuum-processed using RF magnetron sputtering, and a 15 nm film was deposited at room temperature. It was then patterned in the n-channel by wet etching and passivated with a photoresist, which also acted as a protective layer.⁷

Figure 56 shows the AFM topography image obtained in tapping-mode of IGZO deposited on Al_2O_3 surface. The film appears to be quite homogeneous with no visible grain boundaries.

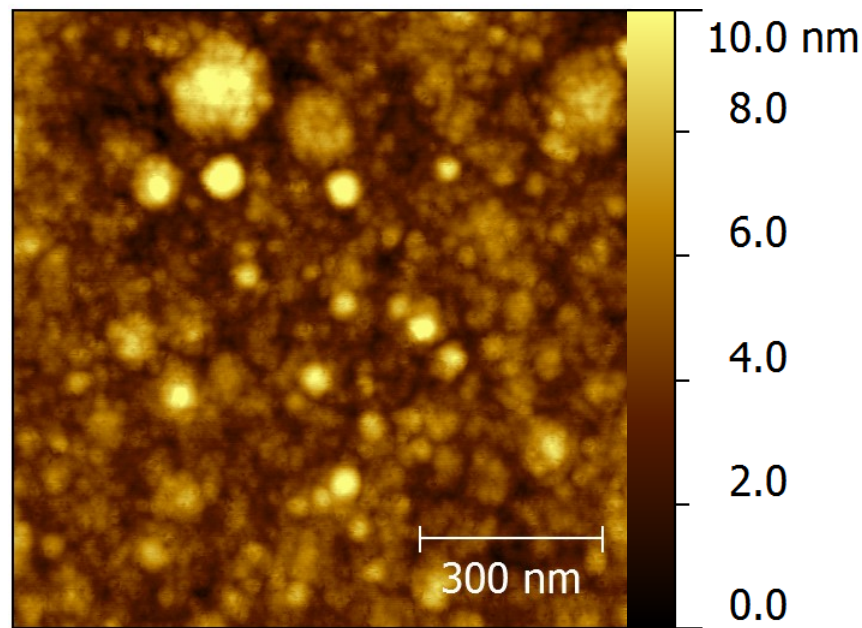


Figure 56: AFM topography in tapping-mode of IGZO film deposited by RF magnetron sputtering on Al_2O_3 surface. The film appears to be quite homogeneous with no visible grain boundaries. (Copyright © 2014, IEEE).²³

To complement IGZO, PFO/(7,5) SWNT dispersion was then spin-coated all over the device area without patterning nor passivation. An alternative deposition technique that enables the patterning of the nanotubes in the p-channel, like spray-coating or inkjet printing, would have been a preferred solution to isolate complementary carrier paths. For this reason, the role of the photoresist on top of the IGZO is of crucial importance as it isolates the channels from direct contact, thus allowing CMOS operation. Figure 57 shows the fabrication process flow and the schematic cross section of the hybrid CMOS inverter. The same device architecture

⁷ RF magnetron sputtering, wet etching and passivation of IGZO have been performed by Dr Luisa Petti at ETH Zurich, as part of a collaboration.

and fabrication process steps have been used also to realize flexible devices on 50 μm free-standing polyimide foils (Kapton).

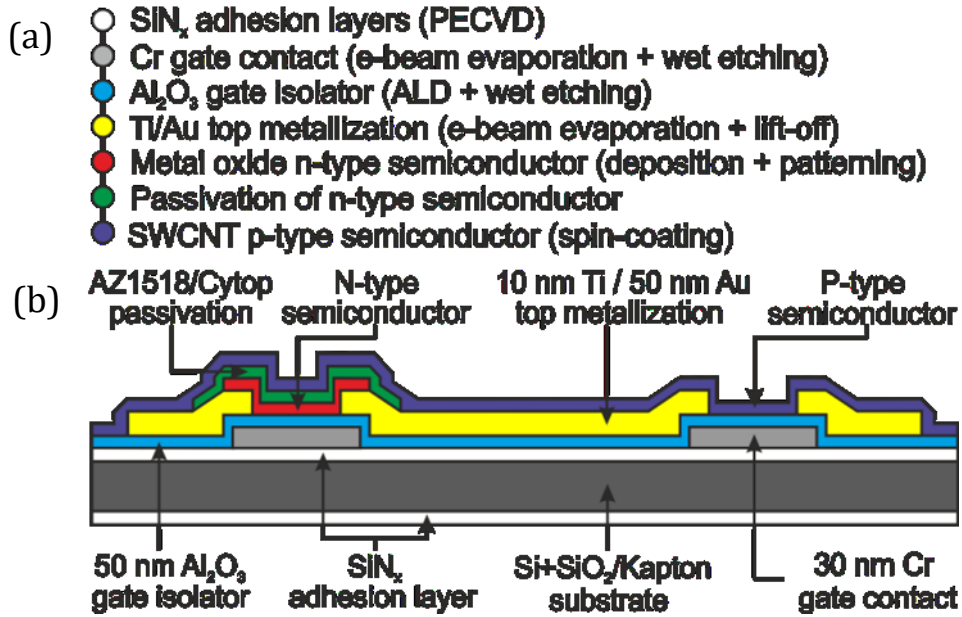


Figure 57: (a) Fabrication process flow and (b) schematic cross section of the hybrid CMOS inverter comprising of PFO/(7,5) SWNT in the p-channel and semiconducting metal oxide in the n-channel. The same architecture is used for flexible devices on polyimide foils (Kapton). (Copyright © 2014, IEEE).²³

Figure 58 shows the output and transfer characteristics of [(a) and (b)] n-type sputtered IGZO TFT and [(c) and (d)] p-type spin-coated PFO/(7,5) SWNT FET fabricated on a rigid SiN_x substrates. These devices are the transistors used in the hybrid CMOS inverter, but they have been previously characterized individually in order to check their stand-alone performances without additional interconnections and parasitic currents, as found in the more complex CMOS layout. Moreover, once the IGZO was passivated, it was no longer possible to clean the substrate before the deposition of carbon nanotubes, thus introducing more variability in device performance and a less ideal behaviour. The IGZO TFT exhibits a low-voltage operation with an electron mobility of $\mu_e = 0.7 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, a threshold voltage of $V_{\text{TH}} = 4 \text{ V}$, and a sub-threshold swing of $SS = 0.12 \text{ V/dec}$. The low electron mobility compared to established literature values⁵² is attributed to the lack of annealing step and to the coplanar device architecture. The PFO/(7,5) SWNT FET yields a predominant p-type behaviour due to the interaction with the Al_2O_3 gate dielectric, as already explained in Section 4.2.3, low-voltage operation with a hole mobility of

$\mu_h = 0.02 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, a threshold voltage of $V_{TH} = -2.8 \text{ V}$, a sub-threshold swing of $SS = 0.42 \text{ V/dec}$, and clear current saturation. Even in this case, the visible current hysteresis is attributed to contaminants and filter residues from the polymer sorting procedure, as explained in Section 4.1.3.

It is important to observe that while L_c is fixed at $25 \mu\text{m}$ for both the p- and n-channel, W_c has been designed to be much longer for the p-channel, in order to compensate for the lower drain current and mobility, following equations (17) and (18). To achieve such optimization, an extensive transistor characterization has been used to design inverters with a centered midpoint voltage ($V_M = V_{DD}/2$). Figure 59 shows the circuit diagram of the hybrid CMOS inverter with the different p- and n-channel dimensions.

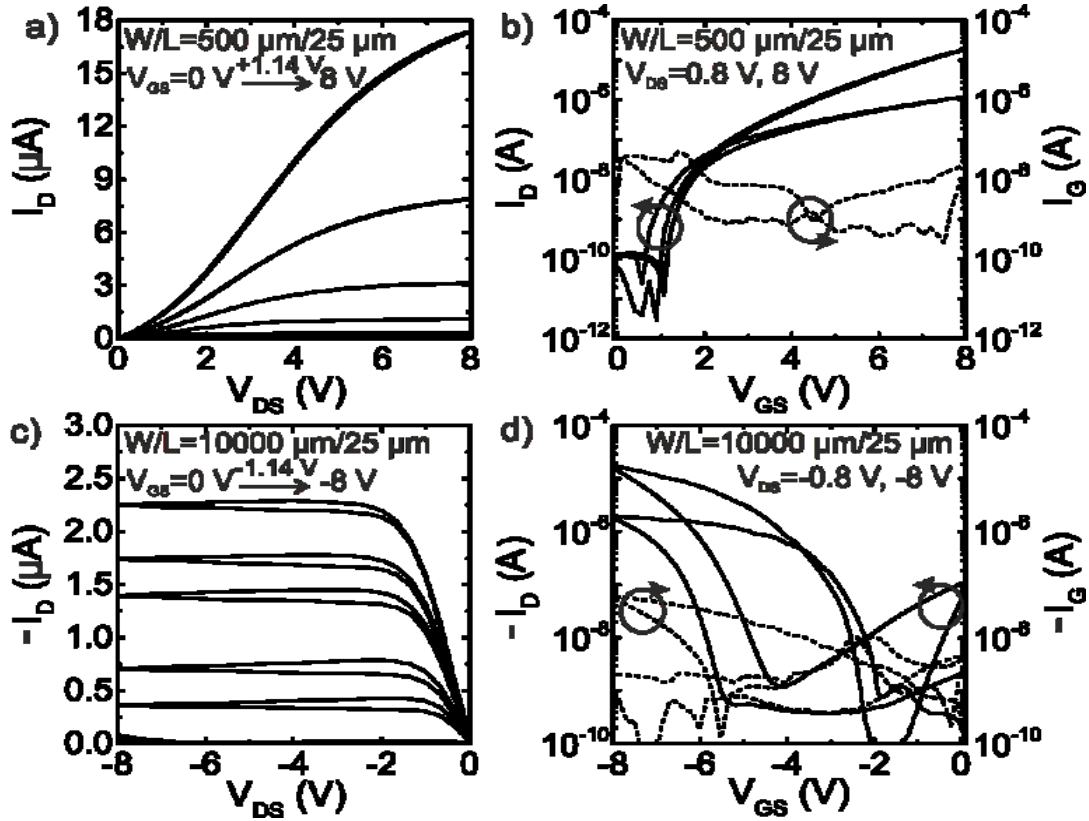


Figure 58: Output and transfer characteristics of [(a) and (b)] n-type sputtered IGZO and [(c) and (d)] p-type spin-coated PFO/(7,5) SWNT transistors fabricated on rigid SiN_x substrates and characterized in a nitrogen glovebox. All devices have $L_c = 25 \mu\text{m}$ while $W_c = 500 \mu\text{m}$ for n-type IGZO TFT and $W_c = 10000 \mu\text{m}$ for p-type PFO/(7,5) SWNT FET, in order to balance electron and hole currents during the inverter operation. (Copyright © 2014, IEEE).²³

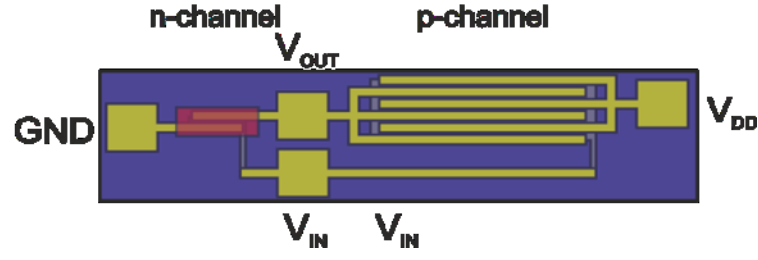


Figure 59: Circuit diagram of the hybrid CMOS inverter with the n- and p-channel transistors with same L_C but different W_C . (Copyright © 2014, IEEE).²³

Figure 60 shows (a) the voltage transfer characteristics and (b) the static gain of an hybrid CMOS inverter realized with a spin-coated PFO/(7,5) SWNT p-type FET and a sputtered IGZO n-type TFT on a SiN_x substrate.

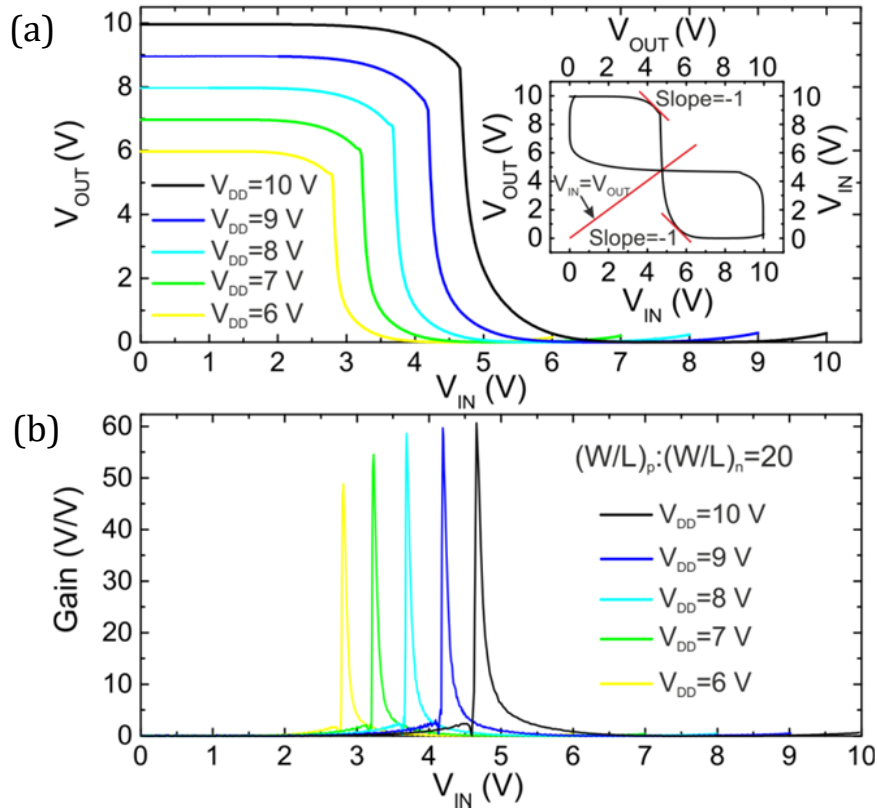


Figure 60: (a) VTC and (b) static gain of complementary inverter based on n-type sputtered IGZO and p-type spin-coated PFO/(7,5) SWNT TFTs on a SiN_x substrate, measured at different supply voltages $V_{DD} = 6, 7, 8, 9, 10\text{V}$. The inset shows the bi-stable hysteresis VTC at $V_{DD} = 10\text{V}$, used to calculate noise margins. (Copyright © 2014, IEEE).²³

The device has been characterized in a nitrogen glovebox with a low-voltage supply ranging from 6 V to 10 V. At $V_{DD} = 10\text{V}$, the inverter exhibits a midpoint voltage $V_M = 4.75\text{V}$, a static gain $G = 60.6\text{V/V}$, a perfect rail-to-rail output swing with

$V_{OH} = 9.95$ V and $V_{OL} = 0.28$ V, and excellent noise margins ($NM_H = 4.33$ V, $NM_L = 4$ V). Moreover, the static power dissipation for $V_{DD} = 10$ V is less than 5 μ W for V_{IN} set as HIGH or LOW, and it reaches a maximum of 17 μ W at $V_{IN} = V_M$, where both transistors are ON simultaneously. Similar results have been obtained by Kim et al.^{132,133} in 2014 and 2015, where complementary inverters based on inkjet-printed SWNTs and ZTO have been fabricated on SiO₂ and glass substrates, showing a low-voltage operation with $V_G \leq 5$ V and a maximum gain of 17 V/V with bottom-gate geometry¹³² and of 34 V/V with a double gate geometry.¹³³

The hybrid CMOS inverter has also been characterized after being exposed to air. Figure 61 shows the VTC and the static gain of the inverter measured under ambient conditions. After being exposed to air, the inverter is fully functional with $V_M = 5.1$ V and $G = 51.6$ V/V. These variations are attributed to changes in the performance of the unpassivated PFO/(7,5) SWNT FET in contact with oxygen, and they can be prevented with a proper encapsulation.

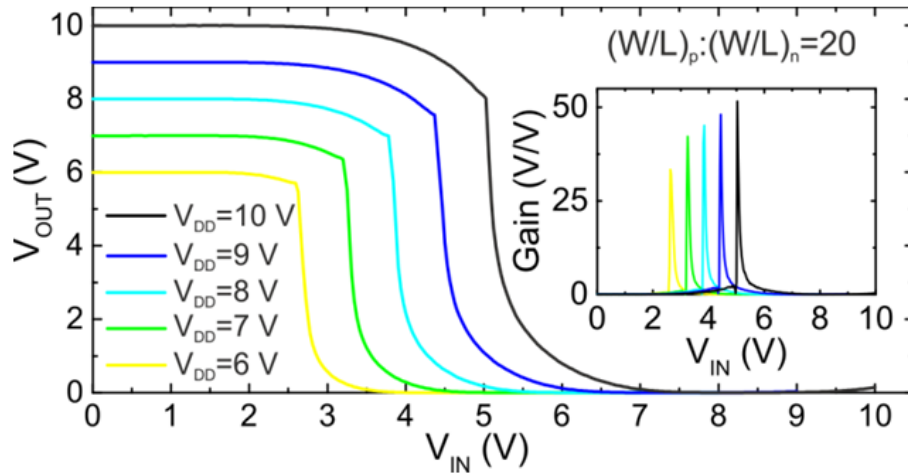


Figure 61: VTC and gain (inset) of an IGZO/SWNT complementary hybrid inverter fabricated on a rigid SiN_x substrate and characterized under ambient conditions. For $V_{DD} = 10$ V, the device operates with $V_M = 5.1$ V and $G = 51.6$ V/V. (Copyright © 2014, IEEE).²³

Finally, mechanical properties have also been studied by performing bending tests on the hybrid CMOS inverters fabricated on free-standing flexible polyimide foils. Initially, the IGZO and PFO/(7,5) SWNT transistors have been mechanically tested one at a time by comparing their transfer curves while flat and bent to a tensile radius of 1 cm, as shown in Figure 62. Both devices show only minor

variations upon the application of the tensile strain ($V_{TH,n} = +30$ mV, $V_{TH,p} = +20$ mV, $\mu_n = -0.8\%$, $\mu_p = +2\%$).

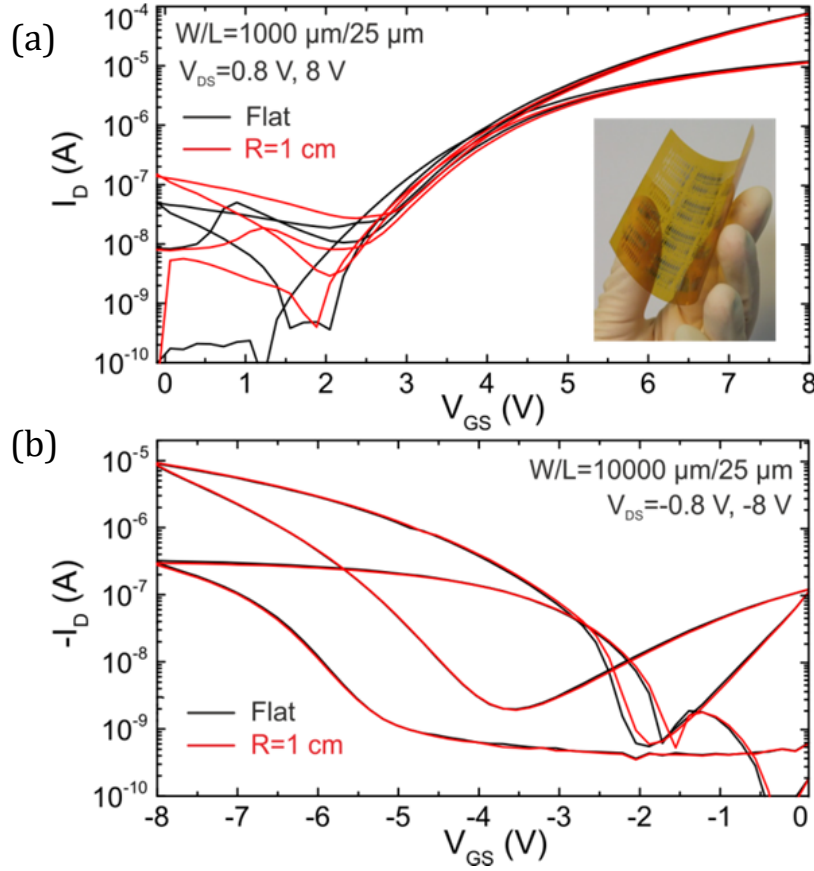


Figure 62: Transfer curves of mechanically flexible (a) IGZO and (b) PFO/(7,5) SWNT transistors fabricated on free-standing polyimide foils, measured while flat and bent to a tensile radius of 1cm. The inset shows a photograph of the fully processed free-standing mechanically flexible foil. Both devices show no major variations upon the application of the tensile strain. (Copyright © 2014, IEEE).²³

Figure 63 shows (a) the voltage transfer characteristics and (b) the static gain of an hybrid CMOS inverter realized with a spin-coated PFO/(7,5) SWNT p-type FET and a sputtered IGZO n-type TFT on a free-standing polyimide foil. The device has been characterized in a nitrogen glovebox while flat and bent around a 1 cm radius rod, with a low-voltage supply ranging from 7 V to 10 V. At $V_{DD} = 10$ V, the inverter exhibits a midpoint voltage of $V_M = 4.39$ V ($V_M = 4.43$ V), a static gain of $G = 87.1$ V/V ($G = 85.7$ V/V), which is the highest gain reported so far for this combination of materials, and a perfect rail-to-rail output swing for the flat (bent) circuit. The slightly variations in V_M and G during bending are attributed to the minor

parameters variation in the two transistors, to performance variability with time and to degradation due to electrical stress.

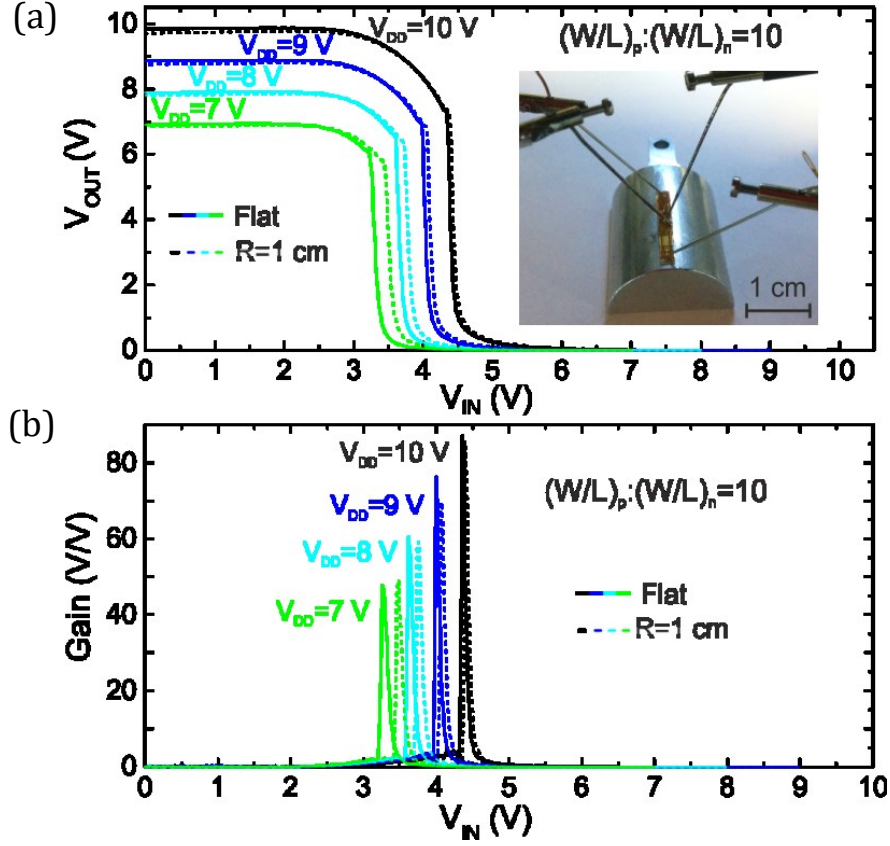


Figure 63: (a) VTC and (b) static gain of a mechanically flexible hybrid complementary inverter based on IGZO and PFO/(7,5) SWNT transistors on free-standing plastic foil, measured at $V_{DD} = 7, 8, 9, 10$ V while flat and bent to a tensile radius of 1 cm. For $V_{DD} = 10$ V, the inverter exhibits $V_M = 4.39$ V and $G = 87.1$ V/V for the flat circuit. The inset shows a photograph of the contacted flexible complementary inverter, bent to a tensile radius of 1 cm. (Copyright © 2014, IEEE).²³

4.3.4 Flexible CMOS Inverter Integrated with InO_x

Following the excellent results obtained with the hybrid IGZO/SWNT CMOS on rigid as well as flexible substrates, another semiconducting metal oxide was used, in order to achieve a circuit with fully solution-deposited semiconductors. Devices were realized by integrating a PFO/(7,5) SWNT FET with an InO_x TFT on the same substrate. Bottom-gate coplanar device architecture with 50 nm Al_2O_3 gate dielectric was used, like the schematic shown in Figure 57. InO_x was deposited from solution in air via ultrasonic spray pyrolysis, using a solution of 30 mg/ml indium

nitrate hydrate dissolved in deionized water.⁸ During the automated spray process, the substrate was heated to 250 °C and the InO_x was patterned in the n-channel using a shadow mask and then passivated with CYTOP, which also acted as a protective layer from the subsequent spin-coating of carbon nanotubes. Figure 64 shows the AFM topography image obtained in tapping-mode of InO_x deposited on Al₂O₃ surface. The film appears to be homogeneous with no grain boundaries.

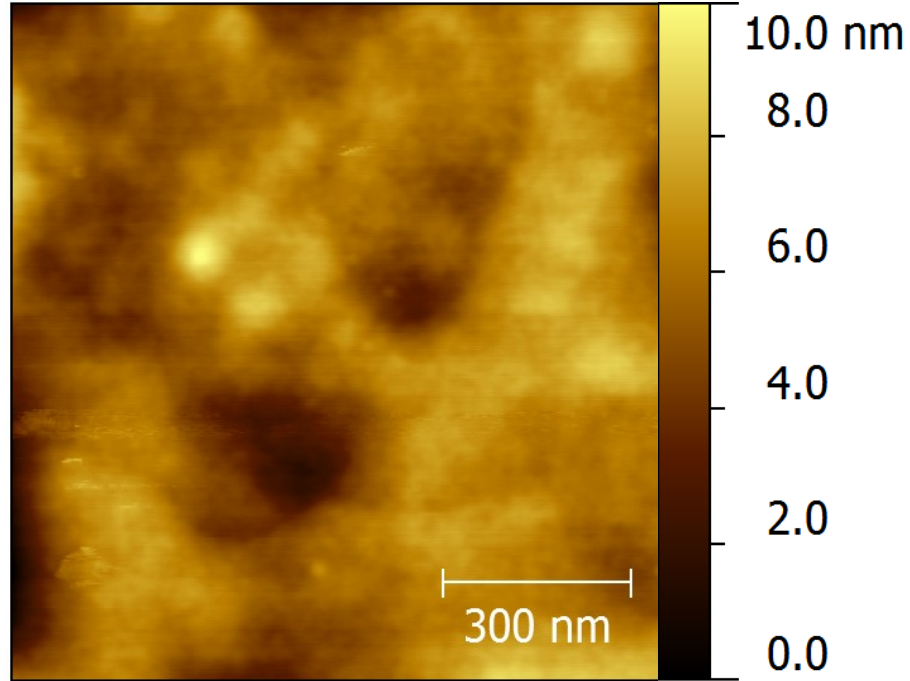


Figure 64: AFM topography in tapping-mode of InO_x film deposited by ultrasonic spray pyrolysis on Al₂O₃ surface. The film appears to be homogeneous with no grain boundaries. (Copyright © 2014, IEEE).²³

Also in this case, the two n- and p-type transistors comprising the hybrid CMOS inverter have been characterized first. Figure 65 shows the output and transfer characteristics of [(a) and (b)] n-type solution-processed InO_x TFT and [(c) and (d)] p-type spin-coated PFO/(7,5) SWNT FET fabricated on a rigid SiN_x substrates. The solution-processed InO_x TFT exhibits a low-voltage operation with an electron mobility of $\mu_e = 0.02 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, a threshold voltage of $V_{\text{TH}} = 1.2 \text{ V}$, and a sub-threshold swing of $SS = 1.5 \text{ V/dec}$. The high OFF current is attributed to the high InO_x carrier conductivity, caused by the generation of intrinsic defects during the spray process.

⁸ Ultrasonic spray pyrolysis of InO_x has been performed by Dr Luisa Petti at Imperial College London, as part of a collaboration.

The PFO/(7,5) SWNT FET yields a predominant p-type behaviour due to the interaction with the Al_2O_3 gate dielectric, as already explained in Section 4.2.3, low-voltage operation with a hole mobility of $\mu_h = 0.01 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, a threshold voltage of $V_{\text{TH}} = -2.4 \text{ V}$, a sub-threshold swing of $\text{SS} = 1.15 \text{ V/dec}$, and clear current saturation. Also in this case, the visible current hysteresis is attributed to contaminants and filter residues from the polymer sorting procedure, as explained in Section 4.1.3.

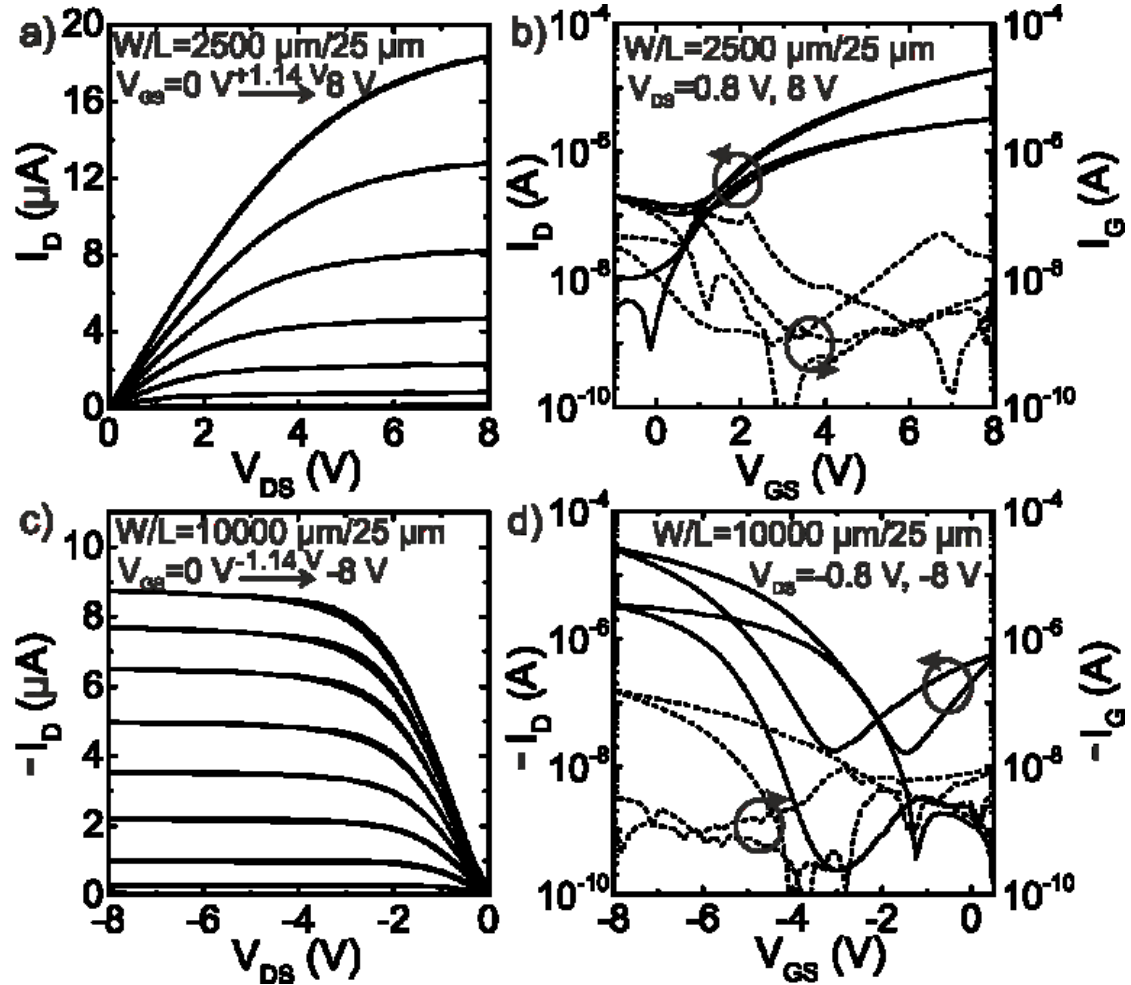


Figure 65: Output and transfer characteristics of [(a) and (b)] n-type spray-coated InO_x and [(c) and (d)] p-type spin-coated PFO/(7,5) SWNT transistors fabricated on rigid SiN_x substrates and characterized in a nitrogen glovebox. All devices have $L_c = 25 \mu\text{m}$ while $W_c = 2500 \mu\text{m}$ for n-type InO_x TFT and $W_c = 10000 \mu\text{m}$ for p-type PFO/(7,5) SWNT FET, in order to balance electron and hole currents during the inverter operation. (Copyright © 2014, IEEE).²³

In order to compensate for the difference in the drain currents and obtain a centered midpoint voltage, channel widths have been designed so that $W_{c,p}/W_{c,n} =$

4, whereas $L_C = 25 \text{ } \mu\text{m}$ for both devices. Figure 66 shows the voltage transfer characteristics and the static gain (inset) of an hybrid CMOS inverter realized with a spin-coated PFO/(7,5) SWNT p-type FET and a solution-processed InO_x n-type TFT deposited on a SiN_x substrate and characterized in a nitrogen glovebox for a low-voltage supply ranging from 6 V to 10 V. For $V_{DD} = 10 \text{ V}$, the solution-processed hybrid inverter yields a midpoint voltage of $V_M = 5.1 \text{ V}$, a static gain of $G = 48.4 \text{ V/V}$, and a perfect rail-to-rail output swing.

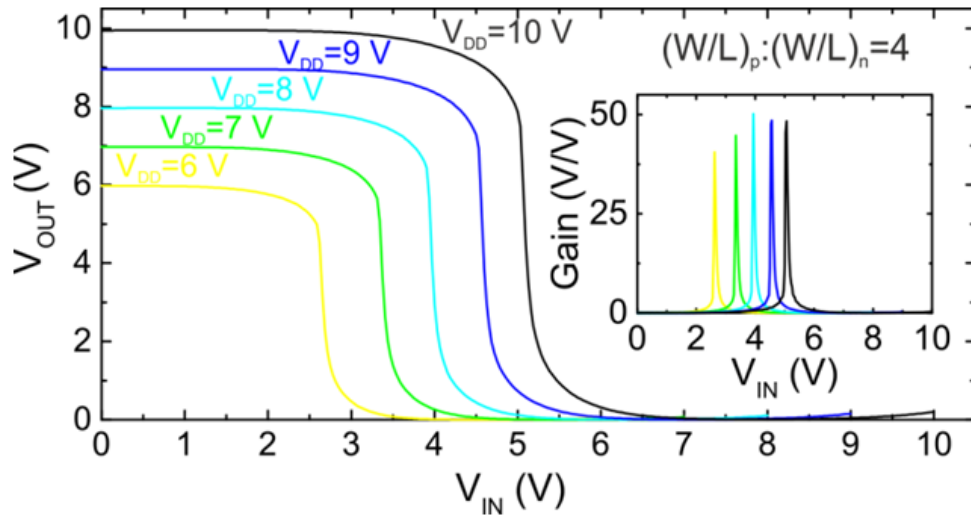


Figure 66: VTC and static gain (inset) of hybrid CMOS inverter with fully solution-processed semiconductors, based on spray-coated n-type InO_x and spin-coated p-type PFO/(7,5) SWNT transistors on rigid SiN_x substrate, measured at $V_{DD} = 6, 7, 8, 9, 10 \text{ V}$ in a nitrogen glovebox. For $V_{DD} = 10 \text{ V}$, $V_M = 5.1 \text{ V}$ and $G = 48.4 \text{ V/V}$. (Copyright © 2014, IEEE).²³

Finally, the same deposition process for both InO_x and SWNT was performed on flexible polyimide foils in order to assess their mechanical properties and compare them to the high-performing hybrid IGZO/SWNT bendable CMOS inverter. Unfortunately, it was possible to characterize devices only while flat on the polyimide substrate. Once they were bent around a 1 cm radius rod, none of them was still working, thus it has not been possible to perform an extensive electrical characterization. Figure 67 shows the voltage transfer characteristics and the static gain (inset) of an hybrid CMOS inverter realized with a spin-coated PFO/(7,5) SWNT p-type FET and a solution-processed InO_x n-type TFT deposited on a flexible polyimide foil and characterized flat in a nitrogen glovebox for a low-voltage supply ranging from 6 V to 10 V. For $V_{DD} = 10 \text{ V}$, the flexible inverter yields a midpoint

voltage of $V_M = 3.97$ V, a static gain of $G = 22$ V/V, and an output swing with $V_{OH} = 9.2$ V. The lower device performance with respect to the rigid InO_x/SWNT inverter is attributed to the poor performance of the flexible InO_x TFT, caused by the increased surface roughness and lower thermal conductivity of the polyimide foil when compared to SiN_x substrates.

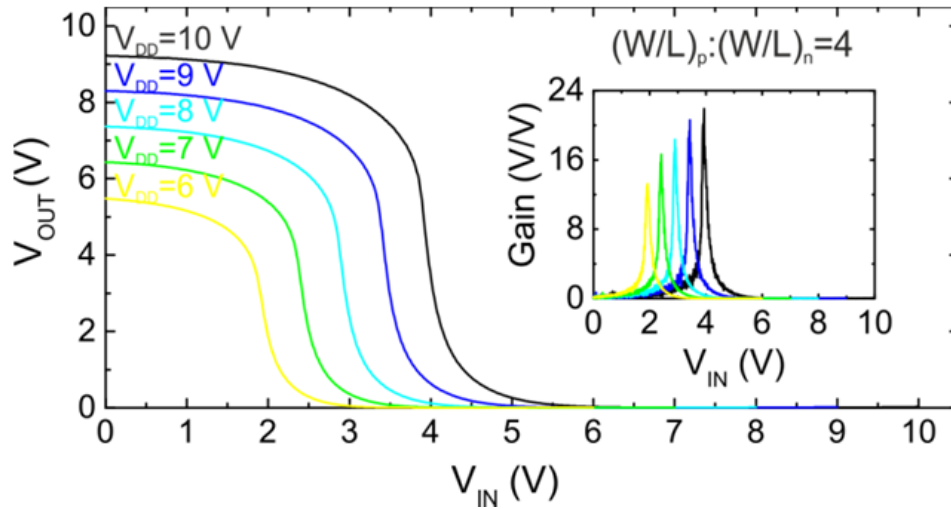


Figure 67: VTC and static gain (inset) of flexible hybrid CMOS inverter with fully solution-processed semiconductors, based on spray-coated n-type InO_x and spin-coated p-type PFO/(7,5) SWNT TFTs on free-standing polyimide foil, measured at $V_{DD} = 6, 7, 8, 9, 10$ V. For $V_{DD} = 10$ V, $V_M = 3.97$ V and $G = 22$ V/V. Differences between flexible and rigid InO_x/SWNT inverters are attributed to the reduced performance of the flexible InO_x TFT. (Copyright © 2014, IEEE).²³

4.3.5 Conclusions

In conclusion, polymer-sorted semiconducting SWNTs have been successfully employed for low-voltage unipolar logic circuits. Moreover, they have been integrated with n-type semiconducting metal oxides on rigid as well as free-standing flexible polyimide foils, and high-performing hybrid CMOS inverters have been realized. Bendable devices based on spin-coated PFO/(7,5) SWNTs and sputtered IGZO exhibited gains as high as 87.1 V/V and a perfect output swing with a low-voltage operation ($V_{DD} = 10$ V), even while bent to a radius of 1 cm. Furthermore, PFO/(7,5) SWNTs have been integrated with spray-coated InO_x onto free-standing plastic substrates, and hybrid CMOS inverters based on fully solution-deposited semiconductors have been realized, paving the way towards large-area solution-processed flexible electronics.

4.4 Alternative Processing Methods for SWNT FETs

4.4.1 Introduction

All previous experimental results have been obtained with polyfluorene-based polymer-sorted semiconducting SWNTs deposited from solution on various substrates. In this section, preliminary results of alternative processing methods to disperse and deposit SWNTs are presented. PFO-BPy/(6,5) SWNTs have been deposited onto SiO₂ substrates by vacuum film transfer in air, thus avoiding re-dispersion in solution. Conjugated polymers absorbing in the visible range, such as P3HT (Poly(3-hexylthiophene-2,5-diyl)) and PTB7 (Poly({4,8-bis[(2-ethylhexyl)oxy]benzo[1,2-b:4,5-b']dithiophene-2,6-diyl}{3-fluoro-2-[(2-ethylhexyl)carbonyl]thieno[3,4-b]thiophenediyl})), have been used as sorting polymers in order to create stable photoactive blends with SWNTs. Both these alternative methods to disperse and deposit SWNTs have been accurately tested with bottom-gate top-contact FETs, as part of ongoing collaborations within the FP7 project POCAONTAS.

4.4.2 Brief Study on Vacuum Film Transfer⁹

Controlled deposition of large-area patterned films of carbon nanotubes with high homogeneity and high conductivity is yet to be accomplished. An interesting deposition technique currently under investigation by many research groups is called *film transfer* or *transfer printing*, and it is commonly used to deposit and pattern conductive electrodes made of mixed metallic and semiconducting nanotubes.^{134–136} The vacuum film transfer process starts from the vacuum filtration step of the purification process, and instead of dissolving the cellulose membrane and re-disperse the nanotubes in solution, the membrane is attached to a substrate and carbon nanotubes are transferred from the membrane to the new substrate. In this way, the resulting film is more uniform, homogeneous, with a controllable thickness, and carbon nanotubes are less aggregated. Figure 68 shows the different process steps of the vacuum film transfer method on glass, starting from the vacuum filtration step of the polymer sorting method (Figure 20).

⁹ Collaboration with Miss Imge Namal, under the supervision of Prof Tobias Hertel at Würzburg University. Results have been obtained and analysed partially at Imperial College and partially at Würzburg University. Namal, I. *et al.*, to be submitted (2016).¹⁴⁹

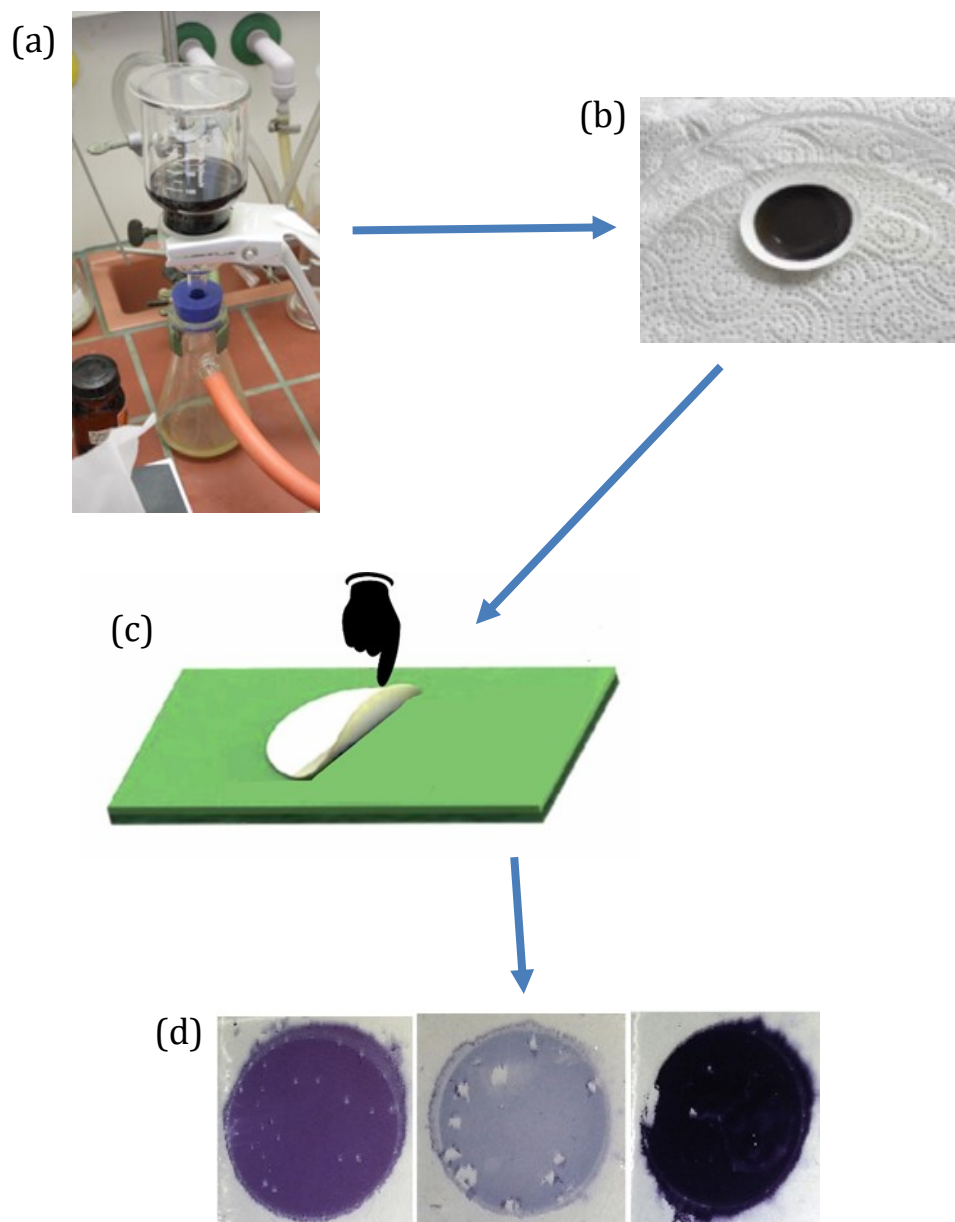


Figure 68: Pictures taken during the various steps of the vacuum film transfer method. (a) The solution is vacuum filtered to remove the excess polymer, (b) the remaining cellulose membrane with the nanotube film on one side is taken and attached upside down to the substrate, (c) the membrane is pressed for 10 minutes on a hotplate at 100°C to make it adheres to the glass substrate. Finally, the substrate is rinsed with acetone for many hours to dissolve the membrane and (d) the resulting films are ready to be used in devices. Depending on the initial amount of filtered solution, the resulting films will have different thicknesses and so different colours. These pictures have been taken by Miss Imge Namal at Würzburg University.

Unlike the standard film transfer process, where mixed SWNT are used as electrodes, in this work the vacuum film transfer process starts from the vacuum

filtration of the PFO-BPy/(6,5) SWNT solution, which is necessary to remove the excess PFO-BPy polymer and keep only the semiconducting (6,5) SWNTs. At this point, the cellulose membrane with the nanotube film on one side is not dissolved but it is wetted with toluene and attached upside down to the substrate. Pressure is applied so that the toluene wetted films are properly sticking upside down on the cleaned substrates in air. The substrates with the films are then left to dry at 100 °C in air for 10 minutes with some weight on in order to maintain the pressure. Finally, they are placed in an acetone bath for at least 3 hours and rinsed every 20 minutes to properly dissolve the filter residues. When Si⁺⁺/SiO₂ substrates are used, bottom-gate top-contact FETs can be fabricated. Best results have been obtained with 100 nm SiO₂ dielectric and 40 nm Au source and drain electrodes, thermally-evaporated on top of the SWNT films with shadow masks.

Figure 69 shows a tapping-mode AFM topography image of a PFO-BPy/(6,5) SWNT film transferred on SiO₂.

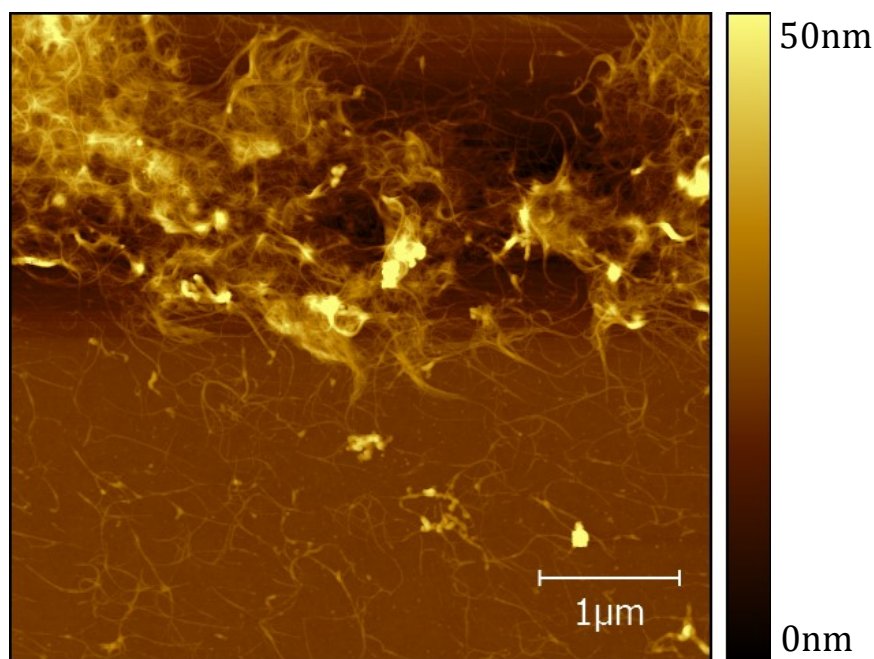


Figure 69: Tapping-mode AFM topography image of a PFO-BPy/(6,5) SWNT film transferred on SiO₂. The initial amount of vacuum filtrated solution is 0.25ml, not enough to form a uniform and homogeneous layer on the cellulose membrane.

In this case 0.25 ml of solution has been vacuum filtrated and transferred on the substrate, resulting in a very inhomogeneous layer of carbon nanotubes, as this

amount of solution is not enough to form a uniform and homogeneous layer on the cellulose membrane.

Figure 70 shows the (a) transfer and (b) output characteristics of a PFO-BPy/(6,5) SWNT FET with $L_C = 40 \mu\text{m}$ and $W_C = 1000 \mu\text{m}$, transferred from the cellulose membrane to SiO_2 .

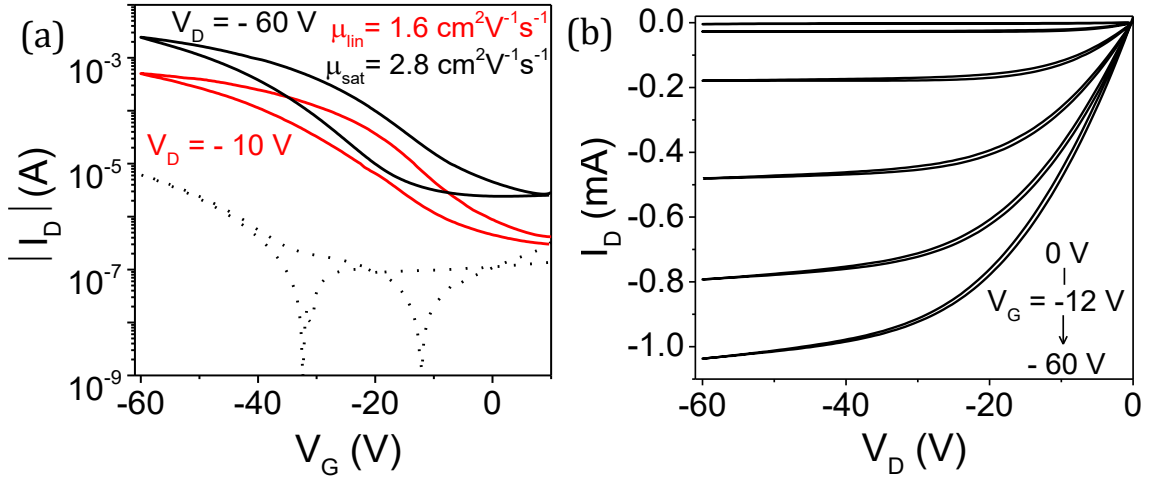


Figure 70: (a) Transfer and (b) output characteristics of a PFO-BPy/(6,5) SWNT FET with $L_C = 40\mu\text{m}$ and $W_C = 1000\mu\text{m}$, transferred from the cellulose membrane to SiO_2 . The initial amount of solution is 0.25ml.

Even though the initial amount of solution is only 0.25 ml and the film morphology is not uniform, as the AFM image in Figure 69 suggests, the device is well performing, with a saturation mobility of $2.8 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, a current ON/OFF ratio of 10^3 , predominant p-type behaviour and only a hint of current hysteresis.

Figure 71 shows the transfer characteristic of a PFO-BPy/(6,5) SWNT FET spin-coated in air from the same solution used for the film transfer process of device shown in Figure 70. It is interesting to observe that there are major differences between the film transferred FET behaviour and the spin-coated FET behaviour. First of all, the current ON/OFF ratio is much higher for the spin-coated device, with a much lower OFF current but also a lower ON current, leading to a lower linear and saturation mobility. Secondly, current hysteresis is more pronounced in the spin-coated device. A possible explanation is that, in addition to surface trap states present at the interface between SiO_2 and SWNTs (see Section 4.1.3), other contaminants are present in the solution, which are not present in the transferred

film. Residues of the cellulose membrane can indeed end up in the SWNT dispersion if not properly dissolved in acetone, and contribute to the current hysteresis.

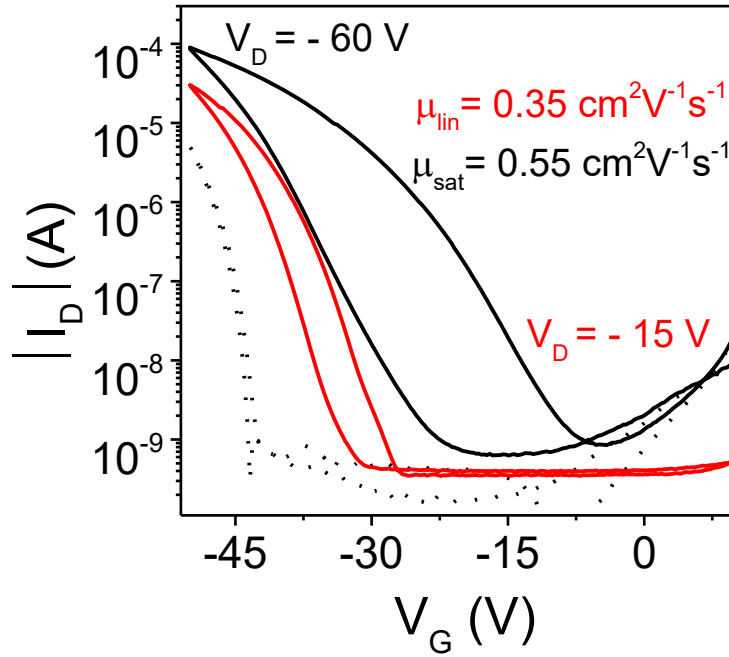


Figure 71: Transfer characteristic of a PFO-BPy/(6,5) SWNT FET with $L_C = 40\mu\text{m}$ and $W_C = 1000\mu\text{m}$, spin-coated from solution in air.

Another contribution to the hysteresis may come from the nanotube surface morphology. It has been already mentioned that vacuum filtered nanotubes form a more compact film, with less aggregates and bundles. It is however already known that carbon nanotubes do aggregate in solution and form bundles, which are then deposited on the substrate through solution-based deposition techniques, such as spin-coating.

The vacuum film transfer technique has been further exploited to study the dependence of charge carrier mobility on SWNT film thickness. Based on the initial amount of filtered solution, SWNT films with different thicknesses are obtained on the cellulose membrane and transferred to the SiO_2 substrate. Figure 72 shows the (a) linear and (b) saturation mobility of many PFO-BPy/(6,5) SWNT FETs as a function of SWNT film thickness. In both cases, mobility increases with the film thickness following a linear behaviour, as indicated by the two dashed best fit lines. Because the surface morphology of the SWNT films is not uniform, devices fabricated in different parts of the same film behave quite differently, and this is

particularly evident from the mobility box plot and whiskers extension towards outliers.

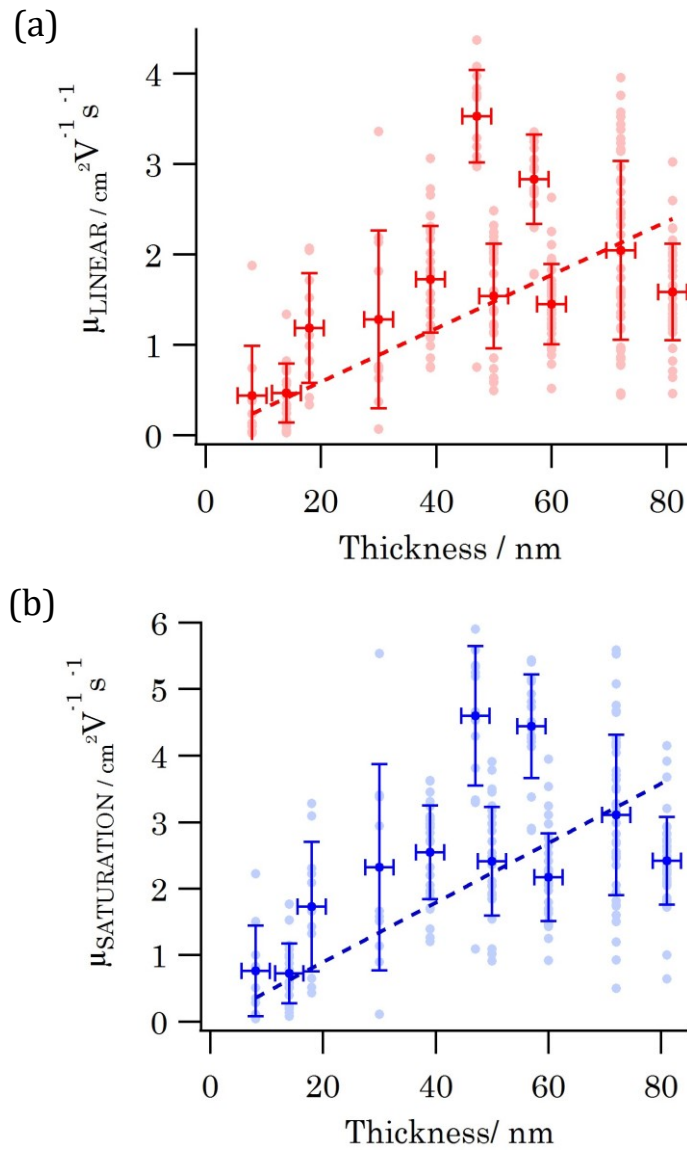


Figure 72: (a) Linear and (b) saturation mobility box plot of PFO-BPy/(6,5) SWNT FETs as a function of SWNT film thickness. Many devices have been characterized per each thickness and analyzed, in order to account for device-to-device variability. Dashed lines represent the two linear best fit lines. These two plots have been prepared by Miss Imge Namal at Würzburg University.

These results suggest that a linear trend is present between charge carrier mobility and the SWNT film thickness. However, increasing even further the film thickness could affect TFT performance, and mobility will likely remain constant or even decrease due to gate voltage screening and to the presence of charge carrier trap states in the thick channel layer.

4.4.3 Preliminary Results on Conjugated Polymers/SWNT Blends¹⁰

Conjugated polymers absorbing in the visible region of the solar spectrum, such as P3HT and PTB7, are commonly employed as donor materials for organic solar cells. Depending on the choice of the acceptor material, power conversion efficiencies higher than 6% have been recently demonstrated for P3HT,^{137,138} and higher than 10% when PTB7^{139,140} is used. Moreover, these polymers have a lower LUMO^{138,141} and a higher conductivity than polyfluorene-based polymers, which makes them the best replacement of PFO and derivatives as the sorting and dispersing polymer in SWNT dispersions, especially for optoelectronic and photovoltaic applications.^{142,143} The main problem regards the selectivity of those polymers towards the semiconducting nanotubes, which is much lower than for polyfluorene-based polymers. Several studies have been already performed on the increase of performance of polymer TFTs with the addition of non-percolating networks of carbon nanotubes acting as conducting bridges between the crystalline regions of the polymer film.^{144–148} Hsieh et al.¹⁴⁴ obtained an increase in mobility by a factor of more than 7 by blending inkjet-printed SWNTs with inkjet-printed PQT-12 (poly(5,5'-bis(3-dodecyl-2-thienyl)-2,2'-bithiophene), with respect to pristine PQT-12 TFT mobility. Similarly, Lin et al.¹⁴⁷ and Park et al.¹⁴⁶ both obtained an enhancement in TFT mobility by a factor of 10 or more, by adding carbon nanoparticles and carbon nanotubes to the P3HT solution, prior to film formation.

In the following study, bottom-gate top-contact TFTs with 100 nm SiO₂ dielectric and 30 nm of Au source and drain electrodes have been fabricated by spin-coating either a dispersion of n-SWNTs, a blend of polymer/SWNT, a bilayer of SWNT + polymer, or a combination of those, in order to evaluate the different interactions occurring at the nanotube/polymer interface.

The polymer solutions have been prepared by dissolving P3HT and PTB7 with a concentration of 5 mg/ml in ODCB (1,2-Dichlorobenzene). The two solutions have then been stirred overnight at 60 °C. The SWNTs solutions have been prepared by dispersing 0.5 mg/ml of n-SWNTs either in ODCB and DMF (Dimethylformamide).

¹⁰ Collaboration with Mrs Diana Figueroa, under the supervision of Prof Guglielmo Lanzani at Istituto Italiano di Tecnologia (CNST). Results have been obtained and analysed partially at Imperial College and partially at Istituto Italiano di Tecnologia (CNST).

The solutions were then sonicated for 1 hour, centrifuged for 30 minutes at 12000 rpm, and finally the supernatant was collected. For the polymer/SWNT blends, different ratios have been tested, with the best one being 2:0.5 mg/ml in ODCB. The different blends were then stirred overnight at 60 °C, sonicated for 1 hour, centrifuged for 15 minutes at 12000 rpm, and finally the supernatant was collected. Table 2 summarises the current ON/OFF ratio and mobility measured in TFTs with SWNT, P3HT and PTB7 deposited with different layer configurations. Rows highlighted in green corresponds to results obtained with P3HT, while rows highlighted in orange corresponds to results obtained with PTB7.

As shown in Table 2, among the many trials done, only few of them produced working devices with acceptable performance, more specifically those with SWNT + polymer bilayers and the blends with 2:0.5 mg/ml ratio of polymer/SWNT. Unfortunately, SWNTs alone could be dispersed only with a very low concentration of 0.5 mg/ml, thus no electrical connections could be made by the nanotubes in the TFT channel, and no SWNT devices were working.

Table 2: Current ON/OFF ratio and mobility measured in TFTs with SWNT, P3HT and PTB7 deposited with different layer configurations. To simplify the comparison between the different layer configurations, devices with P3HT are highlighted in green, and with PTB7 in orange.

	LAYER CONFIGURATIONS	TFT	ON/OFF	μ (cm ² /Vs)
1	0.5mg/ml SWNT in DMF	NO	-	-
2	0.5mg/ml SWNT in ODCB	NO	-	-
3	5mg/ml P3HT in ODCB	YES	4x10 ²	0.85x10 ⁻³
4	5mg/ml PTB7 in ODCB	YES	10 ³	1.2x10 ⁻³
5	2:0.5mg/ml P3HT:SWNT in ODCB	YES	10 ²	0.13
6	2:0.5mg/ml PTB7:SWNT in ODCB	YES	2.2x10 ⁰	1.1
7	1:0.5mg/ml P3HT:SWNT in ODCB	NA	-	-
8	0.5:0.5mg/ml P3HT:SWNT in ODCB	NA	-	-
9	0.5:1mg/ml P3HT:SWNT in ODCB	NA	-	-
10	0.5:0.5mg/ml P3HT:SWNT in DMF	NA	-	-
11	2:0.8mg/ml P3HT:SWNT in ODCB	NA	-	-
12	2:1mg/ml P3HT:SWNT in ODCB	NA	-	-
13	2:2mg/ml P3HT:SWNT in ODCB	NA	-	-
14	2:0.7mg/ml P3HT:SWNT in DMF	NA	-	-
15	BILAYER SWNT in DMF+P3HT in ODCB	YES	1.3x10 ³	3x10 ⁻³
16	BILAYER SWNT in DMF+PTB7 in ODCB	YES	2.5x10 ³	1.8x10 ⁻³
17	BILAYER P3HT:SWNT (2:0.5mg/ml)+P3HT in ODCB	YES	1.2x10 ³	0.12
18	BILAYER PTB7:SWNT (2:0.5mg/ml)+PTB7 in ODCB	YES	3.2x10 ⁰	0.8
19	BILAYER P3HT:SWNT (2:0.5mg/ml)+PTB7 in ODCB	NA	-	-
20	BILAYER PTB7:SWNT (2:0.5mg/ml)+P3HT in ODCB	NA	-	-

Figure 73 shows an AFM topography image of SWNTs dispersed in DMF and spin-coated on a SiO₂ substrate.

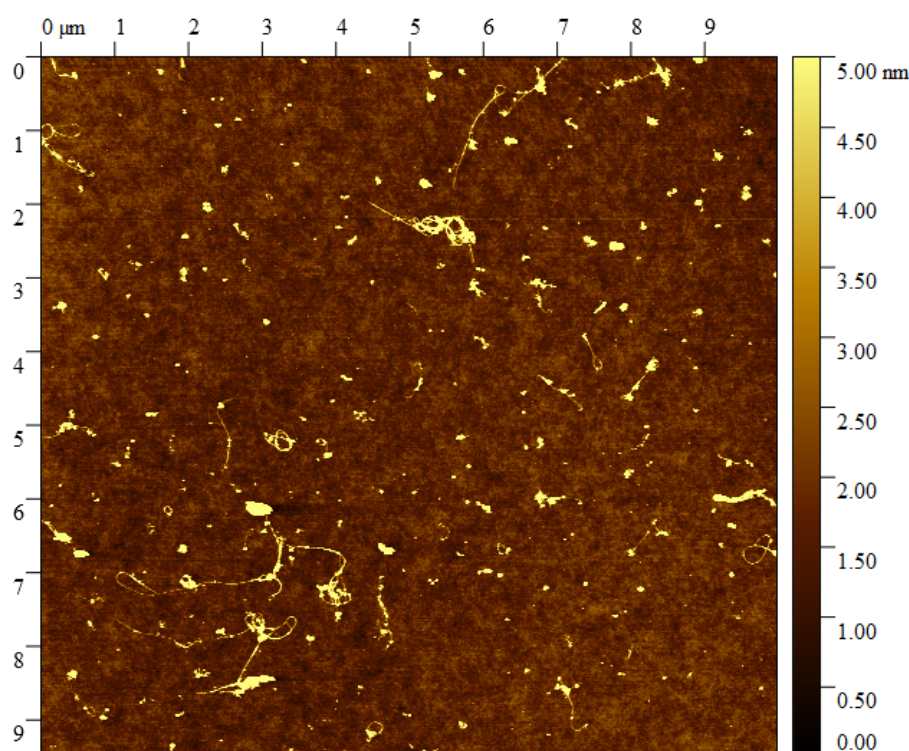


Figure 73: Tapping-mode AFM topography image of SWNTs dispersed in DMF and spin-coated on a SiO₂ substrate. No electrical connection is made between adjacent nanotubes, and thus TFTs cannot work.

The main purpose of this study is to enhance the performance of P3HT and PTB7 TFTs through the addition of semiconducting carbon nanotubes, acting as bridges with a high electrical conductivity. As a control experiment, TFTs with only P3HT and only PTB7 have been fabricated and characterized, as shown in Figure 74. In order to improve the performance polymer TFTs, and especially to enhance the ON current, TFTs comprised of a bilayer structure with SWNTs in DMF as the bottom layer and the polymers in ODCB as the top layer injecting into the Au electrode have been fabricated.

Orthogonality is the reason for the choice of DMF and ODCB as solvents, thus enabling the deposition of a multi-layer structure without dissolving the layers underneath.

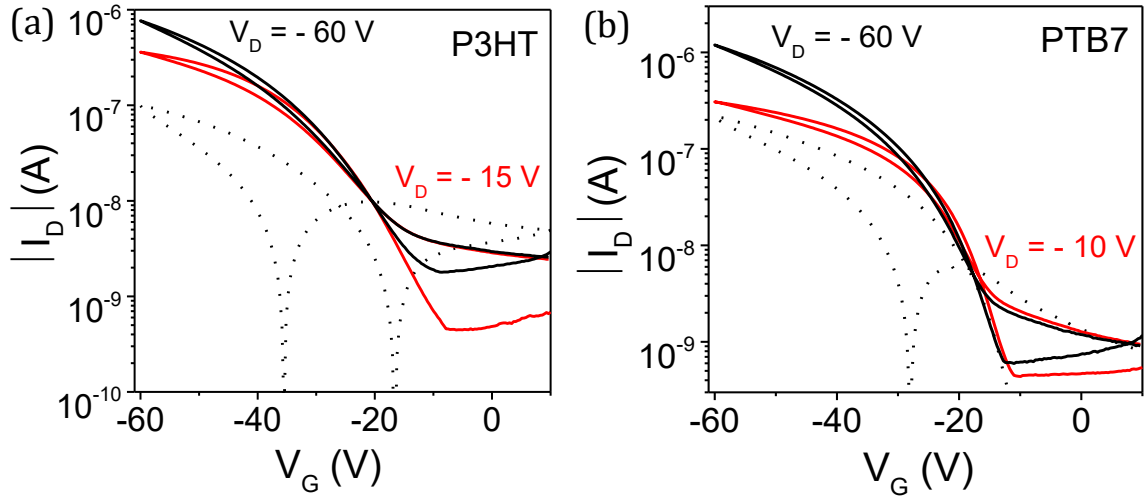


Figure 74: Transfer characteristics of (a) P3HT and (b) PTB7 TFTs, spin-coated from solution on 100nm SiO₂. Both devices are p-type, with a good current ON/OFF ratio, low OFF current and no visible current hysteresis. P3HT TFT shown in (a) corresponds to device #3 in Table 2, while PTB7 TFT shown in (b) corresponds to device #4 in Table 2.

Figure 75 shows the transfer characteristics of TFTs with the SWNT + polymer bilayer structure.

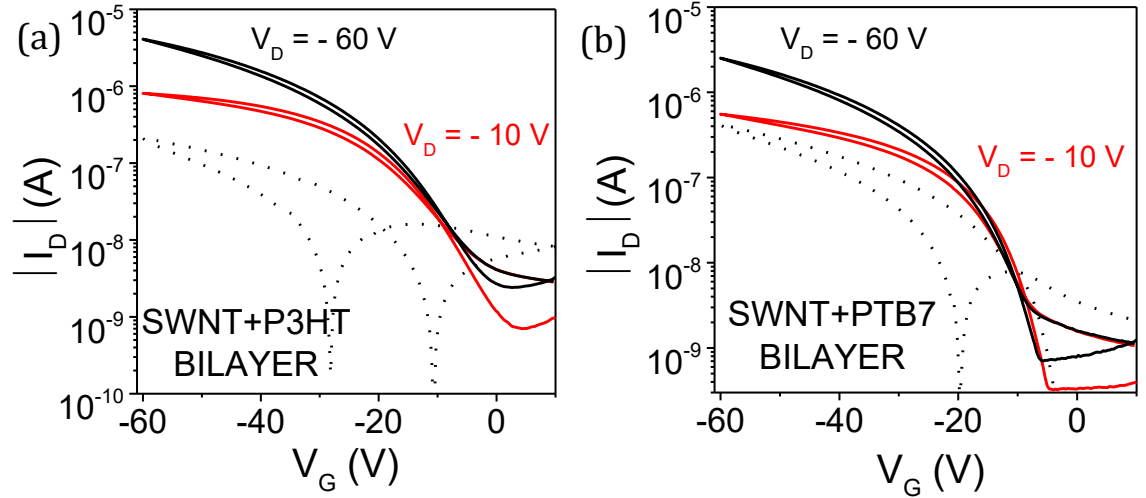


Figure 75: Transfer characteristics of (a) SWNT + P3HT and (b) SWNT + PTB7 bilayer TFTs, sequentially spin-coated from solution on 100nm SiO₂. Both devices are p-type, with a good current ON/OFF ratio, low OFF current and no visible current hysteresis. SWNT+P3HT TFT shown in (a) corresponds to device #15 in Table 2, while SWNT+PTB7 TFT shown in (b) corresponds to device #16 in Table 2.

For both TFTs, the current ON/OFF ratio and the OFF current are almost unchanged with respect to devices with only polymer, however, the ON current is slightly higher, which leads to higher mobility values, as also reported in Table 2. This means that the SWNT bottom layer is effectively enhancing charge transport

along the TFT channel, even though charge injection from the Au electrode to the top polymer layer down to the nanotube layer still remains a slow process.

Figure 76 represents the schematic cross section of the bilayer TFT, in which the role of both layers is pointed out.

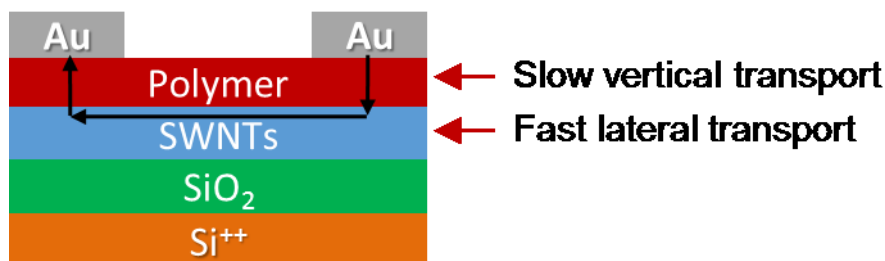


Figure 76: Schematic representation of the bilayer TFT. The bottom SWNT layer efficiently transports holes from one side of the channel to the other, while the top polymer layer, either P3HT or PTB7, slowly transports holes vertically from the electrodes to the SWNT layer and vice versa.

In order to improve vertical transport, SWNTs have been blended together with P3HT and PTB7 in ODCB, with the optimum ratio of 2:0.5 mg/ml (polymer to SWNT). As already mentioned, both P3HT and PTB7 have a lower selectivity than polyfluorene-based polymers towards the extraction of a specific nanotube chirality. Figure 77 shows the absorption spectra of 2:0.5 mg/ml blends of (a) P3HT/SWNTs and (b) PTB7/SWNTs in ODCB. The main peak in the visible range corresponds to the absorption of both P3HT and PTB7, while the smaller peaks around $\lambda = 1000$ nm correspond to the absorption of (6,5), (7,5) and (7,6) semiconducting nanotube chirality. However, a high amount of residual metallic nanotubes is expected to be present in these blends due to the weak polymer selectivity.

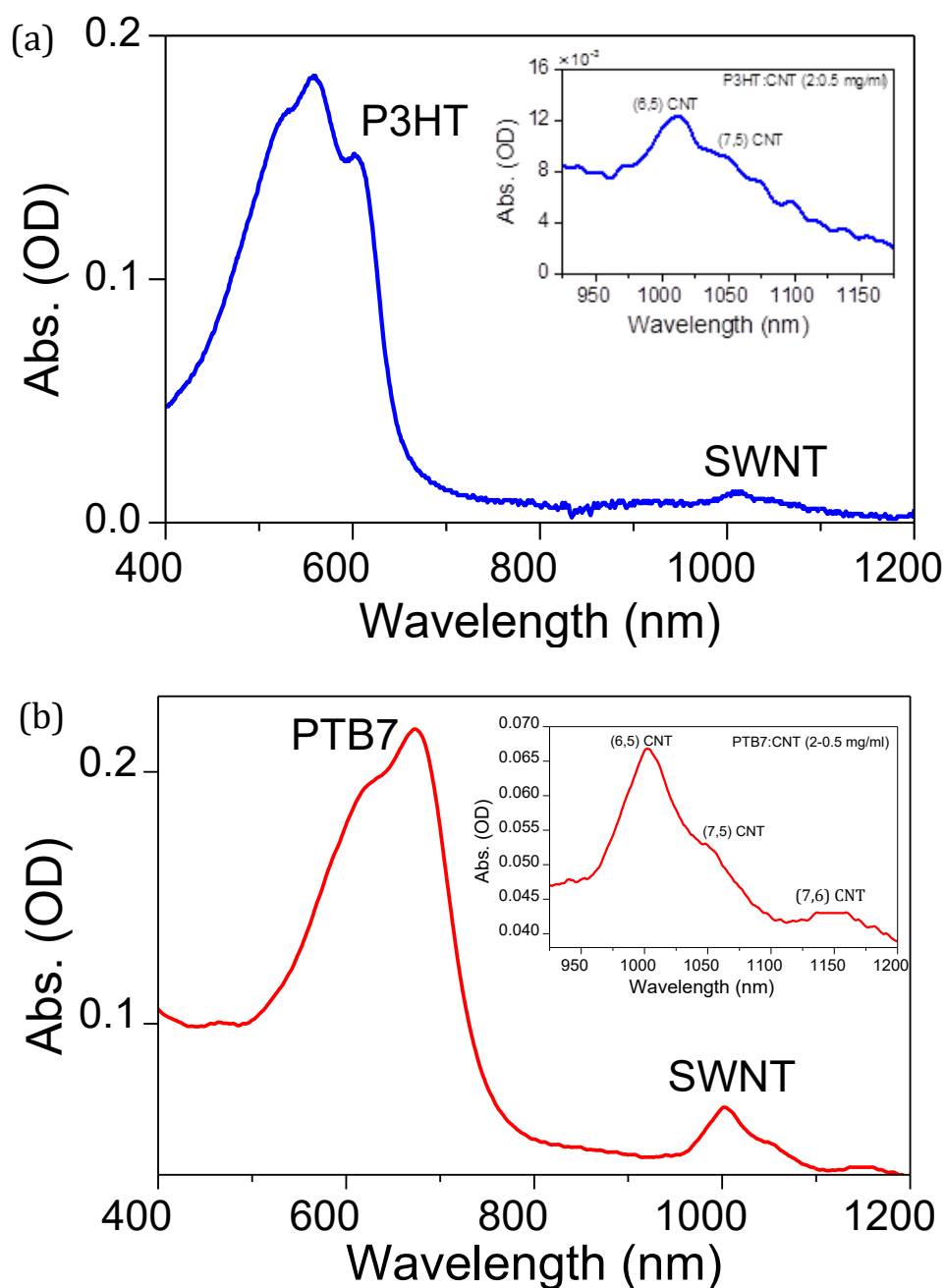


Figure 77: Absorption spectra of (a) P3HT/SWNT blend and (b) PTB7/SWNT blend in ODCB. The peak at $\lambda = 560\text{nm}$ in (a) corresponds to the absorption of P3HT, while the peak at $\lambda = 680\text{nm}$ in (b) corresponds to the absorption of PTB7. Both in spectra (a) and (b), the small peaks around $\lambda = 1000\text{nm}$ (insets) correspond to the absorption of SWNTs. Carbon nanotube selectivity is not as good as in Figure 30 and Figure 45, where PFO and PFO-BPy have been used, respectively.

Figure 78 shows an AFM topography image of the P3HT/SWNT blend spin-coated on a SiO_2 substrate, where SWNTs are well visible in the polymer matrix, covering well the entire surface.

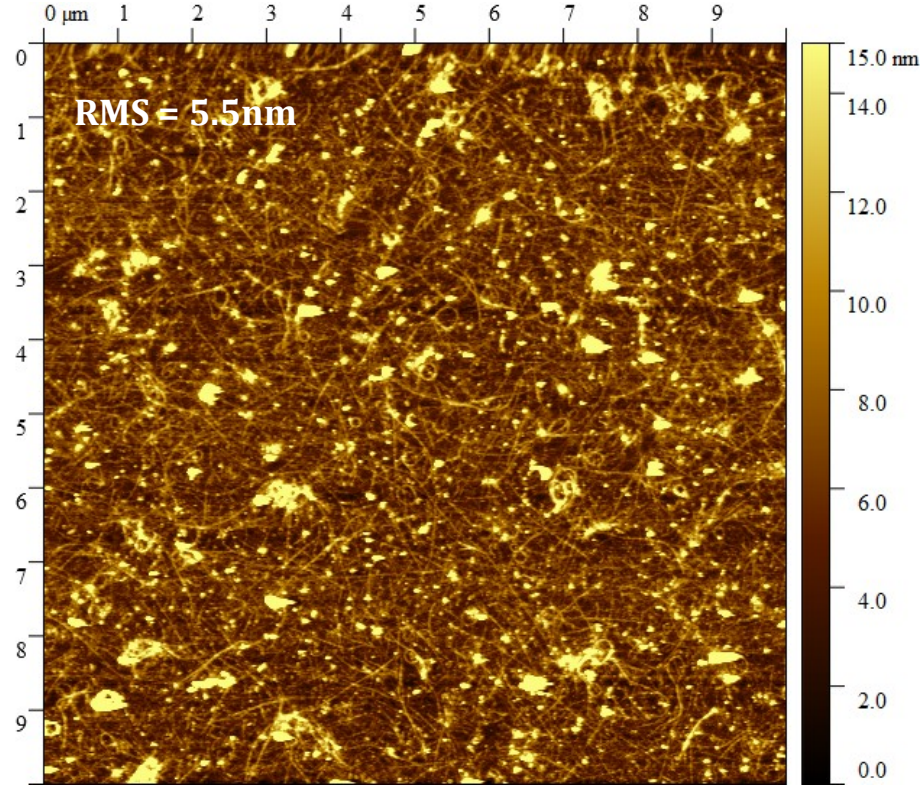


Figure 78: Tapping-mode AFM topography image of the P3HT/SWNT blend spin-coated on a SiO₂ substrate. SWNTs are perfectly visible in the polymer matrix and cover well the entire surface, with a RMS of 5.5nm.

Figure 79 shows the transfer characteristics of the polymer/SWNT blend TFTs.

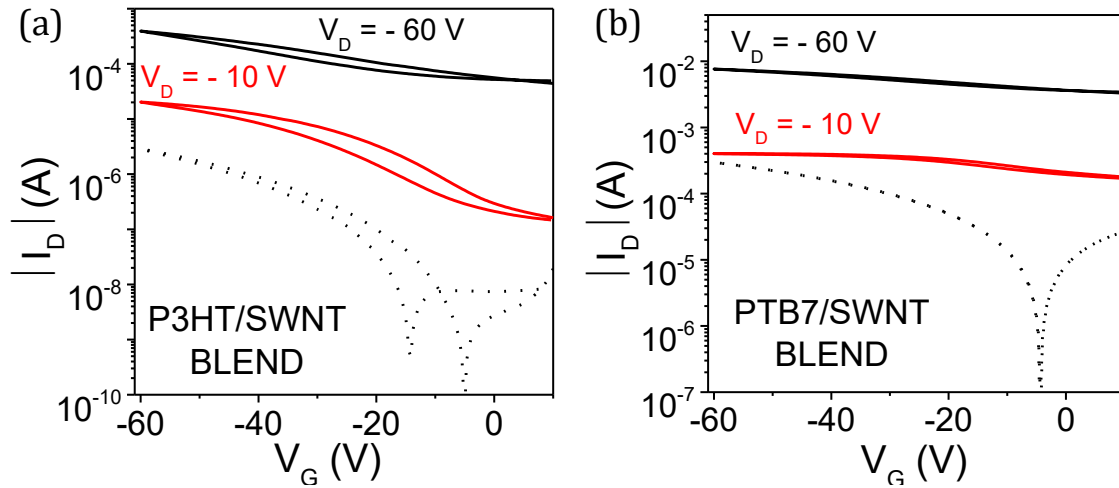


Figure 79: Transfer characteristics of (a) P3HT/SWNT blend and (b) PTB7/SWNT blend TFTs. Both devices, but mainly (b), show a small current ON/OFF ratio and a high OFF current due to the presence of many metallic nanotubes in the blends. TFT in (a) corresponds to device #5 in Table 2, while TFT in (b) corresponds to device #6 in Table 2.

Both devices show a very weak field-effect, with the drain current almost independent from the gate voltage and a high OFF current due to the presence of many metallic nanotubes in the blend. On the other hand, the ON current is strongly increased, together with charge carrier mobility, meaning that charge injection from the Au electrode to the channel is now a faster process thanks to the presence of SWNTs.

The last experiment consists in adding a top polymer layer to the polymer/SWNT blend TFTs, in order to combine the advantage of having a highly conductive channel, but with no metallic nanotubes near the injection area. Figure 80 shows the AFM topography image of a bilayer structure made of a bottom layer with the P3HT/SWNT blend, and a top layer with P3HT. In this case, ODCB has been used for both layers, making it more difficult to optimize the deposition process due to the lack of solvent orthogonality.

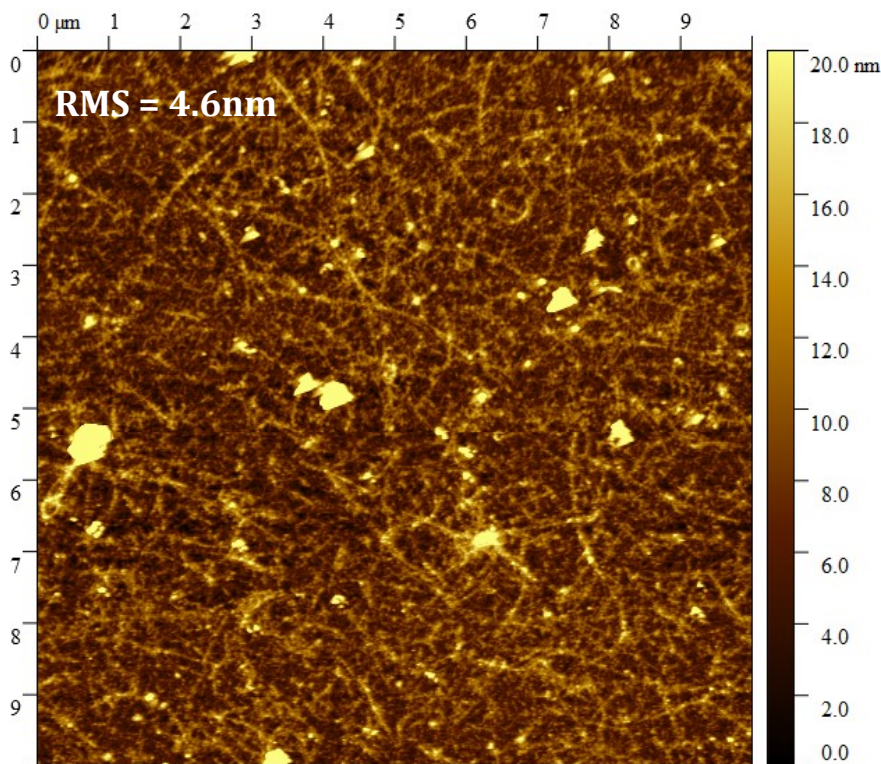


Figure 80: Tapping-mode AFM topography image of the P3HT/SWNT blend + P3HT, sequentially spin-coated on a SiO₂ substrate. SWNTs are perfectly visible in the polymer matrix and cover well the entire surface. Surface planarization, proved by the reduced RMS (4.6nm instead of 5.5nm), is indicative of the presence of the top P3HT layer.

SWNTs are perfectly visible in the polymer matrix and cover well the entire surface. Surface planarization, proved by the reduced RMS, which goes from 5.5 nm of the blend to 4.6 nm of the blend + P3HT, is indicative of the presence of the top P3HT layer even though the same solvent is used for both layers. Figure 81 shows the transfer characteristics of (a) P3HT/SWNT blend + P3HT bilayer TFT, and (b) PTB7/SWNT blend + PTB7 bilayer TFT.

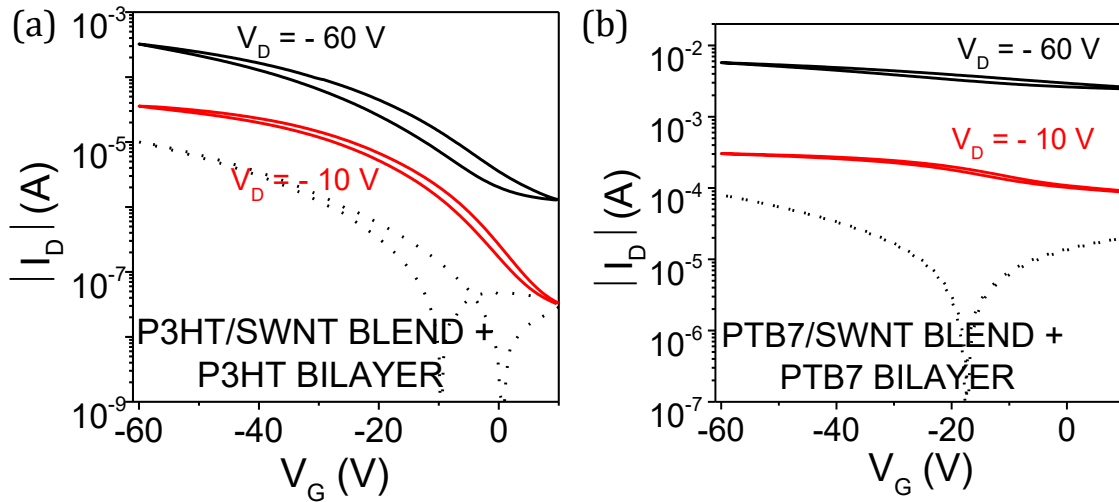


Figure 81: Transfer characteristics of (a) P3HT/SWNT blend + P3HT bilayer TFT and (b) PTB7/SWNT blend + PTB7 bilayer TFT. Device in (a) shows a recovered current ON/OFF ratio and a low OFF current, while device in (b) does not show major improvements, due to the very thin layer of PTB7 deposited on top of the blend, which is not thick enough to prevent direct contact between the Au electrode and the metallic nanotubes in the blend. TFTs in (a) and in (b) corresponds to devices #17 and #18 in Table 2, respectively.

In this case, the P3HT/SWNT blend + P3HT bilayer TFT shows a recovered current ON/OFF ratio and a lower OFF current, thanks to the presence of the P3HT top layer that prevents any direct connection between the metallic nanotubes in the blend and the Au electrode. The same however does not apply for the PTB7/SWNT blend + PTB7 bilayer TFT. According to the AFM topography image shown in Figure 82(b), the PTB7 top layer is very thin and smooth, and probably this is the reason why the electrical connection between the metallic carbon nanotubes and the Au electrode cannot be avoided, and so the OFF current remains high.

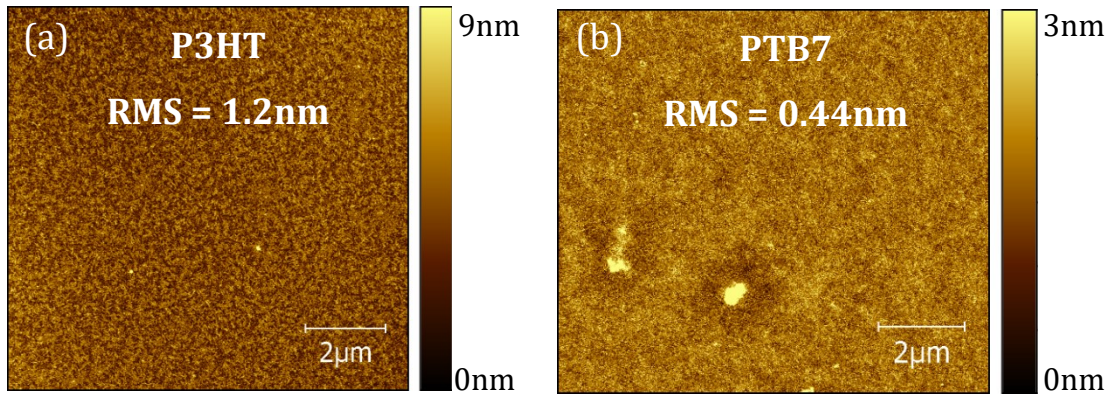


Figure 82: Tapping-mode AFM topography images of (a) P3HT and (b) PTB7 deposited from solution (5mg/ml in ODCB) to SiO₂. PTB7 is thinner and smoother than P3HT, and this may be the reason why the TFT OFF current remains high.

4.4.4 Conclusions

In conclusion, preliminary results on alternative processing methods to disperse and deposit SWNTs have been discussed. In the first part, the vacuum film transfer deposition method has been studied, and results suggest this technique to be very promising for the deposition of SWNT films with a controllable thickness. Moreover, this method enables the deposition of less aggregates and contaminants on the surface, allowing the realization of transistors with better performance than those fabricated through spin-coating deposition, in terms of higher mobility and lower hysteresis.

In the second part, a different set of preliminary results show that electrical performance of TFTs based on conjugated polymers such as P3HT and PTB7 can be enhanced by the addition of pristine SWNTs. However, more work needs to be done to optimize further the structure of the polymer/SWNT TFT, and to improve the quality of the polymer/SWNT blends in order to achieve not only a high mobility, but also a high current ON/OFF ratio.

5 Conclusions and Outlook

The work presented with this thesis focuses on the study of the electronic transport processes occurring in polymer-sorted semiconducting single walled carbon nanotube films and their application to the field of flexible electronics. Here, the conclusions of the four experimental results sections are reviewed, and possible future directions for research in this field are given.

In the first section 4.1, the current percolation behaviour of PFO/(7,5) SWNT networks was analysed, and a novel approach relying on the combination of AFM topography, electrical field-effect transistors and lateral C-AFM measurements was used. AFM topographic analysis of spin-coated SWNT networks and the surface coverage analysis of cylindrical nanoparticles method, described in section 3.3.2.1, were used to fully characterize the surface morphology in terms of nanotube length, surface density, and surface coverage. By combining electrical field-effect transistor measurements with the 2D homogeneous random-network stick percolation model, the surface density of residual metallic carbon nanotubes in the network was quantified. The electrical measurements also revealed the presence of three distinct conduction regimes. Regime I was identified as the direct conduction regime and it was observed for devices with $L_c < 2 \mu\text{m}$. Regime II was identified as the percolation conduction regime and it was found to dominate charge transport in transistors with $2 \mu\text{m} < L_c < 5 \mu\text{m}$. Finally, regime III was attributed to the transport of thermally-excited carriers and it was observed only in transistors with $L_c > 5 \mu\text{m}$. Then, the current percolation pathways in the SWNT network were mapped with nanoscale spatial accuracy by using lateral C-AFM. These measurements allowed calculation of the resistivity distributions in the PFO/(7,5) SWNT networks as a function of (x,y) position, by which their isotropic distribution on the surface could be validated. Most importantly, the proposed approach can be used to quantify the metallic content and the degree of alignment of any semiconducting material disposed in a 2D random network.

In the second section 4.2, PFO-BPy/(6,5) SWNT low-voltage FETs were fabricated first on rigid SiN_x substrates, and then onto free-standing flexible polyimide foils and

characterized under variable tensile strains in order to assess the mechanical bendability of SWNTs. Devices remained fully operational down to 4mm tensile radius and a charge carrier mobility of $8.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ was achieved with a low-voltage operation, which was made possible by the deposition of 50 nm Al_2O_3 gate dielectric.

In section 4.3, polymer-sorted semiconducting SWNTs were successfully employed for low-voltage unipolar and complementary flexible logic circuits. SWNTs were integrated with n-type semiconducting metal oxides on rigid as well as free-standing flexible polyimide foils, and high-performing hybrid CMOS inverters were realized using p- and n-type TFTs. Bendable devices based on spin-coated PFO/(7,5) SWNTs and sputtered IGZO exhibited a gain of 87.1 V/V and a perfect output swing with a low-voltage operation ($V_{\text{DD}} = 10 \text{ V}$), even while bent to a tensile radius of 1 cm. Furthermore, PFO/(7,5) SWNTs were also integrated with spray-coated InO_x in order to realize flexible inverters based on fully solution-deposited semiconductors, thus paving the way towards large-area solution-processed flexible low-voltage electronics.

Finally, in the fourth section 4.4, preliminary results on alternative processing methods to disperse and deposit SWNTs were presented. In the first half of this section, the vacuum film transfer deposition method was studied, and it proved to be a very promising technique for the deposition of SWNT films with a controllable thickness. Moreover, it was demonstrated that this method enables the deposition of less aggregates and contaminants on the surface, allowing the fabrication of SWNT transistors with higher mobility and lower hysteresis than those fabricated through spin-coating deposition. In the second half, it was showed that electrical performance of TFTs based on conjugated polymers such as P3HT and PTB7 can be enhanced by the addition of pristine SWNTs. Even though results are very promising, the polymer/SWNT TFTs need further design optimization and the quality of the polymer/SWNT blends has still to be improved in order to achieve not only a high mobility, but also a high current ON/OFF ratio.

The results presented in this thesis are mainly intended to improve the understanding and performance of semiconducting SWNTs-based electronic devices and to demonstrate the full potential of solution-processed semiconducting SWNTs sorted by means of fluorinated polymer wrapping. Possible improvements

and future works include the optimization of the SWNT dispersion quality and the introduction of a more advanced deposition process that enables SWNT alignment from solution. Regarding the SWNT dispersion quality, many groups¹⁴³ are trying to remove and/or exchange the polyfluorene-based polymers with other conjugated polymers with better optical and electronic properties, so that the latter could contribute and be beneficial also to device performance, and not only be used to sort and disperse the SWNTs in the dispersion. The second possible improvement regards SWNT alignment from solution. Because of ballistic transport along the nanotube axis direction, carbon nanotubes aligned between source and drain electrodes would result in top-performing electronic devices, which now can be obtained only with expensive, high-temperature and non-scalable CVD processes, and not through solution. To this regard, some promising results have been recently obtained through floating evaporative self-assembly deposition of polyfluorene-sorted SWNTs, where a mobility of $46 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ was reported.¹⁷

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7 Appendix

7.1 List of Publications

1. L. Petti, **F. Bottacchi**, N. Münzenrieder, H. Faber, G. Cantarella, C. Vogt, L. Büthe, I. Namal, F. Späth, T. Hertel, T. D. Anthopoulos, and G. Tröster, “Integration of Solution-Processed (7,5) SWCNTs with Sputtered and Spray-Coated Metal Oxides for Flexible Complementary Inverters”, in *IEEE International Electron Device Meeting (IEDM)*, pp. 26.4.1 - 26.4.4, (2014).²³
2. **F. Bottacchi**, L. Petti, F. Späth, I. Namal, G. Tröster, T. Hertel, and T. D. Anthopoulos, “Polymer-Sorted (6,5) Single-Walled Carbon Nanotubes for Solution-Processed Low-Voltage Flexible Microelectronics”, *Appl. Phys. Lett.*, vol. **106**, no. 19, p. 193302, (2015).²¹
3. **F. Bottacchi**, “Solution-Based Single Walled Carbon Nanotubes for Hybrid Solar Cells”, *Scholar’s Press*, (2015).
4. L. Petti, N. Münzenrieder, C. Vogt, L. Büthe, G. Cantarella, H. Faber, **F. Bottacchi**, T. D. Anthopoulos, and G. Tröster, “Metal Oxide Semiconductor Thin-Film Transistors for Flexible Electronics”, *Appl. Phys. Rev.*, vol. **3**, p. 021303, (2016).⁵²
5. **F. Bottacchi**, S. Bottacchi, F. Späth, I. Namal, T. Hertel, and T. D. Anthopoulos, “Nanoscale Charge Percolation Analysis in Polymer-Sorted (7,5) Single Walled Carbon Nanotube Networks”, *Small*, vol. **12**, no. 31, p. 4211-4221, (2016).⁴⁵
6. **F. Bottacchi**, S. Bottacchi, and T. D. Anthopoulos, “A Novel Method for Surface Coverage Spectroscopy with Atomic Force Microscope: Theory, Modeling and Experimental Results for Cylindrical Nanostructures”, *Rev. Sci. Instrum.*, submitted (2016).¹¹⁵
7. D. G. Figueroa del Valle, M. El Gemayel, **F. Bottacchi**, R. Veeravarapu, I. Namal, T. Hertel, J. Morgado, T. D. Anthopoulos, A. Distler, S. B. Meier, G. Lanzani, and F.

Scotognella, “Exploring the Incorporation of (6,5) SWCNTs in Bulk Heterojunction Solar Cells”, *Sol. Energ. Mat. Sol. Cells*, to be submitted (2016).

8. I. Namal, **F. Bottacchi**, F. Schöppler, T.D. Anthopoulos, and T. Hertel, “Optical and Electronic Transport Properties of 18 nm to 750 nm Thick (6,5) SWNT Film Networks”, to be submitted (2016).¹⁴⁹

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Conference Proceedings: 2014 IEEE International Electron Devices Meeting

Author: L. Petti; F. Bottacchi; N. Münzenrieder; H. Faber; G. Cantarella; C. Vogt; L. Büthe; I. Namal; F. Späth; T. Hertel; T. D. Anthopoulos; G. Tröster

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