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LINEAR ISFET ARRAYS AND OPTIMISATION METHODS FOR DNA DETECTION

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Declaration of Originality

I hereby certify that all material presented in this thesis which is not my own work has been properly acknowledged.

London, January 20, 2019

Nicholaos Miscourides

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Nicholaos Miscourides

“ The statements of science are not of what is true and what is not true,
but statements of what is known with different degrees of certainty.”

Richard Feynman – 1955

Abstract

In the early 1970s, at a time when Moore's law was getting up to speed, Piet Bergveld initially described and subsequently pioneered the use of silicon technology in an unconventional way. By combining the field effect present in insulated gate devices and the interfacial double layer formed at the membrane of a glass electrode, he showed that the operation of a MOSFET[1] can be modulated by the ion activity in an aqueous solution. Such a device, aptly called an Ion-Sensitive Field-Effect Transistor, is able to provide chemical inputs to electronic circuits; a concept which has experienced vast developments and a wide range of application to-date. In this context, this thesis largely revolves around the utilization of ISFETs in a practical setting.

This begins by exploring readout methods to facilitate *linear* pH-to-output transduction, achieved by operation in current-mode and biasing the device in the velocity saturation regime. Subsequently, the first ISFET array biased in velocity saturation is shown which leverages on current-mode to demonstrate ion imaging in a scalable, simple and area-efficient topology. This implementation, benefits from short-channel effects in a 0.35 μm CMOS process, to demonstrate a large linear range of operation that increases the robustness against offsets across the array. In addition, to further reduce mismatch across pixels, a programmable gate has been implemented in-pixel in a scalable way. The capacitor facilitating this operation is obtained as the parasitic capacitance across two interleaved metal structures located inside the pixel stack and can be used to fine tune mismatch. This approach has been adopted in a second array shown here for ion imaging which employs current-mode operation and demonstrates integrated compensation. Thirdly, a linear voltage-mode array has been designed which is loosely based on the widely-used source follower topology. Apart from being used to compare against the performance of the current-mode implementations, the combination of these designs has facilitated the derivation of algorithms and methods used to obtained standard metrics that can be used for the benchmarking of ISFET arrays.

The second part of this thesis, focuses on techniques to improve the performance at both a sensor and array level. An investigation into the electrolyte-insulator interface revealed that the two major non-idealities, namely trapped charge and drift, are correlated therefore charge modulation techniques were shown to reduce drift. Additionally, a calibration algorithm is proposed, based on iterative gradient descent, that reduces mismatch due to trapped charge in one iteration step. Lastly, ISFET arrays are demonstrated for the detection of DNA amplification and the diagnosis of infectious diseases. The protocol and methods for improving the robustness of such as platform for monitoring DNA reactions are shown with significant potential towards Point-of-Care diagnostics.

[1] Metal-Oxide-Semiconductor Field-Effect Transistor

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Abbreviations

AC	Alternating Current
APS	Active Pixel Sensor
ADC	Analogue-to-Digital Converter
CDS	Correlated Double Sampling
CM	Current-Mode
CM-PG	Current-Mode with a Programmable Gate
CMOS	Complementary Metal-Oxide-Semiconductor
DAQ	Data Acquisition Unit
DAC	Digital-to-Analogue Converter
DC	Direct Current
DNA	Deoxyribonucleic Acid
FoM	Figure-of-Merit
FPN	Fixed Pattern Noise
FSM	Finite State Machine
GD	Gradient Descent
H^+	Hydrogen ion (proton)
ISFET	Ion-Sensitive Field-Effect Transistor
L	Length (of transistor's gate)
LAMP	Loop Mediated Isothermal Amplification
LoC	Lab-on-Chip
LPCVD	Low Pressure Chemical Vapor Deposition
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
Op-amp	Operational Amplifier
PCB	Printed Circuit Board
PCR	Polymerase Chain Reaction
PECVD	Plasma-Enhanced Chemical Vapor Deposition
PGA	Programmable Gain Amplifier
PG-ISFET	Programmable-Gate ISFET
pH	measure of a solution's acidity or alkalinity, pH=-$\log_{10}[H^+]$. Its definition is disputed and attributed to either mean "power", *pondus hydrogenii*=quantity of hydrogen in Latin, or a simple math designation ("p" and "q") to designate the test and reference solutions used by the concept proposer S. P. L. Sørensen.
PoC	Point-of-Care

PTAT	Proportional To Absolute Temperature
qLAMP	Quantitative LAMP
qPCR	Quantitative PCR
RNA	Ribonucleic acid
SNP	Single Nucleotide Polymorphism
SNR	Signal-to-Noise Ratio
SoC	System-on-Chip
SPI	Serial Peripheral Interface
2(3)T	2(3) Transistor (pixel)
TIA	Transimpedance Amplifier
TTN	TITANICKS chip
TTP	Time-to-Positive
UART	Universal Asynchronous Receiver/Transmitter
UV	Ultraviolet
VHDL	VHSIC Hardware Description Language
VM	Voltage-Mode
VS	Velocity Saturation
W	Width (of transistor's gate)

Preface

The Medici Principle

Our world is continuously growing, evolving and progressing; unquestionably made huge leaps during the course of our own living memory. The push for growth in the last half century has been primarily fueled by advances in technology which have resulted into tangible and ubiquitous impact all around us. This is visible as longer and better lives. It is also evident in more and higher incomes. And it also helps us predict that the world will unequivocally face new challenges in the near future, most prominently related to healthcare, environmental sustainability, education and democratization.

To better prepare for the challenges lying ahead, it would be advised to refer to the past. More often than not, past concepts find new applications and can be the source of much-needed inspiration. Sometimes such sources are not anticipated.

* * *

A visitor to the Italian city of Florence[2], would do well to visit the Uffizi Gallery, the Boboli Gardens or the Basilica of San Lorenzo, all remarkable examples of Renaissance legacy. One might expect Florence, as the city that bred Leonardo da Vinci, Michelangelo and Boticelli (amongst others), to deservedly hold the crown on renaissance art and architecture, as a consequence of the men that dwelt there. One might not expect however, that the presence of talented artists, writers, thinkers and practitioners at that time and place was not down to pure serendipity.

The Medici family was a prominent Florentine family that flourished in the 15th and 16th century initially through the creation of the Medici Bank, eventually Europe's largest bank in the 15th century. Banking and merchandising facilitated the Medici's transition to politics and formed a stage which allowed them to excel in political management[3] as well as enabled them to support their reign through

[2]Host of the IEEE ISCAS 2018 conference.

[3]The Medici supported the introduction of a proportional system of taxation which received strong popular support. They also contributed to accounting as early adopters of the general ledger system of bookkeeping.

social networking. This included a nexus of banking partnerships, marriages of convenience and placing young Medici in the church from an early age[4].

The Medici were businessmen, focused on creating wealth through market domination and were only tangentially interested in art. Interestingly, they are currently considered as the primary driver of the Renaissance. While mostly unintentionally, they do take credit for realizing that bringing together talented people has the potential for disruptive innovation. Part of their genius was in gathering the right people from various disciplines together under the Medici influence and patronage. Famous protégés include multiartist Michelangelo who briefly lived with Lorenzo Medici and this family, polymath Leonardo da Vinci, famous architect of the Florence Cathedral Fillipo Brunelleschi and the father of astronomy Galileo Galilei. Galileo tutored more than one generations of Medici children and in appreciation to the family he named one of his most prominent discoveries, the four largest moons of Jupiter, after four Medici children[5]. Their financial support was also critical to allow for artists to work on their projects unimpeded. Sculptors, scientists, philosophers, poets and others were able to intermingle, learn from one another and tear down the barriers of their disciplines to unleash one of the most innovative eras in history.

* * *

This brief retrospective journey was necessary to fully understand *The Medici Effect*, a term coined by a contemporary American writer to describe "**innovation that happens when disciplines and ideas intersect**" [6]. A term as applicable as ever to modern science and society, it is used to describe the potential held when effective interactions, e.g. between the life and physical sciences, are explored. Evidently, embracing diversity and breaking down traditional barriers separating disciplines and cultures has facilitated the transition from the Dark Ages to the Renaissance. In a modern world turning away from globalization to international isolation and unilateralism, it is easy to ignore the greatest drivers for innovation that are most urgently needed to meet the challenges for healthcare, the environment and society lying ahead.

[4]Three Popes of the Catholic Church in the 16th and early 17th centuries were Medici as well as two queens regent of France.

[5]Galileo's intention was to name the four largest Jupiter moons as the *Medicean stars* in honor of Cosimo II de' Medici and his three brothers. Later they were collectively renamed by astronomers to *Galilean satellites* and were given the names of four lovers of the god Zeus (Greek equivalent of Jupiter) at the suggestion of another famous astronomer Johannes Kepler.

[6]F. Johansson. *The Medici effect: Breakthrough insights at the intersection of ideas, concepts, and cultures.* Boston, Mass: Harvard Business School Press, 2004.

To Demetris & Chrystalla, Xenia & Maria

Chapter 1

Introduction

1.1 Motivation

In the era of exponential technological progress, innovation remains a challenge. Novel solutions are drawing inspiration from a different plane of thinking - moving laterally across disciplines, or from biology - as the most efficient system in existence. Indeed, the most interesting breakthroughs occur when two or more distinct technologies come together to move problem solving into a new dimension. We see the use of nanotechnology and material science targeting therapeutic drug delivery, software applications based on genetic algorithms, biomimicry towards network design and a combination of hardware, software and therapeutics being applied to meet the challenges of the next generation medical devices.

The focus of this thesis concerns a major breakthrough bringing together the electronic with the chemical worlds. An example of *The Medici Effect*[1], Piet Bergveld invented in the early 1970s a solid state device, called an Ion-Sensitive Field-Effect Transistor, initially intended for neurophysiological measurements [1]. The potential of the device had been recognized by Bergveld as combining both the principles of a MOS transistor and a glass electrode i.e. at the intersection of disciplines and ideas. Almost half a century later, fully-electronic ISFET sensors are used to provide chemical inputs to electronic circuits, constituting a novel paradigm in the semiconductor domain that enables the symbiosis of electronics with biology.

Motivation for this thesis is two-fold. On one hand we see the introduction of the ISFET, an electronic component which elegantly brings together the electronic with the chemical worlds. Owing to its

[1] A term that describes "*innovation that happens when disciplines and ideas intersect*", at the suggestion of American author Frans Johansson.

compatibility with modern electronic processes, ISFET-based sensing has the potential for miniaturized, mass-fabricated and low-cost solutions due to the economies of scale of silicon. Furthermore, implementing both the sensing and readout component in CMOS allows for introducing economies of scope[2] with a focus on producing foundry-ready chemical sensing in CMOS. As a result, there is strong motivation to make full use of the sensing capabilities of ISFETs to provide integrated chemical sensing in electronic circuits with immense potential in biomedical applications.

On the other hand, CMOS compatibility exposes two main non-idealities of this approach, specifically threshold voltage instability and mismatch due to inherent limitations of the sensing layer and the ISFET's structure. Subsequent clean-room processing can be employed to reduce the impact of these non-idealities however there is strong motivation to minimize any processing steps post-fabrication to reduce the time and cost associated with sensing-ready solutions. Consequently, it would be beneficial to examine in more detail the fundamental processes driving these non-idealities in order to increase our understanding of the inherent limitations to produce compensation mechanisms and expand the range of applications.

1.2 Research Objectives

This research focuses on the application of ISFET sensors for CMOS-based chemical sensing and large-scale ion imaging. By exploring novel readout methodologies, in the form of current-mode readout that ensures a linear input - output (chemical - electronic) transduction, scalable readout architectures are possible that hold the potential for large-scale sensing. Furthermore, this work explores methods and techniques to counteract and eliminate limitations to the full utilization of the device. Finally, ISFET-based chemical sensing is demonstrated for the real-time DNA amplification detection of various targets in the domain of infectious diseases.

The vision of this thesis is summarized in Fig. 1.1 with the main research objectives that are examined covering the following:

- Introducing the design considerations behind current-mode chemical sensing and developing a current-mode ISFET front-end. Leveraging on the benefits of current-mode with biasing in the velocity saturation region of operation to facilitate scalable pixel architectures that open-up the possibility of high-resolution ISFET arrays.

[2]Economies of scope are economic factors that make the simultaneous manufacturing of different products more cost-effective than manufacturing them on their own.

- Demonstration of linear input-output sensing methodologies. The main objective here is to compare linear current-mode against linear voltage-mode topologies to highlight the benefits / limitations of each and identify areas which merit their respective application.
- Development of a chemical sensing platform to facilitate the aforementioned comparison and provide a processing back-end with chemical sensing front-end for the real-time monitoring of ion activity.
- Investigation into the major ISFET non-idealities by looking into the fundamental interfacial processes and root causes. Consequently, provide practical solutions and workarounds to improve the performance on a sensor as well as array level.
- Validation of ISFET sensing front-end as part of a Lab-on-Chip system for rapid DNA amplification detection. Development of the electrical as well as microfluidic configurations to produce the platform and demonstrate results in real-time DNA amplification and detection with a view for DNA quantification.

Evidently the work presented here includes elements of circuit design (through the design of sensor and array configurations) as well as shallower dives into material science (to investigate the electrolyte-insulator interface) and algorithms (to derive a calibration algorithm) and concludes through the demonstration of the chemical sensing platform in medical applications. By illustrating how the combination of these disciplines is used to improve molecular diagnostics (especially useful in developing countries), the reader is invited to see that when disciplines converge, tangible impact is produced. In some ways, the structure of this thesis resembles an ISFET on its own; it introduces an electrical substrate using devices and circuits, is surrounded by a physicochemical interface that is the origin of both the benefits and limitations, and concludes with a useful chemical sensing application.

1.3 Thesis Structure

Ch 2: CMOS-based Chemical Sensing Systems

This chapter illustrates CMOS and ISFET-based chemical sensing systems which have effectively received research focus in the last 15 years. Firstly, the Ion-Sensitive Field-Effect Transistor is shown which constitutes the common denominator across all aspects of this work. Fundamentals of operation as well as major limitations are examined and quantified whenever possible. Secondly, prior work employing ISFETs for chemical sensing is outlined with an emphasis on ISFET arrays. Only implementations designed in CMOS technology are considered.

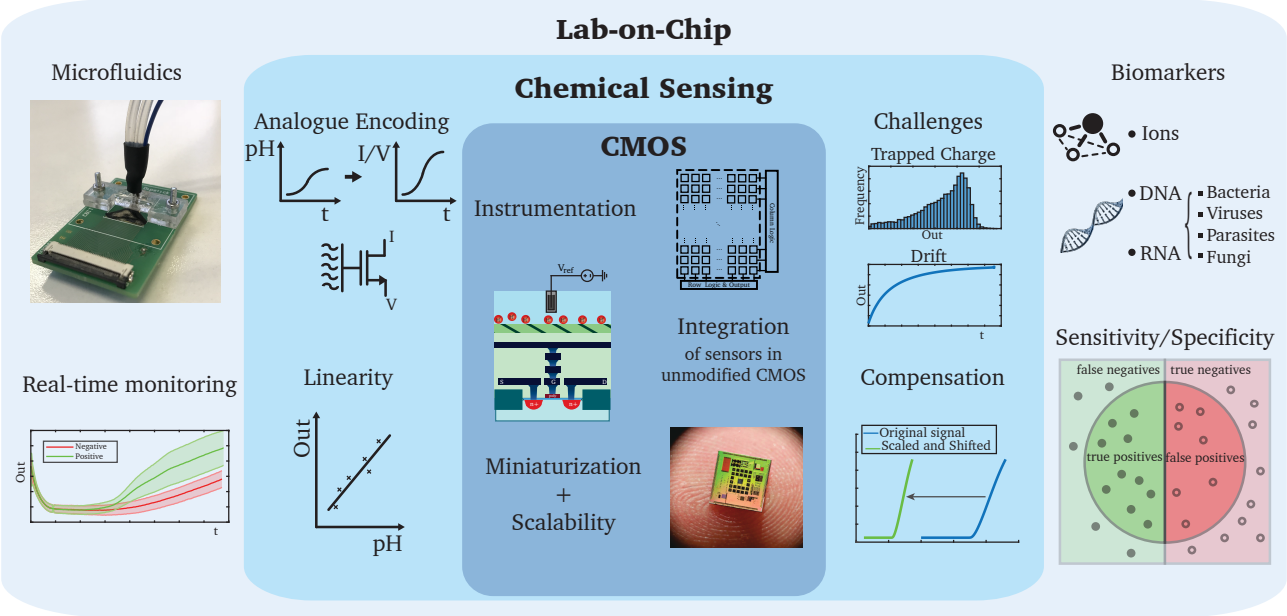


Figure 1.1: Overview of the vision described in this thesis. CMOS-compatible sensors have the capability to integrate chemical sensing with electronic instrumentation. Here, linear front-end sensing is adopted and employed to transduce ion concentrations to electronic signals. The final aim is the design of a Lab-on-Chip platform capable of addressing current needs in healthcare and diagnostics.

1.3.1 Part I - Linear ISFET Arrays in CMOS

Part I covers the electronic aspects of ISFETs and circuit design.

Ch 3: Current-Vs-Voltage Mode for Linear ISFET Operation

This chapter introduces current-mode ISFET sensing and explores the design considerations to realize this. Linear pH-to-current conversion is facilitated with the sensor biased in the velocity saturation region of operation and is compared against the almost universally-used source follower configuration. Design considerations of implementation using ISFETs are detailed such capacitative attenuation, linear range and linearity.

Ch 4: ISFET Arrays for Large-Scale Ion Imaging

This chapter presents implementations of three ISFET arrays, the proposed current-mode array operating in velocity saturation, an adaption of the current-mode array with the introduction of a parasitic programmable gate for offset compensation and a voltage-mode array used in a source follower configuration. All arrays have been included as part of the same chip and are used to create a

comparison framework across CM-VM as well provide a sensing substrate for Lab-on-Chip applications. A novel Figure-of-Merit is proposed to accommodate the various metrics employed.

1.3.2 Part II - ISFET Compensation Techniques and Applications

Part II covers ISFET aspects that are not related to circuit design. That includes dealing with non-idealities as well as chemical sensing applications.

Ch 5: Correlation of Non-Ideal Effects in CMOS ISFETs

This chapter outlines empirical results regarding the trapped charge and drift observed in CMOS ISFETs. It is shown that these effects are to a certain extent correlated since they originate from similar mechanisms in the structure of the silicon nitride used for sensing. It is thus hypothesized that modifying one will modify the other. Indeed drift minimization is shown by the modification of trapped charge through UV irradiation.

Ch 6: An ISFET Array Calibration Method Using a Programmable Gate

This chapter shows an algorithm for offset minimization using the current-mode array including a programmable gate. Initially, a previously-proposed calibration algorithm based on iterative gradient descent is adapted for this array and expanded to include a dynamic convergence point. Subsequently, by noting that in this case gradient descent is not unsupervised, since the step size during calibration is based on a capacitive ratio, the gradient descent algorithm is reduced to a single iteration with comparable performance.

Ch 7: Applications in Lab-on-Chip Diagnostics

This chapter shows the operation of the chemical sensing platform for the real-time detection of DNA amplification. Using Malaria detection as a case study, methods for carrying-out DNA amplification on-chip are illustrated. Subsequently, by leveraging previously-explored methods in drift modelling, compensation for drift is shown on the pH signal obtained during DNA amplification. Finally, using the drift-free response, a relationship between the initial concentration of genetic copies and time-to-positive is derived (quantification) which can be used to predict the concentration of unknown samples.

References

[1] P. Bergveld. “Development of an Ion-Sensitive Solid-State Device for Neurophysiological Measurements”. In: *IEEE Transactions on Biomedical Engineering* BME-17.1 (Jan. 1970), pp. 70–71.

Chapter 2

CMOS-based Chemical Sensing Systems

2.1 Landscape

With the continuous advancements in semiconductor technology, telecommunications and data analysis techniques as well as Moore's law still in effect, we are witnessing new trends in the technological landscape. In contrast with the driving forces in commercial electronic devices of the past decade focusing on a centralised computer hub, the emerging digital ecosystem shows that our everyday activities and utilisation of digital devices is decentralized into various wearable or otherwise portable devices such that each aims to improve a certain aspect of our everyday lives.

These sensors can be integrated into various everyday accessories or clothing such as smartphones, wristwatches, belts or as stand-alone components to allow continuous monitoring with reduced manual intervention. Major enablers of these devices have been the continuous miniaturization of sensors and front-end electronics combined with low-power microcontrollers and wireless data transmission. However, introducing such a degree of monitoring and possibly intrusive or inconvenient wearable devices into our everyday activities would not have reached the current extent if not for secondary drivers such as the rising proportion of ageing population, increased incidences of chronic diseases, increased health (and fitness) awareness and a rise in home and remote patient monitoring [1].

Furthermore, from a commercial perspective, the potential market for useful, autonomous and intelligent sensors is huge, owing both to monitoring applications such as health and wellness monitoring, and to treatment and prediction applications mainly in healthcare and genetics. According to Transparency Market Research the emerging wearables market is expected to reach a market value of $18.9 billion by 2018 [2]. Epigrammatically:

> "The biosensors market is expected to witness considerable growth owing to its wide array of applications in diabetes monitoring, cardiac monitoring, drug discovery, agriculture, environmental and bio-defense practises. Rise in diabetes population coupled with demand for home care diagnostics and point of care diagnostics have boosted the growth of this market. In addition, use of biosensors in non-medical applications is expected to further enhance the growth of this industry."

Additionally, Joseph Wang, professor of nanoengineering at UCSD, California, USA, listed among the 100 most influential people in analytical sciences by Imperial College's UbiMon magazine, reports that

> "Virtually everyone will find some wearable sensor useful, and most of us will want multiple analyses, perhaps on a constant basis: for monitoring sick people, or even babies, for assessing pollution, for measuring physical performance and even detecting pathogens." [3]

For all their recent popularity however, some degree of scepticism still surrounds the extent that wearables are expected to penetrate into our lives especially given the amount of sensitive information that they are bound to collect [4]. In fact, the regulatory framework for dealing with personally identifiable information or health data is still under development and is especially necessary for cloud-based applications. Additionally, aesthetic or convenience reasons have also inhibited the utilisation of wearables.

2.2 Chemical Sensors

With these in mind, the Chapter focuses on a particular subset of biosensors, specifically semiconductor-based chemical sensors. Formally defined as "devices that transform chemical information, [...], into an analytically useful signal" [5], chemical sensors serve as the front-end to numerous applications including pH sensing, glucose sensing, DNA detection etc. In fact, development of these sensors has been fuelled by the desire to expand electronic design such that chemical inputs can be incorporated into otherwise conventional circuits and systems. Given the economies of scale of commercial semiconductor technologies, introducing chemical sensing into solid state circuits holds the key for next generation medical devices.

A major enabling pH sensor which has contributed towards the successful development of fully integrated chemical sensing systems in CMOS is the Ion-Sensitive Field-Effect Transistor (ISFET) [6]. Owing to their compatibility with standard CMOS processes, ISFETs require no post-processing steps

after fabrication which would typically require clean room facilities and expensive equipment. As a result, ISFETs are uniquely suited to address and bridge major limitations in the area of electrochemical instrumentation offering sensor miniaturization, scalability, mass fabrication and low cost. Numerous sensor architectures have appeared in the literature which leverage on the coexistence of sensors and instrumentation on the same IC to facilitate the transition from System to Lab-on-Chip (LoC)[7–10]. Recently, ISFET-based LoC platforms have been used to address the expanding field of rapid diagnostics with applications in infectious diseases [11], cancer [12], SNP identification [13] and multi-ion detection [14].

From a commercial perspective, ISFET sensors are most widely used as the sensing front-end in massively-parallel and large-scale arrays targeting DNA detection and sequencing [15, 16]. Interestingly, the introduction of ISFET technology was accompanied by a paradigm shift in sequencing methods since for the first time the economies of scale of semiconductors were leveraged to drive the cost of DNA detection down, eventually to the $1000 genome milestone [17]. Such sequencing platforms are designed in an imager-like configuration where each pixel aims to identify a fraction of the target sequence. As a result, the sensor density directly affects the throughput of these platforms and the pixel area dictates the overall silicon area and thus cost. Therefore, scalable sensor architectures have apparent benefits in this regard in order to facilitate chemical sensing arrays with similar order of magnitude resolution as optical imagers.

In this context, this Chapter expands on the fundamental mechanisms behind ISFET sensing and operation as well as inherent limitations. Subsequently, a review of ISFET-based chemical sensing platforms is presented detailing the evolutions of ISFET instrumentation and sensing implementations. Finally, given the similarities between chemical and imager array configurations, the last section presents current-mode imager configurations which provided the inspiration behind designing linear ISFET pixels.

2.3 The Ion-Sensitive Field-Effect Transistor

2.3.1 Overview

In the early seventies, Piet Bergveld proposed a solid-state device initially intended for ion measurements in electrochemical and biological environments [18]. His original ideal was to “measure the dynamic ionic activity around nerve and muscle fibres” [19] made possible by the extremely small dimensions of chemical sensors in silicon. The proposed device was based on an underlying MOSFET with a separated

gate connection in the form of a reference electrode inserted in an aqueous solution in contact with the gate oxide [6]. The difference is shown in Fig. 2.1 with the solution in direct contact with the insulating silicon dioxide facilitated by etching away the polysilicon gate. The reference electrode is typically Ag/AgCl which has a stable junction potential.

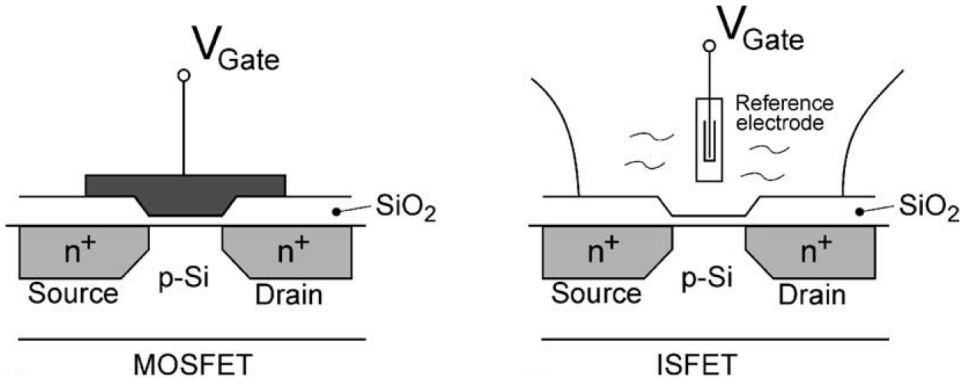


Figure 2.1: Original ISFET as proposed in [6].

Exposing the silicon dioxide to an electrolytic solution creates the dependence of the device characteristics on the pH of the solution due to chemical interactions between the solution and dioxide. This relationship can be interpreted as modification of the gate-source voltage V_{GS} however Bergveld theorized that the reference electrode can be considered as a remote gate, thus suggesting than any interfacial potential should be described in terms of V_{TH} [6]. In practice, FETs are biased with an overdrive voltage of $V_{GS} - V_{TH}$ therefore the net effect is the same. Nevertheless, according to Bergveld's reasoning, the total threshold potential of ISFETs is described by:

$$V_{TH(ISFET)} = V_{chem} + V_{TH(MOSFET)} \tag{2.1}$$

where V_{chem} is the sum of potentials causing the threshold voltage shift.

The threshold voltage V_{TH} of a MOSFET represents the value of V_{GS} that inverts enough carriers to create a channel from the source to drain. It is defined as:

$$V_{TH(MOS)} = \frac{\phi_m - \phi_{si}}{q} + 2\phi_f - \frac{Q_{ox} + Q_{ss} + Q_{depl}}{C_{ox}} \tag{2.2}$$

where $\phi_{m/si}$ is the workfunction of metal / silicon, ϕ_f is the difference in Fermi and intrinsic level of the semiconductor, C_{ox} is the oxide capacitance and $Q_{ox/ss/depl}$ is the charge in the oxide, at the oxide-silicon interface and depletion region respectively.

In the case of a ISFET, the metal workfunction ϕ_m is replaced by the reference electrode potential E_{ref} and the potential due to the existence of dipole molecules in the solution. Overall, the combined

threshold voltage is described by:

$$V_{TH(ISFET)} = E_{ref} - \psi_0 + x_{sol} - \frac{\phi_m}{q} + V_{TH(MOSFET)} \tag{2.3}$$

$$V_{chem} = E_{ref} - \psi_0 + x_{sol} - \frac{\phi_m}{q} \tag{2.4}$$

where ψ_0 is the chemical potential related to pH and V_{chem} is the conventional term of describing this difference.

2.3.2 pH Sensitivity: Site-Binding Theory and Double-Layer Capacitance

The interaction between the electrolyte and insulating layer is explained by the Site binding model expanded in detail by Chan et al in 1976 [20]. When the surface of the insulator is brought into contact with the electrolyte, free ions interact with the insulator and cause an accumulation of charge on that surface. The resulting charge is dependent on the hydrogen ion concentration at their interface since the model predicts binding of the hydrogen ions with the silicon dioxide. Oxides typically contain hydroxyl $[OH]$ groups, as is the case with SiO_2, which act as traps or site binding locations for hydrogen ions. Depending on the pH of the solution, such locations can be neutral, act as proton donors or proton acceptors resulting in $[OH]$, $[O^-]$ or $[OH_2^+]$ sites respectively [21]. As a result, they are described as amphoteric i.e. able to behave both as a base and an acid. For a solution of constant ionic concentration, an equilibrium is reached which is described by the following association-disassociation reactions:

$$SiOH \overset{K_a}{\Longleftrightarrow} SiO^- + H_S^+, \qquad K_\alpha = \frac{[SiO-][H^+]_S}{[SiOH]} \tag{2.5}$$

$$SiO^- + H_S^+ \overset{K_b}{\Longleftrightarrow} SiOH_2^+, \qquad K_\beta = \frac{[SiOH_2^+]}{[SiO-][H^+]_S} \tag{2.6}$$

with $[H^+]_S$ representing the concentration of hydrogen ions at the surface and K_a and K_b the corresponding equilibrium constants. These reactions show the conversion of a binding site from neutral ($SiOH$) to positively ($SiOH_2^+$) or negatively charged (SiO^-). Therefore, the hydrogen ion concentration or charge density at the surface can be described by the difference between the positively and negatively charged site groups and the capability of the surface to act as a buffer, i.e. store charge as a result of small change in concentration. This buffer capacity β_{int} is intrinsic since small changes can be

buffered only close to the surface and not in the bulk of the solution and is given by [22]:

$$\beta_{int} = \frac{d\left([SiO^-] + [SiOH_2^+]\right)}{dpH_S} = N_S \frac{K_b a_{H_S^+}^2 + 4K_a K_b a H_S^+ + K_a K_b^2}{\left(K_a K_b + K_b a H_S^+ + a_{H_S^+}^2\right)^2} 2.3 a_{H_S^+}^2 \tag{2.7}$$

The result of charge building up at the surface is a corresponding potential across the interface, described by the double-layer diffusion model following a Gouy-Chapman-Stern model [23]. The double layer consists of a Helmholtz plane, which describes the distribution of charge attracted to the surface sites of the insulator, and the Gouy-Chapman layer which describes diffusion of charge. The Helpmholz plane results in a linear decrease in charge density while moving away from the interface whereas the Gouy-Chapman follows a Boltzmann distribution which is exponential and eventually evens out. The distribution of charge and resulting potential is shown in Fig. 2.2. Both phenomena can be modelled by the addition of two series capacitances:

$$\frac{1}{C_{diff}} = \frac{1}{C_{Helm}} + \frac{1}{C_{Gouy}} \tag{2.8}$$

with C_{diff} capturing the total capacitance at the double layer. The next step regards deriving a pH-

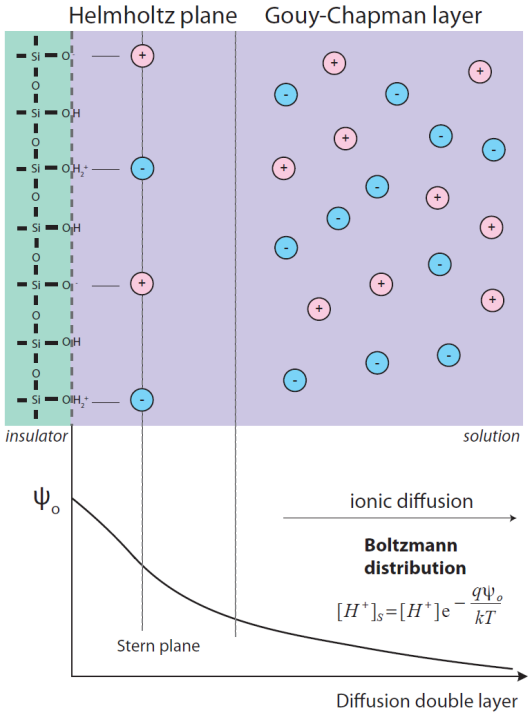


Figure 2.2: Charge and potential distribution at the electrolyte-insulator interface resulting in a Helmholz plane and a Gouy-Chapman layer. Figure from [24].

dependent relationship noting that the concentration of hydrogen ions binding on the surface $[H^+]_S$ originates from the concentration of ions in the bulk of the solution $[H^+]_{bulk}$ and is related through the

Boltzmann distribution.

$$[H^+]_S = [H^+]_{bulk} \exp\left(\frac{-q\psi_0}{kT}\right) \tag{2.9}$$

Therefore the hydrogen ion concentration (pH) of the solution is given by:

$$pH = -\log[H^+] \tag{2.10}$$

$$pH_{sol} = pH_{bulk} + \frac{q\psi_0}{2.3kT} \tag{2.11}$$

According to the Nernst equation, the potential generated due to ion activity on either side of a semi-permeable membrane is given by:

$$E_{mem} = \frac{RT}{z_i F} \ln\left(\frac{a_{i,sol}}{a_{i,bulk}}\right) \tag{2.12}$$

where R is the universal gas constant, T is the temperature, z_i is the charge of the ion i , F is the Faraday constant and $a_{i,x}$ denotes the activities of the ion concentration on the insulator side which is in contact with the solution or bulk. Applying the Nernst equation to the hydrogen ion concentration $[H^+]$ and using the result $\frac{RT}{z_i F} = \frac{kT}{q}$ gives the theoretical maximum (Nernstian) pH sensitivity:

$$S_N = \frac{dE_{mem}}{dpH} = \frac{d\psi_0}{dpH_{bulk}} = -\frac{2.3kT}{q} = -59.2\,mV \;@\; 298\,K \tag{2.13}$$

This value represents the maximum change of the potential at the insulating layer for a unit change in pH. In practice, ISFETs can approach but not exceed the Nernstian sensitivity. The negative sign arises from the definition of the pH scale as the more acidic the solution (more protons), pH reduces yet the gate potential increases. Taking into account this effect, a dimensionless scaling term α is introduced ($0 < \alpha < 1$) to represent the represent the deviation of the actual (S) from the Nernstian sensitivity:

$$S = -\alpha\frac{2.3kT}{q} \tag{2.14}$$

$$\alpha = \frac{S}{S_N} = \frac{1}{\frac{2.3kTC_{diff}}{q^2\beta_{int}} + 1} \tag{2.15}$$

V_{chem} can now be compactly described as in [25], in terms of a pH dependent term and a constant:

$$V_{chem} = \gamma + 2.3\alpha\frac{kT}{q}pH \tag{2.16}$$

where γ groups all the non-pH dependent terms.

2.3.3 ISFETs in CMOS

In order to fully establish ISFETs as the sensing front-end of a biocompatible system, they need to be compatible with CMOS processes in order to fully exploit their economies of scale. Furthermore, it is desirable to avoid or minimize any post processing steps, such as the original method of etching away the polysilicon gate, that would increase cost, time and effort for fabrication. In CMOS, that would correspond to etching away the passivation layer, metal layers and polysilicon in order to reach the silicon dioxide gate insulator.

Fabrication in unmodified CMOS has been reported for the first time by Bausells et al in 1999 [26] who proposed the "extended gate" approach. Their proposal involved the extension of the polysilicon gate to the top passivation material via suitable vias through the metal layers. The two differences compared to the original approach regard the new material used for sensing which now silicon nitride or silicon oxynitride used for passivation (added by Plasma Enhanced Chemical Vapour Deposition) and the introduction of an additional series capacitance due to that insulating passivation layer. Silicon nitride binds to hydrogen ions with similar mechanisms as the dioxide with Bausells reporting a sensitivity of 47 mV/pH. However, the first unmodified CMOS ISFET fabrication revealed some of the non-idealities of the device such as a threshold voltage average of 6.5 V and large threshold voltage variation. In addition, the presence of the passivation capacitance needs to be taken into account, since it effectively reduces the magnitude of the equivalent capacitances in the ISFET macromodel. An ISFET in unmodified CMOS is shown in Fig. 2.3.

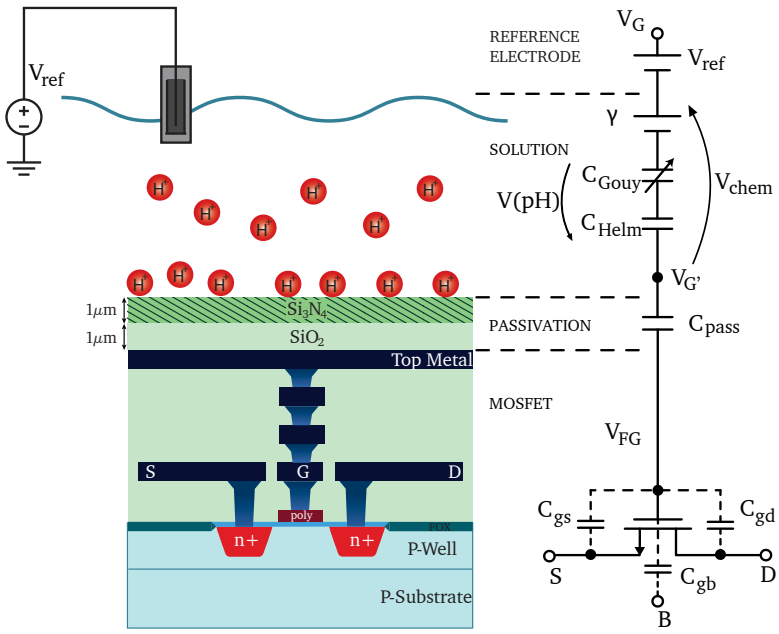


Figure 2.3: An ISFET fabricated in unmodified CMOS technology showing a simplified cross-section of the process and equivalent ISFET macromodel.

2.3.4 Challenges and Non-idealities

In recent years, designing reliable ISFET interfaces in CMOS mainly lies in finding ways to work around the non-idealities of the device which originate primarily due to sensing through the passivation layer. The actual readout method can by essentially any method that allows for recording of the gate voltage or the drain current and various ways have been proposed in the literature, examined later in this Chapter. However, designing in unmodified CMOS introduces a degree of freedom over which designers have no control; sensing through a passivation layer deposited using foundry-specific PECVD processes in high temperatures and can be of poor quality. Overall, sensing through the passivation adds additional challenges since a) a floating metal exists at the gate with no direct path to ground - charge might stay trapped in a floating node, b) an additional equivalent capacitance attenuates the concentration-induced potential and c) the quality of the passivation layer modifies the site-binding mechanism and can cause variations in the potential induced. Furthermore, other CMOS-related effects such as noise and temperature dependence are also present. This section describes further these challenges in the context of ISFET sensing.

Trapped Charge

ISFETs suffer from high and large threshold voltage variations not only among processes but also when devices of the same process are considered [27]. In order to bias the underlying device, trapped charge needs to be counteracted by the input voltage and causes the deviations observed. The proposed explanation for the large inconsistencies of the threshold voltage is that charge remains trapped in the ISFET structure. There are two possible explanations: charge at the floating gate or charge residing in the insulator/passivation. Trapped charge in floating gate transistors left during fabrication is expected as it has been reported in the case of floating gate transistors used in analogue memory [28]. A thorough examination carried out by Prodromakis et al in 2009 [29] showed that the mobile ionic charge induced in the sensing membrane when the membrane is in contact with the ionic-solution, increments the effective capacitance of the membrane and causes deviations in the threshold voltage. This suggests that charge interactions at the electrolyte-insulator interface also affect the total charge trapped in the structure. Overall, the magnitude of trapped charge seems random and has been reported in various ranges spanning $\pm 10\,V$ [30] to $\pm 0.5\,V$ [28]. Previous characterisations of trapped charge is shown in Figs 2.5a and 2.6a. Additionally, the complete ISFET interface in Fig. 2.4 includes the locations where trapped charge may appear and how that differs with potential-induced charge. Q_{TCfg} and Q_{TCfp} denotes trapped charge in the floating gate and passivation respectively.

Hammond, Ali and Cumming [31] were the first to present a method to remove trapped charge by using UV radiation to excite charge out of the ISFET structure and reduce the threshold voltage back to normal levels. By using a differential measurement between an ISFET and a reference FET (called REFET) they were able to achieve pH sensitivity up to $43\,mV/pH$. Migrew and Cumming were also the first to show trapped charge compensation via bulk-substrate biasing and UV radiation on a 2×2 array of ISFETs [32]. Consistent threshold voltages means that a single reference electrode can successfully bias all the ISFETs into conduction. A different approach has been shown by Georgiou in 2009 [33] using hot-electron injection to counteract the trapped charge. By inducing a large source-drain current on a p-type ISFET, high energy electrons can cross the oxide layer onto the gate, subject to a vertical field across the gate oxide present. Applying a V_{DS} of $8\,V$ was shown to cause a change in the V_{TH} of up to $2.8\,V$. Nevertheless, this method requires threshold voltage programming of each ISFET separately and is not practical for large arrays. Furthermore, Georgiou proposed a programmable gate ISFET which uses a capacitively coupled floating gate to allow tunability of its operating point to counteract the large threshold voltage [34]. Summarizing the methods documented, Prodromakis et al [29] proposed that apart from UV exposure and programmable gate ISFETs, high quality sensing membranes and ISFET 'burning time' before utilisation can bring the threshold back to normal levels. Burning time in this case relates to the time that ISFETs are soaked in a solution and counts towards saturating the oxide layer by the presence of mobile ionic charge.

In Chapter 5, trapped charge residing in the passivation layer is examined in more detail and a relationship between trapped charge and drift is derived.

Drift

Drift refers to the slow change of the concentration-induced potential typically sensed at the floating gate of an ISFET. Even in cases of a solution of constant ionic concentration in contact with the insulator, the sensed signal coupled to the floating gate is slowly varying which has been equivalently described as threshold voltage variation [30].

As illustrated in Fig. 2.4, drift relates to the presence of buried sites in the first atomic layers of the insulator in contact with the solution. These buried sites act as ion traps for free hydrogen ions in the electrolyte which diffuse into the insulator and hydrate the surface layer. The growth of this surface layer has been hypothesized to affect the equivalent passivation capacitance through a modification of its dielectric thickness [36]. In amorphous materials, such as silicon dioxide, the growth of the surface layer has been shown to occur due to a mechanism known as "dispersive transport" with an equivalent thickness following a stretched-exponential time response [37]. Consequently, it is reasonable to

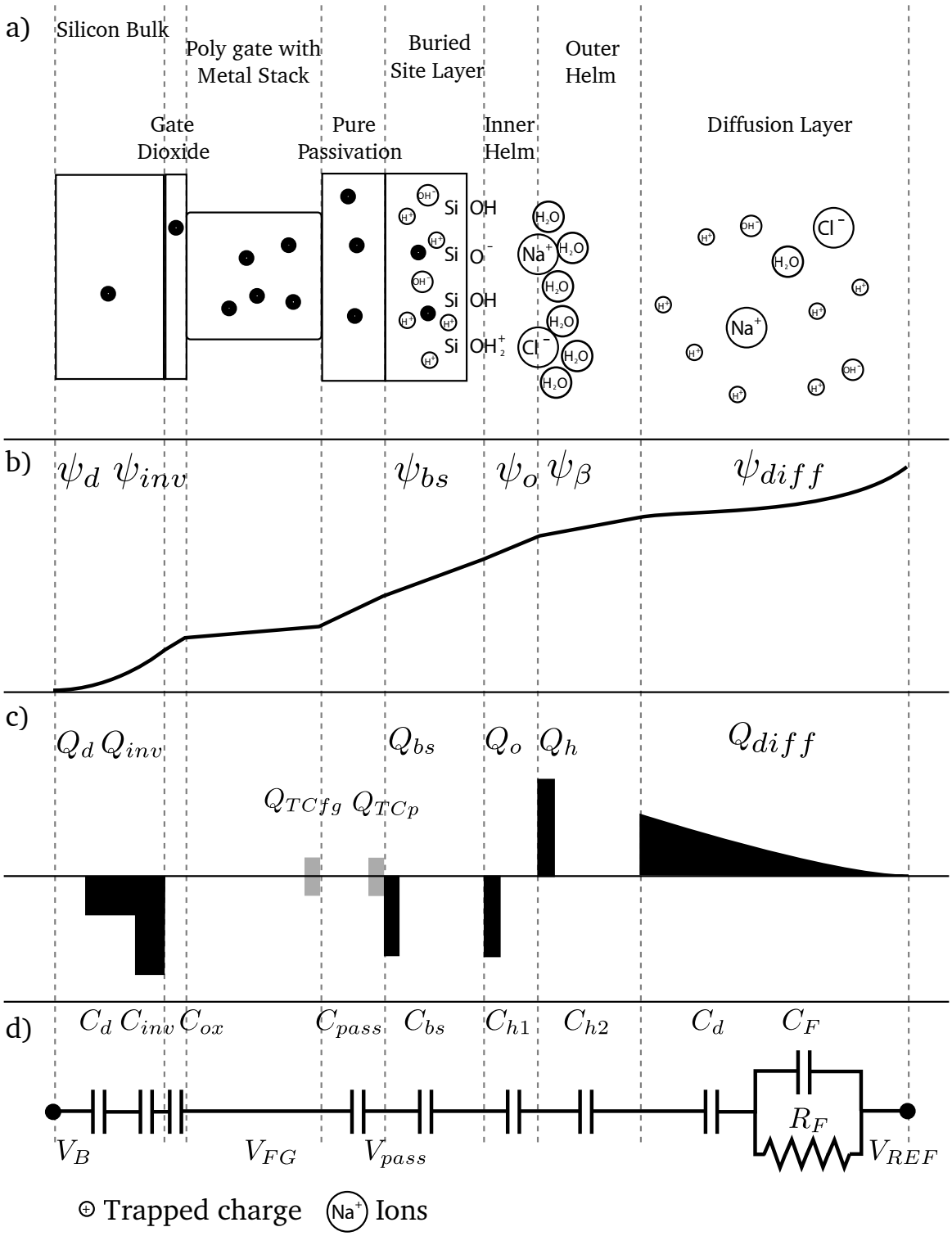


Figure 2.4: Complete ISFET interface including: a) ISFET cross-section showing the locations of ions and bonds at the surface, b) Potential distribution, c) Charge distribution with solid area indicating potential-induced charge and grey area indicating trapped charge and d) Simplified equivalent capacitance model. Figure redrawn from [35].

assume that the surface of other glass-like materials such as silicon nitride will behave in a similar manner. In [36], the same model has been adopted for Si_3N_4 ISFETs which showed a good agreement of the theory with experimental results with drift hypothesized to occur solely due to a change in the passivation capacitance.

As modelled in [36], the slow change at the floating gate due to hydration of the surface can be described as:

$$\Delta V_G = \frac{\Sigma Q}{\Delta C_I} \tag{2.17}$$

where ΔC_I refers to the change in the capacitance of the insulator. Also, ΣQ includes the total charge in the depletion region, insulator and inversion charge. By considering the total charge per unit area in each region as Q_D, Q_I and Q_{inv}, then drift is modelled as:

$$\Delta V_G = -(Q_D + Q_I + Q_{inv}) \left(\frac{\varepsilon_{ins} - \varepsilon_{sl}}{\varepsilon_{ins}\varepsilon_{sl}} \right) x_{sl}(t) \tag{2.18}$$

where $\varepsilon_{sl,ins}$ represent the dielectric constants of the surface layer and insulator respectively and x_{sl} the thickness of the hydrated surface layer. This relationship illustrates the dependence of the gate voltage to the thickness of the surface layer, which follows a stretched-exponential response given by:

$$x_{sl} = \left\{ 1 - \exp\left[-(t/\tau)^{\beta} \right] \right\} \times x_{sl}(\infty) \tag{2.19}$$

where $x_{sl}(\infty)$ describes the final thickness of the hydrated layer, τ is the time constant and β is the dispersion parameter. The overall response has equivalently been modelled in terms of the threshold voltage as in [38]:

$$\Delta V_T(t) = \Delta V_T(\infty) \left\{ 1 - \exp\left[-(t/\tau)^{\beta} \right] \right\} \tag{2.20}$$

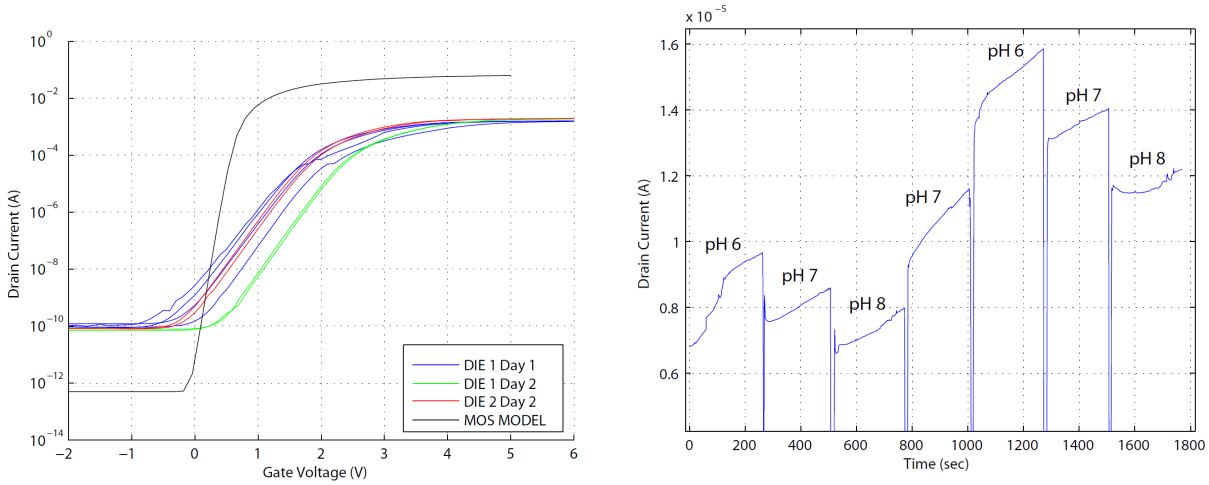
Non-linear parameter fitting on experimentally-obtained drift data can be used to extract values of the fit parameters to give a quantitative indication of drift. Table 2.1 illustrates this.

Table 2.1: Drift coefficients obtained after parameter fit

Ref.	Year	Material	$\Delta V_T(\infty)$ (mV)	τ (hr)	β
[36]	1998	Si_3N_4	79.7	53.4	0.613
[38]	2005	Si_3N_4	963	3.48	0.722

The large deviation in the final drift rate and time constants was hypothesized to originate due to differences in the deposition method of the silicon nitride. Jamasb in [36] used LPCVD (low-pressure chemical vapour deposition) at a high temperature (700-800 ^{o}C) resulting in dense film with few pinholes. Conversely, the passivation layer in unmodified CMOS used in [38] is deposited after the

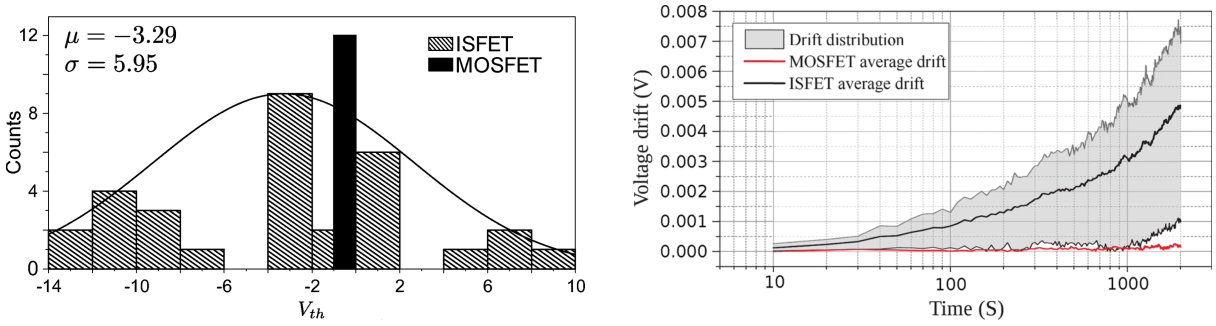
metal layers which requires low temperature (250-350 ^{o}C) plasma-enhanced CVD (PECVD). Passivation films deposited by PECVD have a lower density and contain more pinholes which could explain the higher drift rate as more hydrogen ions diffuse into the nitride at a higher rate. Figs. 2.5b and 2.6b show drift recorded in unmodified CMOS. Furthermore, Chapter 5 examines drift in more detail.



(a) Offset due to trapped charge and capacitive division in weak inversion.

(b) Drift which appears as a slow monotonic change.

Figure 2.5: Non-ideal effects in CMOS ISFETs as presented in [27].



(a) Offset observed due to trapped charge shown as a distribution of V_{th}.

(b) Drift distribution and comparison with MOSFETs.

Figure 2.6: Non-ideal effects in CMOS ISFETs as presented in [30].

Chemical Noise

Not limited to electrical noise ever present in electronics, the chemical interface is believed to cause an additional source of noise which can be referred to the floating gate.

Low frequency noise in ISFETs has been studied by Palan et al [39] and Jacobson et al [40] in 2000 who have identified a flicker noise pattern when the gate leakage current was lower than 1 nA. More recently, the work by Liu et al [30] proposed a two-fold noise model in which ISFET noise is attributed

to contributions of both the underlying MOSFET and chemical noise. Their results confirmed the presence of chemical noise and showed that the combined noise floor makes it very challenging for applications requiring measurement accuracy of $5\,mV/hr$ or lower.

In [30], ISFET flicker-like noise was attributed due to both intrinsic channel flicker noise and chemical noise:

$$\begin{aligned}\overline{V_n^2(ISFET)} &= \overline{V_n^2(MOFET)} + \overline{V_n^2(chem)} \\ &= \frac{K_f}{WLC_{ox}f}\frac{C_{chem}^2}{C_{pass}} + \frac{K_{chem}}{f}\end{aligned} \tag{2.21}$$

where K_{chem} describes the chemical related effect due to long-term electrode degradation and surface chemical noise and K_f is the electrical noise coefficient of the underlying transistor. By measuring the low frequency noise and noise power spectrum, Fig 2.7 shows that measured ISFET noise is 1 order of magnitude higher than measured MOSFET noise which is 1 order of magnitude higher than simulation results. The latter can be attributed to localised temperature drift and instrumentation noise. In any case, the chemical flicker noise dominates at least in the low-frequency region. From empirical measurements in [30], the worst case K_{chem} has been determined as $1\,nV^2Hz$.

Additionally, in [35], K_{chem} was proposed to originate due to long term drift which appears in the low-frequency spectrum of the output signal. By carrying-out the Fourier transform on the stretched-exponential model

$$\overline{S_{(ISFET)}^2} = \left(\frac{C_{pass}}{C_{Tfg}}\right)^2 \frac{K_f}{WLC_{ox}f} + \left|\frac{1}{(1+(-i\omega\tau))^\beta}\right|^2 \tag{2.22}$$

shows that the noise spectrum is related to the drift parameters.

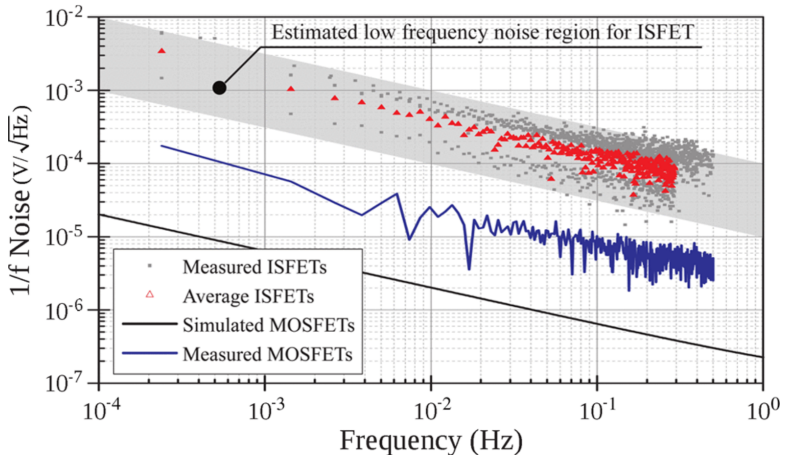


Figure 2.7: Chemical noise and comparison with MOSFET low-frequency noise [30].

Attenuation

Fabrication in unmodified CMOS typically results in an ISFET structure shown in Fig. 2.3 in which a double insulating layer exists between the top metal and solution. Silicon dioxide is used to encapsulate the metal layers (including the top metal) whereas silicon nitride is added at the top for protection. Overall, the passivation capacitance can be estimated using:

$$\frac{1}{C_{pass}} = \frac{1}{C_{SiO_2}} + \frac{1}{C_{Si_3N_4}} \tag{2.23}$$

Substituting $C = \frac{\varepsilon A}{d}$, gives the predicted value for the passivation capacitance, assuming no fringing effects.

$$C_{pass} = (WL)_{chem}\varepsilon_0 \frac{\varepsilon_{Si_3N_4}\varepsilon_{SiO_2}}{\varepsilon_{Si_3N_4}t_{SiO_2} + \varepsilon_{SiO_2}t_{Si_3N_4}} \tag{2.24}$$

where WL_{chem} is the area in contact with the solution, ε is the dielectric constant and t the thickness of each layer.

Typical values of the passivation capacitance will depend on size of the device $(WL)_{chem}$ however they will be comparable with the parasitic capacitances at the gate. On the other hand, the Gouy-Chapman capacitances are several orders of magnitude larger than the passivation therefore the passivation will dominate the response. By using typical values for dielectrics and thicknesses in CMOS the resulting passivation capacitances is shown in Table 2.2 [42]. In comparison, typical values of C_{Gouy} and C_{Helm} are $0.14\,pF/\mu m^2$ [41].

Table 2.2: Passivation Capacitance across CMOS processes.

	0.35 µm	0.18 µm	130 nm	90 nm
ε_{SiO_2}	3.9	3.9	4.1	4.1
$\varepsilon_{Si_3N_4}$	7.9	7.9	7	7
$t_{SiO_2}\,(nm)$	1030	1350	400	500
$t_{Si_3N_4}\,(nm)$	1000	450	400	500
$C_{pass}\,(aF/\mu m^2)$	22.66	21.96	57.23	45.78

Temperature Effects

ISFETs demonstrate a temperature dependence owing both to the underlying electron physics as well as due to chemical effects. The combined effect has been measured in [43] and is shown in Fig. 2.8. Furthermore, is has been reported through simulation that the ISFET undergoes a change equivalent of 1 pH every 7 K around the ambient temperature [44].

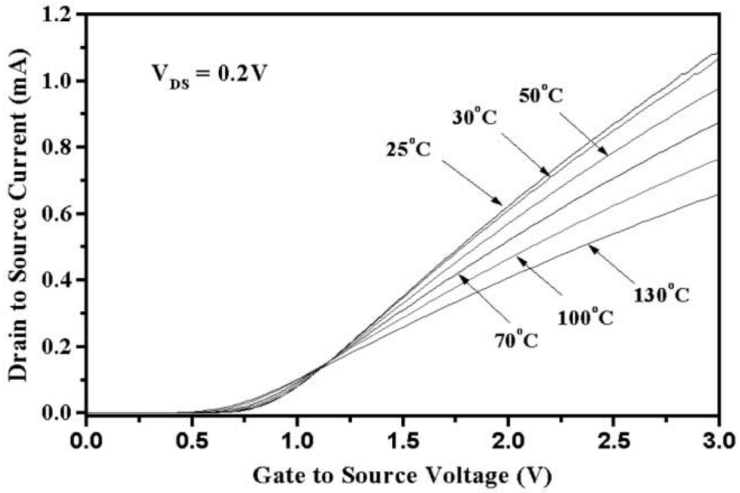


Figure 2.8: Temperature dependence on ISFET's I-V characteristics [43].

Considering the temperature dependence across all variables in the ISFET structure is significantly more complex than that of a MOSFET's. In brief, the temperature contributions to be considered are that of a) the underlying transistor physics modifying the drain current, b) the solution pH which can be modified through modification of the equilibrium of redox reactions, c) the electrolyte-insulator interface in which the site-binding mechanisms depend on the association-disassociation constants (K_a and K_b) and d) the reference electrode whose potential varies proportionally to temperature [45]. As a result, the temperature dependence is not analytically derived here and a constant temperature during operation is assumed. This is the case even in Chapter 7 in which ISFET sensors were used to detect DNA amplification at a constant temperature of 63 ^{o}C.

2.4 ISFET Instrumentation

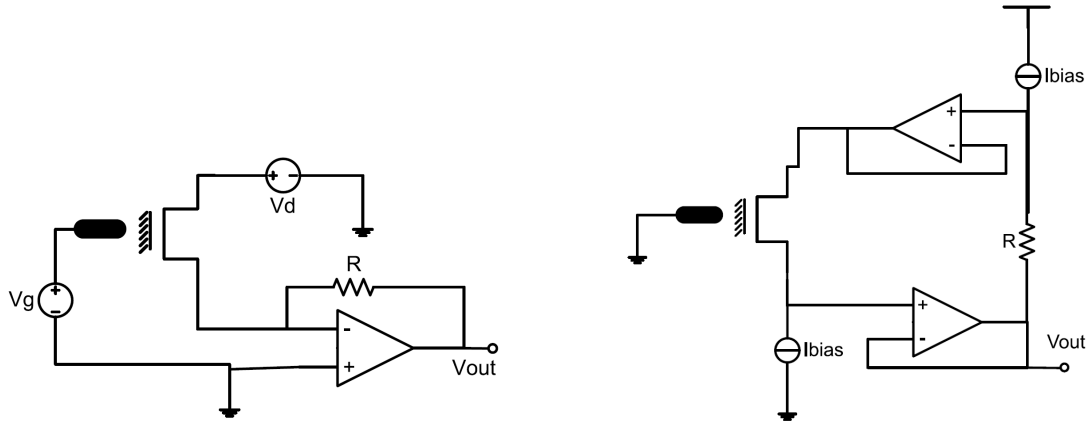
By exposing the ISFET to the solution, the I-V characteristics of the underlying transistor are modified to include the chemical contributions as shown below:

$$\begin{aligned} I_D &= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_G - V_{chem} - V_S - V_{th})^2(1+\lambda V_{DS}) \\ &= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_G + \frac{C_{pass}}{C_T}\psi_0 + \sum\frac{Q_i}{C_T} + k - V_{th})^2(1+\lambda V_{DS}) \end{aligned} \tag{2.25}$$

where $\sum \frac{Q_i}{C_T}$ takes into account the combined effect of trapped charge and k is the chemical contribution. The remaining parameters were previously defined or follow the MOSFET conventional parameters.

In general, two types of instrumentation circuits have been proposed in the literature to sense the

variations in the chemically-induced potential [46]. The first is constant biasing by fixing all ISFET terminal voltages thus measuring the resulting change in the inversion condition of the device through the output current. Alternatively, constant inversion operates by employing a feedback loop to maintain a constant current through tuning of the terminal voltages.



(a) Constant biasing circuit. (b) Constant inversion circuit.

Figure 2.9: Two main types of ISFET interfaces [35].

The constant biasing circuit in Fig. 2.9a fixed the ISFET terminals through V_d and V_g and uses a transimpedance amplifier to convert the sensed drain current to an output voltage through the resistor R. This approach provides a simple interface however it's susceptible to non-linearities in the I-V characteristics of the ISFET. Alternatively, constant inversion in Fig. 2.9b is maintained through a source-drain follower which employs a fixed current through a resistor to fix the V_{DS} and drain current of the ISFET. The source voltage tracks the chemical changes.

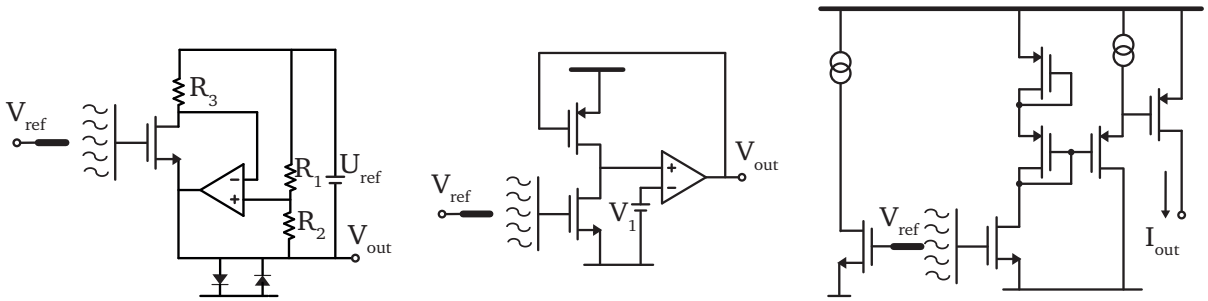
2.4.1 Single-Sensor Readout

At first, circuit design and implementation of ISFET circuits focused on pH determination. In this case, a single sensor is employed to convey that information. Notable implementations are presented here in chronological order with the majority able to be classified as either constant inversion (voltage-mode) or constant biasing (current-mode).

Not surprisingly, the first ISFET-based configuration for pH sensing was proposed by Bergveld [6] and is shown in Fig. 2.10a. Constant V_{DS} and biasing current ISFET conditions ensure that the overdrive V_{GS} voltage will always be constant. This way the variations of the source voltage will reflect any variations of the gate potential with which the solution is in contact. An operational amplifier ensures a constant V_{DS} for the correct operation of this configuration.

Since ISFETs were used as discrete components at the time, they did not suffer from monolithic integration issues such as body effect. Body effect however would affect the operation of the previous configuration since the source and body terminals are at different potentials. For this reason, Morgenshtein et al [47] proposed the Complementary ISFET/MOSFET (CIMP) pair shown in Fig. 2.10b This configuration uses negative feedback to compensate for changes in V_{TH} according to pH while ensuring constant biasing and a zero V_{BS} to eliminate body effect. This group has reported a sensitivity of 58 mV/pH from simulations of their configuration.

More recently in 2005, targeting low-power operation, Shepherd proposed a translinear principle for ISFET biased in weak inversion. In this region, a linear relationship between hydrogen ion concentration and drain current was shown valid over 4 decades. This configuration is shown in Fig. 2.10c and illustrated the similarity between exponential voltage-to-current characteristics in this region and chemical-to-voltage conversion.



(a) Source-drain follower circuit from [6].

(b) Complementary ISFET/MOSFET (CIMP) pair from [47].

(c) Current-mode using the translinear principle from [48].

Figure 2.10: Realizations of single-sensor single-output configuration using either the source voltage or drain current to convey the chemical information.

2.4.2 Multi-Sensor Readout - ISFET Arrays

Expanding from single-input to multi-input or imaging, the development of ISFET arrays characterizes the trend of ISFET instrumentation in the post 2000s. By scaling previously implemented topologies, such as the source-drain follower, and leveraging imager configurations, ISFET arrays have been developed for a variety of applications such as proton imaging, genetic sequencing and multi-ion detection [7].

The case of sensing arrays for multi-input sensing seems straightforward since arrays have been used to primarily facilitate either ion imaging or in-parallel detection of different reactions particularly for DNA sequencing. Yet, the case of employing an array of sensors for detecting a single input has been motivated by the following main reasons:

- **Noise reduction.** ISFET pixels behave as independent sensors (assuming no cross talk between pixels) therefore their noise is uncorrelated. Averaging over independent sensor leads to (mean square) noise reduction by $\frac{1}{\sqrt{N}}$ where N is the number of sensors and hence improves the overall sensitivity.
- **Sensor redundancy.** Especially relevant for ISFETs to ensure a degree of robustness against trapped charge outliers as well as ensuring that available pixels are present under a microfluidic setup which might cover some silicon area.
- **Potential of adaptation.** Regions of the array can target either different ions (by adding membranes of different specificity) or additional reaction chambers for in-parallel sensing (assuming suitable microfluidics setup).
- **Spatiotemporal profile.** To facilitate the extraction of additional information from a spatiotemporal reaction profile (yet different from imaging). E.g. in the case of DNA amplification detection, the output is a single sigmoid change. However, the reaction propagates spatially following a chain reaction hence monitoring the spatio-temporal profile holds potential for real-time tracking of the reaction - not yet been demonstrated.

A brief overview of ISFET sensing applications covering both single and multi-output operation is shown in Fig. 2.11. Furthermore, each array implementation is typically application-specific. This is driven by the various requirements for pH sensing which impose different constraints on the sensor sensitivity, scalability, speed etc. Typical applications and their corresponding constraints are shown below:

- **DNA sequencing** as in [15] benefits from large arrays to facilitate in-parallel detection therefore small and scalable pixels are preferred. However, a lower limit exists due to physical size of the DNA molecules being loaded in each chamber (pixel).
- **DNA amplification** and detection as in [13] is an example application with a single input which typically outputs a binary decision indicating whether amplification has occurred or not. Adding an array has a double potential: averaging to reduce noise and monitoring the spatiotemporal profile to extract novel insights from the reaction.
- **Monitoring ionic diffusion** [49] which requires data readout at least as fast the diffusion rate. In comparison, this is at least an order of magnitude faster that monitoring DNA amplification.
- **Metabolite quantification** as in [50] employs a large-scale array in order to reduce noise through averaging.

Furthermore, the development of ISFET arrays over the last 15 years is summarized in Table 2.3 and is briefly described below in chronological order.

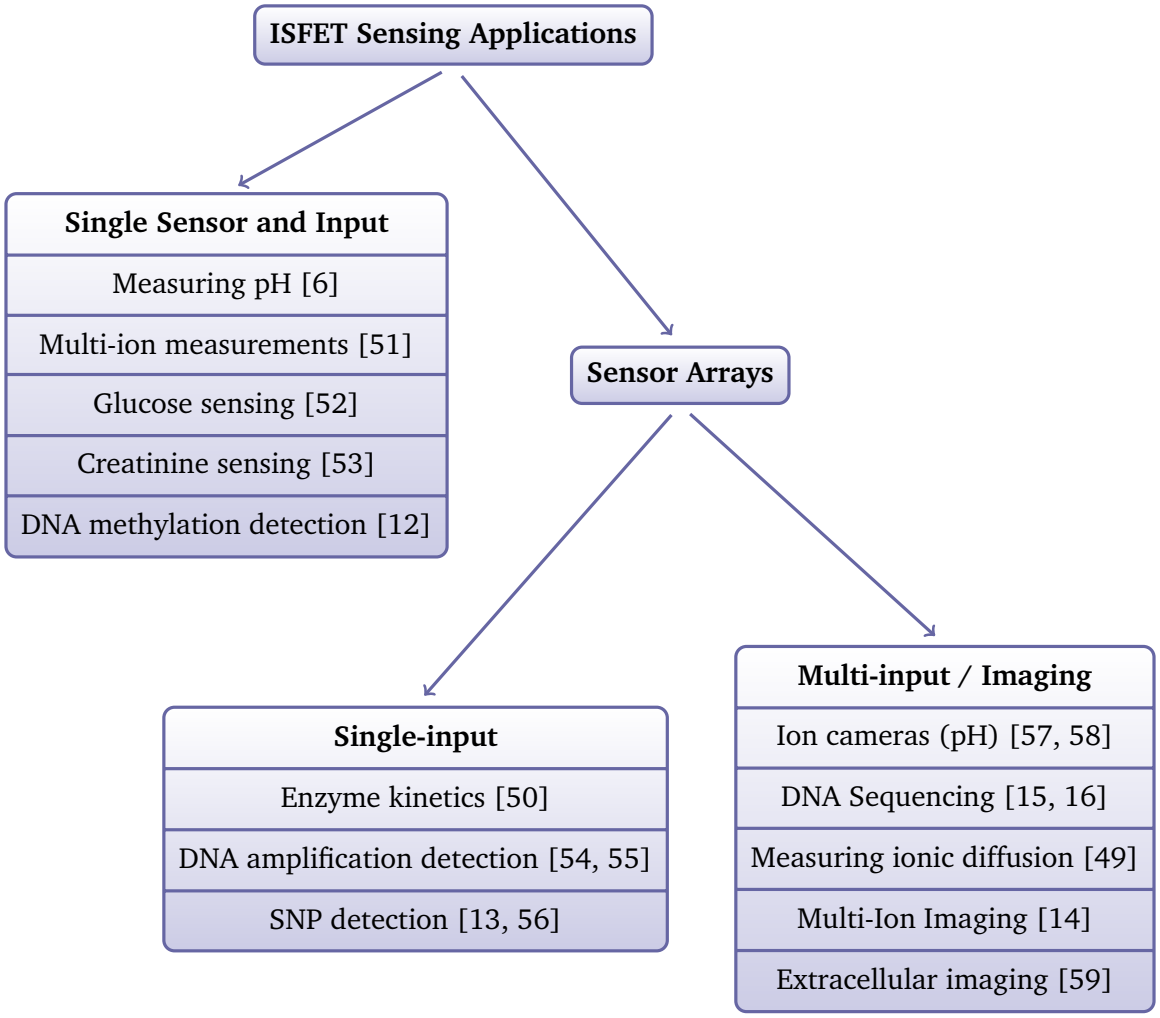
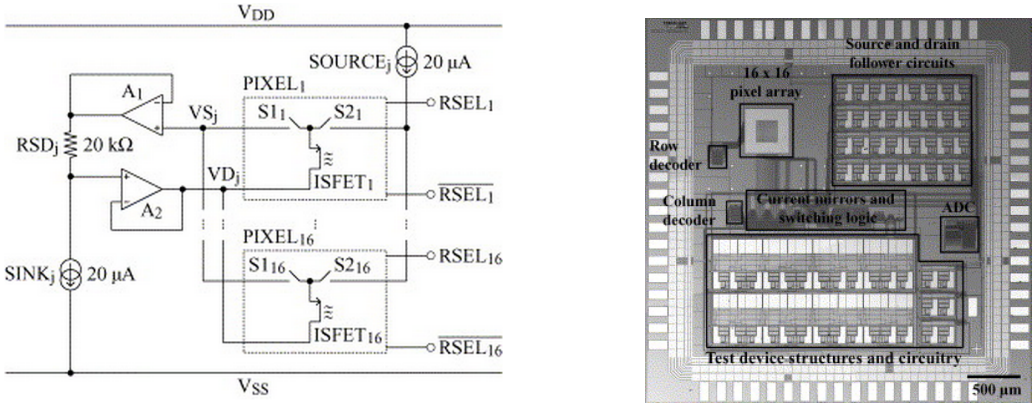


Figure 2.11: Examples of single- against multi-output applications of ISFET sensors. Sensor arrays have been demonstrated in both cases.

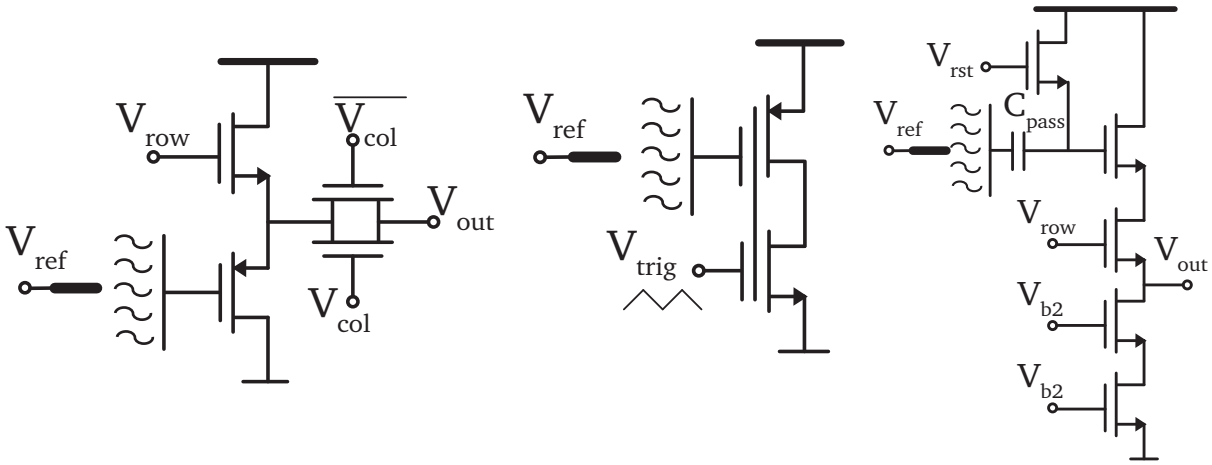
Early stages of ISFET arrays

Relatively small arrays have been fabricated as early as 2001 by Lauwers et al [60] who used the ISFET as an input to a symmetrical OTA, connected in a buffer configuration. The OTA was part of a larger multiparameter microsensor chip which also included temperature control, amperometric and conductometric cells. However, even for a small array (6x1) the resulting area is 25.7 mm^2 which makes this architecture unsustainable for large arrays.



(a) Pixel Schematic (b) Chip Layout

Figure 2.12: ISFET array based on a source-drain follower (2005) [59].



(a) Source-follower pixel(2012) [57]. (b) ISFET inverter (2012) [61]. (c) APS-based pixel configuration (2015) [62].

Figure 2.13: Various configurations of ISFET pixels.

The first approach consisting entirely of ISFET sensors, was demonstrated at the University of Glasgow by Milgrew, Hammond and Cumming in 2004, who configured the ISFET in a source-drain follower [63]. They achieved a sensitivity of 40 mV/pH while noting that the threshold voltage of the fabricated devices was varying in the range of 1-4 V. In addition, they provided some of the first observations illustrating the quality of encapsulation on the lifetime of ISFET chips. When monitoring cell cultures,

the chip was made unusable after a maximum of 7 days due to excessive leakage currents.

The same group demonstrated a 16×16 array [59] in 2005 with a source and drain follower circuit maintaining a constant V_{ds} of 400 mV across the ISFETs showed in Fig. 2.12a. They achieved a sensitivity of 46 mV/pH by etching the chip in a 1:5 buffered hydrofluoric solution for 30 s prior to experiments. They successfully used their array for extracellular imaging for 72 continuous hours at a time. Using the same design, Milgrew and Cumming demonstrated in 2008 a proton camera for imaging of hydrogen ion activity of cells grown *in vitro* [64]. Their main self-criticism point was that significant fixed pattern noise occurred on the 16×16 chemical image due to the digital electronics being positioned too close to the analogue circuitry resulting in coupling between them.

In 2012, the Glasgow group demonstrated a new high-speed sensor, with the same number of pixels (16×16) achieving a frame rate of 333 frames/s [49]. The source-drain follower topology was replaced by a source follower configuration such that by monitoring the source of each ISFET any changes in the threshold voltage due to changes in pH can be determined. The authors noted that the system requires precise biasing in order for the output voltage to stay within its linear range. Each pixel demonstrated a sensitivity of 17 mV/pH and was used to determine diffusivity coefficient values for various analytes. By injecting selected analytes (HCl and NaOH) on the surface of the chip and recording successive frames, the authors were able to determine the rate of diffusion of the analyte which was then compared to the theoretical diffusion rates of those analytes. Finally, the same group, demonstrated a new 64×64 array (pixel shown in Figure 2.13a) with ISFETs in source follower configuration used for proton imaging [57]. The new chip showed a 20 mV/pH sensitivity and operation at 100 frames/s. They also demonstrated a nearly perfect linear response between pH 4-10 tested by injecting citric acid into alcali (NaOH).

A different architecture for an ion-sensitive chemical imager chip was presented in 2008 by Georgiou and Toumazou [65] who encoded the chemical sensor information using address event representation (AER) implemented with integrate and fire neurons. This neuromorphic architecture was aimed to measure fine changes in pH due to cell metabolism and achieved 42 dB of dynamic range which is about 7 bits in resolution.

ISFET arrays with integrated compensation

Other arrays of various sizes and target applications have appeared in the literature which aim to address the challenges when using ISFETs for pH detection. As outlined earlier, when fabricating an ISFET in unmodified CMOS, some charge remains at the floating gate node left over from fabrication

which causes large threshold voltage differences between devices. In order to address this issue, Milgrew and Cumming (2008) used ultraviolet radiation on a 2×2 ISFET array to remove the trapped charge and match the transconductance characteristics of the devices [32]. The ISFET array had a measured sensitivity of 46 mV/pH however, this process required a total of 10 hrs of UV exposure.

Circuit-based techniques for offset compensation were subsequently adopted with Chan et al [66] demonstrating an array of 64 pixels which takes the average of all pixels to reduce the effect of outliers and uses negative feedback to achieve linear output. In the next year, Liu and Toumazou [67] showed how feedback applied directly at the gate of the ISFET through auto-zeroing amplifiers and a ping-pong control scheme compensated for a threshold voltage variation of ±5V and enhanced the pH sensitivity to 100 mV/pH. Furthermore, in 2011, Goh et al [58] demonstrated an auto-calibration algorithm operating an an 8×8 array of sensors using the Programmable-Gate technique for offset compensation. In this case, mismatch was reduced by implementing a gradient-based calibration algorithm to equalize the gate voltages which were applied during array readout and stored in on-chip memory, with the system architecture shown in Fig. 2.14.

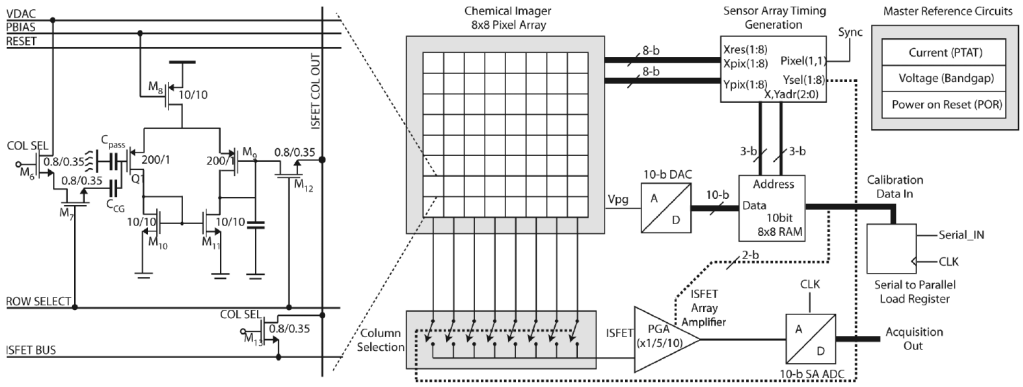
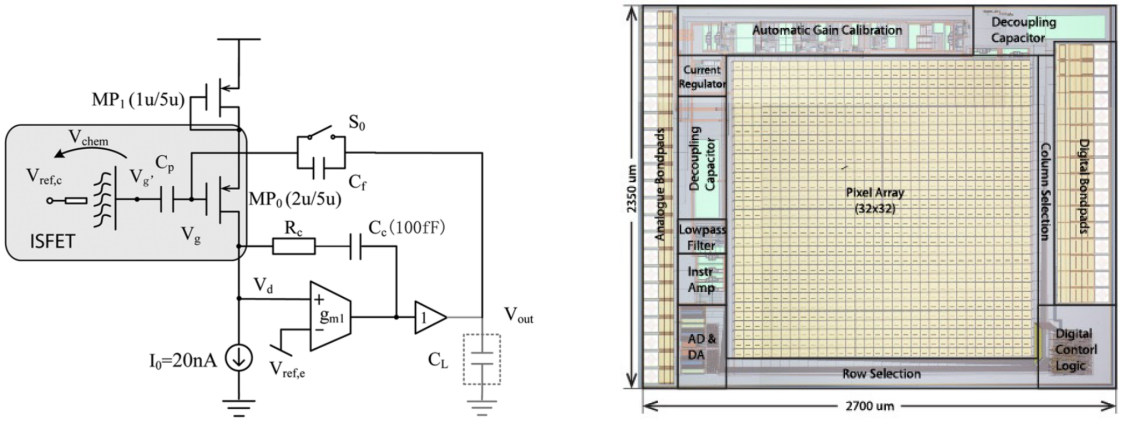


Figure 2.14: Pixel and system architecture in [58] using an in-pixel unity gain buffer and a Programmable gate for offset compensation.

A different approach based on a Time-to-Digital converter and signal encoding in the time-domain was proposed in 2012 by Wang et al [68]. The aim of this approach was to minimise the interference usually introduced in the analogue front end and to simplify the sensor interface. This approach was demonstrated on a 3×3 sensor array, achieved a pH resolution of 0.028 pH and sensitivity of 27 ns/pH. Similarly, Liu proposed a minimal readout scheme for an ISFET pixel (shown in Fig. 2.13b) which quantizes the chemical signal in-pixel using an inverter and a programmable gate. By introducing an additional signal at the shared gate of the inverters in the form of a triangular wave, results in pulse-width modulated signal and eliminates the need for an ADC. Simulated results showed a capability of $\pm$ 1 V offset compensation and a pH sensitivity of 2 % phase change.

In 2015, Moser proposed a pH-to-Time configuration for ISFET pixels, which modulates the pH signal in a pulse-width encoding similar to the APS design in optical pixels. By introducing a compensation scheme for offset based on source-voltage modulation, the proposed configuration achieves a compensation range of up to 1.25 V and a resolution of 20 mpH. Using a similar pixel configuration, Huang et al proposed in 2015 [62], a dual-mode ISFET array with both optical (CMOS image sensor) and chemical (ISFET pH sensor) sensing capabilities in each pixel. The 64×64 dual-mode array is targeting DNA detection and aims to eliminate erroneous step pH detection in empty microwells usually caused by crosstalk from wells containing DNA microbeads. This system correlates the chemical and optical images to verify that the recorded changes in pH come indeed from a well containing a DNA-bearing microbead. The ISFET pixel schematic based on an APS configuration is shown in Fig. 2.13c and uses correlated double sampling for noise reduction. The chemical sensor showed a pH sensitivity of 26.2 mV/pH whereas the whole system operates at a readout speed of 1200 fps.

Lastly, in 2017, Hu et al showed a 32×32 pixel array, shown in Fig. 2.15 which uses capacitive feedback to improve the attenuation due to the passivation capacitance, a low-leakage switch for offset compensation and in-pixel buffering to drive the output bus capacitance. The main limitation despite the triple compensation mechanisms, was the occurrence of large amounts of electrical drift originating due to leakage through the gate-reset switch. That was the case even after implementing a low-leakage switch typically used in analogue storage cells.



(a) Pixel Schematic.

(b) Chip Layout.

Figure 2.15: ISFET array using a gate-reset switch for offset compensation, in-pixel buffering and capacitive feedback for signal enhancement (2017) [9].

ISFET arrays for DNA detection

Comprising the largest commercial application of ISFET arrays, this section describes ISFET array implementations for DNA detection. In general, such implementations are either targeting Single-Nucleotide Polymorphisms (SNPs) and short sequences or large unknown DNA sequences with each having different design requirements.

An array able to detect single nucleotide polymorphisms (SNPs) was initially presented by DNA Electronics and Imperial College in 2011 [13]. The array, designed as a single row of 40 columns, eliminated the requirement for tagging the DNA prior to detection and included all the discrete laboratory apparatus used for SNP detection including ISFET front-end for chemical sensing, temperature sensors, resistive heating, signal processing and control circuitry, all integrated to produce a full system-on-chip. Complete demonstration for SNP detection was subsequently shown in [16] with DNA amplification and detection taking place simultaneously on-chip. The authors pointed out the scalability of such a system and its potential as a point-of-care platform since the detection occurs much faster than traditional laboratory-based tests.

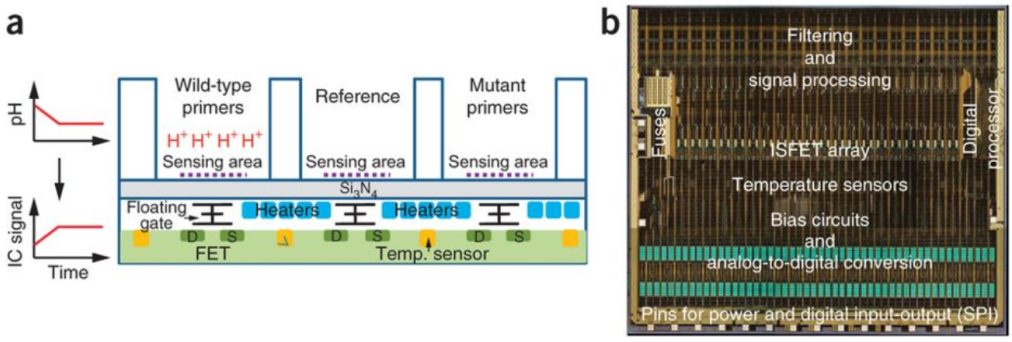
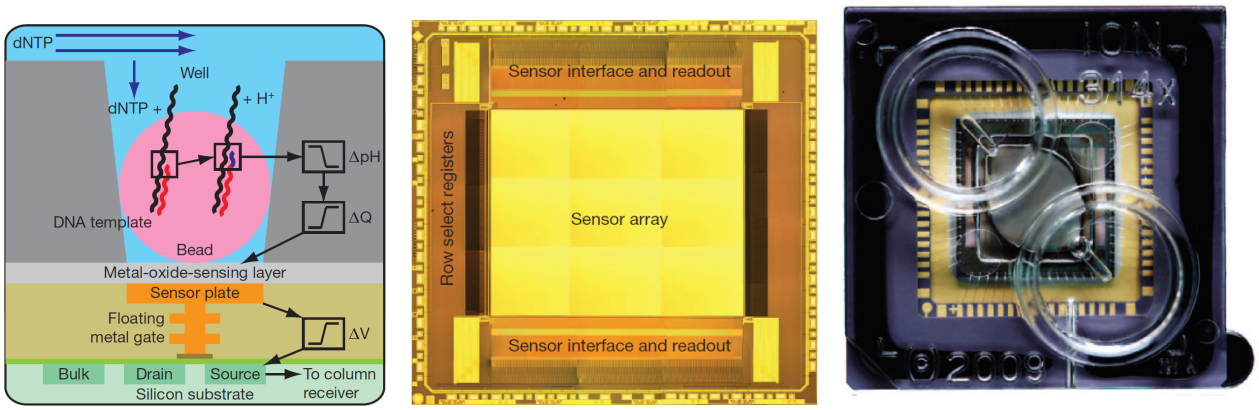


Figure 2.16: (a) illustration of the cross-section of the ISFET array showing ISFETs, temperature sensors and digitally controlled resistive heater elements all embedded under the silicon nitride (Si_3N_4) sensing surface of the chip. Additionally, a polymer fluidic assembly (flow cell) creates separate reaction chambers, each of which may contain a unique primer set. (b) CMOS-fabricated chip [16].

The huge potential of ISFETs was demonstrated in 2011, when Ion Torrent achieved *de novo* genome sequencing on an ISFET array with 1.5 M sensors and 1.2 M wells [15]. This design adopted a simple source-follower pixel comprising an ISFET and a switch with no compensation schemes implemented. Nevertheless, the native CMOS passivation layer was removed and tantalum pentoxide (Ta_2O_5) was deposited to improve performance. The reported proton sensitivity reached the almost-Nernstian 58 mV/pH. Ion Torrent recognised the immense scalability potential of the sensor and envisioned the production of one-billion-sensor chips and low-cost routine human genome sequencing.



(a) Cross section of a sensor and well.

(b) Annotated die post fabrication.

(c) Packaged die and microfluidic arrangement.

Figure 2.17: ISFET array with 1.2 M active sensors for DNA sequencing [15].

2.5 Summary

Evidently, different methods, architectures and implementations have been proposed and implemented in the past regarding chemical sensing systems with an ISFET front-end, usually driven by an application-specific design. A lot of effort has been put into compensating for the ISFET non-idealities (explored further in Chapters 5 and 6) specifically the sensor drift, threshold voltage mismatch and minimise noise contributions however the fundamental question still remains if "one size fits all".

A summary of ISFET array implementations is shown on Table 2.3, yet a direct comparison is challenging since each architecture was built as application-specific. Furthermore, it is evident from the table that as time progresses, larger and larger ISFET arrays are designed which resemble the architectures of CMOS image sensors. In fact, in prior works [15] and [16] which present commercial applications of ISFET pH sensing, the pixel designs are based on source-follower APS almost identical to the 3T APS (3-transistor active pixel sensor) which is the standard pixel configuration in imagers. Furthermore, in [62] the pixel contains both a photodiode and ISFET for photo and chemical imaging with almost identical readouts. Since, the CMOS imaging industry has been active for much longer than ISFET chemical sensing and has already produced large-scale and fast arrays for photonic imaging [69], it is only natural to draw upon their experience to adapt or derive new ISFET architectures.

Table 2.3: CMOS ISFET arrays in a nutshell. In bold are the implementations included in this thesis.

Year	Node (μm)	Array Size	Application	Compensation	Group	Ref.
2001	1.2	6×1	Blood Gas	–	Lueven	[60]
2004	0.35	2×2	Cell Culturing	–	Glasgow	[63]
2005	0.35	16×16	Extracellular Imaging	–	Glasgow	[59]
2006	0.18	5×10	DNA Detection	–	Stanford	[70]
2008	0.35	3×11	Electrolyte Imaging	–	Imperial	[65]
2008	0.35	16×16	Extracellular Imaging	UV irradiation	Glasgow	[64]
2008	0.35	2×2	Electrolyte Imaging	–	Glasgow	[32]
2009	0.18	8×8	Hand-held Instrument	Global averaging	Imperial	[66]
2009	1.2	16×16	DNA detection	–	Nagoya	[71]
2010	0.35	40×1	DNA Detection	Differential (REFETs)	DNAe/IC	[13]
2010	0.35	8×1	Electrolyte Imaging	Offset compensation	Imperial	[67]
2011	0.35	8×8	Opto-Chemical Imaging	Programmable-Gate	Imperial	[58]
2011	0.35	1280×1152	DNA Detection	–	Ion Torrent	[15]
2012	0.18	3×3	DNA Detection	–	Imperial	[68]
2012	0.35	16×16	Electrolyte Imaging	–	Glasgow	[49]
2012	0.35	64×64	Electrolyte Imaging	–	Glasgow	[57]
2013	0.35	40×1	DNA amplification	Differential measurements and dedicated DACs	DNAe/IC	[16]
2015	0.18	64×64	DNA Detection	CDS	Nanyang	[62]
2016	0.35	256×256	Metabolite Quantification	–	Glasgow	[50]
2016	**0.35**	**64×200**	**Electrolyte Imaging**	**Programmable-Gate**	**Imperial**	**[72]**
2017	0.35	32×32	Electrolyte Imaging	Gate-reset switch	Imperial	[9]
2017	0.35	1×9	On-body pH measurement	–	Imperial	[73]
2017	0.35	128×128	DNA Detection	Source modulation	Imperial	[55]
2018	0.35	128×128	Electrolyte Imaging	Gate-reset switch	Imperial	[74]
2018	**0.35**	**64×200**	**DNA Detection**	–	**Imperial**	**[54]**
2018	**0.35**	**3 arrays**	**Electrolyte Imaging**	–	**Imperial**	**[75]**

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Part I

Linear ISFET Arrays in CMOS

Chapter 3

Current-Vs-Voltage Mode for Linear ISFET Operation

3.1 Introduction

Evidently ISFET arrays enable a novel type of biomedical Lab-on-Chip platform, as elaborated in Chapter 2, which is not only capable of combining microfluidic and other lab functions on a single chip but also making use of the chip's surface to *image* ions in contact with the native passivation layer in CMOS. Consequently imager configurations can be adapted to the design of ISFET sensors in large arrays owing to similarities in their design objectives[1] and propelled by the fact that CMOS imager field predates ISFETs by at least two decades. Thus, the widely-used configuration of ISFET pixels, e.g. for large-scale and high-throughput DNA sequencing in [1], follows that of well-established optical pixel designs such as the 3T-APS (3-transistor active pixel sensor). This approach adopts a source follower configuration which ensures linear input-output characteristics i.e. pH-to-V_{out}. Subsequent efforts have focused on further adaptation of optical architectures (e.g. using the backside of the chip for sensing similarly to backside illuminated imagers [2]) or introducing novel albeit non-linear readout configurations primarily to facilitate circuit-based compensation for known ISFET non-idealities such as trapped charge and drift [3].

Linearity across input-output is a crucial design parameter in sensor instrumentation, in this case to facilitate a straightforward representation of the target solution's ion concentration. ISFET applications are concerned primarily with differences in pH rather than absolute values e.g. to detect the pH

[1] In a typical imager configuration such as the 3T APS, the objective is to monitor the photodiode current during light incidence through the difference in photodiode voltage sensed at the gate of the source-follower device, whereas in chemical pixel design the objective is to monitor the pH-induced V_{chem} which similarly appears at the floating gate of the sensor.

change following DNA amplification that is carried-out using double-sampling or sample difference techniques. Effectively, a reference (initial) sample is subtracted from subsequent measurements in order to detect the pH differences with less emphasis on the absolute pH. Consequently, linear input-output characteristics ensure that the useful signal variations are accurately captured and signal subtraction does not cause any undesired artefacts except removing DC. Thus, the next step in linear ISFET pixel design concerns secondary pixel characteristics which are outlined below.
ISFET pixel characteristics:

- Internal
    - Input-output linearity
    - Maximizing linear range
    - Scalability / Silicon footprint
    - Speed - Vs - Power trade-off
- External
    - Minimizing attenuation due to the floating gate structure
    - Drift and offset due to impurities in the sensing layer

In this chapter, the concept of ISFET current-mode operation is introduced with the device biased in the velocity saturation region of operation which ensures linear pH-drain current characteristics. The theoretical framework and expected characteristics which guide pixel design in current-mode (CM) are presented as well as a CMOS implementation. Furthermore, an adaptation of the CM pixel to include a programmable-gate (CM-PG) is shown which was introduced to allow for offset compensation. Finally, a voltage mode (VM) pixel is presented based on a source-follower configuration in order to serve as a comparison metric between the CM and VM approaches.

3.2 Current-Mode Pixel Design

3.2.1 Overview

CMOS Trend

CMOS compatibility ensures that the sensors conform to a scaling trend according to Moore's law [4] which has apparent benefits in terms of sensor density and thus increased in-parallel detection. However, analogue operation in sub-micron processes is significantly impacted by short-channel effects which have changed the operational characteristics of transistors. In sub-micron processes, the typical FET

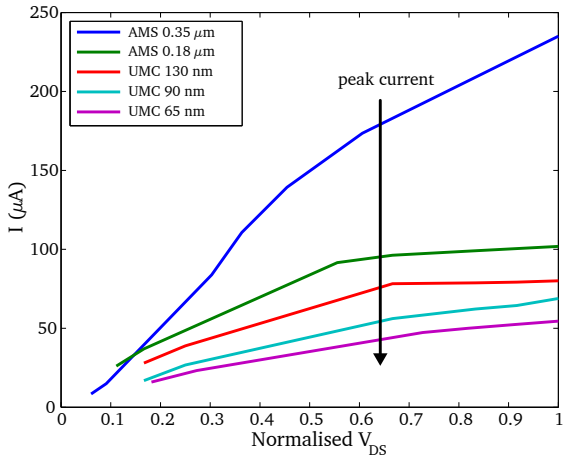


Figure 3.1: Velocity Saturation current (I_D at peak g_m) across scaling technologies.

regions of operation have shrunk to include the velocity saturation (VS) region at high electric fields. In general, biasing in VS being avoided by designers due to its low-gain properties for single transistor amplifiers [5] since the transconductance of the device no longer follows a quadratic relationship but reduces to linear due to carrier saturation effects. Nevertheless, in practice, this region is suitable for applications which benefit from a linear gate voltage - drain current ($V_{GS} - I_D$) relationship, something that is argued here that is the case for the pH-induced gate voltage variations with ISFETs operating in current-mode [6].

Following the CMOS scaling trend, the velocity saturation region is expected to occur at lower biasing voltages and drain currents, thus mitigating concerns about its corresponding power consumption. To illustrate this trend, Fig. 3.1 shows the scaling VS current across five commercial CMOS processes for a normalised V_{DS} i.e. as a percentage of the supply voltage for that process. Specifically, for each process the maximally linear current has been determined (the current whose V_{GS} maximises g_m) across V_{DS} voltages and through normalisation, a direct comparison can be made. Velocity saturation occurs for normalised V_{DS} values above 0.5 (approximately), showing the reduction of current in this region for deep sub-micron technologies.

Consequently, velocity saturation holds potential as a feasible region of operation since it provides a linear input-output relationship ($pH - I_D$) for sensing and is expected to become more dominant in the increasingly accessible sub-micron processes.

Current-Mode Imagers

Current-mode readout is an avenue previously explored in imaging arrays, approximately two decades before being considered here for chemical readout. Current was initially introduced as the signal of interest in analogue image processing owing to the trivial manner of conducting arithmetic operations in the current domain. This enabled more complicated operation such as filtering [7], convolution [8] and image reconstruction [9]. Furthermore, carrying-out on-focal-plane signal processing in the current domain has shown benefits in terms of the readout speed since no charging/discharging occurs if the output bus is kept at a fixed potential, low power supply voltage and less silicon area [10]. The main drawback of current-processing has traditionally been higher noise (quantified as Fixed Pattern Noise in the imager community) due to the electrical characteristics of the active device [10, 11]. Consequently, improving pixel matching and image quality using noise suppression and correlated double sampling circuits has been a major concern in CM optical pixel design which has hindered the CM approach from fully competing with VM in recent years.

Operating in linear current-mode (as opposed to exponential in weak inversion) was initially shown with the active device biased in the triode region [12]. Non-ideal effects such as mobility dependence on the gate voltage of the readout device and non-linear photodiode voltage discharge were highlighted as the major causes of non-linearity. Mobility dependence is not a concern in VM which uses a source-follower for readout since the mobility relationship depends on the overdrive voltage term ($V_{GS} - V_{th}$) which stays constant. To further compare the two approaches, a dual mode imager was shown in [13], with voltage mode operation compared to current mode which included readout devices biased both in triode and velocity saturation. Velocity saturation showed higher linearity compared to triode due to less dependence on second-order sources of non-linearity but lower compared to VM. Additionally, design consideration regarding the sizing requirements for the readout device were highlighted and are included in Table 3.2. The VS approach was elaborated further in [14, 15]. Evidently, operating in VS for image sensors pixel showed advantages regarding linearity (due to higher output impedance and improved mismatch) and compatibility with advanced (sub-micron) CMOS processes, nevertheless even after CDS and correction for the output bus potential variation, the FPN level was close but not better than VM. A summary of current-mode imagers operating in either the triode or velocity saturation regions of operation is outlined in Table 3.1.

A fundamental difference between optical imagers and ISFET arrays is the requirement for reset. In imagers, every pixel provides an illuminosity-dependent signal which is independent at each frame readout i.e. an absolute value is recorded. Therefore CDS is used to minimise mismatch and offsets of the instrumentation. Instead, in chemical imagers this approach can't be adopted since differences

betwen measurements are considered and there is no need for reset. Temporal signal differences are the objective and offsets due to trapped charge will not be improved after CDS.

Table 3.1: History of Current-mode Imagers

Year	Node (μm)	Array Size	Biasing region	Ref.
1997	0.8	768 × 512	Saturation	[16]
2004	0.5	40 × 40	Triode	[12]
2006	0.5	300 × 200	Triode/VS/VM	[13]
2006	0.35	128 × 128	-	[17]
2006	0.18	100 × 50	Triode	[18]
2007	0.35 / 0.18	40 × 40	Triode	[19]
2007	0.5	110 × 200	Velocity Saturation	[14]
2008	0.25	576 × 576	Velocity Saturation	[20]
2008	0.5	100 × 256	Triode	[21]
2008	0.5	50 × 128	Triode	[22]
2010	0.5	128 × 109	Triode	[23]
2012	0.6	128 × 109	Triode	[24]
2014	0.18	54 × 60	Velocity Saturation	[15]
2014	0.18	220 × 128	Triode	[25]

ISFETs in Current-Mode

Taking the above into consideration, similar principles apply regarding designing an ISFET current-mode pixel for chemical sensing compared to an imaging one. In this case, the ISFET will serve as the transconductance device biased in CM whereas the photodiode and reset switch are no longer needed and the overall design can be simplified. Design methodologies with ISFET biasing in the triode or velocity saturation regions have been presented in [6] with a qualitative summary shown in Table 3.2.

Despite the expected benefit of lower pixel power consumption (due to lower ISFET drain current), triode region biasing is not adopted here for two main reasons. Firstly, it shows more susceptibility to sources of non-linearity such as mobility degradation as identified in [13] and secondly, it would require a generally large device in a sub-micron process to ensure short-channel effects do not occur. On the contrary, theoretical analysis in the rest of this chapter shows that VS is insensitive to length mismatches which usually occur with short length devices, naturally benefits from a small device (and thus small pixel footprint) and ensures a large linear range. Regarding noise performance, a small device will indeed contribute more low-frequency noise which however in both cases will be buried in

[2]This regards pixel only. In an array, the peripheral hardware consumption is expected to be the dominant contribution.
[3]Considering the frequencies of interest ($< 10\ kHz$) where flicker noise is more dominant.

Table 3.2: Qualitative comparison of ISFET biasing in Current-Mode with ✓indicating a score.

	Triode Region	Velocity Saturation
Linearity	✓✓	✓✓✓
Gain (g_m)	✓	✓✓✓
Speed	Comparable	
Power consumption[2]	✓✓	✓
Z_{out}	✓	✓✓
Scalability	Comparable	
Device Sizing	$\downarrow W \uparrow L$	$\downarrow W \downarrow L$
Noise[3]	✓✓	✓

the chemical noise that has been shown to be at least an order of magnitude higher than electrical [26]. As a result, biasing in velocity saturation is adopted for ISFET current-mode readout.

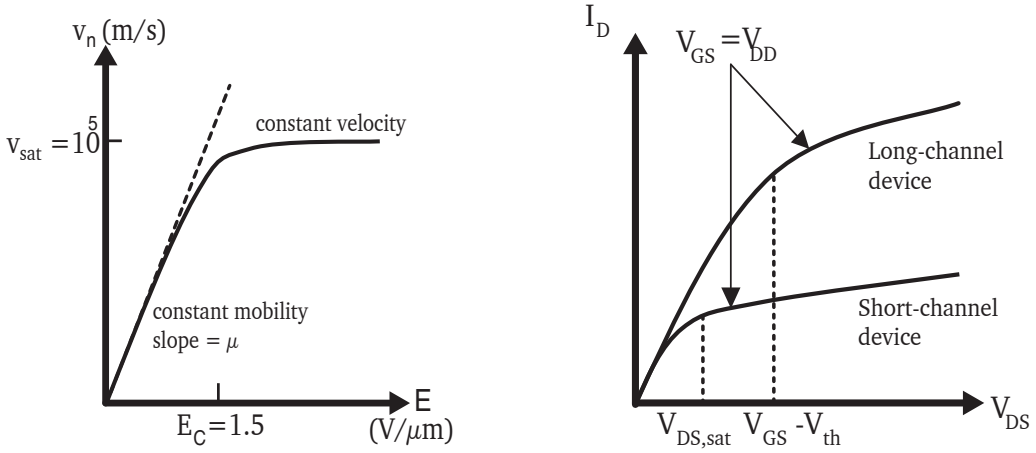
3.2.2 Velocity Saturation Fundamentals

In sub-micron processes, second-order effects such as carrier velocity saturation, threshold voltage variations and hot carrier effects which were often ignored with long channel devices (when $L > 1\mu m$) are becoming more prominent and have already started to dictate the operation of devices. Velocity saturation of the charge carriers when travelling along the channel is the most impactful effect on the characteristics of the device and is described in more detail below since it is a mode of operation that is exploited to linearise the voltage-to-current operation of the device. On the other hand, hot carrier effects (which cause a slow modification of V_{th} from extensive use due to electrons tunnelling in the oxide) and additional variations to the threshold voltage (due to V_{th} becoming a function of L, W and V_{DS} on top of V_{BS} and process parameters) cause smaller deviations especially when the device is biased in velocity saturation. Here, the focus is on the most impactful effects and the main causes of deviation from the expected characteristics.

The behaviour of a MOSFET is typically described with the model shown below:

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right] \tag{3.1}$$

where μ_n is the mobility of carriers (electrons), C_{ox} the oxide capacitance and $W\&L$ the device's dimensions. The carrier mobility μ_n determines the electron velocity v_n scaled by the electric field E



(a) Carrier velocity saturates at high lateral electric field values.

(b) The I-V characteristics are modified to show an extended saturation region.

Figure 3.2: Expected behaviour of a short channel device due to velocity saturation.

along the channel ($E \propto V_{DS}$).

$$v_n = -\mu_n E(x) \tag{3.2}$$

where x denotes distance. For decreasing transistor size, the effective channel length decreases which causes the electrical field along the channel ($E(x)$) to increase. Consequently, the electron velocity should increase at a rate proportional to the rising electric field as described in Eq. 3.2. However, when a critical velocity value is reached, $E_C = 1.5 \times 10^6\, V/m$ for p-type silicon, the carrier velocity tends to saturate approaching a rate $v_{sat} = 10^5\, m/s$ (shown in Fig. 3.2a) due to collision and scattering effects. The drain-source potential that corresponds to the E_C field value is denoted $V_{DS,sat}$, above which the carrier velocity stays approximately constant. At higher V_{DS} potentials, carriers reach the saturated velocity earlier along the channel as they propagate from the source to drain diffusion regions. Under these conditions, a first order approximation for modelling the device can be made by assuming that:

$$v = \begin{cases} \mu_n E(x) & \text{for } E \leq E_C \\ \mu_n E_C = v_{sat} & \text{for } E \geq E_C \end{cases} \tag{3.3}$$

Additionally, the drain-source potential at which E_C is reached is assumed to be constant and given by:

$$V_{DS,sat} = L \times E_C = L\frac{v_{sat}}{\mu_n} \tag{3.4}$$

Therefore, operation in the triode region remains the same as the case of a long-channel device whereas the saturated current $I_{DS,sat}$ equation is obtained by substituting Eq. 3.4 to Eq. 3.1. As shown in Fig. 3.2b, $V_{DS,sat}$ occurs earlier than $V_{GS} - V_{th}$ and an extended saturation region is obtained. Furthermore, $I_{DS,sat}$ and the maximum transconductance (gain) in this region are described by:

$$I_{DS,sat} = v_{sat} C_{ox} W \left[(V_{GS} - V_{th}) - \frac{V_{DS,sat}}{2} \right] \tag{3.5}$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = v_{sat} C_{ox} W \tag{3.6}$$

According to the equations above, in velocity saturation the drain current is linearly dependent on the overdrive voltage $V_{GS} - V_{th}$ and the width W of the device while being insensitive to V_{DS}. Additionally, the saturated current is less dependent on second order effects such as mobility (μ) degradation as well as the device's length (L) which suggests that infinite output impedance is expected and that operation is insensitive to length mismatches which usually occur with minimum length devices. In practice, the device exhibits a high output impedance and channel length modulation similar to normal saturation due to the fact that different regions along the channel might behave as in different regions of operation, specifically velocity saturation early on along the channel and normal saturation throughout the rest. However, higher output impedance is expected in general which reduces the susceptibility to bias voltage variations and increases its usability as a programmable current source. Further information on device modelling in velocity saturation and higher order effects can be found in [5, 27].

3.2.3 ISFET in Velocity Saturation

In the case of an ISFET, an additional V_{chem} term is included in the device model which appears in series with the overdrive voltage. Therefore, in velocity saturation an ISFET will behave as:

$$I_{D,ISFET} = v_{sat} C_{ox} W \left[(V_{GS} - V_{chem} - V_{th}) - \frac{V_{DS,sat}}{2} \right] \tag{3.7}$$

Thus, I_D is linearly proportional to pH and the pH sensitivity is given by:

$$g_{m(pH)} = \frac{\partial I_D}{\partial pH} = -v_{sat} C_{ox} W (\alpha S_{Nernst}) \tag{3.8}$$

As a result, the pH transconductance of the device evaluates to a constant which depends on the device's width, process parameters and the quality of the sensing layer. As long as the transconductance

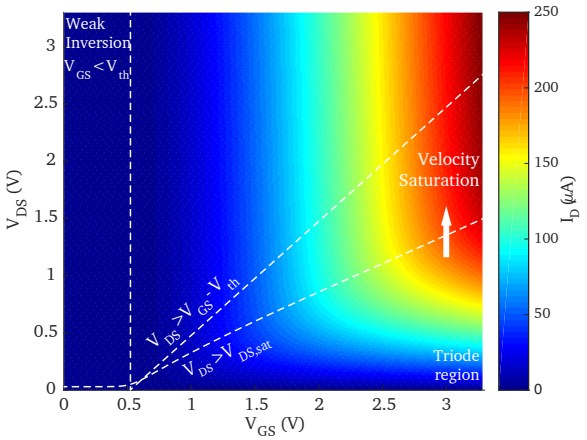
is constant, given the operating conditions, then linear pH-to-current conversion is ensured. From the above equations, insight on how to size an ISFET for operation in velocity saturation can be derived. Specifically, a short length is naturally selected to ensure that velocity saturation is reached whereas a short width might also be preferred in order to limit the biasing current occurring at high V_{GS} and V_{DS} potentials. Effectively, sizing the sensing device comes down to a trade-off between DC current bias in velocity saturation and device gain in this region ($g_{m_{(pH)}}$). In the 0.35 μm process used here, the device has been sized such that the velocity saturation current is in the order of $100\,\mu A$ and maximum $200\,\mu A$ as a trade-off between sufficient gain against pixel power consumption.

To verify the expected characteristics, Fig. 3.3 shows simulation results of the drain current and transconductance of a short length device in the 0.35 μm commercial CMOS process. Both I_D and g_m are plotted on linear axes and shown as a function of the V_{GS} and V_{DS} potentials of the device with the substrate tied to ground ($V_{BS} = 0V$).

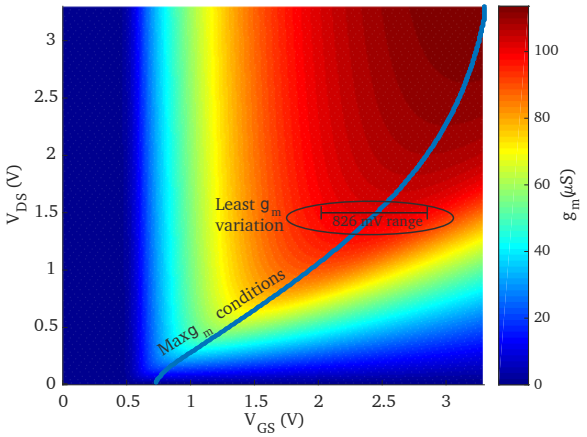
Evidently from Fig. 3.3a velocity saturation causes the device to display an extended saturation region since $V_{DS,sat}$ occurs earlier than the typical "knee" of the $I_D - V_{DS}$ response (when $V_{DS} \geq V_{GS} - V_{th}$) with a long channel device. As a result, a linear $I_D - V_{GS}$ response is expected with the gradient (gain) given by the transconductance of the device. Considering the 3D transconductance of the same transistor on Fig. 3.3b, g_m increases with increasing V_{GS}, for a given V_{DS}, until a relatively flat peak is reached and subsequently decreases due to second order effects such as mobility degradation. This behaviour is similar to the expected response for a long channel transistor which exhibits only traditional saturation however in this case g_m will not reach such a high value and will show a flatter peak. Additionally, for very high V_{DS} potentials $\left(V_{DS} > \frac{V_{DD}}{2}\right)$, g_m increases monotonically with increasing V_{GS} and reaches its highest point when V_{GS} approaches the power supply.

In the case of designing an ISFET for linear $V_{GS} - I_D$ conversion, the major concern is a large g_m to maximize the intrinsic gain as well as obtaining a wide peak to ensure linearity. Furthermore, it is preferable to do so without resorting to very high V_{GS} and V_{DS} potentials (and thus drain current) which will increase the power consumption of the sensor. As a result, the best biasing point for a current-mode ISFET is annotated in Fig. 3.3b where the widest linear range is recorded as a trade-off with biasing current.

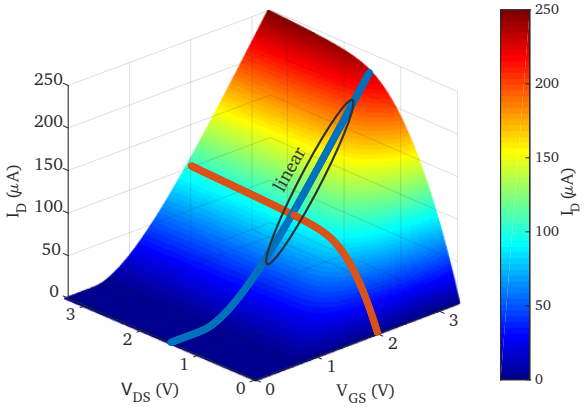
To determine the expected operating range for a single device, we assume a maximum pH sensitivity of $59\,mV/pH$ ($\alpha = 1$) therefore the entire pH scale would need $14 \times 59 = 826\,mV$. In practice, the observed sensitivity rarely exceeds $50\,mV/pH$ which would need very high quality sensing membranes, therefore $700\,mV$ would cover the entire pH range. Nevertheless, this model doesn't take into account the signal attenuation due to the passivation capacitance observed at the floating gate as well as



(a) Drain current (I_D) 3D plot with operating regions annotated.



(b) Transconductance (g_m) 3D plot. The region with the flatter g_m is annotated with peak $g_m = 100.9\,\mu S$ and variation of $\pm 3.88\%$ for a $826\,mV$ range at $V_{DS} = 1.5\,V$.



(c) Indicative cross-sections of the drain current 3D plot at $V_{DS} = 1.5\,V$ (blue) and $V_{GS} = 2\,V$ (orange).

Figure 3.3: Simulation of a short channel transistor with $W/L = 0.5/0.4\ \mu m/\mu m$, in the AMS 0.35 µm process with 3.3V supply showing the (a) drain current, (b) transconductance and (c) cross-sections of (a) as a function of the V_{DS} and V_{GS} potentials with $V_{BS} = 0\,V$.

trapped charge at the passivation layer which typically occurs with floating gate devices. For a single device,offsets can be mitigated with precise biasing of the reference electrode, however for an array of sensors sharing a common reference electrode different biasing points across devices can be expected. As a result, it is preferable to operate in a region which offers the widest linear range possible. This way, global biasing of the sensors through the reference electrode can be optimized to maximise the number of active pixels irrespective (to a degree) of trapped charge mismatch while delivering linear input-output transduction.

Table 3.3: ISFET Linearity in Velocity Saturation

V_{GS} Range	I_D Linearity (R^2)
826 mV	99.999 %
1 V	99.998 %
$V_{DS,(sat)} \rightarrow V_{DD}$	99.128 %
$V_{th} \rightarrow V_{DD}$	98.814 %

In order to quantify the linearity of the device for a given V_{GS} range, the coefficient of determination R^2 is used which indicates the extent to which the data points approximate a straight line. Table 3.3 shows indicative V_{GS} ranges and the corresponding linearity in I_D for the device plotted in Figs. 3.3a-3.3c. Evidently, a short channel device biased in velocity saturation achieves almost perfect linearity, remarkably consistent throughout a large range of V_{GS}. This is a consequence of carrier velocity saturation ($V_{DS} = 1.5\,V$) which corresponds to a peak $g_m = 100.9\,\mu S$ varying only by $\pm 3.88\%$ across a $826\,mV$ range. Therefore, it is possible to convert the pH-induced V_{GS} variations to drain current variations in a linear fashion with no linearisation method considered other than designing the underlying device to operate in velocity saturation.

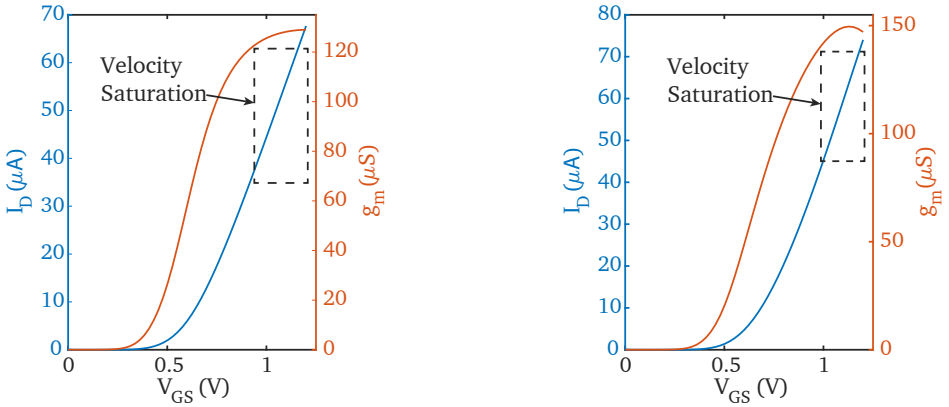
Comparison with 65nm

The 0.35 µm process ensures that velocity saturation is reached with a short channel device while allowing for a wide range of input V_{GS} voltage for which the output current is linear. As a result, this wide range can accommodate trapped charge commonly found in ISFET sensors to a large extent without the need for mismatch calibration since the difference in successive measurements will be linear even if they start at different DC points. Compared to more advanced processes, a standard device in a 65 nm commercial process operates with a power supply of 1.2 V which reduces the available range of linear V_{GS}. To demonstrate this, Fig. 3.4 shows simulation results of the I-V characteristics in velocity saturation in a 65 nm process and Table 3.4 shows the corresponding V_{GS} range for which

Table 3.4: Linear V_{GS} range for a $W/L = 500/400\ nm/nm$ Device

Process	V_{GS} of peak g_m	Linear V_{GS} Range	Power Supply
65 nm	1.13 V	375 mV	1.2V
0.35 µm	2.47 V	1.4 V	3.3V

I_D if perfectly linear. This range has been obtained as the V_{GS} range at which g_m is maximally flat to within $\pm 10\%$ of its maximum. Alternatively, advanced process nodes typically offer the option of higher V_{DD} devices for analogue applications. In the 65 nm process, devices with 2.5 V supply can be used to increase the available linear V_{GS} range in velocity saturation. However, these devices have an increased minimum device size of $W/L = 400/280\ nm/nm$ which is comparable to minimum size in the 0.35 µm process and offer comparable performance with similar silicon area.



(a) $W/L = 120/60\ nm/nm$ (b) $W/L = 500/400\ nm/nm$

Figure 3.4: $I_D - V_{GS}$ and g_m characteristics in a 65 nm commercial process with $V_{DS} = V_{DD}/2 = 0.6V$. The device in (a) is minimum size and in (b) is the same size as the device in Fig. 3.3.

3.2.4 Expected Attenuation in CM

Apart from selecting biasing region, designing an ISFET entails taking into account the attenuation of the input signal due to the floating gate structure of the device. Sensing takes place via the site-binding characteristics of the passivation Si_3N_4 material thus this layer leads to the formation of an equivalent capacitance, (denoted C_{pass}). As a result, a series capacitive network is formed due to C_{pass} in conjunction with the gate parasitic capacitances (and chemical capacitances) as shown in Fig. 3.5. C_{pass} is typically several orders of magnitude smaller than the chemical capacitances [28] therefore the passivation primarily determines the overall behaviour. In fact, the case when C_{pass} and C_{gg} are of similar order of magnitude essentially determines the worst case coupling efficiency of the chemical signal to V_{GS}.

C_{pass} can be estimated by taking into account the size of the top metal layer $(W \times L)_{chem}$ which is typically defined by the pixel size as well as the process parameters (passivation thickness and dielectric constant) in a structure as shown in Fig. 2.3 using Eq. 2.24.

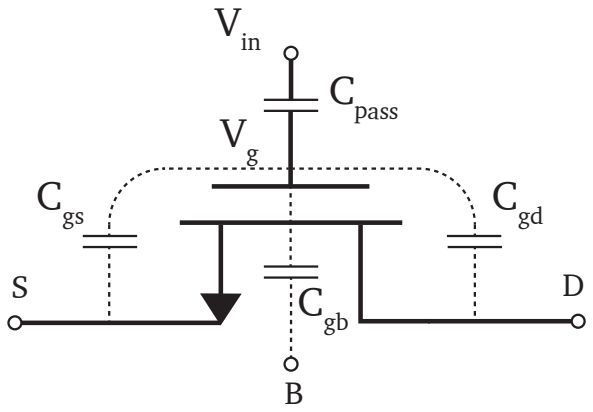


Figure 3.5: Simplified ISFET macromodel showing the capacitive network created due to the formation of an equivalent passivation capacitance in series with the gate parasitic capacitances.

Furthermore, the attenuation depends on the magnitude of the gate parasitic capacitances which depend on both the gate area and biasing region as described in [4]. In the CM case, a single device operates with fixed V_{DS} and V_{GS} potentials, hence the attenuation A can be described by:

$$A = \frac{V_g}{V_{in}} = \frac{C_{pass}}{C_{pass} + C_{gg}} \tag{3.9}$$

where $C_{gg} = C_{gd} + C_{gs} + C_{gb}$ denotes the sum of the gate parasitic capacitances.

From Eq. 3.9, the attenuation minimizes for a large passivation capacitance and/or small gate parasitics. In a given CMOS process (thus materials with fixed thickness and dielectric constants), C_{pass} is directly proportional to the size of the top metal electrode therefore a larger metal area is beneficial. Nevertheless, this comes at the expense of a larger pixel area with trade-offs associated with increased silicon area, array resolution and compactness. Alternatively, the attenuation can be reduced by using a small size device which ensures C_{gg} is small. In current-mode, having a small device is required in order to reach the velocity saturation region. Therefore, the gate parasitics are reduced to a minimum thus attenuation in current-mode is a function of the size of C_{pass} which constitutes a trade-off with pixel size. This trade-off needs to be optimized to achieve a scalable pixel design but also ensure sufficient resolution for the target application.

3.2.5 Pixel Design

Similarly to the current-mode imager architecture as in [19], the proposed configuration is a 2-transistor (2T) topology and is shown in Fig. 3.6. It consists of an ISFET device and a column selection switch thus achieving a very small silicon footprint. The ISFET is designed to operate in its target operating region through suitable biasing set by both the external reference electrode potential and the voltage of the drain row, V_{DR}. V_{DR} will be set by a current conveyor (shown in Fig. 4.2(e)) which fixes the effective V_{DS} of the device and provides the pixel current in velocity saturation ($I_D < 200\,\mu A$). External control through the reference electrode will be used to set the gate biasing of the device whereas reaching the target region will verified by monitoring the output current. Furthermore, external control of V_{ref} allows for voltages larger than V_{DD} to be applied if trapped charge of such magnitude needs to be accommodated.

This design corresponds to a silicon footprint of $6.5 \times 7.8\ \mu m^2$ shown in Fig. 3.6b and indicates the size of the top metal (MET4). Using Eq. 2.24, this metal size results to an estimated passivation capacitance of $C_{pass,CM} = 1.15\,fF$. In order to get an estimate of the attenuation A (Eq. 3.9), the lumped gate-parasitics value $C_{gg} = 0.815\,fF$ is obtained from the simulator software[4] as well as the extracted capacitance post-layout from the floating gate to ground $C_{fg-GND} = 0.930\,fF$ [5]. As a result, the expected attenuation evaluates to $A_{gg} = 0.59$ and $A_{fg-GND} = 0.55$ respectively.

Pixel Evaluation

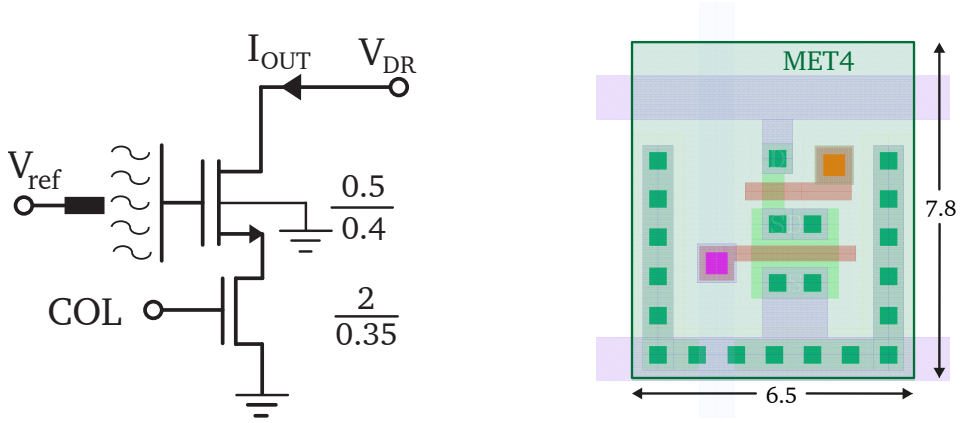
To verify the expected output current range for step pH changes, Fig. 3.7a shows the corresponds I_D step occurring at VS biasing through the reference electrode. A pH sensitivity of $30\,mV/pH$ was assumed which was previously shown for ISFETs in CMOS [29]. The corresponding step changes in drain current effectively show the transconductance of the device and are perfectly linear ($R^2 = 1$) as shown in Fig. 3.7b. In this region, g_m is approximately flat (shown in Fig. 3.3b) which enables linear pH-current conversion with around $3\,\mu A/pH$ sensitivity. As a result, no additional signal amplification is required for detection.

Overall, the CM pixel provides a feasible and scalable design owing to the simplicity of the pixel architecture and suitable biasing in VS. Risks associated with this approach concern primarily the trade-off between pixel size and scalability. A small pixel size ensures a small silicon footprint and scalability into large arrays, yet it introduces signal attenuation since C_{pass} is of similar order of magnitude as the

[4] Simulations were carried-out in Cadence Virtuoso IC6.1.7-64b.500.4.

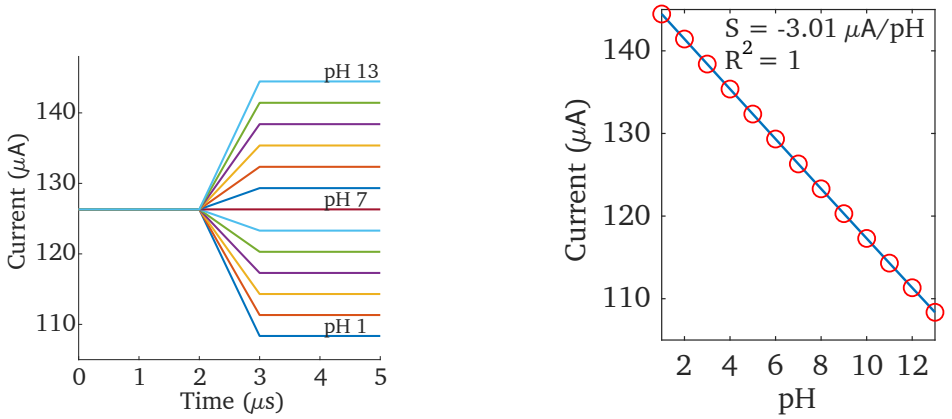
[5] The extracted capacitance value was obtained using Mentor Graphics Calibre PEX Toolbox v2012.2 and PEX v2017.3_38.30.

gate parasitic capacitances. This effect can be mitigated by using a very small device (optimum for VS biasing) and designing metal layers (e.g. signal buses) as fas away as possible from the floating gate. In this case, this trade-off resulted into a pixel of $50\,\mu m^2$ silicon area with an expected attenuation of around 0.57. Furthermore, a potential limitation regarding scalability will be the variation in V_{DR} for long buses due to the metal track resistance. This effect is mitigated in velocity saturation (which is relatively insensitive to V_{DS} variations) nevertheless, an improvement in this case would be a feedback mechanism similar to [15].



(a) Schematic (b) Layout

Figure 3.6: Current-Mode (CM) pixel operating in velocity saturation. All sizes in μm.



(a) Transient pH steps (b) Corresponding pH sensitivity

Figure 3.7: Transient simulation showing the sensitivity to pH steps assuming a sensing layer sensitivity of $30\,mV/pH$, $V_{DS} = 1.5V$ and V_{GS} of max g_m.

3.3 CM with Programmable-Gate

3.3.1 In-pixel Programmable-Gate for Offset Compensation

ISFETs fabricated in unmodified CMOS are in a frontrunner position to be adopted as the front-end for fully-electronic chemical sensing. However, the resulting floating gate structure has been shown to be susceptible to trapped charge at either the floating gate or in the passivation layer which manifests as large threshold voltages and mismatch between devices. Effectively, this phenomenon causes a large and random offset between devices of several hundred millivolts [26]. Overall, the main operational drawback is that assuming an ISFET array with common biasing through the reference electrode, a large pixel mismatch may cause ISFETs to deviate from their target operating region. Also, it is important to note that mismatch due to trapped charge is expected to be significantly higher than the electrical mismatch due to process variations. In this case, biasing in VS is beneficial since its large linear range allows for a large trapped charge spread to be accommodated without the need for further compensation.

Suitable compensation methods as well as more in-detail explanation on the origin of trapped charge is included in Chapter 2. In brief, compensating for trapped charge can take the form of post processing or a circuit-based technique. Post processing typically requires UV irradiation of the floating gate [30] whereas circuit-based techniques include either a programmable gate [31] or a gate reset switch [32]. A gate reset switch has been shown to reduce the offsets amongst pixels of an array but to significantly increase the total drift observed due to leakage through the switch [33].

On the other hand, the programmable gate (PG) approach introduces an additional gate capacitor C_{CG} which is used to modify the floating gate gate potential while keeping the gate electrically floating, as shown in Fig. 3.8. This way post processing steps such UV irradiation are avoided and biasing of the device is reconfigurable. The drawback of this approach is the introduction of an additional element inside the pixel which compromises the pixels area/scalability.

An ISFET with a Programmable-Gate is shown in Fig. 3.8 and will operate the same way as described in Section 3.2 with a new floating gate potential established through the weighted sum of the surrounding potentials:

$$V_{FG} = \frac{V_G' C_{pass} + V_{CG} C_{CG} + V_S C_{gs} + V_D C_{gd}}{C_T} \tag{3.10}$$

$$C_T = C_{gg} + C_{pass} + C_{CG} \tag{3.11}$$

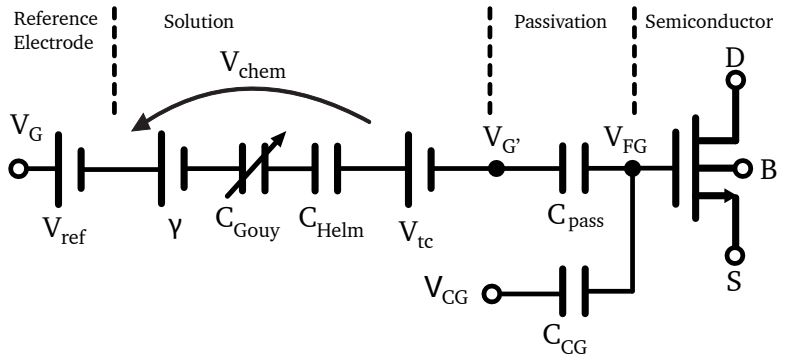


Figure 3.8: Programmable-Gate ISFET.

$$V_{G'} = V_G - V_{tc} - V_{chem} \tag{3.12}$$

with V_{tc} representing the trapped charge equivalent potentia which can be either positive or negative and the remaining notation follows the same definition as in Section 3.2. Evidently, the signal applied to the control capacitor can be used to compensate for trapped charge when:

$$V_{CG} = -\frac{C_{pass}}{C_{CG}} V_{tc} \tag{3.13}$$

The drawback of this approach is that the apparent pH sensitivity is reduced since variations in the input signal $V_{G'}$ are coupled to the floating gate through a gain of C_{pass}/C_T with C_T including the additional contribution of C_{CG}.

$$pH \text{ Sensitivity} = \frac{\partial V_{FG}}{\partial V_{G'}} = \frac{C_{pass}}{C_T} = \frac{C_{pass}}{\underbrace{C_{gg} + C_{pass}}_{as\ before} + \underbrace{C_{CG}}_{new}} \tag{3.14}$$

For a small device in VS, C_{pass} and C_{gg} are comparable therefore the relative size and magnitude of C_{CG} compared to both C_{pass} and parasitics determines the overall attenuation.

3.3.2 Pixel Design

Here, a PG ISFET is shown which includes a parasitic programmable gate such that the pixel scalability is not compromised. The PG capacitor has been implemented as the parasitic capacitance across metal layers in the CMOS process thus it is included *vertically* inside each pixel. As a result, the CM-PG, shown in Fig. 3.9 ,is designed with the same silicon footprint as the CM pixel (and the same C_{pass}).

The magnitude of C_{CG} depends on the dielectric of the insulation material ($\varepsilon_{SiO_2} = 4.1$), the distance between the metal layers and number of interdigited fingers. In this case, C_{CG} occurs across the

leftmost Metal 3 layer (shown in Fig. 3.9b) and the rightmost Metal 3 layer which is also connected to Metal 4 and the floating gate with a gap of $0.85\,\mu m$. In addition, to ensure that an individual V_{CG} can be applied to each pixel, two selection switches are introduced and are connected to the Metal 3 node. This approach allows for the externally provided V_{CG} to be tailored to each pixel in order to compensate for mismatch across pixels. Additional mismatches such as electrical mismatch and variations between C_{CG} will also be accommodated at an accuracy dependent on the C_{CG} gain ($\frac{C_{CG}}{C_T}$) and resolution of the V_{CG} signal.

To estimate the expected attenuation with the introduction of the additional capacitor, the gate parasitic capacitances are estimated as $C_{gg} = 0.819\,fF$ from simulations whereas the extracted (post-layout) value of the floating gate to ground capacitance is $C_{fg-GND} = 0.748\,fF$. The extracted value of $C_{CG} = 3.27\,fF$ [6]. A similar order of magnitude across all capacitances is obtained which means that C_{CG} can be used to fine tune the floating gate voltage. The corresponding attenuations are given by $A_{gg} = 0.219$ and $A_{fg-GND} = 0.222$.

Pixel Evaluation

With the extracted values of $C_{CG} = 3.27\,fF$ and $C_{pass} = 1.15\,fF$, Fig. 3.10 illustrates the programmability of the PG ISFET. A shift of approximately $640\,mV$ is obtained for step changes of $1\,V$ in V_{CG}. To verify this, the expected floating gate sensitivity to C_{CG} using the extracted capacitance values is given by:

$$\frac{\partial V_{FG}}{\partial V_{CG}} = \frac{C_{CG}}{C_T} = 0.63 \tag{3.15}$$

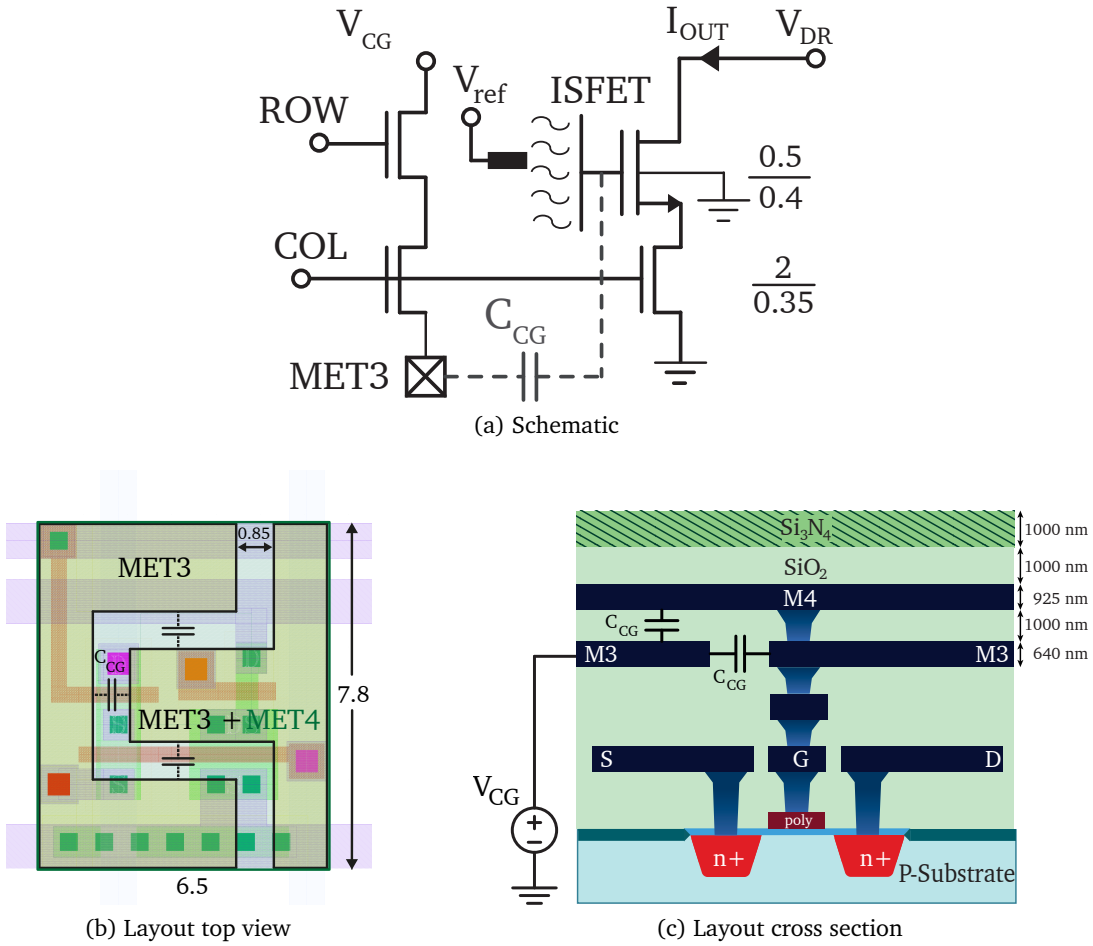
Overall, with a maximum supply voltage of 3.3V, this approach can compensate for trapped charge of up to $2.11\,V$ per pixel.

3.4 Voltage-Mode Pixel Design

3.4.1 Overview

In this section, the design of a voltage-mode (VM) pixel for ISFET-based chemical sensing is presented. Voltage-mode ISFET pixels resembling the widely used 3T-APS in imagers have already been adopted in the case of designing very-large-scale ISFET arrays for DNA sequencing [1]. In this case, a similar configuration is adopted with the aim of providing a benchmark to compare the proposed CM pixels

[6] The measured value of after fabrication was determined at $C_{CG} = 0.96\,fF$ using the method outlined in Appendix C.



(a) Schematic

(b) Layout top view

(c) Layout cross section

Figure 3.9: Current-Mode with a parasitic PG (CM-PG) pixel operating in velocity saturation. All sizes in μm.

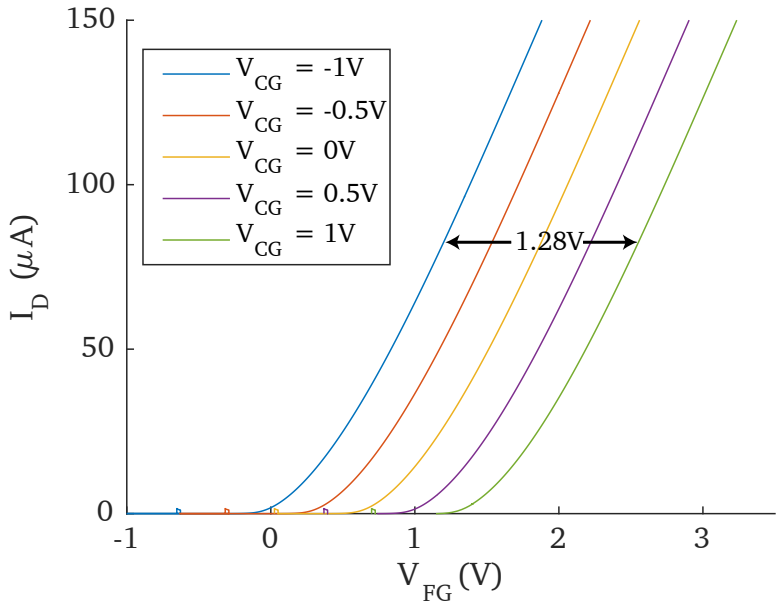


Figure 3.10: PG-lSFET programmability through step changes in V_{CG} of 0.5V causing an effective change of 0.32V at the floating gate.

with the main linear VM configuration. Fabricating all configurations on the same silicon will allow for the first head-to-head comparison of CM against VM, covering linear topologies and sharing the same sensing layer i.e. same pH sensitivity. This way a *homogeneous* comparison is possible which is not straightforward otherwise given the two modes of operation.

A theoretical analysis of the expected attenuation using an ISFET in a source-follower configuration is presented below including the differences with CM. Subsequently, a VM pixel with programmable load is demonstrated.

3.4.2 Expected Attenuation

In the case of a source follower configuration, a fixed current biases the ISFET in saturation to set the V_{GS} potential. Thus, the signal sensed at the floating gate is buffered to the source with a corresponding gain G_{SF} described in [5] and given by:

$$G_{SF} = \frac{V_{out}}{V_g} = \frac{\frac{1}{g_{mb}}//r_o//r_S}{\frac{1}{g_{mb}}//r_o//r_S + \frac{1}{g_m}} \tag{3.16}$$

The described voltages are shown in Fig. 3.11a with V_{out} denoting the voltage at the source terminal, g_{mb} the transconductance due to non-zero body-source voltage, r_o the device's output impedance and r_S the impedance looking in the current sink. From the above equation, it is evident that $G_{SF} < 1$ and is typically ~ 0.85.

G_{SF} appears across C_{gs} which scales that capacitance according to the Miller effect by: $C'_{gs} = C_{gs}(1 - |G_{SF}|)$. Overall, the effective value of C_{gs} reduces and the input signal (probed at the floating gate) experiences a two-fold attenuation A_{SF} described by:

$$A_{SF} = \frac{V_{out}}{V_g} \times \frac{V_g}{V_{in}} = \underbrace{\frac{\frac{1}{g_{mb}}//r_o//r_S}{\frac{1}{g_{mb}}//r_o//r_S + \frac{1}{g_m}}}_{G_{SF}} \times \underbrace{\frac{C_{pass}}{C_{pass} + C_{gs'} + C_{gd} + C_{gb}}}_{G} \tag{3.17}$$

Overall, any input signal will be attenuated through this network which can be generalized using the macromodel in Fig. 3.11b such that:

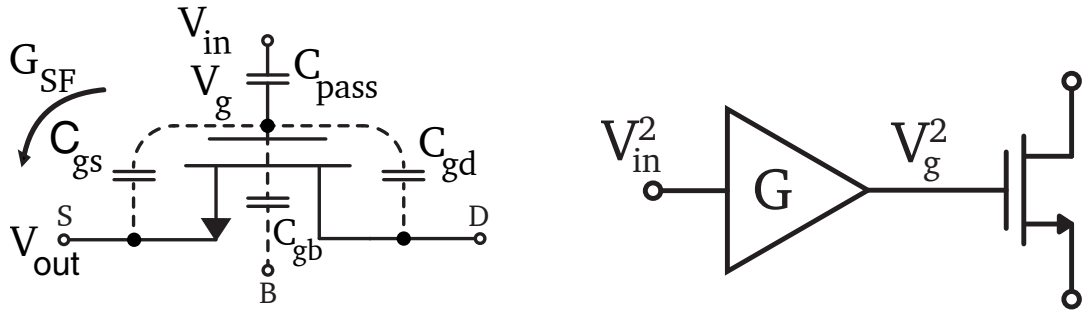
$$V_{in}^2 = \frac{V_g^2}{G^2} \tag{3.18}$$

where $G = \frac{V_g}{V_{in}}$. Overall, G_{SF} shows dependency on the operating region and the gate area (which determine the magnitude of the parasitic capacitances [4]) and is fixed for a given biasing condition whereas the second term G depends on the sizes of the sensing area and the ISFET device and is fixed

for a given design.

$$G_{SF} = f(V_{GS}, V_{DS}, W, L) \quad G = f(W, L, W_s, L_s) \tag{3.19}$$

where W_s, L_s denote the size of the top metal defining the pixel size.



(a) Gate parastitic capacitances. (b) Macromodel behaviour

Figure 3.11: Device in a source follower configuration.

Compared to CM, larger gate parasitic capacitances are expected since VM design does not benefit from a minimum or very small device. However, the effect of the major parasitic contributor C_{gs} will be mitigated due to Miller effect so overall the attenuation $\frac{V_{out}}{V_g}$ should be better than CM. Nevertheless, an additional term G_{SF} exists which will increase attenuation by ~ 0.85.

3.4.3 Pixel Design

The voltage mode pixel configuration is shown in Fig. 3.12. It consists of the ISFET device in a source follower configuration with a programmable load. An externally supplied signal, V_{load} sets the bias current through the pixel to ensure that the ISFET operates in saturation. All the remaining transistors operate as switches which serve a dual role: select the intended pixel through the row and column signals and reduce the power consumption of the array by turning off the pixel when the corresponding row is not selected.

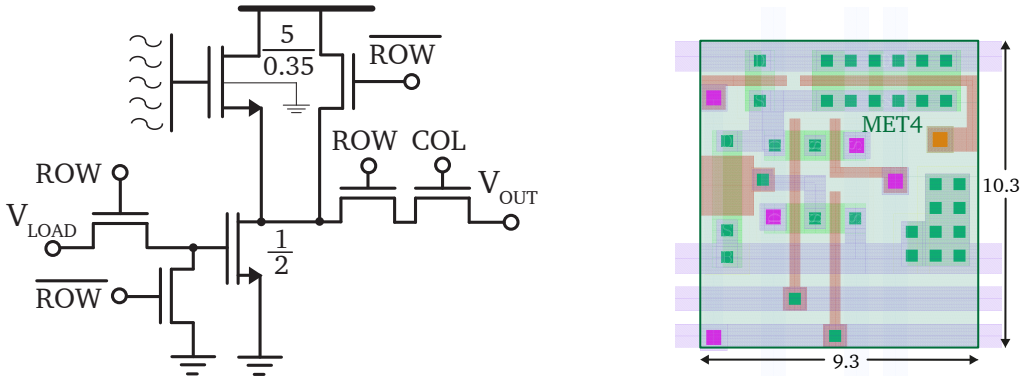
The layout of the VM pixel is shown in Fig. 3.12b with a silicon footprint of $9.3 \times 10.3\,\mu m^2$ which corresponds to a passivation capacitance of $2.17\,fF$. Furthermore, the value of the parasitic capacitances have been determined from simulations as $1.99\,fF$ (after taking Miller effect into consideration) which corresponds to an expected attenuation of $A_{VM} = 0.52$. Parasitic extraction in this case will not give representative results given the gain across C_{GS}.

Pixel Evaluation

The pixel operation is shown in Fig. 3.13 as a function of the ISFET V_{GS} and programmable pixel load V_{load}. Linear input-output $V_{GS} - V_{out}$ characteristics are obtained where the transconductance is

uniform. From Fig. 3.13a and 3.13b, the pixel biasing current I_D and g_m are constant in the annotated regions. Lower V_{load} causes both the ISFET and load device to operate in weak inversion whereas higher V_{load} reduces the available voltage headroom. Therefore, $V_{load} = 1\,V$ is chosen as the operating point which corresponds to $I_{bias} = 7\,\mu A$.

Fig 3.13c shows the pixel output with operating regions annotated, in order to get a feel when non-linearities occur as well as the range of operating voltages, whereas Fig 3.13d shows the V_{out} plane with a cross section at the selected $V_{load} = 1V$. The output is linear with respect to V_{GS} for a wide range.

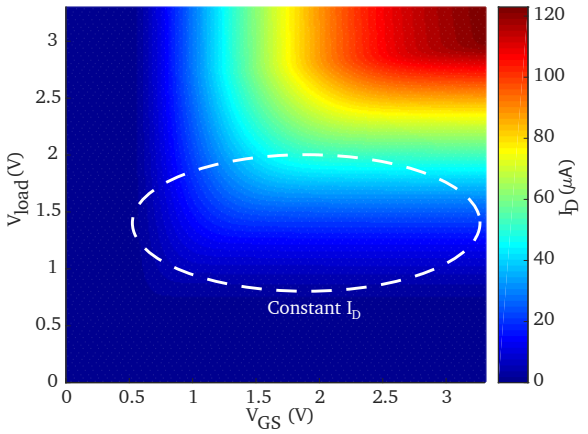


(a) Schematic (b) Layout

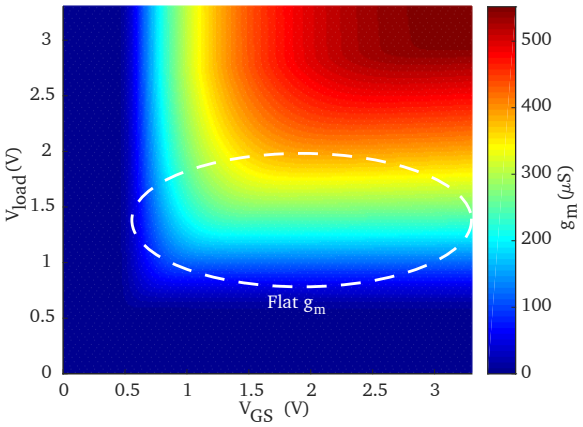
Figure 3.12: Voltage-Mode (VM) Pixel (Sizes in μm).

3.5 Comparison and Summary

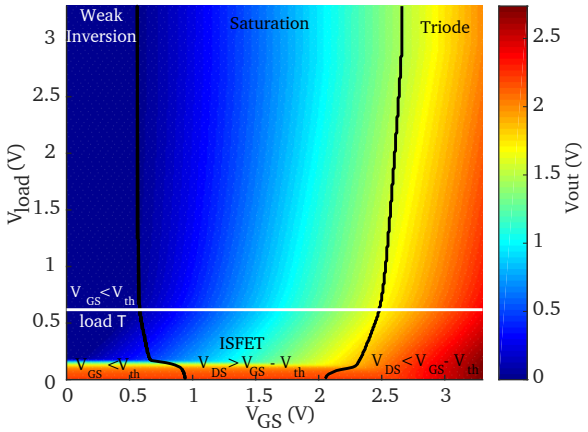
Overall, the most important factors in ISFET pixel design are input-output linearity and linear range. The first one to facilitate frame subtraction/double sampling and the second to accommodate a large spread of trapped charge across multiple sensors in an array. Both CM and VM approaches are able to deliver a large and very linear response with a corresponding current or voltage output and respective gain in $\mu A/V$ or V/V. Table 3.5 shows a qualitative comparison of the pixel configurations with the results obtained from simulations. A benefit of CM is the simplicity of the pixel design with a 2T approach and a corresponding area-effective design. The CM-PG approach has the added benefit of compensating for mismatch across pixels at the expense of reduced pH sensitivity. From an electronic point of view all approaches would ensure reliable operation and are consistent with modern CMOS processes.



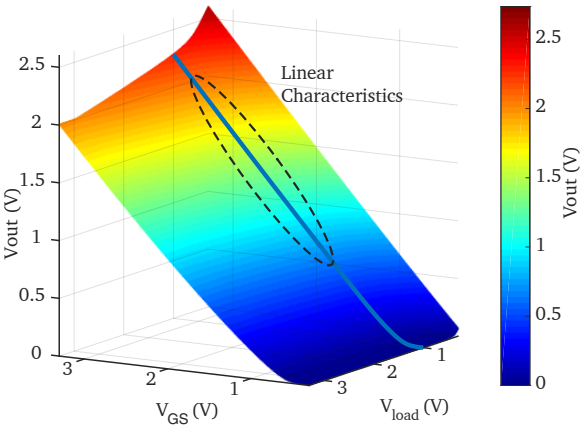
(a) Drain current (I_D) 3D plot.



(b) Transconductance (g_m) 3D plot.



(c) Pixel output V_{out}.



(d) Indicative cross-sections of the V_{out} 3D plot at $V_{load} = 1V$.

Figure 3.13: Simulation of a device with $W/L = 5/0.35\ \mu m/\mu m$ in the AMS 0.35 µm process as a function of the V_{GS} and load potential V_{load} (shown in Fig. 3.12a) with a 3.3 V supply showing the (a) pixel biasing current, (b) ISFET transconductance, (c) the pixel's output voltage and (d) cross-sections of (c) to illustrate the operating behaviour at $V_{load} = 1\,V$.

Table 3.5: Qualitative comparison of pixel configurations

	Current-Mode (in VS)	CM + PG	Voltage-Mode
Linearity	✓✓✓	✓✓✓	✓✓✓
Linear range	✓✓✓	✓✓✓	✓✓
Gain	$\sim 100\,\mu A/V$		$\sim 0.85\,V/V$
Pixel Size	✓✓	✓✓	✓
Offset Compensation	-	✓	-
Attenuation (simulated)	✗	✗✗	✗

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Chapter 4

ISFET Arrays for Large-Scale Ion Imaging

4.1 Introduction

ISFETs form an attractive substrate for Lab-on-Chip applications due to facilitating sensing while not interfering with the solution which is in direct contact. As a result, they lend themselves to sensing *array* architectures in order to maximize the amount of information extracted from the sensing surface. Such arrays have already been implemented for a number of different applications, examined in more detain in Chapter 2, where sensor arrays have been demonstrated in both single-input and multi-input applications.

The theoretical characteristics of *linear* ISFET sensing and expected behavior have been examined in Chapter 3, guiding the design of a corresponding chemical sensing pixel. Following that analysis, this chapter describes the first implementation of an ISFET Current Mode array biased in Velocity Saturation for ion imaging. This array leverages short-channel effects to facilitate perfectly linear pH-to-current transduction while exploiting the large available V_{GS} range of the 0.35 μm process to provide a large linear output current range. This way, common biasing through the reference electrode can be optimised to maximise the number of pixels within that range which are robust against trapped charge.

The CM array is characterised in depth including the performance at a pixel/array level as well as the non-idealities that appear with chemical sensors. Various metrics have been defined to quantify the performance such as linearity, speed, power consumption, size, attenuation and noise following wet measurements. Furthermore, this Chapter illustrates the methods and techniques used to obtain these metrics (e.g. deriving the pixel attenuation and trapped charge) in order to serve as a reference guide aiming to standardize the comparison of ISFET arrays. Throughout this comparison, relative merits and

limitations are identified to be used as a guide for future designs which are usually application-specific. Moving forwards, a figure-of-merit (FoM) has been derived, using all the predefined metrics, that is used to capture the overall performance of the array.

In order to fully identify the potential of the CM array, it should be benchmarked across the linear Voltage-Mode configuration also presented in Chapter 3. For this reason, all three topologies described in the previous chapter have been scaled into three arrays on the same chip. That includes the current-mode array (hereafter CM array), the CM array with the inclusion of a programmable gate (PG) for offset compensation (CM-PG array) and a linear voltage-mode configuration based on the source-follower topology (VM array). The purpose of this implementation is to compare all configurations in the most homogeneous way possible - sharing the same chip and sensing layer, therefore removing the need to consider different pH sensitivities or variations in the passivation Si_3N_4 layer. pH sensitivity typically appears as a quantifiable system metric in ISFET literature - nevertheless the inherent sensitivity (without amplification of the pH signal) occurs irrespectively of the system itself, rather as a result of the proton binding capabilities of the passivation layer. Thus, by fabricating both CM and VM on the same chip, a degree of freedom is removed and comparison regards solely the electronic performance. Despite the different modes of operation (current-vs-voltage), a head-to-head comparison is possible using the FoM defined earlier.

All ISFET arrays have been designed as part of a larger System-on-Chip (SoC) on the TTN[1] microchip which adopts a modular approach for independent control and readout from each array. Following the SoC outline and description, a microfluidics configuration and manifold are presented in order to facilitate the transition from System to Lab-on-Chip. The manifold is based on a custom design and has been used to characterise the passivation surface at various pH values and flow variations. Wet measurements as well as in-detail characterisation of the various modules of the system are presented. Data readout and visualisation takes place using a custom SPI protocol communicating to a microcontroller serving as an intermediary node between the chip and a MATLAB-based graphical user interface. The resulting chemical sensing platform is used to obtain, visualize and characterize the CM, CM-PG and VM approaches both at a pixel and array level.

Overall, the performance of an ISFET-based system depends on two factors:

(I) The electrical performance of the pixel and readout circuits.

(II) The behaviour of the material that facilitates sensing which is typically Si_3N_4 in unmodified CMOS.

[1]The microchip is called TITANICKS or TTN and is the name adopted hereafter and throughout the remaining of this thesis.

As seen in Chapter 2, the thickness of Si_3N_4 modifies the input signal attenuation (through the equivalent capacitance in Eq. 2.24) whereas Chapter 5 elaborates on the factors which affect trapped charge and drift. Evidently, the sensing (passivation) material is foundry-dependent and with limited scope of influence from the designer. In this case, no post processing steps were taken to modify the sensing layer to improve (II) hence the results concern unmodified CMOS. Instead, here the focus is on (I) and the performance of linear ISFET instrumentation arrays.

4.2 A versatile microchip for both current and voltage-mode readout

TTN is the microchip used for all measurements taken and presented in this thesis.

4.2.1 TTN System Architecture

The system has been designed in the AMS 0.35 μm process[2] and spans a silicon area of $2 \times 4\,mm^2$. The Current-Mode and Voltage-Mode arrays, based on the respective CM, CM-PG and VM pixel architectures, have been split into 4 independently-controlled sub-arrays. Two identically-sized arrays with 64×200 pixels each form the CM and CM-PG arrays. In this case, pixel size is kept the same to allow for precise determination of the reduction in pH sensitivity following the introduction of the programmable-gate capacitor in the CM-PG array. Nevertheless, the CM-PG array is the only implementation where calibration can be realized. Additionally, the VM array has been split into two smaller sub-arrays of 64×64 pixels each to better match the layout floorplan and split the maximum bus length for the unbuffered voltage signals. Fig. 4.1 shows a microphotograph of the whole chip as well as illustrations of the system floorplan.

4.2.2 Analogue Blocks

This section describes the analogue signal readout pipeline including the four arrays as well as other blocks in that pipeline.

[2]Austria Micro Systems CMOS C35 2P4M 3.3V process. It is an established process for biomedical circuits and systems with presence since 2002.

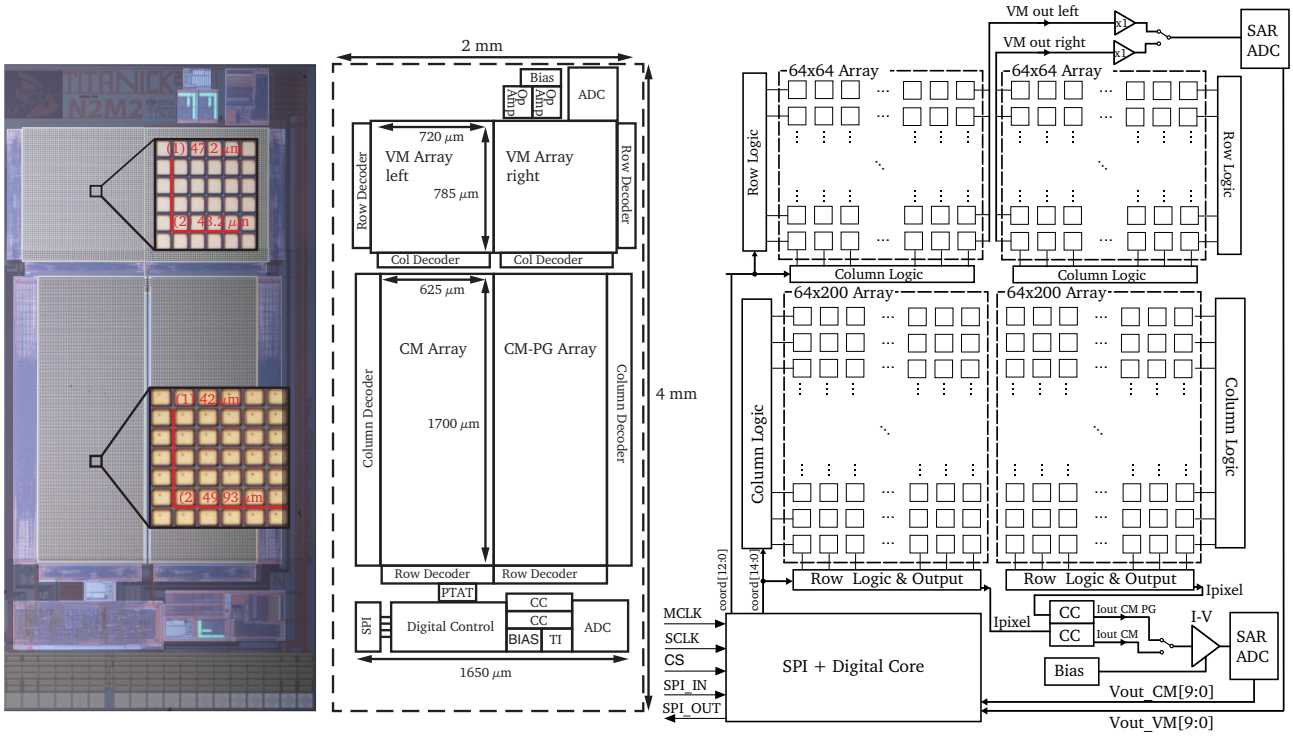


Figure 4.1: Microphotograph of the $2 \times 4\ mm^2$ fabricated chip (left) with illustrations showing the system layout and floorplan (centre and right).

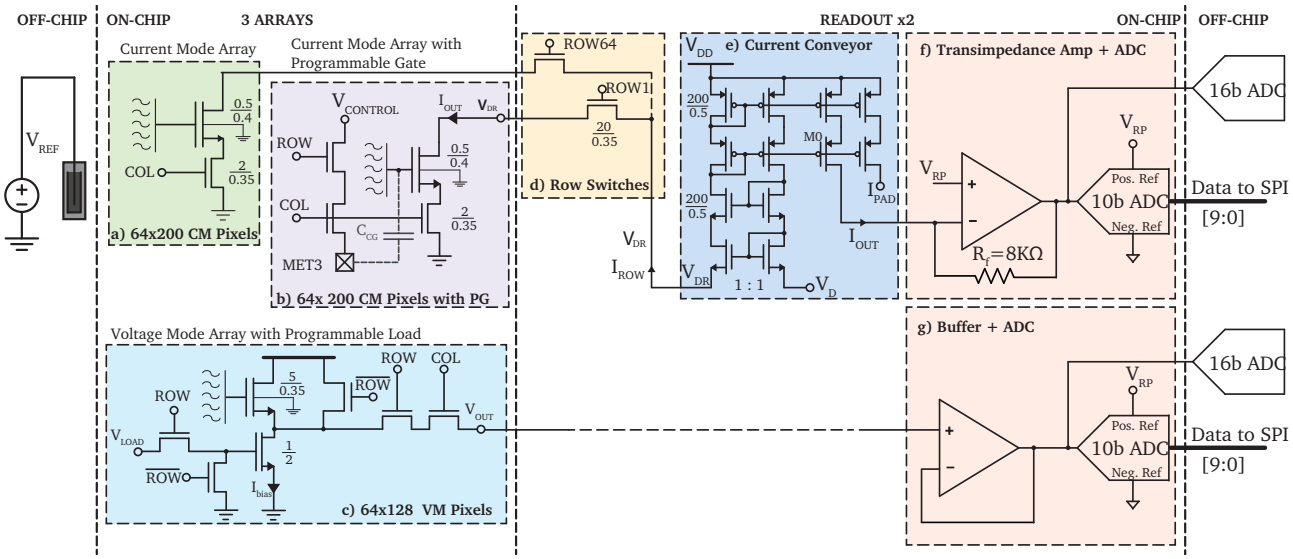


Figure 4.2: Schematic of the system showing a) CM 2T pixel architecture configured in a 64×200 array, b) CM-PG pixel architecture in a 64×200 array, c) VM pixel architecture configured in a 64×128 array, d) Row selection switches for the CM and CM-PG arrays, e) Current conveyor that sets an externally controlled voltage V_D as the V_{DR} row potential (V_{DS} of the ISFETs) and mirrors the drain current to f) a transimpedance amplifier & ADC for sampling and g) Buffer & ADC for the VM array. External ADC option is available and is used here to sample at a 16-b resolution.

Current-Mode Pipeline

Overall, following linear pH-to-current conversion and readout, the selected ISFET's drain current is generated and mirrored for current-to-voltage conversion and sampling. This approach is identical for both the CM and CM-PG topologies since pH sensing is facilitated the same way. Figs. 4.2 (a) and (b) show both the current-mode pixels which include in-pixel column selection switches (following the design in Chapter 3) whereas the row selection switches have been moved outside the pixel on a per-row basis. This way, the pixels has a very small footprint whereas the row switches can be designed with a large aspect ratio to minimize their ON resistance which appears in series with output current (shown in Fig. 4.2(d)).

The pixel current I_{pixel} is provided by a current conveyor (shown in Fig. 4.3) which is also used to fix the voltage on the drain row bus V_{DR} at a point by an externally controlled reference V_D. The current conveyor is based on a cascoded current mirror topology, previously used to provide similar functionality in imagers [1]. The upper current mirror fixes the current flowing through both branches, therefore the bottom one will provide equal currents when the respective source voltages are the same. Since, the currents are already equal, V_D and V_{DR} are matched. In the case of a pixel current in velocity saturation, the conveyor needs to accommodate a large output current at a relatively high V_D. At the same time, cascoding boosts the output impedance at the expense of reduced headroom therefore a design trade-off exists. Overall, the devices are designed with a very large aspect ratio to accommodate a pixel current of $I_{pixel} \leq 200\,\mu A$ at $V_D \leq 1.5\,V$ i.e. in velocity saturation. Post layout simulations with the devices split into common centroid layout verify this operation. Additionally, the current conveyor is used to mirror I_{pixel} to a transimpedance amplifier (TIA) for I-V conversion as well as to a pad for external sampling. Measured results and further characterisation of the current conveyor are shown in Appendix E.1.

I-V conversion is facilitated using a wide-bandwidth op-amp[3] provided by the AMS Process Design Kit. The TIA is designed to convert a $0 - 200\,\mu A$ current range to $1.6\,V$ range for sampling i.e. with a gain of $8\,k\Omega$. Subsequently, a 10-b ADC has been added to sample the converted signal in the range $V_{RP} - V_{offset}$ where V_{RP} is used to define the load of the current-conveyor and the positive reference of the ADC and V_{offset} denotes the input offset of the op-amp. This ADC is based on a successive-approximate register topology and requires 11 clock cycles per conversion. In this case, external sampling has been employed to provide sampling at a higher resolution (16-b) than the internal ADC.

[3]All the standard cell used here (Op-amp, ADC and bandgap voltage reference) are provided from the AMS 4.10 HitKit Analogue Cells library.

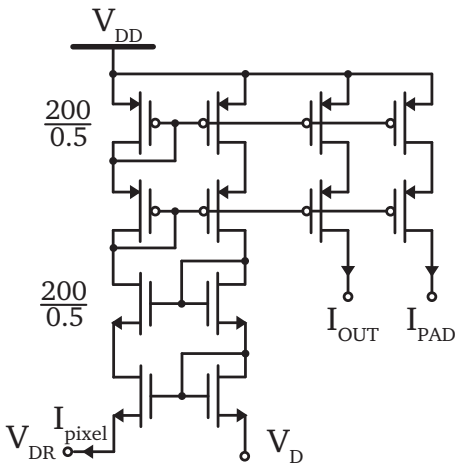


Figure 4.3: Current Conveyor topology. Sizes in $\mu m/\mu m$.

Temperature Sensor

A temperature sensor has been added on the chip in order to monitor the silicon temperature in cases such as when carrying-out DNA reactions which typically require precision temperature control. An external instrument will be used to set the temperature profile nevertheless this sensor will confirm that the chip's temperature is at the required level.

The sensor is based on a modified version of a bandgap voltage reference (provided by AMS) whose output is proportional to the absolute temperate (PTAT). A generic PTAT schematic as well as the readout circuit is shown in Fig. 4.4. Simulations of the this subsystem are shown in Fig. 4.5 including the current output for a temperature sweep as well as the final voltage V_{temp} with a final sensitivity of $14\,mV/^oC$.

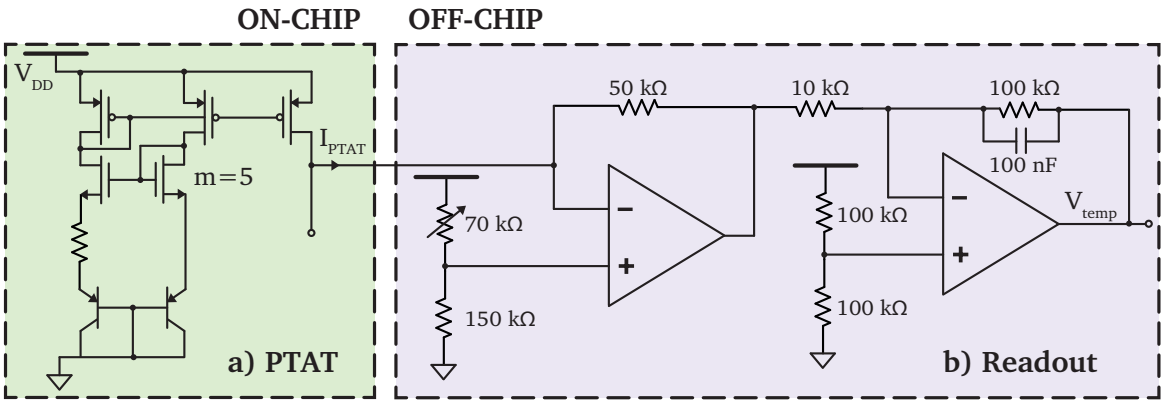
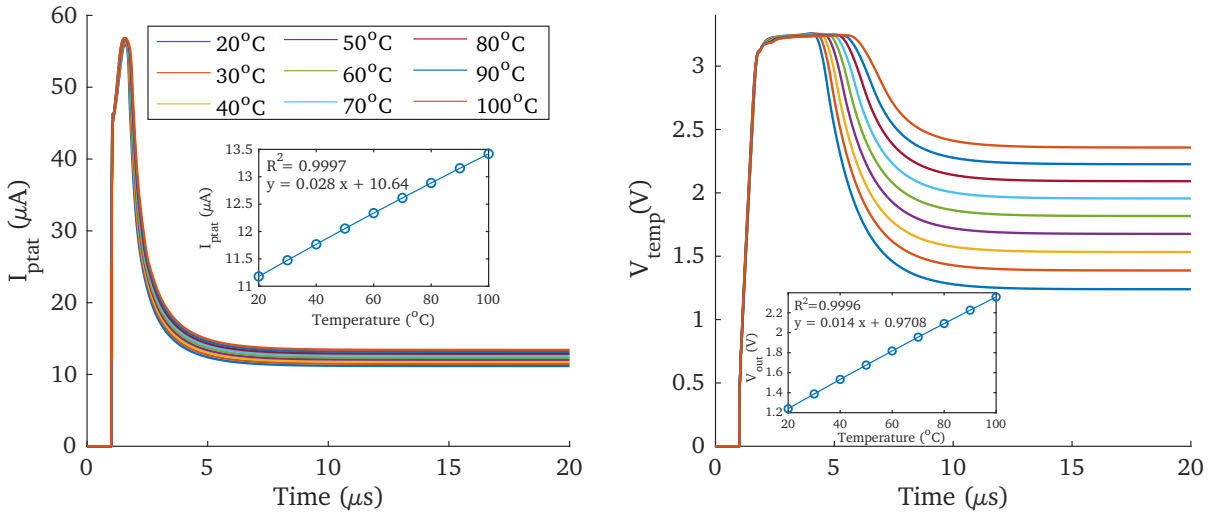


Figure 4.4: PTAT (generic schematic) and readout subsystem. The PTAT current is amplified and converted to a voltage for sampling.



(a) I_{PTAT} against temp. (b) V_{temp} against temp.

Figure 4.5: Transient simulation at different silicon temperatures. The PTAT block is reset in the first few μs of the simulation.

Voltage-Mode Pipeline

Similarly to the CM arrays, two VM sub arrays have been designed of 64×64 pixels each (shown in Fig. 4.2). The array has been split in order to reduce the maximum output bus length for the unbuffered signals. As opposed to CM, every pixel has been designed with precise pixel control i.e. only one pixel can be ON at any given time. This is the case since in VM, the output voltage (after settling) shouldn't change according to the magnitude of the series ON resistance of a transistor switch. Therefore, there is less need for peripheral circuits and all the pixel outputs are connected together. A wide-bandwith op-amp is used to buffer the selected pixel's output. Similarly to the current-mode readout pipeline, the buffered signal is available for sampling using a 10-b SAR ADC or external sampling for higher resolution readout.

4.2.3 Digital Control

A central block for on-chip digital control has been included which comprises a synthesized Finite-State Machine (FSM) from a VHDL source file and a separate 16-b Serial Peripheral Interface (SPI) communication link (from a schematic implementation). Conversion of VHDL to Verilog and digital synthesis (Verilog to gates) took place using the Cadence Encounter RTL Synthesis Compiler using the AMS HIT-Kit: Digital cell library (CORELIBD).

The digital block is operated at a clock frequency of 1 MHz, (theoretical maximum is at least an order of magnitude higher synthesized assuming a Xilinx Spartan 3 target) and carries-out three main

functionalities:

- Controls the system timing for each state and carries-out its corresponding operation e.g. cycle through an array or pixel random-access.
- Provides synchronization between the SPI block which is asynchronous (according to the SPI protocol) and a synchronous main digital core. In this case, the chip constitutes the slave of the SPI transaction whereas the external microcontroller is the master .
- Generates a synchronisation signal, called `data_available` which is used as an interrupt signal from the external microcontroller to indicate when the current pixel is available for sampling or when the ADC data are available on the SPI register.

The main functionalities are expanded below.

Finite-State Machine

The chip's operation is controlled by an FSM which allows for multiple modes of operation. Selecting an FSM state is controlled by the two most significant bits of the SPI word. An overview of the state diagram is shown in Fig. 4.6 and a summary in Table 4.1. The `Idle` state puts the chip in sleep mode where all outputs are turned-off and reset and the SPI block echoes back the incoming command for testing purposes. The `Safe` and `Safe_PG` states are used for random access of individual pixels with `Safe` allowing access on any array up to pixel $2^{12} - 1 = 4095$ whereas `Safe_PG` specifically on the CM-PG array up to pixel $12,799$. This state has been added to allow for sufficient time for the calibration signal to be applied to each CM-PG pixel individually at a later stage. The last state, `Read`, is customizable regarding the type of sampling (internal or external) and is used to automatically cycle through an array following a raster scan. Depending on the type of sampling, a programmable number of clock cycles per pixel or ADC conversions per pixel is allowed, in the range $1 - 2048$. Consequently, the `data_available` signal generates an interrupt at the last clock cycle before the next pixel is selected or at each End-of-Conversion of the ADC to request an SPI read. The FSM implementation in VHDL is shown in Appendix I.

Table 4.1: FSM States

State	SPI[15:14]	Functionality
`Idle`	00	All outputs disabled and all pixels off
`Safe_PG`	01	Select any pixel (14b address) from CM-PG array
`Read_frame`	10	Cycle any array automatically with or w/o sampling using the internal ADC
`Safe`	11	Select any pixel (using a 12b address) on any array

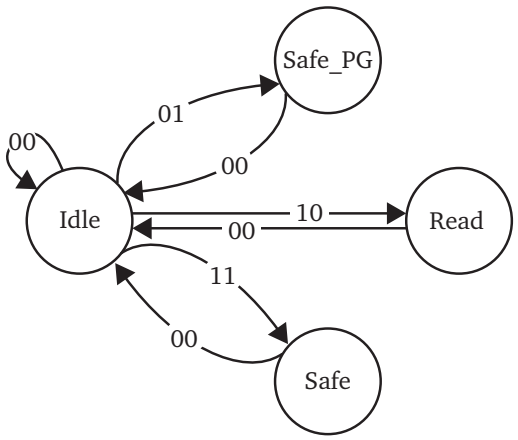


Figure 4.6: FSM with the state transitions driven by the 2 MSBs of the SPI instruction.

SPI Communication

The SPI protocol provides a simple and time-efficient method of exchanging the contents of two registers on the master and slave devices. Data on a 16-b shift register is transferred serially using four signals and is initiated by the master device (microcontroller).

- `SCLK`: SPI clock enabled only to facilitate a transaction. Target at 10 MHz.
- `CS`: Chip Select which is used to select the target slave device.
- `MOSI`: Master Output Slave Input which corresponds to the 16-b data sent from the master to the slave.
- `MISO`: Master Input Slave Output which corresponds to the 16-b data sent from the slave to the master.

The incoming SPI instructions are defined in a custom-written protocol which includes 4 selection bits for the target array and state of operation, a single bit selecting on-chip or off-chip sampling while the rest providing a state-depended command to the FSM. In-detail breakdown of the communication encoding is shown in Table 4.2.

4.3 Testing Setup for Wet Measurements

4.3.1 Encapsulation & Microfluidics

After the chip is fabricated, it is encapsulated and prepared for wet experiments i.e. by bringing the top surface in contact with a solution while ensuring that the bondpads, sides of the chip and any pad openings are protected.

Table 4.2: 16b SPI custom encoding protocol

Encoding breakdown

Bit Position:	15	14	13	12	11	10									0
SPI Word:	S	S	A/X	A/X	C/X	X	X	X	X	X	X	X	X	X	X
	FSM State		Array Address		Samp.	Command									

Array Address (AA)

SPI[13:12]	Array
00	CM
01	CM-PG
10	VM-left
11	VM-right

Internal Sampling (C)

SPI[11]	State	Functionality
0	`Read_frame`	On-chip ADC disabled
1	`Read_frame`	On-chip ADC enabled
X	`Safe`	In address of array AA
X	`Safe_PG`	In address of CM-PG

Command (XXXXXXXXXXXXX)

State	SPI[13:0]	Functionality
`Read_frame` AND `C=0`	AACXXXXXXXXXXX	SPI[10:0] is # of clock cycles per pixel for array AA
`Read_frame` AND `C=1`	AACXXXXXXXXXXX	SPI[10:0] is # of ADC conversions per pixel for array AA
`Safe`	AAXXXXXXXXXXXX	SPI[11:0] is the pixel coordinate for array AA
`Safe_PG`	XXXXXXXXXXXXX	SPI[13:0] is the pixel coordinate for CM PG array

A custom cartridge 65×50 cm PCB (shown in Fig. 4.7a) is used to host the chip which is glued on a ground plane (gold). Subsequently, electrically insulating epoxy (EPO-TEK T7139) is used to cover the bond pads and serve as glob top encapsulant. Depending on the microfluidic manifold used, encapsulation can cover the bottom part of the chip (pads + bondpads) or all around as shown in Fig. F.1. Encapsulation was carried-out manually, using a needle or similar object, to spread the epoxy at the sides of the chip while aiming to keep all arrays exposed.

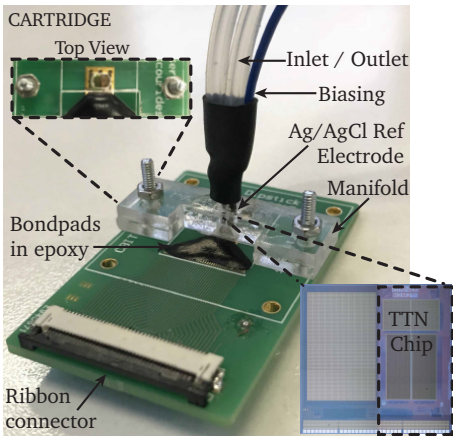
In order to insert various solutions while keeping a continuous flow, such as for pH characterisation, a custom microfluidic manifold has been designed which forms a reaction chamber of 2.8 mm × 2.2 mm and brings the top surface of the chip in contact with a solution as shown on Fig. 4.7b. This chamber allows for $\sim 300\mu m$ of space on each side of the chip thus ensuring that the larger part of the arrays are exposed. The manifold is formed from two layers of acrylic sheet that have been laser cut and are screwed down on the cartridge PCB. Additionally, double sided bio-compatible adhesive tape has been added around the microfluidic chamber that is in contact with the chip to ease the stress from screwing and prevent leakage.

With this approach, a very small chamber is created to ensure that during continuous fluid flow the new solution will completely displace the previous one from the chamber with minimum residue. In the case of solution flow from an inlet point far from the chip, there is a higher probability of the formation of a dam around the surface of the chip due to the encapsulating epoxy all around and thus subsequent solutions would be mixed instead of displaced.

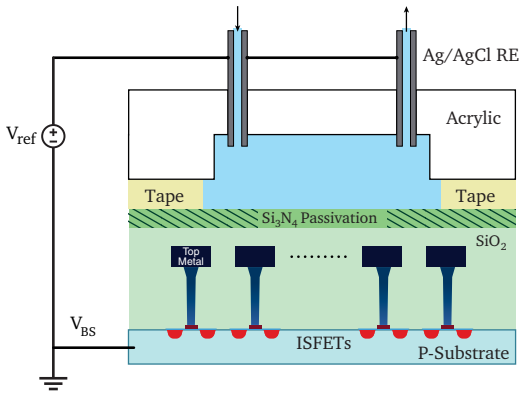
With this configuration, the inlet and outlet tubes essentially take up most of the chamber area leaving no space for a typical Ag/AgCl wire reference electrode. Instead, biasing is facilitated using silver tubes as the last stage of the inlet/outlet which had undertaken galvanostatic oxidation as proposed in [2]. Following the oxidation process, an aluminium wire was soldered on both tubes and connected to a voltage reference to be used for biasing. Two silver tubes of outside diameter 1mm and wall thickness 0.175mm were used and a heatshrink tube was added for protection of the tubes and prevention of any other material getting in touch with the reference.

4.3.2 Motherboard PCB

A motherboard PCB has been designed which is used to communicate with each cartridge PCB and chip. The main operations include regulating the chip power supply, providing bias voltages and hosting a microcontroller that serves as an intermediary data link between the chip and a PC. The PCB is shown in Fig. 4.8.



(a) Cartridge PCB to host, glue and encapsulate each chip. Also shown is the the microfluidics manifold which provides a solution flow on the surface of the chip. The manifold is formed by two layers of laser-cut acrylic glued together.



(b) Cross-section of the fabricated chip and the microfluidic manifold. Figure not drawn to scale.

Figure 4.7: Measurement setup for wet testing of the TTN chip. The Ag/AgCl reference electrode is facilitated by two oxidized silver tubes which also serve as the inlet/outlet of the solution.

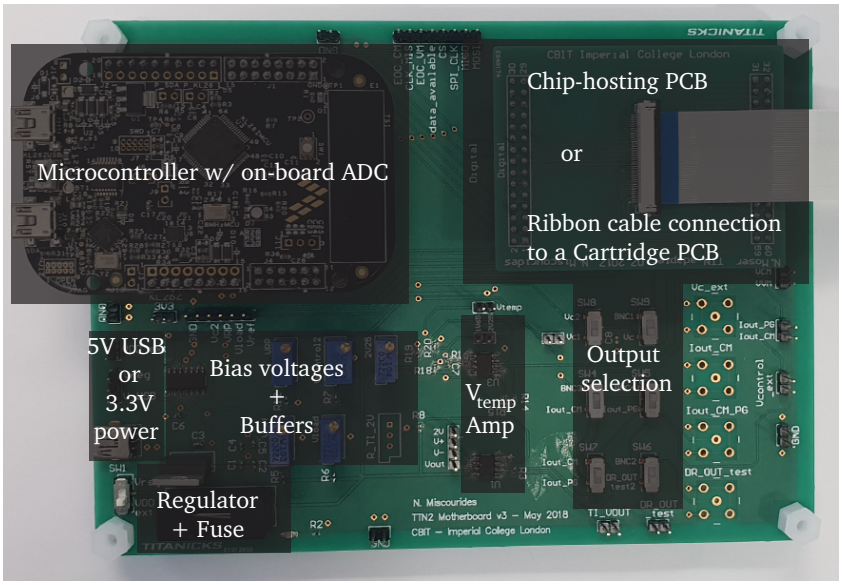


Figure 4.8: Motherboard used to power, provide biasing voltages and host the microcontroller to communicate with the chip.

4.4 Current-Mode Characterisation

This section outlines the characterisation of the current-mode array and is compared to the simulated responses in Chapter 2. In the end, all metrics used are combined in an FoM that captures the overall performance of the array.

Unless otherwise specified, measurements were taken at a solution of constant pH (typically 7) or in de-ionized water.

4.4.1 Pixel Characteristics and Attenuation

The input-output characteristics of the CM pixel were determined through sweeping the reference electrode biasing the solution. Fig. 4.9 shows a typical response obtained. It is described by a scaling and a shift term compared to the simulated response using MOSFETs. These deviations occur due to expected ISFET non-idealities. Specifically, the scaling effect is the result of the capacitive attenuation due to C_{pass} as modelled in Eq. 3.9 whereas the shift term occurs due to trapped charge. In order to quantify these effects experimentally, a modelled is developed such that the experimentally obtained response X_{exp} occurs as a linear transform of the simulated response X_{sim} such that:

$$X_{sim} = \alpha \times X_{exp} + \beta \tag{4.1}$$

where α describes the scaling term due to the capacitive attenuation and β describes the shift due to trapped charge. An algorithm to fit the I-V responses and determine α and β has been developed and is outlined in Appendix C.

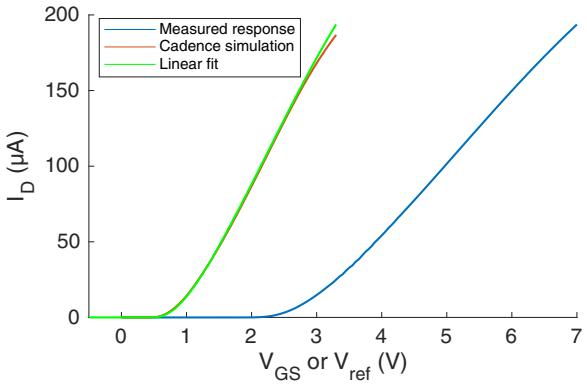


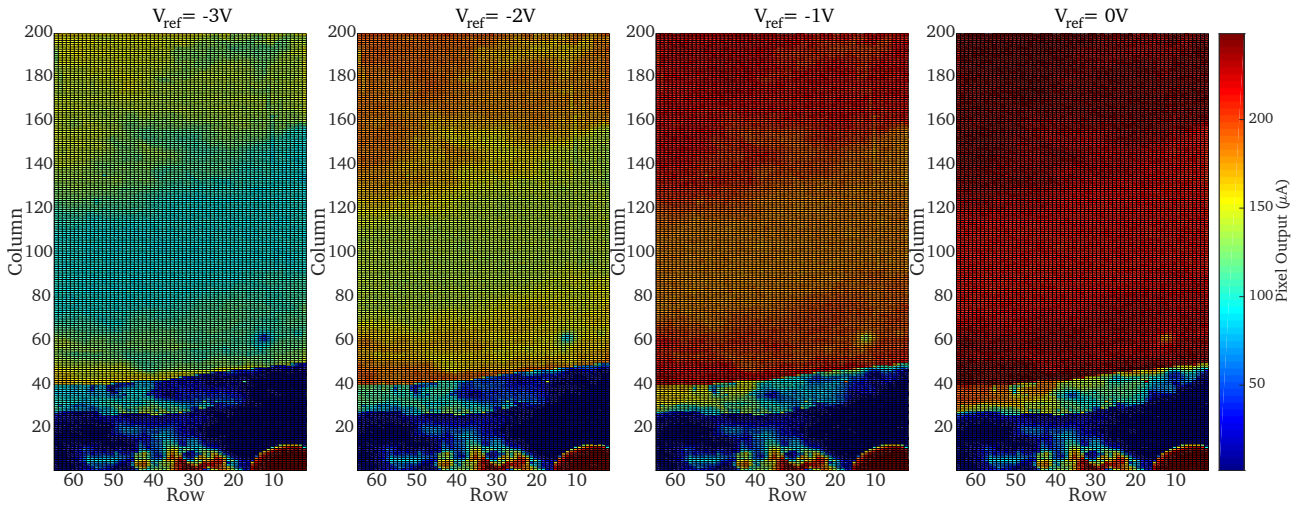
Figure 4.9: CM Pixel Response at $V_D = 1.5\,V$.

Fig. 4.9 shows the simulated, experimentally obtained and fitted responses of a CM pixel with a very large amount of trapped charge evident from the large shift in the response. The obtained response

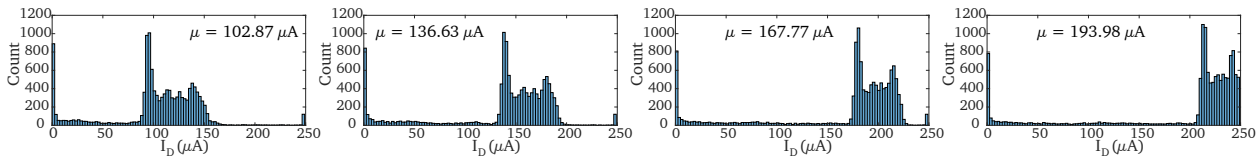
(rightmost curve) was obtained by sweeping V_{ref} and monitoring the current conveyor output current I_{CC} which mirrors the ISFET drain current. After fitting to the $I_D - V_{GS}$ response, experimentally measured values for α and β were obtained with typical values shown in Table 4.3. Specifically, the experimentally derived attenuation has been measured as $\alpha = 0.57$ which is similar to the simulated result for the CM pixel of 0.59 described in Section 3.2.5.

4.4.2 Trapped Charge

To illustrate the trapped charge spread, Fig,. 4.10 shows the array output at different points of the reference electrode potential. The bottom part of the array is covered by the microfluidics manifold and shows no response to the sweep. The remaining pixels lie approximately within a 60 μA current range which shifts according to the DC point of the reference electrode. With this spread, all active pixels can be biased in velocity saturation and reside within the perfectly linear range. In this case, with all non-active pixels caused by encapsulation and no extreme trapped charge cases, the sensing area corresponds to 9984 pixels or 78%.



(a) Recorded frames



(b) Histograms

Figure 4.10: Reference voltage step in a solution pH 7 showing the trapped charge spread across the array. The bottom part is covered by the microfluidic manifold and shows no sensitivity to reference voltage when the solution is not in contact.

4.4.3 Drift

To get an idea of the sensor drift, a new die is exposed to a solution of pH 7 and is monitored for 100 minutes. The output of all pixels is shown in Fig. 4.11 with the average drift rate throughout the time course of this recording being 0.6874 $\mu A/min$.

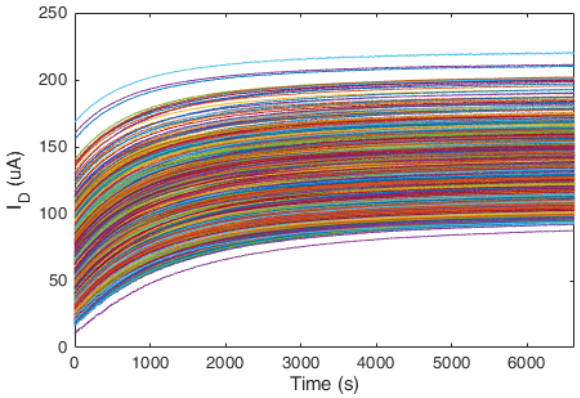


Figure 4.11: Output drift for all pixels at a constant V_{ref}.

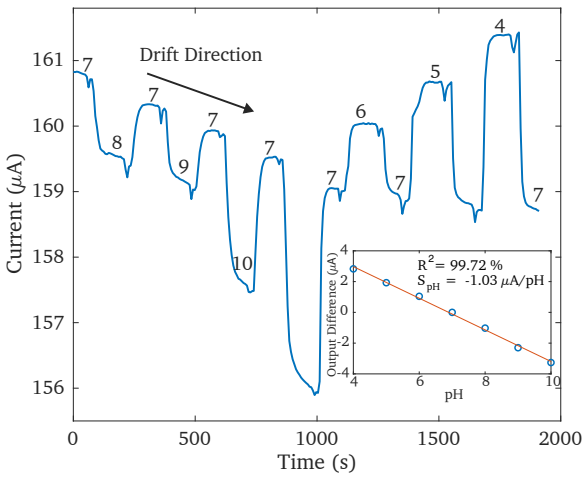
4.4.4 pH Sensitivity

The pH sensitivity for all pixels has been obtained using in-house prepared pH buffers in a range $4-10$. To prepare the buffers, de-ionized water, KCl 3M (Sigma Aldrich 60137) and Tricine 1M (Sigma Aldrich T0377) were mixed to prepare the main buffer solution whose pH was increased or decreased using 1M NaOH (SigmaAldrich 71463) or 1M HCl (SigmaAldrich 318949) respectively. Subsequently, a peristaltic pump was used to pump each buffer through the microfluidic arrangement with momentary interruptions in the flow to switch the solution. In between measurements, pH 7 was inserted in order to record the step differences in pH in the presence of drift.

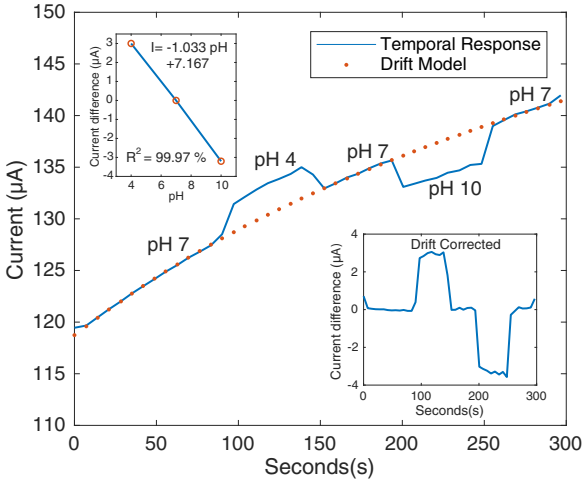
The first pH variation experiment was carried out on two different chips to verify the silicon nitride response. In Chip 1, a pH variation of 4-10 was carried out with a step of 1 pH whereas on Chip 2 the same process was applied with a step of 3 pH. The graphs show the temporal output obtained from the mean of the active CM pixels operating in the linear range. Furthermore, the insets show the drift corrected response (if applicable) and the resulting pH sensitivity in μA/pH.

In the cases where drift was affecting the results, an exponential fit was applied at the regions of pH 7 in order to obtain a compensated response. The observed drift is not related to the sensor configuration, rather on other parameters such as the specific biasing conditions and chip conditioning time. As such, the drift-compensated responses were considered for the comparison measurements.

Subsequently, the Si_3N_4 layer pH sensitivity was derived by dividing the obtained pH sensitivities by the attenuation calculated earlier. The sensitivity of the passivation layer was evaluated at 18.3 mV/pH.

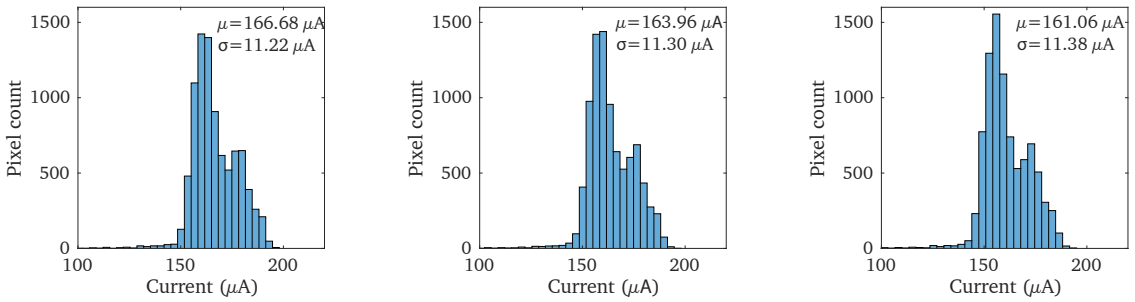


(a) Chip 1 pH variation experiment in a range of $4-10$ pH units with a step of ± 1, showing the mean output of the CM array with no drift correction. The insets show the resulting response and the overal pH sensitivity of the CM pixels.



(b) Chip 2 pH variation experiment in a range of $4-10$ pH units with a step of ± 3, showing the mean output of the CM array. The insets show the resulting response after calibrating for drift (exponential model fit shown by the dotted line) and the overal pH sensitivity of the CM pixels.

Figure 4.12: CM array pH Sensitivity



(a) pH = 4 (b) pH = 7 (c) pH = 10

Figure 4.13: Mean current change for Chip 1 for a pH step of 4, 7 and 10, also showing the trapped charge spread.

4.4.5 Speed

Typically, the maximum readout speed for an imager configuration is dictated by the pixel settling time, assuming a faster readout pipeline, which is measured by applying a step or square signal. However, in the case of ISFETs, applying a high frequency and amplitude input signal at the floating gate is not trivial since the signal will be applied through the reference electrode (with an equivalent RC model) to a large load comprising the series resistance of the solution and the double-layer chemical capacitance of several pF. In order to stay within the current driving limits of the programmable voltage source

supply used to bias the reference electrode, an alternative method has been employed here.

Specifically, in order to demonstrate the worst case settling time of a pixel configuration, a very fast raster scan through the array is carried-out (clocked at 1 cycle per pixel = $1\,\mu s$ per pixel) and the settling time of the output switching between two consecutive pixels with a large trapped charge difference is recorded. As a result, the worst case output for that specific array is obtained since it corresponds to the pixel pair with the most sudden shift in output. Even though this test has been included for characterization, such a change is unlikely to occur at the input of the sensors due the nature and magnitude of the chemical capacitances. Instead it is provided here as a metric for settling time and maximum possible array scan rates.

To record in a sampling rate that can capture the worst case settling time, an oscilloscope (LeCroy WaveSurfer 434, 2GS/s, 350 MHz) is used to record up to $100\,\mu s$ segments from the array raster scan. A representative example is shown from the CM array which should indicate the settling time of ISFETs operating in velocity saturation. The system master clock is included as well for synchronization and to illustrate the transition to the next pixel since the scan operation is designed to increase the pixel address at a clock rising edge. In addition, the op-amps used as TIAs for the CM pixels and buffering the VM signals are designed for a wide bandwidth with typical settling times of $70\,ns$ rising and $40\,ns$ falling. All traces shown were recorded at $1\,GS/s$.

Fig. 4.14 (a) shows a region of the CM-PG array scan biased at a reference voltage whereas Fig. 4.14 (b) shows the clock signal and Fig. 4.14 (c) shows the superimposed traces illustrating the worst case output difference. The corresponding worst case settling time is $243\,ns$ for a decreasing output. The same test applied to the CM array resulted in a worst case settling time of $216\,ns$ with both results shown in Table 4.3.

4.4.6 Noise

The noise of this architecture, including both the chemical and electrical contributions, was captured using an external high precision data acquisition unit (PowerLab 8/35, ADInstruments). This DAQ was used to sample a random pixel at a constant V_{ref} at the final stage of the readout pipeline before sampling which corresponds to the output of the TIA in the case of the CM array. Therefore, a voltage output was sampled with special care taken to ensure that is was approximately at the same starting DC level for all pixels sampled ($1.5 - 1.6\,V$). Time-domain signals were captured for 10 minutes at a sampling frequency $f_s = 20\,kHz$, with 16-bit accuracy across a $\pm$ 2V maximum input signal range i.e. 62.5 μV resolution. The test DAQ has an input impedance of $1M\,\Omega\,||\,100\,pF$ and all signals recorded

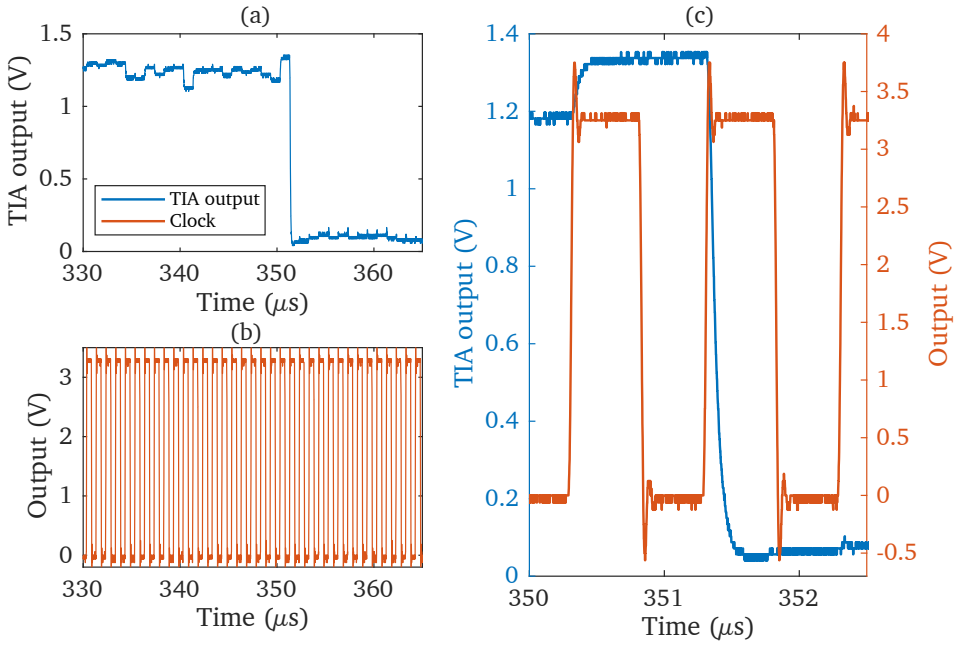


Figure 4.14: Determination of worst case settling time for a CM pixel showing (a) excerpt from the CM array scan at the point of the largest DC transition (b) master clock signal and (c) superimposed clock and array output with the settling time measured at the high-to-low transition.

were filtered using a $25\,kHz$ low-pass filter.

Subsequently, the input-referred noise (IRN) was obtained by dividing with any gain along the readout pipeline, that is between the input (reference electrode) and sampling points assuming that the current conveyor has a current gain of 1. Specifically, for a CM pixel the input referred power spectral density (PSD), S_{CM,V_n}, is obtained by:

$$S_{CM,V_{FG}} = \frac{S_I}{g_m^2} = \frac{S_V}{R_f^2} \times \frac{1}{g_m^2} \times \frac{1}{\alpha_{CM}^2} \tag{4.2}$$

where S_V represents the output PSD in $\frac{V^2}{Hz}$ at the TIA output and S_I represents the current PSD at the TIA input in $\frac{A^2}{Hz}$. A detailed explanation on current noise in TIAs is found in [3]. Additionally, R_f represents the gain of the TIA amplifier, g_m corresponds to the transconductance of the device at the specific DC biasing condition during sampling and α_{CM} represents the attenuation of a CM pixel shown in Table 4.3. The current conveyor has been assumed to have a gain of unity through the current mirror topology. Nevertheless, this assumption is not valid if the power gain was considered.

For comparison, the resulting input-referred PSD (in $\frac{V}{\sqrt{Hz}}$) for all pixels types is shown in Fig. 4.15. Regarding the electrical performance only, the introduction of the current conveyor in the CM pipeline adds an additional noise-contributing block compared to VM. In fact, the current conveyor contributes more noise than any single pixel owing to the cascoded topology which on one hand boosts the output impedance yet on the other introduces additional thermal noise through the drain-source resistances.

Since the current is copied to the output through the current mirror topology, noise is effectively doubled.

In all cases however, the noise response is dominated by the chemical noise which has been shown to increase electrical noise by at least one order of magnitude compared to MOSFETs [4]. Furthermore, at very low frequencies noise is dominated by the chemical drift which masks the intrinsic flicker noise of the sensing devices. In this case, the sensing surface was allowed to settle in de-ionized water and constant V_{ref} for two hours before measurements were obtained to allow sufficient time for drift to reach the flat region of its exponential response [5]. Sensors exhibiting drift of less than 0.5 mV/min were considered for measurements with $V_{ref} = 0V$. To illustrate the effect of drift on the overall noise PSD, Fig. 4.16 shows three sensors from the same array (CM-PG) exhibiting various drift rates at the same V_{ref} due to different trapped charge causing different rates of modification of the surface layer. Evidently, the low frequency components of the PSD reflect the observed difference in sensor drift.

Since, typical applications of ISFET-based chemical sensing include monitoring of low frequency reactions [6, 7], the spot IRN at $10\,Hz$ is shown in Table 4.3 as well as the integrated noise in a $10^{-1} - 10^{4} Hz$ bandwidth.[4] Overall, the VM topology contributes the least noise with CM as a close second. Since the VM ISFET has the largest gate area it will intrinsically contribute the least flicker noise however this is counteracted by the attenuation factor α_{VM} which is slightly worse than α_{CM}. As a result, the difference between CM and VM is reduced but VM is still beneficial in terms of noise. On the other hand, the noise of the CM-PG topology is significantly higher due to increase in attenuation (α_{CM-PG}) leading to higher IRN as well as the additional capacitance and MOSFET switches connected to the gate.

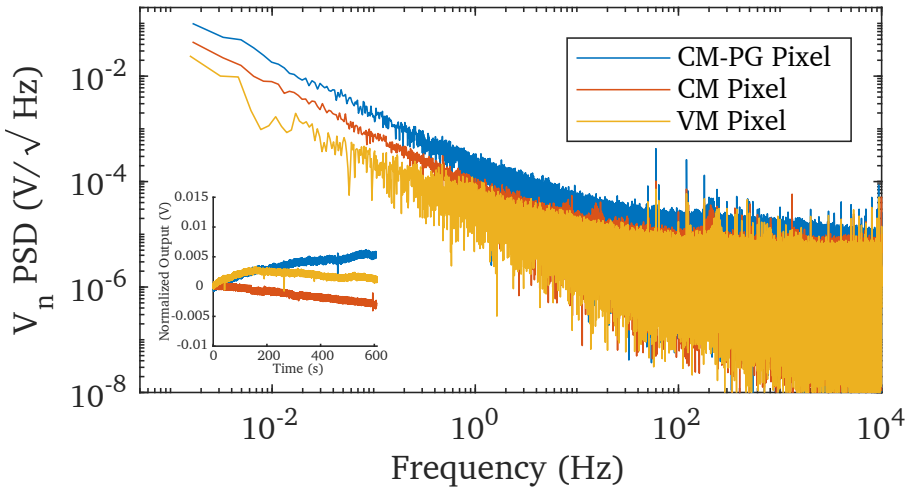


Figure 4.15: Noise power spectral density of each pixel topology referred to the ISFET's input. The inset shows the corresponding time-domain signals.

[4]The op-amp used as a TIA and buffer contributes $0.613\,\mu V/\sqrt{Hz}$ @ $10\,Hz$.

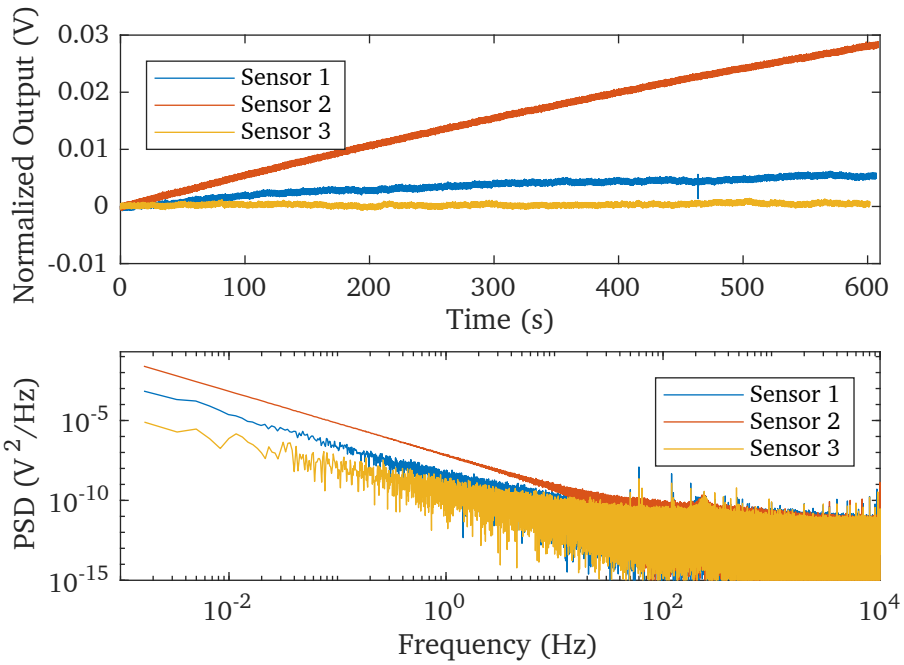


Figure 4.16: Output noise PSD of three sensors of the same topology exhibiting different drift rates which is evident in the low frequency ($< 10\,Hz$) region.

4.5 CM-PG Characterisation

This section adopts a similar methodology to characterise the CM-PG pixel and array. In the cases of trapped charge, drift, settling time and noise, the responses are equivalent to that of CM or have already been presented and thus have been omitted from this section. Instead, the expected differences with regard the pixel attenuation and pH sensitivity.

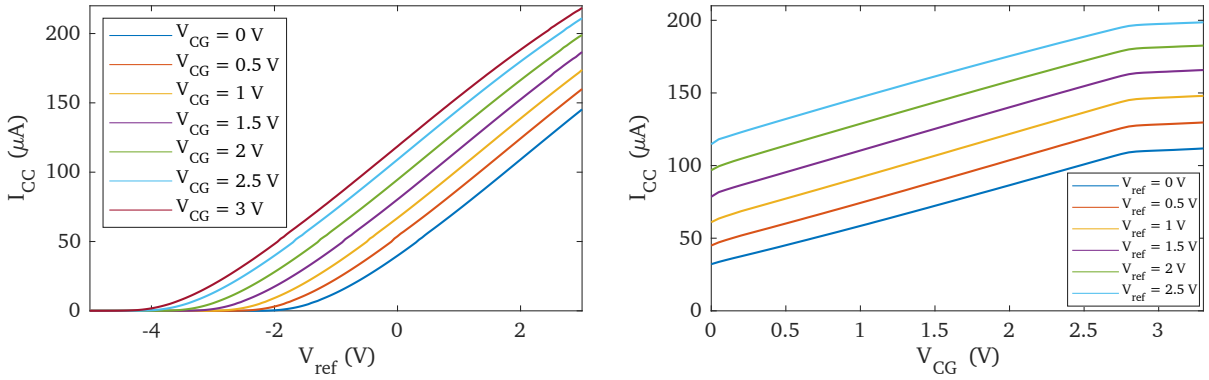
4.5.1 Pixel Characteristics

The programmable-gate contribution and effect on the CM-PG pixel response is shown in Figs. 4.17a and 4.17b. Specifically, Fig. 4.17a shows the $I_{CC} - V_{ref}$ response with fixed V_{CG} similar to the CM pixel response of Fig. 4.9, whereas Fig. 4.17b shows the $I_{CC} - V_{CG}$ response with a fixed V_{ref}. The capability of C_{CG} to program the floating gate is quantified by deriving the mean sensitivity of I_D to V_{CG}:

$$S_{V_{CG}} = \frac{dI_D}{dV_{CG}} = 30.38\,\mu A/V \tag{4.3}$$

experimentally obtained from Fig.4.17b. Furthermore, the magnitude of the parasitic C_{CG} has been determined using the combination of measured $I_D - V_{ref}$ and $I_D - V_{CG}$ sweeps to be $0.96\,fF$. The method followed for calculating C_{CG} is illustrated in Appendix C. As expected for the CM-PG, the overall attenuation has increased compared to CM, due to the introduction of C_{CG} and has been

determined in the same way as the CM pixel. The experimentally measured attenuation obtained was 0.37 whereas the simulated value was estimated at 0.38 assuming the C_{CG} value derived above.



(a) CM-PG Pixel Response with linear V_{CG} steps at $V_D = 1.5\,V$.

(b) CM-PG Pixel Response when sweeping V_{CG} and $V_D = 1.5\,V$. Average sensitivity of I_D to V_{CG} is $S_{V_{CG}} = 30.38\,\mu A/V$.

Figure 4.17: CM-PG Pixel Response at $V_D = 1.5\,V$.

4.5.2 pH Sensitivity

The pH sensitivity has been determined following the same method as in CM. As expected, the CM-PG pixel shows decreased pH sensitivity due to the added attenuation of introducing C_{CG} at the gate. The response is shown in Fig.4.18 and the measured sensitivity is -0.717 μA/pH.

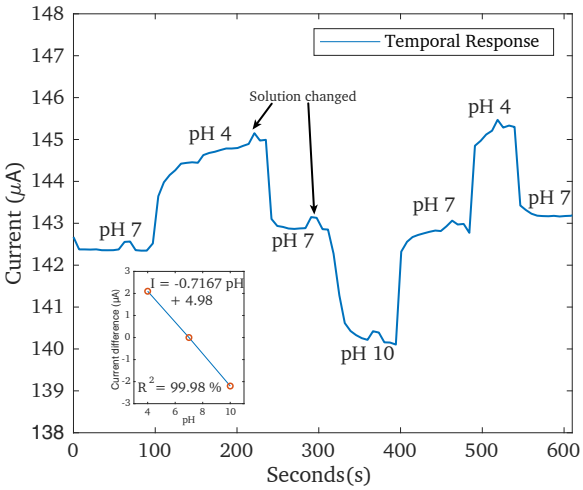


Figure 4.18: Chip 2 pH variation experiment in a range of $4 - 10$ pH units with a step of ± 3, showing the mean output of the CM-PG array. The inset shows the pH sensitivity obtained for the CM-PG pixels.

4.5.3 Noise

The input-referred PSD of a CM-PG pixel is obtained by replacing α_{CM} with α_{CM-PG} as shown in Eq. 4.4. Both values are shown in Table 4.3 and the CM-PG input-referred PSD is shown in Fig. 4.15.

$$S_{CM,V_{FG}} = \frac{S_I}{g_m^2} = \frac{S_V}{R_f^2} \times \frac{1}{g_m^2} \times \frac{1}{\alpha_{CM-PG}^2} \tag{4.4}$$

4.6 Voltage-Mode Characterisation

To complete the pixel comparison, this section outlines the characterisation of the VM pixel and array.

4.6.1 Pixel Characteristics

To characterize the VM pixel, a similar methodology as above is assumed even though the output is a voltage instead of a current. As shown in Fig. 4.19, V_{OUT} is linear with respect to V_{ref} as long as the device operates in saturation. The attenuation of this pixel has been experimentally measured as 0.48 and has been simulated using Eq. 3.17 to be 0.44 where $G_{SF} = 0.85$ verified through simulation. Note that despite the larger size of the pixel which increases C_{pass} and reduces the attenuation, the final attenuation value is similar or less to that of the CM pixel due to the larger ISFET device with larger associated parasitic capacitances (C_{gg}).

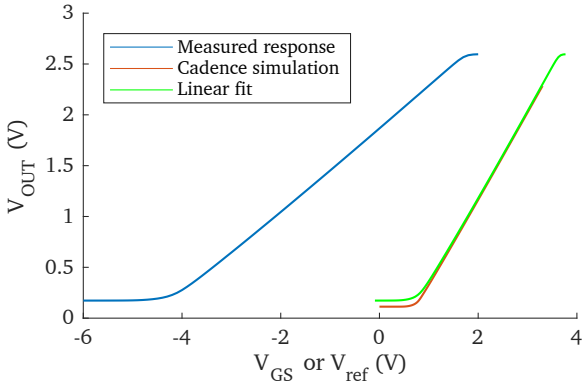


Figure 4.19: VM Pixel Response at $V_{load} = 1\,V$ and $I_{bias} = 7\,\mu A$.

4.6.2 pH Sensitivity

The pH changes in V_{out} for changes in pH is shown in Fig. 4.20. The resulting pH sensitivity has been determined as -9.23 mV/pH.

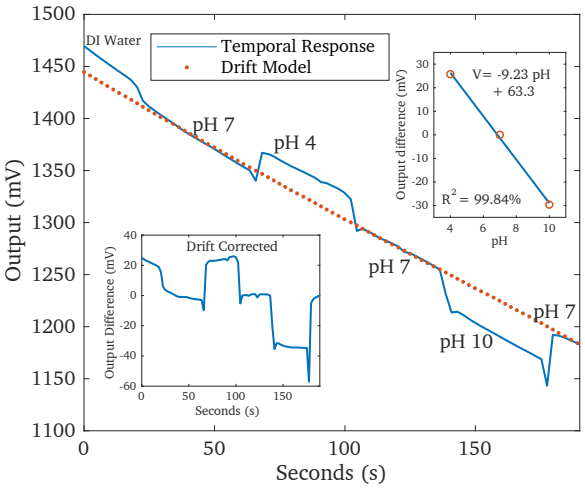


Figure 4.20: Chip 2 pH variation experiment in a range of $4-10$ pH units with a step of ± 3, showing the mean output of the VM array. The insets show the resulting response after calibrating for drift (exponential model fit shown by the dotted line) and the overall pH sensitivity of the VM pixels.

4.6.3 Trapped Charge

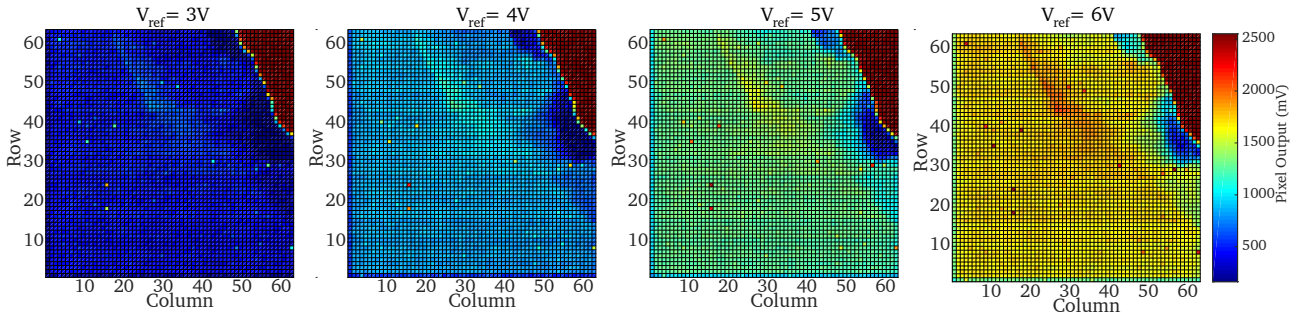
To illustrate the trapped charge spread, Fig,. 4.21 shows the array output at different points of the reference electrode potential. In this case, the rightmost 64×64 VM array is shown, with its top right corner covered by the encapsulating epoxy. The remaining pixels lie approximately within a 300 mV output voltage range which is shown to shift according to the DC point of the reference electrode. As a result, almost all the remaining pixels can be biased in the linear range of the instrumentation. In this case, active pixels correspond to the ones that are not covered by the encapsulation as well as the ones that are within 500 mV and 2000 mV at a suitable V_{ref}. In this case with $V_{ref} = 5V$, 91.9% of pixels are considered active and therefore convert changes in pH linearly.

4.6.4 Drift

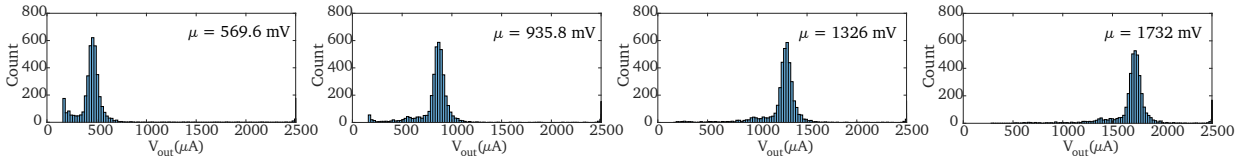
With a new chip exposed to a solution of pH 7, the time domain responses for approximately 100 mins is shown in Fig. 4.22. The average drift rate through the time course of this recording was -1.61 mV/min.

4.6.5 Speed

The speed and settling time of the VM array is determined in the same method as that of the CM array. Parameters influencing the worst case settling time are the operating V_{load} and thus I_{bias} point. Evidently, the voltage mode pixels designed here are slower than the CM which is a consequence of the lower pixel biasing current. Inherently, a faster settling time is expected for a pixel with biasing in



(a) Recorded frames



(b) Histograms

Figure 4.21: Reference voltage step in a solution showing the trapped charge spread across the VM (right) array and the corresponding change for V_{ref} variations. The top right of the array is covered by the encapsulating epoxy.

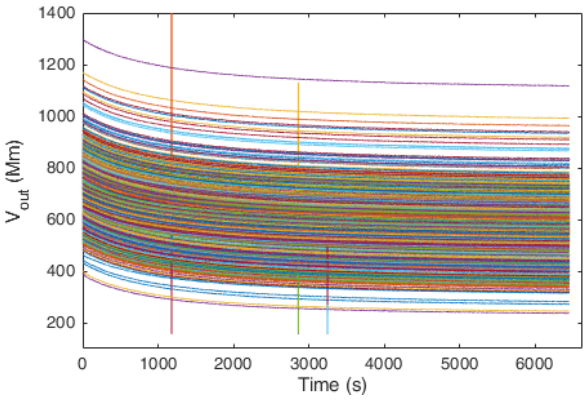


Figure 4.22: Output drift for all pixels at a constant V_{ref}.

velocity saturation as opposed to saturation which is reflected in the results obtained. However, the designs for all arrays presented here were not optimized for speed and very fast voltage mode pixels with ns settling times are certainly possible. Instead, what is illustrated here is the difference in speed for ISFET pixels optimized for chemical sensing in both modes of operation.

Fig. 4.23 shows a scan through the VM array capturing the transient across two pixels with very large trapped charge difference. Compared to CM, the array scanning speed has been decreased to $5\,\mu s$ per pixel (5 clock cycles) in order to allow sufficient settling time for this type of pixels. The worst case recorded is shown in Fig. 4.23 (c) which corresponds to $3.2\,\mu s$ for a decreasing output, determined by the discharge current through the load transistor.

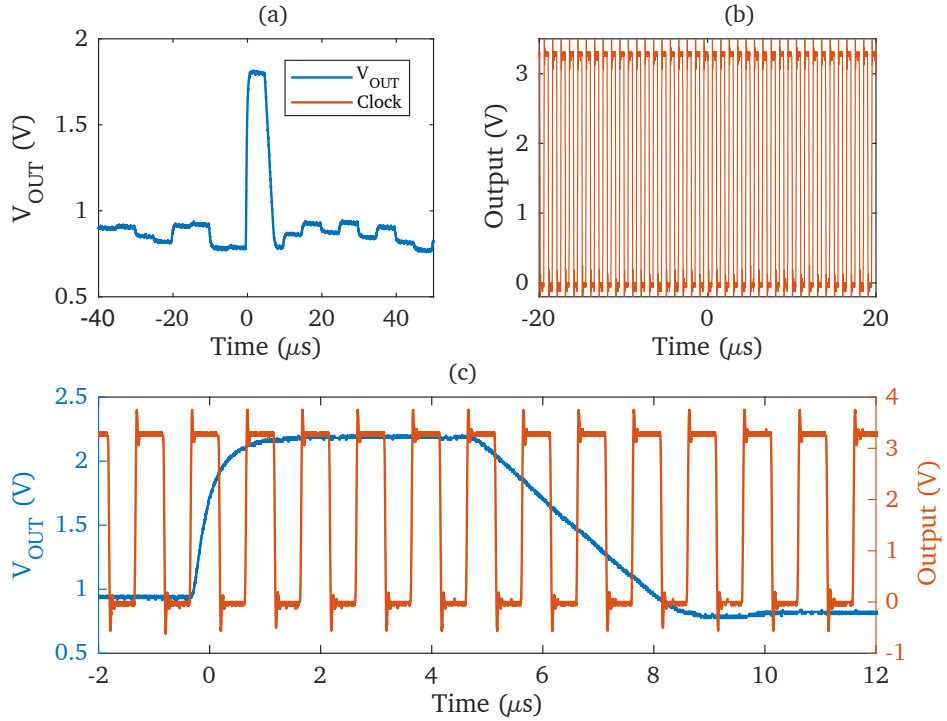


Figure 4.23: Determination of worst case settling time for a VM pixel showing (a) excerpt from the VM array scan at a point of a pixel with large offset (b) master clock signal and (c) superimposed clock and array output with the settling time measured at the high-to-low transition.

4.6.6 Noise

The output noise of a VM pixel was recorded using a similar method and same DAQ as the previous. The recording point in this case was the output of the buffer in the VM pipeline. In this case, the input referred PSD for the voltage mode pixels, S_{VM,V_n}, is given by:

$$S_{VM,V_{FG}} = \frac{S_V}{\alpha_{VM}^2} \tag{4.5}$$

where S_V represents the PSD at the output of the buffer and α_{VM} represents the VM attenuation shown in Table 4.3.

4.7 Comparison and Discussion

The previous sections provided an in-detail analysis and comparison of the pixels presented using various performance metrics. In order to summarize the results, Table 4.3 shows quantitatively the pixel comparison metrics whereas the remaining of this section provides qualitative discussion on the key points for ISFET design.

Linearity and Linear Range

The linearity of each pixel response has been quantified by using the coefficient of determination R^2 for the valid output range of each pixel's response. For the two current-mode pixels, the valid output region spans $80 - 180\,\mu A$ where the g_m in velocity saturation is approximately flat whereas for the VM pixel the output range is set by the onset of the ISFET entering saturation until $V_{DD} - V_{GS} \approx 2.5\,V$. As shown, in Table 4.3 all responses are almost perfectly linear in their target input ranges. The CM topology is considered to have a larger linear range if the equivalent linear V_{GS} ranges are considered.

Pixel Size & Attenuation

The CM topology provides a smaller pixel and more scalable design as a result of the target biasing region and requirement for a short-channel device which ensures small parasitic capacitances. Specifically, the impact of having a small C_{pass} due to the small pixel size is counteracted by C_{gg} being of low magnitude for a small device resulting into a *better* attenuation factor than the VM which has a larger C_{pass} but larger intrinsic parasitics.

Speed and power consumption

Both are inter-dependent and are determined by the selected design and I_{bias}. For the CM pixels, a linear VS current is required whereas for a source follower the device can be sized to sink much less current while still in saturation. Therefore, there is an order of magnitude difference in I_{bias} between CM and VM. Nevertheless only one pixel is active during normal operation so the array power consumption is equal to that of a single pixel.

Noise

Dominated by the low frequency chemical noise which is caused by chemical phenomena at the Si_3N_4-electrolyte interface. The effect of drift is evident on the low frequency region of the PSD which masks the noise of electronics. Nevertheless, after recording with similar drift rates across topologies, the VM approach was exhibiting the least noise in the bandwidth of interest due to the ISFET device being larger and exhibiting less flicker noise. Additionally, the current conveyor has been identified as the most noise contributing block in the instrumentation pipeline.

Programmability

The CM-PG topology allows for floating gate programmability at the expense of more attenuation. To quantify this trade-off, the Normalized Input Range (NIR) is defined to show the increase in input range available due to the programmable gate.

$$NIR = 1 + \frac{\text{Added range}}{\text{Input range}} \tag{4.6}$$

In the CM-PG topology, the programmable gate capacitor causes approximately $30\,\mu A/V$ change which significantly increases the linear current range of the ISFET ($80 - 180\,\mu A$). Assuming a $2.8\,V$ linear V_{CG} range as shown in Fig. 4.17b and using the value of $S_{V_{CG}}$, NIR evaluates to 1.85.

FoM

In an attempt to capture the complete pixel performance, a Figure of Merit (FoM) is defined that aims to represent as many of the trade-offs associated with the pixel design. Specifically, the trade-offs taken into account include the Pixel (sensing) area (WL_{chem}) versus Attenuation (α), the I_{bias} versus Speed and the Noise versus Electric area ($(WL)_{elec}$) trade-offs. Additionally, the increase in available input range (NIR) when using a PG gate is taken into account at the expense of more attenuation (α). Therefore, the FoM is defined as:

$$FoM = \left[\frac{(WL)_{chem}}{\alpha}\right] \times \frac{[I_{bias} \times t_{settle}] \times [V_n \times (WL)_{elec}]}{NIR} \tag{4.7}$$

where V_n is the integrated IRN and NIR is the normalized input range. Superior performance is indicated by lower values. As shown in Table 4.3, the CM pixel evaluates to a better FoM primarily due to its small size which is not reflected in the attenuation. The speed vs power consumption trade-off

essentially evens out between CM and VM whereas noise is slightly higher in CM yet with a smaller device. In the case of CM-PG, the increase in attenuation is partially counteracted by the increase in available input range nevertheless noise is higher due to additional components connected to the floating gate resulting into a worse FoM. In the case of VM, despite having the least noise, it evaluates to the worst FoM since the increase in pixel size is not reflected in an improvement in the attenuation which is a consequence of the additional source follower attenuation G_{SF}. It should be noted that this FoM does not take into account the amount of peripherals used to interface with each array which in the case of the CM and CM-PG arrays is higher.

4.8 Other blocks and supplementary material

Other blocks that are included in this design such as the current conveyor[5] and temperature sensor have been characterised individually and are included in Appendix E.

Furthermore, to illustrate the ion imaging capabilities of the whole sensing surface, a snapshot at constant V_{ref} is shown in Appendix F.

Lastly, a MATLAB-based graphical user interface was designed and is shown in Appendix G. The GUI is used to facilitate data visualization and serve as the master control of both the microcontroller and by extension the chip. A custom communication protocol has been defined which encodes commands in character vectors of 6 characters each and it communicated via UART to the microcontroller. Subsequently, the microcontroller decodes the commands into functions which result into a specific chip state and operation.

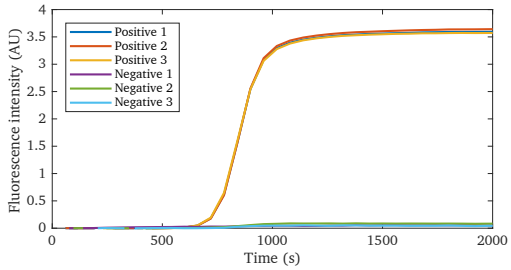
4.9 Demonstration in DNA amplification detection

To demonstrate the potential of a platform sensing in unmodified CMOS in a realistic scenario, detection of DNA amplification was performed on chip with results shown in Figs. 4.24 and 4.25. The protocol and experiment methodology are described in Chapter 7. Instead, here both types of arrays are demonstrated to accurately detect the change in pH occurring due to DNA polymerisation and amplification during a LAMP reaction. The pH change (recorded with a commercial meter) indicating a positive reaction is compared with the change observed of the average output of each array in Table 4.4.

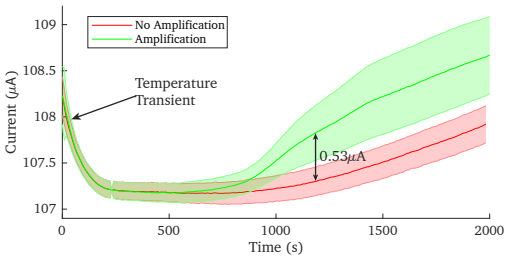
[5]A current conveyor test block has been included on a different chip, Chip 24, and is the block used for individual characterisation.

Table 4.3: System Summary and Pixel Comparison

Chip Summary			
Process	AMS C35B4 2P4M 0.35 µm CMOS		
Power Supply	3.3 V		
Silicon area	$4 \times 2\,mm^2$		
Configuration	**VM**	**CM**	**CM-PG**
Area			
Array Size	$2 \times 64 \times 64$	64×200	64×200
Array Area (mm^2)	0.565	1.06	1.06
Pixel Sensing Area (μm^2)	9.3×10.3	6.5×7.775	6.5×7.775
Passivation Effects			
C_{pass} (fF)	2.17	1.15	1.15
Attenuation (α) (Simulated)	0.44	0.59	0.38
Attenuation (α) (Measured)	0.48	0.57	0.3
Si_3N_4 Sensitivity (mV/pH)	19.2	18.0	18.7
System Description			
Topology	Source Follower	CM in VS	CM in VS with PG
Instrumentation range	$0.15 - 2.5\,V$	$20 - 200\,\mu A$	$20 - 200\,\mu A$
Linearity	$R^2 = 99.98\%$	$R^2 = 99.99\%$	$R^2 = 99.99\%$
Nominal I_{bias} (μA)	7	100	100
pH Sensitivity	-9.23 mV/pH	-1.03 µA/pH	-0.717 µA/pH
t_{settle} (μs) (worst case)	3.2 (falling edge)	0.216 (falling edge)	0.243 (falling edge)
C_{CG} (fF)	–	–	0.960
IRN @ $10^1\,Hz$ $(\mu V/\sqrt{Hz})$	9.204	13.05	29.81
IRN Integrated (mV) $(10^{-1} - 10^4 Hz)$	0.267	0.384	0.816
Normalized input range	1	1	1.85
FoM $(mV \times \mu m^4 \times \mu A \times \mu s)$	2089	147	292

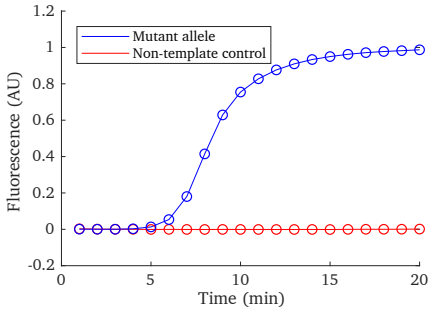


(a) Fluorescence output from positive and negative reactions conducted in the LC96 System.

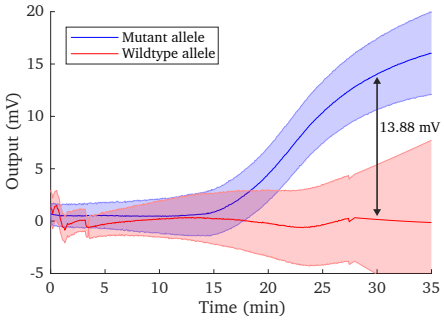


(b) Mean output of exposed pixels in VS after positive and negative pH LAMP reactions with the standard deviation indicated by the shaded bars.

Figure 4.24: Results from both positive and negative reactions for the detection of the NDM gene in *E. coli* in (a) an LC96 benchtop instrument and (b) on-chip. The CM array is used for detection.



(a) Fluorescence output from positive and negative reactions conducted in the LC96 System.



(b) Mean output of exposed pixels after positive and negative pH LAMP reactions with the standard deviation indicated by the shaded bars.

Figure 4.25: Results from positive and negative reactions for the detection of the Kelch 13 gene in the *P. falciparum* parasite that causes malaria in (a) the benchtop instrument and (b) on-chip. The target (mutant) allele is compared with the normal (wildtype). The VM array is used for detection.

Table 4.4: DNA amplification on-chip

Target	Array used	ΔpH (actual)	Signal change and equiv. pH
E. Coli	CM	0.6	$\Delta I_{out} = 0.53\,\mu A = 0.55\,\text{pH}$
Malaria	VM	1.32	$\Delta V_{out} = 13.88\,mV = 1.5\,\text{pH}$

4.10 Design considerations for CMOS ISFET arrays

This section summarizes the key factors / trade-offs that should be taken under consideration when designing ISFET sensors in CMOS based on the experience gained and the results presented here:

- **pH sensitivity** - Evidently, using ISFETs as pH sensors fabricated in an unmodified CMOS technology entails a sub-Nernstian sensitivity caused primarily by the quality of the sensing material. In this case, sensitivities of 18 mV/pH were observed. Even though the useful signal can be amplified, the reduced sensitivity still can be tolerated for applications such as DNA

amplification as described here were a relatively large pH change (>0.5 pH) is expected. In practice, CMOS ISFETs can be used in applications which benefit from monitoring changes in pH rather than the absolute value. For applications requiring high resolution, re-passivation with higher quality membranes such as Ta_2O_5 would help to reach almost ideal inherent pH sensitivity.

- **Trapped charge** - Trapped charge is essentially random and is not expected to follow a normal distribution similarly to mismatch. In an array of sensors, a certain extent of offset can be tolerated with extreme cases of charge appearing as pixel outliers. Practically, designing an array with no in-pixel compensation means that some sensors will be inactive therefore the next challenge is to maximise the input range for which offsets can be tolerated. A large power supply (as the 3.3V used here) allows for a large linear range in either current mode through biasing in velocity saturation biasing or voltage mode through biasing in normal saturation.
- **Drift** - Drift occurs due to hydration of the sensing surface which cannot be avoided when measuring ion concentrations in aqueous solutions. A superior quality insulator through post processing can decrease drift without the need for targeted solutions. In practice, drift has a very long time constant, which is reasonable since it is associated with a modification of the insulator, and for applications where pH changes are faster, signal processing methods can be used to compensate.
- **Longevity of sensors** - Two major factors were noted to affect the longevity of ISFET chips, specifically the quality of encapsulation and chip handling. For the former, the epoxy used to cover the sides and bondpads of the chip is not expected to degrade after re-use, however it is still possible for the solution to penetrate below. Freshly-prepared epoxy in large amounts should be used to maximise re-usability. Monitoring the reference electrode current is the first sign for package degradation. Regarding chip handling, it was observed that when small chambers were used, such as for pH variation, too much pressure on the manifold can induce cracks on the chip. Additionally, a high pull force when removing the manifold, which is adhesively attached on the chip, can have the same effect. Using such a manifold has the benefit of the solution never reaching the epoxy at the sides therefore the encapsulation is robust. However, maximum care should be employed when attaching/removing or even introducing ethanol in the chamber before removal which serves to reduce the tape adhesiveness.
- **Technology Selection** - In unmodified CMOS, the most typically used material for insulation is Si_3N_4 which is deposited above an encapsulating layer of SiO_2 that increases the magnitude of C_{pass}. In some cases, polyimide is also added on the surface for further protection which inhibits chemical sensing and should be avoided. In general, a single layer of thin passivation is expected

to yield better sensors regarding the capacitive coupling.

- **Sensor and Array Design** - Since ISFETs are essentially capacitively sensing, it is generally assumed that a large pixel area ensures better performance (through $\frac{C_{pass}}{C_{pass}+C_{gg}}$ approaching unity). For small pixels, such as the ones designed in this thesis, a smaller CM pixel had similar coupling efficiency with a larger VM pixel due to the difference in C_{gg}. The attenuation observed here is tolerable since the resulting signal is of the order of μA / mV, which can be amplified further if needed. For larger pixels, such as with instrumentation in-pixel, C_{pass} is much larger than C_{gg} therefore this effect is not observed, nevertheless at the expense of array resolution.

4.11 Summary

This Chapter has presented the first ISFET array in current-mode with sensors biased in the velocity saturation regime. Biasing in VS enables perfectly linear pH-to-current transduction with a high degree of linearity across a large range which increases the robustness against offsets. Furthermore, two more ISFET arrays have been presented, specifically the CM-PG array, which shows an extension of the CM array to include a programmable-gate for compensation against non-idealities at the expense of signal attenuation and the VM array which is based on a widely-used source follower topology used in imagers. Since the arrays are fabricated together, a detailed comparison is possible with no inconsistencies in the chemical characteristics. Performance metrics such as the linearity, speed, power consumption, size, attenuation and noise have been experimentally measured and a figure-of-merit has been defined to compare topologies.

Overall, the relative merits and limitations of each topology were illustrated with the CM approach resulting in the best overall performance. Nevertheless, this does not render current-mode a universal solution since typically the best designs are application-specific. Instead, given the recent trend of adopting ISFET arrays as the front-end in a chemical sensing applications such as Point-of-Care diagnostics and DNA sequencing this study is aimed to serve as a reference point for future designs and illustrate methods used to obtain standard ISFET performance metrics. Finally, design considerations have been described to improve future implementations.

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Part II

ISFET Compensation Techniques and Applications

Chapter 5

Correlation of Non-Ideal Effects in CMOS ISFETs

5.1 Introduction

It is widely known that ISFETs fabricated in CMOS processes suffer from two major non-ideal effects which limit their commercial viability and suitability for long term measurements. These effects are described as threshold voltage mismatch and threshold voltage instability, the latter commonly referred to as drift. When testing CMOS ISFETs in Chapter 4, their contribution was apparent (Fig. 4.13) and manifested as a large mismatch across pixels whose magnitude exceeded the expected due to mismatch/process variations as well as a large temporal change in a pixel's output for constant chemical input.

In a CMOS ISFET, i.e. using silicon nitride to sense pH owing to the site binding of Si_3N_4 with hydrogen ions, the quality of that layer is essential to the performance of the sensor. Even though re-passivating, etching and other post-processing methods can be used to improve the sensitivity of that material, Si_3N_4 has been shown to demonstrate sensitivities in the range $36.6 - 56\,mV/pH$ depending on the stoichiometry of the nitride layer [1–3]. Other materials, such as Ta_2O_5, have shown sensitivities much closer to the ideal Nernstian $S_N = 59\,mV/pH$ in room temperature [1].

In the case of the TTN chip, a large deviation from the expected characteristics of Si_3N_4 CMOS ISFETs has been observed with

- Measured pH sensitivity of $S_{Si_3N_4} = 18\,mV/pH$.
- High drift rate (shown in Fig. 4.13.)

- Large amount of trapped charge both in the DC value of the reference electrode as well as spread across pixels.

These parameters indicate that differences in the foundry process and/or material quality used for passivation is driving the reduction in performance. Nevertheless, the very high drift rates observed in this process allows for a closer look on the drift mechanism at the electrolyte-insulator interface.

In this Chapter, an examination into the non-ideal effects is presented which shows a correlation between drift and trapped charge. This correlation manifests as a linear empirical relationship and indicates that drift is modified by charge. To demonstrate this relationship, data from individual sensors as well as the 64×64 VM array are presented which clearly indicate this correlation. Empirical and modelled drift responses are compared and two metrics are used to quantify drift. The average drift rate of the equivalent floating gate voltage as well as the charge term (ΣQ) obtained from parameter fitting of the observed drift to the drift model. Evidently ΣQ against trapped charge shows the same trend as the average drift rate during long-term measurements which indicates their inter-dependence.

As a result, charge modulation schemes are hypothesized to influence drift in CMOS ISFETs by modifying trapped charge.[1] The relationship between threshold voltage and drift of ISFETs can be derived through the initial measurements and an optimal biasing point for drift minimization can be identified. Subsequently, charge modulation (in this case through controlled UV irradiation) can be used to modify the trapped charge and minimize drift according to the prior relationship.

Additionally, a second empirical non-linear relationship is presumed to exist; between drift and electric field across the insulator. Recordings of drift at various reference electrode voltages illustrate this dependence which goes as much as reversing the drift direction. Cycling the electric field across the insulator is shown to modify drift when the amplitude is varied and is independent of frequency i.e. dependence on the *average* electric field.

Overall, it is reasonable to believe that the combination of factors such as trapped charge, passivation capacitance modification and electric field across the insulator influence contribute to drift. This manifests as a trade-off when considering ISFETs: since a reference electrode voltage and thus electric field will be either way applied to bias the underlying device in the target operating region, some drift is expected. Nevertheless, the existence of a trapped charge value which cancels out drift is shown here which theoretically leads to ideal operation by managing to bias the device while neutralizing the local electric field across the insulator. In practice, it is challenging to precisely reach that point since charge (especially trapped charge) is not trivially modulated.

[1] Useful discussions about these phenomena with Dr Yan Liu are acknowledged and greatly appreciated.

5.2 Non-ideal effects and mathematical modelling

5.2.1 A closer look on the electrolyte-insulator interface

The interface between the insulator and electrolyte of an ISFET determines its pH sensing capabilities through a combination of the site-binding and double-layer capacitance theories. Mathematically, the V_{chem} term is introduced that describes the concentration-induced potential gradient and the potential drop at the interface between different materials [2]. Looking at the electrolyte-passivation interface, it can be roughly split into four layers: passivation, buried site layer, Helm layer and diffusion layer. The diffusion and Helm layers describe the ion distribution from the bulk electrolyte to the insulator surface and have been described in Chapter 2. Instead here the focus is on the buried sites which is generally believed to be the primary reason for the non-ideal behaviour. The location of buried sites in the structure is shown in Fig. 5.1.

Origin of drift

In [4], it was first suggested that buried sites of silanol (Si-OH) composition within a SiO_2 sensing layer (either due to oxidation or exposure to water) could be the cause of drift. Silicon nitride is also known to undergo a similar process even though it is expected to exhibit a higher resistance to hydration compared to the oxide [5, 6]. In fact, the presence of an oxygen-rich region on Si_3N_4 following a 14hr ageing period in water had already been confirmed by Auger electron spectroscopy at a depth of at least a few atomic layers [6]. Other sensing materials such as Al_2O_3 and Ta_2O_5 are expected to behave similarly even though at much lower modification rates [7]. Later, [8] suggested an empirical model of the pH response of Si_3N_4 due to the presence of buried sites and surface oxidation of the nitride. Charge was assumed to diffuse in the material during a pH change which would lead to a slow and pH-dependent response. A constant diffusion length was assumed and overall a voltage-dependent density of the silanol sites was shown. In [9], the same theory was adopted with the introduction of a time relaxation model for the diffusion coefficient. Measurements in Si_3N_4 ISFETs, show a trend in the passivation capacitance change due to reduced insulator thickness after hydration which was in accordance with the diffusion model used.

Origin of trapped charge

The buried sites of silicon nitride have been also investigated due to its use as a dielectric in metal-nitride-oxide-semiconductor (MNOS) non-volatile memories [10]. It was observed that "deep trapping

centres" limit its usefulness as a dielectric by causing Si_3N_4 to show a memory behaviour of its own. Different models were put forward to explain the charge trapping behaviour such as nitrogen dangling bonds [11], silicon dangling bonds [12] and silicon-hydrogen bonds [13]. In [14], a strong correlation between the density of paramagnetic silicon dangling bonds and change in the space-charge density was observed which was subsequently modified by UV illumination.

More recently in [15], the composition of hydrogenated SiN_x layers was studied as well as the mechanism behind trapping generation. It was suggested that the PECVD procedure followed was crucial regarding the passivation quality and metrics used for quantifying the quality involved the Si-H bond density as well as the total bond density.

Even though the trapping mechanisms and the PECVD process are not the focus of this work, it is evident that they play a major role regarding the overall performance of a device using Si_3N_4 for sensing. In brief, the literature suggests that:

1. Both drift and trapped charge appear as a consequence of the amorphous nature of silicon nitride and the formation of buried sites in the material.
2. Buried sites form regions of positively or negatively charged silicon centres i.e. *trapped charge*.
3. When in contact with an electrolyte, hydrogen ions will diffuse into the silicon nitride with a certain diffusion and relaxation coefficient i.e. *drift* (albeit other phenomena are involved too).
4. The fabrication method and deposition chemistry determine the quality of the material therefore are the underlying factors affecting the sensing performance.

5.2.2 Overview of compensation methods

Trapped Charge

Compensation methods for trapped charge have followed both typical methods used in non-volatile memories (such as UV irradiation) as well as other circuit-based methods. Specifically, UV irradiation has been shown to reduce mismatch across a small array of ISFETs on the same silicon substrate [16], even though the exact modification area (passivation layer, floating gate or both) could not be determined. Alternatively, hot electron injection has been shown to permanently shift the threshold voltage of a single device by modifying the charge trapped at the floating gate [17]. Conversely, non-permanent compensation methods have been proposed such as the programmable gate approach by introducing an additional capacitor at the gate [18], source voltage (V_S) tuning to reduce mismatch in V_{GS} [19] and a gate reset switch to fix V_{GS} [20]. The robustness of the latter however showed a large susceptibility

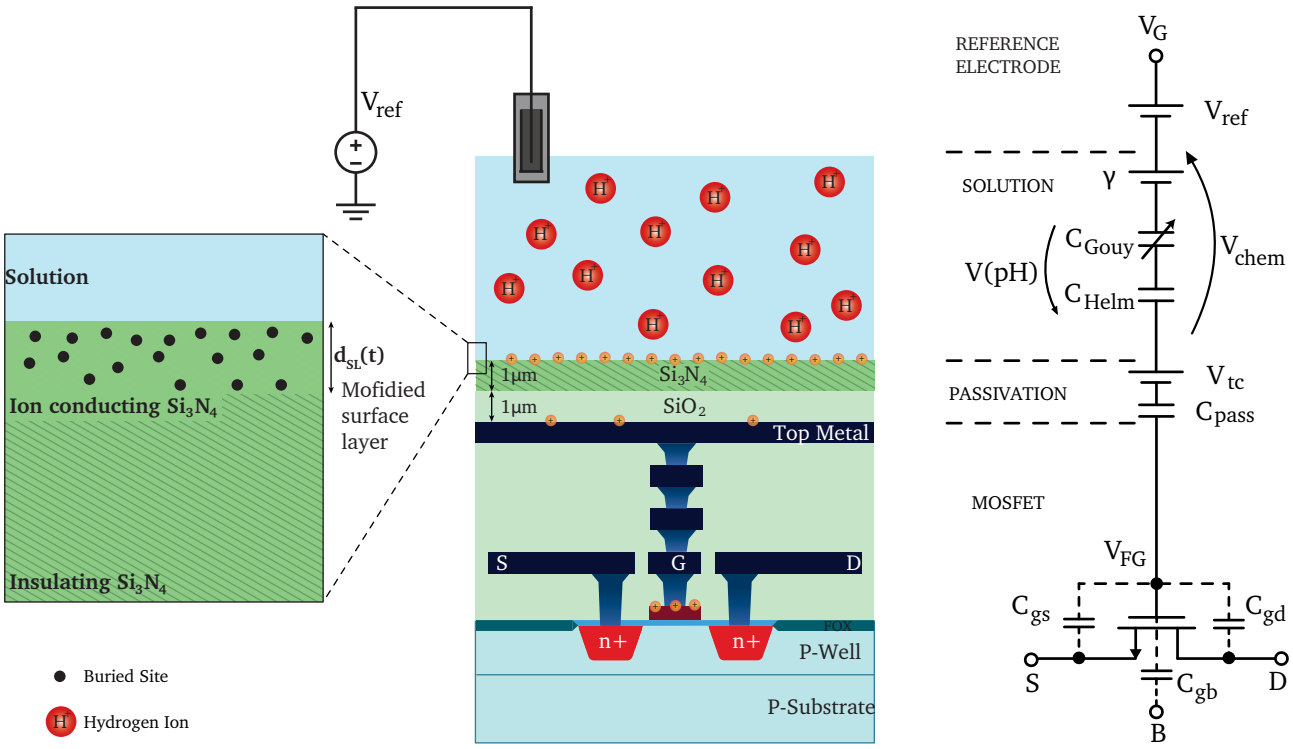


Figure 5.1: ISFET cross-section in unmodified CMOS and equivalent macromodel using an NMOS device. The leftmost close-up shows the modified surface layer of thickness $d_{SL}(t)$ after exposure to an aqueous solution.

to the non-zero leakage through the switch. It is important to note here that while fixing V_{GS} (for example using a gate switch) is an efficient way of establishing the operating point of the device, it does not remove charge which may be trapped in the passivation layer. More recently in [21], a compensation scheme based on a translinear loop was shown which showed compensation of up to 380 mV. Nevertheless, this is an area-consuming approach with a limited compensation range. Furthermore, in [22] a trapped charge cancellation scheme via direct tunnelling is proposed. In this case, the gate of a thin oxide device is connected to the floating gate such that the gate leakage current can provide a programmable current path for mismatch compensation. Simulation results in a 65 nm process showed compensation for a trapped charge spread of 1.6 V within 10 minutes.

Drift

On the other hand, methods to counteract drift in CMOS ISFETs have been scarce owing to the difficulties understanding the origins of drift itself. General explanations include the presence of buried sites within the insulator and the dispersive transport of charge carriers present in the electrolyte into an amorphous material (such as SiO_2 and Si_3N_4) [4]. Charge diffusing in SiO_2 has also been associated with a slow pH response which appears in conjunction with surface oxidation and leads

to a voltage-depended depth of the buried layer [8]. In [9], the buried site theory has been adopted with the introduction of a time relaxation model to describe the dispersion coefficient which matches well the passivation capacitance (C_{pass}) change observed during the course of drift. Owing to the complexity of the drift process, compensation methods have only revolved around post-processing of the recorded signal using derivative-based methods [23–25]. This approach however, is only valid when the instantaneous drift rate is small compared to the rate of change of the analyte concentration whereas the drift itself or the underlying process is not modified. A more recent approach, demonstrated with an ISFET in a MultiMEMS process, showed that drift resets to the same starting point after the electric field across the insulator is alternated [26]. Fig. 5.2 outlines these methods.

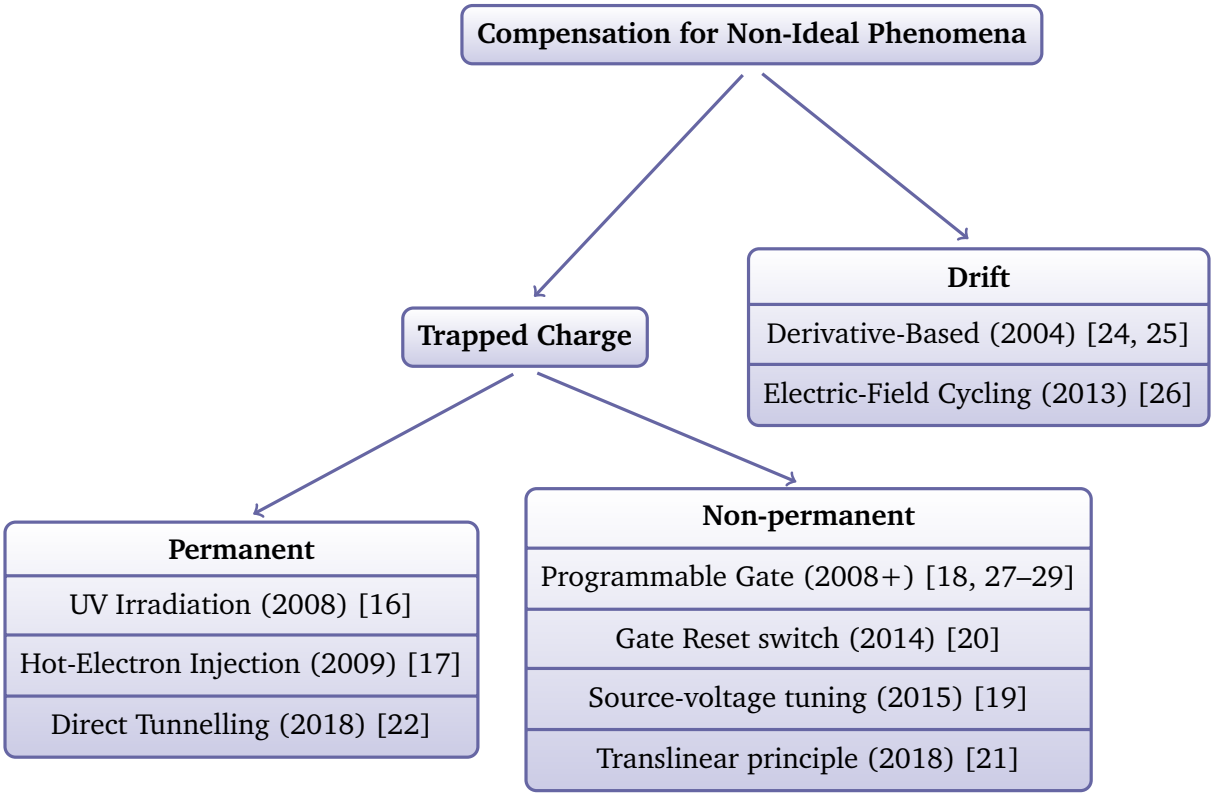


Figure 5.2: Summary of compensation methods for ISFET non-idealities.

5.2.3 ISFET Drift Modelling

Modelling the non-ideal phenomena constitutes the first step towards deriving compensation methods. Trapped charge is generally considered as a permanent modification therefore it is not mathematically modelled other than a random offset. On the contrary, modelling the behaviour of Si_3N_4 has formed a relatively active area of research due to the multiple uses of the material; as a protective layer in a $Si - SiO_2$ system, as a dielectric in non-volatile MNOS memory and as a sensing material in metal-insulator-semiconductor photovoltaic panels. In the case of ISFETs, the point of interest regards

the total change on the floating gate potential V_{FG} due to the underlying physicochemical processes causing drift. In general, the total change at the floating gate node can be influenced by either a change at the overall capacitance seen at that node, variation of charge or a combination.

$$\Delta V_{FG} = \frac{\Delta Q_{FG}}{\Delta C_{T,FG}} \tag{5.1}$$

where ΔQ_{FG} denotes the total change in charge and $\Delta C_{T,FG}$ the total change in capacitance at that node. Looking at the contributory capacitances to $\Delta C_{T,FG}$, it is reasonable to exclude the gate parasitics and chemical capacitances since the former are fixed for a constant biasing point and the latter are much larger than the passivation capacitance. Therefore by ignoring constant terms which are expanded in [30], Eq. 5.1 is equal to:

$$\Delta V_{FG} = \Delta Q_{FG} \times \frac{1}{C_{pass}} + (\Delta C_{pass})^{-1} \times \sum Q_{FG} \tag{5.2}$$

It indicates that drift can be influenced by charge diffused into the passivation layer *and* the potential change due to the passivation capacitance variation.

The change in passivation capacitance ΔC_{pass} originates from the variation in thickness due to hydration of the material. In this case, the rate of hydration is described by a hopping and trap mechanism known as dispersive transport. In an amorphous material, dispersive transport occurs from random hopping between localized states with the density of the trap sites or dangling bonds following a stretched-exponential decay law [31] given by:

$$\Delta n_{BT}(t) = n_0 \exp\left[-(t/\tau)^{\beta}\right] \tag{5.3}$$

where n_{BT} denotes the density of traps at equilibrium, Δn_{BT} the deviation from the equilibrium point, β the relaxation decay parameter and τ the transition time. The transition time relates to the thickness of the material as well as the electric field [32]. Based on this, the following relationship is derived which describes the thickness of the modified surface layer d_{SL} due to hydration [33]:

$$d_{SL}(t) = d_{SL}(\infty) \times \{1 - \exp[-(t/\tau)^{\beta}]\} \tag{5.4}$$

To derive a complete model for drift, the following simplifying assumptions are made:

1. The ISFET has a fixed threshold voltage, terminal voltages, parasitic capacitances and trapped charge at the floating gate.
2. The consistency of the hydrated layer is the same .

3. The contribution of ions diffusing in the material is small compared to the contribution of the change in capacitance due to its thickness variation.
4. The passivation capacitance change due to the modification is small compared to the magnitude of the intrinsic passivation capacitance.

Assumption 1 is reasonable when the device is biased at a fixed point. Assumption 2 is a first order approximation since in practice the surface layer is a combination of a top layer with both amino and silanol sites close to the surface and a second of silanol buried below [34]. Assumption 3 has been verified in [4]. Assumption 4 has been verified in [9].

Recalling that

$$V_{th,(ISFET)} = V_{th,(MOSFET)} + V_{chem} + \frac{\Sigma Q_{TC}}{C_{pass}} \tag{5.5}$$

where V_{th} denotes the threshold voltage, Q_{TC} the trapped charge, C_{pass} the passivation capacitance and V_{chem} the chemical ion contribution given by $V_{chem} = \gamma + \alpha S_N \; pH$. Therefore drift is modelled by considering the equivalent change at the floating gate voltage following the slow change on C_{pass} only (i.e. ΔC):

$$\Delta V_{FG}(t) = -\Sigma Q \left(\frac{\varepsilon_{ins} - \varepsilon_{SL}}{\varepsilon_{ins} \times \varepsilon_{SL}} \right) d_{SL}(t) \tag{5.6}$$

where ΣQ represents the total charge stored in this structure (depletion layer, inversion layer and insulator), ε_{ins} and ε_{SL} denote the dielectric constants of the insulator and modified surface layer respectively and $d_{SL}(t)$ describes the depth of the modified layer over time (shown in Fig. 5.1).

Equivalently, the response on the floating gate due to capacitance change over time can be modelled as:

$$\Delta V_{FG}(t) = \frac{dV_{FG}}{dC_{pass}} \times \frac{dC_{pass}}{dt} \tag{5.7}$$

and by assuming that changes in $V_{th,(ISFET)}$ are dominated by changes in trapped charge, then the overall drift at the floating gate is described by:

$$\Delta V_{FG}(t) = \underbrace{-\left(V_{th,(ISFET)} - \overbrace{V_{th,(MOSFET)} - V_{chem}}^{constant} \right) C_{pass}}_{\frac{dV_{FG}}{dC_{pass}}} \times \underbrace{\left(\frac{\varepsilon_{ins} - \varepsilon_{SL}}{\varepsilon_{ins} \times \varepsilon_{SL}} \right) d_{SL}(\infty) \left[1 - e^{-\left(\frac{t}{\tau}\right)^{\beta}} \right]}_{\frac{dC_{pass}}{dt}} \tag{5.8}$$

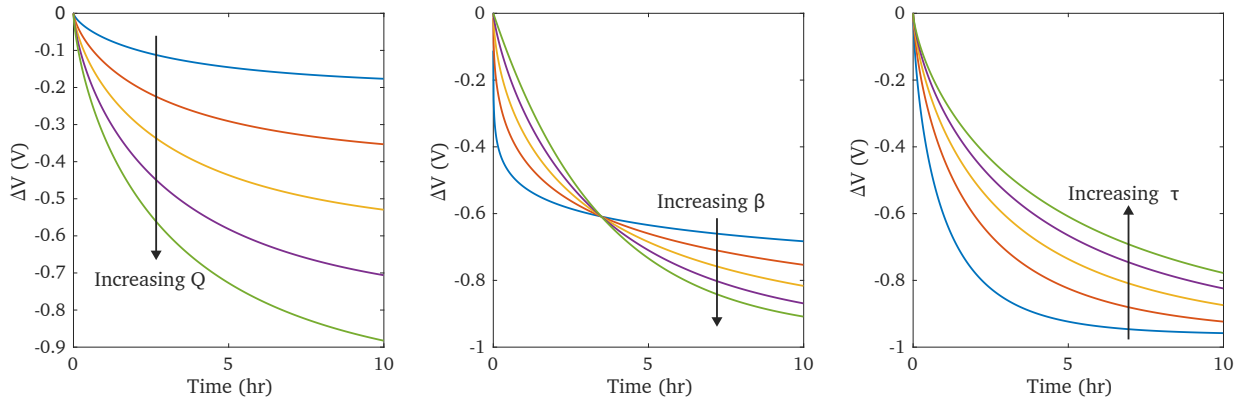
This equation shows that a linear relationship exists between drift and $V_{th,(ISFET)}$. By grouping constant terms, as shown in Eq. 5.9, experimentally measured responses can be fitted into three

constants: $\mathcal{Q}'$, τ and β where $\mathcal{Q}'$ corresponds to a scaled charge times distance term.

$$\Delta V_{FG}(t) = \mathcal{Q}' \left[1 - e^{-\left(\frac{t}{\tau}\right)^{\beta}}\right] \tag{5.9}$$

It should be noted here that second order effects such as floating gate leakage, electrode degradation etc. have not been considered i.e. drift originates only due to variations in C_{pass}.

The relationship in Eq. 5.9 is modelled in Fig. 5.3 illustrating the effect of each drift parameter. The original parameters from [35] were assumed with $\Delta V(\infty) = 963\,mV$, $\beta = 0.722$ and $\tau = 3.48$ hrs.



(a) Drift across $\mathcal{Q}'$ (b) Drift across β (c) Drift across τ

Figure 5.3: Simulated drift across its various parameters.

5.2.4 Drift Minimization

By using Eq. 5.8, the biasing point of the ISFET can be used as a direct indicator to the polarity and magnitude of the drift, thus threshold voltage tuning can lead to drift minimizing. This is specially true if other parameters, e.g. transistor size, MOSFET threshold voltage, electrode offset are the same as in a sensor array. Hereby, a procedure is proposed to minimize drift:

- Determine the drift and biasing point relationship.
- Locate the optimum biasing point for drift minimization.
- Modify $V_{th,(ISFET)}$ using UV or hot-electron injection.

5.3 Methods and Testing Procedure

5.3.1 ISFET readout

For the tests described here, both single sensors and arrays have been used from the TTN chip. In the cases where the type of sensor is not mentioned, the VM (left) array was used. The voltage output of the array gives a direct indication of the floating gate voltage since it is based on a source follower topology. For the VM array, each pixel spans approximately $96\,\mu m^2$ of silicon area, as shown in Fig. 5.4, which corresponds to an equivalent $C_{pass} = 2.17\,fF$. All arrays were designed with $2\,\mu m$ pixel spacing to reduce cross-talk. Alternatively, single sensors have been used to record the drain current of the device which were of the CM-PG pixel configuration. That corresponds to $50.54\,\mu m^2$ and $C_{pass} = 1.15\,fF$. Lastly, the pH sensitivity of the Si_3N_4 layer has been measured to be $\sim 18\,mV/pH$.

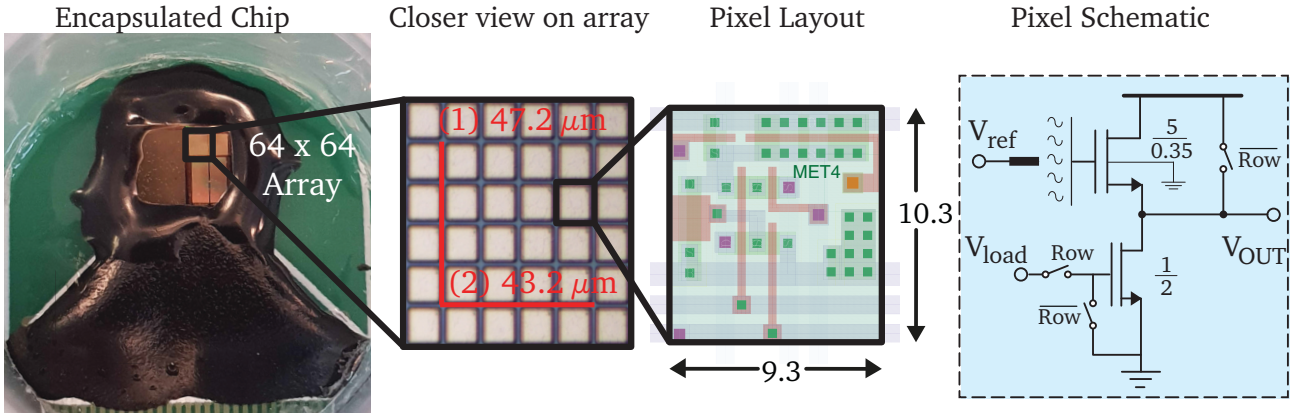


Figure 5.4: Test Setup showing an encapsulated chip, a microphotograph of the array surface showing a 6×6 section, the pixel layout and schematic.

5.3.2 Test Setup and Methodology

The test setup for long-term wet measurements is shown in Fig. 5.4. Each chip is glued on a gold plane and encapsulated using glob top insulating epoxy. A plastic tube is added around to host a solution chamber whereas a reference electrode inserted in the solution is used to provide DC biasing. For drift measurements the following process was followed:

1. The solution was biased at a constant DC point by applying a fixed V_{ref} in a buffer solution of pH 7.
2. The spatial spread of trapped charge across the array was obtained from the first frame measurement.

3. Pixels whose output over the whole drift period resided well inside the linear range of the source follower ($0.5V < V_{OUT} < 2V$) were considered as the active pixels whereas the rest were classified as outliers and disregarded from the analysis to ensure that 1) the op-amp buffering V_{OUT} operates in the linear range and 2) that V_{FG} doesn't exceed V_{DD} .
4. V_{OUT} was referred to the floating gate (V_{FG}) by using a look-up table obtained from simulation. The spread of V_{FG} with a fixed V_{ref} is considered to give a representative indicator of the trapped charge which could equivalently be represented as $V_{th,(ISFET)}$ spread.
5. Drift is recorded across the whole array for at least 100 minutes with a sampling rate of 0.3 fps. Measurements with a reference electrode current of $> 100\,nA$ were disregarded.

5.3.3 UV Irradiation

To modulate the threshold voltage, an off-the-shelf LED was used for irradiation with an output in the UV spectrum ($\lambda = 370\,nm$) at $10\,mA$ forward current. Additional details on the setup as well as results from UV irradiation on a single sensor are shown in Appendix C.

5.4 Results

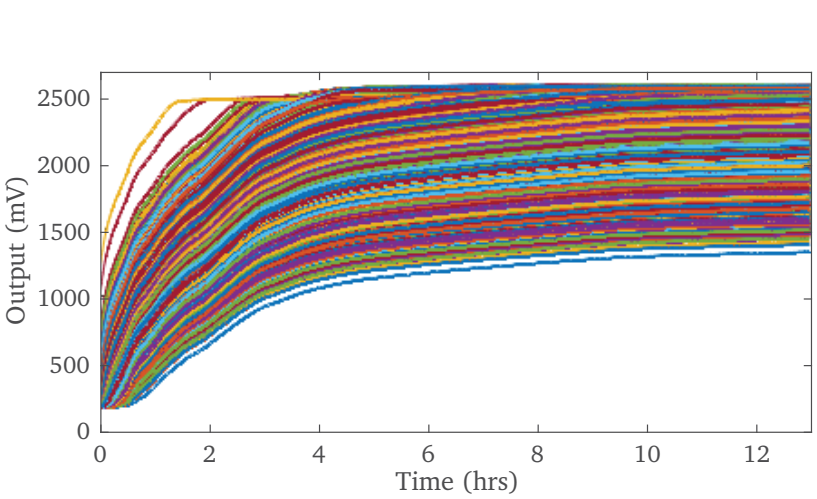
5.4.1 Drift Vs Operating Point

Drift Behaviour

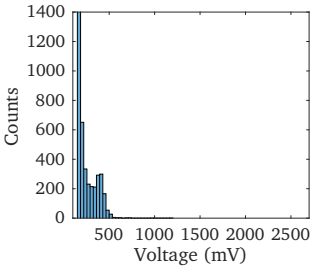
The long-term behaviour of drift is shown in Fig. 5.5 which shows the output of all pixels of the VM array for a time course of 13 hours. This is an extreme case of continuous measurements with some devices reaching the limits of the instrumentation range. Drift follows a stretched-exponential model with a relatively high drift rate at the beginning of measurements which eventually reaches a flat top. The recording was taken at a constant V_{ref}.

Additionally, the drift of the drain current of a single sensor at different V_{ref} potentials is shown in Figs. 5.6a-5.6c. Measurements were taken using a Keithley 4200 SCS platform. The DC value of the drain current reflects the reference electrode potential applied however the drift rate and/or polarity of drift also changes. This implies the existence of a relationship between the drift rate and the potential of the reference electrode or alternatively the electric field across the insulator. Furthermore, this implies that a V_{ref} value exists that minimizes or completely cancels out drift. It is important to note here that while this value might exist, it is unrelated to the biasing of the underlying devices therefore

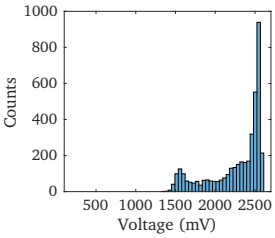
could be of little use when the V_{ref} needs to bias the devices at a certain point and/or counteract trapped charge. Nevertheless, this implies that trapped charge can be used to serve the same role.



(a) Output of all pixels in Chip 1 over the course of 13 hrs.



(b) First frame



(c) Final frame

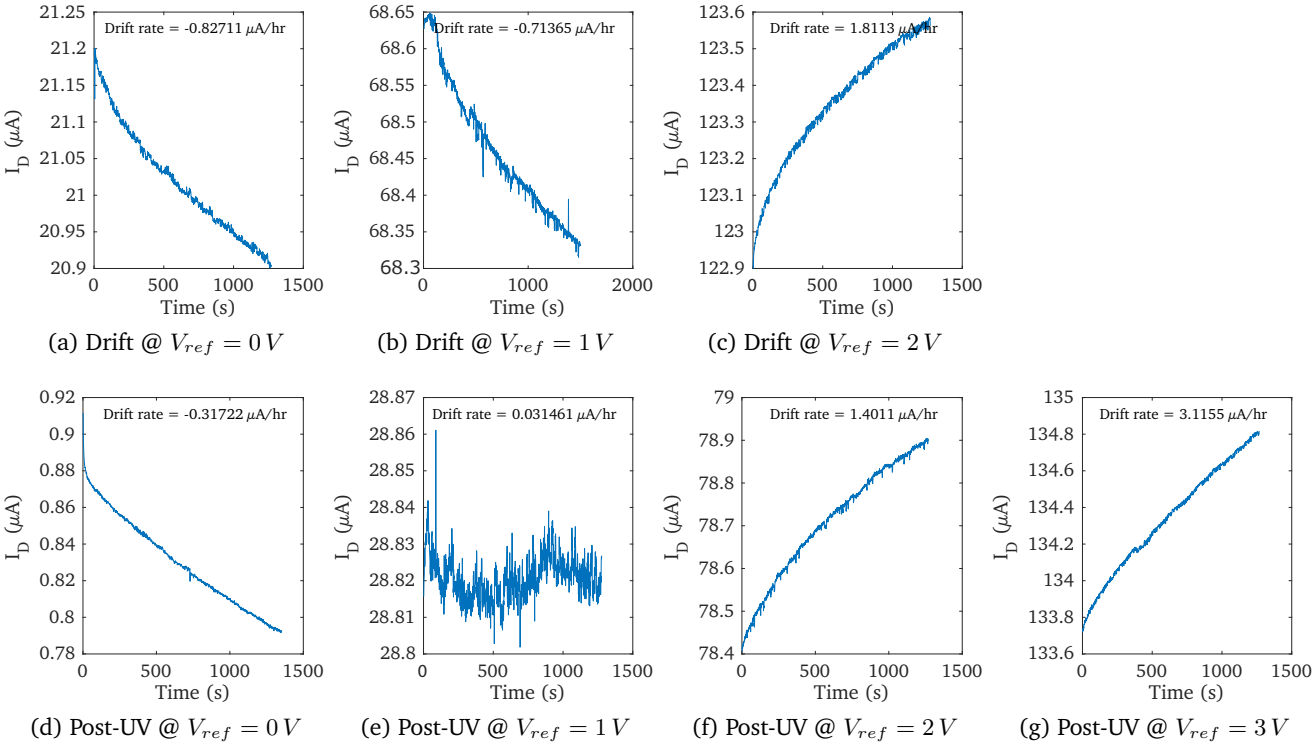
Figure 5.5: Long-term (13 hr) continuous wet measurements showing the drift of all (4096) pixels. The response follows the stretched-exponential model of dispersive transport. In the case of such long-term measurements, ISFET drift imposes a limit on the dynamic range and linearity. The readout range of the instrumentation used here is $0.25 - 2.5\,V$.

UV irradiation on single sensor

Figs. 5.6d - 5.6g show the drift of the same sensor after 16 hrs of UV irradiation. Using the same V_{ref} biasing points as before it is evident that 1) the trapped charge has reduced since the DC point is lower and 2) the drift rate is lower. Sensor modification via UV irradiation is also shown in Fig. 5.7 which illustrates the $I_D - V_{ref}$ sweep before and after irradiation. The V_{ref} value needed for the device to sink $100\,\mu A$ has been reduced by $0.81\,V$. Additional measurements regarding the I-V characterisation of this sensor before and after UV is shown in Appendix C. Furthermore, Fig. 5.8 illustrates the relationship between V_{ref} and drift rate before and after UV. In the common range of V_{ref} tested (0-2V), the absolute value of drift is lower post UV. From this empirical relationship, the biasing point for which drift is minimized can be deduced. It lies approximately at 1.3V initially and reduces to almost exactly 1V post UV.

5.4.2 Sensor Array

The average drift of the active pixels in ISFET array across 4 chips was recorded and is shown in Fig. 5.9a. All measurements were taken at a fixed reference electrode potential and at a point which



(a) Drift @ $V_{ref} = 0\,V$ (b) Drift @ $V_{ref} = 1\,V$ (c) Drift @ $V_{ref} = 2\,V$

(d) Post-UV @ $V_{ref} = 0\,V$ (e) Post-UV @ $V_{ref} = 1\,V$ (f) Post-UV @ $V_{ref} = 2\,V$ (g) Post-UV @ $V_{ref} = 3\,V$

Figure 5.6: Drift of the same sensor at various V_{ref} biasing points. The absolute value of drift reduces after UV irradiation and depends on the V_{ref} applied.

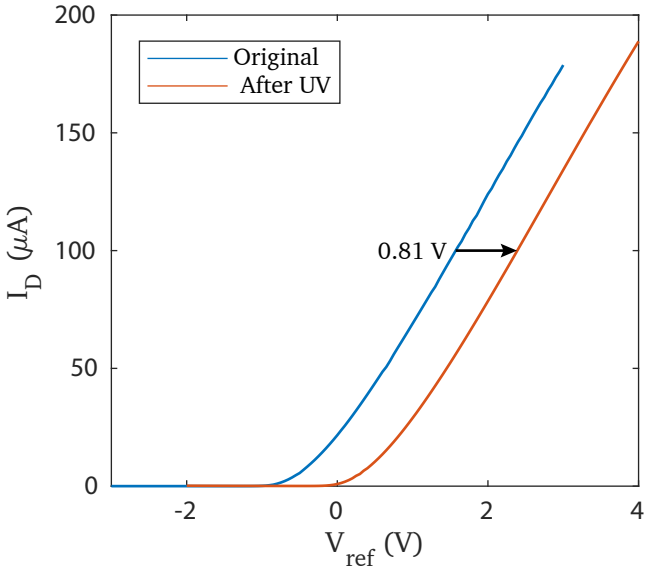


Figure 5.7: Effect of UV irradiation on the I-V characteristics of a single CM-PG test sensor. Measurements were taken at $V_{CG} = 0\,V$ after 16 hrs of irradiation.

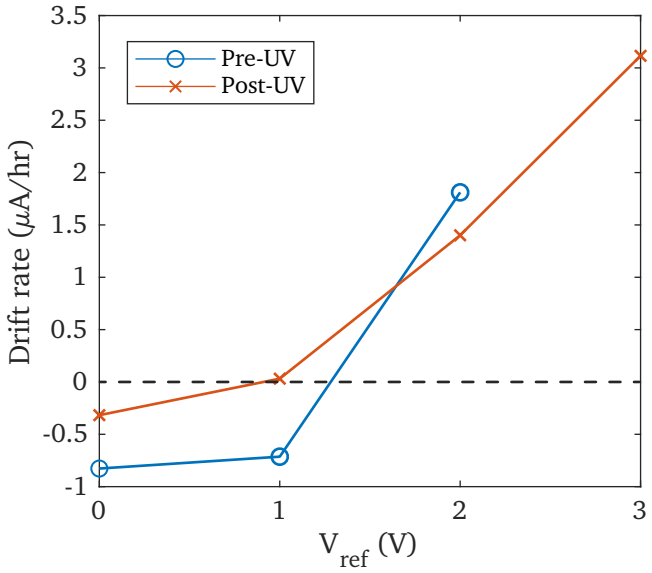
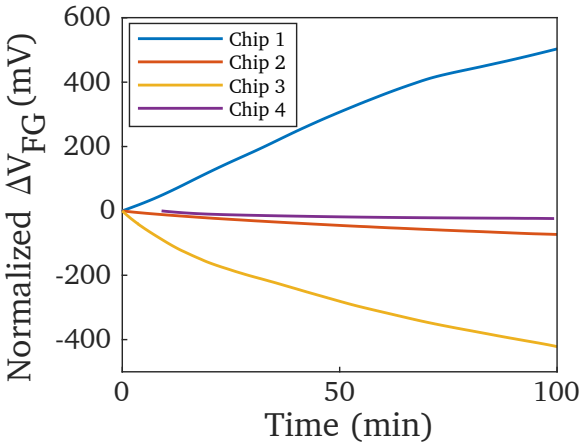


Figure 5.8: Relationship between V_{ref} and average drift rate on the same single sensor. A sweet spot exists which minimizes drift. Originally, it lies around $1.3V$ which reduces to almost $1V$ post irradiation.

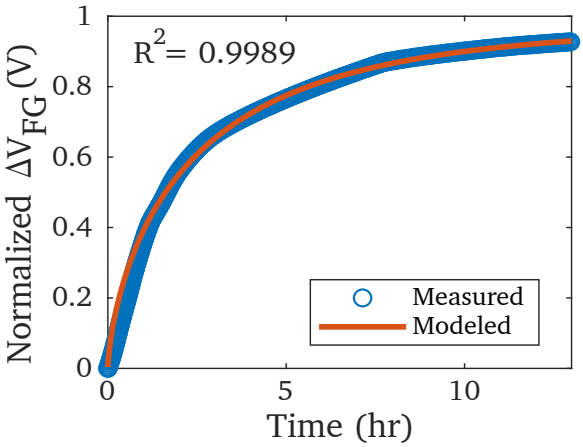
maximised the number of active pixels. Evidently, the magnitude of drift is different across chips owing to the specific biasing conditions (trapped charge spread and V_{ref} magnitude). Furthermore, Fig. 5.9b shows the average drift of Chip 1 over a longer time period (13 hr) to cover the whole course of drift with the measured data modelled using Eq. 5.9 are described with $R^2 = 0.9989$,.

In order to examine the relationship between trapped charge and drift, Fig. 5.10 shows the the drift characteristics for all active pixels of each chip against a trapped charge metric. Specifically, the top graphs show the average drift against the initial V_{FG} for that pixel, where the V_{FG} spread is correlated to trapped charge since V_{ref} is fixed. In all cases, (the absolute value of) drift is larger for higher V_{FG} (and hence less trapped charge). Moreover, the bottom graphs show the value of $\mathcal{Q}'$ obtained after fitting each pixel to the drift model, which clearly show the same trend as above. This trend wasn't obtained for the respective β and τ values (not shown). Overall, there exists a correlation between the amount of charge in the ISFET structure (captured by $\mathcal{Q}'$) and the magnitude of drift which is caused by trapped charge since all other parameters are identical for each array. It should be noted that even if this linear trend exists for each array, it may not be consistent across chips due to different setup (V_{ref}) and/or second order effects mentioned in section 5.2.4.

Even though the origins of drift itself are complex due to more than one chemical phenomena, this demonstrates that there is an optimum trapped charge point that minimizes drift.

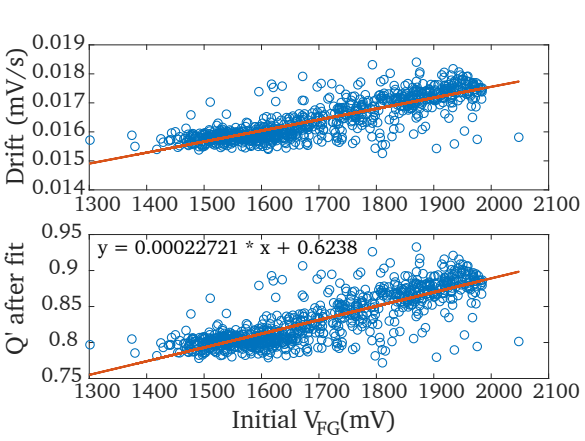


(a) Average drift of active pixels with fixed V_{ref}.

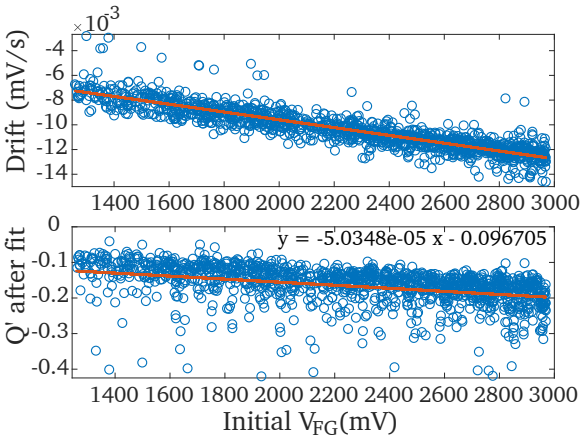


(b) Long-term drift of the ISFET array on Chip 1. Fit parameters on the drift model: $\mathcal{Q}' = 0.97329$, $\beta = 0.70059$ and $\tau = 2.5776$ (in hrs).

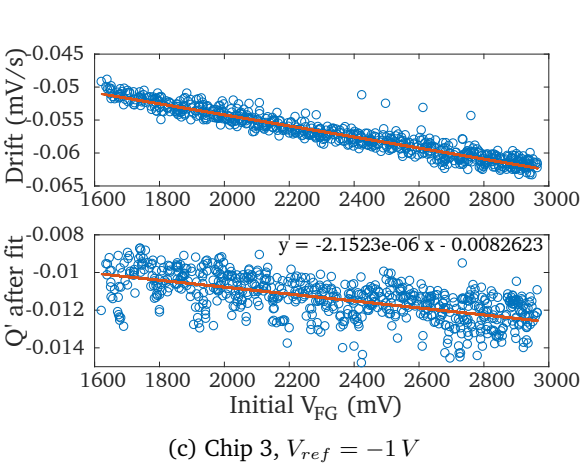
Figure 5.9: Drift characteristics in the time domain.



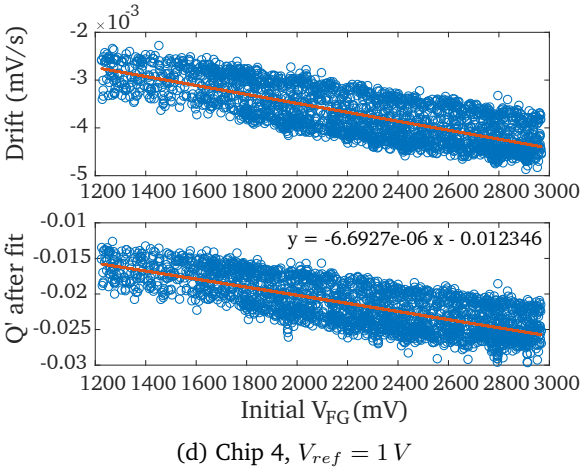
(a) Chip 1, $V_{ref} = 17\,V$



(b) Chip 2, $V_{ref} = 0\,V$



(c) Chip 3, $V_{ref} = -1\,V$



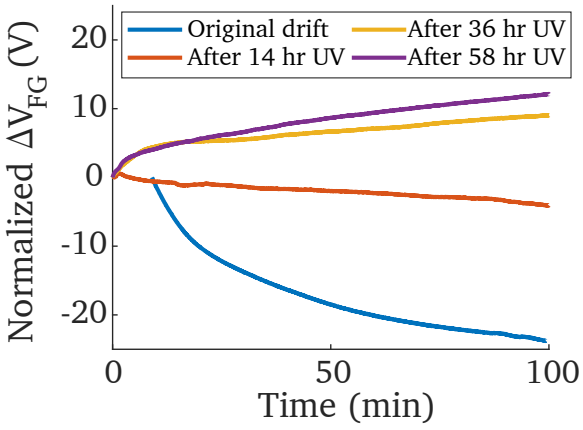
(d) Chip 4, $V_{ref} = 1\,V$

Figure 5.10: Drift characteristics of Si_3N_4 ISFETs across 4 chips, with a fixed reference electrode voltage, quantified as: average drift (top) and $\mathcal{Q}'$ term obtained after parameter fit (bottom) with respect to the initial V_{FG} as a measure of the trapped charge spread. In all cases, the absolute value of drift is higher for larger trapped charge at that pixel.

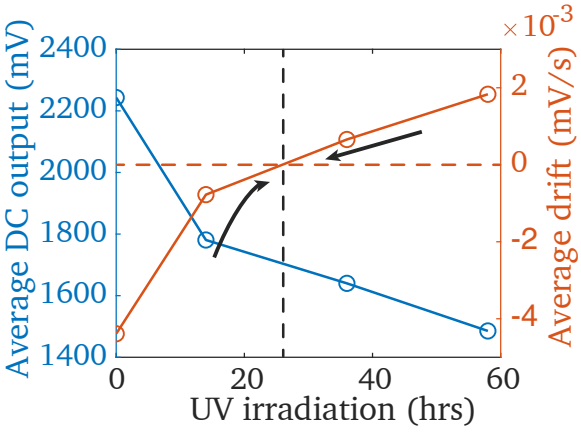
5.4.3 Drift Minimization

To verify this hypothesis, Chip 4 was irradiated for a total of 58 hours. Fig. 5.11a shows the average drift of active pixels at different points when irradiation was paused. Additionally, Fig. 5.11b shows the average drift as well as DC point of the array against time period of UV irradiation. Evidently, irradiation has modified the average trapped charge on the array which has reduced drift from 4.4 to $0.7\,\mu V/s$ after 14 hrs of UV. Further irradiation has reduced trapped charge even more which increased drift to $1.8\,\mu V/s$ after 58 hrs. This indicates that the trapped charge "sweetspot" has been exceeded, with drift now occurring monotonically in the opposite direction.

In order to verify the pH sensitivity of Si_3N_4 following UV irradiation, Fig. 5.12 shows the average array output of the same chip (Chip 3) before and after UV irradiation for 26 hrs in conditions of step pH changes. Step pH response was obtained by adding $5\mu L$ of HCl (Sigma-Aldrich H9892) to a buffer solution of pH 7 which was monitored using a commercially available pH meter (Sentron SI600). As shown in Figs. 5.12a and 5.12b, after UV irradiation the drift observed reduces enough to clearly show the step pH response following the addition of acid. Even though the pH steps are not linear, the average sensor output matches well the measured pH, shown in Fig. 5.12c. Irradiation has reduced drift rate by approximately three times.



(a) Average active pixel drift.



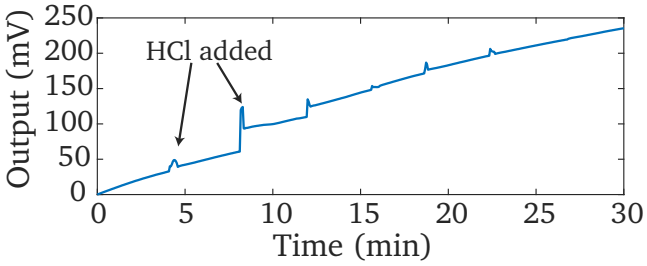
(b) Average array DC point.

Figure 5.11: DC characteristics of the ISFET array on Chip 4 before and after steps of UV irradiation. All measurements were obtained with $V_{ref} = 1V$.

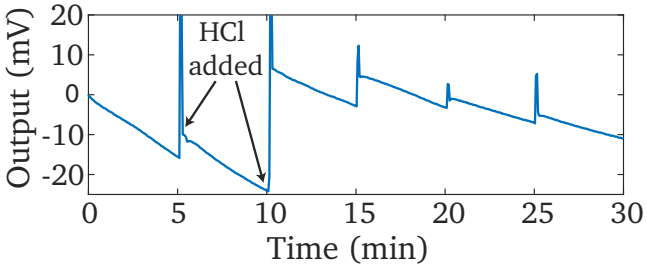
5.4.4 Discussion

Overall, two empirical conclusions can be extracted regarding the behaviour of drift in CMOS ISFETs.

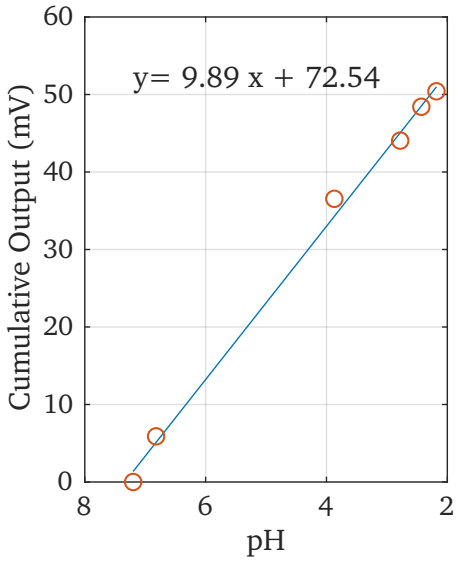
1. Firstly, a linear relationship exists between trapped charge and drift. This relationship predicts



(a) Before UV irradiation.



(b) After UV irradiation.



(c) Measured pH against the cumulative average array output.

Figure 5.12: (a) and (b) show the average array output following $5\mu L$ of HCl added at 5-min intervals to a buffer solution of pH 7. (c) shows the normalized array output after correcting for (linear) drift at each HCl addition against the pH measured using a commercially available meter.

that an optimum point exists which minimizes drift through modifying trapped charge. This optimum point can be identified as either threshold voltage offset or operational point depending on the biasing scheme of the readout circuits, which can be programmed via UV irradiation. To verify this, drift modification in an array of ISFETs is shown by removing trapped charge which improves the overall sensor performance.

2. Secondly, an empirical relationship between the magnitude of drift and potential of the reference electrode was observed which can be equivalently considered as the electric field across the insulator. This dependence modifies not only the magnitude of drift but its direction. This is in contrast which other works which mention that gate voltage is drift is expected to occur in opposite directions for n-channel and p-channel devices [9].

Electric Field Effect

Drift dependence on the electric field has been scarcely researched and it is considered to be related to the transition time τ in the drift model [32]. Specifically, the transition time of dispersion in an amorphous solid was shown to be inversely proportional to the electric field based on the theory of exponential decay of hopping energy.

High electric fields are expected to increase the reference electrode current which is another common cause of drift in electrolyte-insulator structures [9]. However in an ideal measurement setup and

constant chemical conditions, the reference electrode current should be negligible with no DC path to ground. Therefore, this effect should be minimized by improving the chip encapsulation, reference electrode chloridation and general configuration setup.

In [32], the transition time was observed to show a dependency on the electric field and was modelled by $\tau \propto (L/E)^{2.2}$ where L corresponds to the material thickness. As a result, the drift equation can be modified as:

$$V_{FG}(t) = \mathcal{Q}' \left(1 - \exp(-tk_\tau E^{2.2})^\beta\right) \tag{5.10}$$

where k_τ captures the proportionality term and any constants. This relationship predicts that higher electric fields will modify drift by accelerating the process. Assuming a constant electric field strength across the passivation, the electric field can be modelled as below and assuming $V_{pass} \approx V_{ref}$):

$$E_{pass} = (V_{pass} - V_{FG})/d_{pass} \propto V_{ref}\, C_{pass} \left(1 - \frac{C_{pass}}{C_{Tfg}}\right) \tag{5.11}$$

where C_{Tfg} denotes the total capacitance seen at the gate. A dependence of drift to the pixel size is also predicted through the inclusion of C_{pass} i.e. for sensors of same electrical area, the electric field will be higher for a smaller chemical area and thus inducing higher drift. Additionally, Eq. 5.11 predicts that drift can change direction.

To illustrate this dependence, a different chip (Chip 5) was selected for measurements with which large amounts of trapped charge were observed. As a result, a large electric field is developed across the passivation and large amount of drift is expected. Fig. 5.13 shows the average output of the VM array at two different V_{ref} points which reverse the drift direction. The DC point changes due to different biasing however it is evident that the drift is modified. The electric field across the insulator is different due to the capacitive attenuation from V_{ref} to the floating gate i.e. a 1 V change of reference electrode will change the floating gate potential by 480 mV in the case of the VM array. Therefore, the corresponding electric field across changes.

Practically, the dependence of Si_3N_4 modification on electric field can be exploited in the case of ISFETs when the electric field is cycled with a square wave such that the average electric field cancels out drift. To be able to use ISFETs, the target biasing conditions should occur at either the high or low edges of the square wave with synchronised readout. Initial measurements investigating this approach were obtained with a single sensor of Chip 5 where a reference voltage of $V_{ref} = 12\,V$ was needed to bias the device. The output of the sensor was recorded with an external ADC of 1 mV LSB at a sampling frequency of 20 kHz. The square wave was applied through the reference electrode which was connected to a Keithley 2602 instrument and subsequently controlled via a MATLAB-based serial

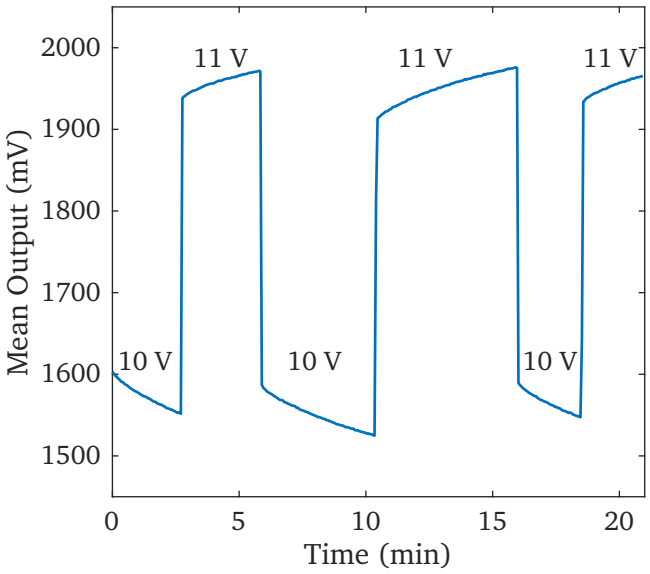


Figure 5.13: Dependence of drift direction on V_{ref}.

interface. With this instrument, the maximum frequency of cycling a voltage source was 20 Hz with an available square wave amplitude of ±20 V.

Two effects were investigated regarding the expected drift dependence on electric field, specifically the amplitude and frequency of the square wave applied to the reference electrode. Fig. 5.14 shows the effect of various amplitudes on the drift direction and magnitude. A resting $V_{ref} = 12\,V$ was required to bias the device at $V_{out} \approx 0.59\,V$, with upwards drift direction, that was subsequently cycled as shown in the figure. For an amplitude of $12 - 5 = 7\,V$, the envelope of the square wave stays approximately flat i.e. no drift. At larger amplitudes obtained by decreasing the lower limit of the square wave (e.g. 4 V), drift starts to occur monotonically downwards with an increasing rate for a larger amplitude. When the amplitude reduces (e.g. $12 - 6 = 6\,V$) drift starts moving in the upwards direction with an increasing rate for decreasing amplitude. Consequently, it is observed that the drift rate is modified by the electric field across the insulator which however is not quantified here.

Furthermore, Fig 5.15 shows the effect on the same sensor with square wave of fixed amplitude across various frequencies. The frequency varies from 20.44 Hz to 0.1 Hz and in all cases the drift direction is downwards. For very low frequencies, the effect of reversing polarity or direction is evident. Nevertheless, it is believed that the overall polarity is caused by the *average* electric field across and that the frequency of the square wave shouldn't have an effect on the overall behaviour.

It is important to note here, that these results represent initial empirical measurements leaving significant room for further investigation. The electric field is believed to not only modify the relaxation constant but also able to pull/push ions into the surface of the insulator Due to combination of these two effects, the total drift is caused by both the capacitance change and charge change and hence

is related non-linearly to the biasing conditions. Further results are needed to derive and validate a complete model for drift. Additionally, there is significant motivation in producing a simple and straightforward method for drift compensation in CMOS ISFETs. That could potentially be realized as programmable cyclic biasing with synchronised readout at the one of the biasing edges.

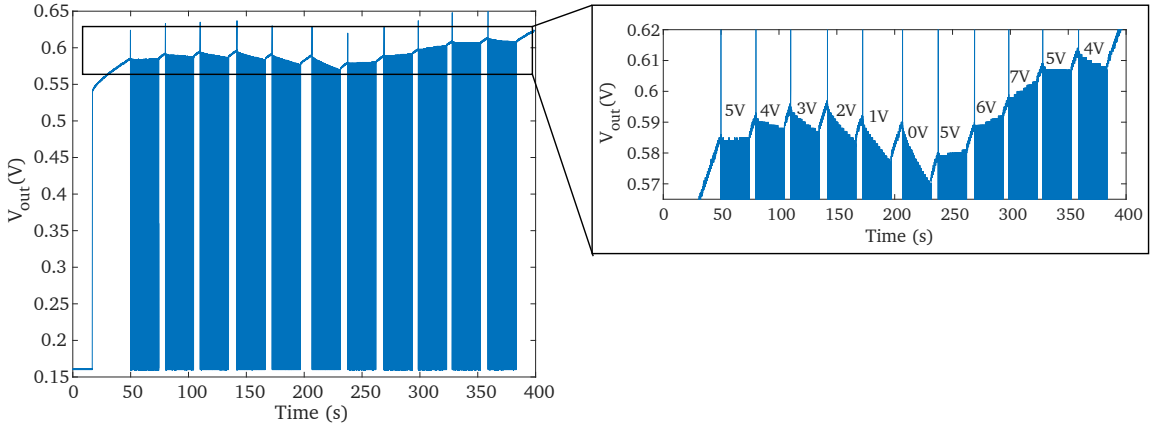


Figure 5.14: Effect of the cycling electric field amplitude on drift on a single sensor. The pulsed signal applied is cycled between 12 V and the annotated values. Evidently, drift charges both direction and rate according to the average electric fiend across the insulator.

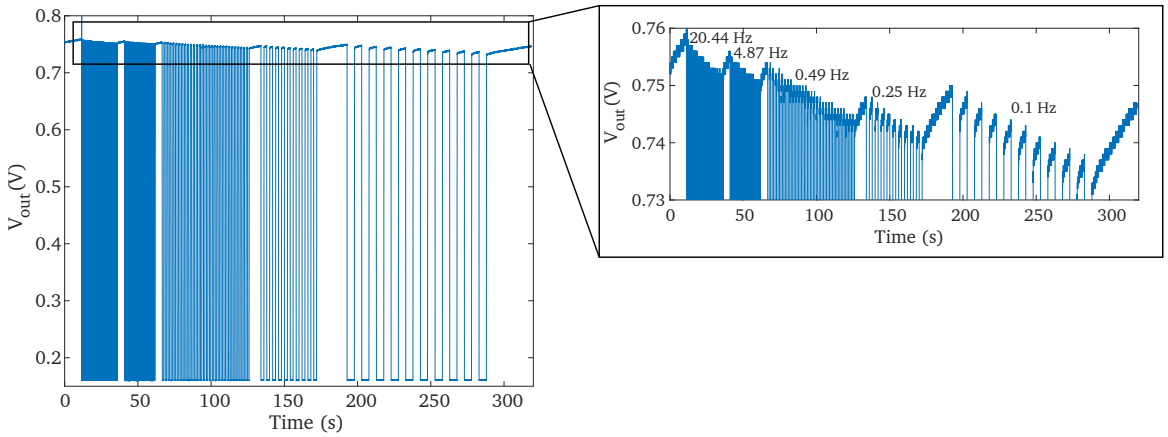


Figure 5.15: Effect of low frequency cycling of electric field on drift. No visible modification is observed since the drift direction is overall downwards with approximately the same rate at the various cycling frequencies.

5.5 Summary

This Chapter outlined the current theory and showed empirical results tying together trapped charge and drift. Evidently, these two effects are parts of a symbiotic relationship originating due to structural imperfections in the silicon nitride which allows buried sites to be formed. These sites can form charged areas i.e. trapped charge, which cause ion diffusion manifesting as drift upon contact with an aqueous solution.

Overall, a correlation is observed between the two which has been experimentally verified through both the use of single sensors as well as arrays. In the case of single sensors, the drift magnitude and direction was affected by the modification of trapped charge through UV irradiation. On the other hand, in the case of the VM array the correlation was observed even during the case of observing the drift characteristics of each pixel and correlating that to its trapped charge. Furthermore, controlled UV irradiation on the array showed the modification on the average drift observed due to modification in trapped charge. As a result, a trapped charge point is theorized to exists that cancels out drift and charge modulation techniques can be used to modify drift.

Furthermore, an additional dependence of the electric field across the insulator on drift was observed. That dependence was observed to modify drift in a non-linear way, nevertheless an electric field point which minimizes drift exists. Modifying the electric field is significantly easier than charge modulation however the precise mechanisms describing that dependence are not well understood. Given that the material quality causing these non-idealities in CMOS ISFETs is not controlled, further research along this path has the potential to not only expand the current understanding on the underlying mechanisms but also derive a method for drift compensation in unmodified CMOS sensors.

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Chapter 6

An ISFET Array Calibration Method Using a Programmable Gate

6.1 Introduction

In Chapter 5, the origin of non-ideal phenomena was investigated as well as an overview of compensation methods (in Fig. 5.2). Both major non-ideal effects, namely trapped charge and drift, originate due to the amorphous structure of the insulator with different characteristics each. Specifically, and from a modelling perspective, drift follows a stretched-exponential time response whereas trapped charge appears as a random offset across sensors. Even though methods exist which have been shown to modify both phenomena e.g. UV irradiation, introducing such a post-processing step in the sensor fabrication process is a time-consuming and costly step while it is not yet fully clear the exact extend of the modification. Instead, approaches which are well controlled by designers such as circuit-based compensation methods have been investigated especially to reduce the offset across sensors due to trapped charge.

In Chapters 3 and 4, the programmable gate approach was adopted to guide the design of a pixel and array configurations to include offset compensation. The PG modifies the floating gate potential therefore can be used to counteract for mismatch across sensors of common biasing. The main benefit of this approach is that the gate remains electrically floating and thus leakage is avoided which appears as electrical drift. Furthermore, in this work the PG capacitor is added *vertically* inside the pixel stack as the parasitic capacitance between two interleaved metal layers with SiO_2 dielectric and thus the pixel's scalability is not compromised. On the other hand, the main drawback of the PG approach is the reduction of the effective pH sensitivity due to the increase of the total capacitance seen at the floating

gate. The corresponding pH sensitivities with and without the PG capacitor are shown in Table 6.1 with a resulting decrease of 30.4% due to the PG.

In this Chapter, a calibration method to compensate for mismatch in large ISFET arrays is demonstrated based on the programmable gate technique. The only previous work showing calibration through the PG has been presented in [1] using an 8×8 ISFET array. In this case, the same method (Gradient Descent) is expanded on the 64×200 CM-PG array and adds a dynamic convergence point (rather than fixed at $V_{DD}/2$ as in [1]). Additionally, using *a priori* knowledge about the calibration step size, since it depends on a capacitance ratio, the calibration method is shown here to reduce from iterative gradient descent to a single iteration step. The two methods are compared on two different chips (and thus trapped charge spreads) with almost identical performance.

It is important to note that even though this method shows a significant reduction in mismatch across pixels, it does not remove trapped charge but counteracts its effect. As a result, calibration needs to take place every time the sensors are operated. Nevertheless, the trapped charge spread is reduced significantly enough such that in both chips tested, the majority of pixels lie within the linear range of the instrumentation therefore frame subtraction can be used to obtain linear signal differences. Pixels whose trapped charge is at extreme points such that they cannot be counteracted even for the full calibration range have been excluded from the measurements. Nevertheless, this is the case for a small minority of pixels and not in every chip tested. The trapped charge spread is indeed random across chips.

6.2 Gradient Descent

Gradient Descent (GD) is a widely-used optimization method for approximating the minimum of a function with an arbitrary number of dimensions [2]. Typically, GD is used to minimize the error or cost function in a convex optimisation problem. Assuming that a function is defined and differentiable, the magnitude and direction of its gradient can be evaluated. The main idea behind GD is that the minimum point can be approached by moving along the opposite direction of the gradient i.e. if at a certain function evaluation the gradient is positive then the minimum lies in the opposite direction and vice versa. The minimum of a 2D convex function is shown in Fig. 6.1.

Mathematically, considering an error function $F(w)$, the minimum can be approximated in small consecutive steps $w_0, w_1, w_2, ...$ which move in a direction opposite to the gradient. Equivalently, the sequence

$$F(w_0) \geq F(w_1) \geq F(w_2) \geq ... \tag{6.1}$$

must be monotonic for convergence. Evidently, the convergence performance is determined by the update rule (or learning rate) which determines the process of determining the next w. The update rule is given by:

$$w_{i+1} = w_i - \alpha_i \frac{df}{dw}(w_i) \tag{6.2}$$

such that the next function evaluation at the point w_{i+1} is obtained in an iterative way proportional to the gradient magnitude ($\times\alpha_i$) and opposite to the gradient direction. The step size determines the speed of convergence and is crucial for the correct implementation of GD. If the step size is too small, then convergence will be reached at the cost of an unnecessary number of function evaluations (shown in Fig. 6.2a). Conversely, if the step size is too large (shown in Fig. 6.2b), the minimum can be exceeded (overshoot) which can even cause divergence from the minimum. The gain parameter α_i is used to balance the two in order to find the optimum convergence rate.

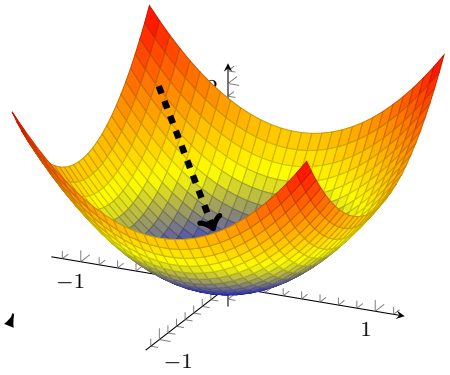
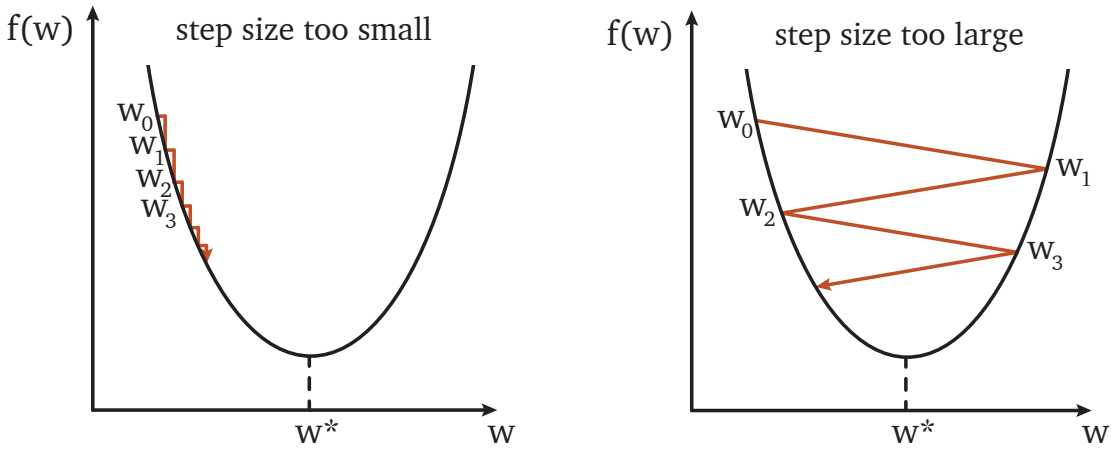


Figure 6.1: 2D convex function whose minimum can be reached using descending gradient steps until the gradient reaches zero.



(a) Slow convergence due to a small step size.

(b) Overshoot due to a large step size.

Figure 6.2: Illustration of the speed of convergence against step size $\alpha_i \times \frac{dF}{dw}$. The optimum parameter vector is given by w^*.

6.3 Calibration using GD

6.3.1 Calibration Algorithm

In this section, a calibration method based on GD is shown which aims to minimize the offset between pixels of the CM-PG array. An implementation of this method has been shown in [1] with an ISFET pixel configured in a unity-gain buffer configuration and a PG capacitor of $C_{PG} = 500\,fF$. In this case, the parasitic PG capacitance has been determined at $C_{PG} = 0.96\,fF$ using the method outlined in Appendix C.2.

During calibration, this method assumes chemical equilibrium i.e. constant pH, and constant biasing through the reference electrode. Biasing is expected to be at point which already maximizes the number of active pixels. Therefore, the algorithm aims to equalize the output of all pixels by reducing the differences in the current output I_{out} in velocity saturation.

The error function F in this case is defined as the mean-squared error (MSE) between the array output (CM-PG frame) and operating point I_{op}. Given an initial frame measurement, I_{op} is determined dynamically as the average output of the first uncalibrated frame and is a scalar parameter. With appropriate biasing in VS, it is expected between $100 \pm 20\,\mu A$. The MSE is defined as :

$$\mathbf{F}(\mathbf{V_{PG}}) = \frac{1}{N}\sum_{i=1}^{N}[\mathbf{I_{out}}(\mathbf{V_{PG}}(\mathbf{i})) - I_{op}]^2 \tag{6.3}$$

where $\mathbf{V_{PG}}$ denotes the vector of PG values in the range $0 \leq \mathbf{V_{PG}} \leq 3300\,mV$, $\mathbf{V_{PG}} \in \mathbb{R}^N$, N denotes the dimensionality which is equal to the number of pixels, $N = 12800$, and $\mathbf{I_{out}} \in \mathbb{R}^N$ holds the output vector at the corresponding $\mathbf{V_{PG}}$ vector. $\mathbf{F}$ is minimized when the error function is flat and thus gradient is zero:

$$\nabla\mathbf{F}(\mathbf{V_{PG}}) = \frac{2}{N}\sum_{i=1}^{N}(\mathbf{I_{out}}(\mathbf{V_{PG}}(\mathbf{i}) - I_{op})\,\nabla\mathbf{I_{out}}(\mathbf{V_{PG}}) = 0 \tag{6.4}$$

A general optimization algorithm to solve this problem involves searching for a sequence $\{\mathbf{y_k}\}$ that begins from an arbitrary initialization vector and converges to the set $Z = \{\mathbf{y} \in \mathbb{R}^N : \nabla\mathbf{F}(\mathbf{y}) = 0\}$. The corresponding gradient descent algorithm would be as shown in Algorithm 1.

6.3.2 Implementation

Implementing this algorithm for the CM-PG array, involves searching for the sequence of $\{\mathbf{V_{PG}}\}$ voltages that minimize the MSE between the target I_{op} and $\mathbf{I_{out}}$ vector holding the actual frame

Algorithm 1: Gradient Descent algorithm

```
begin
    Initialize: y_k ∈ ℝ^N, k = 0
    while y_k ∉ Z do
        Compute gradient direction d_k ∈ ℝ^N.
        Compute step α_k × d_k ∈ ℝ^N along d_k.
        Compute y_{k+1} ⇐ y_k + a_k d_k.
        Compute k ⇐ k + 1.
    end
end
```

output (in μA). Compared to the generic GD, there are two parameters to be determined, the gain of the step size α_i that determines the speed of convergence and the termination conditions which must be robust to quantization and other sources of noise. For this reason, α_i is programmable in order to test various convergence rates. Secondly, the terminating query has been modified from $\nabla \mathbf{F}(\mathbf{V_{PG}}) = 0$ to $\mathbf{F}(\mathbf{V_{PG}}) < \varepsilon_{thr}$. That means that the search for the optimum control gate voltages is completed when the MSE falls below a threshold instead of when the output stays the same for two consecutive steps. Mathematically, the search terminates when $\{\mathbf{F}(\mathbf{V_{PG}})\}$ converges to the set $Z = \{\mathbf{V_{PG}} \in \mathbb{R}^N : \mathbf{F}(\mathbf{V_{PG}}) < \varepsilon_{thr}\}$. Additionally, the algorithm terminates when a maximum number of iterations M is exceeded in order to avoid either a very slow convergence rate or oscillations around the optimum point.

This algorithm has been implemented as part of the Matlab GUI shown in Fig. G.1 split between embedded `C` and Matlab. At each iteration, a vector of $\mathbf{V_{PG}}$ is computed in Matlab and communicated to the microcontroller. During a frame readout, the microcontroller applies sequentially each $\mathbf{V_{PG}}(\mathbf{i})$ and reads the output of the corresponding pixel. The resulting vector of pixel values is communicated back to Matlab to compute the gradient and provide the next $\mathbf{V_{PG}}$ vector. Each $\mathbf{V_{PG}}$ is applied using a 12-b DAC with a 3.3V supply i.e. $805\,\mu V$ resolution.

A summary of the implementation is outlined below and diagrammatically in Fig. 6.3.

6.3.3 Results

This approach is based on a variable step size, $dI \times \alpha_i$, which decreases when the algorithm converges to the target operating point. Therefore, the magnitude of α_i constitutes a trade-off between speed and accuracy of the algorithm. To illustrate this, Fig. 6.4 shows the MSE as a function of iteration number at various convergence rates when the algorithm is operated on Chip 1. For small values, (e.g. $\alpha_i = 2$) the minimum is reached but it takes a large number of iterations for convergence. Conversely, for large

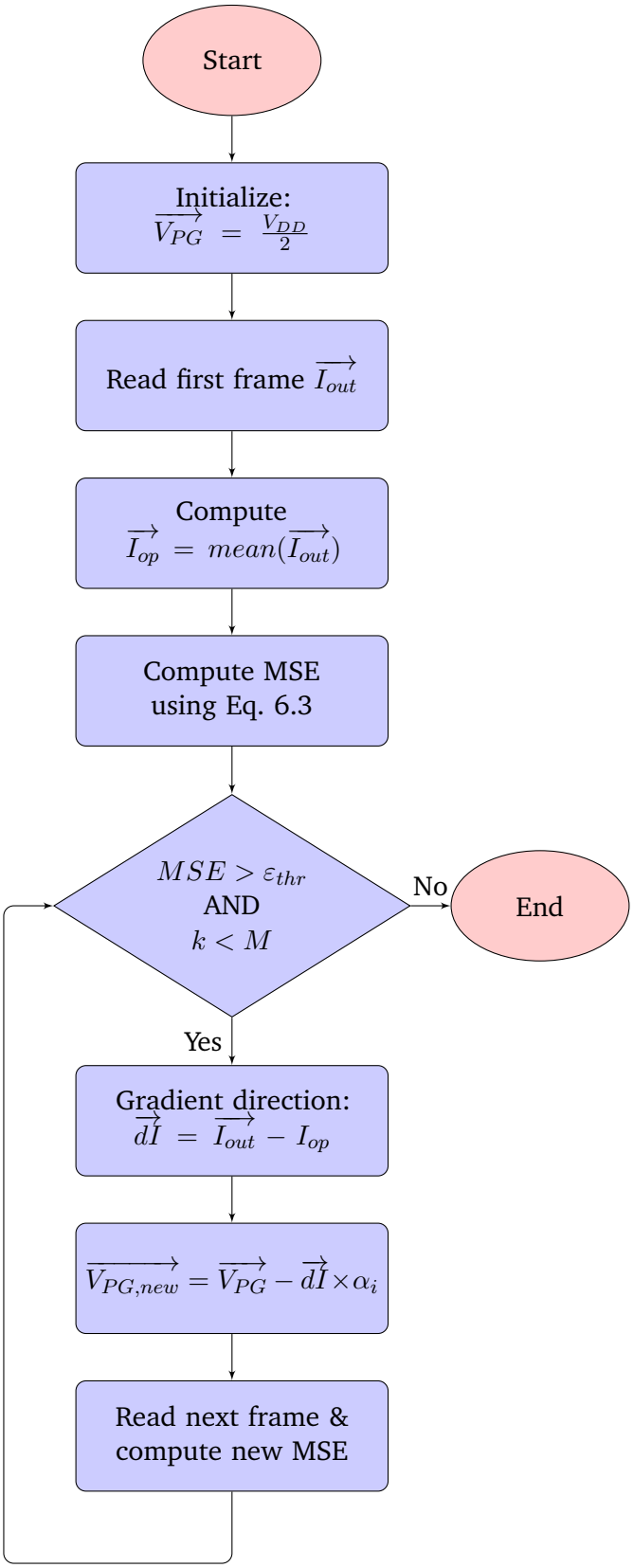


Figure 6.3: Algorithm structure using gradient descent to determine the V_{PG} vector that minimizes the error between the target I_{op} and array output I_{out}.

Algorithm 2: Gradient Descent implementation

begin
  Initialize $V_{PG} \Leftarrow \frac{V_{DD}}{2} = 1650\ mV$
  Read First frame: I_{out}
  Compute $I_{op} \Leftarrow mean(I_{out})$
  Compute MSE using Eq. 6.3
  while $MSE > \varepsilon_{thr}$ *and* $k < M$ **do**
    Compute Gradient direction: $dI \Leftarrow I_{out} - I_{op}$
    Compute New $V_{PG} \Leftarrow V_{PG} - \alpha_i \times dI$
    Read Next frame & compute new MSE
  end
end

values (e.g. $\alpha_i = 100$), the minimum point is exceeded which causes oscillations around the minimum point and divergence. As a result, $\alpha_i = 20$ has been selected as it optimizes the performance in terms of accuracy and convergence speed.

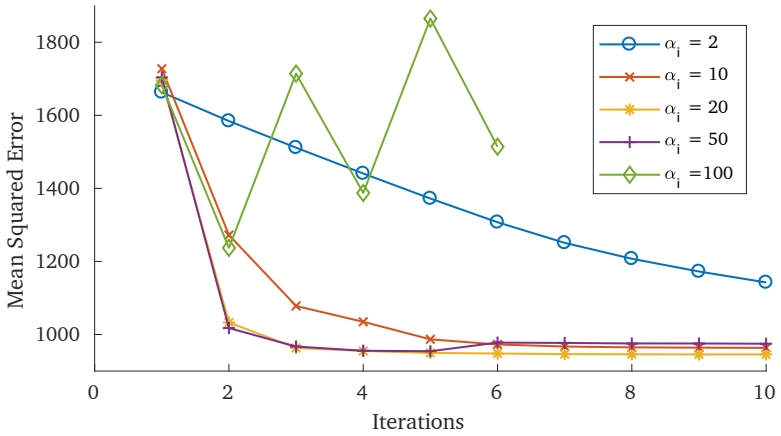
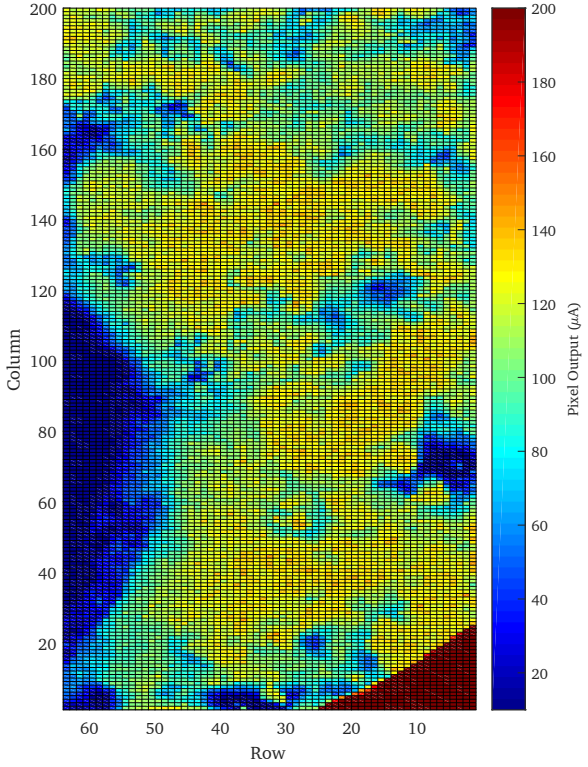


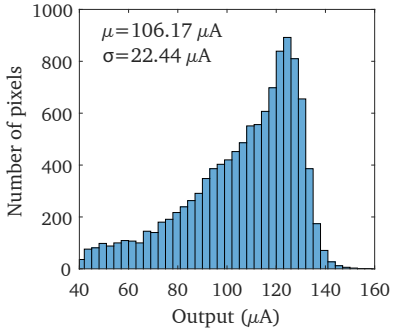
Figure 6.4: Plot of the mean square error (MSE) against iteration number k when calibrating Chip 1. For increasing magnitude of α_i, convergence to minimum MSE increases. Nevertheless, for very large step sizes (such as $\alpha_i = 100$) overshoot is observed and the output oscillates.

Figs 6.5-6.8 demonstrate the performance of the GD algorithm on 2 different chips with a different trapped charge spread each. The measurements have been taken at a constant V_{ref} and in de-ionized water. To quantify the mismatch improvement, the standard deviation of the output spread is used which shows a significant improvement of 81% and 75% for each chip. Additionally, the initial and final $\mathbf{V_{PG}}$ vectors are included to show the results of the optimization process.

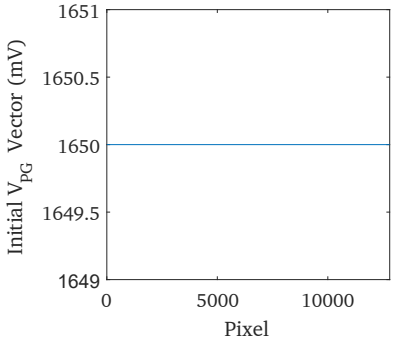
For both chips, the bottom left corner of the CM-PG array is covered by the encapsulating epoxy and is unresponsive to V_{ref}. Additionally, some regions of very low trapped charge are not significantly modified by V_{PG}. Therefore, pixels whose output lies $40 < I_{out} < 160\,\mu A$ are included in the histograms and are considered for the standard deviation measurements.



(a) First frame

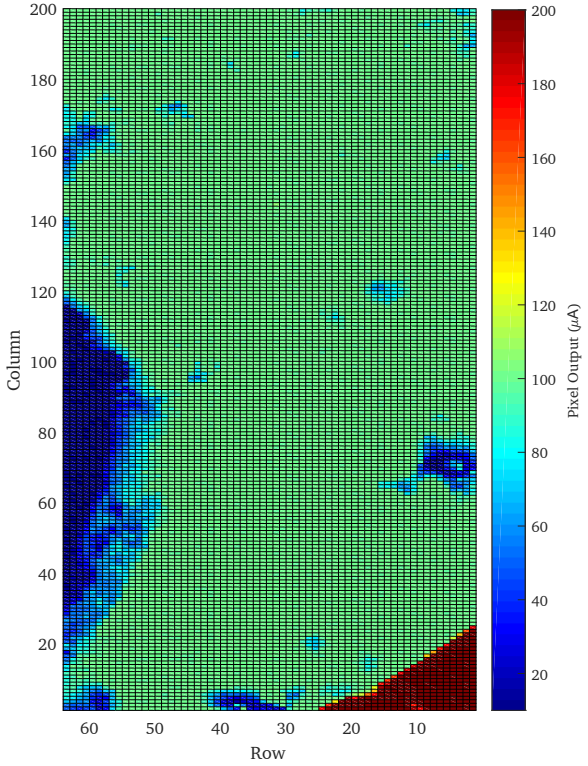


(b) Histogram

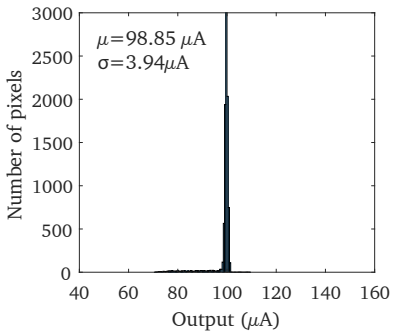


(c) Initial V_{PG} vector

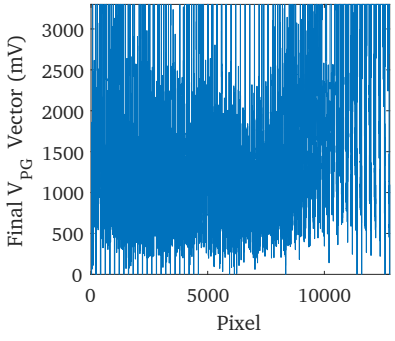
Figure 6.5: Chip 1 before calibration.



(a) Final frame

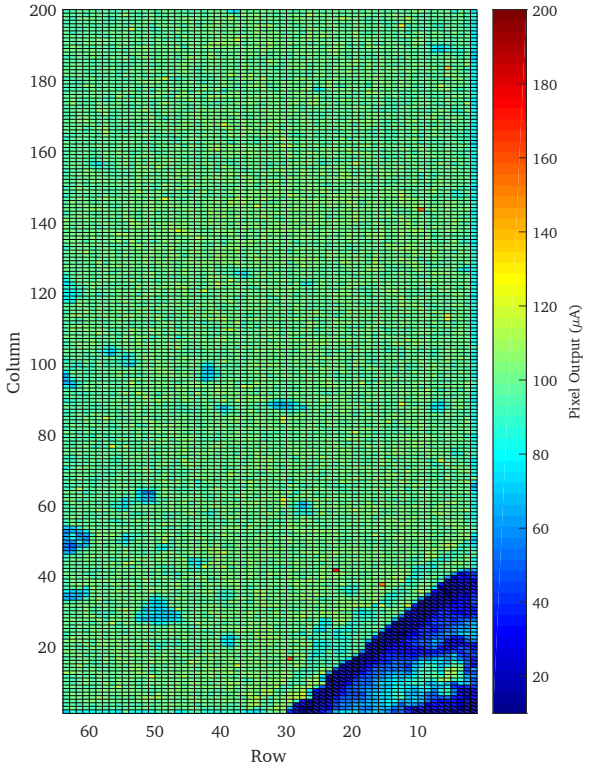


(b) Histogram

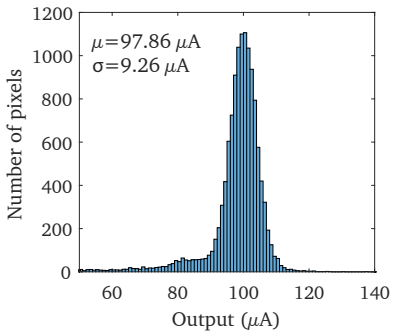


(c) Final V_{PG} vector

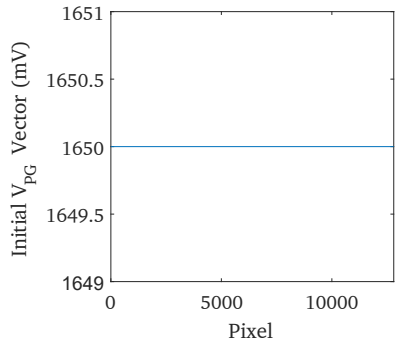
Figure 6.6: Chip 1 after calibration.



(a) First frame

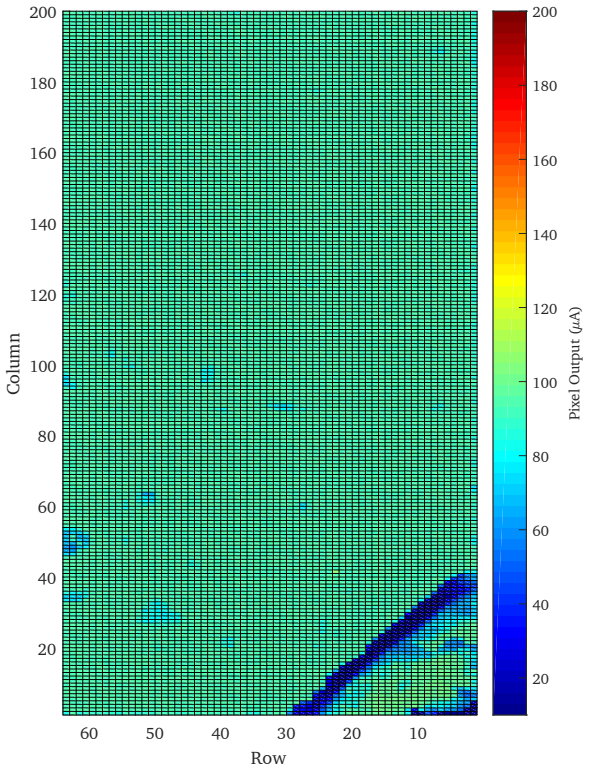


(b) Histogram

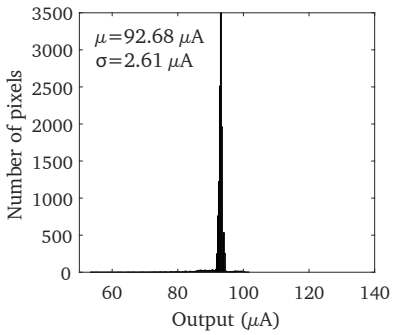


(c) Initial V_{PG} vector

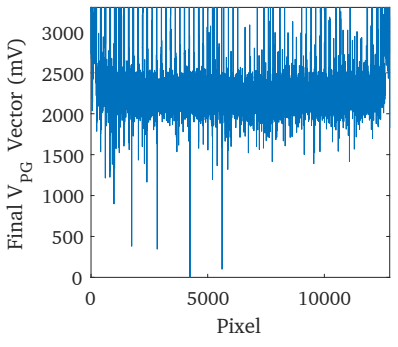
Figure 6.7: Chip 2 before calibration.



(a) Final frame



(b) Histogram



(c) Final V_{PG} vector

Figure 6.8: Chip 2 after calibration.

6.4 One-step Calibration

6.4.1 Calibration Algorithm

The algorithm previously described optimizes the $\mathbf{V_{PG}}$ vector in an unsupervised manner i.e. in small steps determined by a programmable step size α_i until an arbitrary minimum is reached. In this case however, it is possible to leverage *a priori* information regarding the expected response of the pixel when V_{PG} changes to make an estimate on the total step size.

Recalling that the response of the CM-PG pixel is given by Eq. 3.10, the programmable gate voltage needed to compensate for trapped charge is given by $V_{PG} = -C_{pass}/C_{PG}V_{tc}$ where V_{tc} denotes the trapped charge yet can include any type of offset across pixels. The sensitivity of I_{out} to V_{PG} is given by:

$$S_{PG} = \frac{\partial I_{out}}{\partial V_{PG}} = g_m \frac{\partial V_{FG}}{\partial V_{PG}} = g_m \frac{C_{CG}}{C_T} \tag{6.5}$$

Furthermore, the CM-PG pixel response has been experimentally characterised in Fig. 4.17 across the full range of both V_{ref} and V_{PG}. Therefore, by differentiating the measured response in Fig. 4.17b, the actual $\frac{\partial I_{out}}{\partial V_{PG}}$ can be obtained and is shown in Fig. 6.9 for an output range $40 < I_D < 200\,\mu A$.

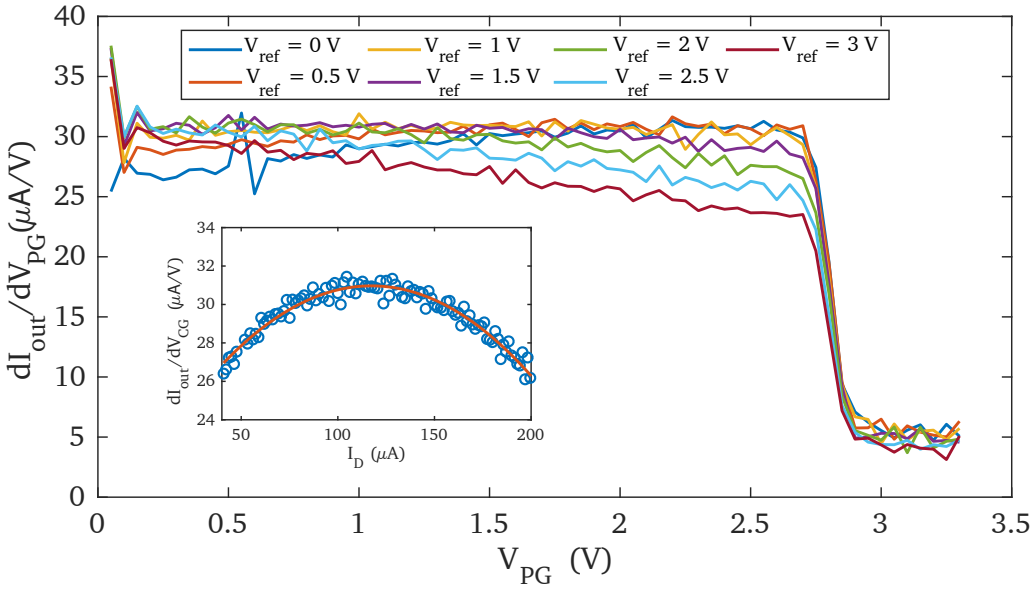


Figure 6.9: Sensitivity ($\frac{\partial I_{out}}{\partial V_{PG}}$) of the output current to V_{PG}. The inset shows the total response for a current range $40 < I_{out} < 200\,\mu A$ obtained by concatenating all the individual responses.

As a result, the total change that will cause the output of each pixel to converge to I_{op} can be estimated which will also minimize the MSE. By noting that $d \times \alpha_i$ is the inverse of S_{PG} (where S_{PG} is obtained

from Fig. 6.9), the new step size is given by :

$$d \times \alpha_i = \frac{dI}{S_{PG}} = dI \times \left(\frac{\partial I_{out}}{\partial V_{PG}} \right)^{-1} \tag{6.6}$$

As a result , the new V_{PG} that will cause the output to reach I_{op} can be estimated. The pseudocode is shown below and diagrammatically in Fig. 6.10.

Algorithm 3: One-step Calibration algorithm

```
1 begin
2     Initialize V_PG ⇐ V_DD/2 = 1650 mV
3     Read First frame: I_out
4     Compute I_op ⇐ mean(I_out)
5     Compute Gradient direction: dI ⇐ I_out − I_op
6     Compute Average sensitivity S_PG along dI
7     Compute New V_PG ⇐ V_PG − dI/S_PG
8     Read Last frame
9 end
```

6.4.2 Results and Discussion

The calibration performance of the 1-step algorithm is shown in Figs. 6.11-6.14. Chip 2 has been used to demonstrate the algorithm with at two different array biasing points to illustrate the dynamic convergence point at the mean of the first uncalibrated frame. The improvement in standard deviation before and after 1-step calibration is 52% and 86% respectively when biasing with $V_{ref} = 6\,V$ and $V_{ref} = 5\,V$. Pixel spread lies within a small range such that biasing is optimal with a common Vref across the array. In this case of velocity saturation, this maximizes the number of pixels that are operating in the perfectly linear $pH - I_D$ regime and thus the number of active pixels during array readout. Additionally, a single-step calibration process allows for calibration to be carried-out in more frequent intervals during readout in order to compensate for drift which affects the output in long-term measurements.

Overall, calibration in one step ensures performance comparable with the GD method while reducing the time needed for calibration. Further points to note regarding this approach are that:

- Quantifying the trapped charge spread using the standard deviation σ of the array histogram is not a representative metric when the spread is not gaussian. For Chip 2, the initial spread (shown in Fig. 6.11b resembles a normal distribution however for Chip 1 it does not. An alternative metric could be more appropriate to quantify the calibration performance.

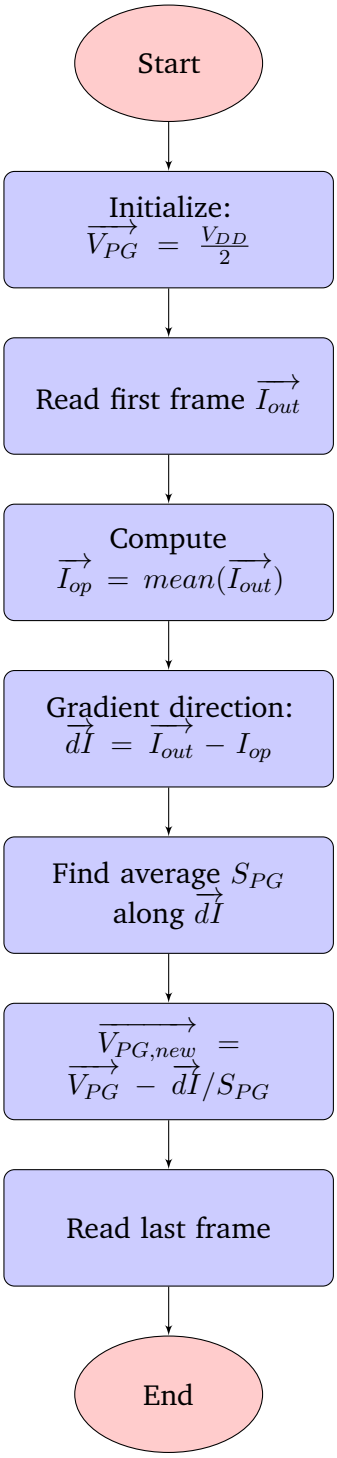


Figure 6.10: Algorithm structure using 1-step calibration to determine the V_{PG} vector that minimizes the error between the target I_{op} and array output I_{out}.

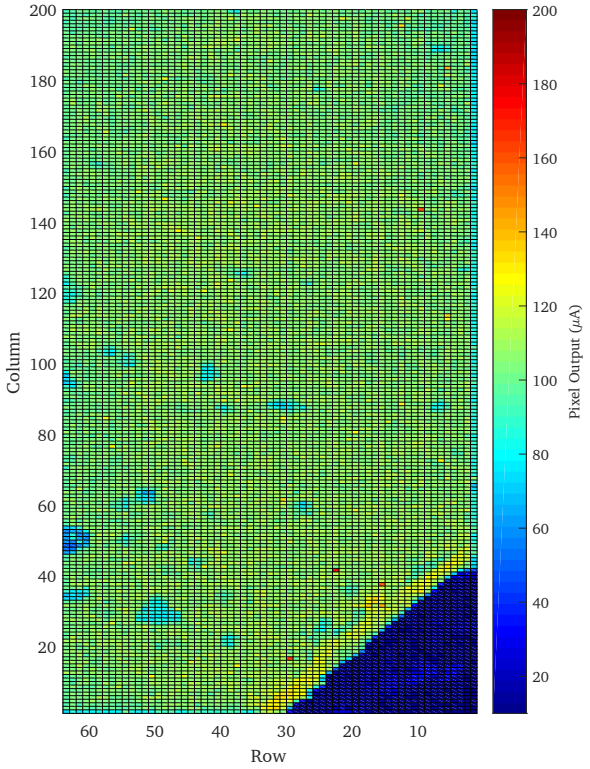
- The size of the PG capacitance constitutes a trade-off between the resolution and calibration range. In this work, a very small capacitance allows for fine tuning within the compensation range. In [1], a very large C_{PG} allows for more control on the floating gate voltage (sensitivity of V_{out} on V_{PG}) at the expense of reduced resolution. A trade-off between the two could be the best way forward in order to ensure that all pixels can be biased correctly even at extreme trapped charge offsets. Some mismatch can be tolerated when the outputs lie within the linear range of the instrumentation and can be compensated using double sampling.
- A simplifying assumption in this chapter has been that calibration will not be affected by drift which is only valid when the calibration process is fast compared to drift. Therefore, by implementing the algorithm in one step is advantageous for meeting this assumption and enabling the algorithm to be carried-out in more frequent intervals along the course of a readout proces

The table below shows a comparison between the approaches mentioned here and previous works for offset compensation in ISFET arrays.

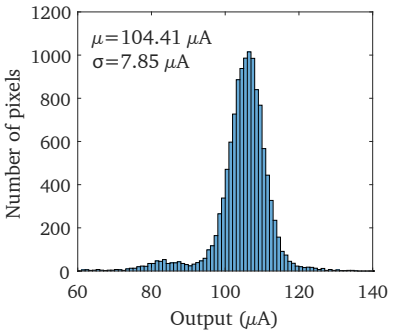
Table 6.1: Comparison with other works

Year	2008	2010	2011	2018
Reference	[3]	[4]	[1]	This work
Technology	CMOS AMS $0.35\mu m$ 2P3M	CMOS $0.35\mu m$	CMOS AMS $0.35\mu m$ 2P4M	CMOS AMS $0.35\mu m$ 2P4M
Array Size	2×2	40×1	8×8	64×200
ISFET size ($\mu m/\mu m$)	$1/0.35$	–	$200/1$	$0.5/0.4$
$C_{pass}\,(fF)$	–	–	57	1.15
$C_{CG}\,(fF)$	n/A	n/A	500	0.96
Sensing area (μm^2)	11.6×11.6	–	50×50	7.8×6.5
Method	UV irradiation	Digital calibration with summing amplifiers	PG ISFET with GD	PG ISFET with GD and 1-step calibration
Calibration	Off-chip	System level	In-pixel	In-pixel
Accuracy	10 mV[a]	3 mV	4.5 mV$\times G$[b]	$0.024\,\mu A$[c]

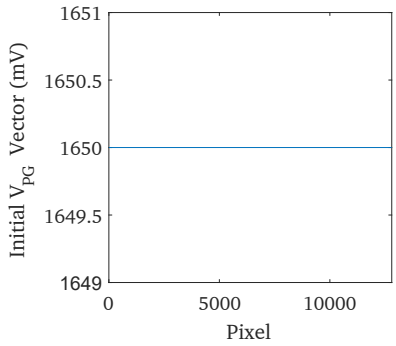
[a] Pixel-to-pixel variation.
[b] PGA gain.
[c] Obtained as the minimum resolution of the instrumentation = $S_{PG}\times$ DAC resolution = $30\,\mu A/V \times 805\,\mu V$.



(a) First frame

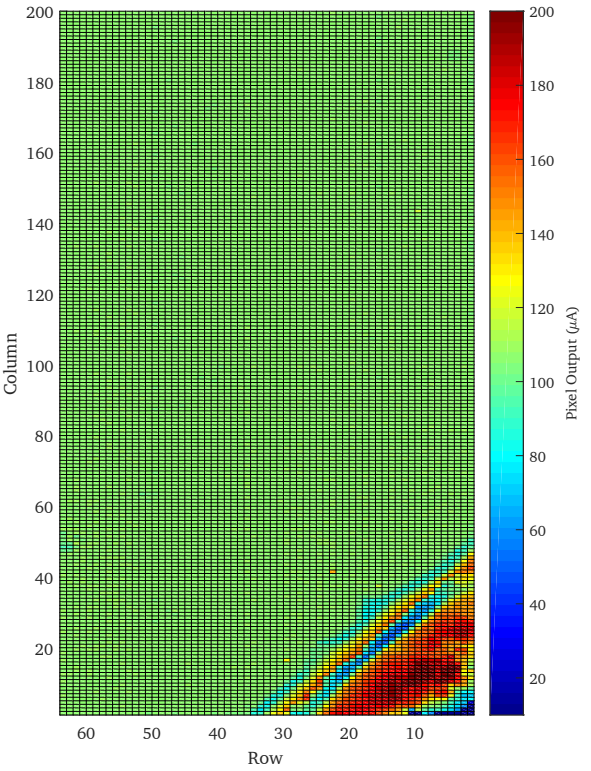


(b) Histogram

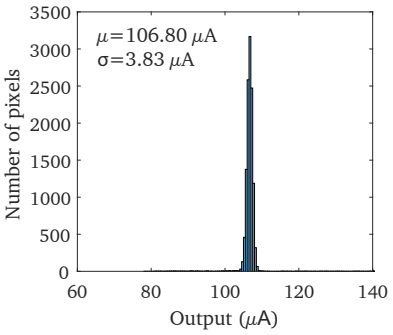


(c) Initial V_{PG} vector

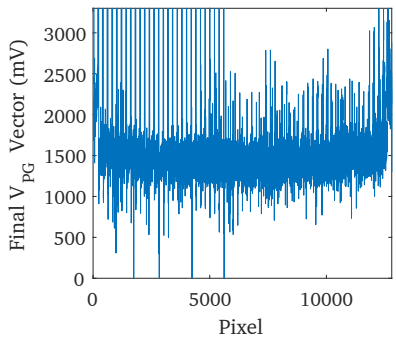
Figure 6.11: Chip 2 before calibration at $V_{ref} = 6\,V$.



(a) Second frame

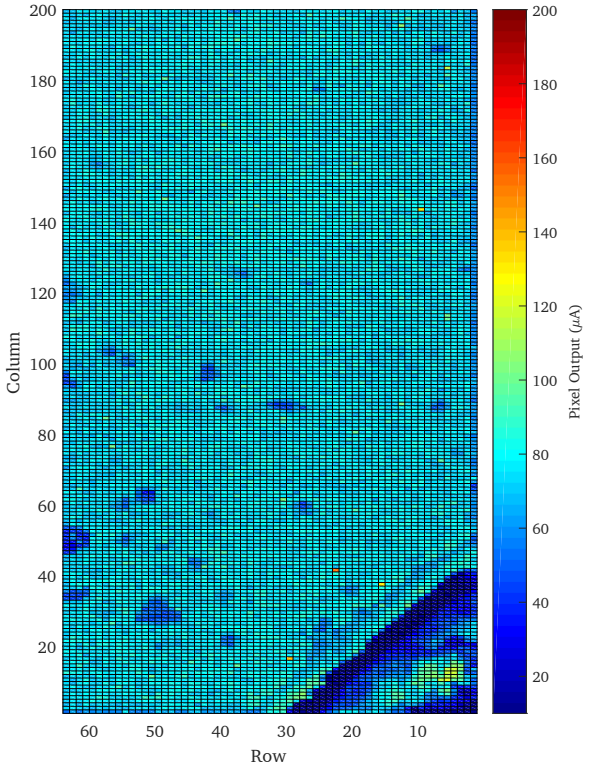


(b) Histogram

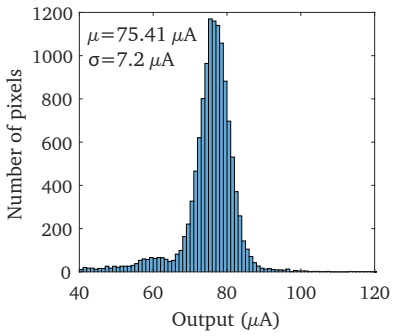


(c) Final V_{PG} vector

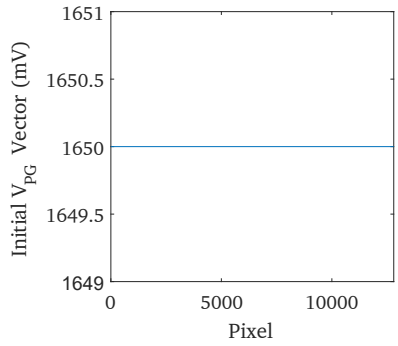
Figure 6.12: Chip 2 after 1-step calibration at $V_{ref} = 6\,V$.



(a) First frame

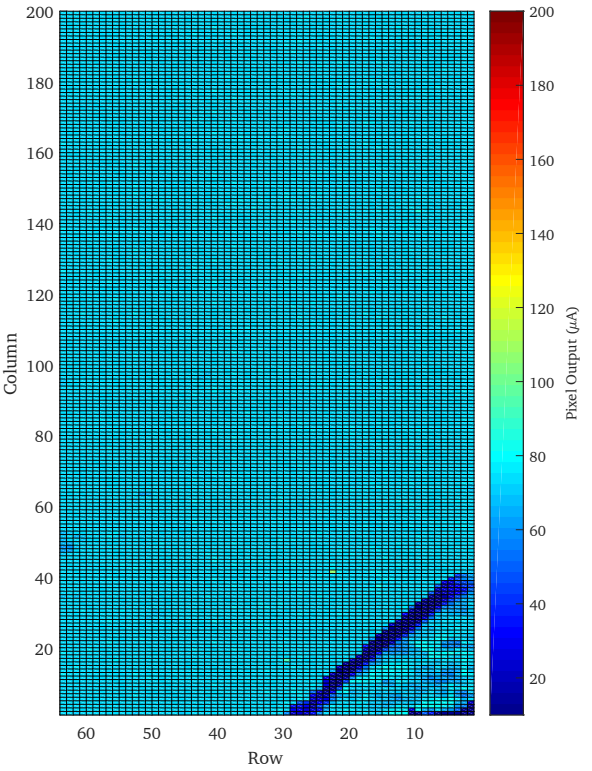


(b) Histogram

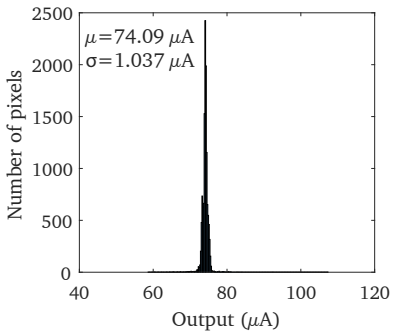


(c) Initial V_{PG} vector

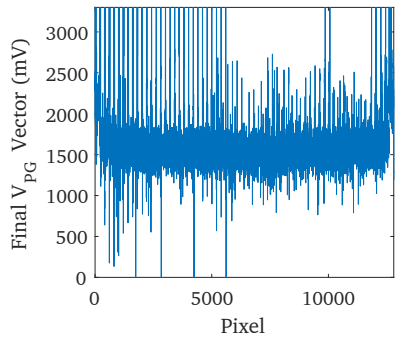
Figure 6.13: Chip 2 before calibration at $V_{ref} = 5\,V$.



(a) Second frame



(b) Histogram



(c) Final V_{PG} vector

Figure 6.14: Chip 2 after 1-step calibration at $V_{ref} = 5\,V$.

6.5 Summary

This Chapter demonstrates two implementations for mismatch calibration in large-scale ISFET arrays using the Programmable-Gate approach. A gradient descent method is demonstrated which estimates the PG vector that minimizes the mismatch between pixels in successive iteration steps. Furthermore, the effect of the calibration signal on the output can be determined by carrying-out an initial PG characterisation step. This way, an *a priori* estimate on the step size used by the calibration algorithm can be obtained which is leveraged to reduce the number of iteration to one. Implementations of both algorithms are shown on the CM-PG ISFET array with comparable performance.

References

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[2] J. Barzilai and J. M. Borwein. “Two-Point Step Size Gradient Methods”. In: *IMA Journal of Numerical Analysis* 8 (1 Dec. 1988), pp. 141–148.

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[4] D. M. Garner et al. “A multichannel DNA SoC for rapid point-of-care gene detection”. In: *2010 IEEE International Solid-State Circuits Conference - (ISSCC)*. Feb. 2010, pp. 492–493.

Chapter 7

Applications in Lab-on-Chip Diagnostics

7.1 Introduction

CMOS technology can be used to fabricate not only electronic but chemical sensors side by side. In order to meet the potential of such chemical sensors, it is necessary to pursue innovation at the intersection of disciplines by bridging the gap across electronics, genomics, molecular biology, microfluidics and biotechnology. This might entail tailoring molecular processes to become compatible with ISFET sensors i.e. by generating a pH signal, ideally where changes in pH carry the useful information. Fusing these technologies leads to the formation of the Lab-on-Chip (LoC) concept, a platform combining electronic sensors and instrumentation on a sensing substrate and a microfluidic arrangement for the integration of one or more laboratory functionalities. LoC has inherent benefits such as low sample (reagent) volumes, miniaturization and rapid reaction times, driven primarily by small feature sizes [1].

Leveraging on the benefits of CMOS compatibility and advances in nucleic acid amplification, ISFET-based sensing platforms have been demonstrated for detecting the presence or sequence of nucleic acid (DNA or RNA). Deoxyribonucleic acid (DNA) is the molecule containing all genetic information of any living organism and has a structure as shown in Fig. 7.1 The sequence of the DNA chain is organised in genes which in turn describe a certain function in an organism. Serially detecting an unknown sequence base-by-base is called DNA sequencing whereas detecting a specific segment of that chain has been typically referred to as DNA detection. Both have been shown possible with ISFETs [2, 3].

Both approaches for DNA detection rely on measuring the hydrogen ion release during DNA polymerization which leads to a change in pH and can be used to detect an unknown DNA sequence as well as determining the presence of a target sequence through amplification. Nevertheless, different design requirements are needed for each approach. DNA sequencing platforms benefit from very large

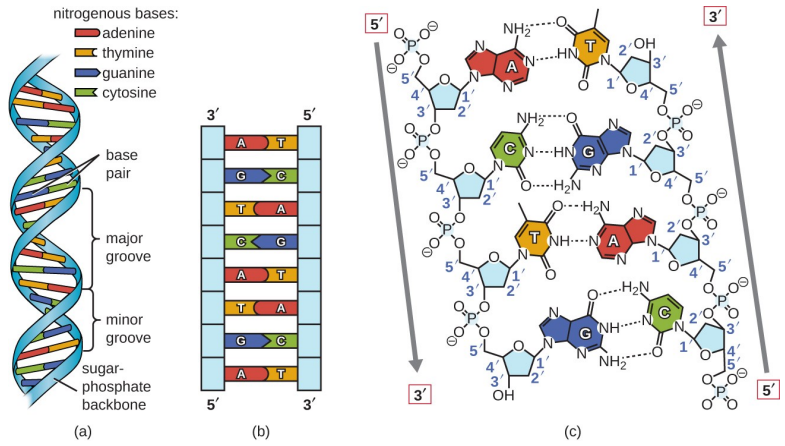


Figure 7.1: DNA model proposed by Watson and Crick. (a) The double-helix structure with sugar-phosphate backbones on the outside. (b) Two DNA strands that are antiparallel to each other. (c) The direction of each strand is identified by numbering the carbons (1 through 5) in each sugar molecule. The 5' end is the one where carbon #5 is not bound to another nucleotide; the 3' end is the one where carbon #3 is not bound to another nucleotide [4].

ISFET arrays ($> 1M$ pixels) to detect an unknown sequence in-parallel where each pixel is responsible for detecting a fraction of the total sequence. Such a task requires powerful instrumentation, real-time microfluidic operations and signal processing to assemble the final sequence and it's typically carried-out in a specialized benchtop lab instrument. Instead, DNA amplification and detection has the potential of miniaturization, rapid detection and high specificity and thus lends itself to Lab-on-Chip implementation.

Overall, there exists significant potential in transferring amplification chemistries to Lab-on-Chip biosensing technology. DNA amplification can be conveyed into a pH signal which indicates the existence of the target in the sample. In that sense a "sample-to-result" format is possible which satisfies a major requirement in Point-of-Care (PoC) diagnostic systems. Other requirements as outlined in [1] include:

- Rapid test results.
- Accurate and quantitative results comparable with that of bench-top analyzers.
- Easy-to-use systems that can be used by non-experts or after minimum training.

PoC systems have been recognised as a crucial tool in the diagnosis of infectious diseases and anti-microbial resistance by being able to meet the urgent needs for rapid, portable and ultra-sensitive diagnosis [5]. Microchip-based LoC technologies are able to tackle theses challenges and provide a solution for PoC diagnostics that can be deployed in the lab, in the doctor's office as well as in remote communities.

In this context, this chapter describes the process of operating the sensing platform described in

Chapter 4 for monitoring the pH changes during DNA amplification. A wide set of targets have been isolated and transferred for on-chip amplification. They are outlined below in chronological order:

1. The NDM-1 gene isolated from *Escherichia Coli* (Synthetic DNA) [6]. Bacterial strains that carry the NDM gene represent a major health care challenge worldwide since they are resistant even to carbapenems antibiotics which are used as a last resort when common antibiotics have failed [7].
2. Single Nucleotide Polymorphism (SNP) present in a gene (Kelch 13) within the parasite species *Plasmodium Falciparum* which causes Malaria (Synthetic DNA). The presence of that mutation indicates that the parasite is resistant to artemisinin-based combination therapies therefore the patient will not respond to treatment [8]. Additionally, the same target (Kelch 13) is detected with the aim to detect the species specifically, i.e diagnosing the type of malaria.
3. Tandem repeat (short repetitive sequence) in Azole-resistant *Aspergillus fumigatus* (Synthetic DNA) [9]. That repeat can be considered as a mutation identifying the species of fungus.
4. SNP in a human genome gene (PIK3CA) that indicates a high probability of Breast Cancer (Synthetic DNA).
5. Human genes that could be used to differentiate bacterial vs viral infections in febrile children. RNA biomarkers were extracted directly from human blood samples.

The following sections present the experimental setup as well as a collection of results from the DNA amplification experiments with Malaria detection as a case study.[1] Furthermore, the approach to extract the amplification signal which resembles a sigmoid pH change, in the presence of drift, is outlined. This method uses a quantitative drift model, derived in Section 5.2.3, Eq. 5.9, to compensate for drift during and after amplification with the final response approximating the output obtained from a qPCR instrument used as control. Lastly it should be noted that even though the experimental setup presented here does not qualify as a PoC device due to additional functionalities needed to be miniaturized for portability, the ISFET sensing protocol and sample preparation for on-chip sensing have been already optimized for PoC. Only electrical functionalities remain to be adjusted such as temperature control of PCB hosting the chip. The methods and approach to obtain reliable results from carrying-out DNA amplification on the passivation surface are described which should serve as a reference point to a future device aiming at diagnosing infectious diseases at the point-of-care.

[1] All molecular targets used here were provided and kindly prepared by Kenny Malpartida-Cardenas, Ivana Pennisi, Dr. Betty Ling-Shan Yu, George Alexandrou and under the supervision of Dr. Jesus Rodriquez-Manzano.

7.2 Motivation

7.2.1 Infectious Diseases

Infectious diseases pose a major threat to the global population, classified as a leading cause of death worldwide alongside wars and famine [10]. Broadly speaking, infectious diseases can be categorised into newly evolved strains of pathogens (e.g. multi-drug resistant tuberculosis), pathogens that have recently entered the human population (e.g. HIV1) and pathogens that have had presence in humans but have increased in incidence (e.g. Lyme disease) [11]. A combined of 334 infectious diseases have been reported between 1940 - 2004 [11]. Both the emergence as well as the spread of these pathogens cause a significant burden on global economies and public health. Such challenges are highlighted in low- and middle- income countries (LMIC) where nutritional deficiencies and inadequate hygiene increase the risk of disease contraction.

A key element in meeting the challenges of emerging infections lies in surveillance and response. This translates into rapid detection and diagnosis as well as containment within a population or environment. In developed countries, diagnostic tests are becoming increasingly automated and constitute a fundamental element of clinical practice. By reducing the turnaround times of lab tests, which are becoming integrated with digital medical records, patient care is improving [12]. Despite these advances, standard diagnostic technology is still inaccessible or prohibitive in resource-limited scenarios such as developing countries since such technologies are typically centralised, time-consuming, require specialized equipment and highly trained staff. In response, the UN (amongst others), has called for new diagnostic methods to operate in restricted environments such as Point-of-Care tests [13, 14]. Such tests can have a dramatic impact on the global response against diseases. Deploying rapid and PoC tests against just four infections (malaria, syphilis, tuberculosis and bacterial infections) has been estimated to prevent 1.2 million deaths worldwide [15].

7.2.2 Diagnosing infectious diseases

Overview

A limited number of gold standard methods exist to diagnose infectious diseases. Summarized in Table 7.1, these include cell cultures, antibody assays and nucleic acid amplification tests[2]. Various trade-offs exist for each method which tailor or disqualify a method with regards to an application.

[2]This table was kindly provided by Dr Jesus Rodriguez-Manzano.

Cell cultures provide a cost-effective way to diagnose an infection but are extremely time consuming, a prohibitive parameter in the case of PoC. On the contrary, molecular methods such as antibody assays and nucleic acid amplification tests are suitable candidates for rapid diagnosis but are more expensive and require highly skilled staff.

Table 7.1: Landscape of diagnostic methods for the detection and identification of infectious diseases.

Method	Analyte	Test Duration	Cost / test	SEN[a] (%)	SPE[b] (%)	PPV[c] (%)	QNT[d]	PoC Device	Ref.
Culture	Live Viral or bacteria	1-10 days	**£1-6**	∼ 83	∼100	∼100	**Yes**	No	[16]
Fluorescent - antibody assays	Antigen	1-4 hr	£2-7	∼ 50	∼95	∼94	**Yes**	No	[17]
Rapid Diagnostic Tests	Antigen	**15-30 min**	£10-20	20-70	90-95	6-93	No	**Yes**	[18]
Nucleic Acid amplification tests	DNA or RNA	15 min - 8 hr	£30-300	**98-100**	**98-100**	∼**100**	**Yes**	No	[19]

[a] SEN = Sensitivity (true positive = probability of positive result amongst those with the disease).
[b] SPE = Specificity (true negative = fraction of those without disease who give a negative result)
[c] PPV = Positive Prediction Value (probability of being infected among positive screening tests)
[d] QNT = Quantitative

Out of these methods, nucleic acid (DNA or RNA) amplification has emerged as a suitable candidate for PoC diagnosis which has the potential for compatibility with microchip technology. This technique relies on creating additional copies of the target DNA or RNA sequence present in a solution using either the Polymerase Chain Reaction (PCR) or Loop-Mediated Isothermal Amplification (LAMP) techniques. Therefore diagnosis is relatively straightforward with the occurrence of the amplification indicating the presence of the target nucleic acid sequence in the sample. Furthermore, not limited to a "sample-to-answer" method, this way allows for quantification of the sample i.e. estimating the number of copies present before amplification.

Nucleic Acid amplification

As previously mentioned, in the context of biology, amplification refers to the creation of additional copies of a genetic sequence. As a result, a specific sequence can be targeted which may indicate a gene, pathogen or other. Standard laboratory methods primarily rely on optical means to monitor the process of amplification and corresponding signal [20]. Identifying a target sequence is facilitated by the use of primers which are synthetic nucleic acid strands that are designed to bond with (and thus detect) the target.

Chronologically the first as well the most widely used method for amplification is the Polymerase Chain

Reaction [21]. This method was developed in the 1980s and enables the synthesis of DNA fragments using a DNA-polymerase enzyme used as a catalyst to synthesize the complementary sequence of the target. The target sequence to be replicated is specified by the use of primers, with each replication cycle doubling the amount of DNA copies present. This process is facilitated by a 3-step thermal cycling in the range of 50 to 95 ^{o}C. An initial high temperature of 95 ^{o}C breaks the hydrogen bonds between base pairs and opens the DNA double - helix. Subsequently, at a temperature between 50-65 ^{o}C the primers attach themselves on specific locations on the single strands, followed by a final stage at 72 ^{o} during which the polymerase enzyme extends the primers resulting into two double DNA strands. The overall result is the exponential creation of copies of a target sequence (amplifications) which can reach a very large number (e.g. 10^9).

In addition to PCR, several other methods have been invented such as nucleic acid sequence-based amplification (NASBA) [22], self-sustained sequence replication (3SR) [23], strand displacement amplification (SDA) [24] and loop-mediated isothermal amplification (LAMP) [25]. All of these methods take place in isothermal conditions which relax the requirements on temperature control and cycling. The most recent LAMP technique uses a DNA polymerase and a set of four primers which recognize a total of six different sequences on the target DNA. This method is based on strand-displacement of DNA which creates loops around which the target sequence is amplified. Compared to PCR, it has been reported as simpler due to removing the need for expensive equipment, faster, and more specific as more target-specific primers are involved [26].

Table 7.2: Qualitative comparison of PCR and LAMP

	PCR	LAMP
Temperature	Cycling 65 $\leftrightarrow$ 95 ^{o}C	Isothermal at 60-65 ^{o}C
Number of primers	2	4 to 6
Speed	✓	✓✓
Specificity	✓	✓✓

Opportunity for ISFETs

Independently of the amplification method used, detection has been traditionally carried-out using optical means by employing fluorescent primers or fluorescent nucleotides to create a fluorescently-labelled amplified target sequence [27]. This method offers many advantages such as high sensitivity, safety and in-parallel reactions as well as the ability to measure multiple fluorescent properties. Specifically, optical microscopes or cameras in conjunction with microarrays form the gold standard in DNA amplification detection where the fluorescent change from each well is monitored to quantify the

amount of amplification products. Such methods are labelled *quantitative* (qPCR / qLAMP) since the monitored signal is proportional to the amount of amplification.

Both qPCR and qLAMP rely on DNA polymerization which denotes the method of synthesizing DNA from a polymerase enzyme. On a fundamental level, this describes the process of a single DNA nucleotide (A,C, G, T) incorporating in an existing DNA strand. This reaction releases hydrogen ions [H^+] described by the following reaction [3]:

$$H_x dNTP + DNA \rightarrow DNA^{+1} + H_y PPi + H_z \tag{7.1}$$

where DNA represents the target strand DNA and $H_x dNTP$ represents any of the four triphosphate bases (dATP, dCTP, dTTP, dGTP). Hydrolysis and incorporation of the nucleotide results in an extended strand, represented as DNA^{+1}, pyrophosphate $H_y PPi$ and hydrogen ions, H_z.

A pH change is observed if there exists a proton disequilibrium across the two sides of the reaction i.e $z < x - y$ or $z > x - y$. Additionally, this change is regulated by the buffer capacity (β_{int}) of the solution. Overall the change in pH is given by:

$$\Delta pH = N \frac{H_z}{\beta_{int}} \tag{7.2}$$

where N denotes the total number of nucleotides incorporated during amplification. Evidently, the change in pH is proportional to the total number of nucleotide insertions and inversely proportional to the buffering capacity of the solution.

Traditionally when using optical means of detection, the reaction mix is kept in a well-buffered background with the pH remaining approximately constant at the beginning and end of the reaction. By modifying the reagent chemistries to a low buffered solution, a pH variation will be induced which indicates the occurrence of amplification as well as provides a quantitative result given by Eq. 7.2. As a result, this opens up the possibility of electronic sensing whereby ISFETs can be used to track the pH change during nucleic acid amplification. The expected modification in ISFETs is described by:

$$\Delta V_{chem} = \gamma + 2.3\,\alpha\,U_T\,N\,\frac{H_z}{\beta_{int}} \tag{7.3}$$

This equation can be used to qualitatively describe the amplification curve which follows an exponential profile. At the early stages of the reaction, the amount of protons generated is not enough to overcome the buffering capacity of the solution and could also be very small compared to the sensitivity of the sensing layer. Eventually, the amount of protons accumulated is enough for to show a detectable

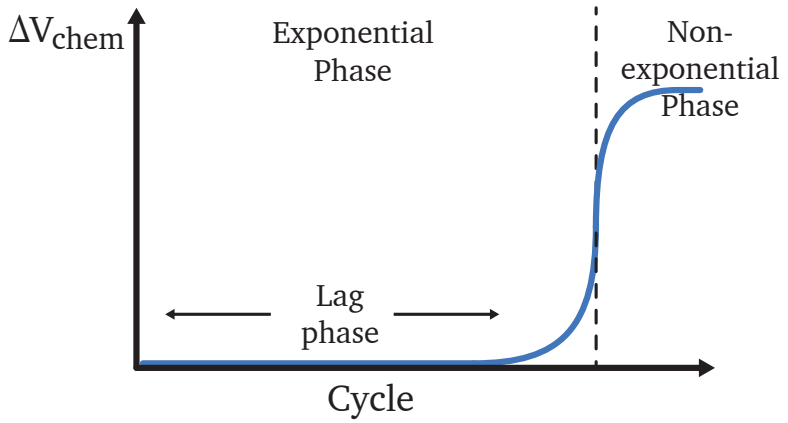


Figure 7.2: Qualitative demonstration of a nucleic acid amplification reaction. Figure redrawn from Supplementary Figure 2 in [3].

(exponential) signal as shown in Fig. 7.2. Subsequently and as the amount of reagents is exhausted, the reaction profile enters the non-exponential saturation stage and reaches a plateau. The polymerase activity contributing to the non-exponential phase and the completion of amplification is likely to be affected by the transition into suboptimal pH conditions.

The following sections outline the approach taken to conduct isothermal amplification (LAMP) on chip using one array from the TTN chip for monitoring pH changes. LAMP is suitable for electronic detection since running at a constant temperature prevents temperature transients in analogue signals. Additionally, its high specificity renders it an attractive choice for molecular diagnostics as it reduces the possibility of false positives. Finally, the time-to-positive (TTP) is extracted from the amplification data and it is correlated to the amount of initial DNA copies present (quantification).

7.3 Experimental Setup

To demonstrate the feasibility of the TTN system as a Lab-on-Chip platform, this section presents its application in real-time DNA amplification taking place in a microfluidic chamber on top of the chip. For this experiment, the acrylic manifold shown in Fig. 4.7a was replaced with one of open top such that the cartridge PCB can be inserted in a flat block PCR machine (Veriti Thermal Cycler, Applied Biosysems) for temperature control. Since LAMP was selected for amplification, the temperature is kept constant at 63 ^{o}C. From the TTN chip, the VM array was mainly selected for continuous monitoring of the solution due to its smaller size and faster frame readout. The average output of active pixels (pixels which lie in the linear range) was used as an indicator of changes in the solution pH.

A typical experiment was conducted in the following way:

1. The cartridge PCB with the chip and microfluidic manifold is prepared. Double-side adhesive tape with an opening of the size of the reaction chamber placed inbetween the manifold and chip prevents leakage of the reaction mix.
2. A 0.03mm diameter silver wire is chlorinated to obtain a Ag/AgCl reference electrode and subsequently inserted in the chamber (between the tape and manifold) to provide biasing. Due to its small diameter, sealing with adhesive tape is enough to prevent leakage. The voltage is externally controlled.
3. The chip's functionality and sensor responsiveness is evaluated by inserting de-ionized water in the chamber and varying the reference electrode voltage. A point which maximises active pixels is selected.
4. The temperature of the cartridge PCB and chip is raised to 63 ^{o}C using the Veriti Thermal Cycler and allowed to settle. A drop of mineral oil on top of the solution or a piece of plastic tape is used to cover the top of the reaction chamber in order to prevent evaporation.
5. In isothermal conditions, the de-ionized water in the reaction chamber is replaced with the reaction mix. The chip is continuously reading data from the selected array.

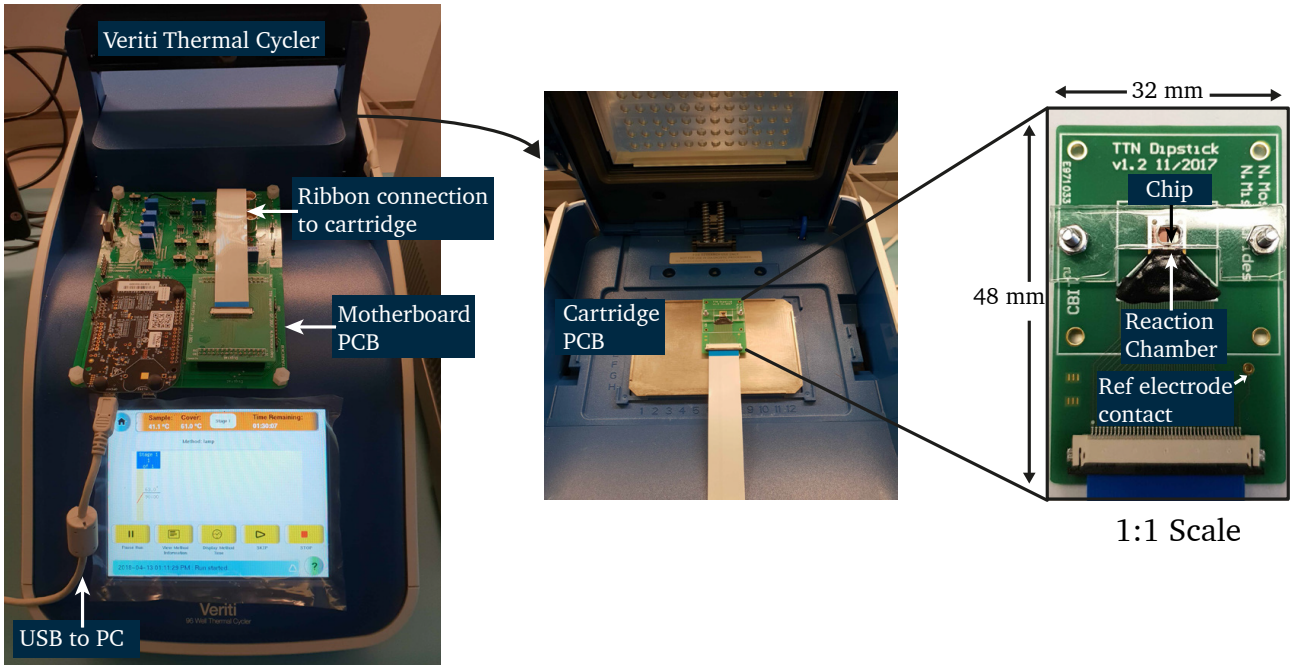


Figure 7.3: Measurement setup for the DNA amplification experiment

7.4 Results

As described in the previous sections, by modifying the solution chemistries during LAMP, it is possible to use the pH signal as an indicator of both the occurrence of amplification as well as a quantitative

measure of the DNA yield. Furthermore, the resulting pH change is *independent* of the target used. That means that virtually any DNA target can be selected for amplification assuming that suitable primers have been designed. During the course of optimizing the experimental setup for on-chip amplification, malaria targets have been primarily used and the method of obtaining the time-to-positive to quantify the initial DNA concentration is illustrated below.

A sample of other targets is shown in Appendix H.

7.4.1 Case study: Detection of Malaria

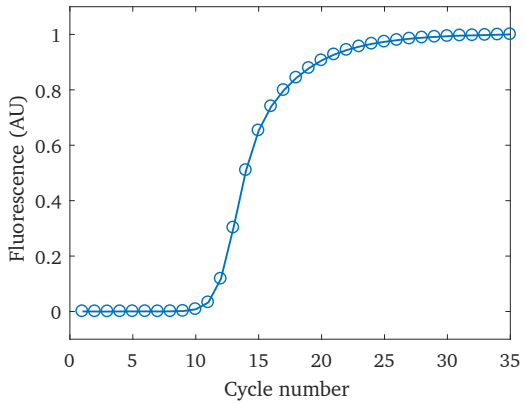
The target used here is *Plasmodium falciparum*, a human parasite and causative agent of malignant malaria [28]. It is transmitted through mosquito bites and is responsible for approximately 50% of all malaria cases which resulted in 435,000 deaths in 2017 [29].

Synthetic DNA of *Plasmodium falciparum* at different concentrations (10^3, 10^5 and 10^7 copies in 10 μL solution) was prepared in the lab and amplified on-chip. The time-to-positive has been extracted from which the relationship between initial concentration and TTP was derived. Subsequently, two clinical samples were amplified with an unknown initial concentration. Reactions were carried-out in parallel on the TTN platform and in a conventional real-time benchtop instrument (LightCycler 96 System, Roche) using fluorescence dye (SYBR green) for the detection of the dsDNA products. Fig. 7.4 shows both the on-chip and control responses.

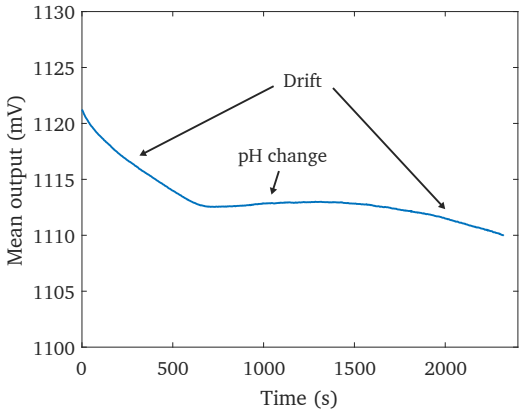
The expected lag-exponential-saturation behaviour was obtained both from the LC96 control reaction and on-chip. The main difference is that the chip output suffers from significant drift which appears as a slow monotonic change on the signal. After approximately 10 minutes, the reaction reaches its peak exponential phase which slowly saturates. Drift occurs throughout the reaction, nevertheless the rate of change of pH during amplification is higher therefore the signal is detectable.

7.4.2 Extracting Time-to-Positive

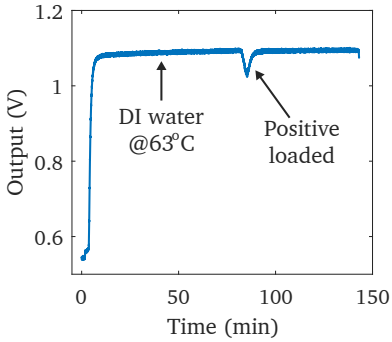
Despite the popularity of LAMP, metrics to quantify the outcome that can be used for comparison of results are still an active point of research. In benchtop instruments, such as the LC96, the metric indicating an amplification reaction is the Time-to-Positive which is obtained by using a threshold on the normalized fluorescent output. An alternative method in [30] uses an empirical logistic regression function, fitted on the sigmoid response obtained after amplification, to derive the TTP as the time when the initial response (during the lag phase) intersects with the linear extrapolation of the peak



(a) Normalized fluorescence output from the LC96 System.



(b) Mean output of exposed pixels in the VM array.



(c) Temperature profile during a complete experiment.

DNA Yield (ng/μl)		pH		
Pre	Post	Pre	Post	ΔpH
19.9	828	8.4	7.8	0.6

(d) DNA yield and pH change before and after amplification.

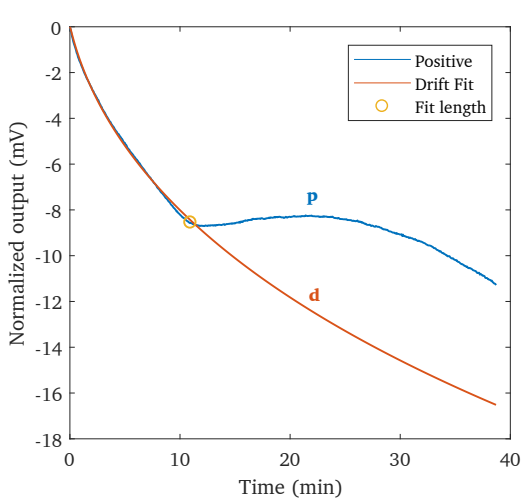
Figure 7.4: Typical output of DNA amplification in (a) the benchtop instrument and (b) on-chip. The target used here was *Plasmodium falciparum* at a 10^5 concentration of initial DNA copies. (c) shows the output recorded from the temperature sensor and (d) the details of the reaction.

exponential phase. A perfect sigmoid response obtained from an optical measurement instrument is assumed.

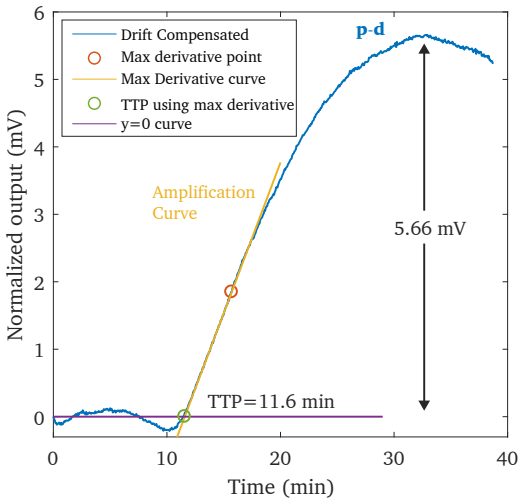
In this case, the same method as in [30] is adopted with the addition of a drift compensation step on the pH signal. Bold notation (e.g. $\mathbf{v}$) is used to indicate vectors or time series.

1. The pH signal $\mathbf{p}$ obtained from an amplification reaction is normalized by removing the DC component.
2. During the first minutes (< 10) after the sample is loaded, sensor drift is modelled using $\mathbf{d} = exp\left[\alpha - \left(\frac{\mathbf{t}}{\tau}\right)^{\beta}\right]$ where the scalar parameters α, τ and β are estimated.
3. $\mathbf{d}$ is extrapolated until the completion of the amplification reaction.
4. The drift-compensated response is obtained using $\mathbf{p} - \mathbf{d}$.
5. The inflection point is determined as the point of maximum derivative of $\mathbf{p} - \mathbf{d}$. A linear response is fitted around the maximum derivative point (amplification curve).
6. TTP is defined as the time when the amplification curve crosses t=0.

This process can be automated for the extraction of TTP in real-time. The only parameter programmed in advance is the number of samples used to fit drift (specified as Fit length in Fig. 7.5a).



(a) Drift signal modelled on the lag phase of the amplification signal. The drift model is extrapolated until the completion of the amplfication reaction.



(b) Drift-compensated signal. The TTP is obtained at the time when the max derivative curve crosses y=0. In this case TTP=11.57 min.

Figure 7.5: Illustration of the method deriving the Time-to-Positive.

Table 7.3 shows a summary of the reaction and comparison of the TTP with the one obtained in-parallel in the LC96 instrument. The resulting TTPs are 11.57 and 11.2 min for the on-chip and instrument respectively. Furthermore, the drift-compensated signal reaches a peak amplitude of 5.66 mV which corresponds to 0.61 pH using the sensitivity value in Table 4.3. In comparison, the pH readings obtained with a commercial pH meter before and post amplification indicate a change of 0.6 which

is in agreement with the measured. The resulting response conveys information both regarding the pH change due to the amplification as well as deriving the TTP. In comparison with standard PoC diagnostics which provide a binary answer indicating the presence of an infection, there is potential for quantifying the reaction i.e. provide a metric indicating the initial concentration of DNA copies.

Table 7.3: DNA Reaction Specifications

DNA Yield (ng/μl)		**pH**			**TTP (min)**	
Pre	Post	Pre	Post	ΔpH	on-chip	LC96
19.9	828	8.4	7.8	0.6	11.57	11.2

7.4.3 DNA Concentration Quantification

Using the same molecular target as the previous sections, the relationship between TTP and initial concentration of DNA copies is investigated further. The TTPs obtained after amplification of a concentration mix of 10^3, 10^5 and 10^7 are plotted against concentration. Two sets of concentration mixes (N) were prepared and conducted with $N = 2$ conducted on-chip and $N = 4$ conducted in the LC96 PCR instrument. The resulting responses are shown in Fig. 7.6 and indicate a linear relationship in both cases. As a result, this characterisation step can be used to estimate the concentration of an unknown sample.

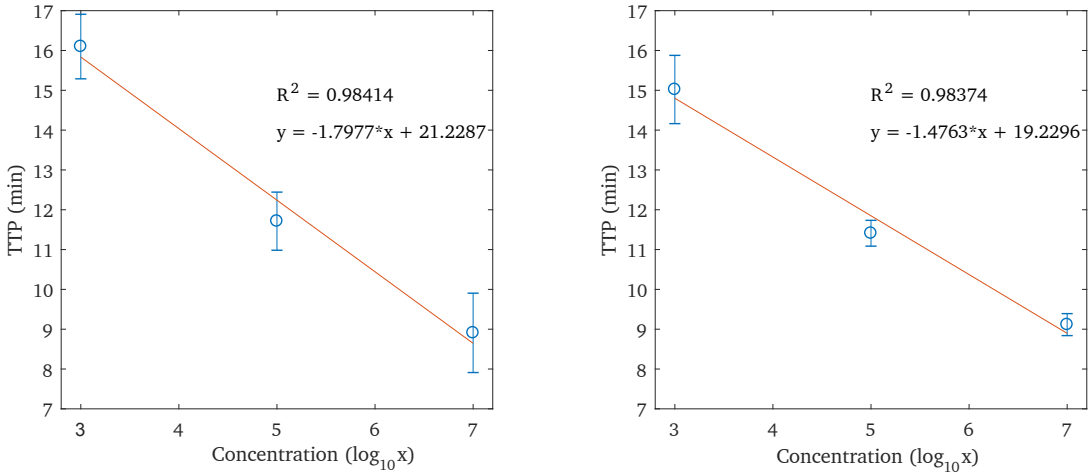
In Fig. 7.6, the error bars indicate the 95% confidence interval of the concentration resulting to that TTP. The confidence interval is obtained using standard methods of calculating statistics of an unknown population assuming that the sampling distribution is normally distributed:

$$\text{95\% limits} = \bar{y} \pm (SE \times 1.96) \tag{7.4}$$

where $\bar{y}$ equals to the sample mean, SE denotes the Standard Error and 1.96 correspond to the 0.975 quantile of the normal distribution. The standard error is calculated using:

$$SE = \frac{\sigma}{\sqrt{N}} \tag{7.5}$$

where σ is the standard deviation of the observations. The data from the on-chip experiments is shown in Table 7.4. Intuitively, the change in pH should correlate with the DNA yield (DNA concentration in $ng/\mu l$) however this relationship is not proven. Instead the average TTP for each concentration is shown in Table 7.5 which shows the same trend across both the sensing platform and the commercial LC96 instrument.



(a) On-chip reactions with N=2.

(b) LC96 reactions with N=4.

Figure 7.6: Time-to-Positive against concentration of DNA copies pre-amplification.

Table 7.4: Data from on-chip reactions

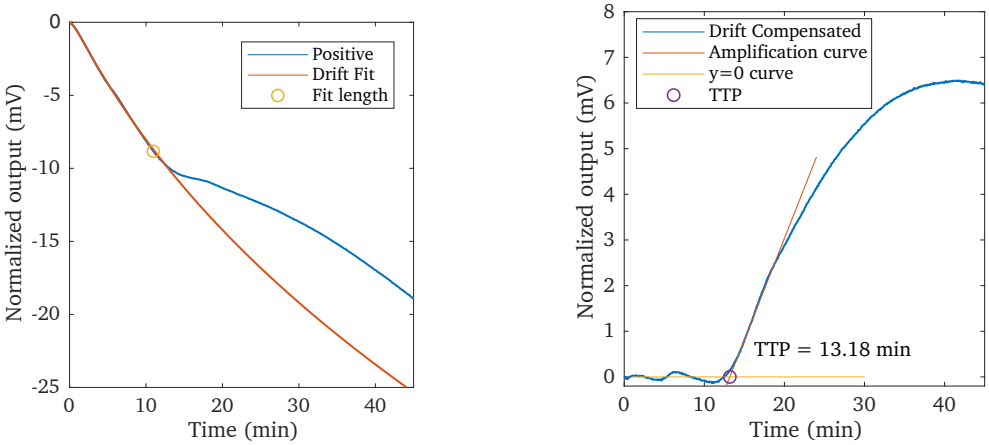
Conc.	**DNA Yield** ($ng/\mu l$)		**pH**		
	Pre	Post	Pre	Post	ΔpH
10^3	18.7	934	8.88	7.73	1.15
10^3 repeat	21.6	954	8.7	7.61	1.09
10^5	19.9	828	8.4	7.8	0.6
10^5 repeat	25.2	876	8.53	7.48	1.05
10^7	23.8	940	8.67	7.78	0.89
10^7 repeat	28.8	988	8.4	7.58	0.82

Clinical samples

Follow the characterisation step, reactions using clinical samples of unknown concentration were conducted both on-chip and on the LC96. The DNA targets were extracted from blood samples of malaria patients. Figures 7.7 and 7.8 show the results obtained after DNA amplification and Table 7.6 summarizes the results obtained. The method and characterisation curve outlined above, allows for estimating the initial copies per reaction contained in the sample.

Table 7.5: Comparison of Time-to-Positive between the on-chip reactions and the LC96 instrument.

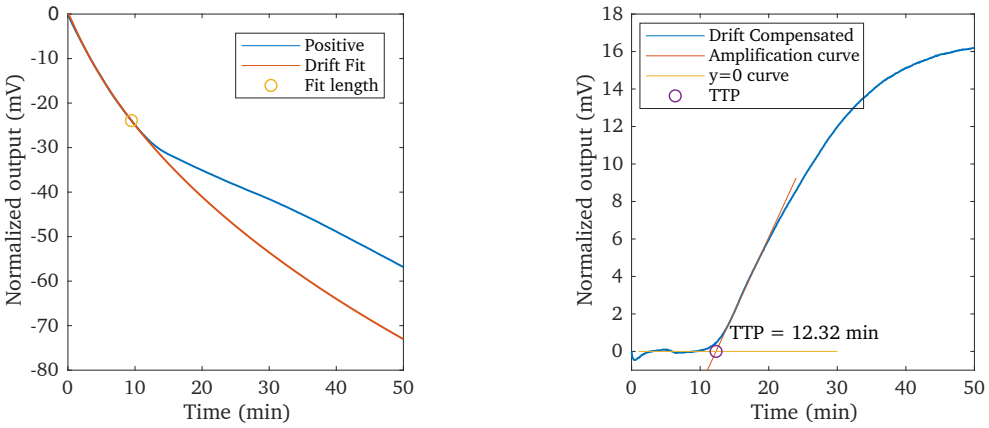
Mean Conc.	**TTP (min)**		**SE (min)**	
	on-chip	LC96	on-chip	LC96
10^3	16.10	15.02	0.41	0.44
10^5	11.71	11.41	0.37	0.17
10^7	8.91	9.12	0.51	0.14



(a) Raw signal and drift model.

(b) Drift compensated response.

Figure 7.7: Clinical malaria sample 1.



(a) Raw signal and drift model.

(b) Drift compensated response.

Figure 7.8: Clinical malaria sample 2.

Table 7.6: Results from clinical samples

	TTP (min)		**Estimated concentration**	
	On-chip	LC96	On-chip	LC96
Sample 1	13.18	13.17	1.27×10^4	3.04×10^4
Sample 2	12.32	13.42	4.79×10^4	9.03×10^4

Table 7.7: Summary of Pathogens Detected On-Chip

Gene	Species	Target	Sample Type*	Diagnosing
Kelch 13	*P. Falciparum* (parasite)	Whole gene	Synthetic + Clinical DNA	Malaria (type of disease)
Kelch 13	*P. Falciparum* (parasite)	Mutation (SNP)	Synthetic DNA	Artemisinin-resistant malaria
CYP51A	*Aspergillus fumigatus* (Fungus)	Tandem repeat (Wildtype)	Environmental (soil)	Azole-resistant mutations
NDM-1	*E. Coli* (bacteria)	Whole gene	Synthetic DNA	Resistance to carbapenems antibiotics
PIK3CA	Human Genome	Mutation (SNP)	Synthetic DNA	High propability of breast cancer
IFI44L	Human Genome	Whole gene	Clinical RNA	Human infection: Viral origin
EMR1	Human Genome	Whole gene	Clinical RNA	Human infection: Bacterial origin
PPIB	Human Genome	Whole gene	Clinical RNA	Reference gene: same expression in bacterial and viral infections.

* This field indicates the origin of the sample. *Synthetic* refers to an artificially-created nucleic acid sequence under lab conditions, *Environmental* refers to a sample obtained in the environment (non-animal origin) and *Clinical* refers to a target extracted from a human sample such as a blood sample.

7.5 Future extensions: Raspberry-Pi Diagnostics

As a first step towards expanding the capabilities of the current platform, a Raspberry Pi interface, including a custom board and Python-based GUI, has been designed and implemented.[3] The R-Pi platform is serves a double purpose:

- Improve portability of the current system towards a Point-of-Care implementation. This happens since data readout, data communication and visualization takes place on the same platform.
- Improve the current data readout process by reducing the number of steps. In this case, a faster communication protocol (than microcontroller-MATLAB through UART) has increased the readout speed from 3.2k pixels/s to 128k pixels/s.

Other portable implementations are typically carried-out using a smartphone application which results in a very slow readout and visualisation in batches [31]. Instead, the Raspberry Pi forms a trade-off

[3]The Raspberry Pi interfacing board and Python GUI presented here were designed by Mr Stefan Karolcik as part of this EEE M.Eng. final year project.

between a PC and smartphone and is still capable of real-time analysis and visualisation while ensuring portability and low cost. At higher readout speeds, faster dynamic transients during ionic concentration changes will be captured at a high resolution enabled by the dense arrays on the TTN chip.

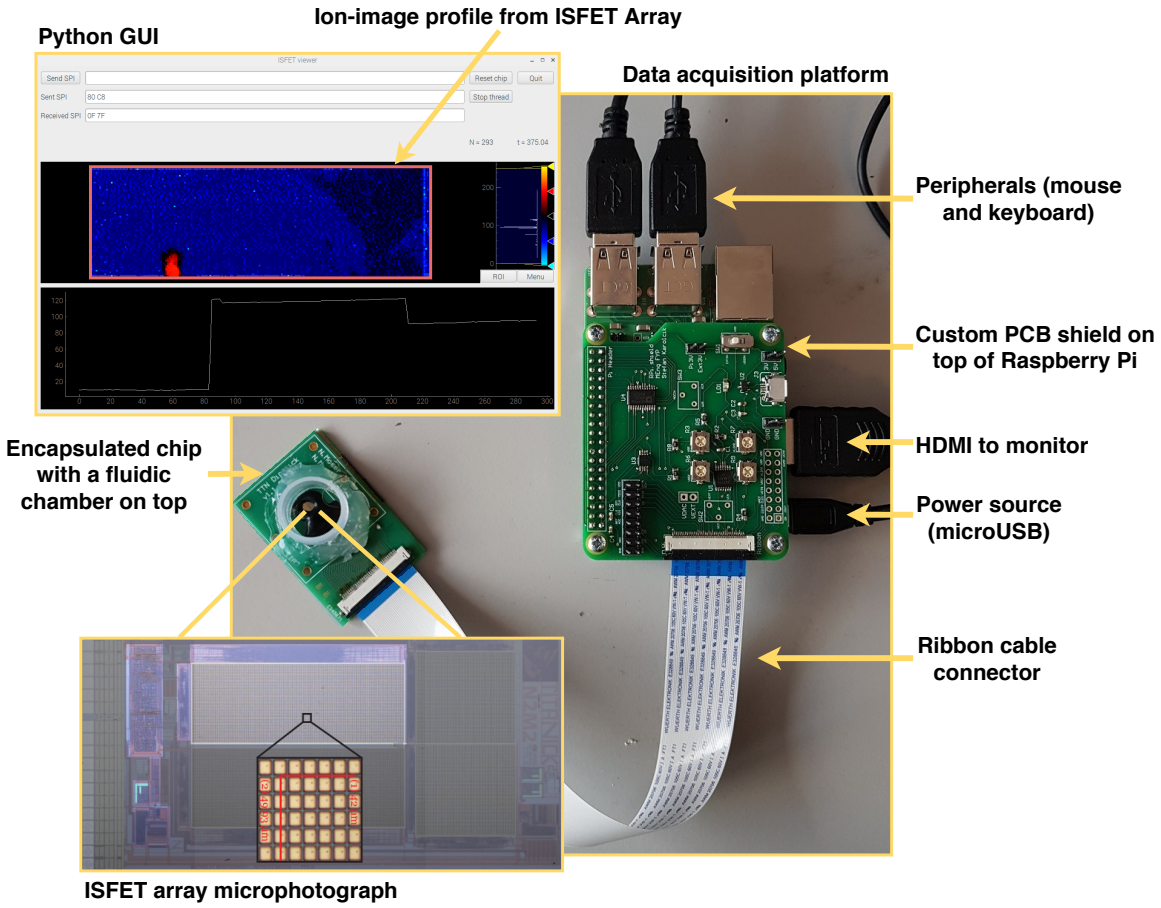


Figure 7.9: Raspberry Pi Platform and interface with the GUI shown in the top left.

7.6 Summary

This Chapter presented an approach and protocol for conducting DNA amplification on-chip with successful demonstration using a variety of targets. These results indicate that using ISFET sensors for conducting DNA amplification experiments is feasible even when using unmodified sensing substrate as opposed to commercial approaches which post-process the sensing surface. The biggest challenge here was to ensure operation at the presence of ISFET drift and trapped charge. For the former, a mathematical model was used to model drift during the course of a reaction which allows for deriving the drift-free response. For the latter, sensor redundancy is employed by using an array of ISFETs for sensing.

The work presented here has significant potential for further research in three directions. Firstly,

improving the portability of the platform used for sensing has the potential to be converted into a PoC device for running DNA amplification experiments on-the-spot (such as hospitals worldwide) by including embedded temperature control and a portable data processing system (such as a Raspberry Pi). Secondly, by improving on the microfluidic arrangement, additional chambers can be placed on the surface of the chip to exploit the sensor availability through the arrays as well as adding the capability of sensing more than one target (such as a set of infectious diseases) in-parallel. Thirdly, by leveraging the use of arrays once more, the potential for monitoring *spatially* a reaction is introduced. Current instruments only provide a single output therefore it would be a major breakthrough if the exponential phase of reaction was visualised spatially in the reaction chamber. This opens up the path for multi-dimensional diagnostics which is a field that recently obtained interest by showing that the amplification curve contains more information that just the indication of a positive reaction [32, 33].

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Chapter 8

Conclusion

8.1 Overview

This thesis introduced linear ISFET sensing in the current domain whereby direct pH-to-current transduction is exploited to obtain a scalable ISFET pixel with the opportunity for in-pixel offset compensation using the programmable-gate technique. Two large-scale ISFET arrays have been designed to demonstrate current-mode operation and are compared with an imager-inspired linear voltage-mode configuration. In-depth comparison of all topologies showed that current-mode outperforms the rest due to its small size, comparable noise and operation in velocity saturation which results in a detectable signal despite the increased capacitive attenuation.

Yet significant non-idealities exist which limit the full utilisation of ISFETs as the front-end of chemical sensing systems with the major ones being trapped charge and drift. An investigation into the mechanisms behind these effects showed that they are correlated and originate from defects in the structure of the sensing material. Based on an empirical relationship, a previously-employed technique for trapped charge modulation has been used to demonstrate trapped charge improvement as well as drift modification. This dependence predicts the existence of a drift free point for a given biasing condition. As a result, it is evident that the co-existence of these two phenomena merits additional research with a focus on deriving a complete behavioural model. Nevertheless, it has been shown here that trapped charge modulation is a method that can be used to minimize drift. Furthermore, in order to minimize the effect of trapped charge, a calibration algorithm has been proposed to reduce mismatch and push as many sensors as possible to operate in the linear instrumentation range.

Lastly, ISFET arrays detecting and measuring DNA amplification reactions have been demonstrated, which hold significant potential due to the combination of amplification chemistries (resulting in

a pH signal) and electronic means of detection. As a result, ISFET sensing can be used to detect molecular targets, subject to suitable primers, with demonstrable results in the diagnosis of infectious diseases whereby the speed and accuracy of detection has been recognised as major enabler for death prevention.

8.2 Contributions

The novel contributions included in this thesis are outlined below:

- A novel topology for ISFET-based pH-to-current has been proposed and pixel design considerations have been identified. This is achieved by biasing in velocity saturation resulting in a constant biasing circuit topology which fixes the ISFET terminals and monitors the drain current.
- The first ISFET array biased in velocity saturation has been demonstrated which demonstrates the benefits of current-mode operation to facilitate ion imaging with perfectly linear pH-to-current conversion using a a simple and area-efficient pixel topology.
- To implement a method for offset compensation, a programmable-gate capacitor has been included inside the pixel without compromising the pixel's area. This has been achieved by implementing the capacitor as the parasitic capacitance between two interleaved metal structures located inside the pixel stack. A method for determining the exact value of that capacitance has been derived.
- A voltage-mode array based on a source-follower configuration has been designed on the same chip as the two current-mode ones. This has enabled a direct comparison since the sensing layer is shared and a determination of the benefits and limitations of each topology captured in a newly defined FoM.
- A investigation into the Si_3N_4 the sensing layer showed a correlation between trapped charge and drift. This relationship was explored further by controlled UV irradiation to modify the trapped charge which resulted into drift modification. Additionally, drift has been shown to depend on the average electric field across the insulator thus the combination of these two effects has the potential for drift-free measurements using cyclic biasing during readout.
- A gradient-descent calibration scheme has been proposed and implemented which predicts the step size for error minimization and approximates the optimum point in one iteration step. A previously proposed calibration algorithm has been expanded to include a dynamic convergence point.
- A test setup for on-chip DNA amplification has been demonstrated with successful detection of

various molecular targets. Furthermore, a method for drift compensation based on parameter fitting on a custom model has been shown as a reliable way to extract the Time-to-Positive metric. TTP can be used to predict an unknown DNA concentration on top of being a molecular biomarker on its own (e.g. in the case of discriminating bacterial vs viral infections).

8.3 Discussion

Following the list of processes, protocols and experiments described here, it is evident that designing ISFET-based circuits and systems is the result of various trade-offs which manifest in all aspects of circuit-design down to material physics. Presumably all aspects touched upon in this thesis can be the focus of further research with aims such as making circuits robust to extreme offsets or improving the quality of passivation deposition to minimize defects. Nevertheless, in this case, it is demonstrated that by making suitable trade-offs whenever appropriate and simplifying processes/mechanisms it is possible to ensure a degree of robustness in practical applications. Hence the title of this thesis which emphasizes the novel contribution in terms of current-mode chemical sensing as well as methods for optimization, describing the trade-offs ubiquitous with ISFETs.

Maximizing robustness in a commercially available process is the first major issue to be addressed. Chips for prototyping purposes, originating in academia, have avoided post processing and primarily relied on circuit or instrumentation methods to meet the challenges of a non-ideal sensing layer. On the contrary, commercial solutions opted straight away for repassivation with a better quality oxide. This has served in keeping pixel sizes small and is aligned with modern imagers where the design trend follows simple pixel topologies, wafer-level post-processing (e.g. thinning the wafer in back-illuminated imagers) and signal processing for compensation. Along theses lines, current-mode processing allows for very small (2T) pixels which achieve a large linear range through biasing in velocity saturation and using a process with a large V_{DD}. Consequently, a simple pixel topology was adopted at the expense of carrying-out all signal processing at a later stage. Yet, even with uncompensated pixels, only a minority of extreme cases of trapped charge rendered pixels unusable.

Moving forwards towards increased adoption of ISFET-based front-end for integrated chemical sensing designed in advanced (deep sub-micron) CMOS processes (with limited analogue dynamic range), it is imperative that the uncertainty regarding the passivation layer reduces. This can happen through chip post-processing and repassivation which ultimately increases cost. Alternatively, foundries should be made aware of the new role of the passivation in this field. Suitable incentives can serve to improve passivation recipes with an immediate impact in sensing.

Despite the major issues, ISFET-based solutions have been increasingly explored in the literature both in the area of sensing instrumentation as well as novel applications. With new areas emerging such as ultra-fast ion imaging, multi-ion analytics and point-of-care sensing it is clear that finding the best trade-offs and optimizing the methods and apparatus, hold the key for successful solutions. This research helps in improving our understanding in making design decisions and aids in revealing some of the potential lying at the intersection of disciplines and ideas.

8.4 Recommendations for Future Work

Following or based on this work, some research paths for future work are outlined below:

8.4.1 Scaling and circuit improvement

In general, there are two approaches in ISFET pixel design: a simplified analogue front-end with digital conversion at the earliest point leaving signal processing at a computer level or an elaborated analogue front-end with in-pixel compensation and/or calibration. The first method has been adopted here yet what both approaches have in common is that they are subject to technology scaling which can be leveraged towards scaling. Moving towards an ultra-large-scale platform for sensing introduces additional considerations regarding power consumption, uniformity across the array and complicated processing. For instance, scaling the current-mode array to 1 billion sensors is unrealistic without considering the impact on linearity, linear range, array scanning rate and most importantly the deviations across sensors due to loading on the signal buses. Redesign of the peripheral circuits with a view on feedback on the output bus and parallelization (e.g. row/column level) processing is needed to scale both in pixel size as well as process. Nevertheless, moving to a deep sub micron process is feasible and aligned with the target operating region in velocity saturation.

8.4.2 Improved communication interface

At the moment, a microcontroller acts as an intermediary node in-between the chip and a computer which handles data transfer between a MATLAB-based interface and the chip. Additionally, several algorithms have been presented such as calibration or extracting the time-to-positive which are communication intensive and limited by the implementation platform (in this case microcontroller). By improving the data interface, it is possible to obtain much faster communication and thus array recording speed. In the case of velocity saturation, 1 μs/pixel is well inside the worst case settling time

whereas by sampling and communicating to a PC through UART, the final recording time increases to 200-300 μs/pixel. Therefore, a custom-built interface including high speed ADCs has the potential of very fast array scans with a theoretical maximum of 78 fps with this settling time. With a view on portability, higher array raster scans are possible by using a basic computer such as a Raspberry Pi to handle SPI communication, data transfer as well as data processing on-board. This way enables portable ion imaging yet has more processing power than smartphone based solutions.[1]

8.4.3 Towards a complete drift model

Further experiments and investigation into the mechanisms behind drift will serve to increase our understanding on the fundamental processes behind these phenomena in amorphous materials. This includes a discrimination between drift caused by capacitance change and that caused by ionic diffusion resulting in charge change. Additionally, the impact of the electric field is not well understood and empirically accelerates or decelerates theses changes. For this reason, new test structures on a different chip have been sent for fabrication including contacts with and without ISFETs around the passivation layer. Hence, the capacitance of that layer can be measured as well as the electric field.

8.4.4 Improved Lab-on-Chip design

The microfluidic configurations used here were designed and built in-house using available technologies. By improving the manifolds used, it is possible to further exploit the use of arrays for sensing using more than one chambers for in-parallel reactions. This has potential both in running positive and negative reactions concurrently as well as allowing for the detection of more than one pathogens simultaneously. A challenge associated with this method will be the placement of the reference electrodes that may need to bias each chamber individually.

[1] First steps towards this approach, including a Raspberry Pi interface for communicating with the TTN chip, have been made by Stefan Karolcik as part of his MEng project and early work in PhD.

Appendix A

List of Publications

Included here

Journal Papers

- N. Miscourides, L. Yu, J. Rodriguez-Manzano and P. Georgiou, "A 12.8 k Current-Mode Velocity-Saturation ISFET Array for On-Chip Real-Time DNA Detection," in *IEEE Transactions on Biomedical Circuits and Systems*, vol. 12, no. 5, pp. 1202-1214, Oct. 2018.
- N. Miscourides and P. Georgiou, ""ISFET Arrays in CMOS: A Head-to-Head Comparison Between Voltage and Current Mode," in *IEEE Sensors Journal*, vol. 19, no. 4, pp. 1224-1238, 15 Feb.15, 2019.

Conference Papers

- N. Miscourides and P. Georgiou, "Linear current-mode ISFET arrays," *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, Montreal, QC, 2016, pp. 2827-2830.
- N. Miscourides and P. Georgiou, "A linear programmable-gate ISFET array operating in velocity saturation," *2016 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, Shanghai, 2016, pp. 292-295.
- N. Miscourides and P. Georgiou, "Mismatch compensation in ISFET arrays using a parasitic Programmable Gate," accepted in *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, Sapporo, 2019.

Other papers

- N. Miscourides and P. Georgiou, “Impact of Technology Scaling on ISFET Performance for Genetic Sequencing,” in *IEEE Sensors Journal*, vol. 15, no. 4, pp. 2219-2226, April 2015.
- W. Xiao, N. Miscourides and P. Georgiou, “A novel ISFET sensor architecture using through-Silicon vias for DNA sequencing,” *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, Baltimore, MD, 2017, pp. 1-4.
- K. Elmantawi, N. Miscourides, E. Koutsos and P. Georgiou, “A 96-channel ASIC for sEMG Fatigue Monitoring with Compressed Sensing for Data Reduction,” *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, 2018, pp. 1-5.
- J. Zeng, N. Miscourides and P. Georgiou, “A 128x128 Current-Mode Ultra-High Frame Rate ISFET Array for Ion Imaging,” *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, 2018, pp. 1-5.
- K. Malpartida-Cardenas, N. Miscourides, Ling-Shan Yu, Jake Baum, J. Rodriguez-Manzano and P. Georgiou, “A CMOS-based diagnostic system for detection of artemisinin-resistant malaria”, *2018 International Conference on Miniaturized Systems for Chemistry and Life Sciences (uTAS)*, Kaohsiung, 2018.
- S. Karolcik, N. Miscourides and P. Georgiou, “Live demonstration: A Portable High-Speed Ion-Imaging Platform Using a Raspberry Pi,” 2019 IEEE International Symposium on Circuits and Systems (ISCAS), Sapporo, 2019.

Appendix B

Fabricated Chips

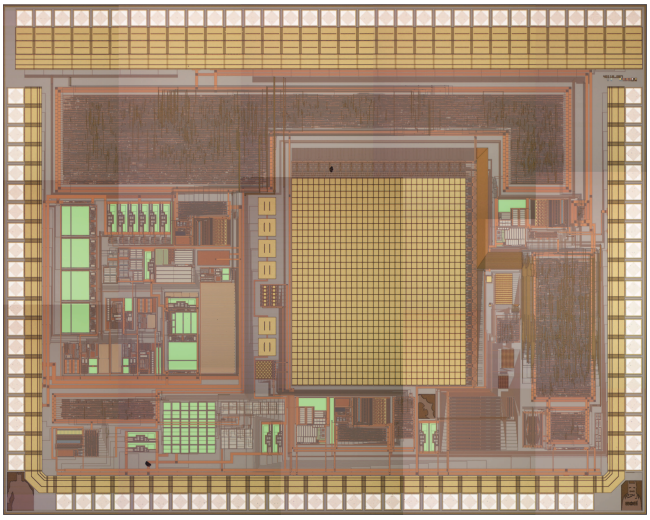


Figure B.1: BATMAN (2015): Three 16×16 ISFET arrays including a current-mode (triode region biasing) topology, a current-mode (velocity saturation biasing) topology and a voltage-mode (source-follower) topology.

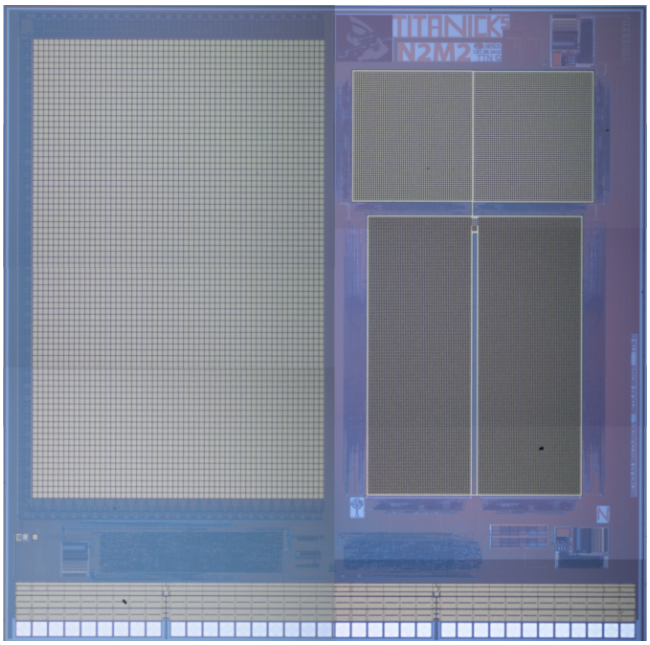


Figure B.2: TITANICKS v1 and v2 (2016&17): Four ISFET arrays including a 64×200 current-mode (VS biasing) topology, a current-mode (VS biasing and PG) topology and two 64×64 voltage-mode (source-follower) topologies.

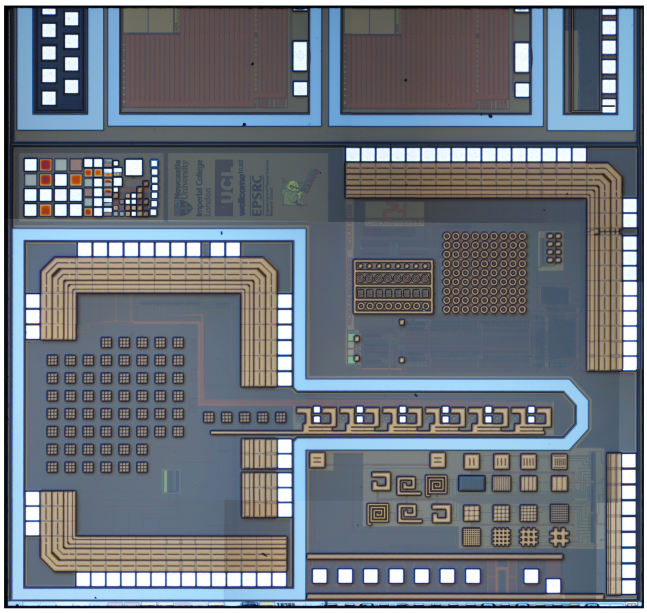


Figure B.3: Chip 24 (2016): Test current conveyor and test ISFET devices of various passivation capacitances.

Appendix C

Algorithms and Methods

C.1 Determining shift and scale on from an ISFET's I-V characteristics

The following algorithm is used to determine the capacitive attenuation and trapped charge of an ISFET by obtaining its $I_D - V_{ref}$ characteristics (X_{est}) and comparing with the corresponding $I_D - V_{GS}$ of a simulated MOSFET (X_{sim}). The algorithm works by assuming that a linear transform can be used to obtain X_{sim} from X_{est}, such that:

$$X_{sim} = \alpha X_{est} + \beta \tag{C.1}$$

where α corresponds to the attenuation due to the passivation capacitance and parasitics (or scaling) and β corresponds to the offset (or shift) due to trapped charge. Interestingly, the scaling term obtained is different from the scaling term previously described in the literature since that assumes biasing in weak inversion[1]. Since the magnitude of the parasitic capacitances depends on the biasing region of the device, a similar yet not identical attenuation term is obtained. As a result, fitting the response in this case will be valid in the velocity saturation region where the $I_D - V_{GS}$ relationship is linear and will show a slight deviation in the other regions of operation. A demonstration of the algorithm is shown in Fig. C.1.

C.2 Calculating magnitude of parasitic programmable-gate capacitance

To estimate the parasitic C_{CG}, consider that the charge equilibrium at the floating gate is established through a weighted sum of the surrounding voltages, with the weights given by the corresponding

[1] P. Georgiou and C. Toumazou. "ISFET characteristics in CMOS and their application to weak inversion operation". In: Sensors and Actuators B: Chemical 143.1 (2009), pp. 211–217.

Algorithm 4: Curve Fitting of I-V sweeps

Data: X_{est}: approximation; X_{sim}: reference curve
Result: X_{est}
begin
  Find derivatives (g_m) of X_{est} and X_{sim}
  Find most linear range (flat) around derivative such that **lin_range =** $\pm$**5%** of peak g_m
  Find gradient of best fit line in **lin_range**
  Scale = (gradient of best fit line in X_{est}) / (gradient of best fit line in X_{sim})
  Find maximum gradient points after scaling
  Shift = x-axis difference of the maximum gradient points
end

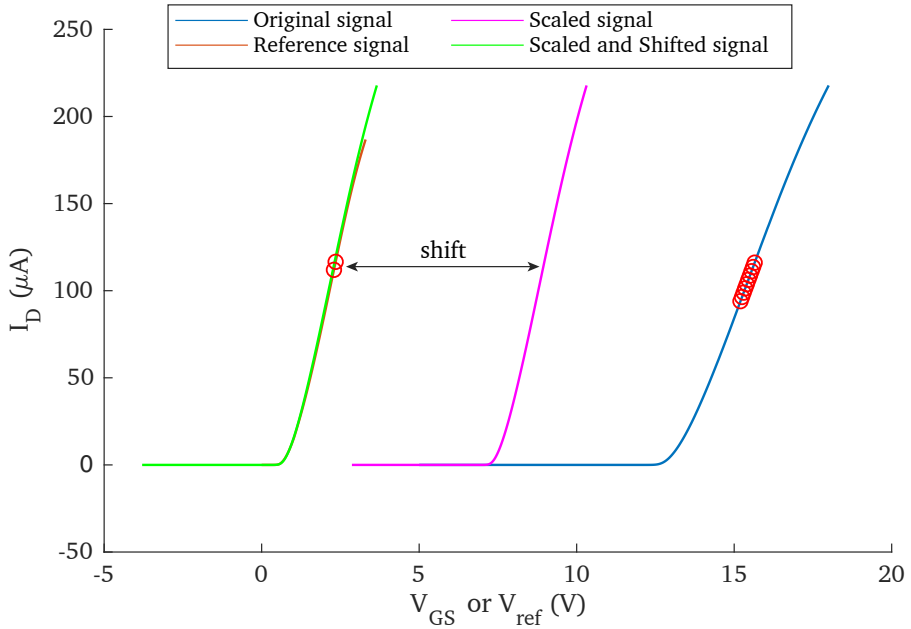


Figure C.1: Algorithm demonstration for an experimentally obtained current-mode $I_D - V_{ref}$ fit. The red circles indicate the regions of maximum linearity i.e. flat g_m, which have been used to determine the **scale** term.

capacitances. Therefore, the following equations describe V_{FG} with and without the control gate capacitance C_{CG}, which correspond to the CM and CM-PG pixels. The floating gate voltages of the devices shown in Figs. 2.3 and 3.8, are described by:

$$V_{FG,CM} = \frac{C_{pass}V_{G'} + C_{gd}V_D + C_{gs}V_S + C_{gb}V_B}{C_{T,CM}} \tag{C.2}$$

$$V_{FG,CM-PG} = \frac{C_{pass}V_{G'} + C_{gd}V_D + C_{gs}V_S + C_{gb}V_B + C_{CG}V_{CG}}{C_{T,CM-PG}} \tag{C.3}$$

where C_T denotes the total capacitance seen at that node.

The following assumptions can be made in order to simplify the calculations:

1. *The source voltage* $V_S = 0\,V$. This is true for the pixels shown in Figs. 3.6a and 3.9a since when the column switch is ON, the source voltage is essentially shorted to ground through a small (triode region) resistance.
2. C_{gd} *is very small.* C_{gd} is typically the smallest from the parasitic capacitances by at at least an order of magnitude[2].
3. C_{gb} *is very small*. C_{gb} is small compared to C_{gs} and also decreases in magnitude when moving from weak to strong inversion which is our intended operating region.

As a result, Eqs. C.2 and C.3 can be approximated with the ones shown below.

$$V_{FG,CM} = \frac{C_{pass}}{C_{T,CM}} V_{G'} \tag{C.4}$$

$$V_{FG,CM-PG} = \frac{C_{pass}V_{G'} + C_{CG}V_{CG}}{C_{T,CM-PG}} \tag{C.5}$$

with $C_{T,X}$ defined as below:

$$\begin{aligned} C_{T,CM-PG} &= C_{CG} + C_{T,CM} \\ C_{T,CM} &= C_{pass} + C_{gg} \\ C_{gg} &= C_{gs} + C_{gd} + C_{gb} \end{aligned} \tag{C.6}$$

The corresponding attenuations have been experimentally measured and are given by:

$$\frac{V_{FG,CM}}{V_{G'}} = \frac{C_{pass}}{C_{pass} + C_{gg}} = \zeta = 0.5727 \tag{C.7}$$

$$\frac{V_{FG,CM-PG}}{V_{G'}} = \frac{C_{pass}}{C_{pass} + C_{gg} + C_{CG}} = \xi = 0.387 \tag{C.8}$$

Hence

$$\begin{aligned} C_{CG} &= C_{pass}\left(\frac{1}{\xi} - \frac{1}{\zeta}\right) \\ &= 0.8379 \times C_{pass} \\ &= 0.9596\,fF \quad \text{using the CM and CM-PG calculated value of } C_{pass} \end{aligned} \tag{C.9}$$

For verification, consider deriving the V_{FG} sensitivity to V_{CG}:

$$S_{V_{CG}} = \frac{dV_{FG}}{dV_{CG}} = \frac{C_{CG}}{C_T} = 0.328 \tag{C.10}$$

[2]Y . Tsividis, “Mixed Analog-Digital VLSI Devices and Technology.” NY:McGraw-Hill, 2002.

With this result, a $1\,V$ change of V_{CG} will modify V_{FG} by $328\,mV$. Assuming $g_m \approx 100\,\mu S$ in velocity saturation for a CM pixel (simulated peak $g_m = 100.9\,\mu S$), this V_{FG} change corresponds to a $32\,\mu A$ change in I_D. Evidently, from Fig. 4.17b, the measured value is $30.4\,\mu A/V$.

C.3 UV Irradiation Process

Before using UV irradiation for matching the transconductance characteristic of ISFETs, it was used for the erasing of EEPROM memory. The energy required for photoemission from the Si valence band to the SiO_2 conduction band is 4.3 eV and the energy required for photoemission from the Si conduction band to the SiO_2 conduction band is 3.2 eV. In Si_3N_4, the bandgap of LPCVD was found greater than 5.5 eV. Nevertheless, lasers with a photon energy of 4.1 eV showed removal of trapped charge in [27, Ch 5]. The illumination study showed that paramagnetic neutral silicon dangling bonds can capture either electrons or holes as shown below:

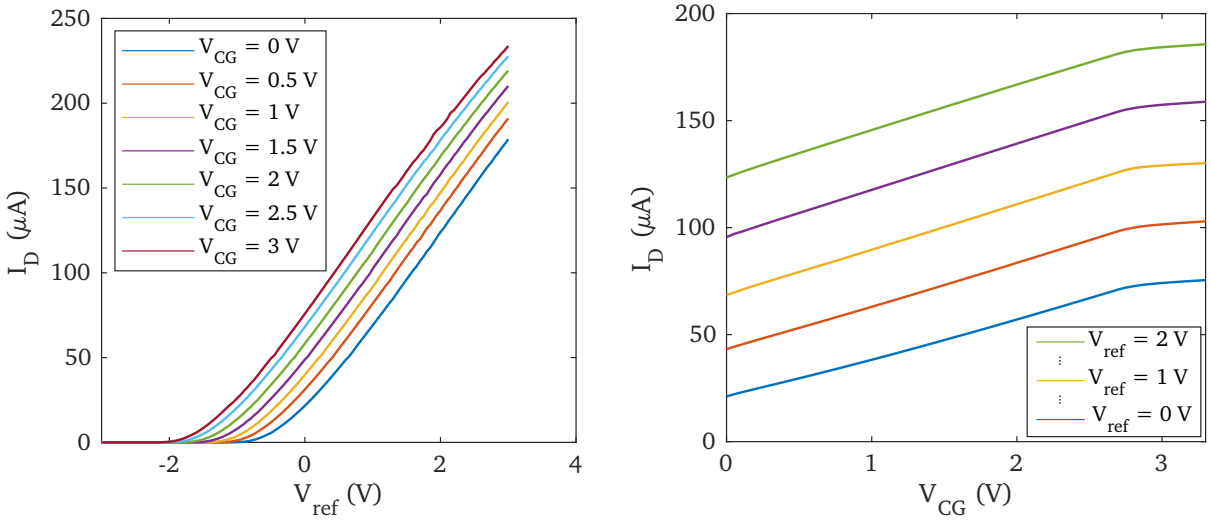
$$K_0 + e^- \overset{UV}{\longleftrightarrow} K^- \tag{C.11}$$

$$K_0 + h^+ \overset{UV}{\longleftrightarrow} K^+ \tag{C.12}$$

where K_0 is a neutral paramagnetic centre and e^-/h^+ are the electron and hole carriers. It was suggested that UV illumination annihilates trapped charge in the silicon nitride but also increases the density of the paramagnetic silicon centres.

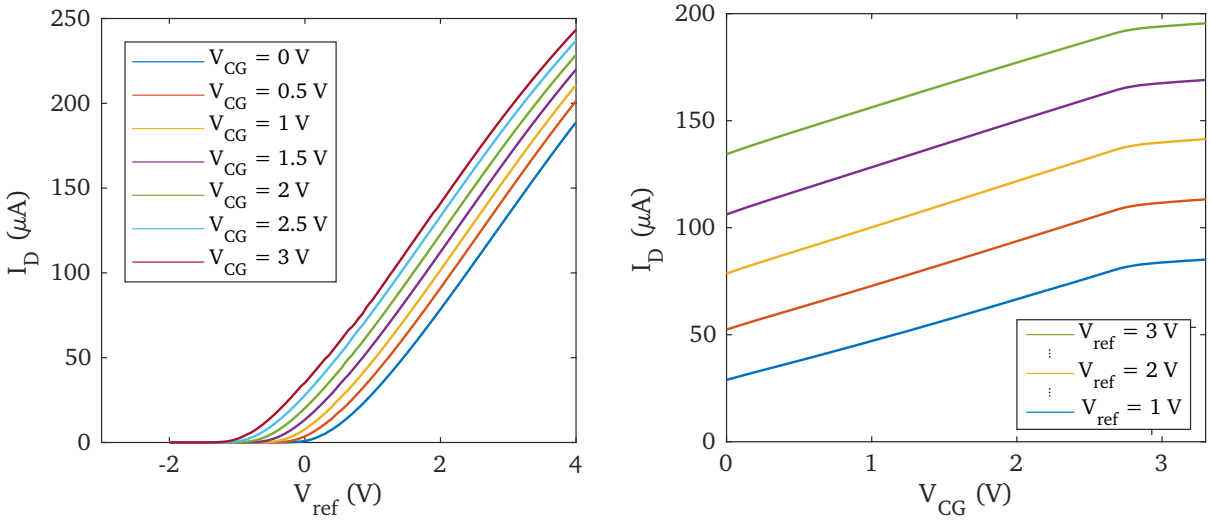
In this case, top metal was used to entirely cover the polysilicon ISFET gate with other metal layers / signal buses also placed inside the pixel stack. Therefore, it is reasonable to assume that trapped charge in the poly-S gate is unaffected by UV irradiation. An off-the-shelf LED (Marl 260019) was used for irradiation with an output in the UV spectrum ($\lambda = 370\,nm$) at $10\,mA,\ 1\,mW$ forward current. This corresponds to a photon energy of 3.35 eV. The LED has a 110^o viewing angle and was placed at $\sim 1\,cm$ distance from the surface of the chip targeting the intersection point of all four arrays. Both the LED and chip (on the cartridge PCB) were fixed on a plane with the irradiation and were left for a minimum of 16 hrs of continuous irradiation.

Fig. C.2 shows the modification obtained on the I-V characteristics of a test CM-PG sensor after 16 hours of irradiation. The I-V characteristics (at various V_{CG} sweeps) were shifted by approximately $1\,V$ towards expected characteristics.



(a) $V_{ref} - I_D$ Pre UV

(b) $V_{CG} - I_D$ Pre UV



(c) $V_{ref} - I_D$ Post UV

(d) $V_{CG} - I_D$ Post UV

Figure C.2: Modification of the I-V characteristics on a test sensor of the CM-PG topology following 16 hrs of UV irradiation.

Appendix D

Lessons Learned

- ISFETs are depended on and limited by the sensing material. In the case of a binary sensing outcome (Yes/No indicating an amplification reaction) poor quality can be tolerated quite well. However, to ensure high pH resolution, some control over the material quality is beneficial. That could be through informed foundry selection or in-house repassivation as a form of post-processing.
- Vast majority of imagers undergo some post-processing before being used commercially. Hence, the real barrier in ISFETs is cost.
- The capacitive attenuation observed with ISFETs, which discourages the design of very small pixels, is not a major issue. Signal is still large enough (order of μA or mV) compared to other electronic applications. The real problem is offset and drift; hence a better sensing material will make smaller pixels even more attractive.
- When working with poor quality Si_3N_4, as is the case here, the best workaround against drift is sensor burning time. Leave the sensors in pH 7 or DI water for half an hour before starting measurements. Effectively avoiding the initial fast phase of the stretched-exponential behaviour.
- ISFET chips are used in an unorthodox way. Instead of hermetically sealed, they are brought into contact with an aqueous solution. Therefore, the quality of encapsulation is crucial and is the single biggest factor determining a chip's lifetime. If encapsulating by hand, add epoxy covering at least $\sim 300\,\mu m$ from the sides of the chip. Also, fresh and well mixed epoxy works best.
- Various microfluidic configurations were presented and used in the literature to facilitate a pH change / solution flow on the surface of the chip. In practice, the smaller the better. Apart from minimizing the amount of pH buffers used, having inlets/outlets in close proximity to the surface means that the new solution will actually displace the previous. Otherwise, it is impossible to know whether the solution has changed or locally mixed.

Appendix E

Supplementary Block Characterisation

E.1 Current Conveyor

The current conveyor block constitutes a major block in the CM pixel pipeline and is characterized on its own. Initially characterisation has taken place at the nominal voltage of the drain bus $V_D = 1.5\,V$. As shown in Fig. E.1, for increasing pixel current I_{pixel}, V_{DR} is struggling to staying constant and reduces to $\sim 1.4\,V$ at $I_{pixel} = 200\,\mu A$. Nevertheless, due to the large output impedance of the cascoded topology, the mirrored current I_{out} follows precisely I_{pixel} even though the I_{out} node is held constant at $2\,V$ to mirror the TIA on the chip.

Furthermore, Fig E.2 shows the measured responses for a range $1 \leq V_D \leq 2\,V$. As V_D and I_{pixel} increase, the current conveyor reaches the limits of its voltage headroom and the drain bus potential V_{DR} drops.

E.2 Temperature Sensor

The PTAT temperature sensor on the TTN chip has been characterised by placing the cartridge PCB inside a flat block PCR machine (Veriti Thermal Cycler, Applied Biosystems) which is employed here as the temperature controller. A temperature profile of $30 - 100^oC$ was programmed with a step of 10^oC. Sufficient time was allowed at each temperature (10 min) in order for the heat to propagate from the PCB to the chip and $15\,\mu L$ of solution in the microfluidic chamber. The overall sensor response is shown in Fig. E.3 with a measured sensitivity of $15.1\,mV/^oC$.

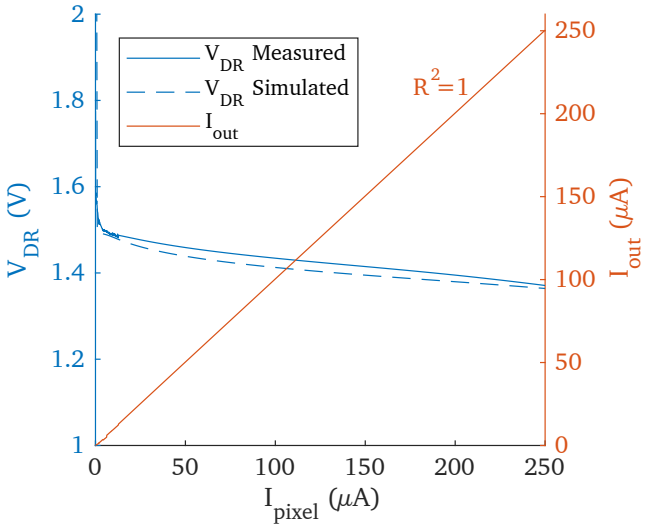
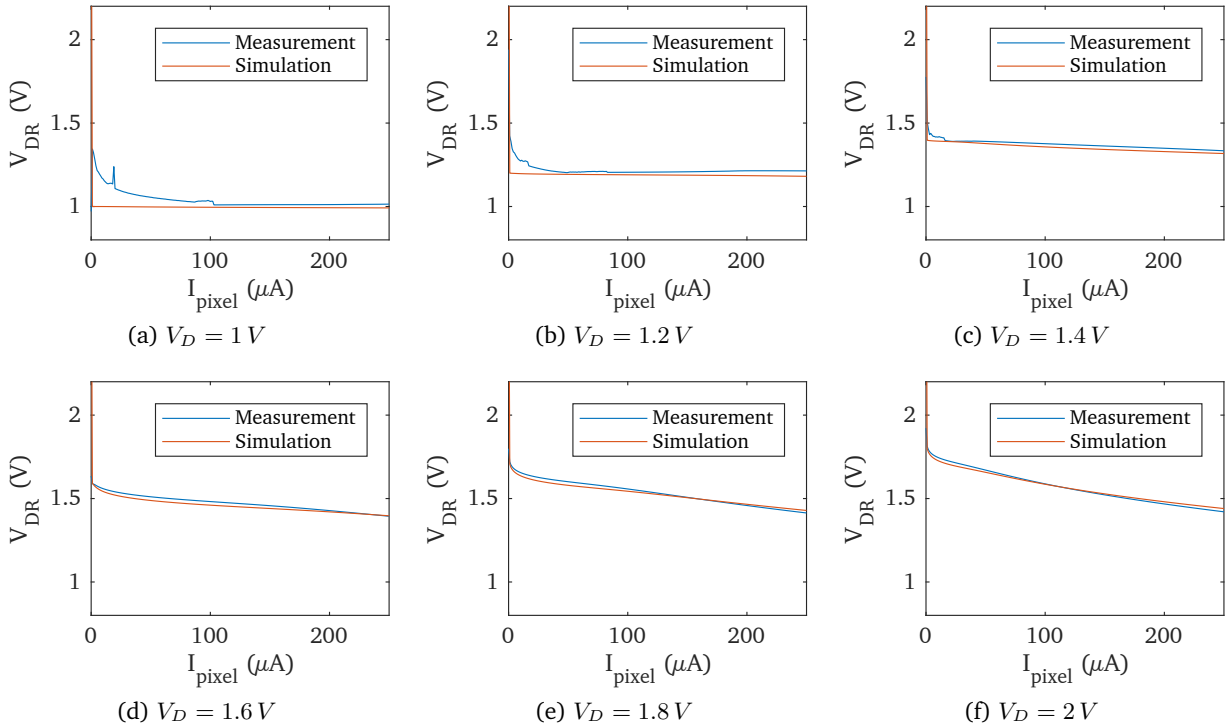


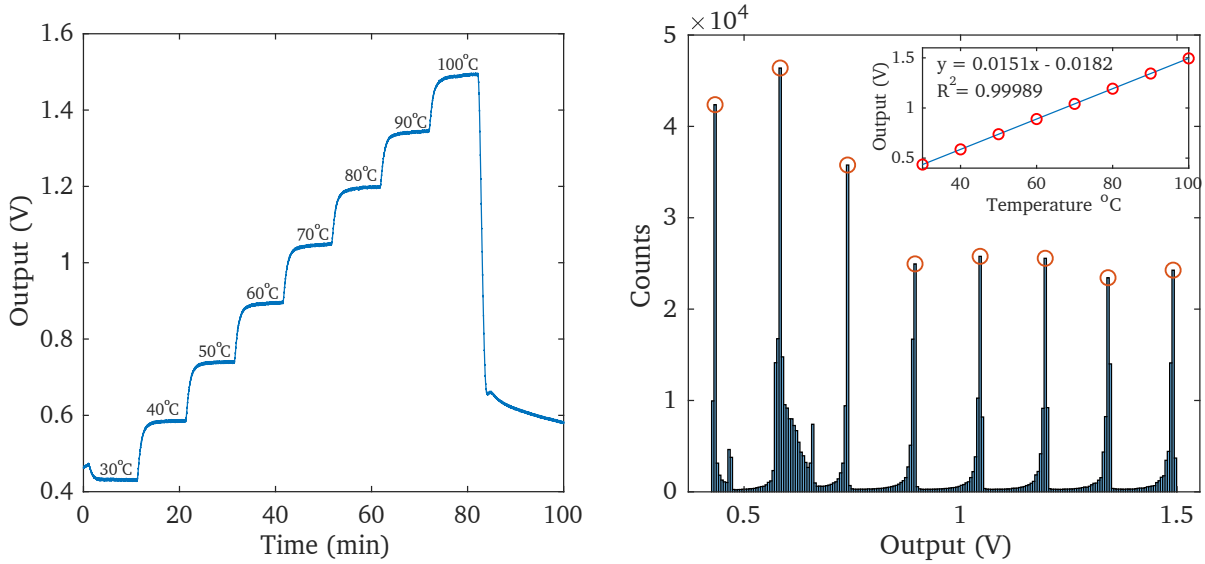
Figure E.1: Current Conveyor Characterisation at the nominal $V_D = 1.5\,V$. Left-hand plot shows the voltage on the Drain Row bus as a function of the pixel current I_{pixel}. Right-hand plot shows the mirrored current I_{out} to the transimpedance amplifier at a $VRP = 2\,V$ which is perfectly linear.



(a) $V_D = 1\,V$ (b) $V_D = 1.2\,V$ (c) $V_D = 1.4\,V$

(d) $V_D = 1.6\,V$ (e) $V_D = 1.8\,V$ (f) $V_D = 2\,V$

Figure E.2: Simulated and measured V_{DR} voltage as a function of the pixel current I_{pixel} for a $1 \leq V_D \leq 2\,V$ range. Evidently, for increasing drain row bus voltages (V_{DR}) and pixel current, the headroom of the cascoded current mirrors in the current conveyor decreases, which causes V_{DR} to deviate from the V_D intended.



(a) PTAT sensor outputfor a temperature change of $30 - 100^oC$ at steps of 10^oC.

(b) Histogram of the temperature output used to determine the temperature sensitivity

Figure E.3: Temperature sensor on the TTN chip with a sensitivity of $15.1\,mV/^oC$ after amplification.

Appendix F

TTN - Sample Output

After electrical testing and encapsulation, a snapshot obtained from all arrays is shown in Fig. 16 obtained at a fixed V_{ref} . The mismatch between pixels illustrates the trapped charge spread observed with floating gate devices. Note that the bottom right of the CM-PG array was covered by the encapsulating epoxy and was not in contact with the solution as shown in Fig. F.1.

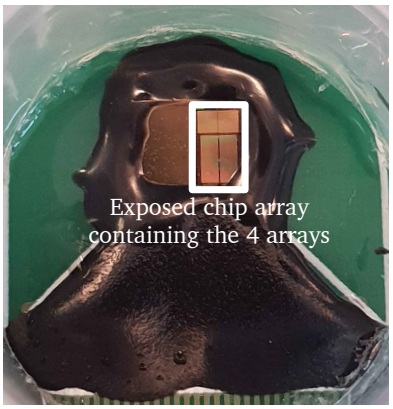


Figure F.1: Chip encapsulation using encapsulating epoxy. A representative output from this chip is shown in Fig. F.2.

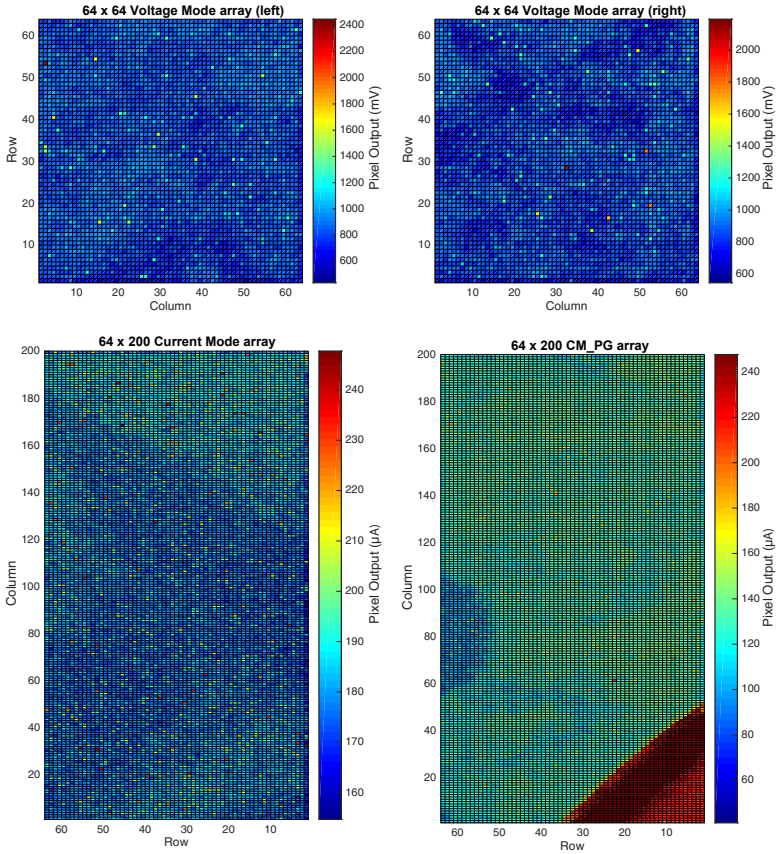


Figure F.2: Snapshot from all arrays at a fixed V_{ref}.

Appendix G

MATLAB GUI

A summary of the operations carried-out by the GUI is outlined below:

- Verify the chip's responsiveness and the operation of SPI block.
- Read the selected array continuously or for a pre-defined number of frames.
- Select a single pixel of any array for external sampling.
- Measure the chip's temperature.
- Visualisation in real-time of each frame as well as of the mean and median.
- Calibration of the CM-PG array.
- Read the CM-PG array while fetching calibration data from memory.

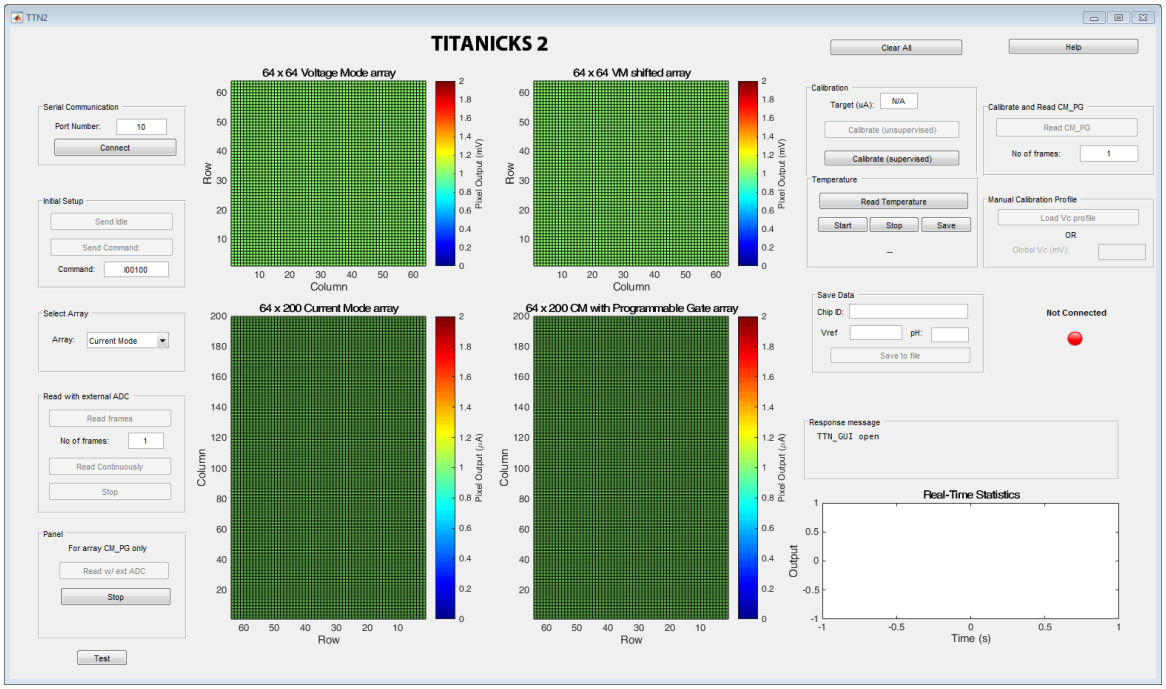
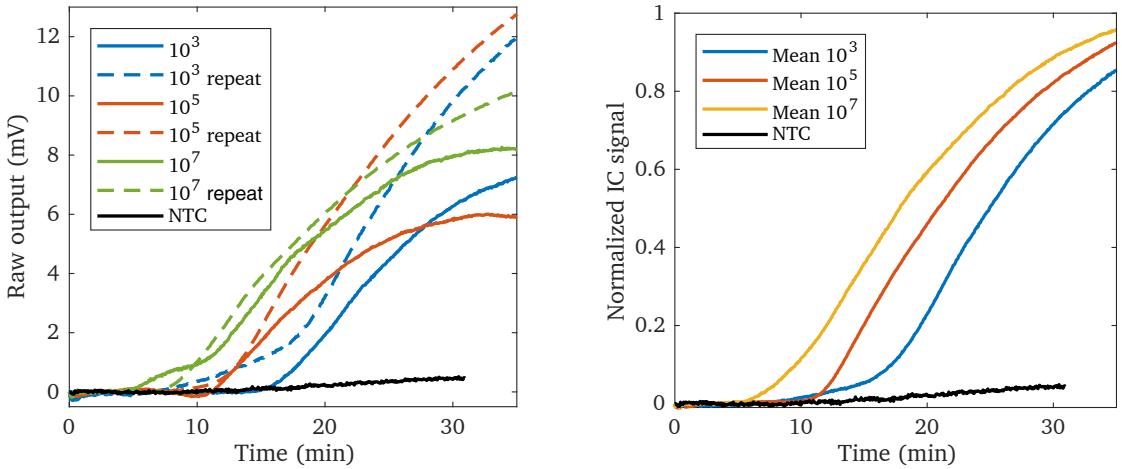


Figure G.1: MATLAB-based GUI

Appendix H

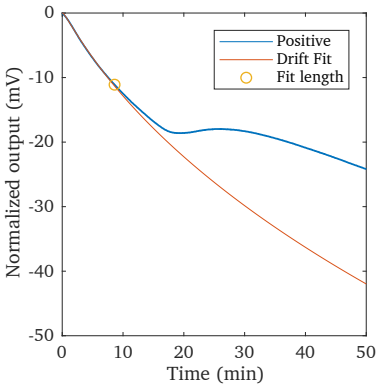
DNA Amplification using various targets



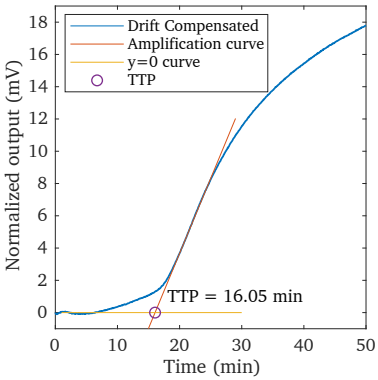
(a) Raw data.

(b) Average and normalized data.

Figure H.1: **Malaria Target:** Responses obtained from 3 synthetic DNA samples at various concentrations targeting an SNP in the Kelch 13 gene in the *Plasmodium falciparum* parasite that causes malaria. A positive signal indicates that the parasite is drug-resistant, specifically to artemisinin The curves obtained here were used to plot the TTP-vs-concentration graph in Fig. 7.6.

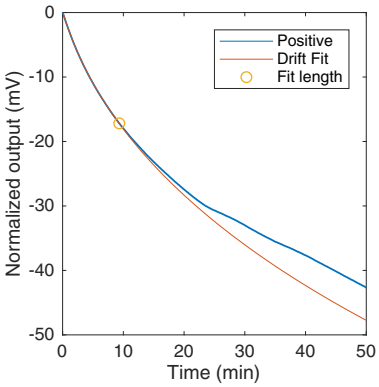


(a) Raw output.

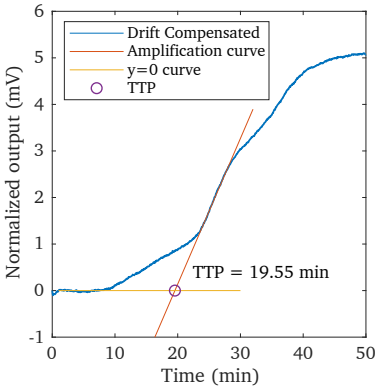


(b) Compensated output showing time-to-positive.

Figure H.2: **Viral target:** Results from the DNA amplification experiment for the detection of the IFI44L human gene which is up-regulated in and indicates viral infections.

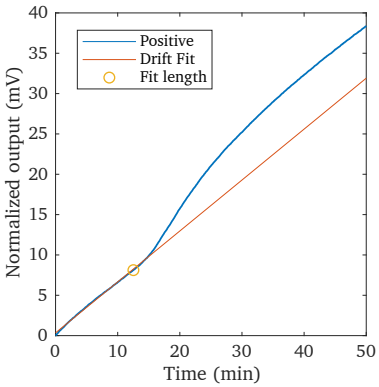


(a) Raw output.

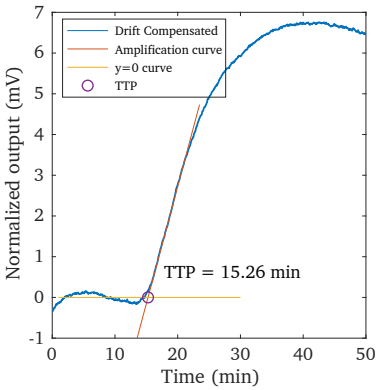


(b) Compensated output showing time-to-positive.

Figure H.3: **Reference human gene:** Results from the DNA amplification experiment for the detection of the PPIB reference gene in humans which shows the same expression level in both bacterial and viral infections.

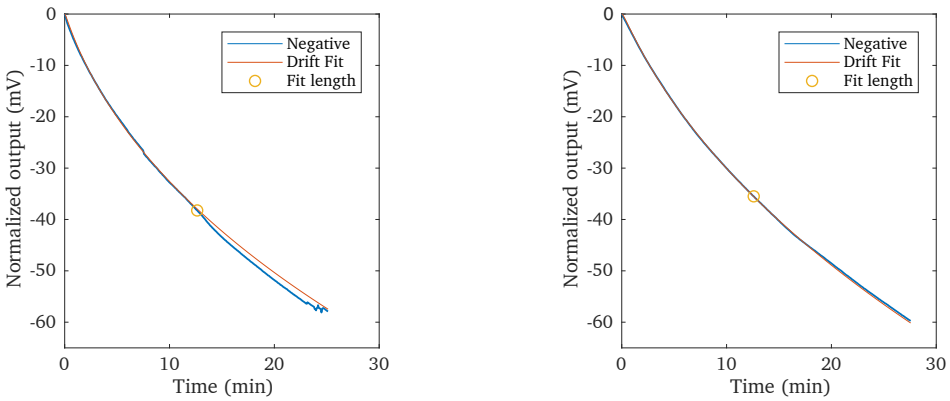


(a) Raw output.



(b) Compensated output showing time-to-positive.

Figure H.4: **Breast Cancer**: Results from the DNA amplification experiment for the detection of a wild-type SNP (i.e. SNP from healthy subject) in the PIK3CA human gene. The presence of a mutant SNP indicates a high probability of the presence of breast cancer.



(a) Raw output.

(b) Raw output.

Figure H.5: **Aspergillus**: used to illustrate a negative reaction. The target is a tandem repeat sequence in the the mutant allele of *Aspergillus fumigatus*. In this case, the reaction included primers which detect the tandem repeat, with samples that do not contain the tandem repeat and no amplification should occur.

Appendix I

Digital Core on the TTN chip

```
--------------------------------------------------------------------------------
------------------------- SPI Decoding and FSM -------------------------
--------------------------- N. Miscourides -----------------------------
--------------------------------------------------------------------------------
--
-- Address is a 16-bit input coming from the SPI
------------------SSAACXXXXXXXXXXX-----------------
-- SS: Select Operation
---- 00: Idle and Reset
---- 01: Safe_PG, used for calibration and readout of PG array
---- 10: Read any frame continuously w/ or w/o ADC
---- 11: Safe, select any pixel from any array (up to pix_coord = 4095)
--
-- AA: Array Addres
---- 00: CM
---- 01: CM_PG
---- 10: VM
---- 11: VM_shifted
--
-- C: ADC conversion enabled or not
--
-- XXXXXXXXXXX: various functions according to state
-- when in Read_frame and ADC then it is the number of conversions per pixel
-- when in Read_frame and no ADC then it is the number of clock cycles per pixel
-- when in Safe then it is the pixel coordinate

LIBRARY IEEE;
USE IEEE.std_logic_1164.ALL;
USE IEEE.numeric_std.ALL;

entity ttn_fsm is
port(
    -- IN
    clk                 : IN std_logic;
    data_spi_in         : IN std_logic_vector(15 downto 0);
    cs                  : IN std_logic;
    adc_in_vm       : IN std_logic_vector(9 downto 0);
    eoc_vm              : IN std_logic;
```

```
39      adc_in_cm          : IN std_logic_vector(9 downto 0);
40      eoc_cm                 : IN std_logic;
41      reset                  : IN std_logic;
42
43
44      --OUT
45      -- Enable signals to decoders
46      en_cm                  : OUT std_logic;
47      en_cm_pg           : OUT std_logic;
48      en_vm                  : OUT std_logic;
49      en_vm_sh           : OUT std_logic;
50
51      -- Pixel addresses
52      cm_row_addr            : OUT std_logic_vector(5 downto 0);
53      cm_col_addr        : OUT std_logic_vector(7 downto 0);
54      cm_pg_row_addr     : OUT std_logic_vector(5 downto 0);
55      cm_pg_col_addr     : OUT std_logic_vector(7 downto 0);
56      vm_row_addr        : OUT std_logic_vector(5 downto 0);
57      vm_col_addr        : OUT std_logic_vector(5 downto 0);
58      vm_sh_row_addr     : OUT std_logic_vector(5 downto 0);
59      vm_sh_col_addr     : OUT std_logic_vector(5 downto 0);
60      -- Data to SPI from ADCs
61      data_to_spi            : OUT std_logic_vector(15 downto 0);
62      -- Start ADC
63      start_adc_vm       : OUT std_logic;
64      start_adc_cm       : OUT std_logic;
65      -- To multiplexer
66      arr_addr_out       : OUT std_logic_vector(1 downto 0);
67      -- For microcontroller synchronisation
68      data_available     : OUT std_logic
69      );
70  end ttn_fsm;
71
72  architecture behav of ttn_fsm is
73
74      --type state_t is (idle, safe_PG, read_frame, safe);
75      --signal state : state_t;
76      signal state           : std_logic_vector(1 downto 0);
77
78      signal data_from_spi   : std_logic_vector(15 downto 0);
79      signal arr_addr        : std_logic_vector(1 downto 0);
80      signal coord_vm        : std_logic_vector(11 downto 0);
81      signal coord_vm_adc_off : std_logic_vector(11 downto 0);
82      signal coord_cm        : std_logic_vector(13 downto 0);
83      signal coord_cm_adc_off : std_logic_vector(13 downto 0);
84      signal adc_sample      : std_logic;
85      signal time_pp         : std_logic_vector(10 downto 0);
86      signal eoc_delay       : std_logic;
87      --signal eoc_delay2    : std_logic;
88      signal cs_sync         : std_logic;
89      signal data_av_adc_off : std_logic;
90      signal data_av_adc_on  : std_logic;
91
92      constant idle : std_logic_vector(1 downto 0) := "00";
93      constant safe_PG : std_logic_vector(1 downto 0) := "01";
94      constant read_frame : std_logic_vector(1 downto 0) := "10";
95      constant safe : std_logic_vector(1 downto 0) := "11";
96
```

```
97  begin
98
99      -- Input data
100     input_data_valid: process(cs_sync)
101     begin
102     -- first CLK rising edge after CS has gone high
103         if rising_edge(cs_sync) then
104             data_from_spi <= data_spi_in;
105         end if;
106     end process input_data_valid;
107
108     -- State Selection
109     ss_process: process(clk)
110     begin
111         if reset = '1' then
112             state <= idle;
113         elsif rising_edge(clk) then
114             case data_from_spi(15 downto 14) is
115                 when "01" => state <= safe_PG;
116                 when "10" => state <= read_frame;
117                 when "11" => state <= safe;
118                 when others => state <= idle; -- "00"
119             end case;
120         end if;
121     end process ss_process;
122
123     data_available <= not(data_av_adc_on or data_av_adc_off);
124
125     -- Synchronous process to generate simple outputs and internal signals
126     reg_process: process(clk)
127     begin
128         if rising_edge(clk) then
129             --Decode SPI command
130             arr_addr <= data_from_spi(13 downto 12);
131             adc_sample <= data_from_spi(11);
132             time_pp <= data_from_spi(10 downto 0); -- max 2047
133
134             -- Data from SPI is read at the next rising edge after (asynchronous) CS has
                    gone high
135             cs_sync <= cs;
136             eoc_delay <= eoc_vm or eoc_cm;
137             --eoc_delay2 <= eoc_delay;
138         end if;
139     end process reg_process;
140
141
142     -- Enable decoders
143     en_proc: process (state, arr_addr)
144     begin
145         if (state = idle) then
146             en_cm     <= '0';
147             en_cm_pg <= '0';
148             en_vm     <= '0';
149             en_vm_sh <= '0';
150         elsif (state = safe_PG) then
151             en_cm     <= '0';
152             en_cm_pg <= '1';
153             en_vm     <= '0';
```

```
154             en_vm_sh <= '0';
155         else
156             en_cm     <= '0';
157             en_cm_pg <= '0';
158             en_vm     <= '0';
159             en_vm_sh <= '0';
160             case arr_addr is
161                 when "00" =>
162                     en_cm     <= '1';
163                 when "01" =>
164                     en_cm_pg <= '1';
165                 when "10" =>
166                     en_vm     <= '1';
167                 when "11" =>
168                     en_vm_sh <= '1';
169                 when others => null;
170             end case;
171         end if;
172     end process en_proc;
173 
174     -- Process to start the two on-chip ADCs at the falling edge such that we know exactly
        when the ADC will start sampling (after half a CC)
175     adc_process: process(clk)
176     begin
177         if falling_edge(clk) then
178             start_adc_cm <= '0';
179             start_adc_vm <= '0';
180             if (adc_sample = '1'and state = read_frame) then
181                 case arr_addr is
182                     when "00" | "01" =>
183                         start_adc_cm <= '1';
184                     when "10" | "11" =>
185                         start_adc_vm <= '1';
186                     when others => null;
187                 end case;
188             end if;
189         end if;
190     end process adc_process;
191 
192     --Process that advances array coordinates when the ADC has finished sampling
193     coord_process: process(clk)--state, arr_addr, eoc_delay2, time_pp,
        adc_sample,data_from_spi);
194         variable count: unsigned(time_pp'range);
195         -- For CM arrays
196         variable col: integer range 0 to 200;
197         variable row: integer range 0 to 64;
198     begin
199         if rising_edge(clk) then
200             case state is
201                 when idle =>
202                     coord_vm <= (others => '0');
203                     coord_cm <= (others => '0');
204                     count := unsigned(time_pp);
205                     col := 0;
206                     row := 0;
207                 -- If a zero count is given then the default is 1.
208                     if count < 1 then
209                         count := to_unsigned(1, count'length);
```

```
210                     end if;
211                     data_av_adc_on <= '0';
212
213                 when read_frame =>
214                     -- 1 CC after EOC
215                     -- The same pixel is selected for <count> number of conversions
216                     data_av_adc_on <= '0';
217                     if ((eoc_delay = '1') and (adc_sample = '1')) then
218                         data_av_adc_on <= '1';
219                         case arr_addr is
220                             when "10" | "11" =>
221                                 coord_cm <= (others => '0');
222                                 count := count - 1;
223                                 if count = 0 then
224                                     coord_vm <= std_logic_vector(unsigned(coord_vm) +
                                        1);
225                                     count := unsigned(time_pp);
226                                     if count < 1 then
227                                         count := to_unsigned(1, count'length);
228                                     end if;
229                                 end if;
230                             when "00" | "01" =>
231                                 coord_vm <= (others => '0');
232                                 count := count - 1;
233                                 if count = 0 then
234                                     col:= col + 1;
235                                     if col = 200 then
236                                         col := 0;
237                                         row := row + 1;
238                                         if row = 64 then
239                                             row := 0;
240                                         end if;
241                                     end if;
242                                     coord_cm <= std_logic_vector(to_unsigned(row,6)) &
                                        std_logic_vector(to_unsigned(col,8));
243                                     count := unsigned(time_pp);
244                                     if count < 1 then
245                                         count := to_unsigned(1, count'length);
246                                     end if;
247                                 end if;
248                             when others => null;
249                         end case;
250                     end if;
251                 when others => null;
252             end case;
253         end if;
254     end process coord_process;
255
256     --Process that advances the selected array coordinates after <count> number of clock
        cycles. Both ADCs are off.
257     coord_process_adc_off: process(clk)
258         variable count: unsigned(time_pp'range);
259         variable col: integer range 0 to 200;
260         variable row: integer range 0 to 64;
261     begin
262         if rising_edge(clk) then
263             case state is
264                 when idle =>
```

```
265                     coord_vm_adc_off <= (others => '0');
266                     coord_cm_adc_off <= (others => '0');
267                     col := 0;
268                     row := 0;
269                     count := unsigned(time_pp);
270                     if count < 1 then
271                         count := to_unsigned(1, count'length);
272                     end if;
273                     data_av_adc_off <= '0';
274                 when read_frame =>
275                     data_av_adc_off <= '0';
276                     if adc_sample = '0' then
277                         case arr_addr is
278                             when "10" | "11" =>
279                                 coord_cm_adc_off <= (others => '0');
280                                 count := count - 1;
281                                 if count = 0 then
282                                     coord_vm_adc_off <=
                                        std_logic_vector(unsigned(coord_vm_adc_off) +
                                        1);
283                                     count := unsigned(time_pp);
284                                     if count < 1 then
285                                         count := to_unsigned(1, count'length);
286                                     end if;
287                                     data_av_adc_off <= '1';
288                                 end if;
289                             when "00" | "01" =>
290                                 coord_vm_adc_off <= (others => '0');
291                                 count := count - 1;
292                                 if count = 0 then
293                                     col:= col + 1;
294                                     if col = 200 then
295                                         col := 0;
296                                         row := row + 1;
297                                         if row = 64 then
298                                             row := 0;
299                                         end if;
300                                     end if;
301                                     coord_cm_adc_off <=
                                        std_logic_vector(to_unsigned(row,6)) &
                                        std_logic_vector(to_unsigned(col,8));
302                                     count := unsigned(time_pp);
303                                     if count < 1 then
304                                         count := to_unsigned(1, count'length);
305                                     end if;
306                                     data_av_adc_off <= '1';
307                                 end if;
308                             when others => null;
309                         end case;
310                     end if;
311
312                 when safe =>
313                     case arr_addr is
314                         when "00" | "01" =>
315                             coord_cm_adc_off <= "00" & data_from_spi(11 downto 0);
316                             coord_vm_adc_off <= (others => '0');
317                         when "10" | "11" =>
318                             coord_vm_adc_off <= data_from_spi(11 downto 0);
```

```
319                             coord_cm_adc_off <= (others => '0');
320                         when others => null;
321                     end case;
322
323                 when safe_PG =>
324                     coord_cm_adc_off <= data_from_spi(13 downto 0);
325                     coord_vm_adc_off <= (others => '0');
326                 when others => null;
327             end case;
328         end if;
329     end process coord_process_adc_off;
330
331     -- Decode coordinate into addresses
332     decode: process (state, arr_addr, adc_sample, coord_vm, coord_vm_adc_off, coord_cm,
        coord_cm_adc_off)
333     begin
334         vm_row_addr       <= (others => '0');
335         vm_col_addr       <= (others => '0');
336         vm_sh_row_addr <= (others => '0');
337         vm_sh_col_addr <= (others => '0');
338         cm_row_addr       <= (others => '0');
339         cm_col_addr       <= (others => '0');
340         cm_pg_row_addr    <= (others => '0');
341         cm_pg_col_addr    <= (others => '0');
342         case state is
343             when read_frame =>
344                 case arr_addr is
345                     when "00" =>
346                         if adc_sample = '1' then
347                             cm_row_addr <= coord_cm(13 downto 8);
348                             cm_col_addr <= coord_cm(7 downto 0);
349                         else
350                             cm_row_addr <= coord_cm_adc_off(13 downto 8);
351                             cm_col_addr <= coord_cm_adc_off(7 downto 0);
352                         end if;
353                     when "01" =>
354                         if adc_sample = '1' then
355                             cm_pg_row_addr <= coord_cm(13 downto 8);
356                             cm_pg_col_addr <= coord_cm(7 downto 0);
357                         else
358                             cm_pg_row_addr <= coord_cm_adc_off(13 downto 8);
359                             cm_pg_col_addr <= coord_cm_adc_off(7 downto 0);
360                         end if;
361                     when "10" =>
362                         if adc_sample = '1' then
363                             vm_row_addr <= coord_vm(11 downto 6);
364                             vm_col_addr <= coord_vm(5 downto 0);
365                         else
366                             vm_row_addr <= coord_vm_adc_off(11 downto 6);
367                             vm_col_addr <= coord_vm_adc_off(5 downto 0);
368                         end if;
369                     when "11" =>
370                         if adc_sample = '1' then
371                             vm_sh_row_addr <= coord_vm(11 downto 6);
372                             vm_sh_col_addr <= coord_vm(5 downto 0);
373                         else
374                             vm_sh_row_addr <= coord_vm_adc_off(11 downto 6);
375                             vm_sh_col_addr <= coord_vm_adc_off(5 downto 0);
```

```
376                         end if;
377                     when others => null;
378                 end case;
379
380             when safe =>
381                 case arr_addr is
382                     when "00" =>
383                         cm_row_addr <= coord_cm_adc_off(11 downto 6);
384                         cm_col_addr <= "00" & coord_cm_adc_off(5 downto 0);
385                     when "01" =>
386                         cm_pg_row_addr <= coord_cm_adc_off(11 downto 6);
387                         cm_pg_col_addr <="00" & coord_cm_adc_off(5 downto 0);
388                     when "10" =>
389                         vm_row_addr <= coord_vm_adc_off(11 downto 6);
390                         vm_col_addr <= coord_vm_adc_off(5 downto 0);
391                     when "11" =>
392                         vm_sh_row_addr <= coord_vm_adc_off(11 downto 6);
393                         vm_sh_col_addr <= coord_vm_adc_off(5 downto 0);
394                     when others => null;
395                 end case;
396
397             when safe_PG =>
398                 cm_pg_row_addr <= coord_cm_adc_off(13 downto 8);
399                 cm_pg_col_addr <= coord_cm_adc_off(7 downto 0);
400
401             when others => null;
402         end case;
403     end process decode;
404
405     -- Process to send data to SPI
406     send_to_spi: process(clk)
407     begin
408         -- Data becomes available from ADC at rising edge so send at falling edge
409         if falling_edge(clk) then
410             -- If no SPI transaction in progress
411             if cs = '1' then
412                 case state is
413                     when read_frame =>
414                         if (adc_sample = '1') then
415                             if ((eoc_vm = '1') or (eoc_cm = '1')) then
416                                 case arr_addr is
417                                     when "00" | "01" =>
418                                         -- -1 not needed
419                                         -- Send Col addr (6b out of 8b) and ADC value
                                            (10b)
420                                         data_to_spi <=
                                            std_logic_vector(unsigned(coord_cm(5
                                            downto 0))) & adc_in_cm;
421                                     when "10" | "11" =>
422                                         -- Send Col addr (6b) and ADC value (10b)
423                                         -- Note that the pixel coordinates have
                                            already advanced when current ADC sample
                                            is valid
424                                         data_to_spi <=
                                            std_logic_vector(unsigned(coord_vm(5
                                            downto 0))) & adc_in_vm;
425                                     when others => null;
426                                 end case;
```

```
427                                 end if;
428                             else
429                             -- If in manual mode send current pixel address
430                                 case arr_addr is
431                                     when "00" | "01" =>
432                                         data_to_spi <= "00" & coord_cm_adc_off;
433                                     when "10" | "11" =>
434                                         data_to_spi <= "0000" & coord_vm_adc_off;
435                                 when others => null;
436                                 end case;
437                             end if;
438                         -- Otherwise send the same command back for verification
439                         when idle =>
440                             data_to_spi <= data_from_spi;
441
442                         when safe =>
443                             case arr_addr is
444                                 when "00" | "01" =>
445                                     data_to_spi <= "00" & coord_cm_adc_off;
446                                 when "10" | "11" =>
447                                     data_to_spi <= "0000" & coord_vm_adc_off;
448                                 when others => null;
449                             end case;
450
451                         when safe_PG =>
452                             data_to_spi <= "00" & coord_cm_adc_off;
453                         when others => null;
454                     end case;
455                 end if;
456             end if;
457     end process send_to_spi;
458
459     -- To select array for ADC
460     arr_addr_process: process(state, arr_addr)
461     begin
462     if state = safe_PG then
463         arr_addr_out <= "01";
464     else
465         arr_addr_out <= arr_addr;
466     end if;
467     end process arr_addr_process;
468
469 end behav;
```