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Dynamic Overload Capability of VSC HVDC Interconnections for Frequency Support

Inmaculada Martínez Sanz, *Member, IEEE,* Paul D. Judge, *Member, IEEE,* Claudia E. Spallarossa, Balarko Chaudhuri, *Senior Member, IEEE,* and Tim C. Green, *Senior Member, IEEE*

***Abstract*—In future power systems reduced overall inertia caused by an increased dominance of asynchronous generation and interconnections would make frequency control particularly challenging. As the number and power rating of Voltage Source Converter (VSC) HVDC systems increases, network service provision would be expected from such systems and to do so would require overload capacity to be included in the converter specifications. This paper studies the provision of frequency services from Modular Multilevel Converter (MMC)-based VSC HVDC interconnections using temperature-constrained overload capability. Overload of the MMC-based HVDC system is achieved through controlled circulating currents, at the expense of higher losses, and subject to a control scheme which dynamically limits the overload available in order to keep the semiconductor junction temperatures within operational limits. Two frequency control schemes that use the obtained overload capacity to provide frequency response during emergency conditions are investigated. The controllers' performance is demonstrated in the context of the future Great Britain transmission grid through a reduced equivalent test system. Simulation results show that even modest temperature margins which allow overload of MMC-based HVDC systems for a few seconds are effective as a primary frequency reserve and also reduce the loss of infeed requirements of such interconnections.**

***Index Terms*—Frequency Control, HVDC, Modular Multilevel Converters (MMC), Power System Dynamics, VSC Overload.**

I. Introduction

OVER the past decade, Voltage Source Converter (VSC) HVDC schemes have become an increasingly popular option for long distance and sub-sea transmission systems. This is due to increasing efficiency levels, new applications such as off-shore wind farms, as well as an opening of the market with several vendors now supplying competing products. The Modular Multi-level Converter (MMC) was proposed in [1] and at present is the standard topology employed in VSC HVDC applications. The MMC consists of six converter arms, each of which contains a valve comprised of a large number of series connected sub-modules, usually in a half-bridge arrangement with two IGBTs and a floating sub-module capacitor. By controlling the switching of each individual sub-module, a highly sinusoidal voltage waveform can be produced, while keeping the average switching frequency of the power electronics low [2].

The authors are with the Control and Power Research Group, Department of Electrical and Electronic Engineering, Imperial College London, London, SW7 2AZ UK. (e-mail: im1309@ic.ac.uk, pj712@ic.ac.uk) and gratefully acknowledge the financial support of the Research Councils UK through the HubNet Project (grant number: EP/I013636/1). Supporting data is available on request: please contact cap-publications@imperial.ac.uk.

The maximum power ratings currently available for VSC systems are in the region of 1.8 GW in a single sub-sea cable based link and 2.5 GW in an on-shore system [3]. As the technology further matures, even higher power ratings are anticipated and VSC converters of such high power rating may be expected to provide ancillary services to the AC systems in which they are located [4]. The provision of these features implies that the converter must have some level of power capability reserved above its nominal rating.

Overload capability is available for Current Source Converters (CSC) based HVDC systems [5] and is a desirable requisite, from a system level perspective, for multi-gigawatt HVDC schemes. However, such overload capability has not yet been demonstrated or presented as an option by VSC manufacturers. This is due to a combination of technology limitations and customer requirements. The thyristor technology used in CSC is very robust and much less susceptible to failure caused by over-currents than the IGBT technology used in VSC. IGBT switches are sensitive to both over-voltage and over-current induced failure mechanisms, as well as thermal runaway [6]. For HVDC applications, where reliability is critical, designing overload capacity into such systems therefore requires special consideration to the limitation of these devices.

In order to provide system support features during emergency conditions, when already operating at rated capacity, a VSC must be capable of moving outside its rated P/Q specification, into an overload region. While doing so, the operational limits of the IGBT devices, both in terms of junction temperature and safe operating area (SOA), must be respected. This could be achieved through the use of an over-sized IGBT, which is capable of reliably switching the increased peak current magnitudes during operation in the overloaded area. Alternatively, overload capability might be achieved without significantly over-sizing the semiconductor devices through the use of controlled circulating currents that reduce the peak current flowing through the converter for a given set-point. Such techniques were initially proposed in [7], [8] as a method of maximizing the overall P/Q capability of MMCs and are now well established strategies [9]. These methods can expand the active power processing capability of the converter by approximately 30%. Although the increased losses within the converter caused by the circulating currents make it un-attractive for steady-state operation, they could be used during emergency conditions, as suggested in [10].

In addition to the peak current handling capability limitations of MMCs, restrictions on the junction temperatures of the IGBT devices also have to be enforced. In [7]–[9] the influence

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of converter temperature dynamics on the achievable overload were neglected. Overload capability of MMC-based HVDC systems considering the temperature dynamics within the converter has arguably only been discussed in [10] and [11]. However, in [11], simplified temperature dynamics were used and implications on the converter design were not addressed.

Provision of network services such as frequency support and power oscillation damping through VSC HVDC has been reported extensively [12] with some papers focusing specifically on MMC-based HVDC [13], [14]. In these works, the headroom for dynamic modulation of active/reactive power was made available by either considering the expensive option of de-loaded operation (below the rated capacity of the converter, e.g. [13], [14]) or by assuming some overload capability without considering the physical constraints of the converters properly [15], [16]. Application of a realistically designed overload capability of MMC-based HVDC for network support has not been demonstrated in a multi-machine system.

This paper builds upon the results presented in [10] to examine the application of the overload capability of an MMC-based HVDC interconnection in order to provide frequency support to an AC grid. Overload is achieved through controlled circulating currents using a proposed control scheme that ensures that the operating limits and thermal constraints of the IGBT modules are respected while providing this network service. This paper is the first to show the potential benefits of MMC-based HVDCs designed with overload capability for grid frequency control. Two different control schemes for frequency response are presented and their benefits for the operation of a representative AC network are analyzed. Furthermore, the influence of the semiconductor junction temperature on the support duration with the different controllers is also studied. The effectiveness of the proposed approach is evaluated through a case study for a representative future scenario in the Great Britain (GB) transmission system with several interconnectors, corresponding either to a connection to a remote AC system or to an off-shore DC network.

The structure of the paper is as follows. Section II describes the MMC reduced dynamic model and its energy control scheme while Section III presents the MMC thermal model. The implementation of the overload capability within MMCs is discussed in Section IV. Section V covers the application of this feature to frequency service provision, proposing two different solutions. The case study is introduced in Section VI and the simulation results to verify the control performance in Section VII. Finally, Section VIII presents some conclusions.

II. MMC Reduced Dynamic Model for Power System Studies

A Reduced Dynamic Model (RDM) of an MMC, implemented within a large-scale power system simulation platform (DigSILENT PowerFactory), is used to carry out detailed system level studies. The use of an RDM allows the main characteristics of an MMC to be captured, while approximating the switching behaviour with simplified functions and controlled sources [17]. The MMC RDM employed in this work was first introduced in [18] and its main features and control philosophy are summarized in this section. The circuit arrangement of the RDM is shown in Fig. 1. It comprises two three-phase controlled voltage sources (V_j^{up}, V_j^{low}) which represent the stack of sub-modules within each arm and two arm inductors and a phase reactor per phase. The DC side is formed by a DC voltage source controlled to supply the specified DC voltage (u^{set}). AC and DC sides are virtually connected by the control scheme. These modelling choices were driven by the software limitations, as discussed in [18]. For a detailed description of the MMC inner variables, one can refer to [8].

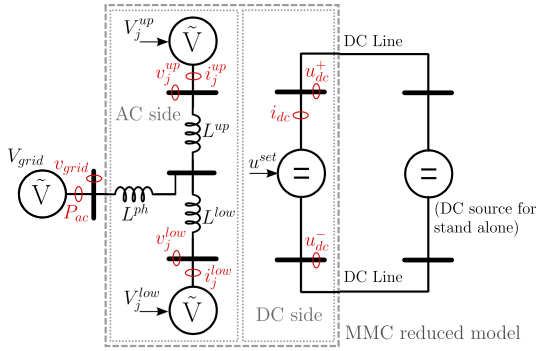


Fig. 1. MMC reduced dynamic model (RDM) single line diagram.

The MMC control scheme is based on an energy balance approach which regulates the amount of energy contained in the arms of the converter [19]. It generates a set of reference signals for the two AC voltage sources in order to nullify the energy deviation between arms and maintain the energy within each arm at a nominal value. Three energy balancing controls (horizontal, vertical and average) perform these tasks. An overview of this control scheme is shown in Fig. 2 and further details of it can be found in [18].

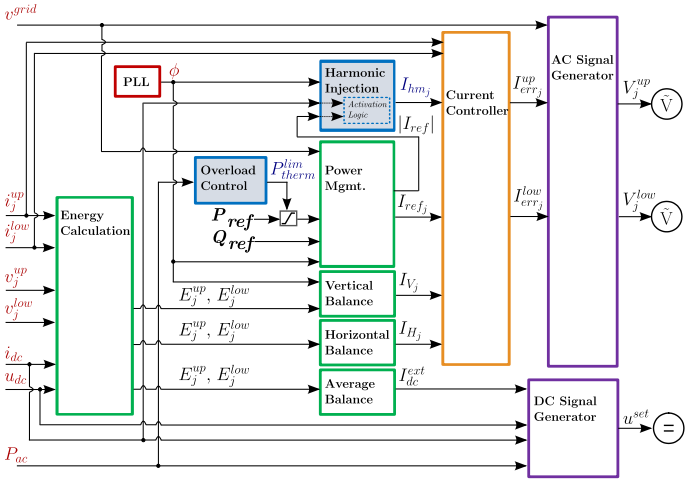


Fig. 2. MMC reduced dynamic model control scheme.

Two additional control blocks have been added to the control system described in [18] and are referred to in Fig. 2 as *"Harmonic Injection"* and *"Overload Control"*. These blocks control the response of the converter during overload conditions and are described in detail in Section IV.

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III. MMC Thermal Model

This section discusses the MMC thermal model adopted in the simulations. Power-loss estimates and transient IGBT thermal models have been considered to derive the junction temperatures of the devices within the converter, following the work presented in [20] and [10]. Limits on these junction temperatures during overload conditions would ultimately determine the effective available response of the MMC.

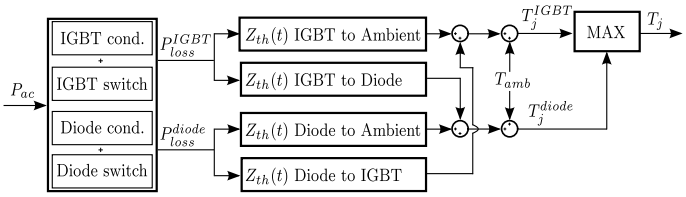


Fig. 3. IGBT power-loss tables and MMC thermal model.

An overview of the thermal model presented in [10] is shown in Fig. 3. We adopt the same modelling scheme and the same IGBT module data (5SNA 1200E330100 [21]) to derive the limiting junction temperature T_j. This temperature is the larger of the diode junction temperature (T_j^{diode}) and the IGBT junction temperature (T_j^{IGBT}). These junction temperatures correspond to the average value of the recorded measurements at each sub-module in the converter.

Note that only the junction temperatures of the lower IGBT module of each sub-module are considered, as in MMCs this module is under significantly more thermal stress than the upper IGBT module [22]. In the simulations presented next we assume the coolant inlet temperature T_{amb} equal to 60^oC.

The power-losses within the IGBT and diode of the lower IGBT module within each sub-module (P_{loss}^{IGBT}, P_{loss}^{diode}) are determined using look-up tables, using the data in [10], which considered the power-loss distribution between diode dies and IGBT dies within the lower IGBT module for active powers in the range of -1.3 to 1.3 p.u. using a detailed switching model of a full-scale converter. Loss values are taken assuming the AC voltage at the converters PCC is at its nominal level. The thermal impedances of the IGBT modules are represented by the transfer functions $Z_{th}(t)$, taken from [10]:

$$Z_{th}(t) = \sum R_i(1 - e^{-t/\tau_i}) \quad (1)$$

where R_i is an equivalent thermal resistance and τ_i a thermal time constant for each conduction path. The thermal impedances used within this paper are derived from an ANSYS IcePak FEM model of a heat-sink mounted device, which is shown in Fig. 4 and was previously presented in [22] and [10]. In [20], the heat-sink was found to contribute significantly to both the overall thermal impedance and heat-spreading effect between dies within the module so was considered necessary to model. This thermal model has been validated against the experimental results presented in [20].

Fig. 5 shows the layers of the cooling path in an IGBT module from the silicon die to the ambient cooling liquid, as well as simulation results showing the difference in temperatures between the internal layers of the IGBT in response

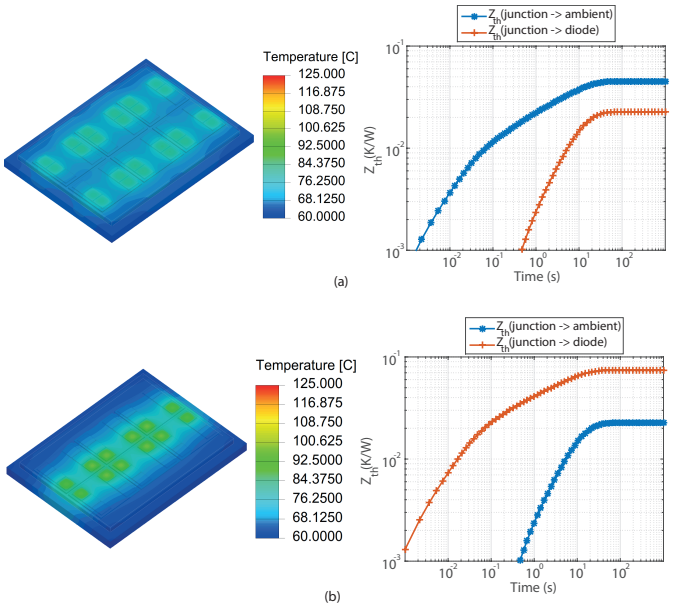


Fig. 4. Thermal impedance of IGBT and diode within IGBT module performed within ANSYS IcePak. (a) Transient thermal impedance of 1 kW evenly distributed between the 24 IGBT dies within the module. (b) Transient thermal impedance of 1 kW evenly distributed between the 12 diode dies within the module.

to a stepped change in heat dissipated at the IGBT dies. The upper layers of the IGBT module, such as the silicon die, copper substrate and ceramic insulation can be seen to heat up very quickly. The lower layers in the cooling path, such as the baseplate and the heat-sink, heat up at much lower rates, as well as contributing a large part of the overall thermal impedance from the silicon die to the ambient cooling liquid. When considering dynamic thermal rating it is mostly the slower response of the IGBT baseplate and heat-sink that will be exploited.

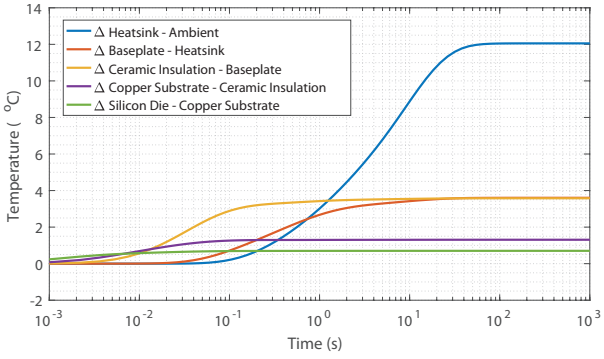


Fig. 5. Difference in layer temperatures in IGBT module in response to a stepped 1 kW of heat at the IGBT dies.

IV. MMC Overload Capability

The P/Q operating envelope of MMCs is limited by four main factors [2], [23]: the peak arm current limit, the peak sub-module voltage, the arm voltage capability and the over-modulation limit of the converter. The peak arm current limit, imposed by the need to respect the safe operating area (SOA)

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of the IGBTs, represents the most significant barrier to increase the active power processing capability of the converter. This limit can be overcome using techniques like the ones reported in [7], [8] where controlled circulating currents are used to reduce the peak of the arm currents, allowing up to 30% increased capacity. The limits imposed by both the peak sub-module voltage limit and the arm voltage capability are influenced by the level of energy stored within the converter and likely to be overcome at some design cost, either in terms of an increased sub-module capacitor size or an increased number of sub-modules within the converter. This may result in some sacrifice of either the converters volume or the efficiency in order to achieve the desired overload capability.

In addition to the four restrictions mentioned previously, the junction temperature limits of the IGBT devices must be respected when designing VSCs. The maximum specified operating temperature for high power IGBT modules is usually 125^oC. This is typically not a concern in MMCs due to the high efficiency which results in relatively low junction temperatures [22], [24]. In [10] however, it was found that utilizing circulating currents to achieve an overload capability of 30% causes approximately a 20^oC increase in the steady-state junction temperatures, when compared against the case where the converter is operating at rated power.

Considering the associated high costs of unplanned outages and failures of HVDC links, manufacturers may desire to maintain significant safety margins on the device junction temperatures, even under such emergency conditions where overload capability would be required. For this reason reference [10] proposed that the available level of overload capability that the converter could achieve be dynamically set so as to limit the peak device junction temperatures, an idea that is adopted and expanded in this work.

It must be acknowledged that other elements in the HVDC system, such as the cable system and converter transformers, may also impose thermal limits on the amount of time the overload capability is available. Overloading of transmission scale transformers is a well understood and utilised in practice in many power-systems [25]. The temperature dynamics of transformers under overload conditions occur over long time-scales, for example in [26], an approximate 30% overload was found to be acceptable for a 1 hour period. Dynamic rating of overhead lines and cables has also been investigated (albeit for AC systems) and found to have similar time constants [27]. The short-term response of an HVDC system, is therefore expected to be dominated exclusively by the limitations imposed by the converter itself, with the other elements within the overall system limiting the power transfer capability at longer time-scales.

A. MMC Overload through Harmonic Current Injection

This work considers the use of controlled circulating currents to facilitate the provision of short-term overload capacity within MMCs, as in [7]. The MMC control scheme described in Section II is updated to include a block which generates the circulating current references (I_{hm_j} with $j = a, b, c$) to allow the converter to move into the overloaded region. The harmonic currents are comprised of even components ($2nd$ and $4th$) and are defined in the *"Harmonic Injection"* block in Fig. 2, as follows:

$$\begin{aligned} I_{hm_a} &= -\hat{I}_2 sin(2(wt+\theta)+\frac{\pi}{2}) - \hat{I}_4 sin(4(wt+\theta)+\frac{\pi}{2}) \\ I_{hm_b} &= -\hat{I}_2 sin(2(wt+\theta-\frac{2\pi}{3})+\frac{\pi}{2}) - \hat{I}_4 sin(4(wt+\theta-\frac{2\pi}{3}))+\frac{\pi}{2}) \\ I_{hm_c} &= -\hat{I}_2 sin(2(wt+\theta+\frac{2\pi}{3}))+\frac{\pi}{2}) - \hat{I}_4 sin(4(wt+\theta+\frac{2\pi}{3}))+\frac{\pi}{2}) \end{aligned} \quad (2)$$

where $\theta = tan^{-1}(Q_{ref}/P_{ref})$, $\hat{I}_2 = 0.3947k$, $\hat{I}_4 = 0.0603k$. Note that $k = 0.6(\sqrt{2}|I_{ref}|/2 + i_{dc}/3 - I_{max})$ is designed such to limit the converter peak arm current to I_{max}. In addition, $|I_{ref}|$=$(P_{ref}^2 + Q_{ref}^2)^{1/2}/(\sqrt{3}|v^{grid}|)$.

The current references $I_{ref_j}^{up}$, $I_{ref_j}^{low}$ for each arm in the converter, passed to the current controller in the scheme of Fig. 2, are now a combination of AC current reference I_{ref_j}, DC current reference i_{dc}, balancing current I_{bal} plus the injected harmonic current I_{hm_j}:

$$\begin{aligned} I_{ref_j}^{up} &= \frac{i_{dc}}{3} + \frac{I_{ref_j}}{2} + I_{bal} + I_{hm_j} \\ I_{ref_j}^{low} &= \frac{i_{dc}}{3} - \frac{I_{ref_j}}{2} + I_{bal} + I_{hm_j} \end{aligned} \quad (3)$$

The circulating harmonic currents are set to allow up to a 27.5% overload of the MMC beyond its active power limit P_{rated} that was set by the peak arm current [10]. Such currents are suppressed during normal operation and will only start circulating to enable the extra capacity when the peak of the arm current to be tracked ($\sqrt{2}|I_{ref}|/2+i_{dc}/3$) goes above the converter arm current limit (I_{max}).

B. IGBT Temperature Control for Extended Thermal Overload

As mentioned before, the obtained overload capability through the circulating currents is subject to thermal constraints of the IGBT modules. Following [10], an overload controller is adopted to establish a dynamic power limit P_{therm}^{lim} which restricts the MMC overload capacity that can be achieved depending on the maximum allowable junction temperature of the semiconductor devices T_{max}. This controller is shown in Fig. 6 and it uses the junction temperature derived by the MMC thermal model (see Section III) to determine this limit.

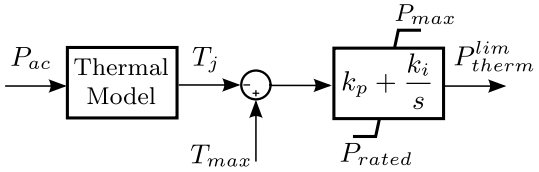


Fig. 6. MMC overload control considering its temperature dynamics (*"Overload Control"* block in Fig. 2).

A saturable integrator with a limit corresponding to the maximum active power capability P_{max} sets the allowable maximum power that the converter can transfer[1]. When the

[1]Note that P_{max} corresponds to the converter peak arm current limit (I_{max}) whereas P_{therm}^{lim} is meant to restrict this value according to the thermal limits of the IGBT modules.

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junction temperature limit of a device T_j is breached, the integrator reduces P_{therm}^{lim} so as to maintain this junction temperature below T_{max}.

The MMC overload control can be extended to an HVDC point-to-point configuration following Fig. 7. Note that P_{therm}^{lim} corresponds to the more restrictive value between the two obtained at rectifier and inverter stations where the overload control is implemented. The rectifier station is set to operate in P-Q control mode, while the inverter end is set to operate in V_{dc}-Q mode, to track a set-point V_{dc}^{ref}. The AC power reference of the inverter is set equal to the measured DC power on the inverter side to maintain the AC/DC power balance.

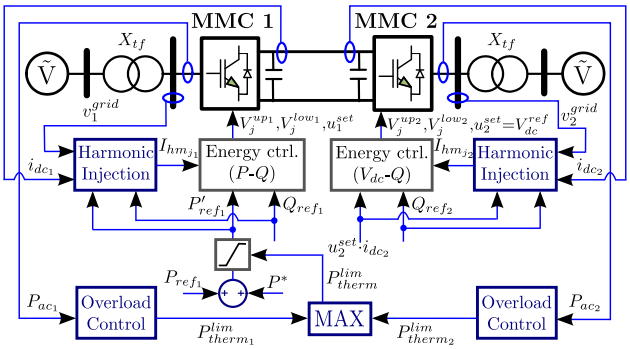


Fig. 7. MMC-based point-to-point HVDC system with overload control.

V. MMC Overload Application to Frequency Service Provision

The short-term overload capability described in Section IV can be used during emergency conditions by MMCs connected to an AC grid to provide ancillary services like, for instance, primary frequency response. This feature will be critical as power systems evolve towards low inertia scenarios. A generic frequency control scheme is presented in this paper to activate the response P^* of an MMC-based HVDC interconnection after a frequency event. The scheme is shown in Fig. 8 and it covers the main characteristics of a primary frequency support controller while also accounting for the overload limits of the two converter stations.

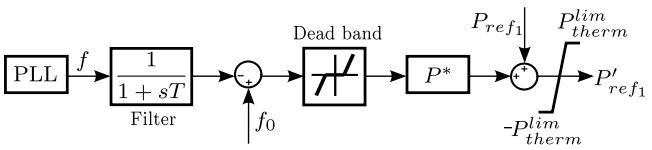


Fig. 8. MMC-based HVDC system overload control for frequency support

Frequency $f(t)$ is measured through a phase locked loop at the AC connection point and filtered with a first order filter with $T = 0.05$ s, which also accounts for any communication delay. A frequency dead-band of $\pm$ 0.15 Hz is initially assumed to trigger the response P^*, which contributes to the power reference P_{ref_1} for the rectifier converter. Note that this dead-band value is chosen such to enable the overload capability only during abnormal frequency conditions. Two alternatives are explored to provide primary frequency support:

1) *Frequency-power droop controller:* the converter support is proportional to the AC system frequency deviation Δf with a gain K.

$$P^* = K \cdot \Delta f(t) = K \cdot (f_0 - f(t)) \tag{4}$$

where f_0 is the nominal frequency of the AC system. In this way, the change in power across the interconnector for a given change in frequency follows a linear characteristic K known as *droop* [28]. This supplementary control would try to maintain the AC frequency within an acceptable range and has already been contemplated in the literature (although without realistically accounting for the link overload) to fully exploit the support capabilities of HVDC interconnectors [28], [29].

2) *Maximum power release controller:* the converter provides the maximum support available P_{max}, corresponding to a 27.5% overload, as discussed in Section IV-A.

$$P^* = P_{max} - P_{rated} = 0.275 \cdot P_{rated} \tag{5}$$

This option is particularly effective as an emergency action for fast frequency recovery during severe imbalance conditions. Such action could be activated only under extreme scenarios by selecting a more restrictive activation frequency dead-band. In addition, the fast response achieved with this controller would lead to reduced RoCoF (rate of change of frequency) values across the system. Mitigating large RoCoFs is a major concern in future low inertia systems as it could trigger the loss of mains protections of embedded generators, creating cascading disconnections and further accelerating the frequency fall [30].

In both cases, the support provision P^* would ultimately be limited by the converters thermal constraints through P_{therm}^{lim}. Both control strategies are implemented in the MMC control scheme of Fig. 7 and tested in Section VII for a frequency disturbance in a representative AC network.

Alternative ways of providing frequency support could be considered within the proposed MMC overload framework. For instance, an hybrid approach could be effective wherein the maximum power release controller switches over to droop control after the inertial period to cope with different loss of infeed sizes while maintaining a very fast initial response.

VI. Case Study: GB Transmission System

A three-generator equivalent model of the Great Britain (GB) transmission system including two future interconnectors (shown in Fig. 9) is used to demonstrate the MMC overload control strategy for frequency support. Such a simplified system model is used to run EMT (Electromagnetic Transient) simulations (with 50 μs time step) within a reasonable time in order to capture the instantaneous variations of phase, arm and circulating currents. It is to be noted that the reported overload control technique for frequency support is generic and could be demonstrated for larger systems using phasor (averaged) models.

The three-machine GB equivalent test system described in [31] has been extended to accommodate two HVDC corridors

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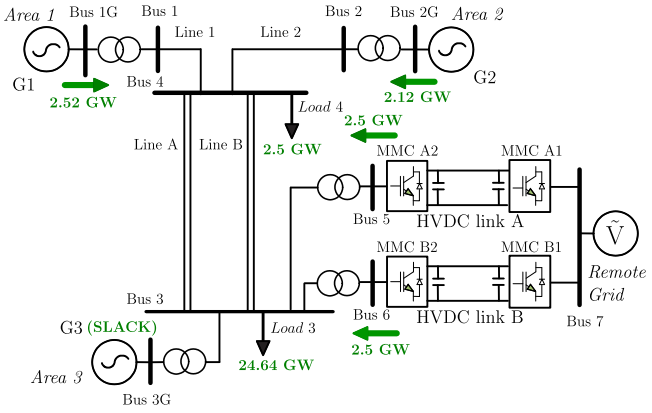


Fig. 9. Three-area GB test system with two MMC-based HVDC interconnections (HVDC link A and HVDC link B) to mainland Europe.

to exchange bulk amounts of power with mainland Europe (represented as an infinite voltage source). This arrangement represents one of the potential interconnections of a future European Super Grid [32], but it can also be seen as a future connection to off-shore wind farm locations [33].

The onshore GB test system consists of three generation areas: Area 1 (southern Scotland), Area 2 (northern Scotland) and Area 3 (England and Wales). In the test system, Line A and Line B are double circuit tie-lines that connect Area 1 (closely coupled) and Area 2 (relatively remote) to the large Area 3 (see [31] for further details). Each area is represented by an aggregated round rotor synchronous generator. These generators are steam turbine-driven, equipped with excitation control and local PSS, according to the control models used by the system operator National Grid (NG) in their dynamic system studies [33].

The two HVDC interconnectors are arranged as balanced monopoles as described in Section IV-B. The rectifier station set-points are 2.55 GW, 0.1 Gvar and the inverters are 1050 kV, 0.1 Gvar. The data for the converter stations and DC cable are presented in Table I. The cables used in the study are based on [3]. The power-rating of the converter stations is currently beyond the capability of any available individual converter design. For this reason each converter station is considered to consist of two 1.275 GW converters, to the same specification reported in [10], operated in parallel in order to achieve the desired power rating.

TABLE I
HVDC SYSTEM DATA

V_{dc}	Converter rated DC voltage	$\pm$525 kV
V_{ac}	Converter rated AC voltage	525 kV
P_{rated}	Converter rated power	2.55 GW
I_{max}	Converter arm current limit (peak)	2.8 kA
L^{up}, L^{low}	Arm inductances	140 mH
L^{ph}	Phase inductance	35 mH
X_{tf}	Transformer leakage reactance	14 %
l	DC line length	300 km
I_{rated}	DC line rated current	2.4 kA
R'	DC line resistance	0.0113 Ω/km
L'	DC line inductance	0.362 mH/km
C'	DC line capacitance	0.212 μF/km

The operating condition chosen for the GB system is very similar to the one described in [31]. It assumes a low demand scenario where the total synchronous generation is 22.14 GW and in addition 5 GW is supplied via the two HVDC interconnectors. The total system inertia is low in line with NG projected future scenarios [30] and equal to 93.5 GW·s. Loads have been modeled as constant impedance type. The spinning reserve in the test system is kept at 2.5 GW to secure it against the loss of a single interconnector. In the actual GB transmission network, the maximum possible infeed loss is currently 1.8 GW [34].

Given the time frame in which MMC overload can be expected to be sustained, we only focus on the primary frequency response in the GB transmission system. This is a service that performs rapid power changes within 10 s of a generator outage, which have to be sustained for further 20 s [35]. The objective is to prevent frequency from going outside certain security thresholds. For instance, the Security and Quality of Supply Standard (SQSS) in GB requires that frequency does not vary outside an acceptable range of $\pm$ 0.5 Hz for more than 60 seconds and NG further imposes a limit on the maximum frequency deviation of 0.8 Hz for large infrequent infeed losses [34]. In order to secure the system against these limits, sufficient power reserves need to be deployed. However, as the system evolves towards low inertia scenarios and larger maximum possible infeed loss due to new DC connections, frequency response from conventional sources alone would become insufficient [30]. Role of short-term overload capability of the planned MMC-based HVDC interconnectors in circumventing the above situation is demonstrated next through simulation results.

VII. SIMULATION RESULTS

Simulation results are presented in two subsections. The first analyzes the frequency service provision in the GB test network from an MMC-based HVDC interconnection with overload capability following the controllers introduced in Section V. The second one focuses on the controllers sensitivity to different temperature limits T_{max} for the IGBT modules to be exploited during overloaded operation. In both cases the frequency event under consideration corresponds to the outage of one of the two DC connections (HVDC link B) which occurs at $t = 10$ s, causing a 2.5 GW infeed loss in the GB grid. Note that the worst case scenario in which both HVDC links are operating at rated power in pre-fault condition is assumed, which results in narrow thermal margins available for overload.

A. MMC Overload for Frequency Service Provision

This subsection evaluates the performance of the described MMC overload control during frequency support. Three different cases are analyzed in the results presented in Fig. 10: 1) no frequency response from HVDC, 2) frequency response from HVDC with a frequency-power droop controller and 3) frequency response from HVDC with a maximum power release controller. For these simulations

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a safety limit of $T_{max} = 106^oC$ (10^oC above the maximum steady-state junction temperature observed) was set and $k_p = 0.1$ p.u., $k_i = 0.3$ p.u., $K = 0.5$ p.u.. Note that in the junction temperature curves presented next there is no cycle-by-cycle power ripple as the power-losses are derived from look-up tables characterized from a detailed switching model.

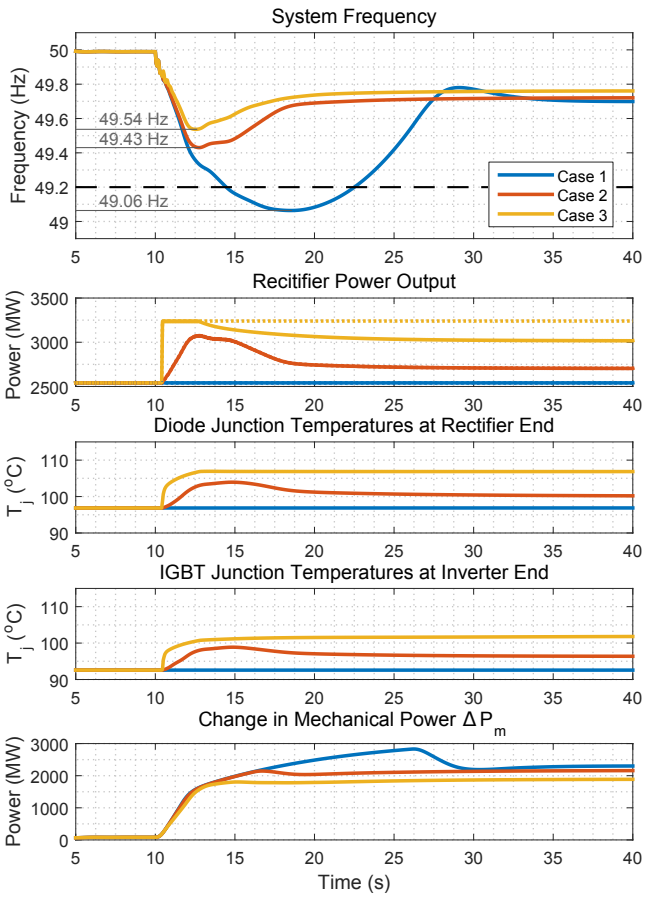


Fig. 10. System response to HVDC link B outage: 1) no frequency response from HVDC (blue traces); 2) frequency response from HVDC with a frequency-power droop controller (red traces); 3) frequency response from HVDC with a maximum power release controller (orange traces).

Without frequency support (blue traces), the system frequency drops significantly after outage of the HVDC link B and goes below the security limit of 49.2 Hz, despite the 2.5 GW spinning reserve allocation. The power at the rectifier terminal of HVDC link A is kept equal to 2.55 GW. As there is no change in the DC power transfers, the junction temperatures at rectifier and inverter terminals remain constant. The system frequency response is much improved when the support from HVDC link A was enabled through the overload capability. With the maximum power release controller (orange traces) the frequency reaches a nadir of 49.54 Hz, while with the droop controller (red traces) it reaches 49.43 Hz. In addition, the maximum power release controller is shown to improve the system RoCoF[2] to -0.29 Hz/s. With the droop controller this value is -0.32 Hz/s and without frequency support -0.33 Hz/s.

[2]RoCoF is calculated using a moving measuring window of 500 ms and then selecting the minimum value [36].

The difference between the RoCoFs achieved here is not much but this could be significant under low inertia scenarios [30]. The associated power changes at the rectifier terminal are depicted in the second subplot of Fig. 10. The final power (P'_{ref_1}) is seen in solid traces and the total requested power ($P_{ref_1} + P^*$) in dashed traces. For operation at a given active power set-point, the expected diode junction temperature within the lower IGBT module during rectifying operation will be higher than the IGBT junction temperature at an equivalent inverting power set-point. This is due to the higher thermal impedance from junction to ambient of the diode [22] in comparison to the IGBT. For this reason the limit P^{lim}_{therm} is set by the diode junction temperature at the rectifier end and so the transferred power is regulated to keep this temperature at the maximum allowable T_{max} value of 106^oC. This can be seen to be respected by both types of frequency support controllers. The performance of these two frequency controllers is found to be satisfactory, with the maximum release case making the most utilization of the available overload capacity. Note that, in the case of the droop controller, the converter is not thermally limited due to the droop gain chosen. The variation of the mechanical power ΔP_m of all three generators in the GB system is also shown in Fig. 10. This value is reduced by the frequency support from the HVDC link. This means that the spinning reserve requirements could be lowered while keeping the system within security limits when considering frequency service provision from MMC-based HVDC systems with overload capability.

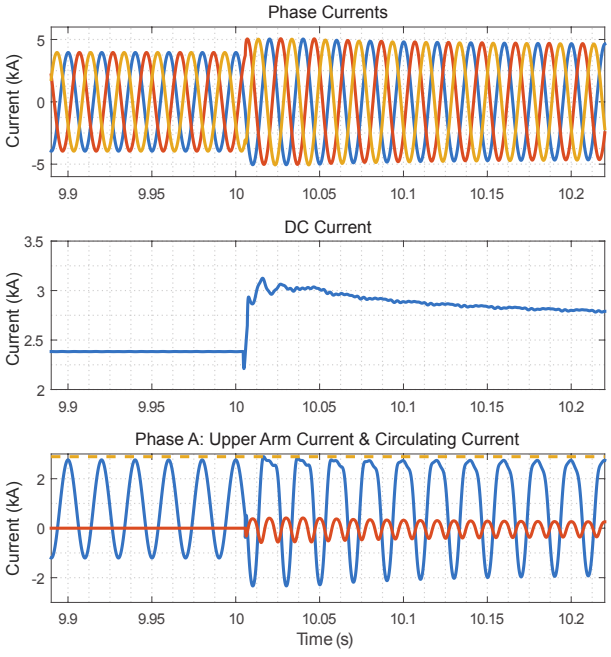
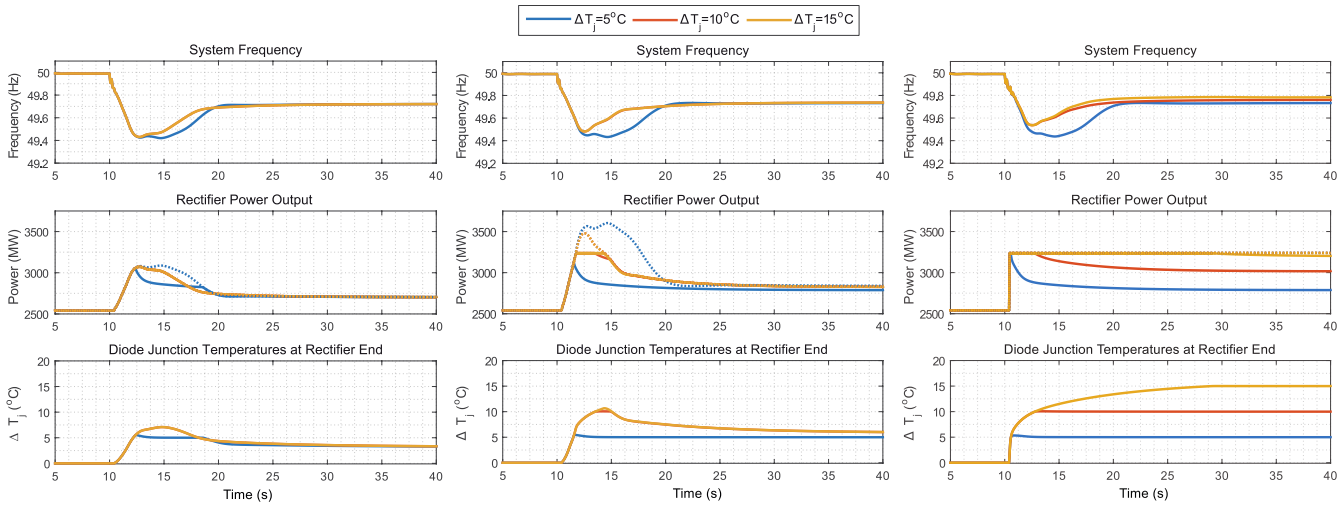


Fig. 11. Resulting converter current waveforms during frequency service provision using maximum power release controller (case 3).

Fig. 11 shows the currents within the rectifier converter for the maximum power release controller case. Harmonic currents start circulating to enable the converter overload capacity using the peak shaving technique described in Section IV-A. Similar curves are obtained for the frequency-power

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(a) Frequency-power droop controller with gain K (b) Frequency-power droop controller with gain $2K$ (c) Maximum power release controller

Fig. 12. Comparison of HVDC frequency support controllers for different $\Delta T_j = T_{max} - T_j$ values in terms of frequency variation, active power at rectifier end (set-point references in dashed lines, achieved active power with overload restrictions in solid lines) and diode temperature variation at rectifier end.

droop controller case, although they build up over a longer time and are not presented here due to space restrictions.

B. Sensitivity Analysis to Security Temperature Limit T_{max}

To account for these variable factors a sensitivity study on the available temperature margin was performed. Fig. 12 shows a comparison of three temperature margins of $\Delta T_j = T_{max} - T_j$ at 5, 10 and 15^oC, applied to three controller configurations: (a) frequency-power droop controller with gain K, (b) frequency-power droop controller with gain $2K$ and (c) maximum power release controller. The lower subplots in the figure show the junction temperatures of the diodes in the rectifier station since this is the limit that applies first and in turn sets the limit on the overload power, P^{lim}_{therm}.

In Fig. 12, for all three controllers, the frequency dip after the outage of HVDC link B is improved as the allowed temperature margin is increased. Considering the frequency-power droop controller with gain K (Fig. 11 (a)), the overload response with $\Delta T_j = 5^oC$ is subject to a limitation on the available power but at 10^oC and 15^oC it is not and the recovery of the frequency is quicker. With twice the droop gain (Fig. 12 (b)) higher powers are injected with limitation now seen for the 10^oC case. The unrestricted response for 15^oC is seen to give a quicker recovery but a broadly similar nadir. The third case, the maximum power release controller (Fig. 12 (c)) achieves the fastest recovery (but similar nadir) and achieves this for ΔT_j of 10 and 15^oC. At 5^oC the initial response only very briefly achieves the full overload of 127.5% and is rapidly reduced toward a long term overload of 110% with a consequently slow recovery of frequency. In the 15^oC case, the greater margin allows close to the 127.5% maximum overload to be deployed for 20 s with a slow reduction thereafter.

All frequency controllers, even those with a very small temperature margin available, show a significant positive impact on the frequency response of the overall system in comparison to the base case where no overload capacity is available. With proper consideration of the limitation of junction temperature to the available margin, MMC-based HVDC interconnections are capable of providing primary frequency reserve.

VIII. Conclusion

Exchange of frequency support through MMC-based HVDC systems with overload capability has been demonstrated in this paper. The overload of the MMC beyond its normal maximum power is achieved through harmonic circulating currents that limit the peak current through the semiconductors, enabling overloads of up to 127.5%. The available overload is dynamically set based upon the estimated junction temperatures of the IGBT devices, limiting the maximum temperature reached.

The efficacy of this short-term and dynamically limited overload was tested with two variants of a frequency support controller applied to an HVDC interconnector. Simulation results have been presented for a large disturbance in a representative AC transmission network, corresponding to the future Great Britain transmission grid. Significant improvements to the frequency nadir following a large outage of 2.5 GW were observed. Useful improvements in recovery times were also observed for temperatures margins as small as 5^oC and overloads of circa 5 s and so it is realistic to expect that overload operation for service provision in commercial schemes is feasible.

With greater use of non-synchronous sources, frequency response may become a functional requirement for future HVDC interconnectors. Oversizing converters to provide this service is unattractive but the short-term overload capability demonstrated here provides the headroom to deliver an effective service. It was also shown that the fast response from one HVDC link can significantly reduce the frequency nadir caused by the outage of a neighbouring link. This could notably reduce the burden of securing against the large infeed loss risk of future HVDC interconnectors. It must be acknowledged that the implementation of schemes described here would ultimately require a frequency support agreement between interconnected system operators (TSOs). Note that the

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proposed overload scheme is beneficial for the AC networks at both ends as it would reduce the frequency deviation in both grids. Exchange of frequency support would decrease the extent of over-frequency at the sending-end and under-frequency at the receiving-end. Specific payment schemes associated to the provision of this service are out of the scope of this work.

Finally, it is important to mention that the overload control technique for MMC-based HVDC links is generic and could be exploited to provide other forms of network support (e.g. power oscillation damping) through HVDC links and meshed DC grids.

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Inmaculada Martínez Sanz (S'13 - M'15) received the degree in Industrial Engineering from Universidad de Sevilla, Seville, Spain, in 2010 and the Ph.D. degree in Electrical and Electronic Engineering from Imperial College London, London, U.K., in 2015. She is currently a Research Associate at Imperial College London. Her research interests include power system dynamics and control, HVDC transmission and wind power.



Paul D. Judge (S'13 - M'17) received a B.Eng. (Hons) degree in electrical engineering from University College Dublin in 2012 and a PhD in Power Converter Design for HVDC Applications from the Control Power Group in Imperial College London in 2016, where he is currently a Research Associate. His main research areas are in power converter design and control, as well as power system integration aspects of HVDC technology.



Claudia Spallarossa (S' 12- M'16) received the Ph.D. degree in electrical engineering from Imperial College London, United Kingdom in 2015. During the Ph.D. the focus of her research was on voltage and frequency stability of mixed AC and DC transmission networks. Since 2016 she has been working at Mitsubishi Electric Europe as HVDC engineer. Her professional interests include protection of meshed HVDC offshore grids, HVDC circuit breakers and modular multilevel voltage source converters.



Balarko Chaudhuri (M'06 - SM'11) received the Ph.D. degree in Electrical and Electronic engineering from Imperial College London, London, U.K., in 2005 where he is presently a Reader in the Control and Power Research Group. His research interests include power systems stability, grid integration of renewables, HVDC, FACTS, demand response and smart grids. Dr Chaudhuri is an editor of the IEEE Transactions on Smart Grid and an associate editor of the IEEE Systems Journal and Elsevier Control Engineering Practice. He is a Fellow of the Institution of Engineering and Technology (IET) and a member of the International Council on Large Electric Systems (CIGRE).



Tim C. Green (M'89 - SM'02) received a B.Sc. (Eng) (first class honours) from Imperial College London, UK in 1986 and a Ph.D. from Heriot-Watt University, Edinburgh, UK in 1990. He is a Professor of Electrical Power Engineering at Imperial College London, and Director of the Energy Futures Lab with a role fostering interdisciplinary energy research. He also leads the HubNet consortium of UK universities. His research interest is in using the flexibility of power electronics to accommodate new generation patterns and new forms of load, such as EV charging, as part of the emerging smart grid. In HVDC he has contributed converter designs that reduce losses while also providing control functions assist AC system integration. In distribution systems, he has pioneered the use of soft open points and the study of stability of grid connected inverters.

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