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Department of Electrical and Electronic Engineering

Analysis and Design of Ultra-Low Power Electronic Circuits for Body Sounds Monitoring

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Declaration of Originality

I hereby certify that all the material in this thesis is on my own work, and I have properly acknowledged the sources of any work that is not my own. This thesis was not and will not be submitted to any other university or institution for fulfilling the requirements of a degree.

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Majd H. Eid
September 2017

Abstract

Chronic Cardiorespiratory diseases such as Sleep Apnea, Asthma, Obstructive Pulmonary Disease (COPD) and Atrial Fibrillation affect more than 780 million across the world. These diseases have a big diverse effect on the quality of patients' life and on the global economy as well. A major cause of these negative effects and economic burden is the traditional diagnoses method of these diseases, which suffer from many limitations. The main limitations are being expensive and not portable.

To improve the detection and monitoring of these diseases and reduce their impact on the patients' life, the idea of a remote diagnostic process for chronic respiratory and cardiac is proposed. The remote diagnostic process is composed of a wearable device that extracts the vital data of interest and algorithms that work on these data to extract disease related parameters that are useful in the diagnosis process. There is significant amount of work in the literature on different algorithms that extract different diseases related parameters from acoustic cardiorespiratory signals. However, there is a lack of true-low power devices to acquire these signals.

This thesis presents the analysis, design, implementation and testing of a low-power wearable system that acquires and monitors the sounds of cardiac and respiratory activities. The system was designed from the transistor level and fabricated using AMS 0.18µ 6M layer technology. This makes it the first wireless acoustic sensor that is completely designed at the transistor level and thus achieves the lowest power consumption and smallest size compared to other works reported in the literature. The chip was directly wire-bonded on a custom made round shaped PCB that has 23mm diameter and integrated with a miniature MEMS microphone to create the final system. Lab measurements shows that the system achieves good functionality at less than 560µW supplied from 1.3V battery and can last on continuous operation for more than 2 weeks when supplied from a Zinc Air P13 battery.

-to my parents-

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List of Abbreviations

Polysomnography	PSG
Electrocardiogram	ECG
World Health Organization	WHO
Obstructive pulmonary diseases	COPD
Atrial Fibrillation	AF
Sudden Arrhythmic Death Syndrome	SADS
Direct Digital Synthesizer	DDS
Signal to noise ratio	SNR
Obstructive Sleep Apnea	OPA
Application-Specific Integrated Circuit	ASIC
Analogue Front End	AFE
Parallel In Series Out	PSIO
Ampere hour	Ah
Coin cell	CC
Button cell	BC
Johnson Space centre	JSC
National Aeronautics and Space Administration	NASA
Commercial-Off-The-Shelf	COTS
Original Equipment Manufacturer	OEM
Microelectromechanical systems	MEMS
Electret condenser microphones	ECM

Lowest significant bit	LSB
Band pass filter	BPF
Low pass filter	LPF
High pass filter	HPF
Printed circuit board	PCB
Charge pump(s)	CP(s)
Switched capacitor	SC
Charge transfer switches	CTS
System on chip	SoC
Fall time	t_f
Rise time	t_r
Operational transconductance amplifier	OTA
Effective number of bits	ENOB
Transconductance	g_m
Common mode	CM
Proportional-to-absolute temperature	PTAT
Power-supply-rejection	PSR
Linear-dropout	LDO
Dynamic range	DR
Successive-Approximation Register	SAR
End of Conversion	EOC
Voltage controlled oscillator	VCO
On-Off keying	OOK
Effective series resistances	ESR
Total harmonic distortion	THD

List of Publications

Peer reviewed journals:

- *M.H Eid and E. Rodriguez Villegas, " Analysis and design of cross-coupled charge pumps for low power on chip applications" Microelectronics Journal, vol. 66, pp. 9-17, 2017.*

Peer reviewed Conferences:

- *S. Iranmanesh, M. Eid and E. Rodriguez-Villegas, "Optimizing simulation times in biomedical systems containing Quasi-Infinite Resistors*," *2016 IEEE Nordic Circuits and Systems Conference (NORCAS), Copenhagen, 2016*

- *M.H. Eid and E. Rodriguez Villegas, " Analysis of reversion loss in charge pumps and its impact on efficiency for low power design*," *2017 15th IEEE International New Circuits and Systems Conference (NEWCAS)*, *Strasbourg, Franc, June 2017*

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Chapter 1: Introduction

1.1 Overview

Respiratory and cardiac chronic diseases such as Sleep Apnea, Asthma, Chronic Obstructive Pulmonary Disease (COPD) and Atrial Fibrillation affect many individuals worldwide. It is estimated that approximately 780 million people across the world are affected by these conditions [1-3]. Respiratory and cardiac chronic diseases result in a heavy financial burden on the global economy, estimated to be more than $2.1 trillion dollars in 2010 [4]. They also reduce the patient's quality of life as they cause, amongst others, irregular sleeping patterns, loss of productivity and breathing difficulties. Asthma and COPD both directly cause the death of more than 3.2 million people each year [5], whereas Sleep Apnea and Atrial Fibrillation greatly increase the risk of other fatal conditions, including heart failure and stroke [6]. Continuous monitoring of cardiac and respiratory signals is essential in managing and diagnosing these diseases.

Sleep Apnea is traditionally diagnosed via a Polysomnography (PSG) test; Asthma and COPD are diagnosed via a Spirometry test; and Atrial Fibrillation requires continuous monitoring of cardiac activity. These diagnostic methods suffer from several limitations including:

- They are expensive. As an illustration, the average cost of a PSG test is $1000 per night [7].
- They cannot be used with certain individuals. For example, spirometry cannot be used with children and patients who have had recent surgical operations [8-9].
- They are restrictive: Patients are required to make frequent or long visits to the clinic, which may restrict their daily life.

This information indicate that there is a great demand for affordable and portable remote diagnostic systems for chronic cardio-respiratory problems that can be used with all types of patients. A remote diagnostic system should remotely monitor and diagnose patients while they are in their homes because this would greatly improve the detection and monitoring of these diseases and reduce their impact on the patients' life. This is because the portable remote

diagnostic process will allow the patients to be continuously monitored and remotely diagnosed which decreases the frequency of hospital's visit and thus allows them to have a less restrictive life.

The remote diagnostic system would be composed of two parts: a wearable device to acquire physiological data and algorithms that extract diseases related parameters from these data (such as heart rate, breathing rate and lung volume). After conducting a literature research, it was found out that there is a lot of work on algorithms that extract diseases related parameters from physiological signals as will be shown in chapter 2. However, there is lack of a true low-power wearable device to acquire these signals. The low power feature of the wearable device is of great importance as this allows the use of small batteries while achieving a reasonable operating life. This allows the realisation of a miniaturized and low weight wearable system, which makes it more convenient, attractive and socially acceptable for the patients to use. Additionally, this can be first step in transforming conventional rigid electronics into transparent flexible one. Therefore, the aim of the work in this thesis is to design, implement and test a miniature ultra-low power wireless acoustic monitoring system for cardiac and respiratory sound signals.

The main contributions of the thesis are:

- To the best of the author's knowledge, the system described in this work is the first wireless acoustic sensor that is completely designed at the transistor level and thus achieves the lowest power consumption and smallest size compared to other works reported in the literature.
- A novel analysis of the operation of the cross-coupled charge pump and different losses mechanisms within it is presented. Based on this analysis, a design procedure to maximize the cross-coupled charge pump's efficiency was proposed.
- A simple and effective data reduction algorithm based on speech elimination was proposed. The circuit that implements the algorithm was analysed in detail to allow an ultra-low power implementation.

1.2 System Architecture

The proposed monitoring system is composed of two parts: a wearable miniature low-power device that is mounted on the neck to acquire acoustic respiratory and cardiac signals and a second RF module that communicates with a base station. This is illustrated in Fig. 1.1.

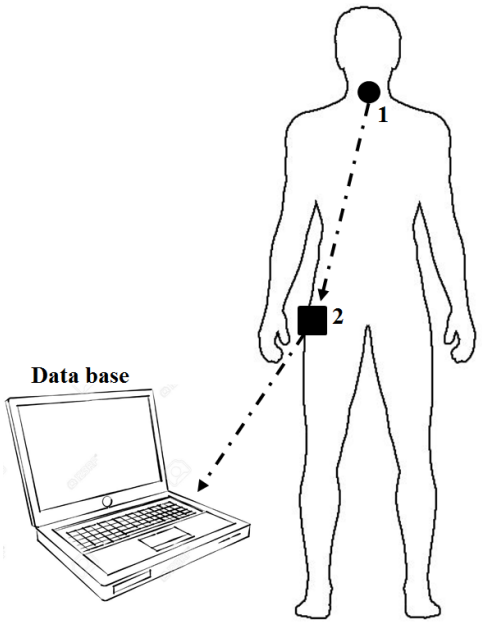


Fig. 1.1. Diagram illustrating the concept of the proposed low power wearable system

The wearable device (labelled as **1**) is placed on the neck. It is composed of a ASIC chip and an acoustic senor and it detects cardiac and respiratory sounds. A secondary small size device (labelled as **2**) is placed inside the user's pocket and it communicates with the base station. The wearable device communicates with the secondary device via RF transmission in the form of data pulses (or packets). The secondary device in turn sends these data packets to the database. Different algorithms can then be applied to the received data to extract disease related parameters and then upload this to cloud storage where it can be accessed by physicians. This architecture allows the wearable device to be designed with extreme low power because it only needs to communicate with a short range device. The secondary device is more power consuming than the wearable device and therefore a bigger battery is required. However this will not cause any discomfort or inconvenience to the user because the secondary device is placed in the pocket and hence its size or weight is not of any concern. The required specification for the miniaturized warble devices are summarized in Table 1.1. The design and implementation of each of these devices is discussed in Chapter 2 section 2.3.

Table 1.1. Required specifications of the wearable device

Parameter	Specification
Weight	**Less than 2g**
Size	**Less than 25mm diameter circular shape**
Operation life	**More than 72 hours**
Discrete factor	**2***
Comfortability	**1****
Ease of use	**Takes less than 1min to wear**

* Discrete factor is an indication of how discrete the device is when it is used in public. It has a scale from 0-5, where 0 being completely invisible and 5 being very visible.

** Comfortability refers to how much the device is comfortable to wear. It has a scale form 0-5, where 0 means that the users feel nothing when watering it and 5 is very uncomfortable to wear.

1.3 Thesis structure

The Thesis is organised in six chapters as follows:

1. Chapter 2 gives a background of chronic cardiorespiratory diseases including statistical data about the number of people affected with these diseases and the financial and physiological burden they cause. The traditional diagnosis methods for these diseases and their limitations are presented as well. The idea of a remote diagnostic system and the different parts within it are discussed. The top-level diagram of a low-power wearable system is described and the specifications of the circuits within it were derived.
2. Chapter 3 gives an overview about charge pump topologies and a suitable topology for this work is described. Different loss mechanisms within the charge pump circuit are derived and a design methodology to maximize its efficiency is proposed. Based on this methodology, a charge pump is designed and its functionality experimentally verified.
3. Chapter 4 describes the design and implementation of the analogue front end. This includes all the circuit blocks within it and the biasing of these circuits as well. The

results from statistical Monte Carlo simulations are presented to show the effect of mismatch and process variations on the performance of the front end.

4. Chapter 5 starts by describing a data reduction method that reduces the amount of transmitted data from the wearable part of the system. The circuit implementation of the data reduction method is presented and its functionality experimentally verified.
5. Chapter 6 presents the implementation of the Analog to Digital Converter (ADC) and the transmitter. Lab measurements of the whole system that verify its functionality are presented as well.
6. Chapter 7 provides the conclusion of the thesis and mentions future work that needs to be done.

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Chapter 2: Chronic Diseases, Remote Diagnosing and System Level Design

2.1 Respiratory and Cardiac chronic diseases

Several respiratory and cardiac chronic diseases affect a large number of individuals worldwide. According to the definition of the U.S. National Centre for Health Statistics, a chronic disease is a disease that lasts longer than 3 months and generally cannot be prevented by vaccines or cured by medications [1]. Moreover, chronic diseases generally have a slow progression over time [2]. This implies that such diseases require continuous monitoring to assess their progression and severity on the patients' wellbeing over time.

2.1.1 Respiratory diseases

A category of chronic diseases, known as respiratory chronic conditions, affect different parts of the respiratory system such as the air pathways and lungs. One of such diseases is Obstructive Sleep Apnea. Obstructive Sleep Apnea is a breathing disorder that occurs when normal breathing ceases due to the relaxation of the muscles and soft tissues in the throat during sleep, as shown in Fig. 2.1.

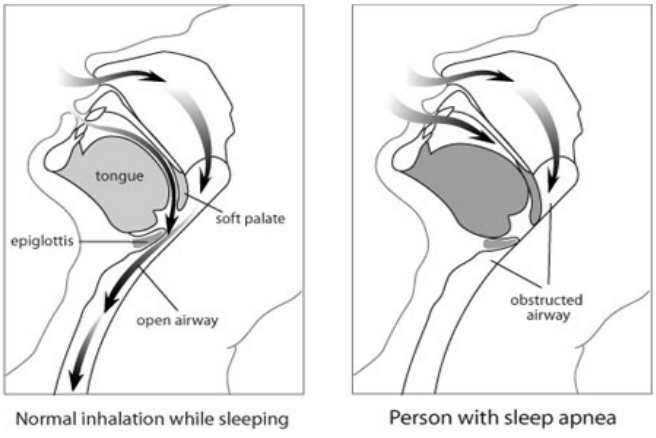


Fig. 2.1. Illustrative diagram explaining Obstructive Sleep Apnea [3]

The relaxation of the muscles and soft tissues in the throat obstructs the air pathway in the throat and stops normal breathing for ten or more seconds. This cessation of breathing is known as an Apnea episode. A patient is diagnosed with Sleep Apnea if they have at least five Apnea episodes during one hour of sleep [4]. Sleep Apnea affects 3% of children [5], 2% and 4% of female and male adults worldwide [6], respectively. Up to 90% of these cases remain undiagnosed [7]. Sleep apnea causes sleep disruption in the patient, which can lead to systemic hypertension, daytime fatigue and severe snoring [8]. Moreover, it has been linked to stroke, diabetes and cardiovascular diseases [9-11]. The gold standard in diagnosing Sleep Apnea is Polysomnography (PSG), a test under which the patient undergoes an overnight sleep in an equipped sleep laboratory to continuously monitor their physiological signals during sleep [12]. A PSG test involves monitoring and recording different physiological signals such as respiratory activity, blood oxygen levels (SPO_2), electrocardiogram (ECG) and many other signals using bulky systems and wires. These bulky wirings cause sleep discomfort to the patient and increase the risk of misdiagnosis [13]. Moreover, a PSG test is time-consuming, labor intensive and expensive [14]. The cost of a PSG test ranges from $600-$5000 with an average of $1000 per night [15]. Developing a wearable and continuous monitoring system for breathing signals would be of great benefit for the patients as it would potentially allow pre-screening of the condition at home. A system of this kind would hence lay the foundations of a remote diagnostic process to allow patients to be diagnosed at the comfort of their own homes at an affordable price. This remote diagnostic process would therefore be more sustainable and more reachable for a larger population compared to the traditional PSG method. This will result in a decrease in the number of undiagnosed cases and help to reduce further complications from the illness.

A second chronic respiratory disorder is Asthma. Asthma occurs when the air passages in the lungs are inflamed, which results in a temporary narrowing of the airways that carry oxygen to these organs, as shown in Fig. 2.2 [16]. This causes frequent wheezing sounds, coughing, chest tightness and shortness of breath [17]. The World Health Organization estimates that 300 million people worldwide suffer from Asthma, with 250,000 annual deaths caused by the disease [18]. Asthma is a leading cause for loss of productivity, with nearly 11 million students missing school days and 14 million adults missing work days in the U.S. alone [19]. Diagnosing and continuously monitoring Asthma is crucial to control its symptoms and allow patients to live a normal active life.

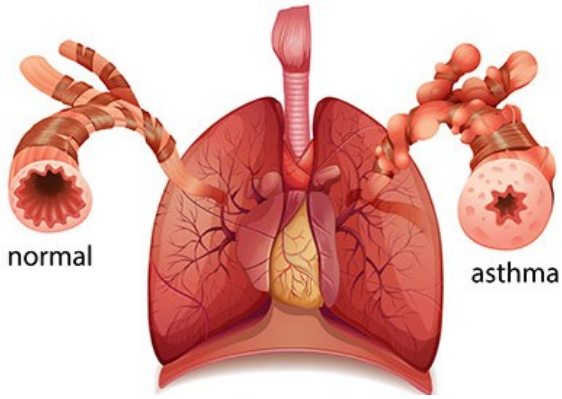


Fig. 2.2. Diagram illustrating narrowing of the airways caused by Asthma [16]

Asthma is diagnosed and monitored via a Spirometry test. This test is carried out using a Spirometer, which is a machine attached by a cable to a mouth piece and used for measuring the volume and flow of air inhaled and exhaled by the lungs. During the test, the patient is asked to take a very deep breath to inhale as much air as possible and then exhale into the mouth piece of the Spirometer with full force until no air left in their lungs [20]. Spirometry is generally a low-risk test. However, because of the strong exhalation during the test, it is not performed in patients that have had a recent heart attack, eye surgery, pneumothorax or an unstable angina [21]. Furthermore, diagnosing Asthma via Spirometry is challenging task for children under 6 years old because they do not easily comply with the test's requirements [22]. Diagnosing and monitoring Asthma requires frequent visits to the physician to perform Spirometry, which makes it an inconvenient diagnosis process over the long term. The total annual Asthma costs in the U.S was $56 billion in 2011 [23]. The same report in [23] states that the average annual healthcare expenditure on Asthma in the U.S between the years 2004 to 2006 was $5322 per person, with 22% of this cost ($1179) due to outpatient visits. The costs due to the outpatient visit can be greatly reduced if the patient can be remotely monitored away from the hospital.

A third type of chronic respiratory disease is Chronic Obstructive Pulmonary Disease (COPD). COPD describes a group of lung conditions that make it difficult to empty air out of the lungs because the airways have been narrowed. Its symptoms include shortness of breath, coughing, wheezing and sputum production. The diagnosis of COPD is similar to Asthma. A Spirometry test is carried out to measure the capacity of the lungs and how quickly they can be emptied from air. It was estimated that COPD affected around 174.5 million people across the

globe in 2015, with 3.2 million deaths from the diseases [24]. The global economic cost due to COPD was estimated at $2.1 trillion in 2010 and is projected to rise to $4.1 trillion in 2030 [25]. The economic cost is incurred in the form of direct and indirect costs. COPD causes a 70% and 50% reduction in the physical exertion and the sleeping pattern of the patients, respectively [26]. This leads to disabling effects from the disease that manifest as absence days from work, which contribute to the indirect costs. On the other hand, direct costs account for 60% of the total costs of the disease. The direct costs are related to the detection, treatment, prevention, and rehabilitation costs. As an example, out of the total direct costs, the total non-medication and hospitalization costs in the U.S. range from $1,170-$10,050 per patient, depending on the severity of the diseases [26]. These costs include: physician office visits, diagnosis and home care. These could be greatly reduced if the disease could be monitored and diagnosed remotely.

2.1.2 Heart Diseases and other conditions

Another category of chronic diseases are cardiac related disorders. Atrial Fibrillation (AF) is a heart condition that causes irregular and sometimes abnormally fast heart rhythm. The global number of individuals with AF in 2010 was estimated to be around 33.5 million, with 62.4% of individuals being males and 37.6% females [27]. AF can cause further complications and symptoms such as tiredness, shortness of breath and dizziness. However, some patients only have mild symptoms that can be easily overlooked while others have no symptoms at all. AF increases the risk of a stroke by four to five times [28] and can even lead to heart failure [29] if it remains untreated. The total economic burden in the U.S due to AF was estimated to be around $6.65 billion per year, with 23% of these costs ($1.53 billion) being related to AF management, including outpatient care and testing [30].

Lastly, a fatal condition that is not a chronic disease but is related to breathing and cardiac failures is Sudden Arrhythmic Death Syndrome (SADS). SADS occurs because of irregular heart rhythm and sudden cessation of breathing. It was estimated by the American heart Association in 2017 that approximately 210,000 Americans die each year due to SADS, at which 10%-12% of them are infants [31]. By continuously monitoring cardiac and respiratory signals, it may be possible to reduce the number of deaths due to SADS by seeking a faster medical intervention.

2.2 Diagnosis Process

From the previous section, the limitation of the traditional diagnosis methods can be clearly seen, such as being expensive, impose a restriction of the patients' life and cannot be used with certain individuals. Therefore, there is a great demand for an affordable and convenient remote diagnostic system for continuous monitoring of respiratory and cardiac chronic diseases. The diagnostic system should be based on continuous monitoring of the patient's vital signals and it must provide accuracy comparable or even better than the in-clinic processes without causing any discomfort to the patients. In recent years, there has been a great effort in the development of affordable and accurate remote diagnostic systems for respiratory and cardiac diseases. These diagnostic systems are composed of two major parts: a wearable device that acquires the patient's vital signals via a sensor, and algorithms to extract disease related parameters that are useful in the diagnosis process. The key parameters in diagnosing respiratory and cardiac diseases are lung volume, rate of breathing and respiratory flow and heart rate [32, 33]. In the next sections, the two major parts of the remote diagnostic system (data acquisition and diagnostic algorithms) will be discussed individually.

2.2.1 Data Acquisition

This subsection reviews different detection methods for breathing and cardiac signals in order to select the most suitable one for the development of a miniature, wearable and low power device to continuously monitor vital signals. Once a detection method is chosen, different locations where the sensor can be placed are discussed to select the optimum position in order to obtain the best signal quality.

2.2.1.1 Detection Methods and Sensors

Breathing and cardiac activities can be detected in a variety of ways that sense different changes that occur in the body due to respiration and blood circulation. The first method to detect breathing is by placing a mask over the mouth and nose or a thermocouple under the nose. This measures the change of air's temperature in this region due to inhalation and exhalation [34]. This method of detection cannot however detect cardiac activity. It is also very non-discrete and thus unsuitable for the application in this work.

A second method to detect breathing is by measuring the expansion and contraction of the chest provoked by respiratory efforts. This is measured via an accelerometer sensor embedded in a strap that is placed across the chest [35]. The accelerometer records the thoracic movement during inhalation and exhalation and thus indicates breathing activity. This method can be also used to detect the cardiac rhythms [36], but is not suitable at all for a miniature device as the belt size is too large and not discrete to wear.

A third detection method of respiratory and cardiac activity is by measuring the electrical impedance of the thorax (the region around lung and heart) [37]. This method is based on the fact that breathing and heart pumping activities change the impedance distribution in the human body due to the flow of non-conductive air in the body during respiration (high impedance) and the movement of conductive blood during cardiac activity (low impedance). The electrical impedance detection method is summarized as follows: A coil is placed near the body (identified as the excitation coil) and is driven with a sinusoidal voltage to create a magnetic field. When this magnetic field is coupled to the conductive body tissues, it creates eddy currents that flow in these tissues. The eddy currents flowing in the conductive tissues re-induce a magnetic field that could be measured with another nearby coil known as the measurement coil. This detection method requires Direct Digital Synthesizer (DDS) for the signal generation, which consumes too much power.

A fourth method to detect breathing and heart signals is based on optical recording from the camera of a mobile phone [38]. This method uses the mobile phone's camera and the white LED (flashlight) to detect subtle colour changes in the skin. This detection method provides an accurate estimation of breathing and heart rate. However, this detection method is not continuous and cannot be used during sleep because it requires the user to manually place their index finger on the phone's camera lens.

All the previously mentioned detection methods have been shown to be unsuitable for a miniature low power wearable device because they require large power to operate, are non-discreet and too bulky to wear, or cannot be used for continuous monitoring. Therefore, the only option left for detecting breathing and cardiac activity is acoustic detection. Acoustic detection is achieved via a microphone that converts sound vibrations into electrical voltages. The microphone can be chosen with ultra-small size and very little power consumption. This detection method therefore satisfies all the requirements that are required in a miniature wearable

low-power continuous monitoring system. The microphone details are described in Section 2.3.1.2.

2.2.1.2 Acoustic signal generation

After choosing the acoustic detection method of cardiac and respiratory signals using a microphone, it is useful to consider the mechanism at which respiratory and cardiac sounds are generated and how they propagate through the body to different possible detection locations. This is important because it helps to determine the optimum location where the sensor must be mounted to acquire the *best* acoustic signal. In this context, the word *"best"* refers to maximizing the signal-to-noise ratio (SNR) of the acquired signals.

A. Respiratory sounds

The respiratory system is a highly complex biological system that is responsible for transferring air to the lungs (inhaling), where the oxygen in the freshly inhaled air is exchanged with carbon dioxide via a diffusion process, and then expels carbon dioxide outside the body (exhaling). The main parts of the respiratory system are the pharynx, larynx, trachea, lungs and diaphragm. Its drawing is shown in Fig. 2.3. The pharynx, larynx and the trachea are responsible for moving gases inside and outside the body. The lungs are where the gas exchange occurs. The diaphragm is a dome-shaped muscled that initiates the flow of air to-and-from the lungs by altering the pressure inside them [39].

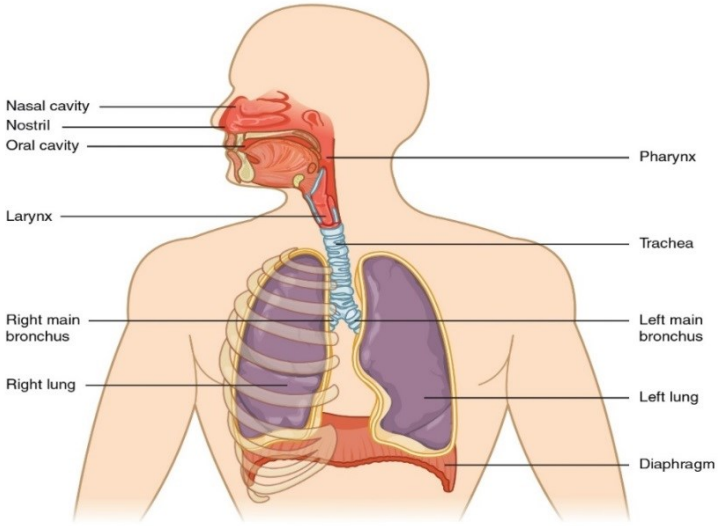


Fig. 2.3. Simplified anatomy of the respiratory system [39]

The process of inhaling is initiated by the contraction of the intercostal muscles (muscles on the ribcage), which causes the ribcage to expand. The expansion of the ribcage forces the diaphragm to contract downwards, which increases the volume of the chest. This makes the air pressures inside the lungs lower than the atmosphere and thus air is sucked into the lungs. The exact opposite process happens during exhalation: the intercostal muscles relax causing the ribcage to contract. The ribcage contraction forces the diaphragm to release upwards decreasing the volume of the chest. This increases the pressures inside the lungs above the atmospheric pressure, which forces the air outside the lungs.

The relationship between the flow rate of air inside and outside the body and the generation of respiratory sounds can be explained by looking at the laws of fluid mechanics. The mechanism at which a fluid (or gas) flows inside a cylindrical tube can be divided into two different ways depending on its flow rate. The first flow mechanism is known as the laminar flow and this is when the fluid flows in a steady fixed direction parallel to the cylinder tube as shown in Fig. 2.4 (a). During laminar flow, the outer parts of the fluid near the cylinder walls move at a slower speed than the central part of it and this is represented by shorter arrows in Fig. 2.4. The second flow mechanism is known as turbulent flow and is characterized by a chaotic and random movement of the fluid (or gas particles) inside the cylindrical tube, which occurs due to the chaotic change in pressure and flow velocity. The mechanism at which a fluid flows inside a cylindrical tube is dependent on its characteristic, velocity and the diameter of the cylinder. A mathematical tool that is used to assess the mechanism of fluid's flow in a cylindrical tube is the Reynolds number (*Re)* and is given as [40]:

$$Re = \frac{\rho v D}{\mu} \tag{2.1}$$

Where ρ is the fluid's density, v is the fluid's average velocity, D is the tube's diameter and μ the viscosity of the fluid. For a given tube's diameter, the velocity at which the flow of fluid changes mechanism is defined as the *critical velocity*. At that velocity, the Reynold's number is defined as the *critical Reynolds number*($Re_{critical}$). A laminar flow is achieved if the Reynold's number of the fluid is less than the critical Reynold number of the medium it flows in, and vice versa for the turbulent flow. This whole process is summarized in Fig. 2.4.

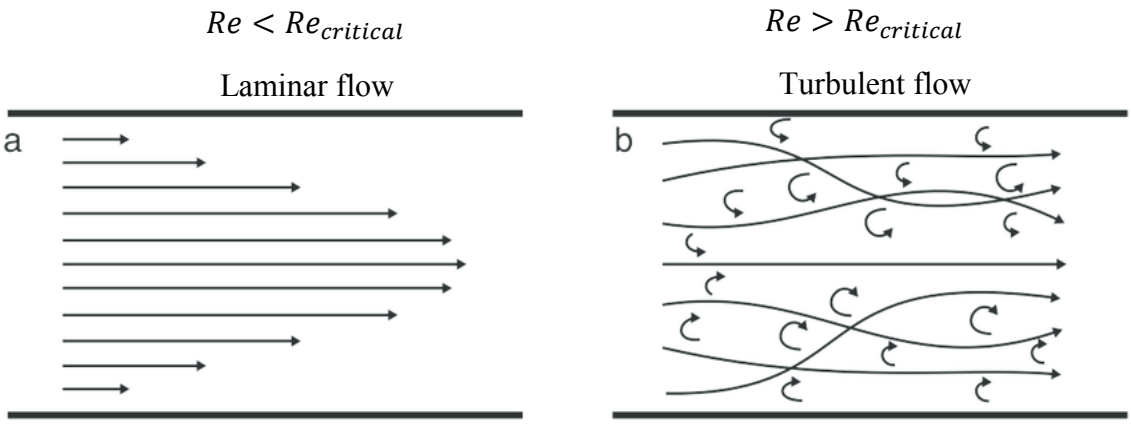


Fig. 2.4. Diagram explaining the laminar and turbulent flow mechanisms and how they are related to the critical Reynold's number [41]

Note that the Reynold's number is not only dependent on the fluid's characteristics, but also on the dimensions of the medium where the fluid flows in. This means that the same fluid with same flow rate will have a different Reynold number when it flows in different cylindrical tubes and thus a different flow mechanism.

Only a turbulent airflow mechanism generates acoustic sounds in the trachea [42]. Therefore, the Reynold's number of the trachea can be used to estimate the critical flow rate (velocity) of air that is needed to generate acoustic respiration sounds. The estimated Reynold's number of the respiratory tract is between 1800-2700 [43]. It was estimated that an air flow of 0.3 L/s in the trachea results in a Reynold number of 2900 [44], which results in a turbulent motion of air particles and thus generation of acoustic respiratory sounds in the trachea. This airflow was detected at the junction of the trachea and larynx, which is a suitable position to mount the microphone (and the wearable device) on. All breathing sounds have a flow rate greater than 0.3 L/s [45] and therefore all breathing activity, if it exists, can be acoustically detected from that location.

B. Cardiac sounds

The heart is the main organ in the cardiovascular system and is responsible for taking in deoxygenated blood from the body through the veins and then delivers it to the lungs for oxygenation before pumping it into the body through various arteries. The structure of the heart is perfectly built for such mechanism. It is composed of four chambers (to receive and pump blood), four valves (to prevent backwards flow of blood) and four main arteries (which act as

transporters of blood to-and-from the heart). The heart's two upper chambers are known as the left and right atria, and two lower chambers which are known as the left and right ventricles. The heart valves are: mitral, tricuspid, aortic and pulmonic valves. The main arteries are: the aorta, superior vena cava, the inferior vena cava and the pulmonary artery. Its diagram is shown in Fig. 2.5 [46].

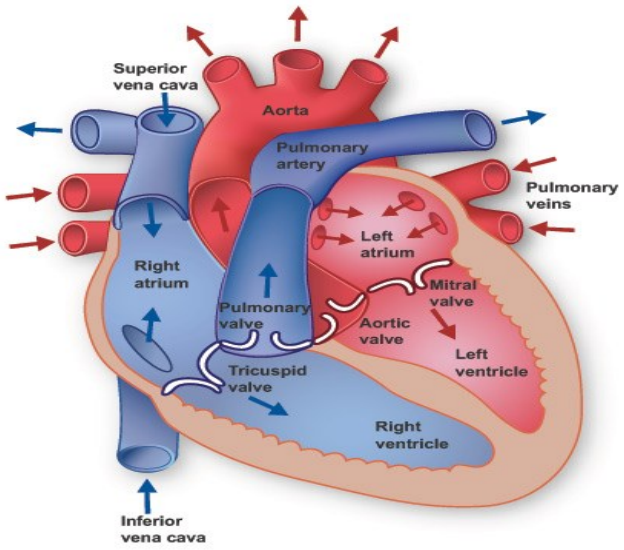


Fig. 2.5. Anatomy of the heart showing the main chambers, valves and arteries [46]

The cardiac cycle begins as deoxygenated blood flows from the body into the right atrium via the superior vena cava and inferior vena cava. In the next phase of the cycle, the right atrium contracts pumping blood into right ventricle through the tricuspid valve. Once the right ventricles are filled with blood, the tricuspid valve closes to prevent blood flowing back into the atrium. The right ventricle contracts forcing the pulmonary valve to open as blood is pumped into the pulmonary artery. Blood then travel to the lungs and the pulmonary valve closes. At the same time, the right atrium relaxes ready to accept the next intake of blood. In the lungs, the blood picks up oxygen and release carbon dioxide. Oxygenated blood flows from the lungs into the left atrium via the pulmonary veins. The left atrium contracts to pump blood into the left ventricle through the mitral valve. Once the left ventricle has filled with blood, the mitral valve closes. Next, the left ventricle contracts, forcing the aortic valve to open allowing blood to be pumped into the aorta and from there around the body. The aortic valve closes to prevent blood flowing

back into the left ventricle and the left ventricle relaxes ready to accept the net intake of blood, at which now cardiac cycle is complete.

Heart sounds generate due to the turbulence caused by the closure of the heart valves. A normal heart produces two sounds that sound like "*lub dub"*. The "*lub"* like sound is known as the S_1 sounds and is composed of two components: M_1 and T_1. M_1 is caused by the closure of the mitral valve, while T_1 is caused by the closure of the tricuspid valve at the start of systole (time when heart's muscles contract). The "*dub"* like sound is known as the S_2 sound at the end of the systole and is composed of A_2 and P_2 sounds. The A_2 sound component is caused by the closure of the aortic valve, while P_2 is caused by the closure of the pulmonary valve. The heart sound waves then travel to the various detection sites within the body like any sound wave travelling through a medium.

2.2.1.3 Sensor Location

The microphone's location will greatly alter the detected signal and therefore the selected location must maximize the detected signal's SNR. The chest and neck area are the two main locations where cardiac and respiratory sounds could be detected. A study performed by Kaniusas "et al" [47] compares the strength of the acoustic respiratory and cardiac signals detected from different locations via a microphone. The locations are the neck and thoracic region as shown in Fig. 2.6.

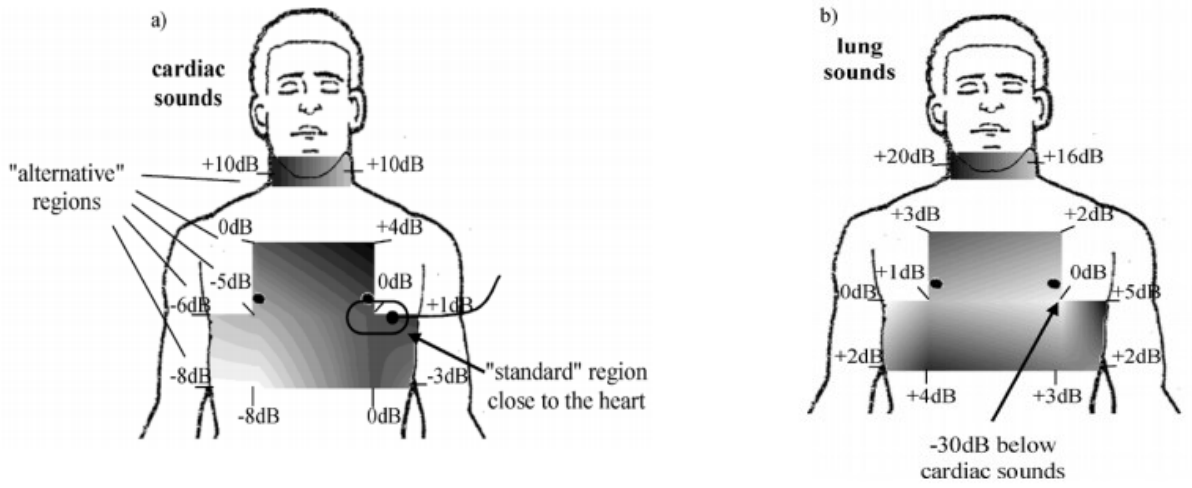


Fig. 2.6. Variations in the acoustic signal strength when detected from different locations from the neck and thoracic region via a microphone. The figure is directly taken from the study performed by Kaniusas "et al" in [47]

The study showed that the acoustic signal strength of respiration sounds is 30 times weaker (30dB lower) than cardiac sounds in the chest region over the heart. The same study also showed that in the neck region, the ratio between cardiac and respiratory sounds' amplitudes improves. Respiration sounds are only 10 times weaker (20dB lower) than cardiac sounds in the neck region. Moreover, gentle breathing sounds are only detectable in the throat region because low air velocity turbulence is only found in the trachea as explained in Section 2.2.1.2. Additionally, the neck area tends to carry less fat than the chest area which provides a significant advantage in detecting the vital signals, especially for overweight people. For all these reasons, the simultaneous detection of cardiac and heart sounds is optimum in the neck region.

Within the neck region, there are two major locations where the microphone could be placed: either on the sides of the neck or on the suprasternal notch. There is not much research in the literature that compares how the location of the microphone on the neck affects the signal's power. The argument between Gavriely [48] and Charbonneau [49] about this topic in 1984 does not lead to any conclusive results. A more recent meaningful experiment that compares the amplitude of the detected acoustic signal at different regions of the neck was conducted by Corbishley in 2008 [50] and gives a conclusive answer about this debate. The experiment measured breathing signals at normal rest on the side of the neck and the suprasternal notch, and the power spectral density (PSD) of the obtained signals was plotted. The results show that the signal detected from the suprasternal notch has greater power in the frequency range 400Hz-800Hz compared to the signal detected from the side of the neck. This is because the suprasternal notch is located directly on the trachea, unlike the side of neck that is located further from the trachea with muscle and fat tissues in-between them that filter out the signal. This section has brought sufficient evidence to suggest that the simultaneous detection of cardiac and respiratory sounds is optimal from the suprasternal notch and thus it was the chosen location.

2.2.2 Algorithms

In this subsection, different algorithms that extract different cardiac and respiratory disease related parameters (such as respiratory rate, respiratory flow, lung volumes and heart rate) are reviewed. These algorithms constitute the first half the remote diagnostic process, and the overall accuracy of the diagnosis depends on their accuracy. The algorithms that are reviewed here use

data from acoustic sensors and perform signal processing algorithms on them to extract the related parameters.

There are several algorithms proposed by Rodriguez-Villegas' research lab that extract several cardiac and respiratory disease related parameters, such as lung volumes, respiratory rate and heart rate [33, 51, 52]. The work in [33] reports an algorithm that automatically estimates the lung tidal volumes from an acoustic signal obtained from a microphone sensor placed on the suprasternal notch. This is the first algorithm that obtains tidal lung volumes from respiratory flow, and has showed very promising results. The results from the algorithm were compared against the results obtained using Spirometry test as the gold-standard and have shown an accuracy of 96%.

The work reported in [51] presents the results obtained from a wearable device for apnea detection developed by the same group. The device consists of a wearable sensor, which will be discussed later, and a novel signal-processing algorithm for apnea detection. The algorithm first separates the wanted signal (breathing) from the unwanted noise (heart signal, speech and movement interference) and then computes the time and frequency characteristics of the breathing signal. This results in 88.6% sensitivity and 99.6% specificity. This device can also be used to monitor patients against SADS because it continuously monitors the respiration rate of the subject.

Rodriguez-Villegas' group has also proposed a novel algorithm that extracts the heart rate from an acoustic signal acquired from the suprasternal notch in [52]. This algorithm is novel in the sense that it extracts the heart rate from cardiac sounds obtained from an acoustic sensor placed over the neck rather than from the chest area as other conventional algorithms [53-55]. The algorithm achieves 90.7% accuracy compared to heart rate values extracted from commercial devices. This algorithm allows the integration of a heart and respiratory monitor into a single wearable device that can be used for diagnosing cardiovascular and respiratory diseases.

The acoustic signal input for the aforementioned algorithms was acquired from a wearable acoustic sensor developed by the same group [56, 57]. This acoustic sensor is not an Application-Specific Integrated Circuit (ASIC) system and was made from off the shelf components, which is not an optimum solution for low power consumption. The present wearable device uses two Zinc air P13 batteries with a total current rating of 300mAh and they

last for 48 hours on continuous operation. Using a bigger battery with the current system is not an option as this would increase the size and weight of the system making it less comfortable and convenient to use. Alternatively, the system could be optimized and reduced even further by designing and implementing it with full custom integrated circuits. This would lead to a new system with fewer batteries that last even longer than the current system. These changes will drastically improve the overall system and make it more convenient, attractive and socially acceptable for the patients to use, as it will be of a smaller size and operate for longer duration.

Another algorithm that uses acoustic signal obtained from the neck is the one developed by Yadollahi and Moussavi in [58], that estimates the respiratory airflow from tracheal sound recordings. Their algorithm first cancels the effect of heart sounds on the entropy of the tracheal sound, and then use the latter (entropy of tracheal sounds) to estimate flow. This resulted in an overall accuracy of 91.7%$\pm$2.8% and 90.4%%$\pm$2.8% for inspiratory and expiratory phases, respectively.

The wearable system proposed in this work is not limited to the algorithms describe above [33, 51, 52, 58]. Hence, it can also be used in other applications that require an acoustic signal detected from the trachea such as the ones reported in [59, 60]. In the work published in [59] by Azarbarzin and Moussavi; the authors proposed an automatic and unsupervised algorithm to detect and analyze snore sounds from tracheal sounds recording. The detection and analysis of snore sounds has many applications including the diagnosis of Obstructive Sleep Apnea (OSA) [61], which requires continuous monitoring of snoring sounds for the entire night. The algorithm in [59] was tested on acoustic data acquired using the Biopac (DA100C) amplifiers connected to a microphone mounted on the trachea. The signal from the microphone was amplified and digitized using the DA100C amplifiers and then fed to a computer via connection wires for analysis. The DA100C amplifier is a general-purpose one-channel amplifier with variable gain and adjustable frequency response. It is used to amplify signals acquired from different transducers that detect different vital and environmental signals. It weighs 350 grams and have dimensions of 4cm×11cm×19cm (W×L×H) [62]. It is obvious that this device is too bulky for wearable applications and thus the system proposed in this work could be utilized with the algorithm proposed for snore detection in [59].

Another application where continuous acoustic monitoring of tracheal sound is required is in swallowing detection [60]. The detection of swallowing events is useful for diagnosing and monitoring swallowing disorders such as Dysphagia. The work reported in [60] by Yagi "et al" proposed an algorithm that extracts and analyzes swallowing sounds for monitoring Dysphagia. Acoustic data of the tracheal activities is required for this algorithm, which could be obtained used the system designed in this work.

2.2.3 Acoustic monitors

The previous section has provided a review of different algorithms to extract parameters that are helpful in diagnosing respiratory and cardiac disorders. These algorithms represent one of the halves of a remote diagnosis process. The wearable device is the other half, and its functionality is as important as the algorithms that analyze the physiological data. This is because, in practice, only a small and low-power wearable device will allow efficient collection of a patient's vital signal data during their daily life activities, minimizing the impact of the disease on the patient's daily life. The power consumption of the wearable device greatly affects its convenience because this determines the number of batteries required to achieve a reasonable operating life. Batteries are the dominant factor in the final size and weight of the wearable system [63] and therefore the number of batteries used must be minimized. This is only achievable if the circuits inside the system are designed to consume the minimum amount of power while achieving the design specifications. In this section, a literature review is conducted on wearable devices that are used to detect and monitor cardiac and/or respiratory acoustic signals for diagnostic purposes.

There is a great shortage in the literature for true low-power wearable systems that acquire and monitor respiratory and cardiac sounds. Only a small number of acoustic monitors that sense cardiac and/or respiratory sounds were found in the literature [64-69]. A wearable acoustic sensor was proposed in [64] as part of Asthma monitoring system. The device contains a microphone, Bluetooth module and a chargeable battery and is attached on the neck using soft malleable plastic straps. This wearable system is not discrete to wear due to its bulky size and the plastic straps that are used to attach it on the neck.

A wireless Stethoscope device for recording heart and Lung sound was reported in [65]. The device consists of a microphone that is placed inside of a tube with a diaphragm end to simulate a Stethoscope. The output of the microphone is amplified, digitized via 8-bits ADC and then

transmitted wirelessly via RF transmitter to a PC for data processing. The device is pressed over the aortic region of the chest and is able to detect cardiac signals and respiratory sounds. However this is done manually which makes it unsuitable for continuous operation.

Another wearable digital stethoscope for heart and respiration monitoring was proposed in [66]. This device consists of a microphone that is embedded in chest pad to capture heart and respiration sounds, an amplification and filtering module, a microcontroller with an ADC to perform analogue to digital conversion and a Bluetooth transmitter module. This system is designed entirely from off-the-shelf components, resulting on significant power consumption. Moreover, the microcontroller used in this system is ATmega328, which runs at a 5V power supply. A 5V battery is bulky and relatively heavy (73 g) for a wearable device.

A wearable heart sensor as a part of multisensor harness system was proposed in [67]. The system includes two acoustic sensors placed on the chest area. The acoustic sensor consists of a microphone coupled to a mechanical acoustic diaphragm interface (to improve the desired signal's SNR) and is connected to an amplifier. This system was designed to monitor the vital signal of firefighters and the acoustic sensor was designed to be worn on top of the firefighting suite without the need of direct sensor contact. The system is worn in a harness style, i.e. strapped across the body, which makes it unsuitable for everyday use by regular people because it is not discrete at all and takes effort to wear it.

In [68], a wearable heart rate monitor connected via a wireless digital link to a home-embedded infrastructure of multimodal health surveillance system was proposed. The wearable device is coin shaped with a diameter of 22mm and weighs 11.2 grams. It is powered from a rechargeable Li-Ion 3.6V battery with current rating of 300mAh. The system consists of an AT91SAM7X256 microprocessor, Bluetooth transceiver module and a single channel custom made analogue front end. This system does not detect breathing sounds and hence cannot be used for simultaneous detection of cardiorespiratory sounds.

An acoustic monitor which is a part of low-power wearable system, for continuous monitoring of environment and health was proposed in [69]. The system contains a microphone with an integrated amplifier embedded in a plastic patch that is placed in the chest area over the heart. The acquired data is sampled at 2KHz via MCS-51 microcontroller and transmitted via a

CC2541 Texas Instruments Bluetooth module to a database. The system was powered from a 3V Lithium battery and has a power consumption of 52mW. This system is not low power (>>1mW) and moreover its characterization was not presented in the publication.

This literature review has revealed the limitations of the reported systems that prevent them from being considered as truly wearable continuous monitoring devices. These limitations are: bulky and not discreet to wear [64,66,67], cannot be used for continuous monitoring [65], or consume too much power and require frequent battery change [68,69]. This work describes the design, implementation and testing of a miniature ultra-low power wireless acoustic monitoring system for cardiac and respiratory signals. To the best of the author's knowledge, the system described in this work is the first wireless acoustic sensor that is completely designed at the transistor level and thus achieves the lowest power consumption and smallest size compared to other works reported in the literature.

2.3 System Design

The proposed system shown in Fig. 1.1 in chapter 1 is going to be described here. The wearable device and the secondary device are going to be discussed and the specifications of different circuit blocks inside these devices will be derived.

2.3.1 Wearable system design

In this section, the top-level diagram of the wearable system is described. The functionalities of different circuit blocks are discussed and their specifications are derived. The system diagram of the wearable medical device in this work is described in Fig. 2.7.

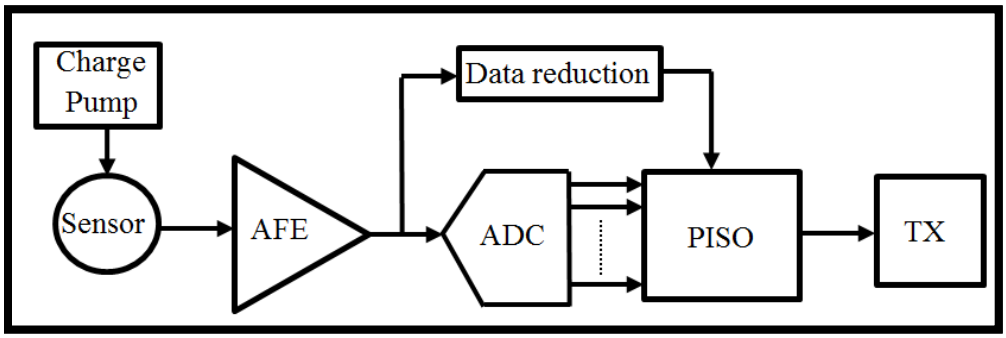


Fig. 2.7. Top-level design of the ASIC in the miniature sensor

The sensor chosen was a microphone (model Knowles SPV1840LR5H-B) that converts sound vibrations in the trachea into electrical voltages. The microphone minimum supply voltage is 1.5V, which is bigger than the battery supply voltage (1.2V-1.4V) and therefore a charge pump was required to boost up the battery supply voltage to the minimum operating voltage of the microphone. This allows the use of a single button-cell battery, which results in a small size and light weight system. Amplification is required to match the input signal to the ADC's input range, and band-pass filtering removes out of band noise. The amplifier and the filter are known together as the Analogue-Front-End (AFE). The ADC digitizes the signal and feeds into a Parallel-In-Series-Out (PISO) digital block, which consist of shift registers. The PISO digital block receives an 8-bits parallel input from the ADC and groups them in data packets with a format that is compatible with a low power Texas Instrument CC2500 transceiver module. These packets are then transmitted using an on-off keying (OOK) scheme via an on-chip transmitter. The transmitter's antenna was implemented as a single loop coil mounted on the final system's PCB. The data reduction circuit implements a data reduction algorithm by identifying speech segments in the amplified acoustic signal and then shut their transmission down to eliminate them.

2.3.1.1 Battery

There are two main types of batteries: rechargeable and disposable ones. In this work, the use of a rechargeable battery was not possible due to the lack of time to design a charging circuit and therefore a disposable battery was used. As previously mentioned, the battery size will dominate the system's total size and weight. However this is not the only criterion that determines the selection of a suitable battery for the wearable system. Other factors such as safety, capacity, energy density, maximum continuous current and internal resistance play a role in the battery selection. A brief definition of these terms is given below:

- Battery safety refers to the safety of the battery when used in different unsupervised conditions. This may be characterized by the likelihood of expelling harmful chemicals from the battery's case under various extreme conditions such as physical damage, high temperatures or a sudden big discharge current if a short circuit happens.

- Capacity is the total energy stored in the battery. This is expressed in units of Ampere-hour (Ah) or (mAh), which is defined as the maximum discharging current the battery can deliver continuously for one hour before its voltage drops to the cut-off voltage (minimum battery's voltage at which it is considered fully discharged). This term is used to calculate the battery's life, approximately as [70]:

$$Battery\ life\ (h) = \frac{Capacity(mAh)}{Average\ Current\ consumption(mA)} \times 0.7 \qquad (2.2)$$

- Energy density is the amount of capacity the battery has per unit of volume. A high energy density battery provides more energy for a smaller size, which is very important for small wearable devices.

- Maximum continuous current specifies the maximum current at which the battery can be discharged continuously. This limit is usually specified to prevent excess discharges rate that would damage the battery or reduce its capacity. As the battery is used for a low power system, this term should not impose any restrictions on the battery selection.

- Internal resistance is the output resistance of the battery. This term is important because it reduces the voltage across the terminals of the battery when a current is drawn. This becomes more noticeable during high current pulses.

In a wearable device, there are different types of batteries that can be used, such as 1/2AA, Lithium ion coin cells (CC) and Zinc air button cells (BC). The 1/2AA battery has the highest capacity. However it would have been unsuitable for the miniature wearable device in this work because it is very bulky (weighs 23g). Lithium ion batteries have better discharge characteristics than the Zinc air batteries when they are discharged at a low current (<1 mA) [63]. However, Zinc air batteries are less bulky and safer to use in wearable devices. A battery comparison and risk assessment study was carried out by the Johnson Space center (JSC) of the National Aeronautics and Space Administration (NASA) in [71]. The report categorizes batteries in four safety categories which are explained below[1] :

[1]Note: the category description is directly quoted form the report.

- Category 1: "S*mall Commonly Used Commercial-Off-The-Shelf (COTS) battery cells that can be used for flight with minimal testing/documentation required"* [71].
- Category2: "C*OTS cells available to the public requiring additional testing/documentation"* [71].
- Category 3: "*Cells available for Original Equipment Manufacturer (OEM) assembly as a pack, but not readily available to the public as loose cells"* [71]
- Category 4: "*Cells and batteries of any size that cannot be used, stored, or transported in a habitable volume"* [71].

The study categorizes Lithium ion batteries in category 3. It states that Lithium ions batteries can be made to yield their contained energy suddenly and explosively under some conditions that include:

- Any condition that makes the Lithium anode in the battery to reach its melting point of 180^{o}C. The excess heat can be due to several reasons such as the heat produced from discharging the lithium cell at a high rate, external high temperatures or manufacturing defect resulting in an internal short.
- Discharging the Lithium cell until its voltage falls below zero and forcing it to go negative.
- Some types of Lithium batteries may release some toxic gases under over-pressurization. These toxic gases include Sulfur dioxide, thionyl chloride, and/or hydrogen chloride, depending on the type of Lithium battery.

Zinc air batteries on the other hand are safer than Lithium ion ones. The hazards from using them are:

- Generation of hydrogen gas when the battery is discharged at a high rate
- Potential leak of potassium hydroxide electrolyte at possible high temperature during short circuits currents.

Nonetheless, the report in [71] categorizes them in categories 1 and 2. Moreover, Zinc air batteries provide higher energy density (1480-9780 Wh/L) compared to Lithium ion batteries (250-693 Wh/L). All these reasons lead to the conclusion that a Zinc air battery is a better choice

than Lithium ion ones for a miniature wearable device. Hearing aids batteries (which are Zinc air types) are used in this project due to their extra small size and light weight. There are a range of hearing aids BC batteries, which are summarized in Table 2.1 [72]. The P13 BC battery provides the highest energy density at a weight of 0.83g and it was the one chosen in this design so that the specifications mentioned in Table1.1 in chapter 1 can be met.

Table 2.1. Summary of different Zinc air BC batteries specifications

Type	Size (Diameter × height) (mm)	Weight (g)	Voltage (V)	Capacity (mAh)	Energy density (mAh/mm^3)
P10	5.8 ×3.6	0.3	1.4-1.2	100	1.05 mAh/mm^3
P312	7.9 ×3.6	0.58	1.4-1.2	180	1.02 mAh/mm^3
P13	7.9 ×5.4	0.83	1.4-1.2	310	1.17 mAh/mm^3
P675	11.6×5.4	1.85	1.4-1.2	650	1.14 mAh/mm^3

2.3.1.2 Microphone

To realize an ultra-small miniature low power device, the microphone must be selected to have the smallest size with the lowest possible power consumption. Micro-electromechanical systems (MEMS) are the most suitable choice as they have the smallest size and lowest power consumption of all types of microphones [73]. MEMS microphones operate in a similar way to Electret Condenser Microphones (ECM) but at a lower power consumption and smaller size. These features stem from the fact that MEMS microphones are fabricated as IC chips on Silicon using modern CMOS technology. In a MEMS microphone different layers of different materials are used to create a moveable diaphragm and a fixed back-plate over a cavity in a Silicon wafer, as shown in Fig. 2.8 [74]. The backplate is a stiff structure with small holes in it (perforated) that allow the air to move easily through it, while the diaphragm is a thin flexible structure that flexes in response to a change in air pressure. The diaphragm and backplate are both made form conductive material and thus a variable capacitor is formed by this structure with a fixed electrical charge applied between the diaphragm and backplate via a charge pump. An incoming sound wave will pass through the holes in the perforated backplate and cause a change in the air

pressure. This causes the thin membrane (the diaphragm) to flex in proportion to the amplitude of the compression and refraction of the wave. This movement changes the distance between the membrane and the back plate, which in turn varies the capacitance created by this structure. An ASIC integrated within the microphone measures the change in voltage due to the change in capacitance.

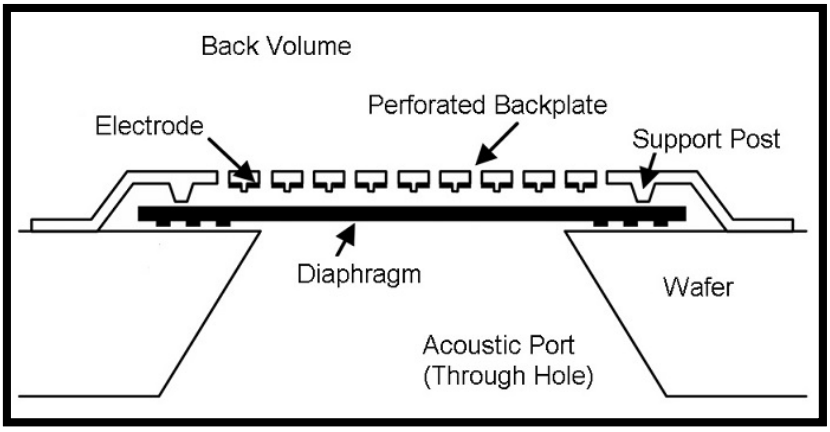


Fig. 2.8. cross sectional of MEMS microphone [74]

The microphone chosen was a MEMS microphone, model Knowles SPV1840LR5H-B [75]. This microphone offers a constant sensitivity of -38dBV/Pa over frequency range 200Hz-1KHz. It also has a very small size and ultra-low current consumption. Its specifications are shown in Table 2.2.

Table 2.2. Specifications of the microphone used in this work

Microphone Model	Knowles SPV1840LR5H-B
Size	2.75 x 1.85 x 0.9 mm
Supply Voltage	1.5V – 3.6V
Power Consumption	< 55 µA
Frequency Range (-3dB point)	100Hz ~ 10kHz
Output Impedance	290 ~ 400 ohms
Output DC Level	1.1V
Max Output Vpk-pk	1003mV
PSRR	-58 dB
SNR	62.5 dBA (Max 10.381 bits resolution)

2.3.1.3 Charge Pump

The microphone requires 1.5V supply and consumes 50µA current. The battery used to power the system is a Zinc air battery with a voltage less than 1.4V. Therefore, the charge pump specifications are to generate at least 1.5V output voltage with a 50µA current sourcing capability and to be supplied from less than 1.4V supply voltage. The other specifications of the charge pump are to consume the least amount of power and require the least amount of design area. This will be discussed in detail in Chapter 3.

2.3.1.4 AFE

The AFE is composed of an amplifier to match the input signal to the ADC's input range and a band-pass filter (BPF) to remove out of band noise and prevent aliasing. The band-pass filter is simply a high-pass filter cascaded with a low-pass filter stage. The specifications for each of the blocks that compose the AFE are discussed below.

A. Amplifier

The amplifier is used to boost the input signal level to the ADC's input range. The ADC input range is from 0-800mV and so the amplifier should be designed to amplify the full range input to the ADC's input range. The minimum detectable input signal to the system is limited by the ADC least significant bit (LSB) and by the amplifier's gain. The LSB of the ADC in this work is 3.125mV and thus the minimum detectable input voltage to the system is $3.125mV/A_v$ peak-peak; where A_v is the amplifier's gain. Any lower voltage level will not be detected by the ADC. The algorithms develop by Rodriguez-Villegas' group [33, 51, 52] have been tested using an off-the-shelf amplifier with a gain of 20dB (10 V/V) and 10-bits ADC with 1.8V reference voltage. This makes the minimum input detectable signal in their system 176µV peak-peak. The algorithms worked successfully with such amplitude. This small amplitude along with the microphone's specifications determine the minimum gain required by the system described here. This work uses an improved microphone model that offers 6dB (2V/V) more sensitivity than the microphone model used in the algorithms testing. This means that the minimum signal the new system should detect for the same algorithms to work is 352µV peak-peak. Therefore, the gain of this system should be at least A_{v_min}=3.125/0.352=8.9V/V or ~19dB. On the other hand, the gain of the amplifier should be small enough so that it keeps the amplified signal within the ADC's

input range (0-800mV). It was empirically estimated that the maximum amplitude of the raw signal from the microphone was 66mv peak-peak, and this occurs during snoring. Hence, the maximum gain of the amplifier is A_{v_max}=800/66=12.2 V/V or 21.6dB.

In summary, the amplifier's gain should be in the range of 19dB<A_v<21.6dB so that the system detects the minimum signal necessary for the algorithms to work with and at the same time does not saturate the ADC for the maximum signal. The midpoint gain of 20 dB was chosen.

B. Band-pass filter

The low-pass filter (LPF) acts as an anti-aliasing filter before sampling the data via the ADC. From Nyquist's sampling theorem, frequencies above half the sampling frequency ($f_s/2$) will get aliased and folded back in the frequency band 0 to $f_s/2$, which includes the bandwidth of the system. A signal at a frequency f, where $f > f_s/2$, will appear at an aliased frequency f_a equal to:

$$f_a = \left| f - f_s \times NINT\left(\frac{f}{f_s}\right) \right| \tag{2.3}$$

where $NINT$ is the nearest integer fucntion and f_a is the aliased frequency of the signal that was originally at frequency f, where $f > f_s/2$.

Equation (2.3) implies that the smaller frequency that will get aliased back into the signal's bandwidth (BW) is equal to f_s-BW. The attenuation of these frequencies should be greater than or equal to the dynamic range (DR) of the signal. The sampling frequency and the signal's bandwidth are 10KHz and 1KHz respectively. Therefore attenuation greater than 50dB is required at frequencies $\geq$ 9 KHz. These specifications assume that the noise at frequencies $\geq$ 9 KHz is at same magnitude as the signal of interest; however in reality it is much lower. Therefore, a small variation in the attenuation at frequencies $\geq$ 9KHz is tolerable which simplifies the design of the LPF. The aforementioned specifications can be met with a 3rd order Butterworth low-pass filter with 1.3KHz cut-off frequency.

The high-pass filter (HPF) main functionality is to attenuate the strong heart signals and prevent it from saturating the ADC, while at the same time not deteriorating the functionality of the breathing and heart detection algorithms. Therefore the order and cut-off frequency of the

HPF must be selected carefully. Testing previously carried out in Rodriguez-Villegas' lab feeding existing acoustic recordings into the HPF transfer function in MATLAB before being applied to the algorithms, showed that a 2nd order HPF with a cut-off frequency at a range 130-150Hz provided the best performance [76]. Thus, a 2nd order Butterworth HPF with 140Hz cut-off frequency was chosen in this work.

2.3.1.5 ADC

As previously mentioned, algorithms previously developed [33, 51, 52] were tested with a 10-bit ADC with 1.8V reference, which puts its LSB at 1.76mV. However, the same algorithms were tested with different lower numbers of bits to see when their performance started to deteriorate. It was found that the algorithms needed a minimum number of 7-bits to work effectively [76] . Therefore, an 8-bits ADC design with 800mV reference was selected.

There is a trade-off between the sampling frequency and the complexity (topology and order) of the LPF. A high sampling frequency will require simpler LPF design and will make the system performance more immune to variations in the latter's performance. This is because with higher sampling frequency the image signal will be pushed at higher frequencies, so it does not matter what the variations in the LPF's cut-off frequency are as long as the gain is uniform between 400Hz-900Hz, and the gain at the image frequencies ($f>f_s-BW$) is less than (A_{vpass}-50)dB. On the other hand, higher sampling frequency translates to higher data rate to transmit, which increases the power consumption of the ADC and the transmitter. The used ADC consumed an average current of 8μA at 10KHz sampling frequency at 1.3V supply. The 10KHz sampling frequency resulted in an ADC's power consumption that is very reasonable for the system described here, and at the same time it is sufficiently high to require a moderately complex anti-aliasing filter design. Hence the sampling frequency was set to 10KHz.

2.3.1.6 PISO digital block And Transmitter

There were no strict requirements on the PISO digital block, other than power consumption and its output format. The PISO digital block function was to take the 8-bits parallel input of the ADC and then format them in packets that were compatible with the Texas Instrument CC2500 transceiver module. This block is composed of shift registers, which meant its design could be

very low power when implemented at the transistor level. The packet format of the CC2500 transceiver module can be made without any extra power budget.

The transmitter is the most power consuming circuit in the system, and it will dominate it. Hence, it was very crucial to select a transmitter design the offers a decent transmission range with acceptable power consumption. Although the transmitter was designed on chip, its antenna was a single coil loop inductor that was soldered externally on the PCB. The reason for this was that coil loop inductors have a higher Q-factor than on-chip inductors and its addition does not increase the system's size or weight, as the latter parameters are dominated by the battery's size and weight.

2.3.2 Secondary device

The secondary device consists of a CC2500 transceiver module that receives data from the wearable device and then transmits/transfers this data to a database. However, the CC2500 is a half-duplex device which means that it cannot be used simultaneously as a receiver and transmitter and therefore it must be configured between the two states in a careful way to ensure not losing data packets. To understand how the CC2500 module must be configured, the shape of the data packets at the transmitter's input in the wearable device has to be first considered:

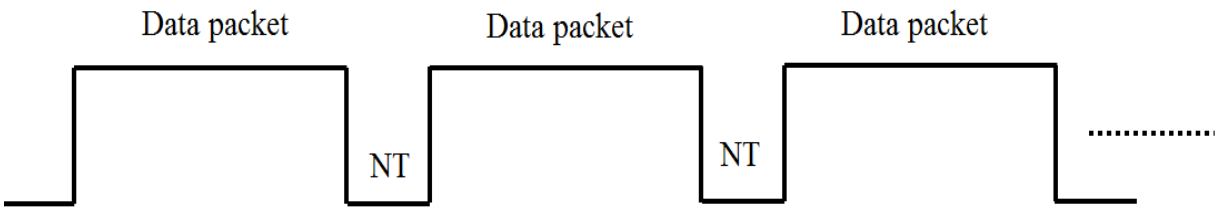


Fig. 2.9. Shape of data packets at the transmitter's input in the wearable device

The transmitted data consists of serial packets with a No-Transmission (NT) gap between them. Note that the data packets are not a straight line; they are composed of binary data that resembles a straight line from a zoomed out view. The NT gap is the time it takes to load the data in the shift registers in the PISO digital block.

The CC2500 module in the secondary device can be programmed to automatically alternate between receiving and transmitting modes[2]. When the wearable device transmits data packets, the CC2500 module in the secondary device is configured as a receiver and as soon as a packet is successfully received the module switches to transmission mode and so on. This implies that during the NT periods, the CC2500 module can be used to transmit/transfer the recently received data packet from the wearable device to the database. Therefore, the time length of the NT period must be of a similar length to the transmitted data packets so that the CC2500 module has sufficient time to transmit a packet and then switch back to receiving mode, ready to receive a new packet from the wearable device. Unfortunately, this is not the case in this work because the idea of the system was adjusted after the chip was fabricated. However this is trivial to change from the PISO digital block and can be adjusted in a future version of the system.

The data received by the CC2500 module must be stored until it switches to transmission mode and is ready to transmit. Once this is accomplished, the data must be output to the CC2500 input pin for transmission at a rate similar to the received data rate. All these functionalities can be accomplished by programming the CC2500 interface microcontroller (MSP430). This results in a simple and compact design that is composed of only a CC2500 module, MSP430 microcontroller, crystal oscillator and battery.

2.4 Conclusion

This Chapter has reviewed different respiratory and cardiac chronic diseases, including their symptoms, diagnosis methods and economic burden. The idea of a remote diagnostic process for these diseases was discussed and the two main parts of it were reviewed. These two main parts are a wearable device that extracts vital data and an algorithm to analyze it. The literature review conducted has shown that the literature is rich in algorithms that analyze acoustic data while there is a shortage of true low-power miniature wearable devices. Therefore, a low power wearable monitoring system was proposed. Further research also revealed that acoustic detection of vital signals via a MEMS microphone is the best method to allow the realization of a small

[2] Note: the switching time between receiving and transmitting modes takes 250 clock cycles which is approximately 9.6μs if the CC2500 is clocked at 26MHz

low-power device. The top-level system of the proposed device was introduced and the specifications of the circuits within it were derived. These specifications were focused on minimizing the power consumption of the system while simultaneously providing a signal that is compatible with the algorithms that analyze the data.

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Chapter 3: Charge Pump

The research presented in this chapter is an edited version of previously published research in:

- *M.H Eid and E. Rodriguez Villegas, " Analysis and design of cross-coupled charge pumps for low power on chip applications" Microelectronics Journal, vol. 66, pp. 9-17, 2017. © Elsevier*
- *M.H. Eid and E. Rodriguez Villegas, "Analysis of reversion loss in charge pumps and its impact on efficiency for low power design," 2017 15th IEEE International New Circuits and Systems Conference (NEWCAS), Strasbourg, France, June 2017. © IEEE*

3.1 Introduction

The wearable device consists of an integrated CMOS chip to process the signal, a printed circuit board (PCB) to mount the CMOS chip on, a sensor to extract the vital signal of interest and a battery. Most often, the battery is the bottleneck when it comes down to how small and light the system can be [1] and using as few batteries as possible is key to small size and light weight systems. Small button cell batteries such as Zinc Air ones are typically used in wearable systems due to their small size, safety and convenient round shape. These batteries usually have an operating voltage below 1.4V, but some of the components in the system require higher voltages to operate. As a result, two batteries are needed which doubles the size and the weight of the wearable device. Alternatively, a charge pump (CP) could be fabricated on chip and utilized to boost up the battery supply voltage to the required operating voltage. Charge pumps (CPs) are switched capacitor (SC) circuits that can be used to boost up the supply voltage. Being inductor-less circuits, they are very effective blocks because they are compatible with a standard CMOS processes. As previously explained in Chapter 2 Section 2.3, a CP is required to boost up the battery supply and power the microphone. The latter requires a minimum supply voltage of 1.5V and consumes 50μA of current.

In this chapter, different topologies of CPs are reviewed to select the most suitable design in terms of power efficiency, design complexity and design area. Once a topology is chosen, the CP circuit operation and different power loss mechanisms within it are analyzed. Based on this analysis, design equations are derived. The derivation of design equations was carried out from

first principles in order to give an understanding of all the non-idealities in the CP as well as the factors that limit the CP's efficiency. The design equations subsequently lead to a complete design methodology that optimizes the efficiency of the single-stage CP. This design methodology includes all the design aspects of the CP, including the power losses due to the output PMOS switches and clock drivers. An expression for the optimum switch's dimensions, to minimize its losses, is also derived. In addition, a design procedure to reduce the power losses in the clock drivers is presented which leads to design recommendations for the clock generator to optimize its power consumption as well. Finally, based on this design methodology, a CP was designed, simulated and experimentally verified.

The rest of the chapter is organized as follows: Section 3.2 provides an overview of different CPs topologies and a suitable topology for the application in this work will be selected. Section 3.3 analyzes the CP circuit operation and the different power losses mechanisms within it. Based on the analysis in this section, an expression for the efficiency is derived and a design methodology is proposed. In section 3.4, a detailed mathematical analysis of reversion losses is provided. In section 3.5, a CP was designed based on the proposed design methodology. Simulations are performed on the circuit to verify the theory and lab measurement of the fabricated CP are presented. Section 3.6 is the conclusion of the chapter.

3.2 Charge pumps Overview

Historically, CPs have been implemented using the Cockcroft-Walton multiplier and were used to accelerate subatomic particles [2]. However, Cockcroft-Walton charge multiplier suffers greatly from parasitic capacitance and thus is unsuitable for on-chip implementation. To overcome this limitation, Dickson proposed a CP [3] where the pumping capacitors are connected in parallel through diodes. This makes the topology less sensitive to parasitic capacitances and thus was the first integrated solution of SC CPs. The diode implementation of Dickson's CP is not a practical implementation in modern CMOS processes, especially for low voltage designs. Therefore, an NMOS implementation of Dickson's CP was proposed in [4], where the diodes are replaced by diode connected NMOS transistors, its diagram shown in Fig. 3.1.

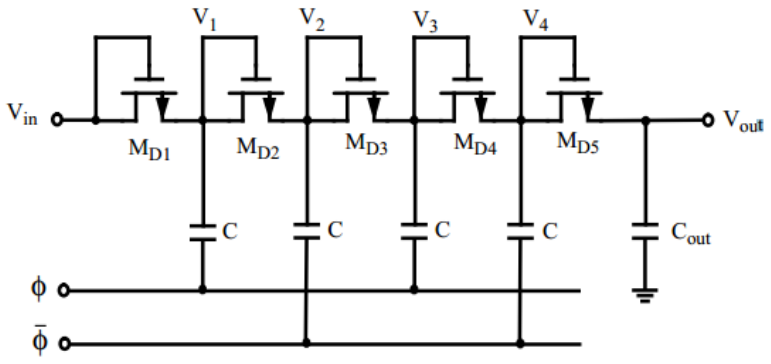


Fig. 3.1. NMOS implementation of Dickson's charge pump

Dickson's CP was a breakthrough in the implementation of on-chip integrated CPs and initiated many innovations in this field. Therefore, the operation of the NMOS Dickson's CP is going to be reviewed, in order to understand its limitations and how it triggered many innovations.

The waveforms ϕ and $\bar{\phi}$ are two complementary clocks with amplitude V_{in} . During phase 1, ϕ is low and $\bar{\phi}$ is high and the voltage at node V_1 is $V_{in} - V_{th}$, where V_{th} is the threshold voltage of the NMOS device. During phase 2, ϕ goes high and $\bar{\phi}$ goes low and, by the law of conservation of charge, node V_1 is boosted to $2V_{in} - V_{th}$. This turns M_{D2} ON and the voltage at node V_2 becomes $2V_{in} - 2V_{th}$. When the circuit enters phase 1 again, the voltage at node V_2 gets boosted to $3V_{in} - 2V_{th}$. By extending this analysis, it can be seen the voltage at N^{th} node (V_N) equals $V_{in}(N+1) - NV_{th}$, and the final output voltage is given as $V_{in}(N+1) - NV_{th} - V_{th}$. If load current is taken into account and ignoring parasitics, the output voltage expression becomes$(N+1)(V_{in} - V_{th}) - \frac{N \times I_{out}}{fC}$, where f is the pumping frequency and C is the pumping capacitor. The voltage gain between two succeeding stages is $G_V = V_{in} - \frac{I_{out}}{fC} - V_{th} = \Delta V - V_{th}$ where $\Delta V = V_{in} - \frac{I_{out}}{fC}$. The final output voltage of the Dickson's CP involves $(N+1)$ NMOS threshold voltage drops, which, for illustration sake, would be 4 times 0.4V threshold voltage in the AMS 0.18µm process. Additionally, in order to achieve a pumping gain in the Dickson's CP, the condition $\Delta V > V_{th}$ must be satisfied. However, for low voltage systems, the value of V_{in} is small, making ΔV too low, and thus multiple pumping stages would be required. This increases the total design area and power consumption of the system. Furthermore in multiple stages Dickson's CP, the body terminal is usually connected at ground level and thus the body effect cannot be ignored [4]. This increases the threshold voltage of NMOS devices,

especially at high voltage nodes near the output, which can substantially degrade the pumping gain with increasing number of stages. This is a limitation of the Dickson's CP for low voltage designs. To overcome this problem, floating devices have been proposed in [5], where PMOS devices with floating body were used instead of NMOS devices with grounded body. This modification completely eliminates the body effect problem, however this approach is not desirable as it causes substrate currents. Moreover, this method does not solve the dependency of the pumping gain on the NMOS threshold voltage. A modification of the Dickson's CP, known as NCP-1, was proposed in [6]. It utilizes static charge transfer switches (CTS) instead of a simple diode connected NMOS transistors. This eliminates the dependency of the pumping gain on the threshold voltage, which translates to an increase in the CP's gain. However, a major drawback of this topology is charge leakage in the reverse direction leading to decrease in the pumping gain. A modified version of the NCP-1 CP is known as the NCP-2 CP and was proposed in [7]. The NCP-2 CP eliminates the reverse charge leakage problem by utilizing extra switches to control the static CTS. It provides a significant improvement over the standard Dickson's CP (50% improvement in pumping gain at 2V input voltage and 10μA load current), however it increases the design complexity.

A different class of non-linear CPs, such as Exponential and Fibonacci CPs, are proposed in [8] and [9] respectively. As their name suggest, these CPs have an exponential voltage gain with the number of stages (2^N) or a gain that follows Fibonacci series with the number of stages (i.e. 2,3,5,8..). These topologies are attractive for applications where a high output voltage is required to be generated via multiple pumping stages because they save up on the total design area. Their analysis is more difficult due to their non-linear behavior, which makes their optimization more complex. Therefore, these topologies are not the most attractive choice for low voltage applications that require a single CP stage.

Another linear CP design that is based on the cross-coupled NMOS voltage doubler was proposed in [10]. This type of CP provides higher pumping efficiency compared to the Dickson or NCP-2 CP, for a given set of conditions (supply voltage, load current and number of capacitors) [11, 12] and it is the most popular for on chip applications [13]. Hence it is the one used in this work.

3.3 Charge pumps Optimization

An extensive amount of work has been done on modeling and optimizing CP circuits [14-19]. The work reported in [14] provides a theoretical model of the transient behavior of two and three stages Dickson's CP. An area efficient optimized design methodology, based on this model, was also proposed. A further extension of this model to N-stages Dickson's CP was reported in [15]. Another design methodology to minimize the power consumption of Dickson's CP was introduced in [16]. This was based on optimizing the number of stages required to achieve a specific output voltage from a given input. An extension of the work done in [16] to other CP topologies was proposed in [17], where an analytical general model of the CP was introduced. This general model can be used to calculate and optimize the efficiency for different CP topologies by using some parameters that describe that specific topology. However to be able to use this model, it is first required to calculate a few parameters that are specific to the topology of the CP used. In [18] , a design methodology to optimize the efficiency versus power density of a SC converter was proposed. This has introduced gate drivers and level shifters design techniques to enable multiple topologies reconfiguration. It thus can be used to efficiently generate a range of output voltages. To further extend the optimization of CPs to a large number of stages (>5), a new CP efficiency optimization method, based on matrix modeling of the pumping capacitors, was proposed in [19]. This was implemented as a CAD tool, making it suitable to analyze and optimize the efficiency of non-linear CPs topologies, such as Fibonacci and Exponential CPs, for a large number of stages without the need of complicated manual analysis. All the previously reported work is used either to optimize multiple stages CPs, or mainly for topologies different than the cross-coupled one. Cross-coupled CPs are, however, the most popular for on chip applications and is the one used in this work. Additionally, the design of clock drivers and the output MOS switches are not discussed. Moreover, miniature transducers that are used in wearable systems nowadays, such as microphones [20] and accelerometers [21], have an operating voltage range of 1.5V-2.5V with a current consumption range of tens to hundreds of micro-amps. Such components need a single stage CP to generate their supply voltage from 1V-1.4V button cell batteries. It is therefore useful to have a complete and specific design methodology to optimize the efficiency of a single stage cross-coupled CP.

In this section, the operation of the cross-coupled CP and different losses mechanisms within it are analyzed. Based on this analysis, design equations are developed. The derivation of design

equations was carried out from first principles, in order to give an understanding of all the non-idealities in the CP as well as the factors that limit its efficiency. The design equations subsequently lead to a complete design methodology that optimizes the efficiency of the single-stage CP. This design methodology includes all the design aspects of the CP, including the power losses due to the output PMOS switches and clock drivers. An expression for the optimum switch's dimensions, to minimize its losses, is also derived. In addition, a design procedure to reduce the power losses in the clock drivers is presented which leads to design recommendations for the clock generator to optimize its power consumption as well.

3.3.1 Circuit architecture and analysis

The circuit diagram of the cross-coupled CP [22] and its timing diagrams are shown in Fig. 3.2 and Fig. 3.3, respectively.

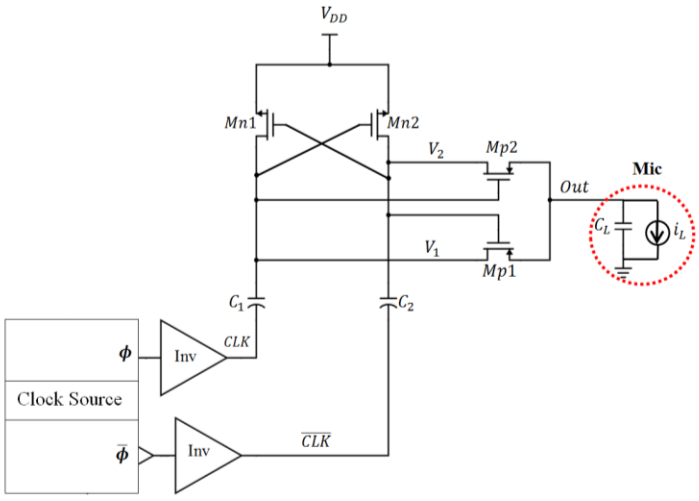


Fig. 3.2. Schematic of the cross-coupled CP with its pumping clock source

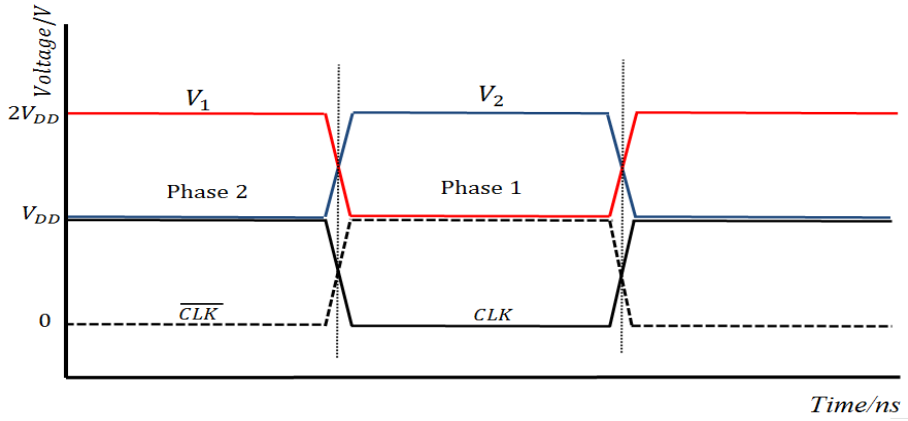


Fig. 3.3. Timing diagram of the cross-coupled CP showing the complementary clocks and the voltage swing at nodes V_1 and V_2

The circuit is perfectly symmetrical and all components have the same design parameters. CLK and $\overline{CLK}$ are two complementary clocks with an amplitude of V_{DD} and the inverters serve as clock buffers. Define phase1 as when CLK is low and $\overline{CLK}$ is high, and phase 2 is the opposite. The circuit principle of operation in steady state is as follows: during phase 2 nodes V_1 and V_2 are at $2V_{DD}$ and V_{DD} respectively. *Mp1* is ON and *Mp2* is OFF and the output is at $2V_{DD}$. When the circuit enters phase1, CLK goes low and $\overline{CLK}$ goes high. Node V_1 is discharged to V_{DD} turning *Mn2* OFF and node V_2 is boosted to $2V_{DD}$ turning *Mn1* ON. This sequence of event turns *Mp2* ON and *Mp1* OFF, thus the output is at $2V_{DD}$. In phase 2 the roles of *Mn1* and *Mn2* are swapped, as well as the role of *Mp1* and *Mp2*, and thus the output sees a constant voltage of $2V_{DD}$.

Assume in a first instance that there is no load and no parasitics. In phase 2 *Mn2* is turned ON and node V_2 is at V_{DD}. The charge stored in C_2 during phase 2 is:

$$Q_{ph2} = C_2 \times V_{DD} \tag{3.1}$$

When the circuit enters phase 1; CLK goes low turning *Mn2* OFF. As $\overline{CLK}$ goes to V_{DD}, the charge stored in C_2 must be conserved as there is nowhere for the current/charge to flow out (because *Mn2* are *Mp2* are still OFF and there are no parasitics connected to node V_2). Thus the voltage at the top plate of C_2 is boosted up to $2V_{DD}$.

If parasitic capacitances at node V_2 are taken into account (coming from the top plate of C_2, gate of *Mp1*, *Mn1* and drains of *Mp2*, *Mn2*) then some charge must flow to these parasitics in order to raise their voltage above V_{DD}. As *Mn2* and *Mp2* are OFF, this charge comes from C_2, as shown in Fig.3.4, which results in a charge loss and voltage reduction.

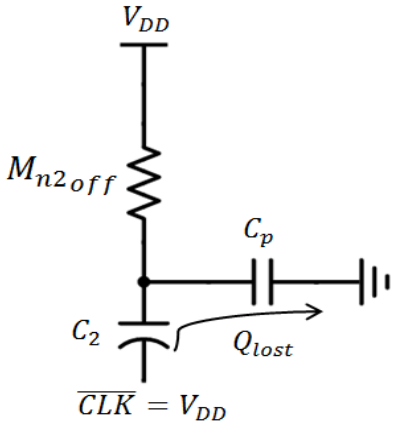


Fig. 3.4. Equivalent circuit explaining the lost charge due to parasitics in phase1

The reduction in voltage (V_{lost}) and the current that flows to the parasitics can be represented as follows:

$$V_{lost} = \frac{Q_{lost}}{C_2} \qquad (3.2) \qquad i_p = C_p \frac{dV_2}{dt} \qquad (3.3)$$

Where i_p is the current that flows from C_2 to C_p in order to charge it up and dV_2/dt is the rate of change of voltage at node V_2. Assuming that $\overline{CLK}$ transitions from low-to-high in linear fashion, the voltage at node V_2 will transition in a linear fashion as well and thus:

$$i_p = C_p \times \frac{V_0 - V_{DD}}{T_r} \qquad (3.4)$$

Where T_r is the rising time of $\overline{CLK}$ from low to high and V_0 is the final voltage reached at node V_2 after clock transition.

A linear clock transition implies that the current that flows to the parasitic capacitance is constant during the transient of the clocks as shown in Fig. 3.5 below:

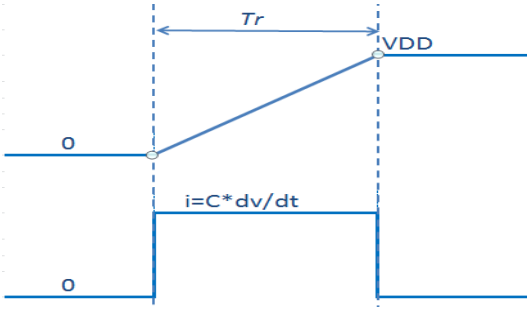


Fig. 3.5 Clock Transient and parasitics charging current

The charge lost from C_2 is:

$$Q_{lost} = \int_0^{Tr} i_p dt = i_p \times T_r \qquad (3.5)$$

Substituting (3.4) and (3.5) in (3.2), the voltage lost due to parasitic capacitance is written as:

$$V_{lost} = \frac{C_p}{C_2} \times (V_0 - V_{DD}) \qquad (3.6)$$

Defining $V_{lost} = 2V_{DD} - V_0$, V_0 can be written as:

$$V_0 = V_{DD} \times \left[2 - \frac{C_{p_t}}{C_2 + C_{p_t}}\right] \tag{3.7}$$

Where C_{pt}=$\sum_{i=1}^{n} C_{pi}$ is the summation of all parasitic capacitances connected at node V_2.

Defining the top plate parasitic of the pumping capacitor (C_2) as a fraction (α_T) of it and assuming that it dominates all other parasitics connected to node V_2; the final voltage can be written as:

$$V_0 = V_{DD} \times \left[\frac{2 + \alpha_T}{1 + \alpha_T}\right] = V_{DD} \times \gamma \tag{3.8}$$

$$\gamma = \frac{2 + \alpha_T}{1 + \alpha_T} \tag{3.9}$$

When a load current is connected at the output, the circuit can be modeled during phase 1 as shown in Fig.3.6. $M_{n2_{off}}$ represents the resistance of M_{n2} when its off, which is very large.

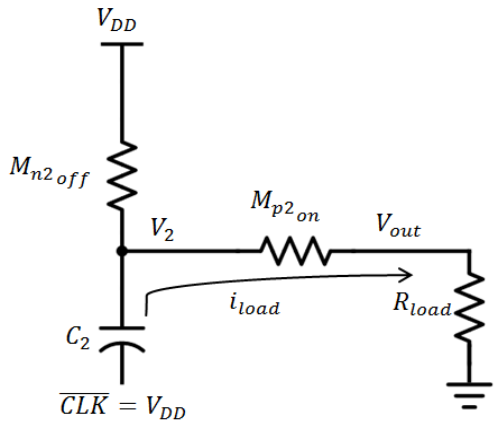


Fig. 3.6. Half circuit modeled during phase 1 when a load is connected

Charge has to flow out of C_2 to supply the load's current which will result in a decrease in the output voltage. The discharge of C_2 can be modelled as:

$$V_2(t) = V_0 e^{\frac{-t}{R_{load} \times C_2}} \tag{3.10}$$

Where V_0 is the maximum voltage reached at node V_2 as $\overline{CLK}$ goes high, defined by (3.8). Assuming negligible voltage drops across *Mp2*, R_{load} can be written as:

$$R_{load} = \frac{V_2(t)}{i_L} = \frac{V_{out}(t)}{i_L} \tag{3.11}$$

Substituting (3.11) and (3.8) back in (3.10):

$$V_{out}(t) = \gamma V_{DD} e^{\frac{-i_L \times t}{V_{out}(t) \times C_2}} = \gamma V_{DD} e^{\frac{-\phi}{V_{out}(t)}} \tag{3.12}$$

Where $\phi = i_L \times t/C_2$. Using Taylor series to expand $e^{-\phi/V_{out}(t)}$ and assuming that $\phi/V_{out}(t)_{min}$<<1, (3.12) can be arranged as:

$$V_{out}(t)^2 - \gamma V_{DD} V_{out}(t) + \phi \gamma V_{DD} = 0 \tag{3.13}$$

This has the following solution:

$$V_{out}(t) = \frac{\gamma V_{DD} + \sqrt{(\gamma V_{DD})^2 - \frac{4 i_L \times t}{C_2} \gamma V_{DD}}}{2} \tag{3.14}$$

This equation models the output voltage with time during half period of the clock cycle (when C_2or C_1 are connected to the output).The final voltage the output settles at, $V_{out-final}$, is equal to

$$V_{out-final} = \frac{\gamma V_{DD} + \gamma V_{DD} \sqrt{1 - \frac{2 i_L}{\gamma V_{DD} \times f C_2}}}{2} \tag{3.15}$$

Where f is the clock frequency. By expanding again the term $\sqrt{1 - \frac{2 i_L}{\gamma V_{DD} \times f C_2}}$ using Taylor series and rearranging, the final expression of $V_{out-final}$ can be written as:

$$V_{out-final} \approx \gamma V_{DD} - \frac{i_L}{2 f C_2} \tag{3.16}$$

These equations are accurate under the condition:

$$\frac{i_L}{2 f C_2} < V_{DD} \tag{3.17}$$

This is true for any practical CP.

The maximum current capacity of the CP is defined as the maximum output current it can provide when the output voltage drops to the minimum output voltage of the CP $(V_{DD} + |V_{thp}|)$, and is expressed by re-arranging (3.16) as:

$$i_{max} = 2fC_2\left[V_{DD}(\gamma - 1) - \left|V_{thp}\right|\right] \tag{3.18}$$

Most often a load capacitor (C_L) is added at the output to reduce the output ripple and smooth the output voltage. The easiest method to find an expression for the final voltage in this case is by considering the charge distribution that occurs between the load and the pumping capacitor [14, 15, 23]. The total charge provided to the load in any phase can be expressed as:

$$Q_{load} = \frac{i_L T}{2} \tag{3.19}$$

This leads to an output voltage ripple defined as:

$$\Delta V_o = V_1 - V_{o2} = \frac{i_L T}{2(C_1 + C_L)} \tag{3.20}$$

Where V_{o1} and V_{o2} are the voltages at the start and end of phase1/phas2 respectively as shown in Fig 3.7.

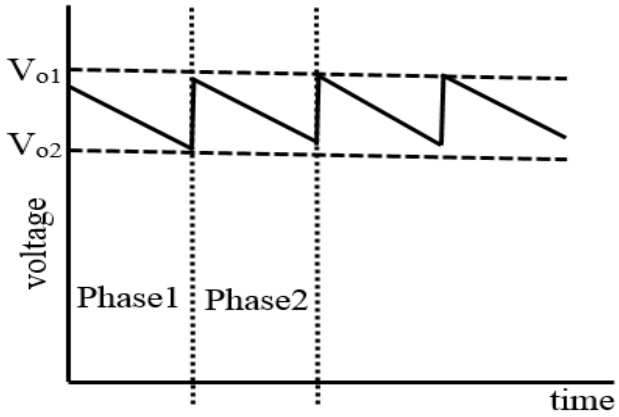


Fig 3.7. Voltage ripple at the output of the CP

When the circuit enters phase1, capacitor C_2 is connected to the output and charge redistribution occurs between C_2 and C_L. Ignoring parasitic capacitances, this is written as:

$$Q_{C_{2_{ph1}}} + Q_{C_{L_{ph1}}} = Q_{C_{2_{ph2}}} + Q_{C_{L_{ph2}}} \tag{3.21}$$

Where $Q_{C_{2_{ph2}}}$ is the charge in C_2 at the end of phase 2 and $Q_{C_{2_{ph1}}}$ is the charge stored in capacitor C_2 at the start of phase 1. Similar logic applies to $Q_{C_{L_{ph2}}}$ and $Q_{C_{L_{ph1}}}$.

Equation (3.21) can be expressed as:

$$C_2(V_{o1} - V_{DD}) + C_L V_{o1} = C_2 V_{DD} + C_L V_{o2} \tag{3.22}$$

Rearranging

$$V_{o2} - V_{o1} = \frac{C_2(V_{o1} - 2V_{DD})}{C_L} \tag{3.23}$$

The circuit is perfectly symmetrical with $C_1 = C_2 = C$. Hence, solving the simultaneous equations (3.20) and (3.23) results in:

$$V_{o1} = 2V_{DD} - \frac{C_L i_L}{2fC(C + C_L)} \tag{3.24}$$

$$V_{o2} = 2V_{DD} - \frac{i_L}{2fC} \tag{3.25}$$

Comparing expressions (3.24) and (3.25) for $C_L = 0$ with expressions (3.8) and (3.16) respectively, they can be written to include the effect of parasitic capacitances:

$$V_{o1} = \gamma V_{DD} - \frac{C_L i_L}{2fC(C + C_L)} \tag{3.26}$$

$$V_{o2} = \gamma V_{DD} - \frac{i_L}{2fC} \tag{3.27}$$

It can be seen from (3.27) and (3.16) that the final output voltage would be the same whether a load capacitor is connected to the output or not because the final output voltage depends on the amount of charged pumped out of the pumping capacitor.

3.3.2 Power Loss Analysis

In order to minimize the power consumption of the CP, it is essential to maximize its efficiency. In this section, the losses due to different mechanisms in the charge pump are analyzed leading to a derivation of the efficiency expression that can help to optimize the CP design. There are four main sources of power loss in a SC CP that can be summarized as follows:

1. Losses due to the output resistance of the CP.
2. Switching/dynamic losses, due to the parasitic capacitances.
3. Conduction losses due to the finite PMOS switch resistances.

4. Losses due to short circuit currents in the clock drivers.

3.3.2.1 Output resistance of the charge pump

The equivalent circuit of CP can be modelled as an ideal voltage source with a series resistance [24] as shown in Fig. 3.8.

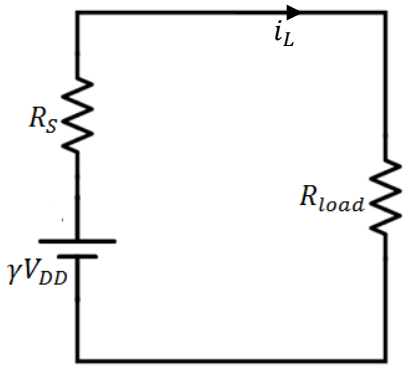


Fig. 3.8. Equivalent circuit of the CP

The CP resistance R_s is the equivalent resistance of the pumping capacitor C when it is used to transfer charge to the output load, and is given by:

$$R_s = \frac{1}{2fC} \tag{3.28}$$

The factor 2 in the denominator arises because C is only transferring charge to the output load for half the period of time, i.e. it is switched at a frequency of $2f$.

The output voltage is the source voltage minus the voltage drop across the CP output resistance R_s, as expressed in (3.16), and the power loss due to R_s is:

$$P_{loss-R_s} = {i_L}^2 \times R_s = \frac{{i_L}^2}{2fC} \tag{3.29}$$

The ON resistance of the PMOS switch (R_{ON}) will modulate the output resistance of the CP by a factor λ given as [25]:

$$R_S = \frac{1}{2fC} \times \lambda \tag{3.30}$$

$$\lambda = coth\left(\frac{T_{ON}}{R_{ON} \times C}\right) \tag{3.31}$$

Where T_{ON} is the duration of time for which the output PMOS switch is turned ON and approximately is equal to $½f$ [26].

This modulation of the output resistance will increase the effective output resistance of the CP which in turn will degrade the efficiency. It has a more pronounced effect on the charge pump output resistance at higher frequencies. The modulation index (ρ) is defined as:

$$\rho = \frac{T_{ON}}{R_{ON} \times C} \approx \frac{1}{2R_{ON} \times fC} \tag{3.32}$$

R_{ON} is given by (3.39).

In order to avoid any modulation of the CP's output resistance, it is important to choose the design parameters in such a way that the modulation index is larger than 2, i.e.

$$\rho > 2 \tag{3.33}$$

This condition makes sure that the factor λ , equation (3.31), always equals one and hence avoid modulation of the CP's output resistance. More on this will be discussed in later sections.

3.3.2.2 Switching losses

Parasitic capacitances exist on both the top plate and the bottom plate of the pumping capacitor. The parasitic capacitances have to charge and discharge every cycle for the internal nodes to swing between V_{DD} and γV_{DD}. This charging and discharging of parasitics is a form of energy loss. Defining the bottom and top plate parasitic of the integrated capacitor *C* as a fraction α_B, α_T of it, respectively, the total power lost due to the integrated capacitor parasitics can be written as:

$$P_{loss-C} = 2fC(\alpha_B + \alpha_T){V_{DD}}^2 \tag{3.34}$$

Moreover, the PMOS output pass transistors introduce parasitic capacitances due to their gate and gate-drain/gate-source capacitances that charges and discharges in every cycle. The total capacitance involved in the process is not very simple to model by hand. Hence a simplified MOSFET parasitic model as in [27] will be used.

Node V_1 swings between V_{DD} and $2V_{DD}$, and similarly for node V_2 but in a complementary fashion, thus C_{gd-Mp2} can be transferred to a capacitor between node V_2 and ground with a value of $2C_{gd-Mp2}$ (Miller effect [28]). This means that the total parasitic capacitance due to the

PMOS switches, lumped at node V_2 to ground, can be expressed as (Switches are in triode region):

$$\begin{aligned} C_{2p} &= C_{g-Mp1} + 2C_{gd-Mp2} \\ &= 2WLC_{ox} + 2WC_{OV} \end{aligned} \tag{3.35}$$

Where, C_{OX} and C_{OV} are the oxide capacitance per unit area and the overlap capacitance per unit width respectively.

Similar expression of the parasitic capacitance lumped at node V_1 to ground (C_{1p}) can be derived because of the circuit symmetry. Furthermore, a gate-source capacitance is connected between the gate of *Mp1* and the output (fixed voltage) and experience a voltage swing of V_{DD}. Hence the total power loss due to the gate-source capacitances of $Mp1$ and $Mp2$ can be approximated as:

$$\begin{aligned} P_{Loss-Cgs} &= fV_{DD}{}^2\left(C_{gs-Mp1} + C_{gs-Mp2}\right) \\ &= fV_{DD}{}^2(WLC_{ox} + 2WC_{OV}) \end{aligned} \tag{3.36}$$

By noting that the voltage swing across all these parasitic capacitances is V_{DD}, the total switching power loss, due to the output PMOS switches, can be expressed as:

$$\begin{aligned} P_{Loss-Switching} &= fV_{DD}{}^2\left(C_{1p} + C_{2p}\right) + P_{Loss-Cgs} \\ &= WfV_{DD}{}^2(5LC_{ox} + 6C_{OV}) \end{aligned} \tag{3.37}$$

The parasitic capacitance of the integrated capacitor (especially the bottom plate) is usually bigger than the PMOS parasitics (assuming medium devices are used), and hence the power loss due to the PMOS parasitics are usually ignored in efficiency calculation. However, if huge devices are used and they are of similar magnitude then they should be included in the efficiency calculations for accuracy. However, for most practical CP circuits this is not the case.

3.3.2.3 Conduction losses due to the PMOS output switches

Node V_2 is connected to the output during phase 1 via the output switch *Mp2*. This switch's resistance appears in series with the CP's output resistance. *Mp2* will be ON during conduction with a small drain-source voltage drop (V_{DS}), this means that *Mp2* will be in the triode region because:

$$Vout > V_{DD} + \left|V_{thp}\right| \tag{3.38}$$

(Note that this is the minimum output voltage the charge pump would be able to give).

Hence *Mp2* resistance is given by:

$$R_{ON} = R_{p2} = \frac{1}{\mu_p C_{OX} \left(\frac{W}{L}\right)_p \left[V_{out} - V_{DD} - |V_{thp}|\right]} \tag{3.39}$$

The conduction power loss is:

$$P_{c-R_{p2}} = \frac{{i_L}^2}{\mu_p C_{OX} \left(\frac{W}{L}\right)_p \left[V_{out} - V_{DD} - |V_{thp}|\right]} \tag{3.40}$$

The conduction losses are inversely proportional to the width of the PMOS transistor while the switching losses are directly proportional. Therefore, increasing the area of the PMOS device may not necessarily decrease the total losses due to the PMOS switch. Hence, the sizing of the PMOS device should be selected such that the efficiency is maximized for a set of conditions. The total power loss reaches the minimum when the conduction loss becomes equal to the switching losses [29]. This is shown in Fig. 3.9.

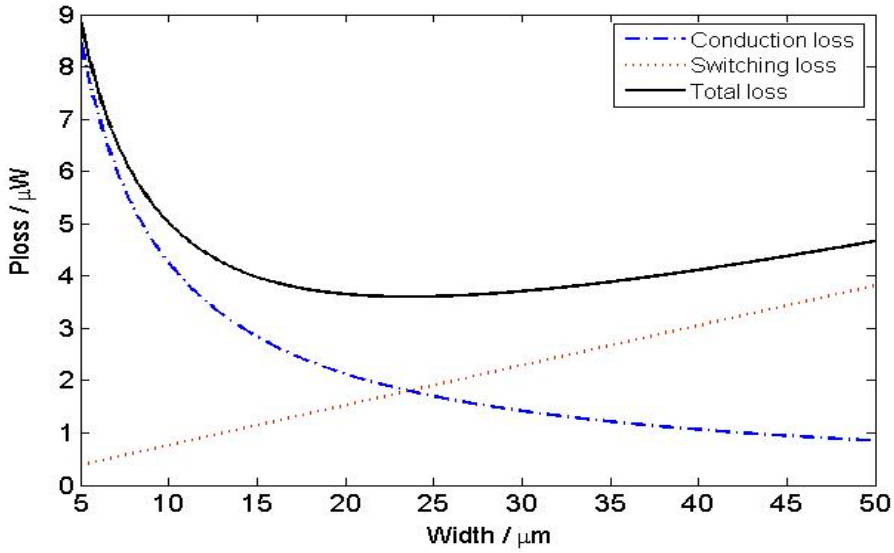


Fig. 3.9. Variations of conduction, switching and total power loss of a MOS device with its width

Equating the conduction losses (3.40) and the switching losses (3.37) and solving for *W*:

$$W = \sqrt{\frac{{i_L}^2 L}{f {V_{DD}}^2 \mu_p C_{OX} (5LC_{ox} + 6C_{OV}) \left[V_{out} - V_{DD} - |V_{thp}|\right]}} \tag{3.41}$$

This value of W is where the total losses due to the PMOS are minimized as shown in Fig. 3.9 and hence it is, approximately, where the efficiency is maximized.

As mentioned earlier, condition (3.33) must be satisfied in order to avoid the modulation of the charge pump output resistance. Hence it is important to select the values of f and C such that condition (3.33) is satisfied. If for given design constraints (such as specific supply voltage, load current, output voltage) and specific values of f ,C and R_{ON}, condition (3.33) is not satisfied, then lowering the frequency and increasing the capacitor value by the same factor should solve this issue without changing any of the design specifications (output voltage or the charge pump current sourcing ability). For a constant output voltage, decreasing the frequency by a factor $\boldsymbol{\xi}$, will increase T_{ON} and the requirement for C by the same factor, and decrease R_{ON} by a factor of $\sqrt{\boldsymbol{\xi}}$ **(**because the optimum PMOS width value has to increase when lowering the frequency). Hence the index of the modulation factor will overall increase by approximately a factor of $\sqrt{\boldsymbol{\xi}}$.

3.3.2.4 Short circuit current

Clock drivers (inverters) are used to drive the pumping capacitors with the pump clock. A typical configuration of the clocking scheme where a clock generator, fabricated on chip, is buffered then fed to the clock driver as shown in Fig. 3.10. The clock generator has its own buffer which was not shown in the diagram. The Clock buffers in Fig. 3.10 were used to create equal delays to the CP drivers as will be explained in Section 3.5.2.

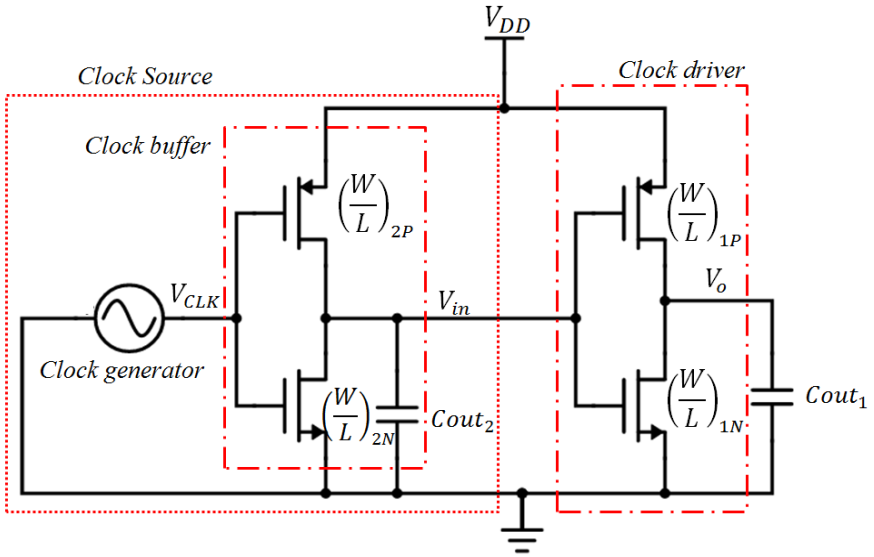


Fig. 3.10. Schematic showing the clock source (which is composed of a clock generator and a buffer) and the clock driver used to drive the pumping capacitors

In the derivations presented below, the width of the PMOS transistors has been chosen as three times the width of the NMOS transistors. This would be a typical choice, for the same length devices, in order to compensate for the differences in holes and electrons mobility.

C_{out2} is the parasitic capacitance at the output of the clock's buffer and can be approximated as:

$$C_{out2} \approx C_{ox}L_1(W_{1P} + W_{1N}) = 1.3C_{ox}L_1W_{1P} \tag{3.42}$$

C_{out1} is the parasitic capacitance at the bottom plate of the pumping capacitor. The pumping capacitor (C) has no effect on this expression because the voltage difference across its terminals is always V_{DD} and hence $C_{out1} = \alpha_B C$.

t_{CLK} is defined as the rise/fall time of the clock at node V_{CLK}. Similar expressions applies for t_{in} and t_o. Expressions t_{CLK} and t_o can be expressed as a percentage (τ) of the clock period (T) as: $t_{CLK} = \tau_{CLK}T$ and $t_o = \tau_o T$.

A short circuit current path is created in the driver (inverter) between the power supply and ground during transitions of the input clock; specifically when the input V_{in} is in the range:

$$V_{thn} < V_{in} < V_{DD} - |V_{thp}| \tag{3.43}$$

That is when the PMOS and the NMOS devices are simultaneously ON. The quicker the input transition is, the smaller is the window of time when both devices are simultaneously ON and hence quick rise/fall time of the input clock gives less short circuit power loss. The short circuit power loss in an inverter with equal threshold voltage devices is [30] :

$$P_{loss-driver} = \frac{\beta t_{in}[V_{DD} - 2V_{th}]^3}{12} f \tag{3.44}$$

It can be seen from (3.44) that the short circuit power losses decrease for lower supply voltages, and are totally eliminated when $V_{DD} < 2V_{th}$, as in this case both devices can never be turned ON at the same time. This implies that using high threshold-voltage devices would reduce the inverter's short circuit power losses.

If the inverter is designed in such a way that the PMOS and NMOS devices are matched then the rise and fall times will be equal. The fall time (t_f) is defined as the time it takes for the

inverter's output to fall from 90% to 10% of V_{DD}, and vice versa for the rise time (t_r). The transistors dimensions to achieve a specific fall/rise time can be approximated as [30] :

$$\beta = \frac{4C_{out}}{t_{f,r}(V_{DD} - V_{th})} \tag{3.45}$$

Where C_{out} is the capacitor at the inverter's output.
The transistor size inside the CP's clock drivers can be then written as:

$$\beta_{1P} = \frac{4\alpha_B C}{t_0(V_{DD} - V_{th})} \tag{3.46}$$

The value of β_{1P} depends on the value of the pumping capacitor. For a fixed t_0, larger transistors will be needed to drive larger pumping capacitors. Substituting (3.46) in (3.44), the CP clock drivers' short circuit power loss can be obtained in terms of the ratio $t_{in}/\ t_0$:

$$P_{loss-driver} = \frac{\alpha_B \frac{t_{in}}{t_0}[V_{DD} - 2V_{th}]^3}{3(V_{DD} - V_{th})} \times fC \tag{3.47}$$

$$= K_{Inv} \times fC$$

In order to minimize the CP clock drivers' power losses, it is important to design the transistors in the inverter in such a way that the rise/fall time at the output is bigger than the rise/fall time of the signal at the input, i.e. $t_{in}/\ t_0 < 1$ [30] . Based on this, it would be best to choose the ratio t_{in}/t_0 as small as possible to reduce the short circuit power loss in the clock driver. This can be achieved by either making t_0 as big as possible or t_{in} as small as possible. There are however limits on the largest value of t_0 and the smallest value of t_{in} and hence there is a limit on the minimum value of $t_{in}/\ t_0$. A slow rise/fall time of the clock at the pumping capacitor (large t_0) will reduce the efficiency and output voltage of the CP. Simulation results indicate that limiting the rise/fall time in one clock period to less than 5% the period (i.e. $\tau_o \leq 5\%$) does not have much effect on the CP performance. On the other hand, a quick rise/fall time of the input clock (small t_{in}) will increase the power consumption of the clock's buffer and will impose a limitation on the clock's generator rise/fall time (t_{CLK}), which increases the clock generator's power consumption as well. This is important because even though the power

consumption of the clock generator and its buffer are not considered in the efficiency calculation of the CP, these will be part the overall System-on-Cip (SoC). Hence their power consumption will affect the performance of the system as a whole. It is therefore important to optimize these blocks' power consumption as well.

The total power consumption of the clock buffer (dynamic and short circuit losses) can be written as:

$$P_{loss-Clk} = fC_{out2}\left(V_{DD}{}^2 + \frac{\frac{t_{CLK}}{t_{in}}(V_{DD} - 2V_{th})^3}{3(V_{DD} - V_{th})}\right) \tag{3.48}$$

Equation (3.48) can be written in terms of $t_{in}/\ t_0$ as:

$$P_{loss-Clk} = fC_{out2}V_{DD}{}^2\left(1 + \frac{\tau_{CLK}}{3\,\tau_o}\frac{(1-2\alpha_{th})^3}{(1-\ \alpha_{th})}\frac{1}{t_{in}/\ t_0}\right) \tag{3.49}$$

Where $\alpha_{th} = V_{th}/V_{DD}$

By designing the ratio $t_{in}/\ t_0$ large enough such that

$$\frac{\tau_{CLK}}{3\tau_o}\frac{(1-2\alpha_{th})^3}{(1-\ \alpha_{th})}\frac{1}{t_{in}/\ t_0} \leq 0.1 \tag{3.50}$$

the total power consumption of the clock's buffer can be made very weakly dependent on t_{CLK}. Equation (3.50) puts a minimum limit on $t_{in}/\ t_0$ and can be expressed as:

$$\frac{t_{in}}{t_0} \geq 3.3\ \frac{\tau_{CLK}}{\tau_o}\frac{(1-2\alpha_{th})^3}{(1-\ \alpha_{th})} \tag{3.51}$$

Satisfying (3.51) will satisfy (3.50). This will make the total power consumption of the clock's buffer, as well as the value t_{in}, and consequently the ratio $t_{in}/\ t_0$, to be very weakly dependent on the input clock rise/fall time (t_{CLK}). This is because the clock's buffer can be designed with fixed transistor dimensions to achieve a specific fixed value of t_{in} with its total power consumption to be insensitive to t_{CLK} as its power consumption will be dominated by its dynamic losses, and hence t_{in} does not have to be adjusted for a change in t_{CLK}. This is a useful feature because it allows flexibility in the design of the clock generator. For example, the clock

generator can be designed in such a way that its area and power consumption are optimized with a specific rise/fall time. This would have a very small effect on the clock's buffer power consumption and on the ratio $t_{in}/\ t_0$.

A plot of (3.51) for $\tau_o = 5\%$ against α_{th} for different values of τ_{CLK} is shown below:

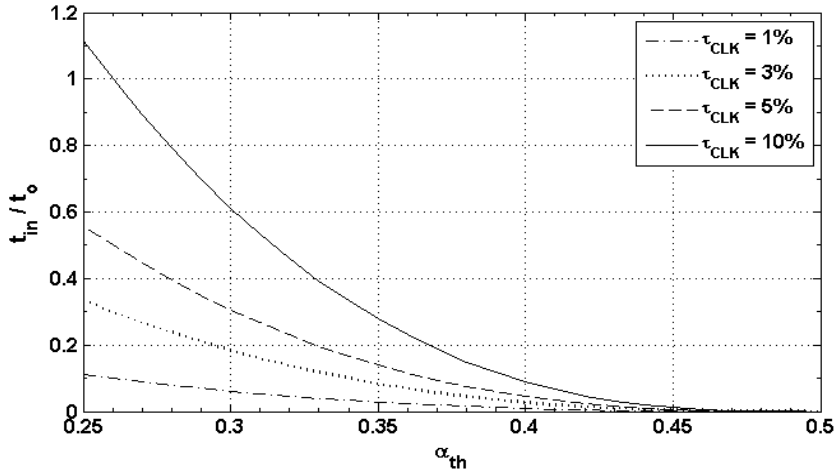


Fig. 3.11. Plot of (3.51) for τ_o=5% against α_{th} for different values of τ_{CLK}

For SoC designs where $\alpha_{th} > 0.3$, the minimum ratio of $t_{in}/\ t_0$ is well below one (~0.6) for t_{CLK} up to 10% of the clock's period. A rise/fall time that is equal to 10% of the clock's period can be easily designed without excessive power consumption in the clock generator. However, if a more relaxed rise/fall time in the clock generator is required, then the ratio of $t_{in}/\ t_0$ can be made a little bit bigger without having much effect on the CP's efficiency. This is because the clock's driver power loss, when carefully designed, represents a small fraction of the total CP's power loss. This can be seen in Fig. 3.13

3.3.3 Efficiency calculation

The CP's efficiency is defined as:

$$\eta = \frac{P_{Load}}{P_{Load} + P_{loss-total}} \tag{3.52}$$

The total power loss $P_{loss-total}$ is:

$$\begin{aligned} P_{loss-total} &= P_{loss-parasitic} + P_{loss-R_s} + P_{loss-driver} \\ &= 2fC(\alpha_B + \alpha_T){V_{DD}}^2 + \frac{{i_L}^2}{2fC} + K_{Inv}fC \end{aligned} \tag{3.53}$$

The power delivered to the load P_{Load} is:

$$P_{Load} = i_L \times V_{out} = i_L \gamma V_{DD} - \frac{{i_L}^2}{2fC} \tag{3.54}$$

Substituting (3.53) and (3.54) in (3.52):

$$\eta = \frac{i_L Vout}{i_L Vout + 2fC(\alpha_B + \alpha_T){V_{DD}}^2 + \frac{{i_L}^2}{2fC} + K_{Inv} fC} \tag{3.55}$$

$$= \frac{2fCi_L \gamma V_{DD} - {i_L}^2}{2fCi_L \gamma V_{DD} + 4f^2C^2(\alpha_B + \alpha_T){V_{DD}}^2 + 2K_{Inv} f^2C^2} \tag{3.56}$$

A plot of the efficiency versus the output voltage is presented in Fig.3.12 below:

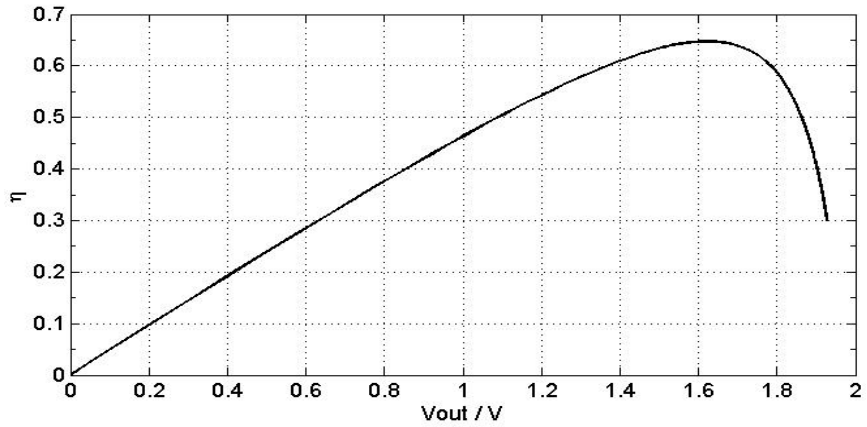


Fig.3.12. Variation of the CP's efficiency with its output voltage

This graph was obtained by varying the value of the pumping frequency from 1MHz to 60MHz in small steps (using MATLAB), and for every step the corresponding output voltage and efficiency were calculated. It can be seen from the graph that the efficiency is maximized at a single output voltage. This output voltage can be obtained by re-writing the efficiency expression as:

$$\eta = \frac{i_L V_{out}}{\frac{i_L(\alpha_B + \alpha_T){V_{DD}}^2 + 0.5K_{Inv} i_L}{\gamma V_{DD} - V_{out}} + i_L \gamma V_{DD}} \tag{3.57}$$

And differentiate with respect to V_{out} to obtain the maximum. This yields the following equation:

$$Vout_{opt} = \frac{b - \sqrt{b^2 - 4ac}}{2a} \tag{3.58}$$

Where: $a = \gamma V_{DD} i_L$

$$b = 2i_L\left((\alpha_B + \alpha_T){V_{DD}}^2 + 0.5K_{Inv} + \gamma^2 {V_{DD}}^2\right)$$

$$c = \gamma V_{DD} i_L\left((\alpha_B + \alpha_T){V_{DD}}^2 + 0.5K_{Inv} + \gamma^2 {V_{DD}}^2\right)$$

The term $0.5K_{Inv}$ is very small compared to the other terms, and hence the variables $a, b\ c$ can be expressed in a more compact form as:

$$a = \gamma V_{DD} i_L \tag{3.58a}$$

$$b = 2{V_{DD}}^2 i_L\left((\alpha_B + \alpha_T) + \gamma^2\right) \tag{3.58b}$$

$$c = \gamma {V_{DD}}^3 i_L\left((\alpha_B + \alpha_T) + \gamma^2\right) \tag{3.58c}$$

This value of V_{out} corresponds to the optimum value of fC:

$$(fC)_{opt} = \frac{i_L}{2\left(\gamma V_{DD} - V_{out_{opt}}\right)} \tag{3.59}$$

This optimum value of fC is approximately the point where the dominant power losses due to various mechanisms are equal. This is visualized in Fig. 3.13:

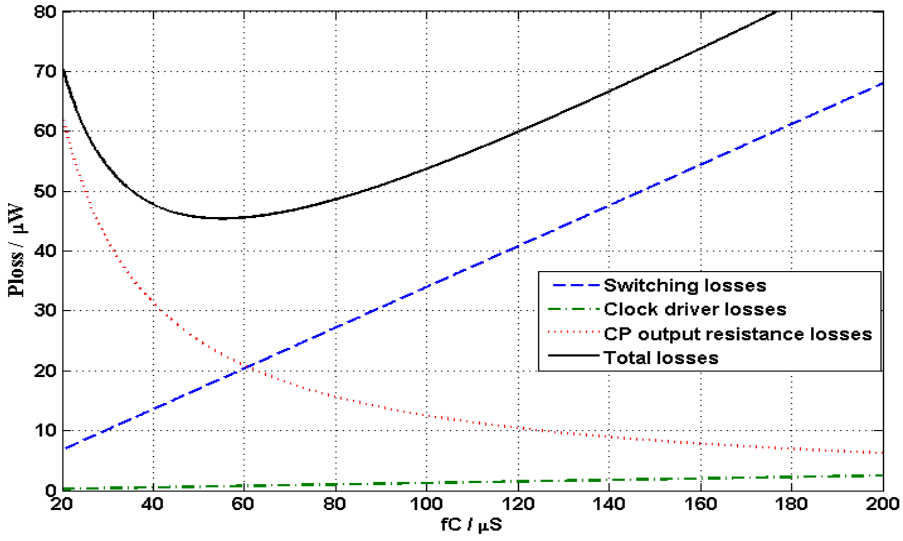


Fig. 3.13. Different power losses and total power losses plotted against different value of fC

Fig. 3.13 shows that the losses due to parasitic capacitances and due to the CP's output resistance are the dominate losses mechanisms. The short circuit power loss in the clock driver can be made a very small fraction of the total losses with proper designing.

A plot of the efficiency versus the ratio of the total parasitic capacitance ($\alpha_{total} = \alpha_B + \alpha_T$) is shown in Fig. 3.14:

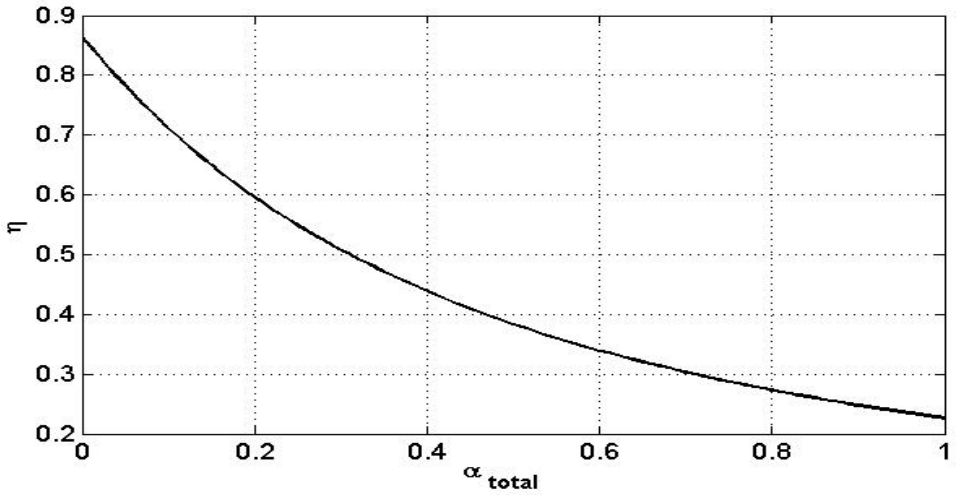


Fig. 3.14. Effect of total parasitic capacitances on efficiency

Fig. 3.14 shows that minimizing parasitic capacitances is crucial to optimize the CP efficiency. Beside the existing parasitic capacitances at the top and bottom plate of the pumping capacitor, it is important to minimize the amount of parasitic capacitors added to the circuit when doing the layout, by employing techniques such as using thin tracks with the highest metal layer to connect the devices in the CP.

The complete proposed design procedure is summarized in the flow chart in Fig. 3.15.

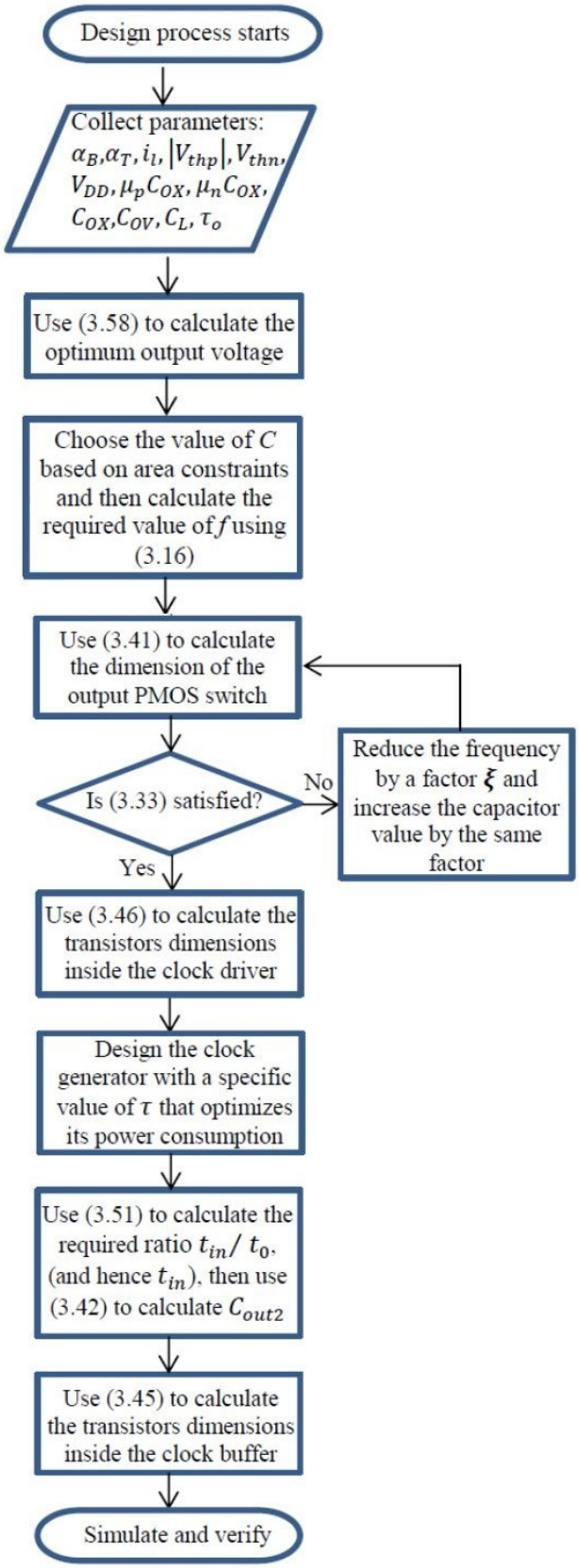


Fig. 3.15. Flow chart of the complete design process to optimize the efficiency of the CP

3.4 Reversion losses in charge pumps

Reversion losses are a major cause in degrading the efficiency of CPs and a non-overlapping clock scheme is crucial to eliminate these losses and improve the CP's efficiency. However, employing a non-overlapping clock scheme will increase the total Silicon area and can increase the total current consumption of the CP. The increase in CP's current consumption, due to a non-overlap clock scheme, is dependent on the scheme's current consumption and on the improvement in efficiency it provides. The latter depends on the severity of reversion losses' impact on the CP's efficiency and output voltage for a set of design parameters. This section analyzes reversion losses in cross-coupled CPs and characterizes them with a mathematical model. The model can be used to evaluate the impact of reversion losses on the CP's efficiency and accordingly assess the merit of using a non-overlapping clock scheme for different design parameters. The model is verified through circuit simulations in Cadence environment using a CMOS 0.18μm 6-metal layers technology.

The CP's efficiency is optimized by eliminating reversion losses, which are a major factor in degrading it, especially at high supply voltage and high clocking frequency [22]. Reversion losses occur due to the overlap of the clocks that control the MOS switches inside the CP, which causes an undesirable reverse flow of charge from higher to lower voltage nodes, degrading the output voltage and the efficiency of the CP. Reversion losses can be eliminated by employing a non-overlapping clock scheme that prevents improper timing of switching the MOS transistors. Several papers that qualitatively analyze reversion losses and propose different non-overlapping clock schemes to eliminate them are reported in the literature [31-34]. These schemes require either extra circuitry to generate the non-overlapping clocks [31, 32, 33] or use large area-consuming poly resistors to control the switching rate of the MOS switches [34]. These solutions are effective when the CP is operated at a supply voltage greater than 2V or when it is used to supply an output load current greater than 5mA. However, no data measurement is presented on their effectiveness at a smaller output load current or at low supply voltage operation. The improvement in CP's efficiency these schemes might introduce, at small output load current and low supply voltage operation, might not be justified by the extra Silicon area and current consumption they add. However, this is very dependent on the design parameters. In order to assess the merit of different non-overlapping schemes, the impact of reversion losses on the CP's efficiency and output voltage must be evaluated. This requires mathematical modelling of the

reversion losses. Unfortunately, such modeling is missing from the literature and is going to be derived here.

3.4.1 Reversion Losses Analysis

The circuit diagram of the cross-coupled CP from [22] and its timing diagram are shown in Fig.3.16 and Fig.3.17 respectively:

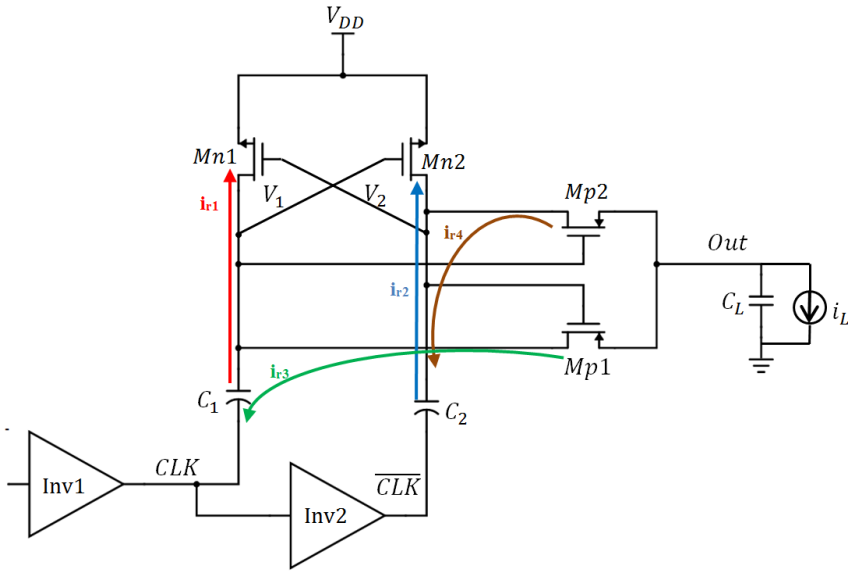


Fig. 3.16. Schematic of the CMOS cross coupled CP with arrows that show the different paths of reversion currents

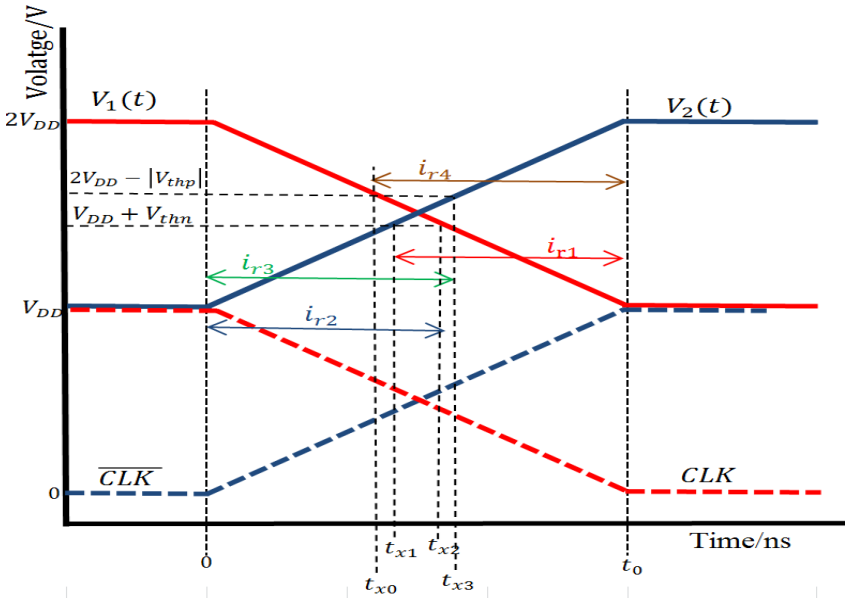


Fig. 3.17. Timing diagram of the CP showing overlapping clocks and the duration of different reversion currents

The circuit is perfectly symmetrical and all components have the same design parameters($C_1 = C_2 = C$), CLK and $\overline{CLK}$ are complementary clocks with amplitude equal to the supply voltage (V_{DD}). The circuit principle of operation in steady state is as follows: node V_1 is initially at $2V_{DD}$ and node V_2 is at V_{DD}. As CLK goes low and $\overline{CLK}$ goes high, node V_1 is discharged to V_{DD} and node V_2 is boosted to $2V_{DD}$ turning *Mn2* OFF and *Mn1* ON. This sequence of events turn *Mp2* ON and *Mp1* OFF and thus the output is at $2V_{DD}$.

Reversion current 2 (i_{r2}) flows because *Mn2* is not fully switched OFF while node V_2 is being boosted above V_{DD} when $\overline{CLK}$ starts rising. This shorts node V_2 to the supply voltage which causes a backward charge flow from C_2 to the supply voltage and decreases the boosted output voltage and the efficiency. The duration of i_{r2} is from when $\overline{CLK}$ starts rising at $t = 0$ until when *Mn2* is switched OFF, which is when V_1 reaches the value of $V_{DD} + V_{thn}$ at $t = t_{x2}$ as shown in Fig. 3.17.

Reversion current 1 (i_{r1}) flows because *Mn1* gets turned on before node V_1 is fully discharged to V_{DD}. It starts flowing when node V_2 reaches the value of $V_{DD} + V_{thn}$ at $t = t_{x1}$ until node V_1 is fully discharged to V_{DD} at $t = t_0$.

The expressions for voltages $V_1(t)$ and $V_2(t)$ during the transition of the clocks are written as:

$$\left.\begin{aligned} V_1(t) &= 2V_{DD} - \left(\frac{V_{DD}}{t_0}\right)t \\ V_2(t) &= V_{DD} + \left(\frac{V_{DD}}{t_0}\right)t \end{aligned}\right\}, 0 \le t \le t_0 \qquad (3.60)\ (3.61)$$

Where t_0 is the overlap time between the rising and falling edges of the complementary clocks.

Time t_{x2} is written as:

$$t_{x2} = (1 - \alpha_n)t_0 \qquad (3.62)$$

Where $\alpha_n = V_{thn}/V_{DD}$

Mn2 is in the triode region from $t = 0$ until $t = t_{x2B}$. Hence:

$$V_2(t_{x2B}) = V_1(t_{x2B}) - V_{thn} \qquad (3.63)$$

Equation (3.63) is solved to find t_{x2B} as:

$$t_{x2B} = \frac{1}{2}(1-\alpha_n)t_0 = \frac{1}{2}t_{x2} \tag{3.64}$$

Current i_{r2} which flows through *Mn2* can be written as the sum of two currents:

$$i_{r2}(t) = i_{r2A}(t) + i_{r2B}(t) \tag{3.65}$$

Where

$$\begin{aligned} i_{r2A}(t) &= \beta_n[V_1(t) - (V_{DD} + V_{thn})][V_2(t) - V_{DD}] \qquad 0 \le t \le \frac{1}{2}t_{x2} \\ &= {V_{DD}}^2\beta_n\left[(2-\alpha_n)\left(\frac{t}{t_0}\right) - 2\left(\frac{t}{t_0}\right)^2\right] \end{aligned} \tag{3.66}$$

$$\begin{aligned} i_{r2B}(t) &= \frac{1}{2}\beta_n\big(V_1(t) - (V_{DD} + V_{thn})\big)^2 \qquad \frac{1}{2}t_{x2} < t \le t_{x2} \\ &= \frac{1}{2}\beta_n {V_{DD}}^2\left[\left(\frac{t}{t_0}\right)^2 + \frac{2t}{t_0}(\alpha_n - 1) + (\alpha_n - 1)^2\right] \end{aligned} \tag{3.67}$$

Equations (3.66) and (3.67) are written under the assumption that V_{DS} is very small and the channel length modulation is negligible. The total charge lost from the pumping capacitor due to i_{r2} is:

$$Q_{loss2} = \int_0^{\frac{1}{2}t_{x2}} i_{r2A}(t)\,dt + \int_{\frac{1}{2}t_{x2}}^{t_{x2}} i_{r2B}(t)\,dt \tag{3.68}$$

Substituting (3.66) and (3.67) into (3.68) to get the total charge loss due to i_{r2}:

$$Q_{loss2} = \frac{5}{48}\beta_n t_0 {V_{DD}}^2(1-\alpha_n)^3 \tag{3.69}$$

This loss in charge will contribute to a voltage loss from node V_2 and prevent it from reaching the ideal value of $2V_{DD}$. The voltage loss is calculated as:

$$V_{loss2} = \frac{Q_{loss2}}{C} = \frac{5}{48}\frac{\beta_n {V_{DD}}^2 t_0}{C}(1-\alpha_n)^3 \tag{3.70}$$

Due to circuit symmetry, currents i_{r1} and i_{r2} have similar magnitude and they flow for the same duration of time. The power loss associated with i_{r1} and i_{r2} is calculated as the difference in the energy stored in the pumping capacitors with no reversion loss and with reversion loss:

$$P_{loss1,2} = 2f\left\{\frac{1}{2}C{V_{DD}}^2 + 2C{V_{DD}}^2 - \frac{1}{2}C(V_{DD} - V_{loss2})^2 - \frac{1}{2}C(2V_{DD} - V_{loss2})^2\right\}$$

$$\approx 6V_{DD}\, fCV_{loss2} = \frac{5}{8}f\beta_n {V_{DD}}^3 t_0(1-\alpha_n)^3 \tag{3.71}$$

Reversion current 3 (i_{r3}) flows because *Mp1* is not fully switched OFF while node V_1 is being discharged to V_{DD} when CLK starts falling. This shorts node V_1 to the output causing a backward flow of charge from the output to node V_1 which decreases the output voltage and the efficiency. The duration of i_{r3} is from when CLK starts falling at $t = 0$ until when *Mp1* is switched OFF, which is when V_2 reaches the value of $2V_{DD}$-$|V_{thp}|$ at $t = t_{x3}$.

Reversion current 4 (i_{r4}) flows because *Mp2* gets turned ON before node V_2 is fully boosted to $2V_{DD}$. It starts flowing once node V_1 reaches the value of $2V_{DD}$-$|V_{thp}|$ at $t = t_{x0}$until node V_2 reaches a voltage of $2V_{DD}$ at from $t = t_0$.

Mp1 will initially be in triode region, when i_{r3} starts flowing until $V_1 \geq V_2 + |V_{thp}|$. To simplify the calculation in this analysis, it is assumed that *Mp1* is in triode region for the whole duration of time that i_{r3} flows for. Hence, i_{r3} is:

$$i_{r3}(t) \approx \beta_p\left[V_{out} - \left(V_2(t) + |V_{thp}|\right)\right][V_{out} - V_1(t)] \quad 0 \leq t \leq t_{x3}$$

$$= {V_{DD}}^2\beta_p\left[(1-\alpha_p)\left(\frac{t}{t_0}\right) - \left(\frac{t}{t_0}\right)^2\right] \tag{3.72}$$

Where $\alpha_p = |V_{thp}|/V_{DD}$

Time t_{x3} is expressed as:

$$t_{x3} = t_0(1-\alpha_p) \tag{3.73}$$

The reverse charge that flows from the output to node V_1:

$$Q_{loss3} = \int_0^{t_{x3}} i_{r3}(t)\, dt$$

$$= \frac{1}{6} {V_{DD}}^2 \beta_p t_0 \left(1 - \alpha_p\right)^3 \tag{3.74}$$

The voltage loss at the output can be written as:

$$V_{loss3} = \frac{Q_{loss3}}{C_L} = \frac{{V_{DD}}^2 \beta_p t_0}{6C_L} \left(1 - \alpha_p\right)^3 \tag{3.75}$$

The power and voltage loss due to i_{r3} are the same as for i_{r4} because of circuit symmetry and hence the total power loss associated with i_{r3} and i_{r4} is:

$$\begin{aligned} P_{loss3,4} &= 2f \left\{ \frac{1}{2} C (2V_{DD})^2 + \frac{1}{2} C_L (V_{out})^2 - \frac{1}{2} (C + C_L)(2V_{DD} - V_{loss3})^2 \right\} \\ &= \frac{2}{3} f {V_{DD}}^3 \beta_p t_0 \frac{(C + C_L)}{C_L} \left(1 - \alpha_p\right)^3 \end{aligned} \tag{3.76}$$

The total power loss due to i_{r1}, i_{r2}, i_{r3} and i_{r4} is approximated as (assuming $C_L \gg C$):

$$\begin{aligned} P_{Rev} &= P_{loss1,2} + P_{loss3,4} \\ &\approx f {V_{DD}}^3 t_0 \left\{ \frac{5}{8} \beta_n (1 - \alpha_n)^3 + \frac{2}{3} \beta_p \left(1 - \alpha_p\right)^3 \right\} \end{aligned} \tag{3.77}$$

For matched NMOS and PMOS devices (3.77) reduces to:

$$P_{Rev} \approx 1.3 f {V_{DD}}^3 \beta t_0 (1 - \alpha)^3 \tag{3.78}$$

And the final voltage of the CP is written as:

$$V_{out} \approx 2V_{DD} - 2(V_{loss3} + V_{loss1}) \tag{3.79}$$

The total power loss is independent on the pumping capacitor. It is dependent on the pumping clock frequency, rise/fall time of the clocks, parameters of the MOS switches and most importantly it is a non-linear monotonic increasing function of the supply voltage.

There are two more paths of reversion currents that flow from the output to the supply voltage(i_{r5}, i_{r6}). Current i_{r5} flows through *Mp1* and *Mn1;* and i_{r6} flows through *Mp2* and *Mn2*. Current i_{r5} flows when *Mp1* and *Mn1* are simultaneously ON, which is represented by the overlap between i_{r1} and i_{r3}. Similarly, current i_{r6} flows when *Mp2* and *Mn2* are simultaneously

ON, which is represented by the overlap between i_{r2} and i_{r4}. Currents i_{r5} and i_{r6} flow when $V_{DD} \geq V_{thn} + |V_{thp}|$ and their duration is proportional to the supply voltage. However for this analysis, the supply voltage is assumed to be sufficiently small such that the duration of i_{r5} and i_{r6} is small compared to i_{r1}, i_{r2}, i_{r3} and i_{r4}.

3.4.2 Reversion Losses and Efficiency

In this section, the effects of reversion losses on the efficiency and boosting ratio of the CP are analyzed for a range of supply voltages. The boosting ratio is defined as the ratio of the output voltage defined in (3.79) over the ideal output voltage $\left(\frac{V_{out}}{V_{out_{ideal}}}\right)$, where $V_{out_{ideal}} \approx 2V_{DD}$ at no load current and neglecting the effect of parasitic capacitances.

The power efficiency of the CP without reversion losses (η_1) is given by equation (3.56) as:

$$\eta_1 = \frac{P_{out}}{P_{out} + P_{res} + P_{dyn} + P_{inv}} = \frac{2fCi_L\gamma V_{DD} - {i_L}^2}{2fCi_L\gamma V_{DD} + 4f^2C^2(\alpha_B + \alpha_T){V_{DD}}^2 + 2K_{inv}f^2C^2}$$

For identical PMOS and NMOS devices inside the inverter, K_{inv} is given by (3.47) as $\alpha_B \frac{t_{in}}{t_0}[V_{DD} - 2V_{th}]^3/3(V_{DD} - V_{th})$.

If a non-overlapping clock scheme is not used, then reversion losses must be taken into account when calculating the efficiency of the CP, and hence (3.56) is re-written as:

$$\eta_2 = \frac{P_{out}}{P_{out} + P_{res} + P_{dyn} + P_{inv} + P_{Rev}} \tag{3.80}$$

A plot of η_1,η_2 and the simulated efficiency (in Cadence CMOS AMS 0.18µm technology) against the supply voltage is in Fig. 3.18 and the ratio of $\frac{\eta_2}{\eta_1}$ and the boosting ratio with simulations is in Fig. 3.19 using the following design parameters:

$f = 10MHz, C = 10pF, i_L = 50\mu A$, $C_L = 100pF$, t_0=1.5 ns, $t_{in} = 0.5ns$, $V_{th} = 0.4V$, $\alpha_B = 0.17, \alpha_T$ =0.03,$\beta = 1 \times 10^{-3}$.

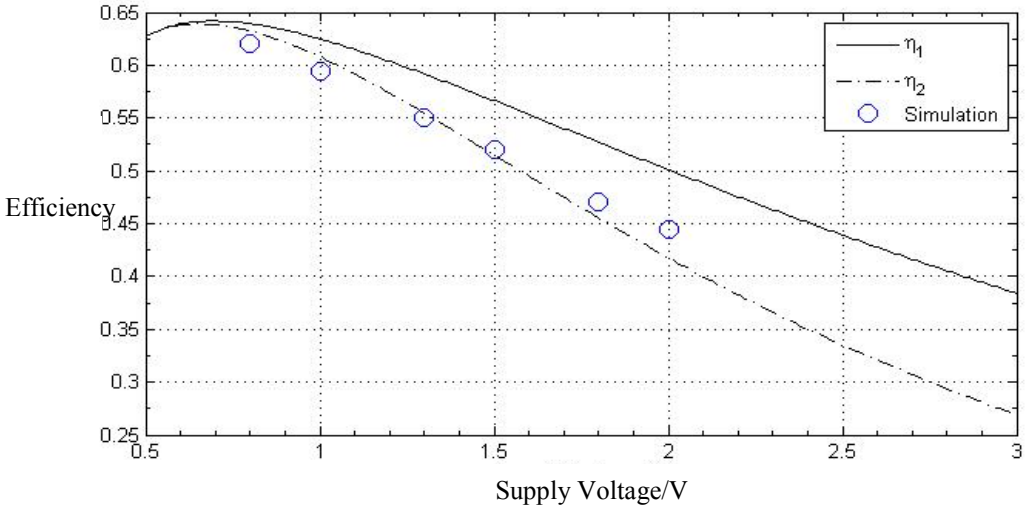


Fig. 3.18. Effect of the reversion loss on CP efficiency against varying supply voltage with simulations results

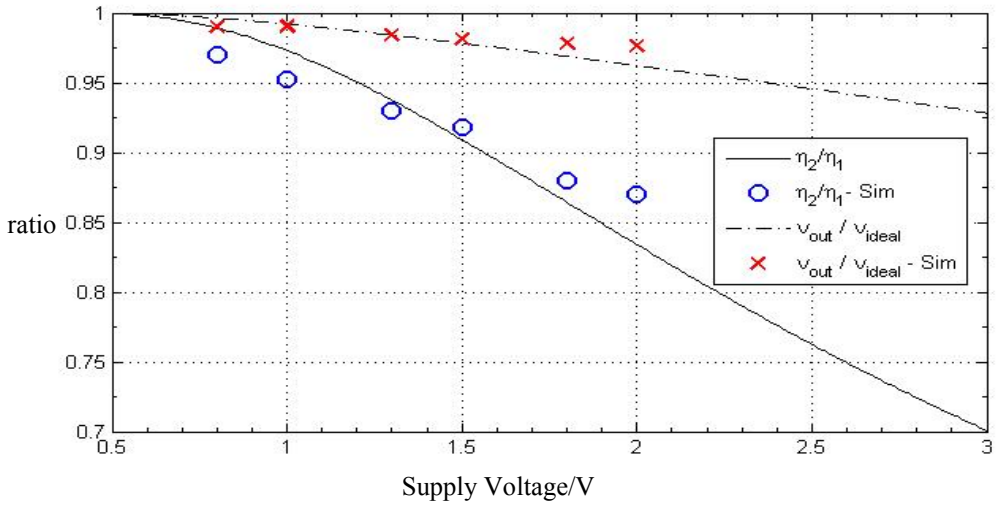


Fig. 3.19. Ratio of deterioration in CP efficiency and boosting ratio due to reversion loss against the supply voltage

Fig. 3.18 and Fig. 3.19 show close simulation results with the theory. The simulation results are below the theoretical ones for lower supply voltage, and exceed them as the supply voltage increases. This is because the rise/fall time of the clocks was assumed to be constant at 1.5ns in theory. However in reality, it is inversely proportional to the supply voltage. Reversion losses are proportional to the rise /fall time of clocks, hence the efficiency is lower than theory at low supply voltage (2% lower at 0.8V) and exceeds it as the supply voltage increases (3.5% higher at 2V).

Reversion losses have stronger negative impact on the CP's efficiency for supply voltages greater than 1.2V as can be seen by Fig. 3.18 and Fig. 3.19. This is expected because equation (3.78) shows that the power loss due to reversion currents is a cubic function of the supply voltage and therefore a non-overlapping clock scheme is mandatory to optimize the CP's efficiency at supply voltage greater than 1.2V. For operation at supply voltages below 1.2V, which is the typical supply voltage for small wearable biomedical devices, reversion losses cause 5% reduction in efficiency. The impact of reversion losses on the boosting ratio is less significant than on efficiency, a 1.5% and 3.5% reduction in boosting ratio due to reversion losses at 1.2V and 2V supply voltage respectively. The 5% and 1.5% improvement in efficiency and output voltage, respectively, introduced by employing a non-overlapping clock scheme at supply voltages less than 1.2V, is not be justified by the extra area and current consumption added with it and therefor a non-overlapping scheme was not used in this design.

The results in this section correlate positively with the Silicon measurements performed in [33], where a new non-overlapping clock scheme was proposed to eliminate reversion losses in the cross-coupled CP. The measurements were done on a cross-coupled CP with 20pF pumping capacitors and 10MHz pumping clock frequency for a supply voltage range of 1V-2V. Measurements have shown that the boosting ratio, for a supply voltage lower than 1.2V, is approximately the same for a non-overlapping clock scheme and for an overlapping one, at 99% (no output load current). As the supply voltage increases to 2V, the boosting ratio remains at 99% for the non-overlapping scheme while it drops to 95% for the overlapping one. These measurements are close to the results obtained from the analysis in this paper and presented in Fig. 3.19.

3.5 Design, simulations and measurements

3.5.1 CP Design

This section describes and illustrates the design process of the CP and its clock source. The charge pump has to be designed to drive the microphone with supply voltage specs in the 1.5V-3V range, with a fixed current consumption of 50 μA. The design parameters are:

$\alpha_B = 0.17, \alpha_T = 0.03, \tau_o = 1.5\%, |V_{thp}| \approx V_{thn} = 0.4\text{V}, \mu_p C_{OX} = 40 \times 10^{-6}, \mu_n C_{OX} = 120 \times 10^{-6}, C_L = 100pF, C_{OX} = 8.5fF/\mu m^2, C_{OV=} 0.5fF/\mu m$

The target is to maximize the efficiency whilst minimizing the area needed to implement the design (i.e. use smallest possible capacitor values). The supply voltage at which the CP is operated at must be determined first. To do that, the efficiency was plotted against the output voltage [equation (3.57)] for different supply voltages in Fig. 3.20, using the previously mentioned designed parameters.

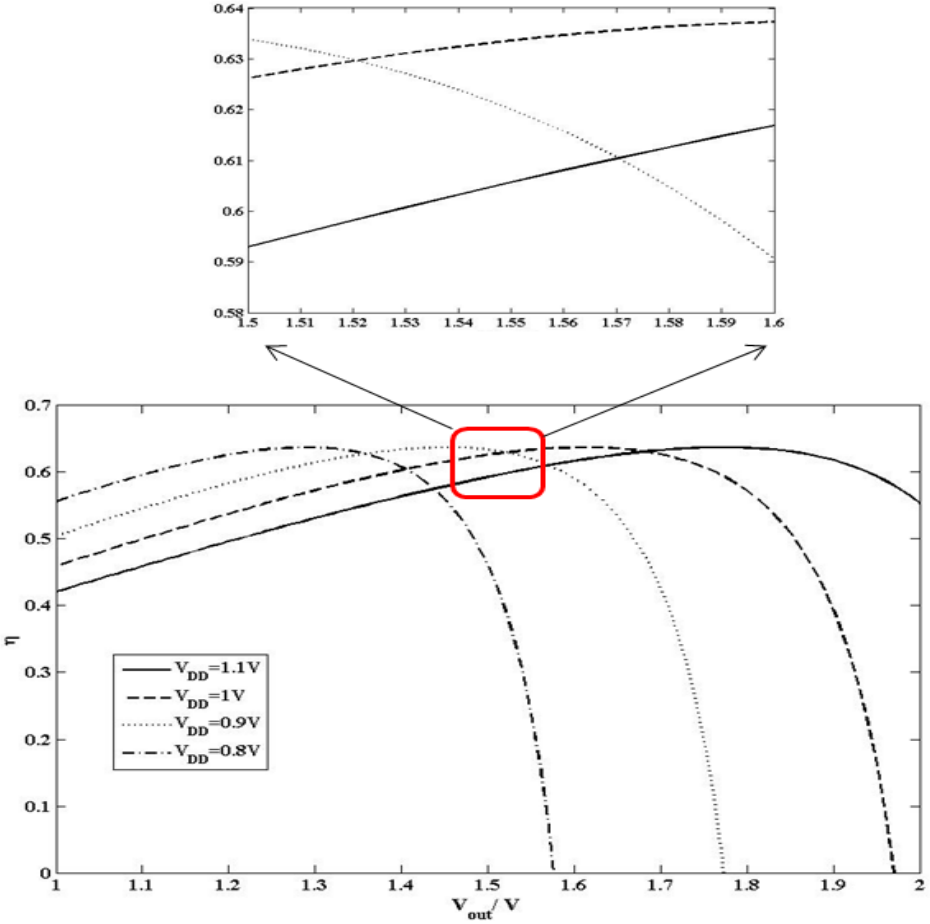


Fig. 3.20. The variation of CP's efficiency with output voltage for different supply voltages

Fig. 3.20 shows that the optimum voltage to supply the CP from is at $V_{DD} = 1V$. This is the minimum supply voltage where the efficiency of the CP is highest between 1.5V-1.6V output voltages and with minimum variations. Thus, the CP supply was set to 1V. The 1V supply will be generated from the chip's supply voltage (1.4V-1.2V) using a resistor as will be explained later in section 3.5.4. Using equation (3.58) to find the optimum voltage for maximum efficiency gives $Vout_{opt}$=1.612V. Choosing the pumping capacitor value as 10pF to keep the design area small, and by using (3.16), the required pumping frequency f=7MHz. Even though the efficiency

plots in Fig. 3.18 and Fig. 3.19 were done using pumping frequency of 10MHz, however they are still valid at lower pumping frequency. This is because reversion losses decrease with lower pumping frequency and hence better efficiency is going to be achieved compared to the results shown in in Fig. 3.18 and Fig. 3.19.

Using (3.41) to calculate the optimum dimensions of the output PMOS switch gives: $\left(\frac{W}{L}\right)_p = \frac{28\mu}{0.2\mu}$.

Check if equation (3.33) is satisfied:

$$\frac{1}{2R_{ON} \times fC} = \frac{71.4n}{892 * 10p} = 8 > 2$$

If this condition was not satisfied, then the pumping frequency would have to be lowered and the pumping capacitor increased accordingly to get the required output.

The value of $t_o = \frac{1.5\%}{7\text{MHz}} \approx 2.2ns$. Use (3.46) to calculate the required transistors dimensions inside the clock driver:

$$\left(\frac{W}{L}\right)_{1P} = \frac{24\mu}{0.2\mu} \qquad \text{And} \qquad \left(\frac{W}{L}\right)_{1N} = \frac{8\mu}{0.2\mu}$$

The clock generator is designed with $\tau_{CLK} = 4\%$ and hence from (3.51) the ratio of $t_{in}/\ t_0 \geq 0.117$. Choose $t_{in}/\ t_0 = 0.2$ and hence $t_{in} = 0.43ns$. C_{out2} is calculated using (3.42) as $44fF$.

Use (3.45) to calculate the required transistors dimensions inside the clock buffer:

$$\left(\frac{W}{L}\right)_{2P} = \frac{9\mu}{0.5\mu} \qquad \text{And} \qquad \left(\frac{W}{L}\right)_{2N} = \frac{3\mu}{0.5\mu}$$

3.5.2 Clock source Design

The clock source consists of a ring oscillator and buffers as shown in Fig. 3.21. The clock source was designed using a ring oscillator with five cascaded inverters connected to 300fF capacitor load to generate a 7MHz clock. The transistors at the bottom of the capacitors were used to control the effective capacitance at the output of the inverter by changing the control signal V_C. This was added to tune the frequency of the oscillator after fabrication and reduce the effect of mismatch and process variation. The voltage range of V_C was from 1.2V-0.55V, which

resulted in a clock frequency range from 5.36 MHz -20.2 MHz respectively. The clock buffers were designed to output two perfectly overlapped complementary clocks to minimize reversion losses in the CP. The perfectly overlapped complementary clocks can be achieved by making the propagation delay from V_{CLK} to V_{in} similar as the propagation delay from V_{CLK} to $\overline{V_{in}}$. This was realized by designing two "fast" inverters to produce $\overline{V_{in}}$ and one "slow" inverter to produce V_{in}. This resulted in propagation delays of 1ns for both clocks paths. The total current consumption of the clock source and its buffers was 12.5µA from 1V supply.

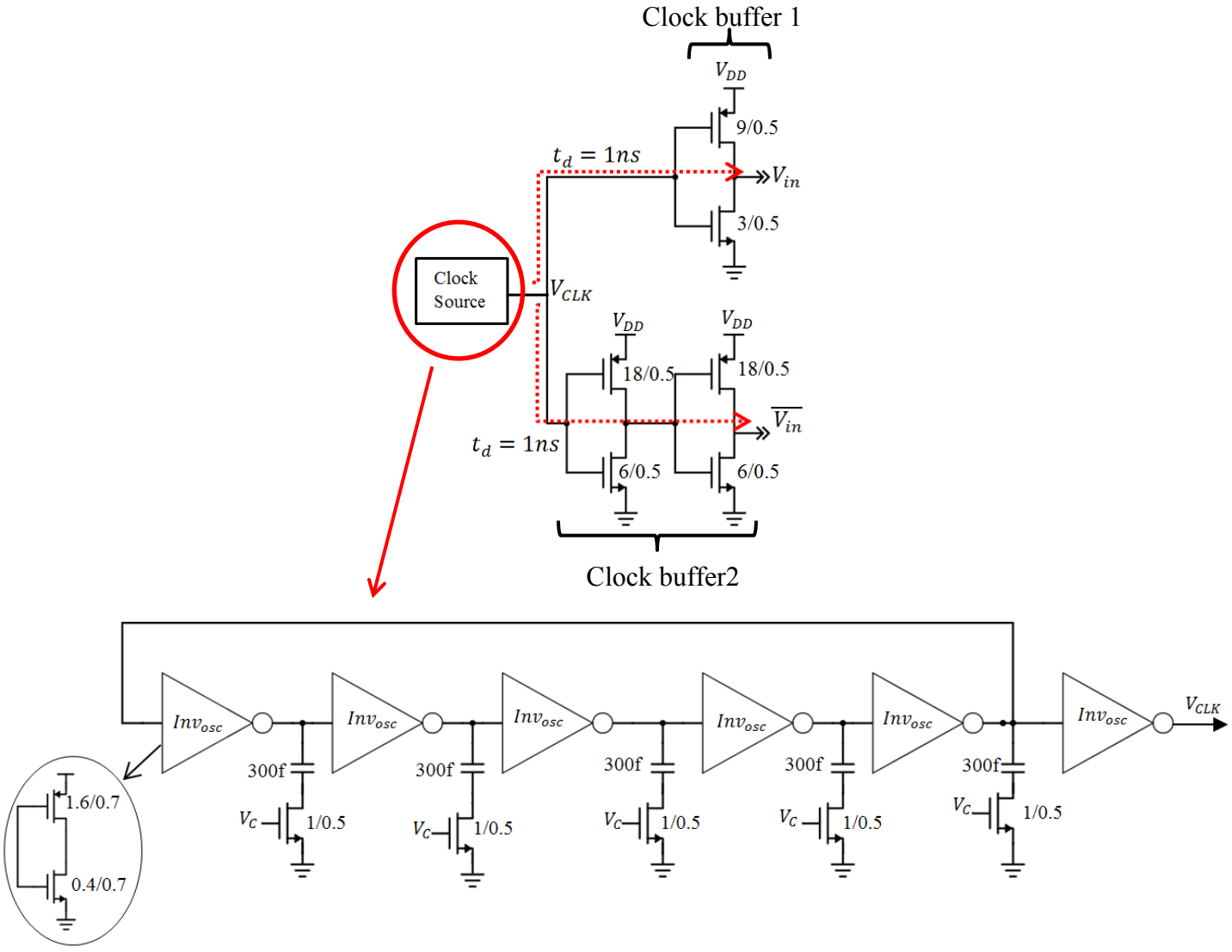


Fig. 3.21. Circuit schematic of the clock source and its buffers

3.5.3 Simulations

Different simulations are carried out in order to verify the theory developed in this work using Cadence environment in AMS 0.18µm technology. The first simulation carried out was to check what output voltage does the efficiency maximizes at. This was achieved by varying the output voltage by changing the pumping frequency from 5MHz to 45MHz and repeating the design procedure in Fig. 3.15 for each frequency of operation, in order to ensure similar performance across all the frequencies. The graphs obtained from simulations along with theory are plotted in Fig. 3.22 and Fig. 3.23.

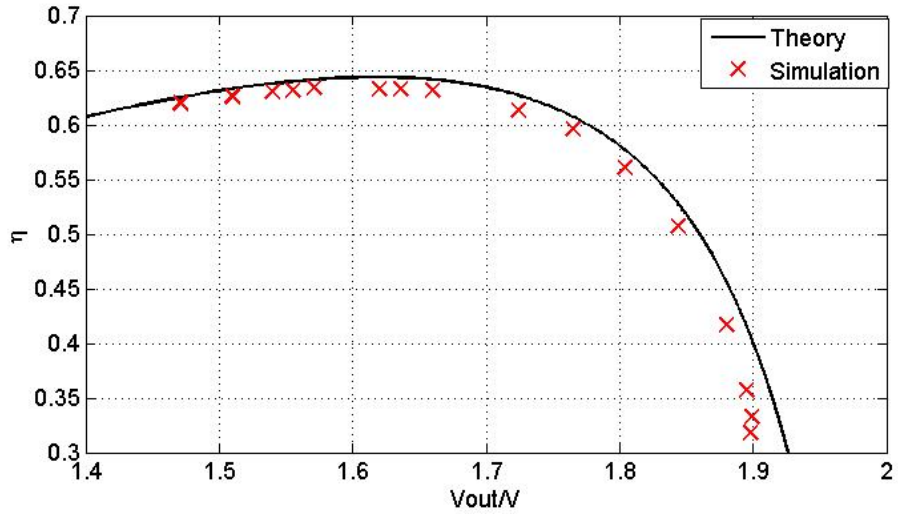
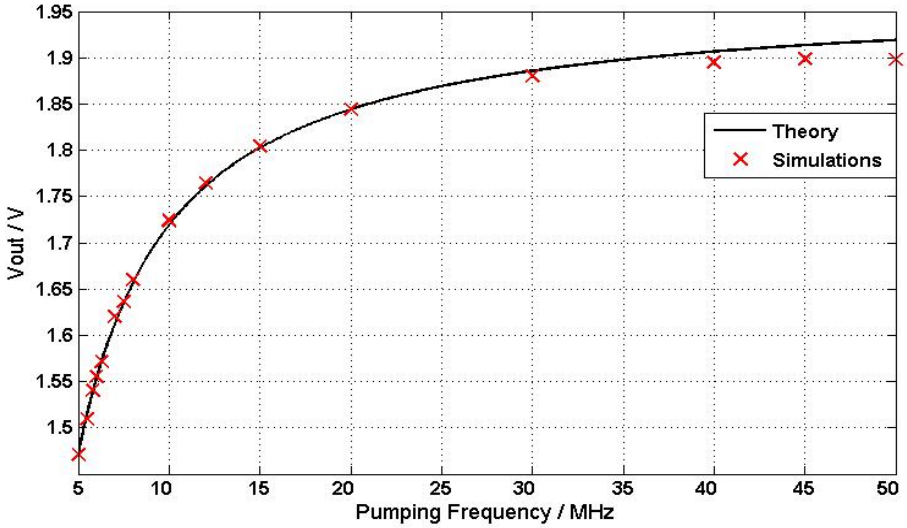


Fig. 3.22. Comparison between theory and simulations for the variation of the CP's efficiency with its output voltage



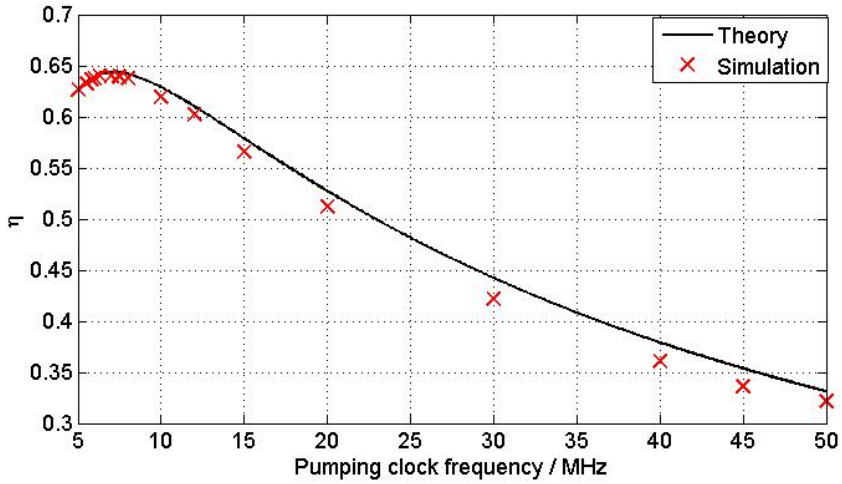


Fig. 3.23. Variation of the CP's efficiency and output voltage with frequency in theory and simulations

The value of the theoretical source resistance $(1/2fC)$, with the simulated source resistance is also plotted in Fig. 3.24.

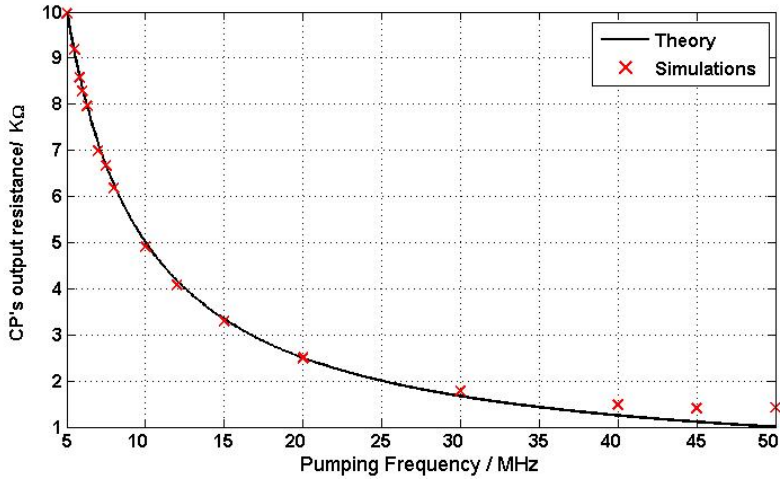


Fig. 3.24. CP's output resistance variation with pumping frequency

The efficiency in Fig. 3.22 maximizes at around 1.62V which is as predicted by (3.58). It can also be seen that at frequencies above 30MHz, the simulated results start to deviate from the theory. This is mainly because the size of the output PMOS switch has to decrease as well as T_{ON} which makes the value of $\frac{T_{ON}}{R_{ON}*C}$ become smaller than one, and leads to modulation of the CP's output resistance. However, this is not a problem as these frequencies are not the frequencies the

CP is designed to work with. They were just used in order to alter the output voltage and verify the theory.

Finally, the variation in efficiency of the CP with the size of the output PMOS switch was investigated. The pumping frequency was set at 7MHz and the pumping capacitor at 10pF. The length of the PMOS device was set to 0.2μm and the width was varied from 1μm to 50μm. For each width value the efficiency was measured. The resulting graph is shown in Fig. 3.25.

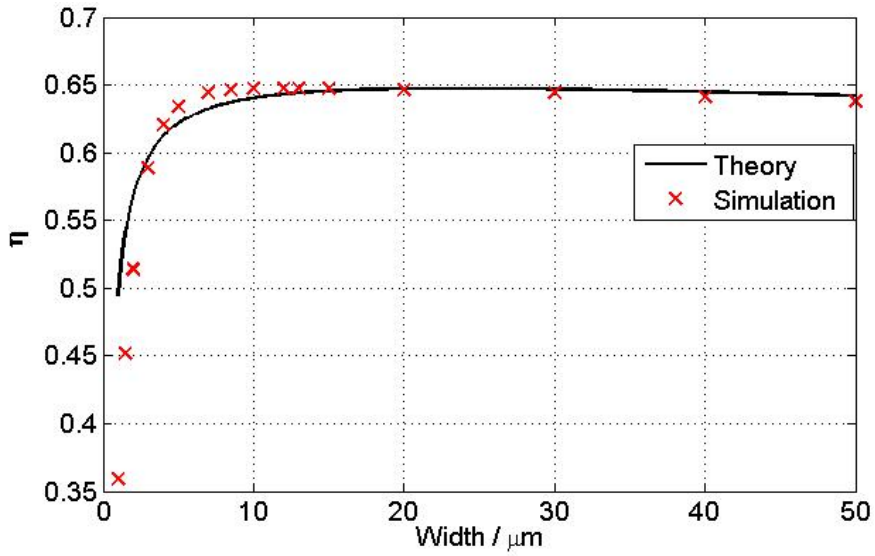


Fig. 3.25. Efficiency variation with the output PMOS width

The efficiency in simulation maximizes at a width of 10μm as opposed to the theoretical value of 28 μm, and that is where the minimum total power loss of the PMOS transistor occurs. The reason for this difference is the simplifications made in calculating the total parasitic capacitance, since some of the very small parasitics were neglected (such as drain/source body capacitances), and also the expressions of the PMOS parasitics themselves followed a linear approximation, whereas these capacitances are not linear. However, the variation in efficiency between the two consecutive width values is very small (<3% change). Therefore, even not having the optimum PMOS width would have little effect on efficiency for widths greater than one calculated by (3.41). In any case, equation (3.41) can be used as a starting point to set the width of the output PMOS switches, and then this can be slightly adjusted using the simulator to find a more exact value for which the maximum efficiency occurs at. The differences that can be seen in efficiency between the simulation and theory values for small transistors' widths are caused by the fact that

the theory was developed assuming that the resistance of the PMOS devices is small such that equation (3.33) is satisfied. This has got an effect in the calculated expressions as the widths are reduced because in this case equation (3.33) is no longer satisfied due to the increased value of R_{ON} with decreased transistor width.

Monte Carlo analysis was performed on the complete post-layout CP circuit including its clock source. Histograms that show the statistical distribution of the CP's output voltage and clock's frequency from 100 Monte Carlo runs are shown in Fig. 3.26.

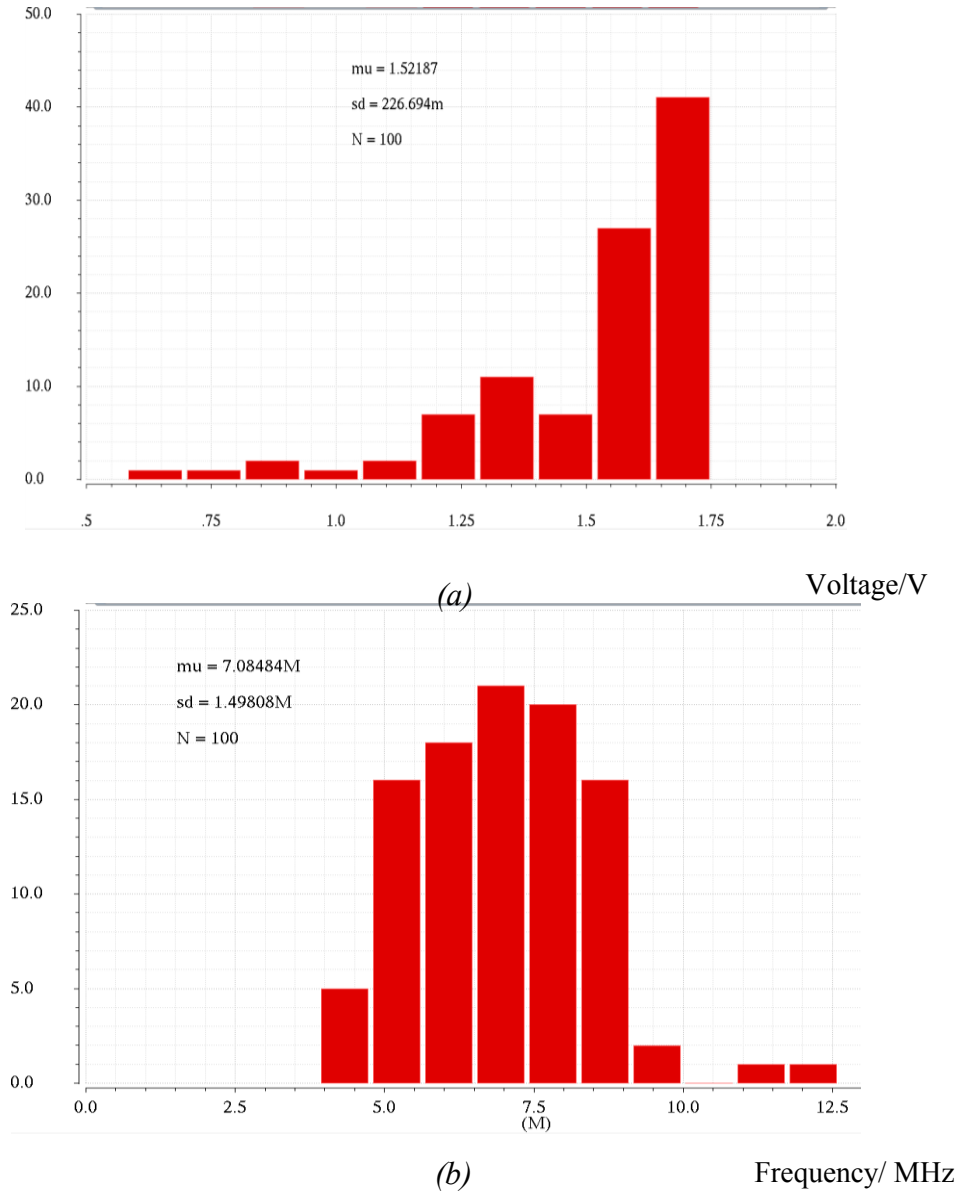


Fig. 3.26. Variations in (a) CP's output voltage and (b) clock's frequency in 100 simulation runs due to process variation and mismatch

The CP's output voltage has a voltage variation from 0.65V-1.75V with an average value of 1.52V. This large voltage variation is due to the clock's frequency, which varies from 4.5MHz – 12.5MHz and has an average frequency of 7MHz. The variation in clock's frequency is hard to control due to the ring oscillator topology used. This variation can be alleviated by tuning the control voltage V_c that controls the gates of the NMOS devices at the bottom of the capacitors in the ring oscillator as shown in Fig. 3.21. The control voltage V_c can be used to adjust the capacitance seen at the inverters' output in the ring oscillator and thus fix the clock's frequency to 7 MHz and compensate for the variations in the clock's frequency due to mismatch or process variation. This in turn sets the output voltage of the CP at 1.61V.

3.5.4 Measured results

The charge pump was powered directly from the chip's supply voltage. In order to create a 1V CP's supply from 1.2V supply, a 1.54 KΩ resistor was added between the chip's supply voltage and the CP's supply to create the voltage drop. The current that flows to the charge pump creates a voltage drop across the series resistor, lowering the supply voltage to 1V. The CP consumed a current of 140 µA at 1V supply and delivered a 1.58V output with a microphone load (50µA) connected. The efficiency was 56%. This efficiency is lower than the one predicted by theory in Fig.3.18 (60% when taking reversion loss into account). This could not be due to the parasitic capacitances added in the layout of the circuit because these were accounted for in simulations. It also could not be due to the PCB parasitics, as the internal nodes of the CP were all internally connected inside the chip and they have no connection to any PCB tracks. One possible reason for this is the slight timing mismatch in the complementary clocks that drive the CP. This results in complementary clocks that are not perfectly overlapping, which has an effect on the efficiency. The measured transient response of the charge pump is shown in Fig. 3.27.

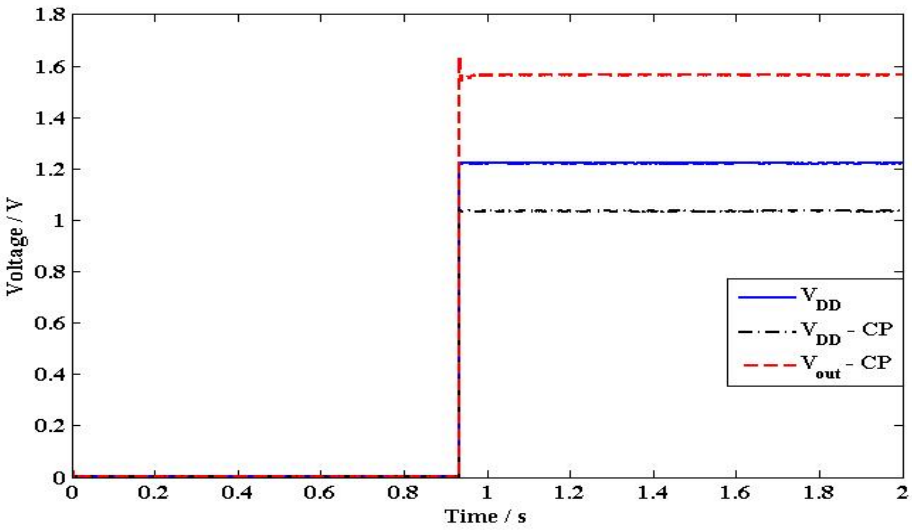


Fig. 3.27. Measured transient response of the CP's output

3.6 Conclusion

This chapter has reviewed different CP's topologies. The cross-coupled topology was chosen due to its suitability in this application. Its operation along with power losses incurred within it has been analyzed and an efficiency expression was derived. A design method has been introduced aiming to optimize the CP's efficiency for a certain set of parameters, while taking design area into consideration. A detailed mathematical analysis of reversion losses was introduced. The latter has shown that non-overlapping clock is not necessary in the application described here.

Based on the design methodology proposed in this chapter, a single stage cross-coupled CP to drive a microphone load was designed, simulated and experimentally verified. The CP shows a good performance, however the measured efficiency was lower than the simulation of the extracted circuit (7% lower). This can be attributed to the slight timing mismatch in the complementary clocks that drive the CP. Nonetheless, this 7% reduction in efficiency results in 10μA increase in the CP's current consumption, which is very little compared to the system's total current consumption.

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Chapter 4 : Analogue Front End

The Analogue front end (AFE) consists of an amplifier and a band-pass filter (BPF) that condition the input signal and make it suitable to be digitized by the ADC. The BPF has mainly three functions: reject high amplitude low frequency signals from the microphone that can saturate the amplifier, attenuate heart signals, remove out of band noise and prevent aliasing. The amplifier's function is to map the full range input signal to the ADC's full input range. This makes sure that weak signals get detected by the ADC and their SNR gets maximised. The main important design specifications of the AFE are: noise, distortion, linearity and power consumption. Linearity refers to the variation of the AFE's cut-off frequency with respect to the input voltage. The more linear the system is, the less variation it exhibits.

There are many trade-offs between different design specifications of the AFE. The trade-offs between the power consumption and other design specifications are not going to be considered. This is because the AFE consumes a very small percentage of the total power in a mixed signal system where there are charge pumps, digital and RF circuits. Therefore, the power consumption of the AFE can be slightly adjusted to meet other design specifications. One of the main design trade-offs is the one between linearity and noise of the AFE. In order to understand how this trade-off arises, a system with cascaded blocks as shown in Fig. 4.1 can be considered.

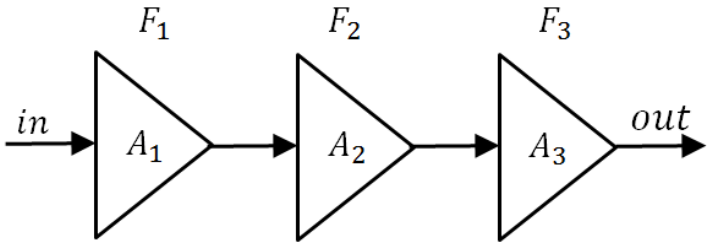


Fig. 4.1. A general diagram showing a cascade of blocks that forms a signal chain

The total noise figure of the system (F_{sys}) can be written using the Friis cascaded noise formula [1]:

$$F_{sys} = F_1 + \frac{F_2 - 1}{A_1} + \frac{F_3 - 1}{A_1 A_2} \tag{4.1}$$

Where A_n and F_n are the N^{th} block gain and noise factor respectively . The noise factor of the system can be understood as a measure of how much noise the system adds to the input signal and hence ideally it should be minimized. By looking at equation (4.1), the gain of the first stage (A_1) must be as large as possible to minimize the noise factor of the system. Hence, it is best to firstly amplify the input signal to the full scale of the ADC's input range before filtering it. However, this requires the operational transconductances amplifiers (OTAs) inside the filters to be linearized to the full scale of the ADC's input range, which is a challenging task especially when the transistors inside the OTAs are biased in the sub-threshold region. Because of this a noise and linearity trade-off has to be found.

Before deciding on how much linearity is required by the OTAs, it is useful first to estimate the noise budget of the AFE. This is defined as how much noise the AFE can add before degrading the noise performance of the whole system. The system is formed by the AFE followed by an ADC. The ADC has its own noise, which is dominated by the quantization noise. Therefore, the noise introduced from the AFE should be sufficiently low so that the total noise performance is not degraded due to the AFE. The total noise of the AFE and the ADC are independent and therefore the SNR of the total system can be derived as:

$$SNR_{total} = -10log\left(10^{-\left(\frac{SNR_{AFE}}{10}\right)} + 10^{-\left(\frac{SNR_{ADC}}{10}\right)}\right) \tag{4.2}$$

Another useful metric that should be taken into account is the *effective number of bits* (ENOB) of the system. This is a measure of the dynamic range of the whole system including the AFE and the ADC. The ENOB is defined mathematically as [2]:

$$ENOB_{total} = \frac{SNR_{total} - 1.76}{6.02} \tag{4.3}$$

The effective number of bits of the system should be at least 7-bits for the algorithms to work as explained in Chapter 2 Section 2.3.1.5. Therefore, the minimum required SNR of the system (SNR_{total}) can be calculated using equation (4.3) to be (6.02×7)+1.76 ≈ 44dB.

The SNR of the ADC (SNR_{ADC}) can be derived as:

$$SNR_{ADC} = 20log\left(\frac{V_{ref}}{2\sqrt{2}}\Big/\frac{LSB}{\sqrt{12}}\right) = 20log\left(\sqrt{3} \times 2^{(n-0.5)}\right) \quad (4.4)$$

Where V_{ref} is the reference voltage of the ADC and n is the number of bits. The ADC was originally designed to be 12-bits, but only 8-bits were used in this design (the most significant ones). As a consequence, its SNR is very close to the theoretical 50dB SNR for 8-bits ADCs because the harmonic distortion and other non-idealities will be manifested in the least significant 4-bits. Substituting the values of SNR_{ADC} as 50dB and SNR_{total} as 44dB in equation (4.2) and solving it for SNR_{AFE} yields the minimum SNR of the AFE to be 45.3dB. To achieve this minimum SNR value, the maximum input referred RMS noise must be less than $130\mu V_{RMS}$ for a 66mV peak-peak full-scale input. The amplifier was therefore split into two stages, one before and one after filtering, with a gain of two and five, respectively, as shown in Fig. 4.2.

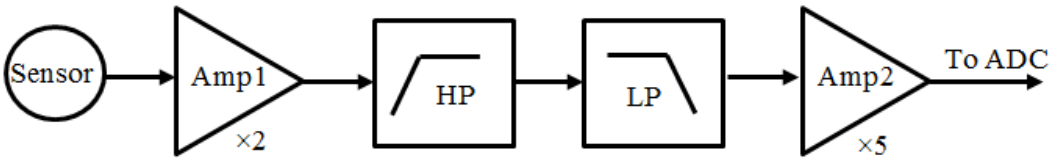


Fig. 4.2. Detailed breakdown of the AFE

The gain of the first amplifier stage was chosen to achieve an input referred noise for the AFE less than $60\mu V_{RMS}$, while maintaining better than 95% transconductance linearity for full scale input. The 95% transconductor linearity will decrease the corner frequency of the filters (low and high corners) by 5% when the maximum input is applied. This is tolerable in this application and will not degrade the performance of the system because the later was slightly overdesigned to compensate for some variations.

4.1. Filter

Given the low power requirements, the low cut-off frequency specification, and the limited value of the capacitors and resistors that can be used on chip, OTA-C filters come naturally as the most suitable choice for such requirements [3]. OTA-C filters are simple to implement yet very effective for biomedical low frequency applications [3]. The cut-off frequency of OTA-C filters is dependent on the transconductance (g_m) of the OTA cell, which can be set by the bias current of the OTA. To achieve a cut-off frequency in the range of hundreds of Hertz, time

constants in the range hundreds of microseconds are required. The maximum values of capacitors that can be used on chip, due to area constraints, are in the range of hundreds of picofarads. This means that the only way to achieve these time constant is by having a g_m in the order of 10's-100's of nanosiemens. This can be achieved by biasing the transistors inside the Gm-cell in weak inversion with nanoamps current.

The band-pass filter (BPF) was created by cascading a high-pass and low-pass section. Both sections were realized using OTA-C biquadratic implementations. The biquadratic implementation is more sensitive to components variations compared to LC ladders [4]. However the former is easier to synthesize and requires less overall design area. The effect of filter parameters sensitivity can be alleviated by adjusting the bias current of the transconductors after chip fabrication.

4.1.1 High-pass filter

The high-pass filter (HPF) has two main functions: remove the high amplitude low frequency signals that come from the microphone's output to prevent undesired saturation of the amplifier; and attenuate the strong heart signals that can saturate the ADC. It was shown in Chapter 2, Section 2.3.1, that a second order HPF's with cut-off frequency at 140 Hz is required in this design. The HPF transfer function was implemented as a 2nd order Butterworth filter with a cut-off frequency of 140Hz. The mathematical transfer function of such filter was derived using the 2nd order Butterworth polynomial for a low-pass transfer function, and then performing a low-pass to high-pass transformation:

$$H_{HP}(S) = \frac{(1.29 \times 10^{-6})s^2}{(1.29 \times 10^{-6})s^2 + (1.6 \times 10^{-3})s + 1} \tag{4.5}$$

The transfer function (4.5) was realised using a biquadratic OTA-C topology as shown in Fig. 4.3 [5]:

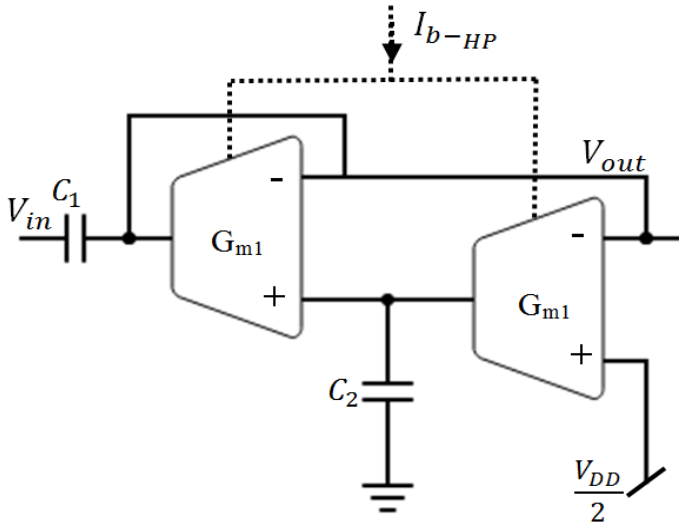


Fig. 4.3. Biquadratic OTA-C implementation of the HPF

The transfer function of the HPF in Fig. 4.3 can be written as (assuming equal transconductors) as:

$$H_{HP}(S) = \frac{\frac{C_1 C_2}{G_{m1}{}^2} s^2}{\frac{C_1 C_2}{G_{m1}{}^2} s^2 + \frac{C_2}{G_{m1}} s + 1} \tag{4.6}$$

By setting the values of $G_{m1} = 12.5nS$, $C_1 = 10pF$ and $C_2 = 20pF$, the transfer function (4.6) reduces to (4.5). This requires the biasing current of the HP (I_{b-HP}) to be set at 3nA. The voltage $V_{DD}/2$ sets the DC level at the output. This is the biasing voltage/common mode (CM) level of the following low pass filter stage.

4.1.2 Low-pass filter

The low pass performs an antialiasing function before digitizing the data via the ADC. As shown in Chapter 2, Section 2.3.1, a 3rd order Butterworth lowpass filter with 1.3KHz cut-off frequency is required to attenuate frequencies greater than 9KHz below the DR of the signal (50dB). The mathematical transfer function of a 3rd order Butterworth low pass filter with a 1.3 KHz cut-off frequency was derived as follows: from the filter table; the normalized factorized 3rd order Butterworth polynomial is obtained as:

$$H_{Norm}(S) = \frac{1}{(S+1)(S^2+S+1)} \tag{4.7}$$

Equation (4.7) was then de-normalized by substituting the term "s" in (4.7) with "s/ω_c", with term ω_c being defined as [5]:

$$\omega_c = 2\pi f_p\left(10^{\alpha_p/10} - 1\right)^{-1/2N} \tag{4.8}$$

where f_p is the frequency where a gain decrease of α_p(dB) below the pass band occurs and N is the filter order. These terms are illustrated graphically in Fig. 4.4. Substituting f_p as 1KHz, $\alpha_p = 1dB$ and N=3 gives $\omega_c = 7870.2$ rad/sec.

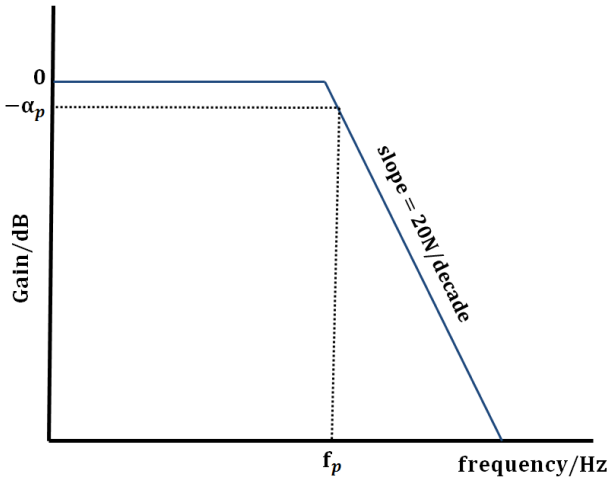


Fig. 4.4. Bode diagram explaining the terms in equation (4.8)

After de-normalization, the LPF transfer function becomes:

$$H_{LP}(s) = \frac{1}{(1.27\times10^{-4}\,s+1)(1.614\times10^{-8}\,s^2+1.27\times10^{-4}\,s+1)}$$
$$= \frac{1}{(2.05\times10^{-12})s^3+(3.23\times10^{-8})s^2+(2.54\times10^{-4})s+1} \tag{4.9}$$

Equation (4.9) was implemented using an OTA-C single stage filter followed by biquadratic section as shown in Fig. 4.5 [5]:

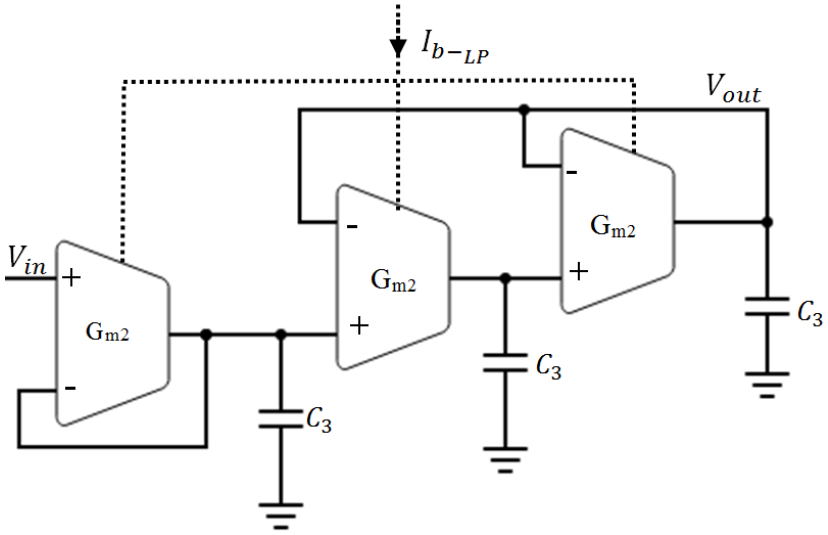


Fig. 4.5. OTA-C implementation of the LPF

For equal transconductances and capacitors, the transfer function of the LPF in Fig. 4.5 can be written as:

$$H_{LP}(s) = \frac{1}{\left(\frac{C_3}{G_{m2}}\right)^3 s^3 + 2\left(\frac{C_3}{G_{m2}}\right)^2 s^2 + 2\left(\frac{C_3}{G_{m2}}\right) s + 1} \tag{4.10}$$

Setting the values of $G_{m2} = 78.7\,nS$ and $C_3 = 10pF$, equation (4.10) reduces to (4.9). This requires the total biasing current of the LPF $\left(I_{b-LP}\right)$ to be set at 30nA.

The final band-pass filter transfer function is computed as:

$$H_{BP}(s) = H_{HP}(s) \times H_{LP}(s)$$

$$= \frac{N_2 s^2}{D_5 s^5 + D_4 s^4 + D_3 s^3 + D_2\, s^2 + D_1 s + 1} \tag{4.11}$$

where $D_5 = \left(\frac{2C^5}{{G_{m1}}^2 {G_{m2}}^3}\right)$, $D_4 = \left(\frac{4C^4}{{G_{m1}}^2 {G_{m2}}^2} + \frac{C^4}{G_{m1} {G_{m2}}^3}\right)$, $D_3 = \left(\frac{4C^3}{{G_{m1}}^2 G_{m2}} + \frac{4C^3}{G_{m1} {G_{m2}}^2} + \frac{C^3}{{G_{m2}}^3}\right)$

$D_2 = \left(\frac{2C^2}{{G_{m1}}^2} + \frac{4C^2}{G_{m1} G_{m2}} + \frac{2C^2}{{G_{m2}}^2}\right)$, $D_1 = \left(\frac{C}{G_{m1}} + \frac{C}{G_{m2}}\right)$ and $N_2 = \frac{2C^2}{{G_{m1}}^2}$

$C = 10pF$, $G_{m1} = 12.5\,nS$ and $G_{m2} = 78.7\,nS$.

4.1.3 Transconductor (OTA) cell

The OTA is the building block of the filters and thus its functionality imposes the main limits in the latter's performance. The OTA is a voltage to current convertor that generates an output current proportional to the voltage difference between its inputs. The OTA in this work was implemented as a single stage differential transconductor amplifier as shown in Fig. 4.6.

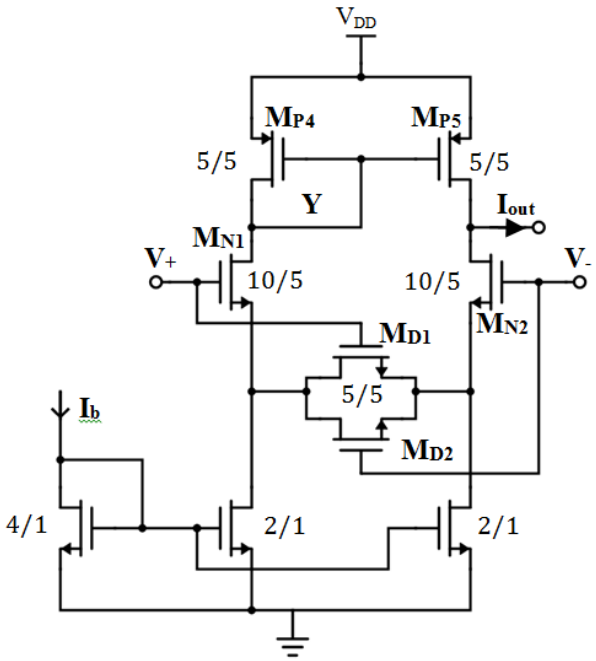


Fig. 4.6: OTA's schematic

This topology is inherently stable without the need of a compensation capacitor. It has very low current consumption and is very suitable for applications where the required bandwidth is up to 10KHz. One issue with the simple one-stage OTA is its small linearity range. The g_m of the OTA will change with the differential input voltage. This can cause problems because a change in the g_m value will translate to a change in the filter's cut-off frequency. For the OTA in Fig. 4.6, writing $V_+ = V_{CM} + \frac{v_d}{2}$ and $V_- = V_{CM} - \frac{v_d}{2}$, where V_{CM} is the common mode DC voltage of the OTA input and v_d is the differential small signal input, the output differential current of the OTA can be derived as [6]:

$$I_{Out} = I_b \times \tanh\left(\frac{v_d}{nV_T}\right) \tag{4.12}$$

And the transconductance in weak inversion is derived as:

$$g_m = \frac{\partial I_{Out}}{\partial v_d} = \frac{I_b}{nV_T} \times \left[1 - tanh^2\left(\frac{v_d}{nV_T}\right)\right] \tag{4.13}$$

where V_T is the thermal voltage and n is the slope factor.

Defining the term g_{m0} as the transconductance at zero differential input voltage, the ratio of g_m/g_{m0} is written as:

$$\frac{g_m}{g_{m0}} = \left[1 - tanh^2\left(\frac{v_d}{nV_T}\right)\right] \tag{4.14}$$

A plot of g_m/g_{m0} versus v_d for V_T=26mV and $n = 1.3$ is in Fig. 4.7.

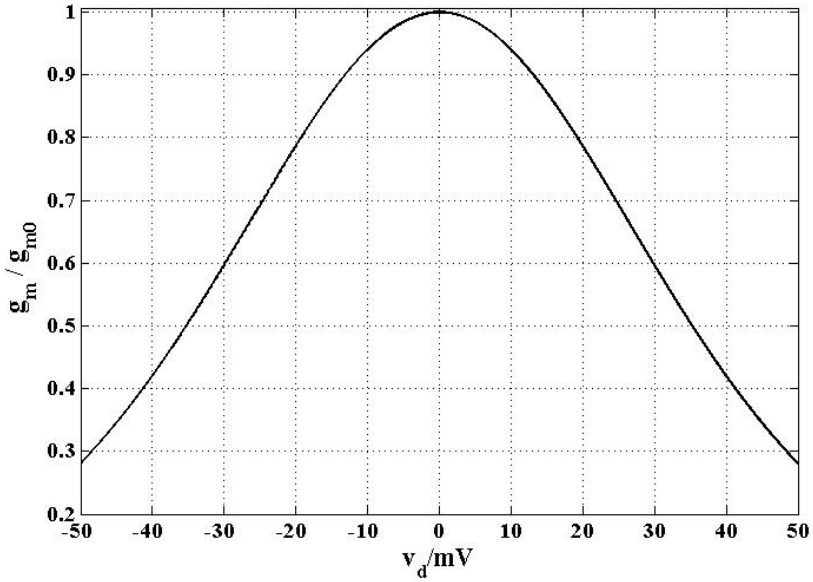


Fig. 4.7. Plot of the ratio g_m/g_{m0} versus v_d for V_T=26mV and n=1.3

Fig. 4.7 shows how the value of g_m is a highly non-linear function of the differential input voltage v_d. A 7% and 20% reduction in the value of g_m occurs at 10mV and 20mV differential input voltages respectively. The non-linearity arises from the $tanh^2$ function in equation (4.13). The OTA must be linearized to an acceptable voltage range before it can be used in the filter. The idea behind the linearization of the OTA is to modify the basic circuit in a way such that

some extra terms are added to equation (4.13). These mathematical terms will reduce the effect of the $tanh^2$ function.

Several methods have been found in the literature to increase the linear range of OTA [6-14]. Bulk driven technique was reported in [7] where the input is applied to the bulk of input transistor instead of the gate. This method might show a good results in simulations; however it is risky and carries a high chance of failure in a real world circuit because the simulator is not very accurate in modelling the bulk terminal behavior.

Another method reported in [8] was used to linearize bipolar transistors by using an asymmetric double differential pair. This method changes the shape of the transconductance graph and flattens it out by stretching its peak over a wider range of differential input voltages. It can be used for weak-inversion MOS transistors as they have exponential current-voltage relation just same as bipolar transistors.

Capacitive attenuation was proposed in [9]. In this method input differential voltage is attenuated by a capacitive divider and, after processing of the attenuated signal by the filter, the original signal level was restored by a negative feedback amplifier with capacitive feedback network. A capacitive divider was used instead of a resistive one to minimize the added noise. This method requires extra capacitors and can change the response of the filter topology due to the extra poles created by the capacitors. Therefore it was not used.

Source degeneration via MOS connected diodes at the expense of decrease of input dynamic range was reported in [10]. Source degeneration via single diffuser and double symmetric diffusers are reported in [11] and [12] respectively. They were originally used to linearize the transconductor in the strong inversion and they were analyzed in [13] for transconductance operating in the weak inversion region. Lastly, combinations of different methods have been reported in [14, 15].

The asymmetric differential pair and the source degeneration via single and double diffusers are good candidates for OTA linearization for on-chip implementation and have been proven to work in real circuits. The experiments and comparisons done in [13] show that the source degeneration via single diffuser technique improves the OTA's linearity more than the double symmetric diffuser or the double asymmetric differential pair methods. However it requires an extra common mode circuit to function properly. The same publication has also showed that the double asymmetric differential pair and the double diffuser techniques both improve the linearity

by equal amounts. Therefore, the double diffuser technique was used in this work due to its simpler implementation, compared to the asymmetric differential pair technique.

The final OTA schematic is shown in Fig. 4.6. Transistors M_{D1} and M_{D2} implement the symmetric diffuser. Analysis of the OTA with double symmetric diffuser reveals that the differential output current gets modified to [13]:

$$I_{Out_lin} = I_b \times \tanh\left(\frac{v_d}{nV_T} - tanh^{-1}\left[\frac{1}{4m+1}tanh\left(\frac{v_d}{nV_T}\right)\right]\right) \tag{4.15}$$

where m is the ratio of dimensions of M_{D1} to M_{N1} (or M_{D2} to M_{N2}): $m = \frac{(W/L)_{M_{D1}}}{(W/L)_{M_{N1}}}$.

The new transconductance expression is the derivative of equation (4.15) with respect to v_d. This expression was not found in the literature and hence it was derived here. Some approximations and simplification were applied to simplify its derivation. The $tanh^{-1}$ function in equation (4.15) can be expanded using Taylor series as:

$$tanh^{-1}\left[\frac{1}{4m+1}tanh\left(\frac{v_d}{nV_T}\right)\right] = \frac{1}{4m+1}\ tanh\left(\frac{v_d}{nV_T}\right) + \frac{1}{3(4m+1)^3}\ tanh^3\left(\frac{v_d}{nV_T}\right) + \frac{1}{5(4m+1)^5}\ tanh^5\left(\frac{v_d}{nV_T}\right) + \cdots \tag{4.16}$$

Equation (4.16) can be approximated as:

$$tanh^{-1}\left[\frac{1}{4m+1}tanh\left(\frac{v_d}{nV_T}\right)\right] \approx \frac{1}{4m+1}\ tanh\left(\frac{v_d}{nV_T}\right) \tag{4.17}$$

This simplification holds true if and only if $\frac{1}{4m+1} > \frac{10}{3(4m+1)^3}$, which leads to the following condition on the variable m:

$$m > 0.2 \tag{4.18}$$

Substituting back (4.17) in (4.15) to get a simplified expression of the output current:

$$I_{Out_lin} = I_b \times \tanh\left(\frac{v_d}{nV_T} - \frac{1}{4m+1}\ tanh\left(\frac{v_d}{nV_T}\right)\right) \tag{4.19}$$

This simplification has led to a simpler expression to differentiate, yet it is accurate, as long as condition (4.18) is maintained. The linearized g_{m_lin} expression can now be derived as:

$$g_{m_lin} = \frac{\partial I_{Out_lin}}{\partial v_d}$$

$$= I_b \frac{1}{nV_T}\left[1 - \tanh^2\left(\frac{1}{nV_T}v_d - \frac{1}{4m+1}\tanh\left(\frac{v_d}{nV_T}\right)\right)\right] \times \left[1 - \frac{1}{4m+1}\left(1 - \tanh^2\left(\frac{v_d}{nV_T}\right)\right)\right]$$

$$= I_b \frac{1}{nV_T} \times \operatorname{sech}^2\left[\frac{1}{nV_T}v_d - \frac{1}{4m+1}\tanh\left(\frac{v_d}{nV_T}\right)\right] \times \left[1 - \frac{1}{4m+1}\operatorname{sech}^2\left(\frac{v_d}{nV_T}\right)\right] \quad (4.20)$$

The nominal value of the transconductance at zero differential voltage $\left(g_{m0_lin}\right)$ is calculated by susbstititung $v_d = 0$ in equation (4.20), which results in:

$$g_{m0_lin} = \frac{I_b}{nV_T}\left(\frac{m}{m+0.25}\right) \quad (4.21)$$

The linearization of the OTA results in a decrease in its g_m value by a factor of $\frac{m}{m+0.25}$. This can be accounted for when setting the OTA's biasing current.

The new ratio of g_{m_lin}/g_{m0_lin} becomes:

$$\frac{g_{m_lin}}{g_{m0_lin}} = \operatorname{sech}^2\left[\frac{1}{nV_T}v_d - \frac{1}{4m+1}\tanh\left(\frac{v_d}{nV_T}\right)\right] \times \left[1 - \frac{1}{4m+1}\operatorname{sech}^2\left(\frac{v_d}{nV_T}\right)\right] \times \left[\frac{m+0.25}{m}\right] \quad (4.22)$$

At first sight, it is unclear how equation (4.22) exhibits a more linear behavior than equation (4.14). This can be made more clear by plotting the individual terms that make up this equation. Defining the terms as follows:

$$A = \operatorname{sech}^2\left[\frac{1}{nV_T}v_d - \frac{1}{4m+1}\tanh\left(\frac{v_d}{nV_T}\right)\right] \;\&\; B = \left[1 - \frac{1}{4m+1}\operatorname{sech}^2\left(\frac{v_d}{nV_T}\right)\right]$$

and plotting them against the differential input voltage for *m*=0.5, as shown in Fig. 4.8:

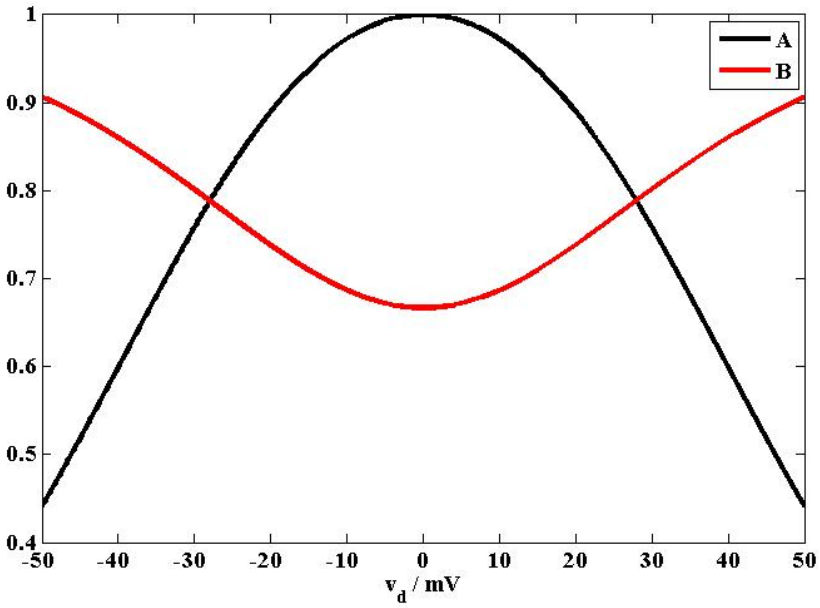


Fig. 4.8. Plot of the terms A and B in equation (3.22) against v_d for m=0.5

It can be noticed that term *A* is a typical g_m graph against the differential input voltage with concave down shape centered at $v_d = 0$ and then rolls down. However, the term *B* has the opposite shape of *A*. It has a concave up shape centered at $v_d = 0$ and then rolls up. When the terms *A* and *B* get multiplied together, the term *B* reduces the roll off rate of *A,* like a counter effect, and the product will have a flatter shape. This is effectively a more linear g_m. The term $\frac{m+0.25}{m}$ in equation (4.22) restores the peak value at 1 after multiplication.

The value of *m* that maximizes the linear range must be selected. This was determined graphically. A plot of equation (4.22) for different values of m using Matlab is shown in Fig. 4.9. This figure shows how smaller linearity range is achieved for larger values of *m* (for larger dimension of M_{D1} and M_{D2}). The maximum flat linearity is achieved when the value of *m* is 0.5. For smaller values of *m*, the traconductance starts exhibiting ripple. Therefore, M_{D1} and M_{D2} were made half the size of the transistors' in the input differential pair, as shown in the OTA schematic in Fig. 4.6.

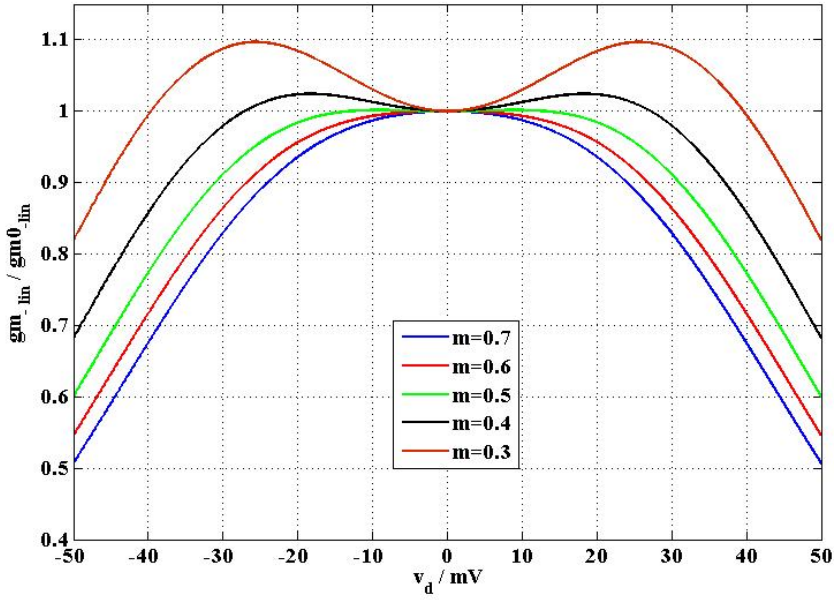


Fig. 4.9. Ratio of linearized g_m over the nominal one versus v_d for different values of m

Circuit simulations in Cadence environment were carried out to verify the OTA's linear range after the circuit modifications. A plot that compares the linearity of the simple OTA and the linearized one is shown Fig. 4.10. The simple OTA's simulated linearity is represented by the cross marks and the modified OTA's simulated linearity is represented by the circles.

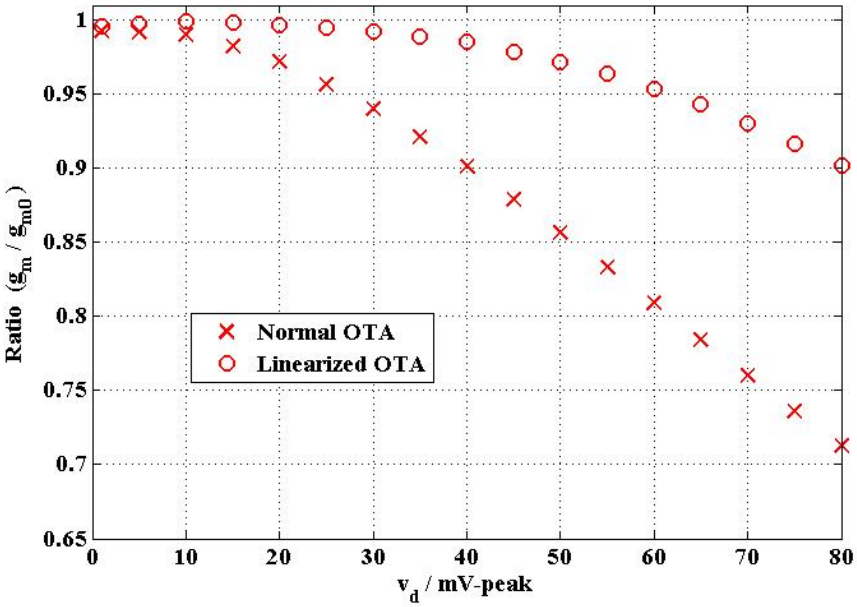


Fig. 4.10. Simulations of the OTA's linear range before and after linearization (m=0.5)

Fig. 4.10 shows a significant increase in the OTA's linearity after linearization. A linearity better than 95% is achieved at 60mV peak input differential voltage. Note that the simulated linearity range is greater than the theoretical one predicted by equations (4.14) and (4.22) and displayed in Fig 4.7 and Fig. 4.9, respectively. This is due to a number of reasons. One of the reasons is that the slope factor *n* gets modulated with the gate voltage [16] and this was not taken into account by the theoretical equations. The other factor could be the simple weak-inversion formula used that does not consider the inversion level of the devices and just simply assumes that they are in deep weak inversion. Nonetheless, this did not have any effect on the design of the OTA, as the simulator was ultimately used to asses and examine the OTA's behavior rather than depending solely on simplified theoretical models.

So far in the text, the OTA was assumed to have an infinite bandwidth (i.e. with no poles or zeroes). However, this is not the case, since OTA's are bandwidth limited. The g_m of the OTA cell will decrease with frequency due to internal poles. The poles of the OTA cell will affect the transfer function of the filter and might increase the likelihood of oscillation. Hence, the effect of the OTA's poles on the filter transfer function had to be investigated. The OTA's transfer function can be modelled with a single pole and zero as follows [17]:

$$G_m = g_{m0} \frac{1 + \frac{s}{2\omega_{Gm}}}{1 + \frac{s}{\omega_{Gm}}} \tag{4.23}$$

where g_{m0} is the nominal transconductance at low frequency and ω_{Gm} is the OTA's pole frequency.

The OTA's pole ω_{Gm} was derived in [17] as:

$$\omega_{Gm} = \sqrt{2}\, \frac{g_{m4}}{C_y} \tag{4.24}$$

where g_{m4} is the transconducatnce of transistor M_{P4} in Fig. 4.6, and C_y is the parasitic capacitance to ground connected at node Y in Fig. 4.6. This can be approximated as:

$$C_y = C_{gb4} + C_{gb5} + C_{gs4} + C_{gs5} \tag{4.25}$$

All the transistors in the OTA are in saturation weak inversion region and therefore the gate-source parasitic capacitances are much smaller than gate-body capacitances, and thus can be ignored. The dimensions of M_{P4} and M_{P5} are the same. Therefore, expression (4.25) can be written as:

$$C_y \approx C_{gb4} + C_{gb5} = 2\frac{n-1}{n} \times W_4 \times L_4 \times C_{ox} \tag{4.26}$$

Where W_4 and L_4 are the width and length of M_{P4} in Fig. 4.6, n is the slope factor and C_{ox} is the oxide capacitance per unit area. Substituting the AMS 0.18µm technology design parameters (n=1.3 and$C_{ox} = 8.5fF/\mu m^2$) and the dimensions of M_{P4} (5µ×5µ) in expression (4.26) gives the value of $C_y = 98fF$.

Two OTAs were used in the band-pass filter. The first OTA (G_{m1}) was used to synthesize the HPF and the second OTA (G_{m2}) was used to synthesize the LPF. These two OTAs have the same device dimensions and therefore C_y is the same for both. However, they are biased with two different currents which results in different values of g_{m4}. The values of $g_{m4_1}$and g_{m4_2} were measured to be 14.9nS and 73.2nS respectively, where g_{m4_n} is the transconducatnce of transistor M_{P4} in the n^{th} OTA. This places their pole frequency (f_{Gm1} and f_{Gm2}) at 34.2KHz and 168.1KHz respectively. The OTAs transfer functions can be then written as:

$$G_{m1} = (1.25 \times 10^{-8}) \times \frac{1 + (2.33 \times 10^{-6})s}{1 + (4.66 \times 10^{-6})s} \tag{4.27}$$

$$G_{m2} = (7.87 \times 10^{-8}) \times \frac{1 + (4.73 \times 10^{-7})s}{1 + (9.46 \times 10^{-7})s} \tag{4.28}$$

Equations (4.27) and (4.28) were substituted in the BPF's transfer function (4.11) using MATLAB to see the effect of the limited bandwidth of the OTA. A Bode plot that compares the ideal BPF transfer function with the real one is shown in Fig. 4.11. The ideal BPF transfer function is shown in solid blue line and the real one with red broken lines. As can be seen in the figure, the poles of the OTA did not cause any major variations in the BPF transfer function, except a higher roll off rate at frequency around 110KHz. This is expected because the OTA poles are at frequency much higher than the BPF cut-off frequency. The increase in the roll-off rate at a frequency of 110KHz is caused by the roll-off of G_{m2}, which occurs at a 168.1KHz.

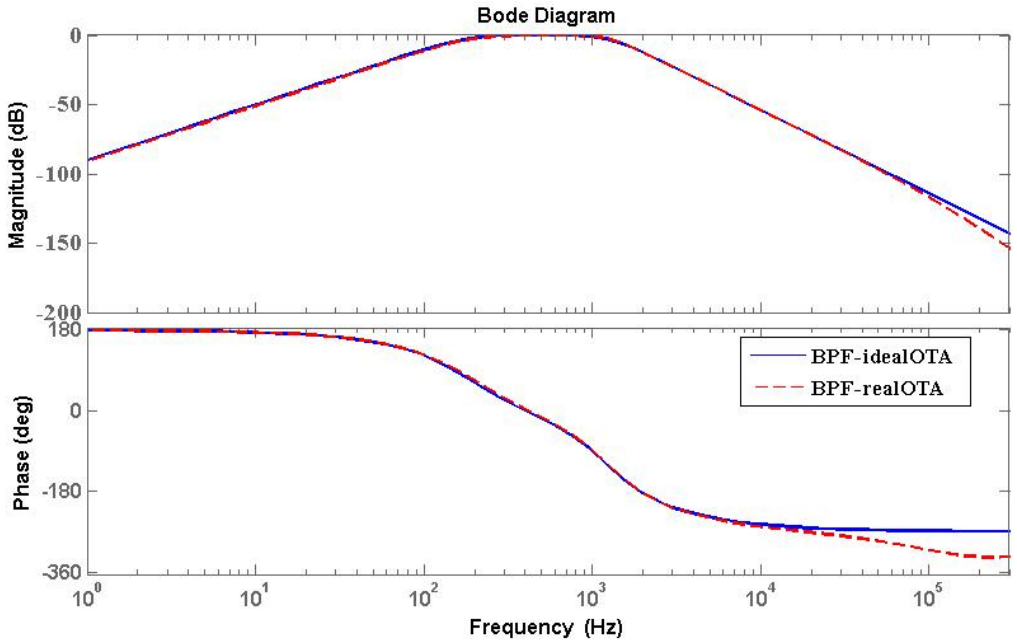


Fig. 4.11. Comparison between the transfer functions of the ideal BPF synthesized with ideal OTA with the ones synthesized with real OTA with poles and zeroes

4.2. Amplifier

The amplifier was implemented as an inverting negative feedback amplifier as shown in Fig. 4.12. The feedback loop was set via capacitors instead of resistors to reduce the noise introduced by the amplifier. The pseudo resistor was used to set the DC operating point at the Opamp terminals.

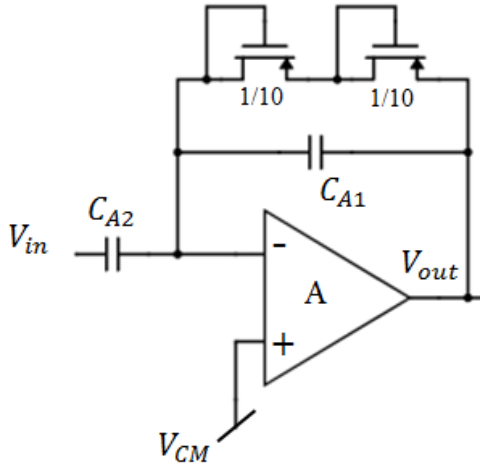


Fig. 4.12. Amplifier schematic

The mid-band gain of the amplifier is set via the capacitive ratio of C_{A2}/C_{A1}. The amplifier's transfer function contains two poles and has the shape of a band-pass response. The first pole location gives the high-pass response. Its frequency (ω_L) is dependent on the capacitor C_{A1} and the resistance of the pseudo- resistor. More specifically it is given as [18]:

$$\omega_L = 1/C_{A1}r_{pesudo} \tag{4.29}$$

where r_{pesudo} is the equivalent resistance of the pseudo-resistor. This cut-off frequency is two orders of magnitudes lower than the cut-off frequency of the succeeding high pass filter stage and thus it is ignored. The other pole location is responsible for a low-pass response. The frequency of this pole is known as the high cut-off frequency (ω_H), which was found to be at a frequency about 1.8 orders of magnitudes greater than the cut-off frequency of the low pass filter (63 times bigger). Hence it is ignored for the purposes of derivations as well. The only effect this pole has is that it increases the roll-off rate of the AFE's overall frequency response at 60KHz.

The Opamp was implemented as a 2-stage Miller amplifier with an open loop gain of 73dB and gain bandwidth (GBW) of 200KHz, using 3µA tail current. The Opamp was designed using the design procedure in [19] and the simulator was then used for final tuning. Its circuit schematic and open loop simulations are shown in Fig. 4.13 and Fig. 4.14 respectively.

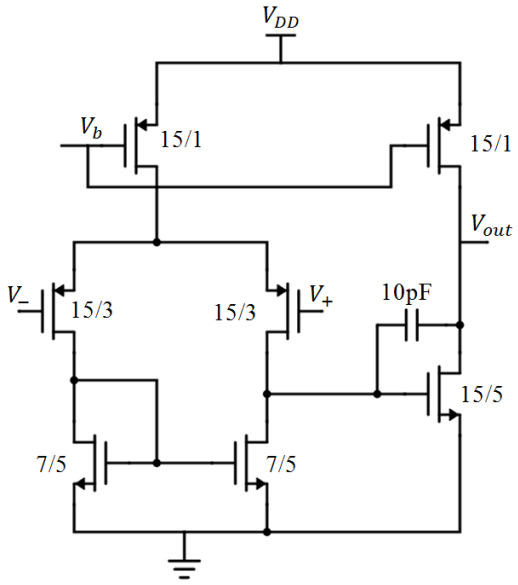


Fig. 4.13. Schematic of the Opamp used in the amplifier

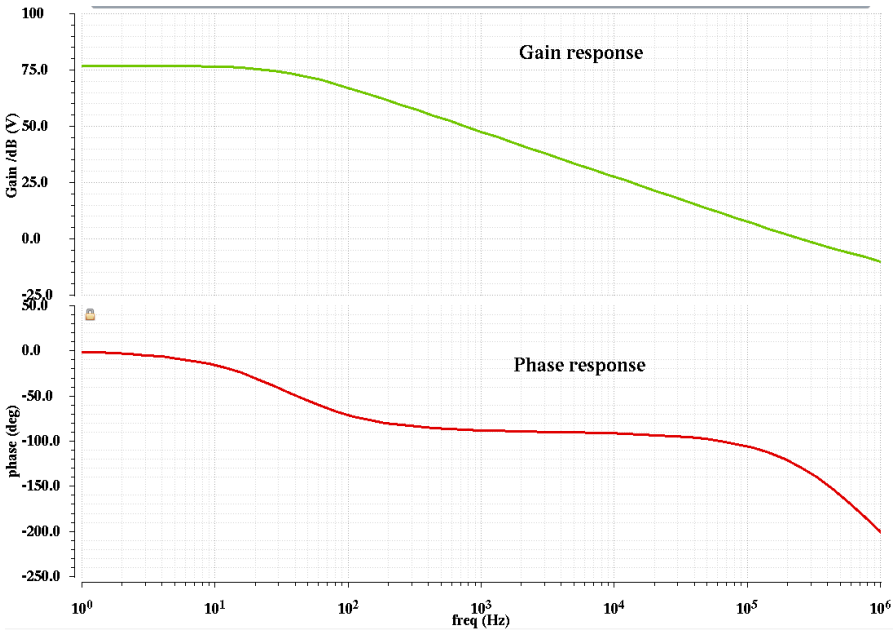


Fig. 4.14 Open loop frequency response of the Opamp

The Opamp was operated at a 1V supply voltage. It consumed 6µA current and had a gain bandwidth product of 250KHz with 51^{o} phase margin. Its output swing was from 20mV-950mV and exhibited a Total Harmonic Distortion (THD) of 0.6% when driven by 700mV peak-peak input sinusoid (i.e. used as a buffer).

The full schematic of the front end is shown in Fig. 4.15.

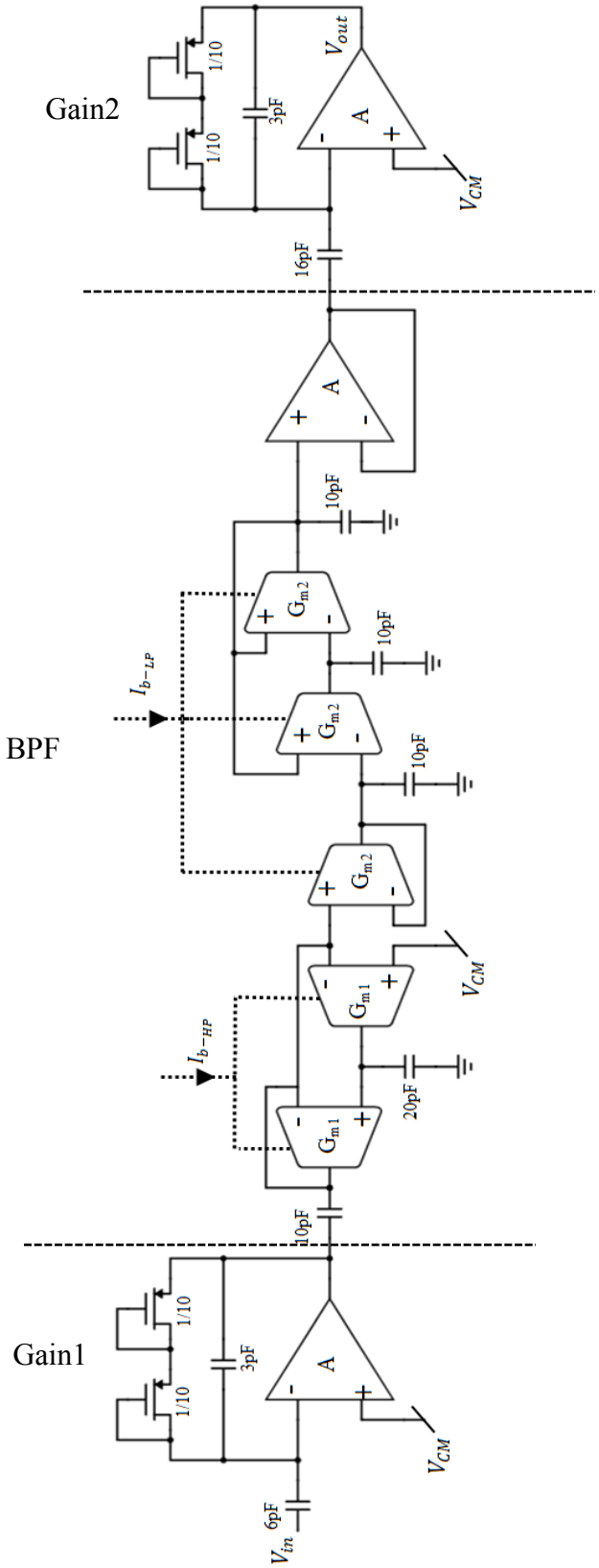


Fig. 4.15. Full schematic of the AFE

As seen in the figure, the first stage is an amplifier with a gain of 2. This was followed by the BPF. The output of the BPF was buffered via a unity gain buffer before the final stage amplifier. This was to prevent from loading the BPF with a capacitive load, which would change its frequency response from the desired one. The last stage is the ADC driver, which is an amplifier with a gain of 5.3. The common mode voltage for the circuits was set to half the reference voltage of the ADC (400mV). This ensured that the output of the AFE, for full scale input, swings within the ADC input range. All the capacitors were implemented as MIM capacitor (metal-insulator-metal) because these have the highest area capacitance density (2fF/μm^2 in the AMS 0.18μ process) and therefore require the smaller design area to implement.

4.3. Biasing Circuits

4.3.1 Biasing Currents

The transconductance of the OTA cell is inversely proportional to temperature and directly proportional to its biasing current. Therefore, a proportional-to-absolute temperature (PTAT) current source was used to bias the OTA and eliminate the dependency of its transconductance on the temperature. This results in a robust filter design that is insensitive to temperature variations. Additionally, the biasing current should be independent on the supply voltage to obtain similar filter performance for a range of supply voltages. The biasing circuit that was used to generate a PTAT current source that is independent on the supply voltage is shown in Fig. 4.16. This is a modified version of the low voltage CMOS bandgap circuit in [20].

Transistors $M_{n1}$and M_{n2} were in saturation weak inversion region. Hence, the current that flows through them can be expressed as:

$$I_{Mn1} = I_{s0}\left(\frac{W}{L}\right)_{Mn1} e^{\left(\frac{V_A - V_{thn}}{nV_T}\right)} \tag{4.30}$$

$$I_{Mn2} = I_{s0}\left(\frac{W}{L}\right)_{Mn2} e^{\left(\frac{V_C - V_{thn}}{nV_T}\right)} \tag{4.31}$$

The voltage across resistor R_x is equal to:

$$V_{R_x} = V_B - V_C \tag{4.32}$$

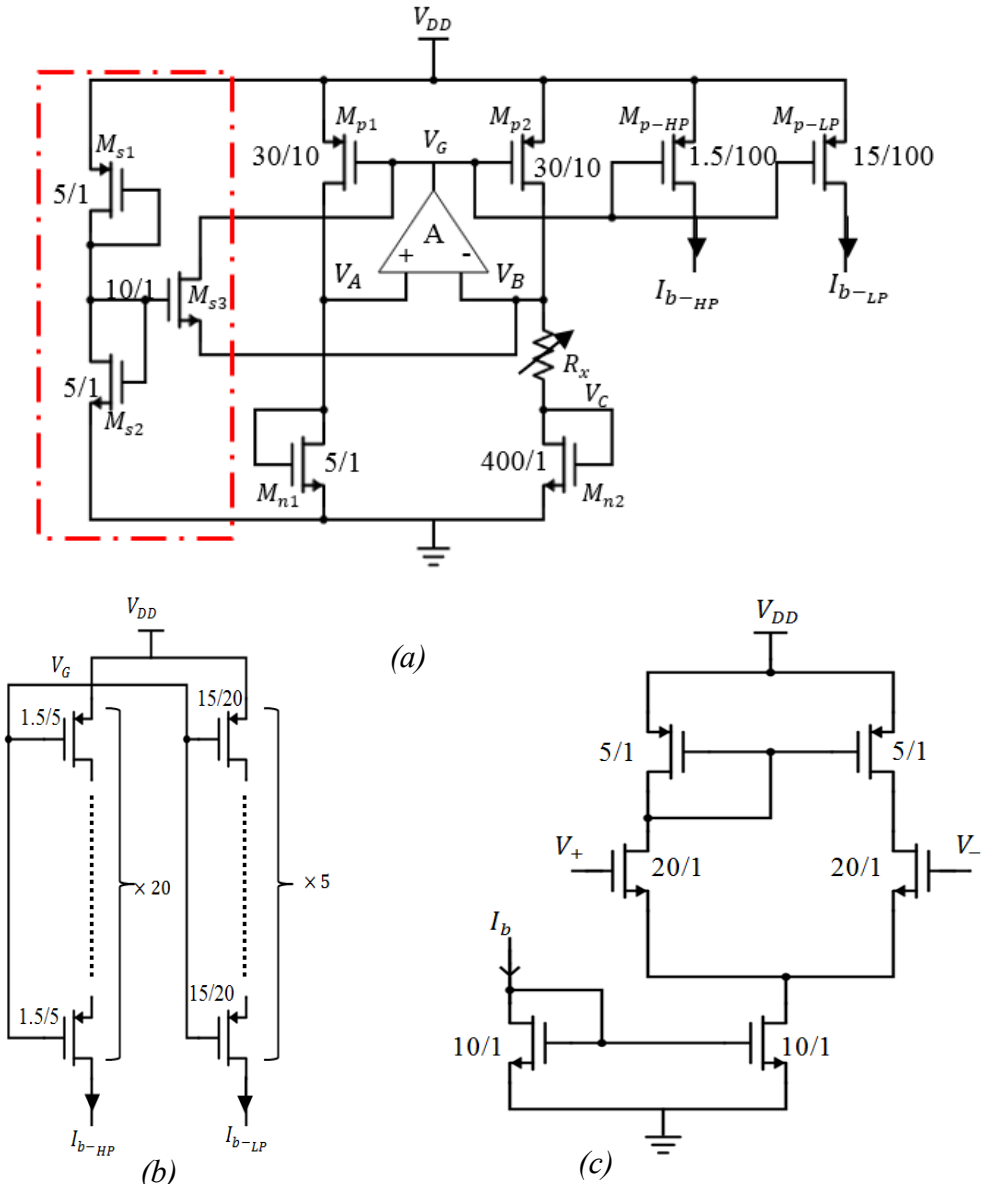


Fig. 4.16. (a): schematic of the PTAT current source (b): break down of the transistors M_{p-LP} and M_{p-HP} (c): Schematic of the Opamp used in the PTAT circuit

The voltages V_B and V_A are maintained at the same level because of the Opamp's feedback. Additionally, the currents I_{Mn1} and I_{Mn2} are equal due to the top current mirror formed by M_{P1} and M_{P2}. Rearranging equations (4.30) and (4.31) to get expressions for V_A and V_C and then substituting them back in equation (4.32):

$$V_{R_x} = nV_T\, ln(r) \tag{4.33}$$

where $r = \frac{(W/L)_{Mn2}}{(W/L)_{Mn1}}$.

The current that flows through R_x (I_{R_x}) is the current that flows through the top PMOS current mirrors and is equal to:

$$I_{R_x} = \frac{nV_T \ln(r)}{R_x} \tag{4.34}$$

If this current is mirrored via other PMOS devices $(M_{p-LB}$ and $M_{p-HB})$ as shown in Fig. 4.16, then the mirrored output current is:

$$I_b = \frac{nV_T \ln(r)}{R_x} \frac{(W/L)_P}{(W/L)_{M_{P2}}} \tag{4.35}$$

where $\left(\frac{W}{L}\right)_P$ is the dimension of the PMOS biasing transistor $(M_{p-LP}$ or $M_{p-HP})$.

The circuit has two stable operating points, one at zero current and the other one as shown in equation (4.34). Therefore, a start-up circuit was used to inject current in the circuit and then disconnect it. The start-up circuit, shown in the red broken box in Fig. 4.16(a), is formed by transistors M_{S1}, M_{s2} and M_{s3}. Transistors M_{S1} and M_{s2} form a potential divider to set the biasing voltage at the gate for M_{s3}, which was set to be lower than the final DC voltage V_B. Transistor M_{s3} injects a small amount of current into the circuit. When V_B reaches its steady state value, transistor M_{s3} enters the cut-off region because it has a negative V_{gs} at that instant. This disconnects it from the circuit without interfering with its normal operation. It is worth noting that the current in equation (4.35) is not dependent on the operating regions of M_{P1}, M_{P2} or the mirroring PMOS transistors $(M_{p-LP}$ and $M_{p-HP})$. The dimensions of M_{P1} and M_{P2} were selected wide and long in order to reduce the effects of mismatch and also set the gate voltages of the bottom NMOS transistors (M_{n1} and M_{n2}) below their threshold voltage but above 100mV, to ensure that M_{n1} and M_{n2} remained in the saturation weak inversion region.

This circuit was used to provide the biasing current for the HPF$(I_{b-_{HP}})$ and LPF$(I_{b-_{LP}})$. The biasing current to the filters can be trimmed by adjusting the value of R_x, which is an off-chip resistor. This adjusts the value of g_m in the filters to compensate for cut-off frequency variations due to process variations or mismatch between the capacitors and thus maintain a robust filter performance. Setting the value of R_x to 300kΩ, the required dimensions of M_{p-LB} and M_{p-HB}

to achieve 30nA I_{b-LP} and 3nA I_{b-HP} were 15µ×100µ and 1.5µ×100µ respectively. Transistor M_{p-LP} was created by cascading 5 transistors in series, each with dimensions 15µm×20µm. Similarly transistor M_{p-HP} was created cascading 20 transistors in series, each with dimensions 1.5µm×5µm, as shown in Fig. 4.16(b). This is an optimum layout for long transistors and helps to reduce the effect of process variation during fabrication.

4.3.2 Biasing Voltage

A biasing voltage (V_b) is required to bias the Opamp and to set the DC common mode of the AFE (V_{CM}). The Opamp's biasing current must be independent on the supply voltage to achieve a similar performance across a range of supply voltages. This is achieved if the gate-source voltage of the top PMOS transistors in Fig. 4.13 is set to be fixed and independent on the supply voltage. This requires the biasing voltage of the Opamp to scale linearly with the supply voltage. Such a characteristic is exhibited by the voltage at node V_G in Fig. 4.16(a). The voltage at node V_G has the following dependency with the supply voltage:

$$V_G = V_{DD} - \alpha_0 \tag{4.36}$$

When this voltage was used to bias the Opamp's top PMOS current mirrors, it resulted in a fixed gate-source voltage of the PMOS transistors equals to α_0 which was set to 460mV in the design.

The common mode voltage of the AFE was set to to half the reference voltage of the ADC as previously mentioned. A potential divider with ratio of half was utilized and supplied from the ADC's reference voltage. As the CM voltage was set via a ratio of components rather than absolute value, the effect of process variations and mismatch on the CM voltage is minimized. The biasing voltages are simply set via a potential divider using PMOS devices as shown in Fig. 4.17.

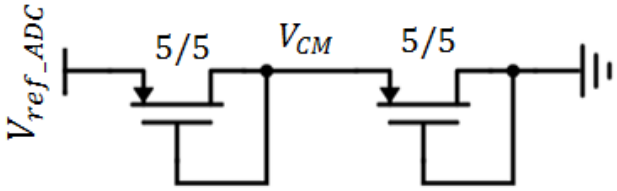


Fig. 4.17. PMOS potential divider to generate a biasing voltage half the ADC reference

This is superior to resistive potential dividers because it consumes less design area and requires low power. No buffer is needed to isolate the biasing voltage. This is because this voltage connects to the gate terminal of other transistors and thus does not have any effect on its DC operation. The circuit consumed a current of 380nA at 0.8V supply. The biasing voltage was fixed during 100 Monte Carlo simulations. This was because this voltage was set by the ratio of the devices and because the devices were designed to have a relatively big area($25\ \mu m^2$) with equal lengths and width (square shape). This improved their immunity to process variations and mismatch. The biasing voltage had no variations across a temperature range from -10^0C to 60^0C. This was expected because only PMOS devices were used and therefore any temperature variation would change the characteristic of the PMOS devices (holes mobility) in equal amounts keeping the ratio of their resistances constant.

4.4. Regulator

A regulator is required to provide a stable 1V supply voltage for the AFE and to boost its Power-supply-rejection (PSR). The PSR is defined as the attenuation of any noise/variations at the supply voltage to the AFE's output. It is crucial that the AFE's PSR equals the DR of the system so that any fluctuations in the supply voltage are suppressed below the DR at the AFE's output. The system had a DR of 50dB and the AFE's had a -20dB of PSR rejection on its own. Hence a regulator with PSR better than -30dB was required. A -30dB PSR is possible to achieve using a conventional linear-dropout (LDO) regulator as shown in Fig. 4.18.

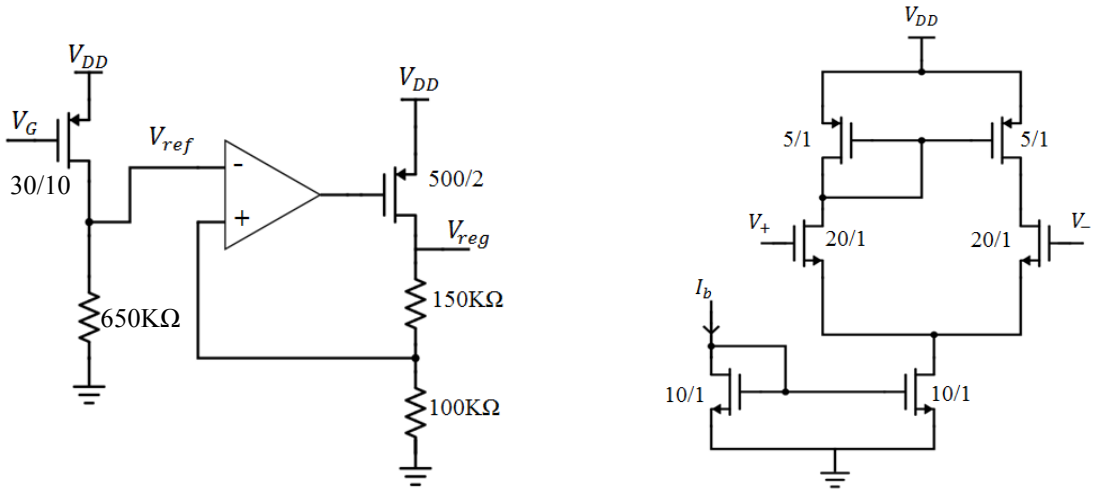


Fig. 4.18. LDO Regulator Schematic (right) and Opamp implementation (left)

The reference voltage was generated using a constant current source that passes through a resistor as shown in Fig. 4.18. The voltage V_G was taken from the circuit in Fig. 4.16(a) and therefore a constant reference voltage that is independent on the supply voltage was generated. The reference voltage was set to 400mV via a 650KΩ resistor and then was boosted to 1V via the resistors ratios in the LDO (boosting ratio of the LDO is 1+150/100).

4.5. Simulations

The full AFE and its biasing were simulated at 1.3V power supply. The circuit consumed 40µW of power (30µA total current consumption). This current consumption included the AFE, biasing circuits and the regulator. The simulated frequency response and the transient response to 10 mV peak-peak 500Hz sinusoidal of the AFE are shown in Fig.4.19 and Fig.4.20 respectively.

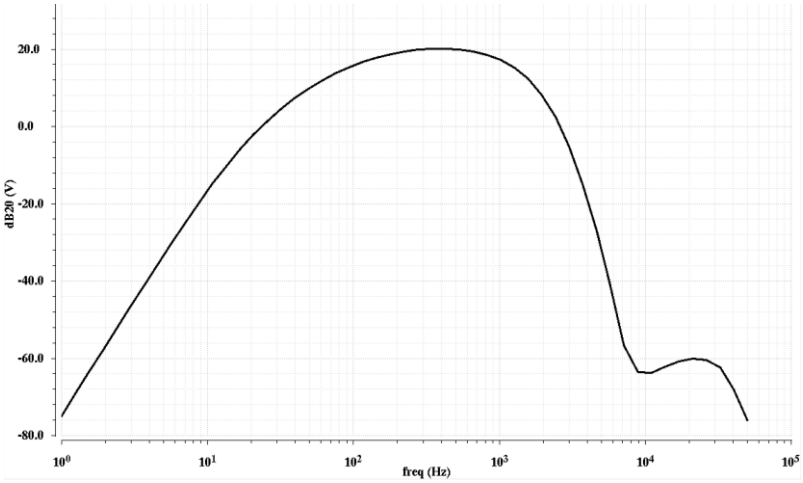


Fig. 4.19. Simulated frequency response of the AFE in Cadence environment

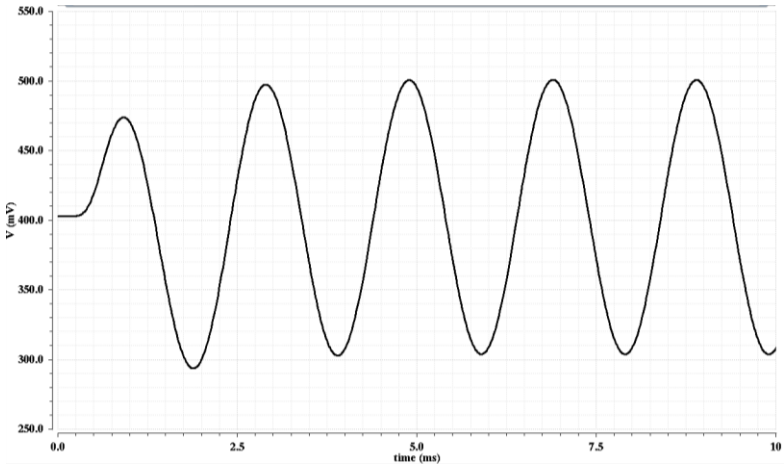


Fig. 4.20. Simulated AFE transient response to 10 mV peak-peak 500Hz sinusoidal

Monte Carlo simulations were performed on the AFE to see the impact of process variation and mismatch on its behavior. 100 Monte Carlo runs at constant temperature of 25ºC were used in the simulations. The variations in the pass-band gain due to process variations and mismatch are shown in the Fig. 4.21.

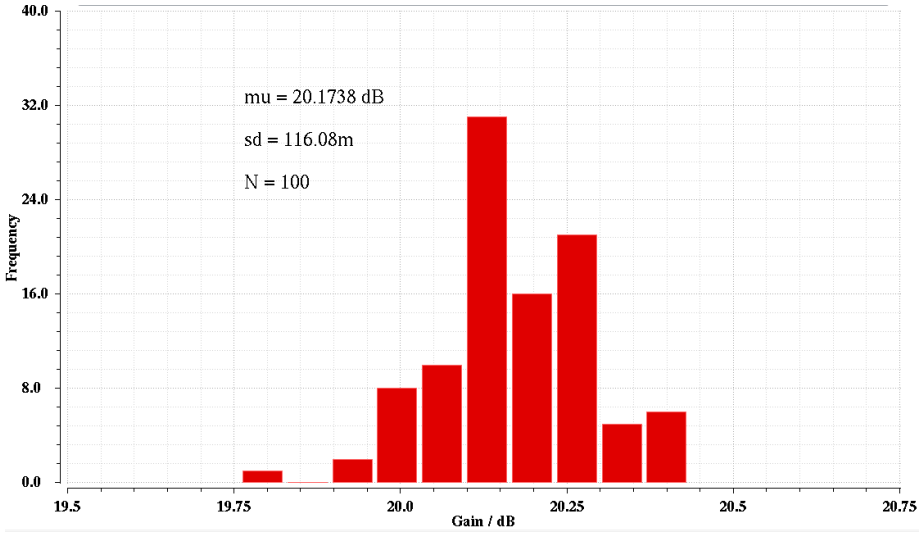
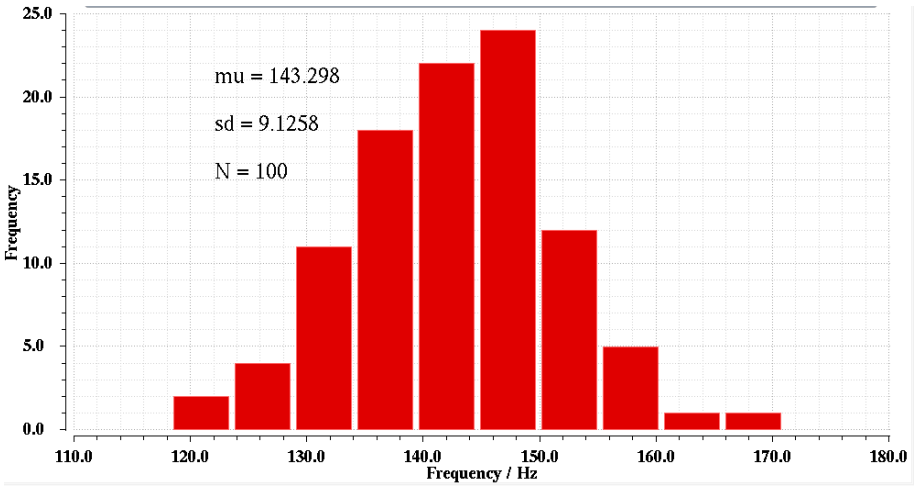


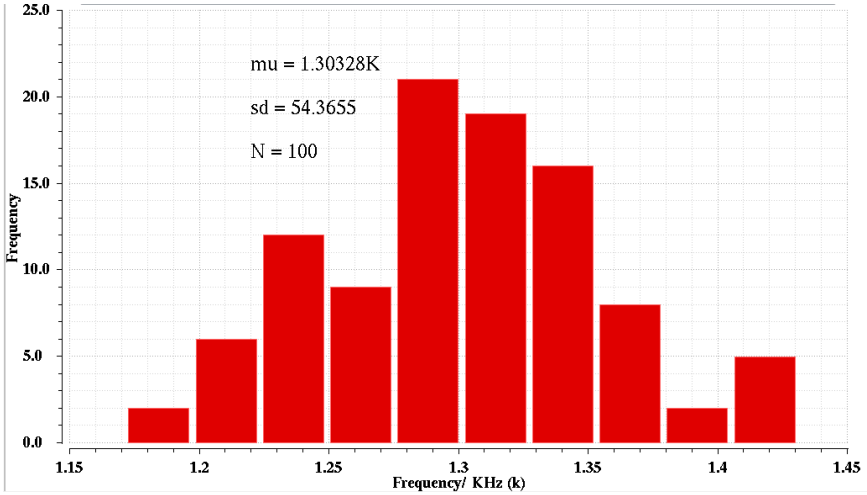
Fig. 4.21. Variations in pass-band gain due to mismatch and process variations from 100 Monte Carlo simulations

Fig. 4.21 shows the gain variation is between 19.75dB - 20.4dB, which is about 0.65dB. This small variation was achieved because the pass-band gain was set by the ratio of two capacitors rather than their absolute value. The variation of on chip capacitors ratio in the AMS 0.18µm process is ±10% while the variation between capacitors was between 0.2%-1%. The negative feedback also makes the amplifier's gain to be much less sensitive to variations in the Opamp's specifications (such as open loop gain or bandwidth).

The variations in corner frequencies due to mismatch and process variations from 100 Monte Carlo runs are shown in Fig. 4.22.



(a)



(b)

Fig. 4.22. Variations in the filter's cut-off frequency due to mismatch and process variation from 100 Monte Carlo simulations: (a)high-pass cut-off frequency. (b) low-pass cut-off frequency

The average high-pass cut-off frequency was 143Hz, varying between 119Hz – 170Hz. This variation is attributed to the variations in the biasing current to the HPF and in the capacitors values. More than 90% of the values of the HPF cut-off frequency were in a frequency range within 130Hz-160Hz. These are very close to the required specs of the HPF described in Chapter 2, Section 2.3.1.4.

The average low-pass cut-off frequency was 1.3KHz and varied between 1.13KHz–1.46KHz. This variation is attributed again to the variations in the biasing current to the LPF and in the capacitors value. The variation in the low-pass cut-off frequency sets the minimum sampling

frequency of the ADC. This is because the variation in the low-pass cut-off frequency will change the frequency at which 50dB attenuation (relative to the pass-band) occurs. Therefore, the sampling frequency must be adjusted accordingly so that frequencies greater than $(f_s - BW)$ get attenuated below the *DR* of the signal (50dB), as explained in Chapter 2, Section 2.3.1.4. The variation in the frequency at which 50dB attenuation occurs is shown in Fig. 4.23.

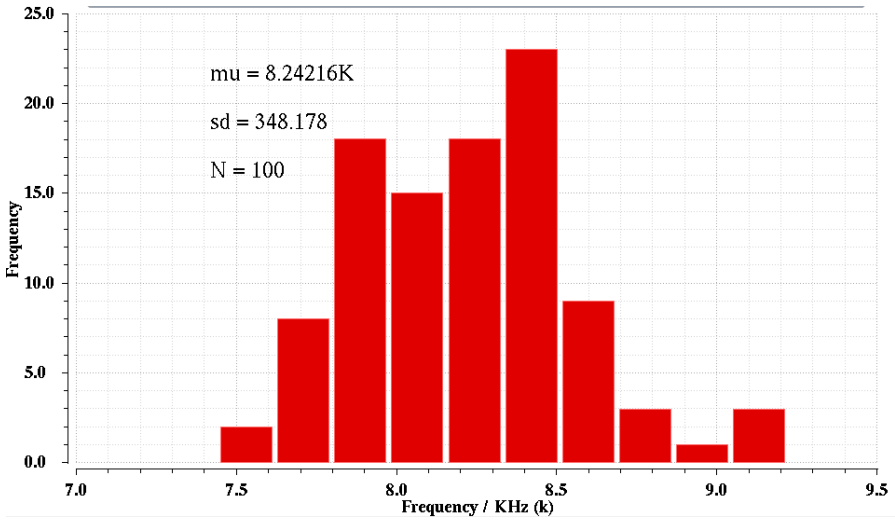


Fig. 4.23. Variations in the frequency at which 50dB attenuation (relative to the pass-band) occurs

The average frequency at which 50dB attenuation occurs was 8.24KHz, with variations between 7.46KHz-9.2KHz. This means that the lowest sampling frequency of the ADC must be around 8.4KHz (7.46KHz + 0.9KHz) in order to ensure sufficient attenuation of the image frequencies. In any case, and as shown in Section 4.3, this frequency can be controlled by trimming the biasing current to the HP via the of-chip resistor R_x.

4.6. Conclusion

This chapter has described the design of the system's AFE. The major trade-off in the AFE between noise and linearity was analysed. This analysis led to the different constituting circuit blocks' specifications. The first stage of the AFE was chosen to be an amplifier with a gain of 2; this was followed by a BPF with bandwidth from 140Hz-1.3KHz; and then an amplifier with a gain of 5.3 to drive the ADC. The circuit implementation of the filters and amplifiers inside the AFE was explained, as well as the implementation of the regulator and the biasing circuits. Simulation results were finally presented, showing that the AFE consumed 40µW of power at

1.3V supply. Finally, Monte-Carlo simulations validated the robustness of the design in the presence of mismatches and process variations.

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Chapter 5: Speech Elimination

5.1. Introduction

Acoustic detection of respiratory and cardiac physiological signals implies that there are acoustic noise artifacts. These artifacts include other noise sources such as surrounding environment sounds and speech sounds. Surrounding environment sounds are weakly detected by the wearable sensor because it is placed in an acoustic chamber which attenuates external sounds to a large extent. However, speech sounds are a strong inherent artifact as they come from the trachea. Speech data, however, have no use in diagnosing respiratory and cardiac diseases and the power consumed from transmitting them, which is proportional to the duration of the speech, is considered an unnecessary waste. It has been estimated that people speak between 16,000-40,000 words a day [1], which is equivalent to 2-5 hours of total speech data on average. This is a substantial amount of unnecessary data. Thus, eliminating speech would reduce the total amount of transmitted data, consequently leading to an increase in the system's battery life. This percentage increase can be expressed as:

$$K = \frac{ah}{24 - ah} \times 100 \tag{5.1}$$

Where K is the percentage increase in battery life, h is the total duration of discarded speech data in hours and a is the percentage of the transmitter's power consumption to the system total power consumption. Assuming the transmitter consumes more than half the current consumption of the system($a > 0.5$), equation (5.1) shows that the battery life can be extended at least by 5%-12% by discarding 2-5 hours of speech data, respectively. This facilitates the use of a smaller battery and hence reduces the system's size and weight, which makes it more comfortable and convenient to use.

In this chapter, a data reduction algorithm based on speech elimination is proposed and implemented wit ultra–low power CMOS circuits. The algorithm and its circuit implementations are simple and can be easily integrated in the existing design. The rest of the chapter is organized as follows: Section 5.2 describes the proposed data reduction algorithm to eliminate speech. In

Section 5.3, analysis of the circuits that were used to implement the algorithm is presented. Based on this analysis, the specifications of different circuit blocks were derived and then implemented in circuit topologies that provide the required performance with ultra-low power consumption. Section 5.4 presents the experimental results to verify the functionality of the circuit and Section 5.5 summarizes the conclusions of the chapter.

5.2. Data Reduction Algorithm

The block diagram of the proposed wearable medical device with the data reduction block included is shown in Fig. 5.1.

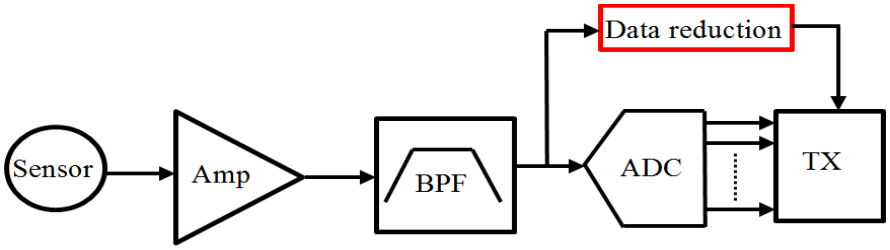


Fig. 5.1. Block diagram of the proposed wearable medical device with the data reduction block

In a wearable system such as the one described by Fig. 5.1, the voltage level associated with physiological signals at the AFE's output has fixed maximum amplitude. This is determined by the amplifier's gain, amplifier's common-mode (CM) output voltage and the maximum amplitude of the raw physiological signal sensed by the microphone. On the other hand, speech signals have larger voltage amplitudes that it will saturate the amplifier's output. This big difference in amplitudes is exploited by different methods to detect speech or breath segments in an acoustic signal. The first method is based on performing complex mathematical transforms, such as Hilbert transform, on the acoustic signal which require a microcontroller to implement [3-6]. This makes it unsuitable for low power wearable applications. The second method is based on spike encoding of the acoustic signal via CMOS circuits [7, 8]. This method generates a train of spikes for which the density is proportional to the amplitude of the input signal. The number of spikes in a fixed time window is counted and divided by the duration of that time window in order to calculate the density of the spikes train. The spikes train's density is then compared with a threshold to identify speech segments. This method requires a digital counter to continuously count the number of spikes, which adds to the power consumption. Furthermore, some of the

design parameters have to be determined empirically before the design process can start, which can be time consuming.

The proposed speech detection in this work is achieved by extracting the envelope of the acoustic signal and then comparing it with a threshold to detect speech segments. The output of the speech detector circuit, identified as *"HALT"*, is a binary signal for which a high level represents speech data and low level represents breathing and cardiac data. This is illustrated in Fig. 5.2 on a 10 seconds acoustic signal.

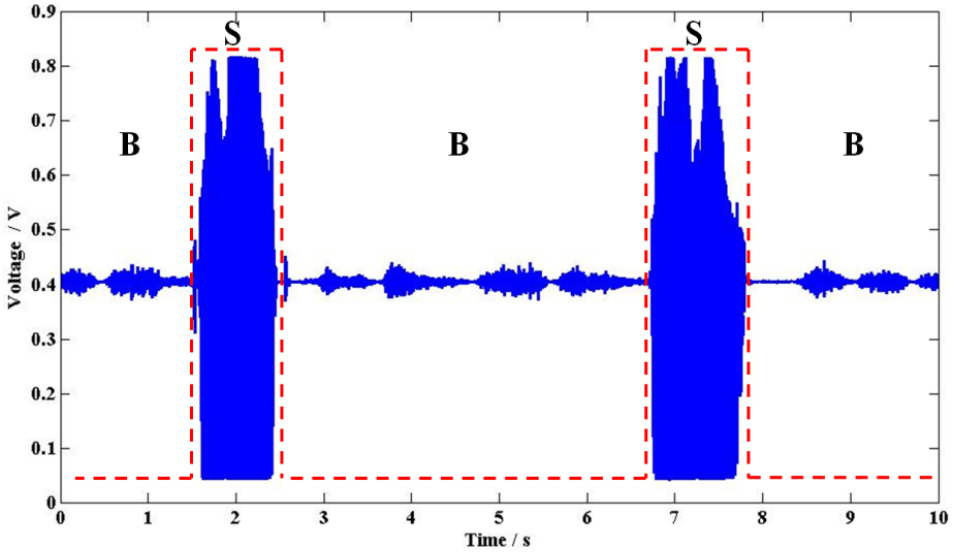


Fig. 5.2. Graphical illustration of the output of the speech detection method on a 10 seconds acoustic signal for the breathing monitor

The regions with letter "***B"*** indicate the breathing/cardiac part of the acoustic signal that needs to be transmitted and the regions with letter "***S"*** indicate the speech part of the signal to be eliminated. The "*HALT"* signal is represented by the red dashed graph. This is used to control the operation of the transmitter according to its voltage level. A high voltage level shuts down the transmitter and thus eliminates speech. To further reduce the total power consumption of the circuit, the resistor value inside the envelope detector was adjusted according to the envelope's voltage level. The full algorithm is summarized in the flow chart in Fig. 5.3.

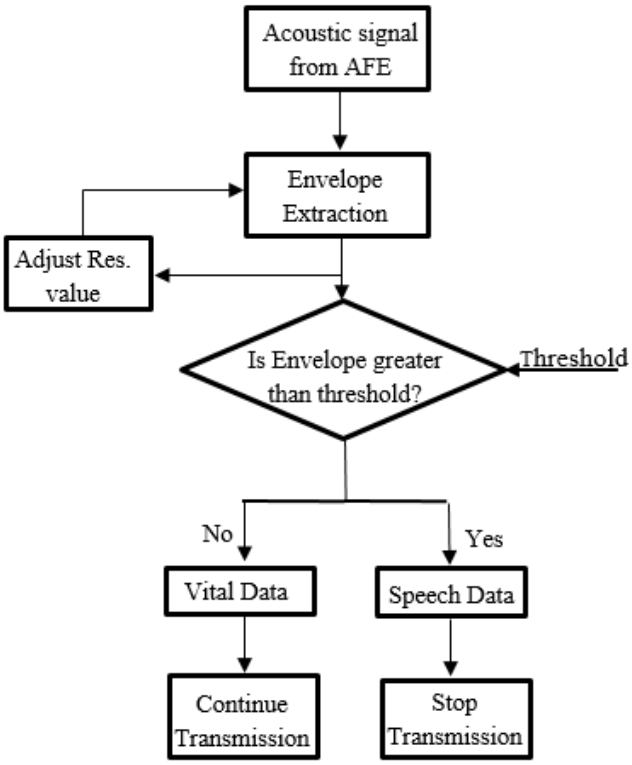


Fig. 5.3. Block diagram of the proposed data reduction algorithm.

5.3. Circuits analysis and design

5.3.1 Envelope Detector

An envelope detector circuit is required to extract the envelope of the amplified and filtered acoustic signal. The signal passes through a band-pass filter that has a bandwidth from 150Hz-1KHz. It then gets amplified by an amplifier with a gain of 10 (20dB) with 400mV CM output voltage and has a saturation output voltage of 800mV, which is reached during speech. The minimum voltage level of breathing signals after amplification is 1.7mV peak. This information indicates that the maximum and minimum input signals' amplitude to the envelope detector are 400mV and 1.7mV, respectively, imposed on a 400mV DC. This is equivalent to 48dB input dynamic range (DR).

Different envelope detectors/rectifiers topologies have been reported in the literature [9-16]. In [9, 10] a transconductor was used to drive a diode in current mode, rather than voltage, which results in larger bandwidth of operation. This type of rectifier has a good performance at a high frequency (MHz range) but suffers from a dead-zone caused by the diode. Another current mode

rectifier topology that does not use diodes and hence eliminates the dead-zone problem was reported in [11] where an Opamp configured in a negative feedback loop is used to buffer the input signal. The current that flows from the positive and negative supply of the Opamp are first converted to voltage via resistors and then buffered by two additional Opamps before getting finally subtracted to obtain the rectification function. This method solves the dead zone problem, however the matching between the resistors and the sensing Opamps is crucial and any slight mismatch causes different delays in the signal path, which limits the performance. An improved version of latter topology was reported in [12], where the Opamp is used in open-loop configuration to drive two-bipolar transistors. Another approach based on current conveyors was proposed in [13]. This consisted of two current conveyors driving four diodes for full wave rectification. All the aforementioned topologies were intended for high frequency operation, required a diode/BJT and had a large power consumption, which made them unsuitable for the application described here. More recent implementations for hearing and breathing sensors applications using only MOS transistors were proposed in [14-16]. The topology presented in [14] was designed for hearing aids/cochlear implant applications. It operates in current mode and has high bandwidth and large dynamic range. However, its power consumption is not ultra-low and hence was considered as unnecessary overdesign for this application. In [15] an envelope detector with a decay time-constant (i.e. time constant that decreases with increasing input amplitude) was reported and used for RMS estimation. This method is used to detect the RMS of the input signal and it produces an envelope that is 70% of the input signal peak, which is not suitable in this application. Another ultra-low power rectifier reported in [16] was used for breathing signal envelope detection. Its principle of operation was based on switching the output either to the input or to a reference voltage, based on the result of a comparison between the input and the reference voltage; if the input voltage was greater than the reference then the input was switched to the output, else the reference voltage (which was zero) was switched to the output. The rectifier had a reported power consumption of 60nW and 80dB *DR*.

The envelope detector proposed in this application is customized for ultra-low power operation, whilst achieving the required DR and frequency of operation. Its topology is shown in Fig. 5.4(a). As the figure shows, an operational amplifier is in negative feedback configuration with a PMOS pass transistor (M_p), a track capacitor (C_t) and a discharge resistor (R_d). The circuit operates as follows: in the *track state,* the input is increasing and is larger than the output. The

Opamp's output (V_g) starts to decrease turning M_p ON and charging the output node up to V_{in}. When the input starts to decrease and gets below the output voltage, V_g increases turning M_p OFF, at which point C_t starts discharging through R_d and brings the output voltage down. This is defined as the *discharge state*. When the input starts increasing again and exceeds the output voltage, M_p is turned ON and the circuit enters the *tracking state*. This continuous *track* and *discharge states* force the output to follow the envelope of the input.

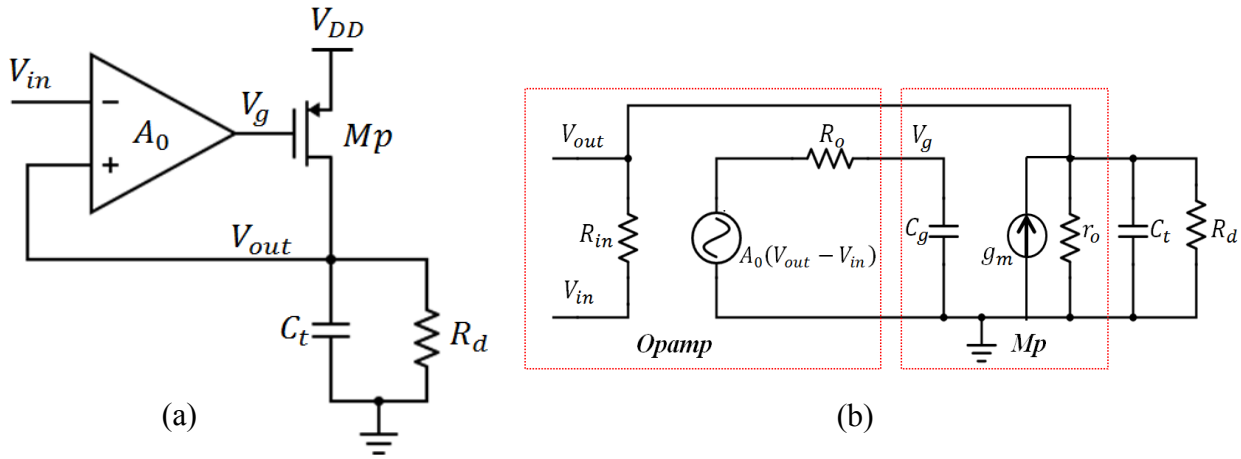


Fig. 5.4. (a) CMOS Envelope detector. (b) its small signal equivalent circuit

The small signal model of the envelope detector in the tracking state is shown in Fig. 5.4(b). A_0, R_{in} and R_o are the DC gain, input, and output resistance of the opamp, respectively. The input resistance of the opamp is assumed to be an open circuit. C_g is the summation of parasitic capacitances at the gate of M_p to ground. g_m and r_0 are the transconducatnce and output resistance of M_p respectively. The open loop transfer function gives an insight on the stability of the envelope detector once the loop is closed and helps in defining the required Opamp's specifications in order to ensure closed loop stability and proper tracking. Assuming that $R_d \gg r_0$ and $A_0 g_m r_0 \gg 1$, the open loop transfer function $L(s)$ can be expressed as:

$$L(s) = \frac{A_0 g_m r_0}{\left(1 + {}^{s}/_{\omega_p}\right)\left(1 + {}^{s}/_{\omega_a}\right)} \tag{5.2}$$

where $A_0 g_m r_0$ is the DC gain of the open loop, ω_a is the pole's frequency at the Opamp's output which is equal to $\omega_a = 1/R_o C_g$, and ω_p is the pole's frequency at the output node which is

equal to $\omega_p = 1/r_o C_t$. The pole at the output node is the dominant pole, i.e. $\omega_p < \omega_a$. This is because $C_t \gg C_g$. The frequency of the output pole is dependent on the value of the current that passes through M_p during tracking (I_{Mp}) and is directly proportional to it. To ensure stability of the closed loop, the pole locations of the open loop must stay far away from each other for all values of I_{Mp}. This is especially important when I_{Mp} is maximum because that is when the two poles are nearest to each other. The further the open loop poles are from each other, the higher the phase margin of the open loop transfer function and thus the higher damping factor of the closed loop.

The closed loop transfer function was used to assess the criterion on the Opamp's bandwidth to achieve a specific damping factor and stability at all conditions. The envelope detector's closed-loop transfer function, $H(s) = V_{out}/Vin$, can be written as $H(s) = \frac{L(s)}{1+L(s)}$ and arranged in the general form of a second order transfer function as:

$$H(s) = \frac{{\omega_n}^2}{s^2 + 2\zeta\omega_n\, s + {\omega_n}^2} \tag{5.3}$$

Where:

$${\omega_n}^2 = A_0\omega_p\omega_a g_m r_0 \quad (5.4) \quad , \quad \zeta = \frac{1}{2}\sqrt{\frac{C_t(\omega_a+\omega_p)}{A_0 g_m}} \qquad (5.5)$$

The damping factor of the envelope detector must be greater than or equal to $1/\sqrt{2}$ to avoid any overshoot in the output and improve tracking accuracy. This leads to the following condition on ω_a :

$$\omega_a \geq \frac{2A_0 g_m|_{max}}{C_t} \tag{5.6}$$

The maximum value of g_m $(g_m|_{max})$ occurs when the charging current of C_t (I_{Mp}) is maximum, which is during the tracking of speech segments in the acoustic signal. The expression of g_m can be written in terms of drain current and Inversion Coefficient (IC) [17]:

$$g_m = \frac{I_{Mp}}{nV_T\left(\sqrt{IC + 0.25} + 0.5\right)} \tag{5.7}$$

Where n is the slop factor (~1.3) and V_T is the thermal voltage $(26mV)$. The expression of IC is

given as [17]:

$$IC = \frac{I_{Mp}}{2n\,\mu_p C_{Ox}\,{V_T}^2 \times \left(\frac{W}{L}\right)_{Mp}} \tag{5.8}$$

During tracking, I_{Mp} is written as:

$$I_{Mp} = C_t \times \frac{dV_{out}}{dt} \tag{5.9}$$

The rate of change of the acoustic signal's envelope is between 10V/sec - 250V/sec. A 200nF off-chip capacitor will result in a charging current range from 2µA-50µA resulting in *IC* between 1- 25. This puts the value of g_m between 35µS-265µS, which requires an amplifier bandwidth of 150KHz with 51dB gain to get a damping factor greater than or equal to $1/\sqrt{2}$. Placing a resistor R_2 in series with C_t, as shown in Fig. 5.5, creates a zero in the transfer function and improves the stability of the envelope detector [18]. This reduces the required Opamp's bandwidth to achieve a proper damped response and hence reduces the total power consumption of the envelope detector.

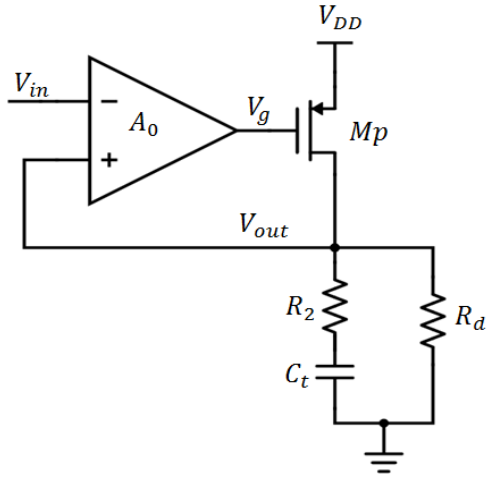


Fig. 5.5. Envelope detector with improved damping after introducing R_2

The new transfer function $H_2(s)$ is written as in [18] (assuming that $R_d \gg r_0$ and $A_0 g_m r_0 \gg 1$):

$$H_2(s) \approx \frac{1 + sR_2C_t}{\left[s^2 \frac{1}{A_0\omega_p\omega_{a_2}g_m r_0} + s\left(\frac{\omega_p + \omega_{a_2}(1 + A_0 g_m R_2)}{A_0\omega_p\omega_{a_2}g_m r_0}\right) + 1\right]} \tag{5.10}$$

Where ω_{a_2} is the new Opamp's bandwidth.

The new quality factor is approximated as (assuming $R_2 \ll r_0$):

$$\zeta_2 = \frac{1}{2}\sqrt{\frac{\omega_{a_2} C_t (1 + A_0 g_m R_2)}{A_0 g_m}} \tag{5.11}$$

Setting the value of $R_2 = \alpha / A_0 g_m$ and assuming that $\alpha \gg 1$, the new specification on the Opamp's bandwidth is:

$$\omega_{a_2} \geq \frac{2A_0 g_m|_{max}}{\alpha C_t} = \frac{\omega_a}{\alpha} \tag{5.12}$$

5.3.1.1 Tracking resistor

The value of the resistor R_2 should be set as big as possible. However there is an upper limit on it. Resistor R_2 will cause an error in the stored value in the tracking capacitor because it introduces an *RC* delay. This will consequently reduce the DR of the envelope detector.

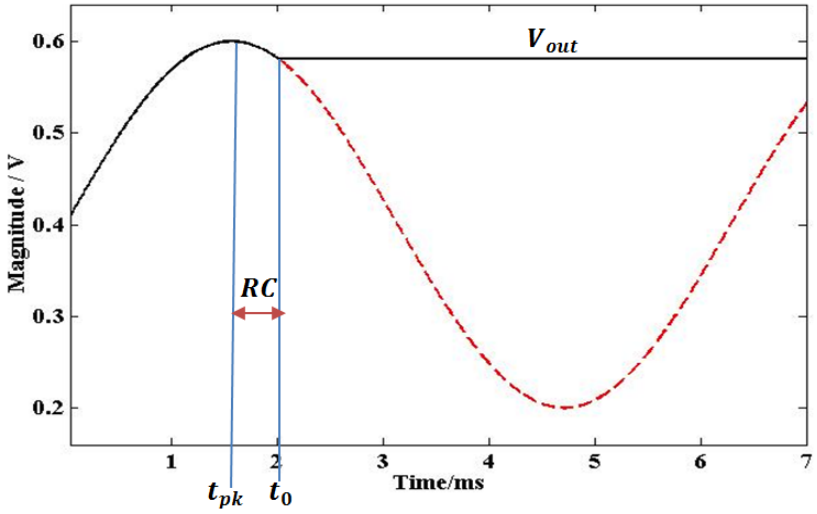


Fig. 5.6. The envelope of a sinusoidal input after adding R_2 showing the error in the stored peak value due to the RC delay

For a sinusoidal input, the stored value in the tracking capacitor is shown in Fig. 5.6 and can be expressed as:

$$V_{out} = V_{in}(t_0) \tag{5.13}$$

The time t_0 is equal to:

$$t_0 \approx t_{pk} + R_2 C_t \tag{5.14}$$

The expression V_{out} can be written approximately as:

$$V_{out} = V_{in_peak} + R_2 C_t \left.\frac{dV_{in}}{dt}\right|_{t=t_0} \tag{5.15}$$

Defining the error in the value stored in C_t as a percentage (δ %):

$$\delta = (V_{out} - V_{in_peak})/V_{in_peak} \tag{5.16}$$

The error due to R_2 is most significant during the tracking of high amplitude signals. To keep the error in the value stored in C_t below a certain percentage (δ %) the maximum value of R_2 must satisfy:

$$R_2 \leq \frac{(\delta/100) \times V_{in_{max}}}{C_t \, dV_{in_{max}}/dt} \tag{5.17}$$

Where $V_{in_{max}}$ is maximum input signal's amplitude and $dV_{in_{max}}/dt$ is the rate of change of maximum input when it is tracked.

The rate of change of the maximum input's amplitude when it is tracked was 250V/s, and the tracking capacitor value 200nF. To keep the error less than 5% for a 400mV maximum input amplitude, R_2 must be less than 400Ω. If more accuracy is required, then a lower value of R_2 should be selected. However, this would require larger Opamp's bandwidth to achieve the desired damping factor. By setting the value of R_2 to 300Ω, the new specification on the opamp's bandwidth became 5.5 KHz as opposed to 150KHz with a gain of 51dB. This required less biasing current for the Opamp and hence reduced the total power consumption of the circuit.

5.3.1.2 Pass Transistor

The current that flows though M_p when tracking the input is dependent on the value of C_t and the rate of change of the envelope (output). The maximum and minimum currents that pass through M_p are during the tracking of speech and breath signals respectively. The size of M_p affects the Opamp's output voltage. A small transistor size will force the opamp's output below its output swing range during the tracking of speech signals, and this will consequently reduce the tracking accuracy. Similarly, the Opamp's output will be forced above its output swing range

during the tracking of breathing if M_p is sized too large. There is therefore an optimal size for M_p.

It is preferred that M_p operates in the moderate-strong inversion region so that it has the lowest value of g_m for a certain drain current and device area [19], and hence the maximum damping factor can be achieved for a set of design parameters. The Inversion Coefficient method was used to determine the dimensions of M_p. The dimension of M_p to achieve a specific IC can be obtained from (5.8):

$$\left(\frac{W}{L}\right)_{Mp} = \frac{I_{Mp}}{2n\mu_p C_{Ox} {V_T}^2 \times IC} \tag{5.18}$$

Where I_{Mp} is the drain current of M_p, and the rest of the symbols have their usual meaning. M_p will most likely enter weak inversion when its IC is minimum during the tracking of the breathing signal. An IC greater than 1 ensures that M_p is in moderate-strong inversion region, and thus the dimension of M_p will be chosen such that its IC is greater than 1 during the tracking of breathing. As the drain current of M_p increases during the tracking of speech signals, its IC will increase, pushing M_p further in the strong inversion region. Therefore, the minimum current dictates the size of M_p. The minimum current carried by Mp was $2\mu A$ and hence from (5.18), $W/L = 30 = 15\mu m/0.5\mu m$, $\left(\mu_p C_{Ox} = 40 \times 10^{-6}\right)$.

When M_p is in moderate inversion region, its overdrive voltage $\left(V_{SG} - \left|V_{thp}\right|\right)$ is in the following range [20]:

$$-70mV < V_{SG} - \left|V_{thp}\right| < 220mV \tag{5.19}$$

From (5.19), the gate voltage of Mp is expected to swing in the following range:

$$V_S - \left(220mV + \left|V_{thp}\right| + \delta\right) < V_G < V_S - \left(\left|V_{thp}\right| - 70mV\right) \tag{5.20}$$

The factor δ is added to account for the fact that M_p will enter strong inversion during the tracking of speech signals because its IC will be greater than 10. Therefore, its overdrive voltage will be slightly above the upper limit of (5.19). The value of δ was calculated using the formula of the gate overdrive voltage presented in [17] :

$$\delta = 2n\, V_T\left(\sqrt{IC_2} - \sqrt{IC_1}\right) \tag{5.21}$$

Where IC_1 is the inversion coefficient of M_p at the boundary of moderate-strong inversion region and equals to 10. IC_2 is the inversion coefficient of *Mp* when the maximum current passes through it, which was 25 in this application (ratio of maximum to minimum envelope's rate of change). Hence δ was calculated to be about 120mV. For a source voltage of 1V and $|V_{thp}| = 400mV$, the voltage swing at the gate of M_p was:

$$260mV < V_G < 670mV \tag{5.22}$$

The maximum and minimum gate voltages occur during the tracking of breathing and speech signals, at which the Opamp had an input CM voltage of 400mV with 400mV peak voltage swing. This information set the specification on the Opamp's input CM range and input and output swing.

5.3.1.3 Opamp

An Opamp with a gain of 51dB and bandwidth of 5.5 KHz was required in this application. The required input CM range was from 400mV-800mV and the output swing between 260mV-670mV. The minimum detectable signal, within certain accuracy, was limited by the Opamp's offset voltage, open loop gain and CM output voltage rather than noise. The expression for the gate voltage of *Mp* during tracking can be written as:

$$V_g(t) = V_{CM} + A_0\big(V_{out}(t) - V_{in}(t) - V_{of_A}\big) \tag{5.23}$$

Where V_{CM}, A_0 and V_{of_A} are the Opamp's CM output voltage, open loop gain and offset voltage referred to the negative terminal, respectively. In order to achieve accuracy greater than *x*% when tracking the minimum input voltage, the maximum limit on the offset voltage can be approximated as (assuming sufficiently large Opamp's open loop gain):

$$V_{of} \leq (1 - x/100)V_{in_{min}} \tag{5.24}$$

To achieve accuracy greater than 90% at 1.7mV minimum input peak voltage, the maximum Opamp's offset voltage must be less than 170µV. Such a small offset voltage requires offset cancellation techniques, which increase the total power consumption. In this application, large errors in tracking the minimum input, which is associated with breathing sounds, were tolerable

and would not affect the algorithm. Hence, using offset cancellation techniques to reduce the offset voltage at the expense of increasing the power consumption was not necessary. On the other hand, the upper limit of the DR is dependent on the Opamp's open loop gain at large input amplitudes. Therefore, the Opamp must be designed in such a way that all the transistors stay in saturation when the maximum input is applied.

The load capacitance at the Opamp's output is the parasitic capacitance at the gate of M_p. The pass transistor will be operating in the strong inversion region and hence the maximum parasitic capacitance at the output of the Opamp can be written as:

$$\begin{aligned} C_L &= C_{gs-Mp} + C_{gd-Mp}\left(1 + \left|A_{v-Mp}\right|\right) \\ &= C_{Ox}\, WL + 2C_{OV} \times W \end{aligned} \tag{5.25}$$

The gain of the pass transistor $\left(A_{v-Mp}\right)$ can be ignored in the tracking state, because most of the current that flows through M_p passes through the capacitor C_t and bypasses the resistor R_d. For transistor dimensions of $W \times L = 15\mu m \times 0.5\mu m$, the estimated load capacitor was about $78fF$ (C_{Ox}=*8.5fF/μm²,* C_{OV}*=0.5fF/μm).* The required Opamp's specifications are summarized in Table 5.1.

Table 5.1. Summary of the required Opamp's specifications

Specification	Value
Bandwidth	5.5Khz @ $78fF$ load capacitor
Gain	51dB
Input common mode	400mV-800mV
Output swing	260mV-670mV
Power consumption	Minimum

These specifications could be met with the least amount of power using a single stage differential Opamp as shown in Fig. 5.7. The Opamp was designed to operate in weak inversion and biased with 60nA tail current. The Opamp's bandwidth was 5.7KHz with a gain of 350 (51dB).

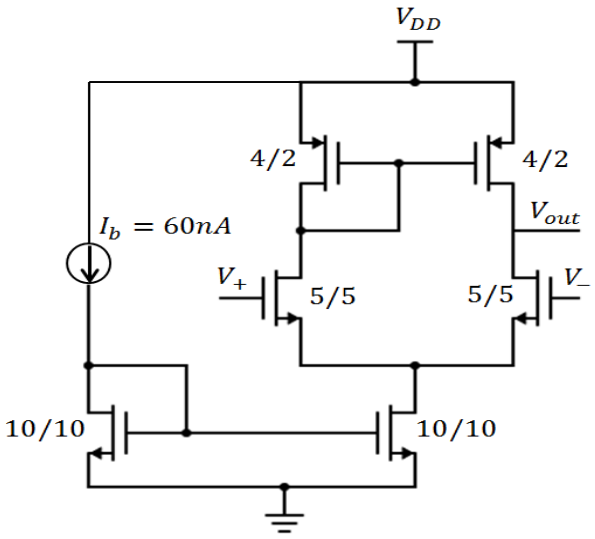


Fig. 5.7. Schematic of the Opamp

5.3.1.4 Tracking capacitor

The value of the tracking capacitor dictates the total power consumption of the envelope detector and the design area. There was no practical upper limit on the value of the capacitor used. This was because a surface mount off-chip capacitor could be used, which had a very small area compared to the total PCB's area and thus would not cause any size penalty. Therefore, the value of the tracking capacitor was selected to minimize the total power consumption. The total power consumption of the envelope detector is divided into two components: the Opamp's power consumption (P_{opamp}) and the power due to the current that passes through M_p in the tracking state (P_{Mp-avg}). P_{opamp} is preset and fixed throughout operation, while P_{Mp-avg} depends on the magnitude of the input signal. As has been derived in Appendix5.1, the total average power consumption of the envelope detector (P_{ED}) can be approximated as:

$$P_{ED} = P_{opamp} + P_{Mp-Avg}$$

$$= V_{DD}\left\{\left(\frac{8C_0A_0}{\alpha\lambda}\sqrt{\frac{2\beta_{Mp}(dVin/dt)_{max}}{n}}\right)\sqrt{\frac{1}{C_t}} + \frac{K_S}{T_S}\left(\left[V_{S_{peak}} - V_S(t_{start})\right]C_t + \frac{V_{S_{peak}}}{R_{D_S}}t_{0_S}\right)\right.$$

$$\left. + \frac{K_B}{T_B}\left(\left[V_{B_{peak}} - V_B(t_{start})\right]C_t + \frac{V_{B_{peak}}}{R_{D_B}}t_{0_B}\right)\right\} \quad (5.26)$$

Fig. 5.8 shows a plot of P_{ED}, P_{opamp} and P_{Mp-Avg} versus C_t from 100pF-500nF for the following design parameters:

$C_0 = 78fF, A_0 = 350, \alpha = 25, \lambda = 0.1, \beta_{Mp} = 0.0012, n = 1.3$, $(dVin/dt)_{max} = 250, V_{S_{peak}} = 0.8V$, $V_S(t_{start}) = 0.79V, R_{D_S} = 2.27M\Omega$, $t_{0_S} = 0.87ms$, $T_S = 7ms, K_S = 0.2, V_{B_{peak}} = 0.43V$, $V_B(t_{start}) = 0.426V, R_{D_B} = 26.7M\Omega$, $t_{0_B} = 0.92ms$, $T_B = 20ms, K_B = 0.8$

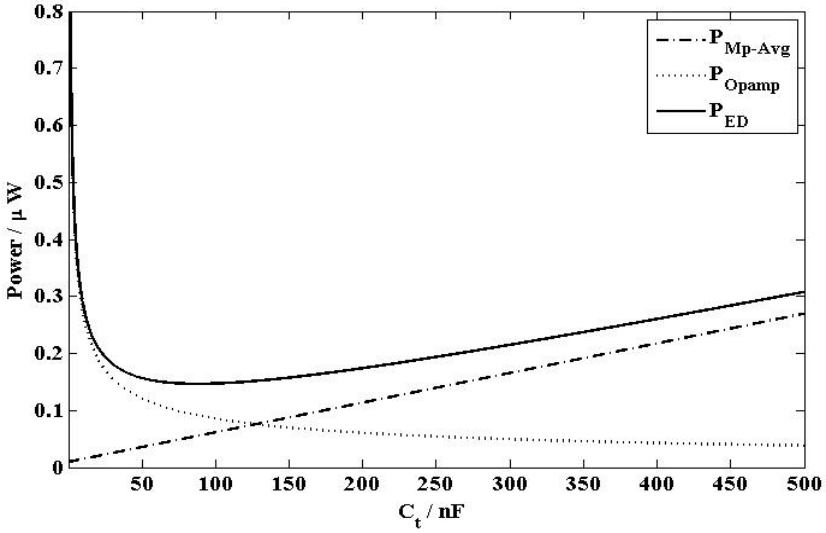


Fig. 5.8. Variation of the total average power consumption of the envelope detector against C_t

At small values of tracking capacitance, the detector's current consumption is dominated by the Opamp, because a high Opamp's bandwidth is required to achieve a proper damped response. On the other hand, the detector's current consumption at large capacitor values is dominated by the charging current of C_t and it becomes linearly dependent on it. In this application, a 200nF off-chip tracking capacitor provided a satisfactory performance.

5.3.1.5 Discharge resistor

The discharge resistor R_d is the discharge path of C_t when M_p is turned OFF in the discharge state. The time constant formed by R_d and C_t dictates the discharge rate of the envelope and consequently how fast the transmission of data is resumed after speech stops. There are no strict requirements on the time window between the end of speech and the continuation of data transmission. However, for the integrity of a monitoring system, the time window should be minimized. In this design, the time window was limited to less than 300ms.

A low value discharge resistor will allow the transmitter to be turned ON more rapidly after the end of the speech segments. However, this can create glitches in the comparator's output due to rapid discharge of the envelope during short durations of low magnitude breathing sounds in-between speech. It was measured that the time duration of these short breaths was less than 100ms. Hence, the value of the discharge resistor was chosen such that the output envelope discharges to the threshold voltage in a time window between 100ms-300ms. It was also desirable to increase the value of the discharge resistor during the tracking of breathing $\left(R_{D_B}\right)$ to reduce the total power consumption of the envelope detector, as can be seen in (5.26). Simulations showed that the total power consumption of the envelope detector could be reduced by 67% by increasing the value of R_{D_B} by a tenfold. Therefore, the discharge resistor was designed to be voltage dependent with its resistance inversely proportional to its voltage. A PMOS transistor was used to implement this functionality as shown in Fig. 5.9.

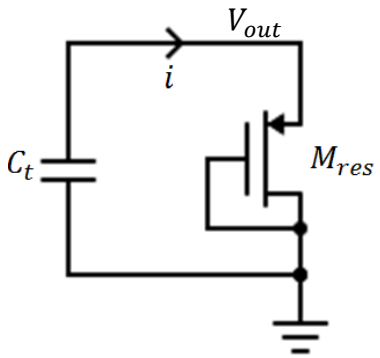


Fig. 5.9. Capacitor discharging through a PMOS transistor in the discharge state when M_p is OFF

The resistance of the PMOS device is minimum during the tracking of speech segments. This allows the envelope to discharge to the reference voltage in the desired time window, which minimizes the duration of un-transmitted breathing signal. When the circuit starts tracking the breathing signal, which is the majority of the time, the resistance of the PMOS device increases and the total power consumption of the envelope detector decreases.

The reference voltage was set to 600mV. This is because the maximum voltage of the raw breathing signal during day time is less than 40mV peak-peak, sensed using a microphone model (Knowles SPV1840LR5H-B). This signal gets amplified using an amplifier with a gain of 10 and CM output voltage level of 400mV, and hence the maximum peak voltage of the amplified breathing signal was around 600mV. Even though during sleep time the maximum peak voltage

of the amplified acoustic signal can reach values higher than 600mV peak due to snoring, the functionality of the speech elimination circuit can be turned off during night time via a control button.

During the discharge of the envelope from 800mV-600mV, the PMOS device is in strong inversion saturation region. Therefore, the discharge of C_t through the PMOS device can be modeled as:

$$-C_t \frac{dV_{out}}{dt} = \frac{1}{2}\mu_p C_{ox} \frac{W}{L}\left(V_{out} - \left|V_{thp}\right|\right)^2, \qquad 0.8V < V_{out} < 0.6V \tag{5.27}$$

Equation (5.27) can be solved and arranged to get an expression for the output voltage as:

$$V_{out}(t) = \left|V_{thp}\right| + \frac{1}{\frac{\mu_p C_{ox} {}^{W}/_{L}}{2C_t}\, t + \left(V_{Amp} - \left|V_{thp}\right|\right)^{-1}} \tag{5.28}$$

The required dimension of the PMOS resistor to discharge the output from an initial voltage $\left(V_{Amp}\right)$ to a final voltage $\left(V_{ref}\right)$ in a time window (t) is:

$$\left(\frac{W}{L}\right)_{Mres} = \frac{2C_t\left\{\left(V_{ref} - \left|V_{thp}\right|\right)^{-1} - \left(V_{Amp} - \left|V_{thp}\right|\right)^{-1}\right\}}{t\mu_p C_{ox}} \tag{5.29}$$

Where V_{Amp} is the saturation voltage of the amplifier. Using the following design parameters: $V_{ref} = 0.6V$,$\left|V_{thp}\right| = 0.4V$, V_{Amp}=0.8V,$C_t = 200nF$, $\mu_p C_{ox} = 40\mu A/V^2$ and $t = 100ms - 300ms$, the required dimension of the PMOS devices is in this range:

$$0.083 < \left(\frac{W}{L}\right)_{Mres} < 0.25 \tag{5.30}$$

The value of W/L was set to 1/10.

5.3.2 Comparator

The comparator compares the acoustic signal's envelope, which is a low frequency signal, with a DC threshold/reference voltage to generate the *"HALT"* signal. Therefore, the comparator is not required to have a high speed, and the main design priority is its power consumption. The

comparator's open loop gain is inversely proportional to its biasing current [21] and hence it can be designed to be ultra-low power with a very high open-loop gain and low speed. However, the comparator must have small offset voltage so that it changes output's state before a 300ms time window after the end of the speech. The condition on the comparator's offset voltage can be written using equation (5.28) as:

$$\frac{2C_t\left\{\left(V_{ref}-V_{of}-\left|V_{thp}\right|\right)^{-1}-\left(V_{Amp}-\left|V_{thp}\right|\right)^{-1}\right\}}{\mu_p C_{ox}\left({}^{W}/_{L}\right)_{Mres}} < 300ms \tag{5.31}$$

Where V_{of} is the comparator's offset voltage. From (5.31), the maximum acceptable comparator's offset voltage is:

$$V_{of} < \left(V_{ref}-\left|V_{thp}\right|\right)-\left\{\frac{0.15\mu_p C_{ox}\left({}^{W}/_{L}\right)_{Mres}}{C_t}+\frac{1}{\left(V_{Amp}-\left|V_{thp}\right|\right)}\right\}^{-1} \tag{5.32}$$

Substituting the design values from the previous section, the maximum acceptable comparator's offset voltage was 18mV. The two stage open-loop comparator without compensation capacitor is a very suitable option to achieve the required specification due to its high open loop gain, low power consumption and small design area. The low power, low speed and high open loop gain implies that the transistors inside the comparator must be designed to operate in the weak inversion region [19] and hence a PMOS input differential stage was used. The schematic of the comparator is shown in Fig. 5.10. The DC open loop gain of the comparator was 98dB with 250Hz bandwidth at 0.5pF load capacitor. The offset voltage was measured to be 2mV.

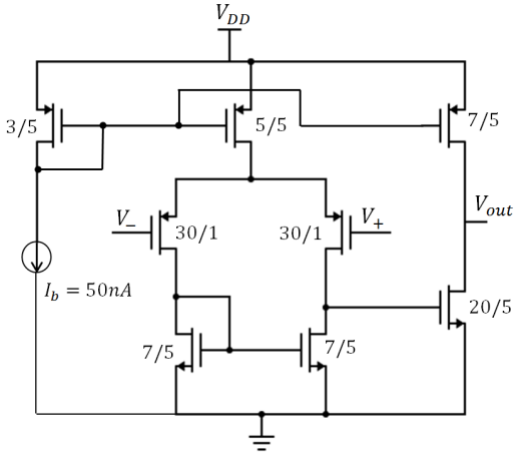


Fig. 5.10. Schematic of the comparator

5.4. Implementation and measurements

The data reduction algorithm was designed as a part of the system and fabricated in AMS CMOS 0.18µm 6M process. The envelope detector was tested with a 200nF off-chip track capacitor (C_t) and 300Ω series resistor (R_2) and supplied with 1V. The average power consumption of the envelope detector and the comparator were 120nW and 200nW, respectively (both excluding the biasing circuits), and the full circuit consumed an average power of less than 350nW. The tracking function of the envelope detector was tested using a 500Hz sinusoid with 200mV amplitude imposed on 400mV DC. The result shows that the envelope detector was properly damped. This is shown in Fig. 5.11. The output tracks the envelope of the input sinusoidal without any overshoot and discharges until the next peak, and then tracks again. A zoomed-in view of the input's peak at 3.5ms is shown in Fig. 5.12. This shows a 0.7% tracking error due to the *RC* delay.

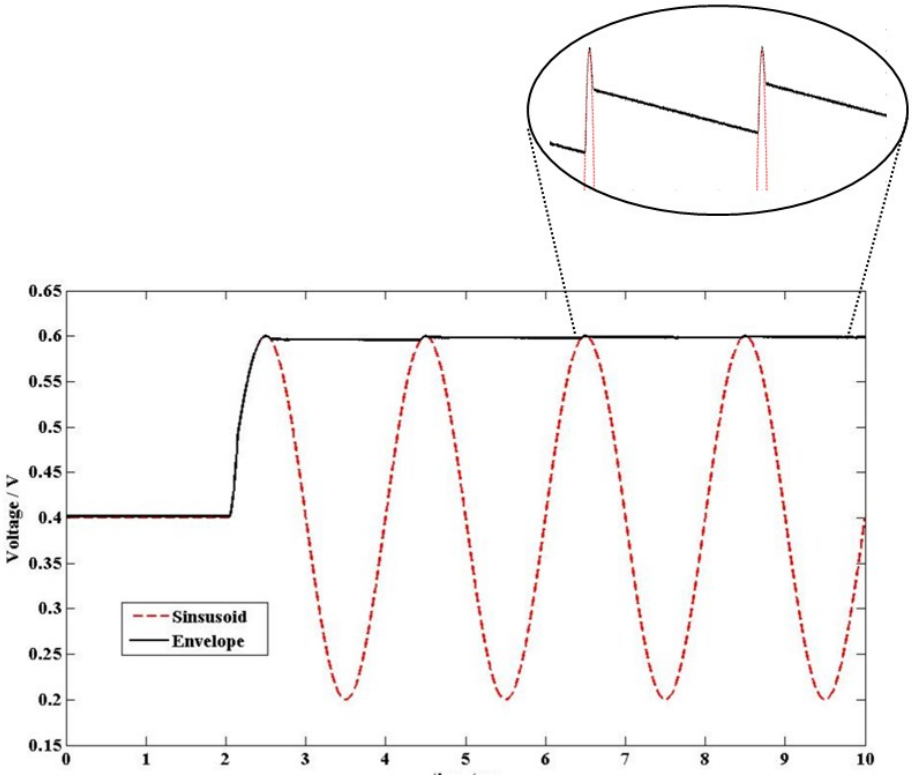


Fig. 5.11. Experimental results of the envelope detector at 500Hz 400mV peak-peak sinusoidal input signal

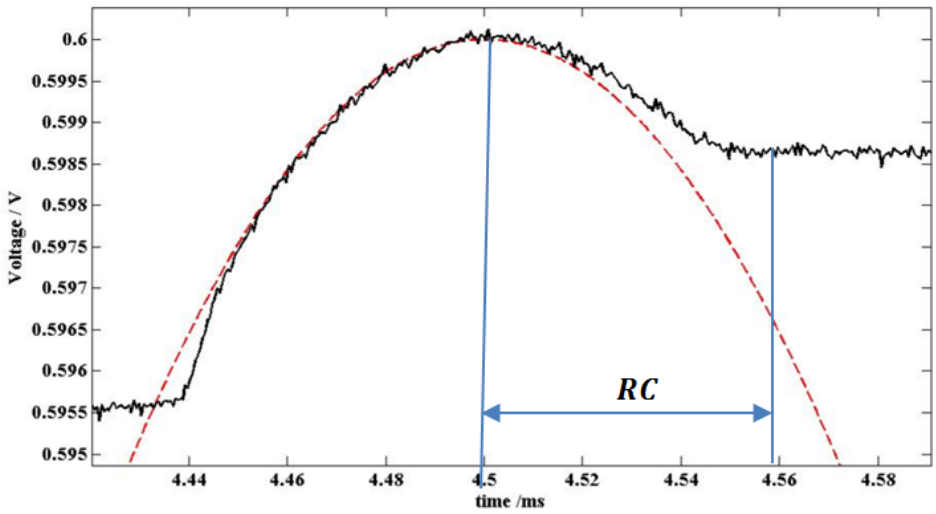


Fig. 5.12. A zoomed in view on the peak of the input voltage and the envelope

The second test carried out was the input-output characteristic of the envelope detector. This was measured using 500Hz sinusoids with amplitudes ranging from 1mV-600mV imposed on 400mV DC. These amplitudes provide an output envelope's rate of change from 2V/sec-1800V/sec (during transient of the input), which includes the acoustic signal envelope's rate of change. The result is shown in Fig. 5.13 along with the theoretical graph of $V_{in}=V_{out}$. The input DR within 10% error was from 12mV-570mV input voltage amplitude, which corresponds to an output envelop's rate of change from 35V/sec-1700V/sec. The envelope detector had a 60%-10% error at 1mV-12mV input voltage amplitudes respectively. This error was acceptable because input voltage amplitudes from 1mV-12mV correspond to breathing sounds and that's where the envelope detector had an output voltage range from 401mV-412mV. This was far below the threshold voltage of the comparator (600mV) and no comparison was being made at this point, therefore a very high tracking accuracy was not crucial in this range. The envelope detector's accuracy increases as the voltage starts to rise. It had a tracking error of 0.4%-4% at input voltage amplitudes from 200mV-400mV respectively. Therefore, the envelope detector could accurately extract the acoustic signal's envelope during speech and hence the comparator could make an accurate decision on when to turn the transmitter ON and OFF.

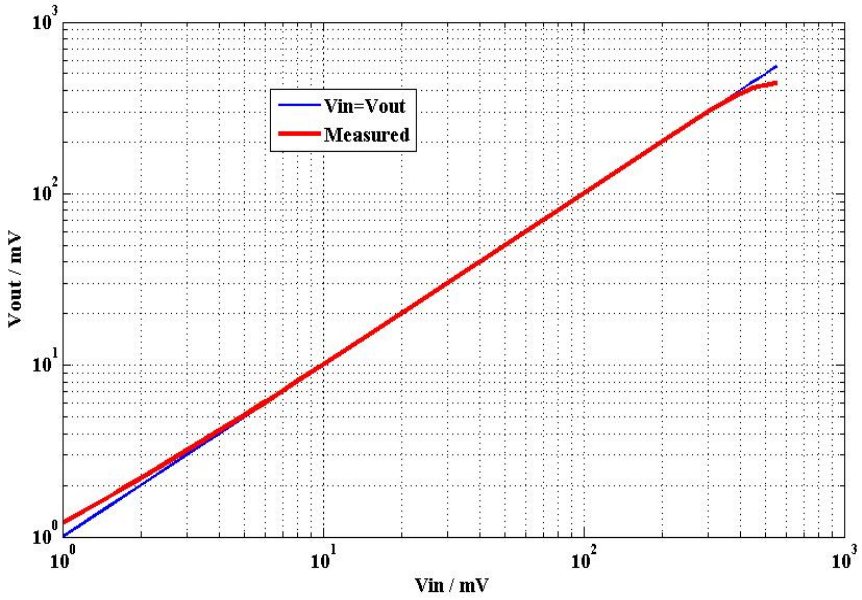


Fig. 5.13. Measured input-output characteristic of the envelope detector in red and the theoretical graph V_{in}=V_{out} in blue

Lastly, a ten second breathing signal was acquired using the microphone. The microphone was placed inside an acoustic chamber in order to reduce the outside noise and improve the signal-to-noise ratio (SNR) of the acoustic signal. The chamber was placed on the suprasternal notch part of the neck using an adhesive biomedical tape. The acoustic signal was fed into the chip to get amplified, filtered and then passed through the data reduction algorithm. The results are shown in Fig. 5.14 - Fig. 5.16. Speech is the high amplitude segments in the acoustic signal (800mV peak-peak) while breathing/cardiac sounds is the low magnitude parts (80mV peak-peak). The circuit could accurately extract the envelope of the acoustic signal without any overshoots, as shown in Fig. 5.14. The detector had the lowest time constant during the speech part of the acoustic signal because that is where the resistance of the PMOS resistor is minimum. As the envelope starts discharging, its discharge rate slows down due to the increased resistance of the PMOS resistor. When the envelope drops below 600mV, the discharge rate became noticeably slower as can be seen in Fig.5.15. However, at this point, the comparator's output was already low signaling the transmitter to resume operation and the discharge rate of the envelope had no effect anymore. The time delay between the end of speech and the *"HALT"* signal going low was measured to be 140ms which was within the requirements. Fig. 5.16 shows that the transmission of data stops when the "*HALT"* is high, thus eliminating speech data. Table 5.2 compares the speech detection proposed in this work with other reported designs in the literature.

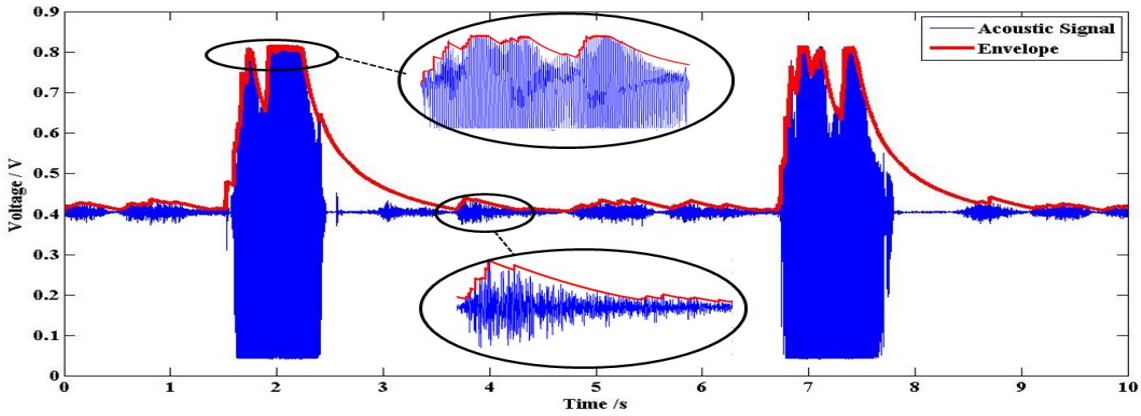


Fig. 5.14. The amplified and filtered acoustic signal with the envelope detector's output.

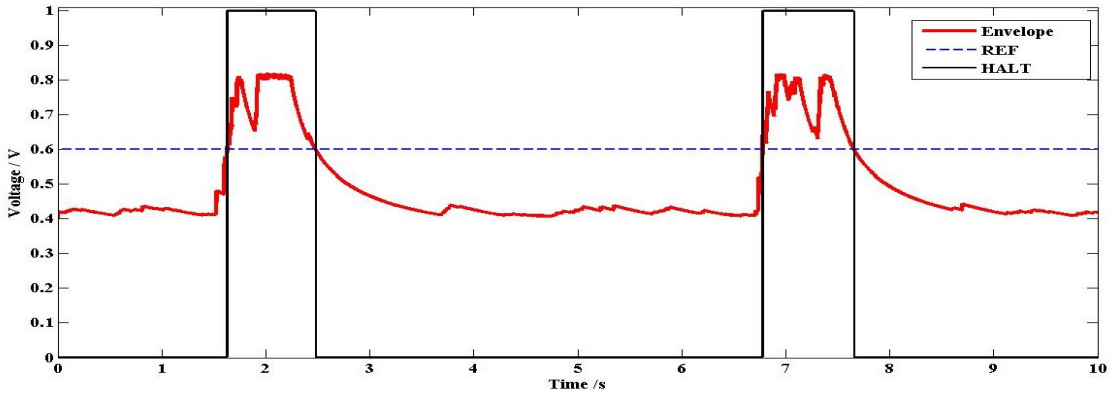


Fig.5.15. The envelope detector's output compared with a 600mV threshold to produce the "HALT" signal.

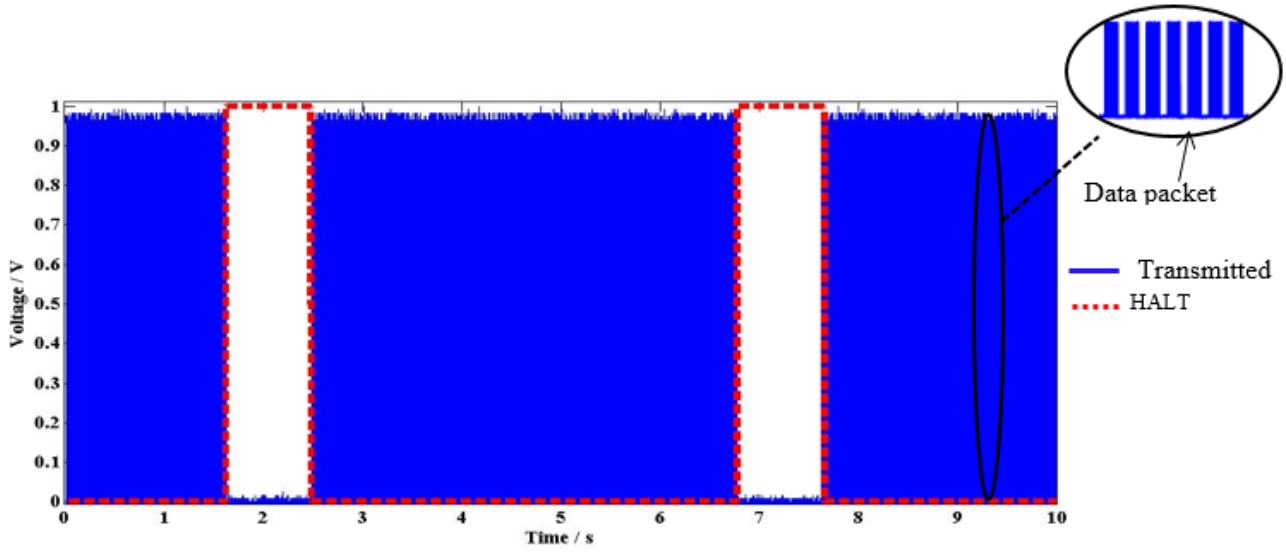


Fig. 5.16. Transmitted data showing that no data are transmitted while the "HALT" signal is high, and hence eliminating speech data

Table 5.2. Comparison of the speech detection method in this paper with other works in the literature

Work	*[7]*	*[8]*	This work
Process	0.5µm	1.6µm	0.18µm
Supply	2.5V	3V	1V
Power	300 nW*	465µW	350nW
DR(<10% error)	34 dB	N/A	34dB
Comment	∗Power consumption excludes the spike counter		

5.5. Conclusion

This chapter has presented an ultra-low power CMOS implementation of a data reduction algorithm that can be used in acoustic based breathing and cardiac wearable monitors. The algorithm reduces the amount of transmitted data by eliminating speech signals that are present in the sensed acoustic signal. This is achieved by extracting the envelope of the acoustic signal and then comparing it with a threshold voltage to identify speech segments. The output of the circuit is a binary waveform with a high level representing speech data and low level representing breathing data. This binary waveform is then used to shut the transmitter down whenever it is at a high level and thus eliminating speech data. The algorithm was implemented and fabricated in a CMOS 0.18µm 6-metal process. The measured results show effective functionality with less than 350nW power consumption.

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Chapter 6: ADC, Transmitter, and Full System Testing

This chapter is composed of four mains sections. Sections 1-3 described the design of the ADC, the transmitter and the PISO digital block respectively. The fourth section presents the lab measurements of the full system to verify its functionality.

6.1 The Analogue to Digital Converter (ADC)

The ADC converts the analogue input to binary bits that are transmitted in packets format. There are different ADC architectures that are suitable for different applications. The most widely used ones are Delta-Sigma, Successive-Approximation Register (SAR), Pipeline and Flash topologies. The choice of one or other architecture in a specific application depends on system/block specifications such as power consumption, sampling frequency and resolution. A performance comparison between different ADC architectures is shown in Fig. 6.1 [1].

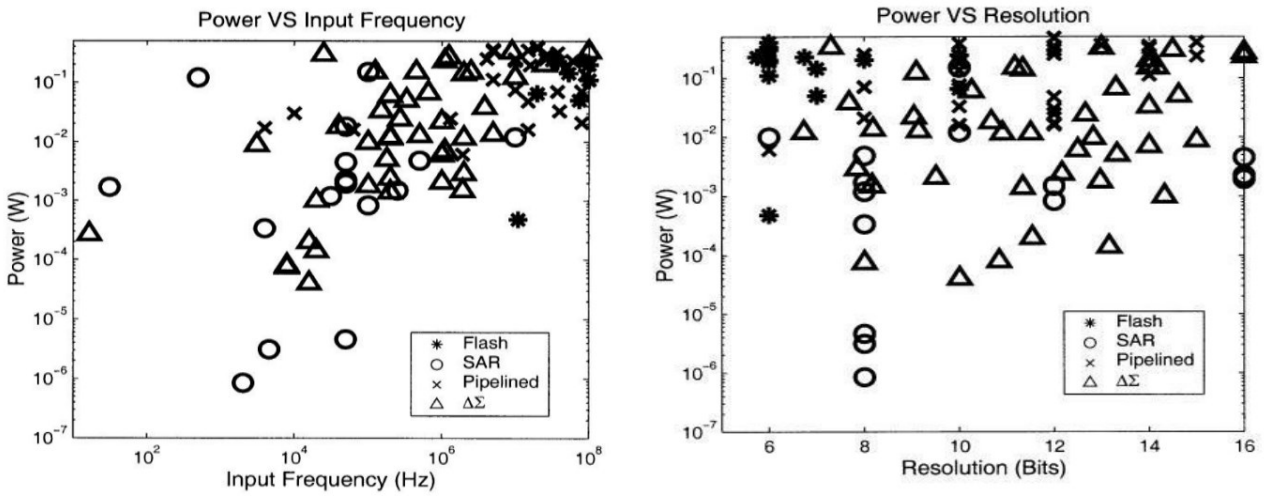


Fig. 6.1. Performance comparison for different ADC architectures [1]

Fig. 6.1 shows that SAR ADC achieves the lowest power consumption for 8-bit operation and input signal frequencies below 1KHz. Therefore, the ADC in this design was implemented as an

8-bit SAR ADC with 800mV reference voltage, allowing it to sample input voltage in the 0-800mV range. The ADC circuit and timing diagrams are shown in Fig. 6.2.

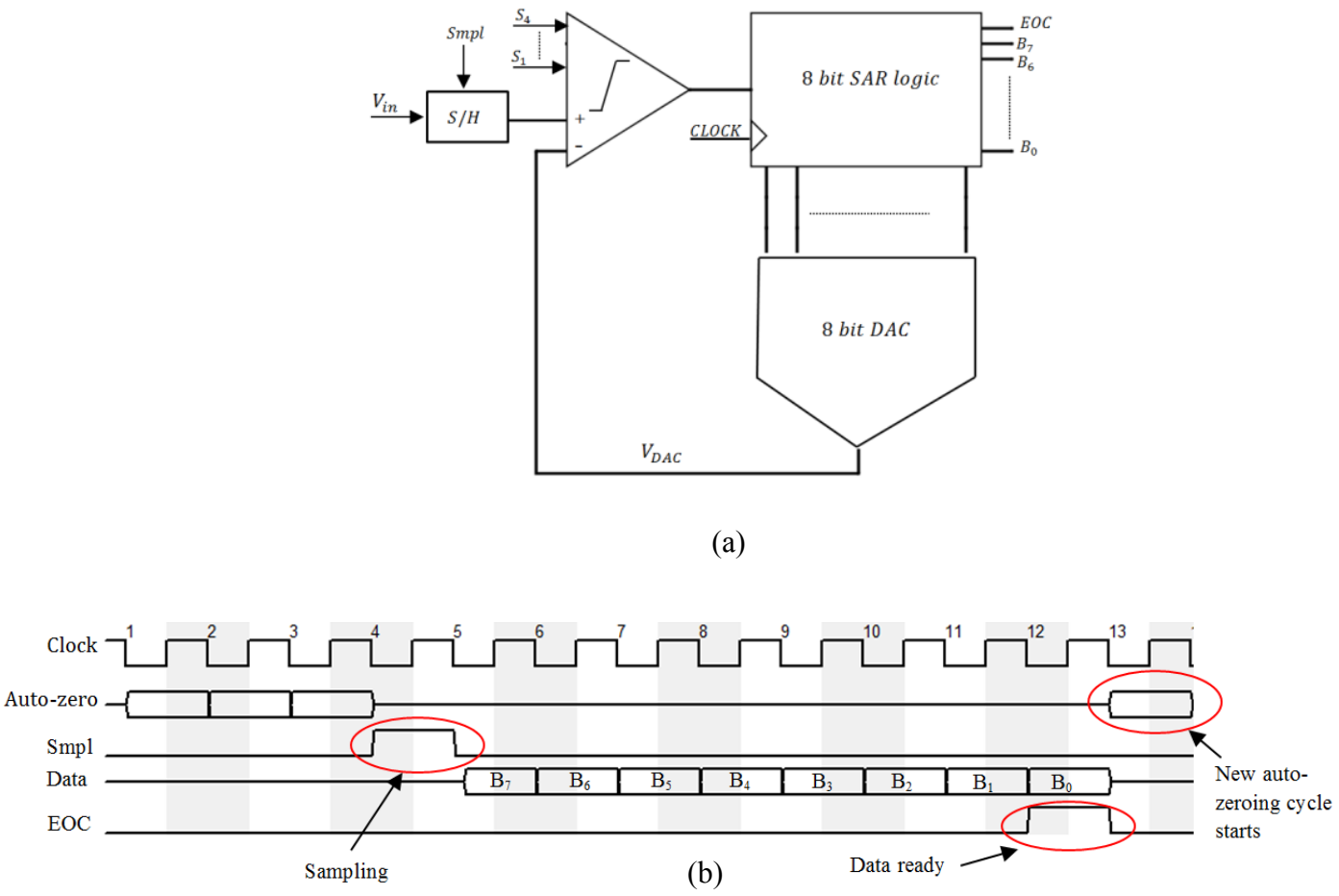


Fig. 6.2. (a) SAR ADC circuit diagram and (b) its timing diagram

The SAR ADC in the system was originally over designed for 12-bit operation by Dr.Zhou Jiang. However, only the 8 most significant bits were used. Therefore, from this point forth the ADC operation will be explained as it was an 8-bits ADC. The ADC was composed of a comparator with auto-zeroing technique to reduce its offset, an 8-bit switched capacitors DAC and SAR logic composed of shift registers. The auto-zeroing function was performed before sampling of the input, in three clock cycles' duration controlled by four clocks ($S_1 - S_4$). The ADC generates 8 bits samples every 12 clock cycles as shown in Fig. 6.2. The End of Conversion (EOC) indicates that the conversion of the current sample is done and the sample is

ready to be read on the falling edge of the EOC signal. The ADC's sampling frequency is 1/12 of the clock's sampling. A 120KHz clock frequency was used to produce the 10KHz ADC's sampling frequency.

6.2 Transmitter

An LC voltage controlled oscillator (VCO) was fabricated on chip and utilized as data transmitter. A cross coupled CMOS VCO topology was used to implement the transmitter as shown in Fig. 6.3.

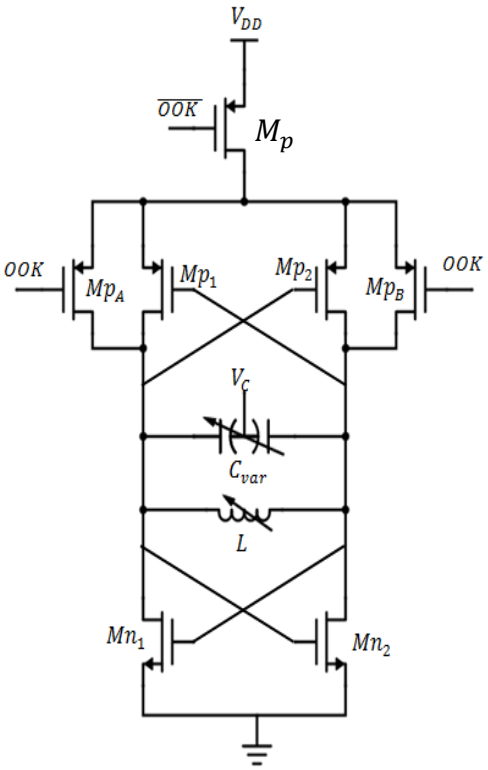


Fig. 6.3. Cross coupled CMOS controlled oscillator

The cross coupled CMOS VCO offers advantages in terms of noise performance and power consumption compared to other topologies (such as NMOS only VCO) [2]. The transmission of data was done via On-Off keying (OOK) scheme. A serial digital data input turned the oscillator on whenever it was at a high voltage level (logic level "1") by turning the top transistor M_p ON. M_p serves as a biasing current source and was designed as a long device to achieve a high output resistance. Transistors Mp_A and Mp_B were used to shut the oscillator down at a quicker rate and

thus maintain a similar rise and fall times of oscillations. A loop coil inductor was used as an antenna for transmission. Its inductance was related to its radius and thickness as [3]:

$$L \approx \mu_0 r[ln(8r/t) - 2] \tag{6.1}$$

Where *r* is the radius of the loop, *t* is the thickness of the loop's coil and μ_0 is the permeability of free space. The voltage controlled capacitors were implemented using six rows of varactors. The frequency of oscillation could be controlled by controlling the bias voltage of the varactor diodes. The operation of the circuit was extensively analysed in [2] where it was shown that in order for the VCO to oscillate, then the following condition must be satisfied:

$$G_{m-MOS} > G_{tank} \tag{6.2}$$

Where G_{m-MOS} is the transconductance of the MOS devices, which can be approximated to be equal to the transconductance of the NMOS or PMOS device (assuming equal g_m for the NMOS and PMOS device) and G_{tank} is the total conductance of the tank's resistive parasitics. The tank and its resistive parasitics can be drawn as shown in Fig. 6.4 and transformed to a parallel representation [4]:

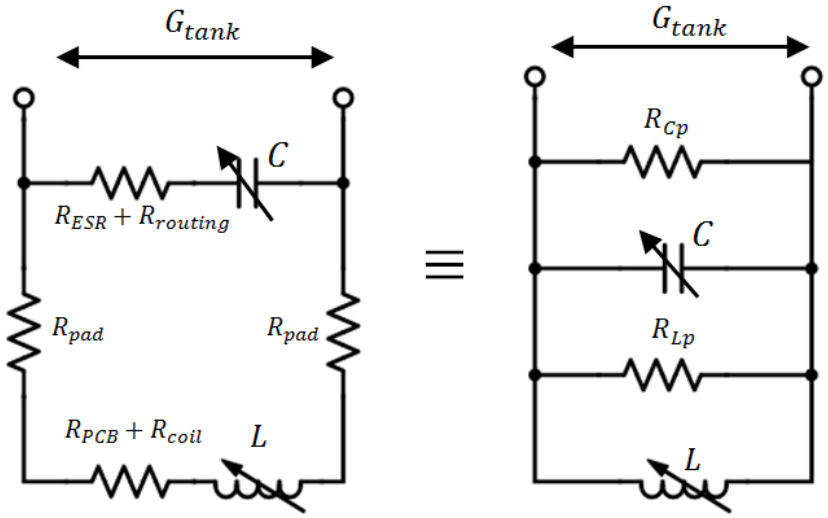


Fig. 6.4. Tank series parasitics and its parallel transformation

This parallel transformation allows the tank losses to be calculated as:

$$G_{tank} = G_{Cp} + G_{Lp} \tag{6.3}$$

where: $G_{Lp} = \frac{\left(2R_{pad} + R_{PCB} + R_{coil}\right)}{\omega^2 L^2}$ and $G_{Cp} = \omega^2 C^2 \left(R_{routing} + R_{ESR}\right)$

The resistances R_{pad} , R_{PCB} and R_{coil} are the output pad's parasitic resistance, the chip-to-PCB routing's resistance and the inductor loop coil resistance, respectively. $R_{routing}$ and R_{ESR} are the total parasitic resistances of the routing metal in the circuit's layout and the capacitor's effective series resistances (ESR), respectively. The inductor and capacitor reactances are equal at the oscillation frequency and hence (6.3) reduces to:

$$G_{tank} = \omega^2 C^2 \left(R_{routing} + R_{ESR+} + 2R_{pad} + R_{PCB} + R_{coil}\right) = \omega^2 C^2 R_T \qquad (6.4)$$

The operating transmission frequency for the CC2500 transceiver module is between 2.4 GHz and 2.4835GHz. The optimum antenna coil radius for maximum far field power transfer is between 7mm-5mm for transmission frequency between 2.4GHz-2.484GHz respectively [5]. The tank's capacitor was set to 200fF, which required an inductor value between 22nH-20.5nH to get the required transmission frequency range of the CC2500 module. This could be achieved by a 6mm coil radius with 0.5mm thickness. The coil radius could be adjusted slightly to account for any change in the capacitor's value due to parasitic capacitances. It was estimated that the maximum total parasitic resistance (R_T) added from the layout routing, output pads and from the wire-bonding of the IC to the PCB was about 1.8Ω. An overdesigning factor of 5 was implemented to put the maximum worst case value of G_{tank} at around 83μS.

6.3 PISO digital block

The PISO digital block was composed of a set of shift registers that were designed from the transistor level in cadence environment using VHDL. The block received 8-bits parallel input from the ADC, formatted them in data packets and then output serially to the transmitter. The data packets are in a format that was compatible with the CC2500 transceiver. This is illustrated in Fig. 6.5 [6].

1. The first $8 \times n$ bits are the "*Preamble bits*". This is the start code of each packet telling the receiver that transmission from the device is about to start. *n* is a number defined by the protocol which is either 2 or 4.

2. The "*Sync word*" is fixed for each packet and is the specific ID for the type of receiver used. It tells the receiver to accept this packet if it matches its general ID.
3. The "*Length field*" is set to the decimal representation of the number of bytes in the packet. In this case, the packet starts from the length field and has 53 bytes. Hence the length field is set to 00110101, which equals 53 in decimals.
4. The "*Address field*" is the ID of that specific receiver. For example for the packet to be received by a specific receiver the address field of the packet must match the receiver one. In order to receive the packet by another receiver the address field has to change to match the other receiver address ID.
5. The "*Data field"* consists of 3 bytes counter and 46 bytes data field. The 3 bytes counter counts the number of packets that is being transmitted. The 46-byte data field are 46 ADC's samples, where each sample represents 1-byte of data.
6. The "*CRC-16"* is a method used to check if data is changed or corrupted while being transmitted. There were three options: 1) To turn the CRC OFF; 2) To turn the CRC on; 3) To use a summation method that mathematically adds the packet bits, starting from the length field, and stores the result in the CRC section. The third option was chosen. The PISO block would add the packet bits, and the receiver would check if the sum after receiving the packets was identical to the sum that was calculated prior to sending them (i.e. 16-bit CRC). If both were identical the receiver would store the packet; otherwise it would discard it.

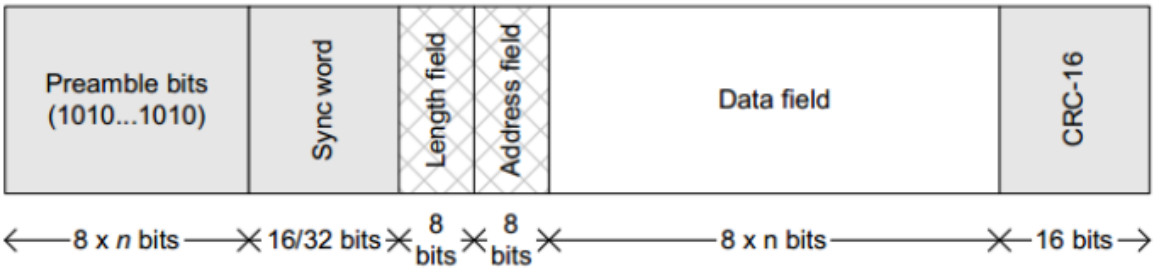


Fig. 6.5: Data package format compatible with the CC2500 tranreceiver [6]

6.4 Full System Testing

The full system was fabricated in AMS 0.18µm 6-metal layer technology. Different layout techniques such as common centroid, inter-digitization, same orientation devices and dummy devices were used to improve the matching between different devices (such as input differential

pairs and current mirrors). Grounded metal tracks were placed between analogue signals and any nearby digital signal to reduce interference and cross-talk. A picture of the full system's layout and a microphotograph of the chip are shown in Fig. 6.6 and Fig. 6.7 respectively.

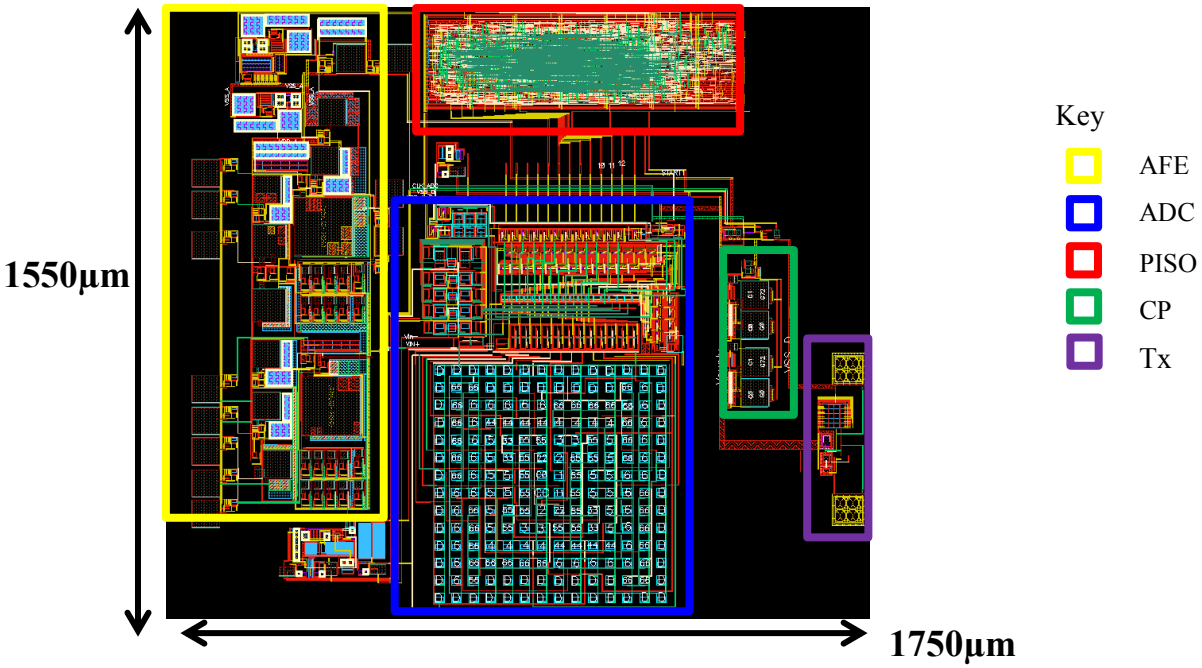


Fig. 6.6. Layout of the full system

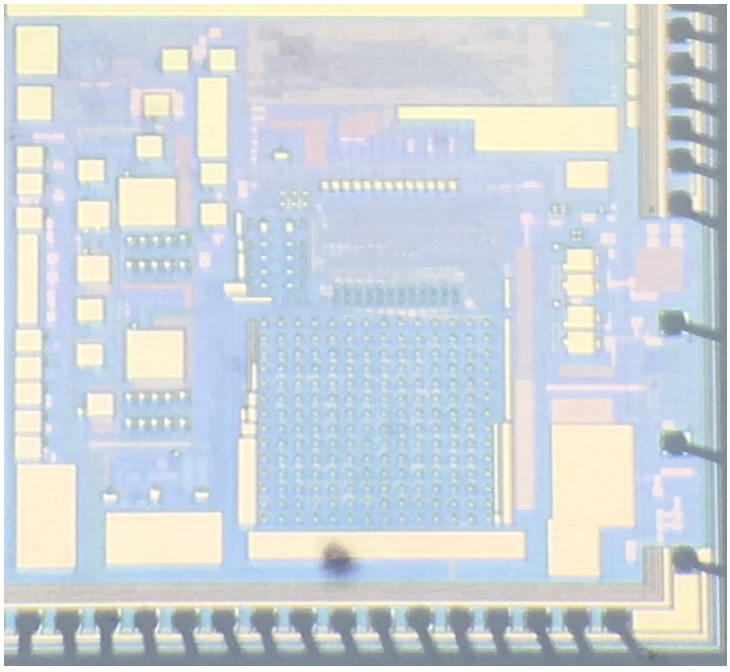


Fig. 6.7. Microphotograph of the chip

In order to test the transmitter of the system, the chip had to be wire-bonded directly on a custom made PCB without any packaging. This was crucial because the wire bonding method adds the least amount of parasitics (capacitive and resistive) from the chip's pad to the coil, compared to Through-Hole mount package. One packaging method that could have been used instead of wire-bonding was to the surface mount package. However this would result in a bigger overall system, compared to the wire-bonding method and hence it was not used. Two PCBs were made, one for testing the functionality of the chip and one for the final system. Their pictures are shown in Fig. 6.8.

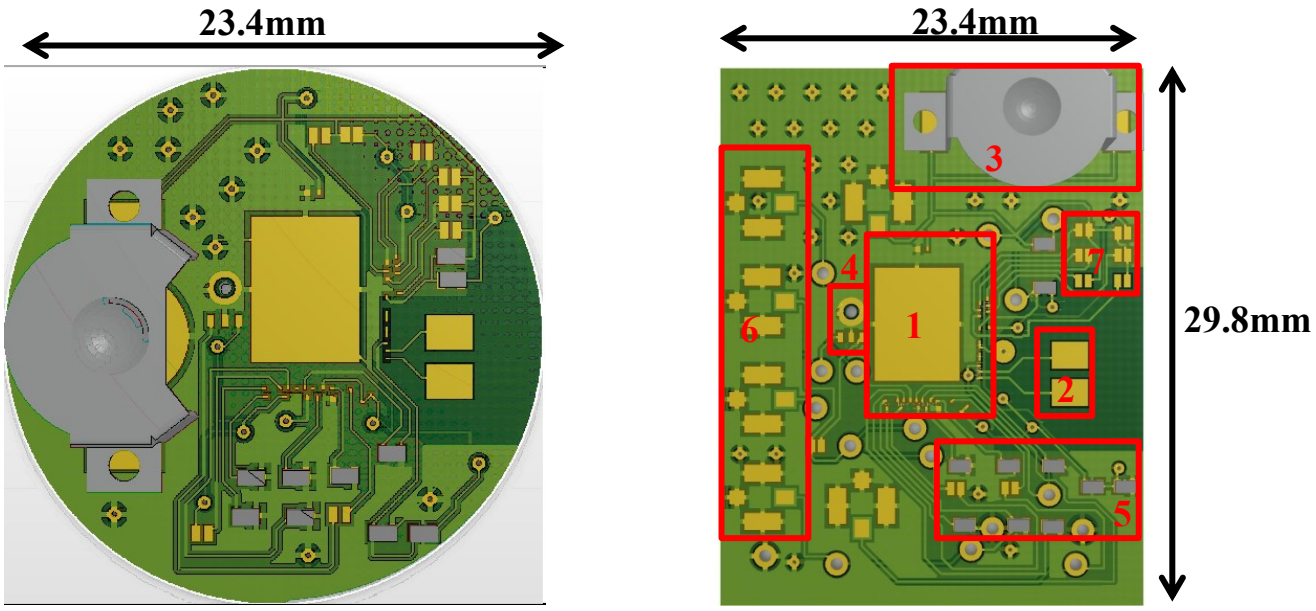


Fig. 6.8. (a) Final system PCB where all the components are assembled on. (b) Testing PCB

The PCb tracks were carefully laid out using minimum area teacks to reduce the parasitic capacitance, espeically the tracks that connect to the antenna pads. The components labels in Fig. 6.8 (b) are as follows: 1- Chip's footprint where it was wire-bonded; 2- Antenna pads; 3- Battery; 4- Microphone; 5- Off-chip capacitors and resistors; 6-N.FL connector footprint; and 7- Solder bridges to connect control signals to different voltages.

For testing purposes, the chip was initially powered from a 1.3V supply voltage using Keithley 2602 Source. The full system consumed a total current of 430µA. Hence the total power

consumption was 560µW. The breakdown of the power consumption of individual blocks is shown in the pie chart in Fig. 6.9.

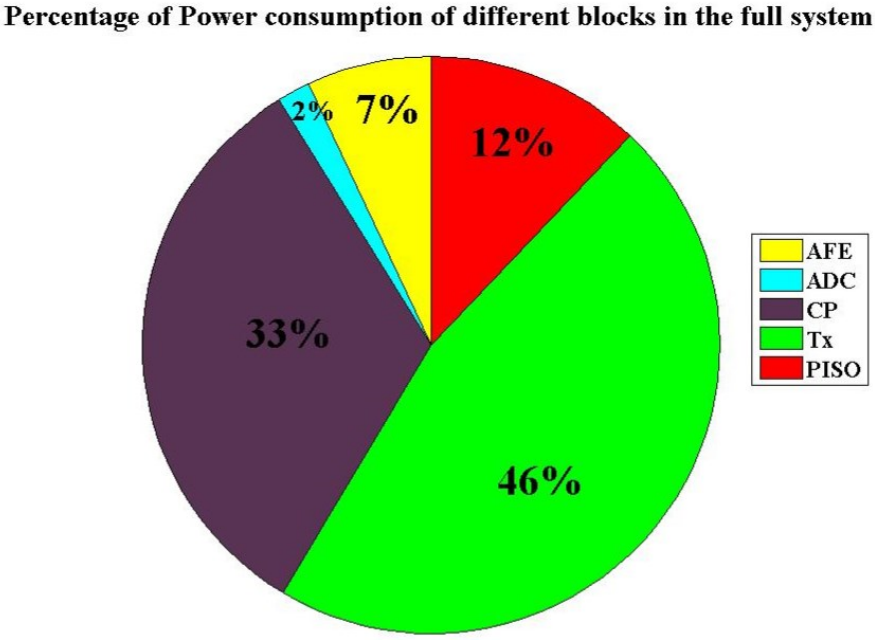


Fig. 6.9. Pie chart showing the percentage of the power consumption of different blocks in the full system

The AFE, ADC, CP, transmitter and PISO block consumed a current of 30µA, 8µA, 140µA, 52 µA and 200µA, respectively. The speech elimination circuit was not included because its current was negligible (350nA). Lab measurements showed that the system could continuously run on a brand new P13 Zinc air battery for more than 2 weeks. During these 2 weeks operation, the P13 battery voltage dropped from 1.4V to 1.28V.

6.4.1 AFE

The AFE was tested at a 1V supply voltage provided by the regulator. The PSR of the AFE when connected to the regulator was tested using the spectrum analyser. This PSR is the addition of the regulator and AFE logarithmic PSRs. The chip was supplied with a 1.3V DC voltage with 50mV peak-peak sinusoidal that swept from 100 Hz – 100 KHz. The PSR is shown in Fig. 6.10. It can be seen that it is fixed at -49dB for the pass-band frequency of the filter (150Hz - 1KHz), and then rolls down. This attenuates any ripples that appear on the chip's main power line within the pass-band.

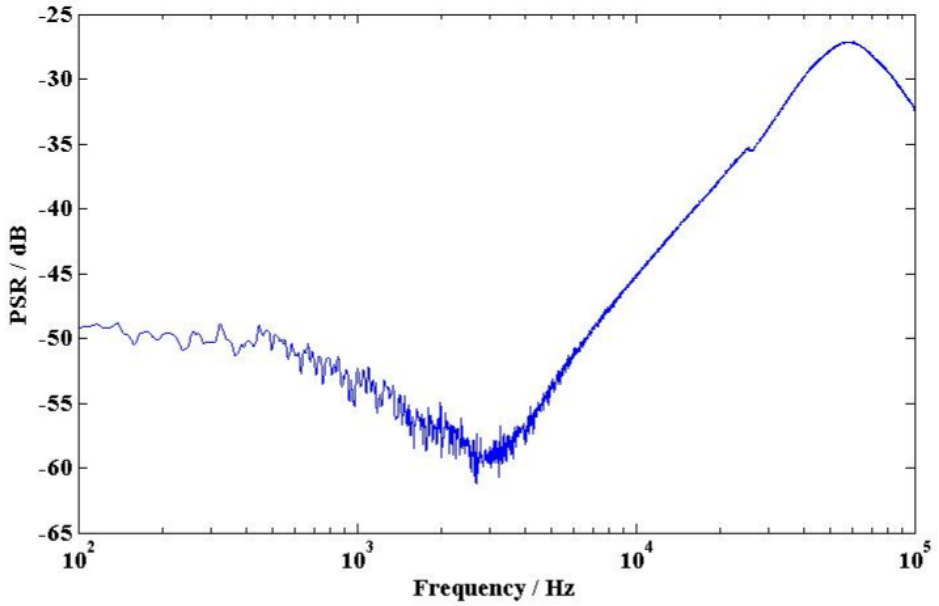


Fig. 6.10. Measured PSR of the AFE when powered from the regulator

The second test carried out was the frequency response of the AFE. The results are shown in Fig. 6.11

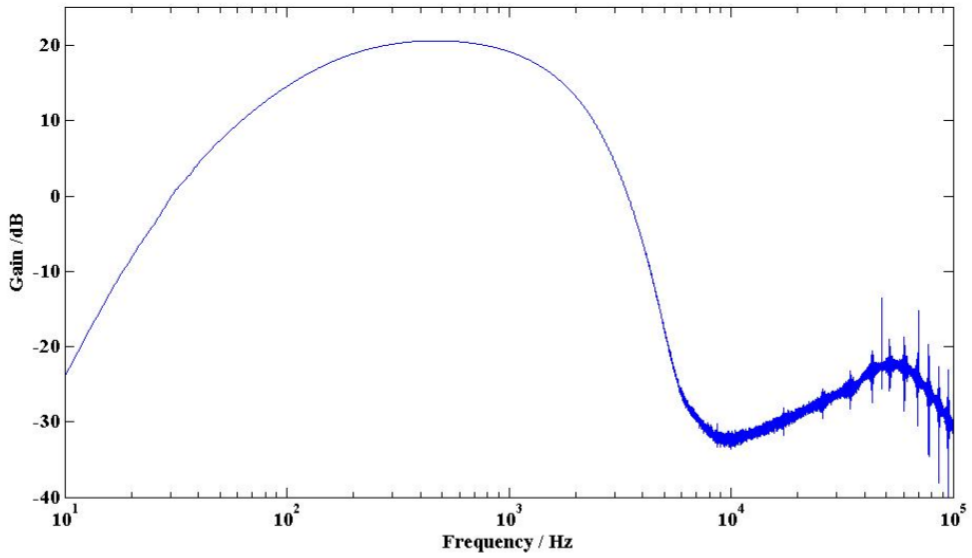


Fig. 6.11. Measured frequency response of the AFE

The mid-band gain was 20.2 dB and the 3-dB bandwidth was from 155Hz-1.26 KHz. The 50dB attenuation relative to the pass-band occurred at 7.65 KHz, which was within the Monte-Carlo simulations range results shown in Chapter 5, Section 5.2.

The measured noise spectrum density at the AFE's output from 10Hz-10KHz is shown in Fig. 6.12. The output noise was calculated by integrating the in-band noise from 150Hz–1KHz, which results in an output noise of 490.16μV_{RMS} as can be seen in Fig. 6.12. The input referred noise in the pass-band is simply the output noise divide by the pass-band gain. This was equal to 49.2μV_{RMS}.

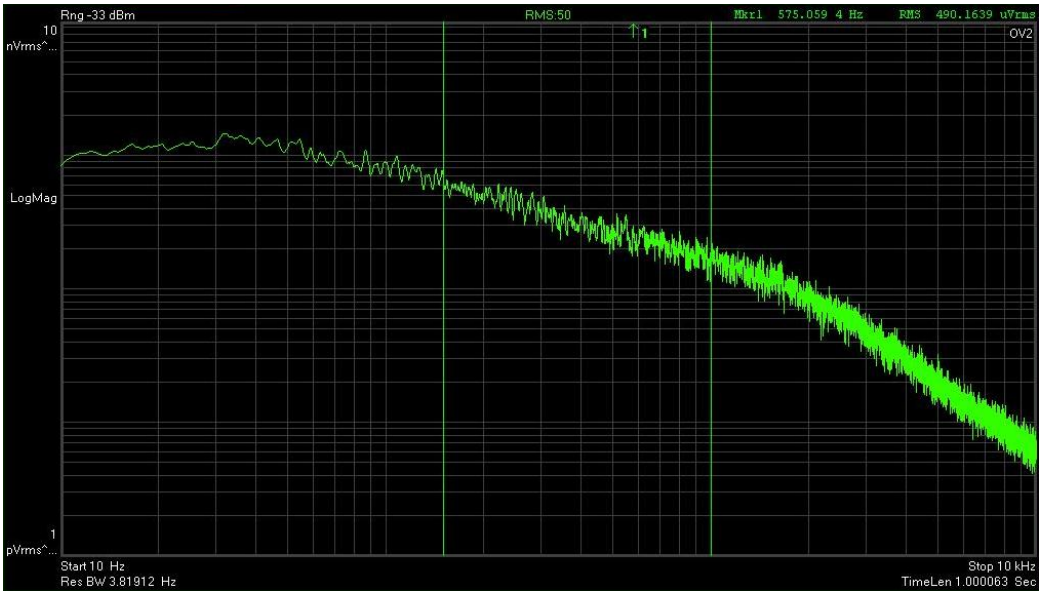


Fig. 6.12: Measured AFE's output noise PSD

A sinusoidal input at 500Hz with 65mV peak-peak amplitude was applied to the AFE's input to measure the total harmonic distortion (THD). The frequency spectrum at the output is shown in Fig. 6.13. The fundamental signal at 500Hz had an amplitude of -12.8dB_{RMS} and the second and third harmonics at -45dB_{RMS} and -67.2dB_{RMS}, respecitvely. The THD of the AFE at 65mV peak-peak input was 2.4%. This is the maximum value of the THD. The AFE will exhibit this distortion only when the subject wearing the device snores because the maximum input amplitude during snoring is 65mV peak-peak. During normal breathing, which is the majority of the time, the input voltage has an amplitude of less than 40mV peak-peak and the AFE exhibits a THD of 1.2%.

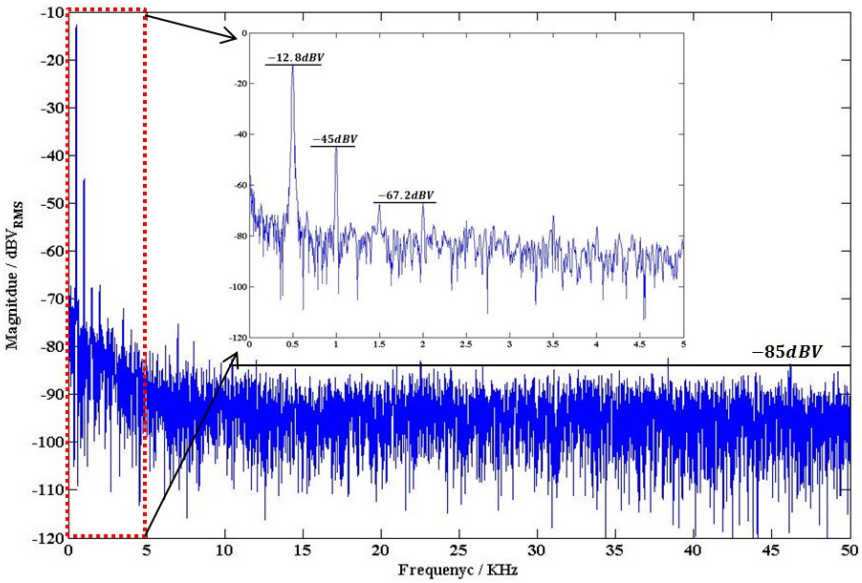


Fig. 6.13. The spectrum of the AFE's output with a 500Hz with 65mV peak-peak sinusoidal input.

The microphone was connected to the AFE's input to test if the system could detect physiological signals. The first test carried out was to check if heart signals could be detected by the device. A subject was asked to hold his breathing for 10 seconds for this test. The result at the AFE's output is illustrated in Fig. 6.14.

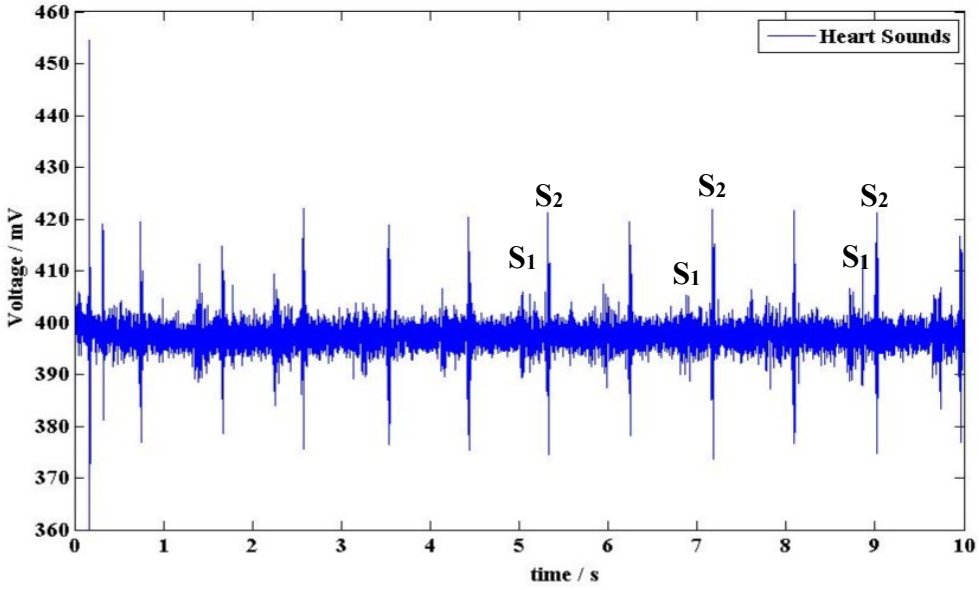


Fig. 6.14. Output signal at the AFE's output when the microphone is connected to the system and breathing is held for 10 seconds

The figure clearly shows that heart sounds S_1 and S_2 are detected by the device. The S_2 sounds have an amplitude of 40mV peak-peak while the S_1 sounds have an amplitude of 12mV peak-peak. To see a clearer heart sound signal, the signal in Fig. 6.14 was passed through a 3rd order low-pass transfer function with a cut-off frequency of 100Hz using MATLAB. The result is shown in Fig. 6.15.

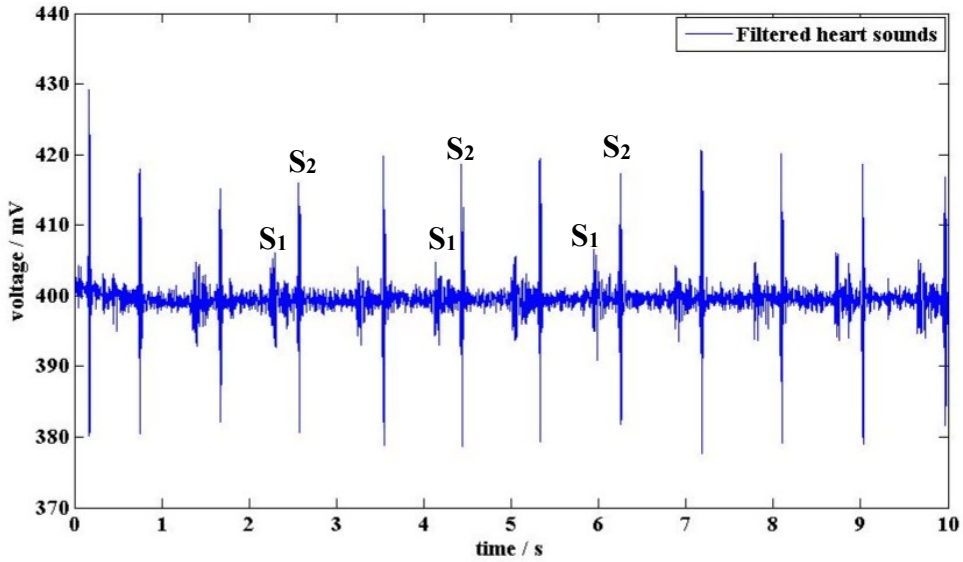


Fig. 6.15. Filtered signal in Fig. 6.14 using a 3rd order low pass filter with 100Hz cut-off frequency

The heart sounds in the filtered signal in Fig. 6.15 are much clearer than in Fig. 6.14. The function of the low pass filter can be implemented by the algorithm that processes the signal. The point of adding a low-pass filter here was simply to show that heart sounds can be clearly detected by the system.

The second test carried out was the detection of breathing signal at rest. The same test subject was asked to breath for 10 seconds at rest. The signal at the AFE's output is shown in Fig. 6.16. Breathing signals have 130mV peak-peak magnitude and the subject's breathing rate equalled 17 breaths per minute. The signal shown in Fig. 6.16 is considered normal breathing because the subject was at rest. During physical activity, the breathing signal magnitude can reach up to 400mV peak-peak with a rate of 30 breaths per minute. This is shown in Fig. 6.17, which was taken from the same test subject after he completed 1 minute of jumping.

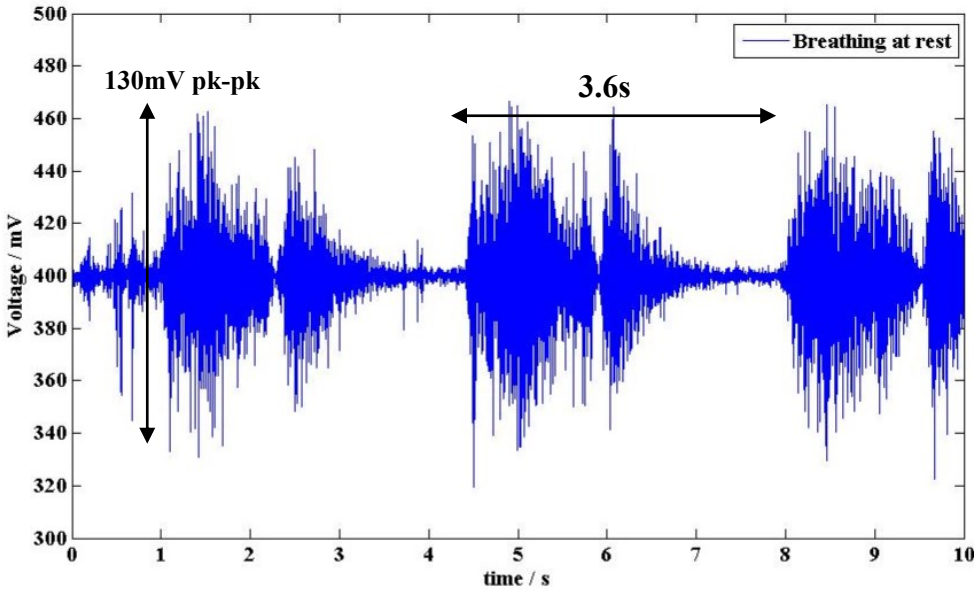


Fig. 6.16. Breathing sound at rest detected at the AFE's output

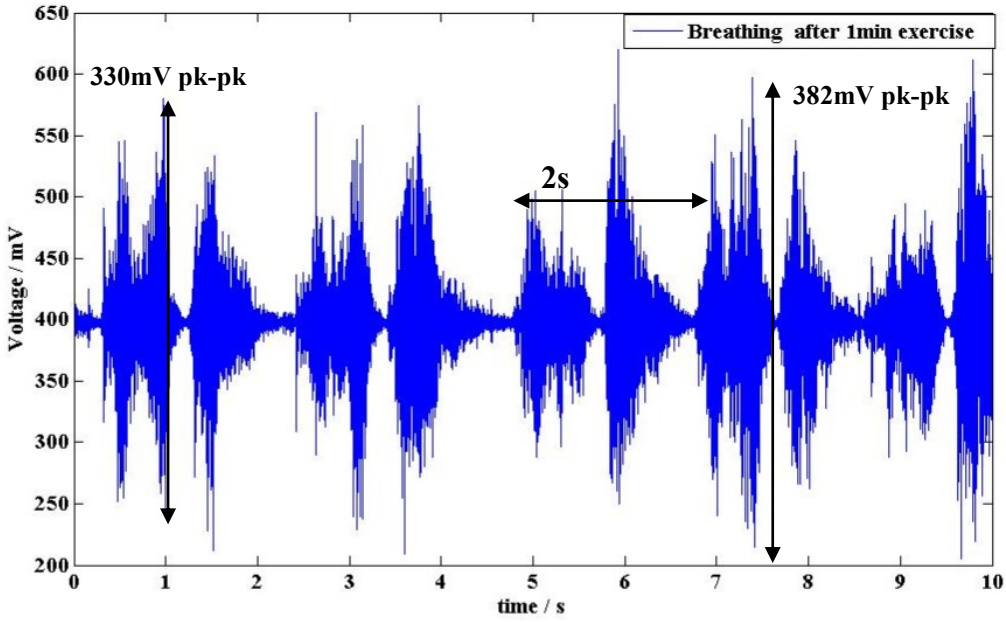


Fig. 6.17 Breathing sounds at after one minute jumping detected at the AFE's output

Lastly, the capability of the device to capture snoring sound without saturating the ADC was tested. The test subject was asked to deliberately snore for 10 seconds and the waveform at the AFE's output was plotted in Fig. 6.18. Snoring sounds can reach amplitudes as high as 630mV peak-peak after amplification by 20dB. They are within the ADC's input range and will not saturate it. This ensures that the device can be used to acquire snoring sounds. If the gain was

22dB, then there would be a very high chance that snoring sounds would saturate the ADC causing a loss of signal.

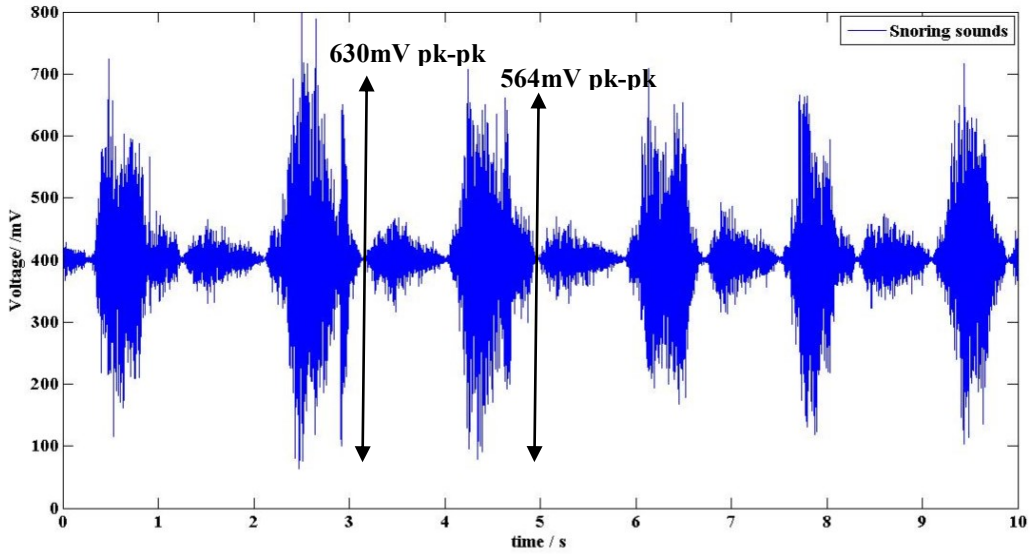


Fig. 6.18. Snoring sounds detected at the AFE's output

6.4.2 Wireless link testing

The transmitter was powered directly from the chip's supply voltage, which ranges from 1.4V-1.2V. The antenna was implemented as a single loop coil with a diameter of 6mm. To test the functionality of the transmitter and, for the sake of simplicity and since the development of the CC2500 receiver module was out of the scope of this thesis, the receiver was implemented using a GNU software define radio instead of the CC2500 module. The code for the GNU radio was already written by Dr.Stuart Bowyer and hence only a minor modification was required. The packet format was compatible with the CC2500 module and the latter could be coded and used in future work. The GNU software radio was implemented on a computer connected to an antenna. The antenna received the RF signal from the transmitter and the GNU radio decoded that signals. Two codes were written in the GNU radio software. The first one displays the spectrum of the received signal in the frequency domain as shown in Fig. 6.19 and the second code displays the received raw data packet as shown in Fig. 6.20. The transmission frequency was at 2483.32 MHz and the received power was -39dB when the transmitter was placed 15cm away from the reciever. The received raw data packets are shown in Fig. 6.20. A zoomed view on an individual packet to show the individual recived bits is illustrated in Fig. 6.21. Each packet of data

contains 46×8-bits (46 bytes) of data sampled at 10 KHz. This implies that each two consecutive bytes represent 0.1ms of data and hence each whole received packet represents 4.5ms of data.

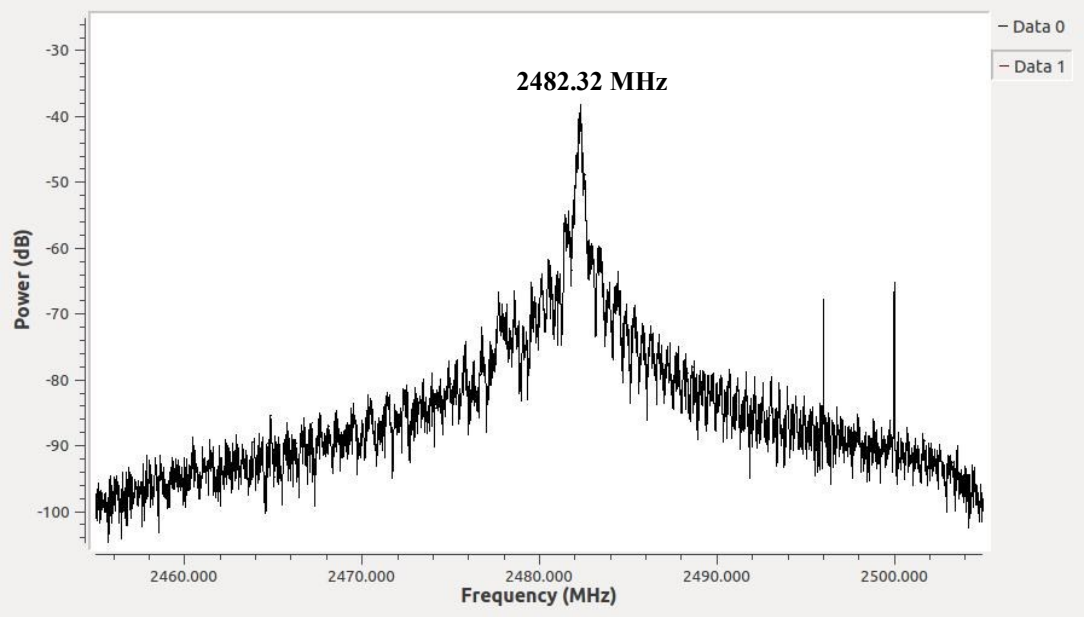


Fig. 6.19. Spectrum of the received signal at the receiver

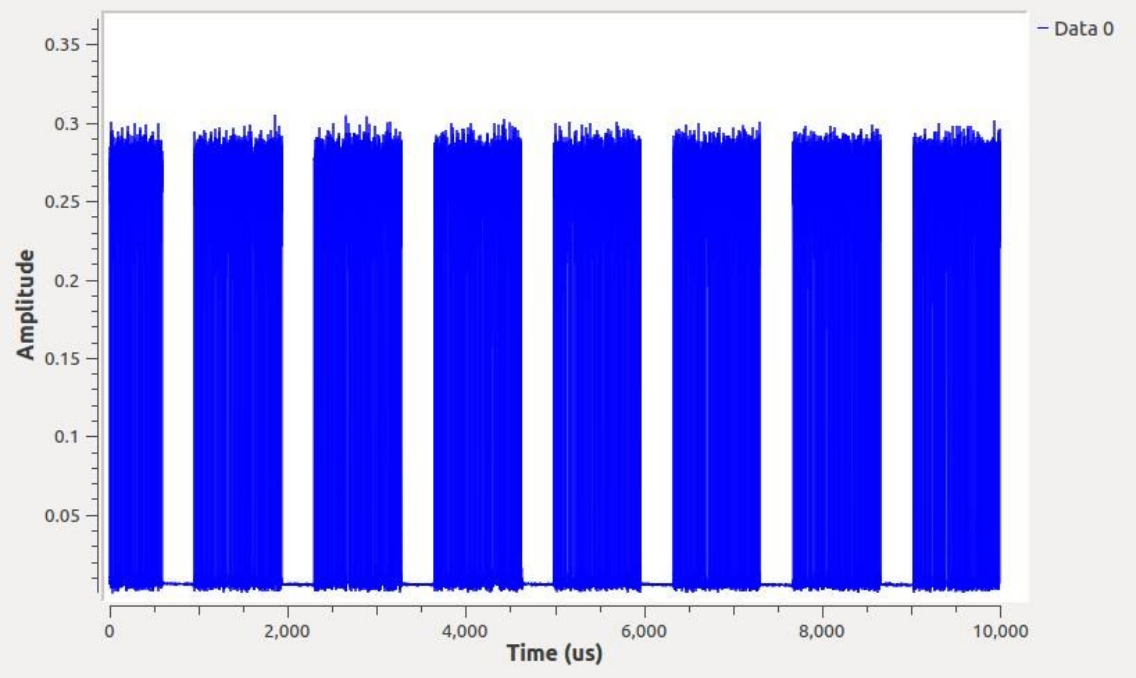


Fig. 6.20. Received raw data packets

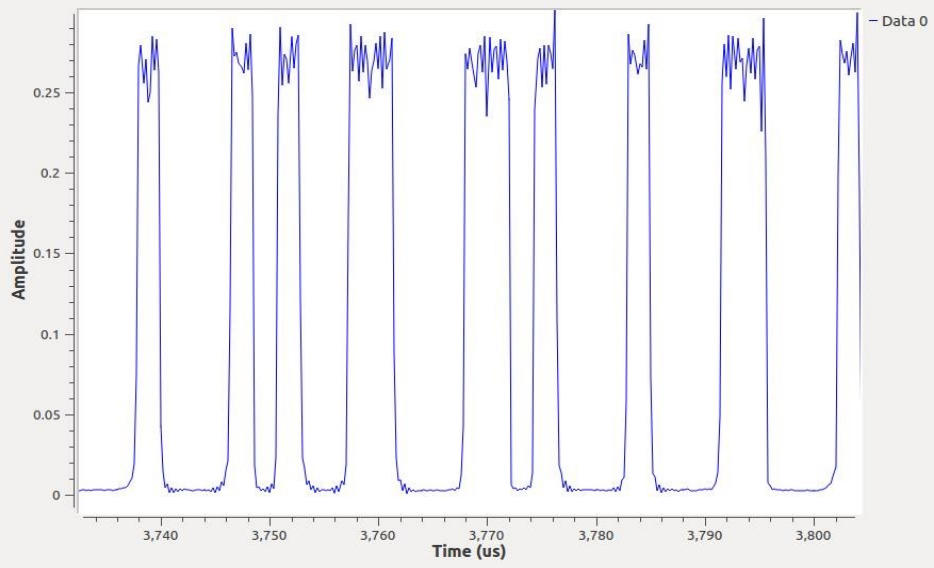


Fig. 6.21. Zoomed view on a received packet

A 500Hz sinusoidal signal with 10mV peak-peak was applied to the system. The transmitted packets were received by the receiver and then uploaded into MATLAB to decode and recover the data in order to test the full functionality of the system. As explained earlier, each packet of data represented 4.5ms of real time data and hence 2 packets were decoded to obtain 9ms of data as shown in Fig. 6.22.

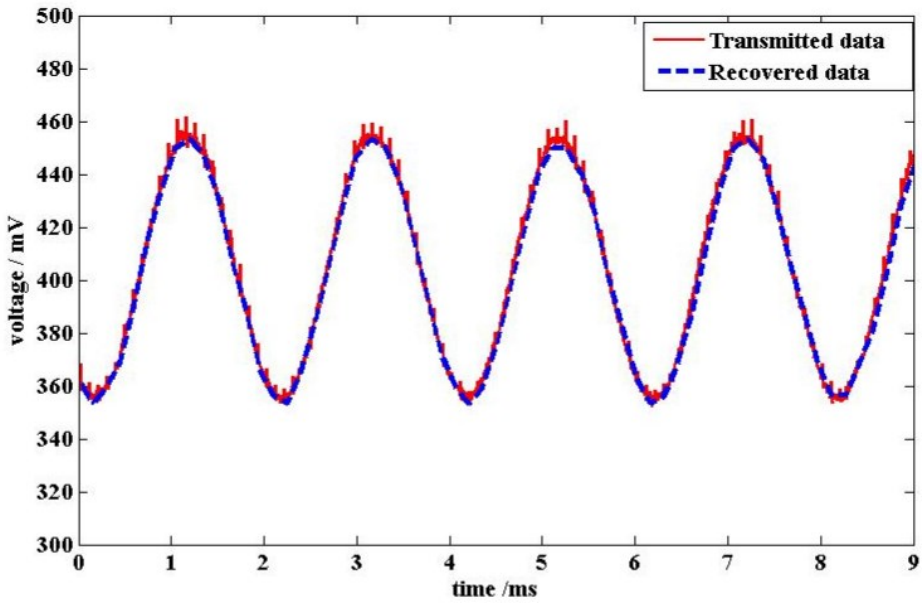


Fig. 6.22. Comparison between the transmitted and recovered 500Hz sinusoidal signal with 10mV peak-peak magnitude

It can be seen how the transmitted and recovered data were identical. The red spikes that can be noted on the transmitted data are due to the data being sampled and switched to a sampling capacitor. The percentage error between the transmitted and recovered signal is plotted in Fig. 6.23 and it shows a maximum error of less than 0.7%.

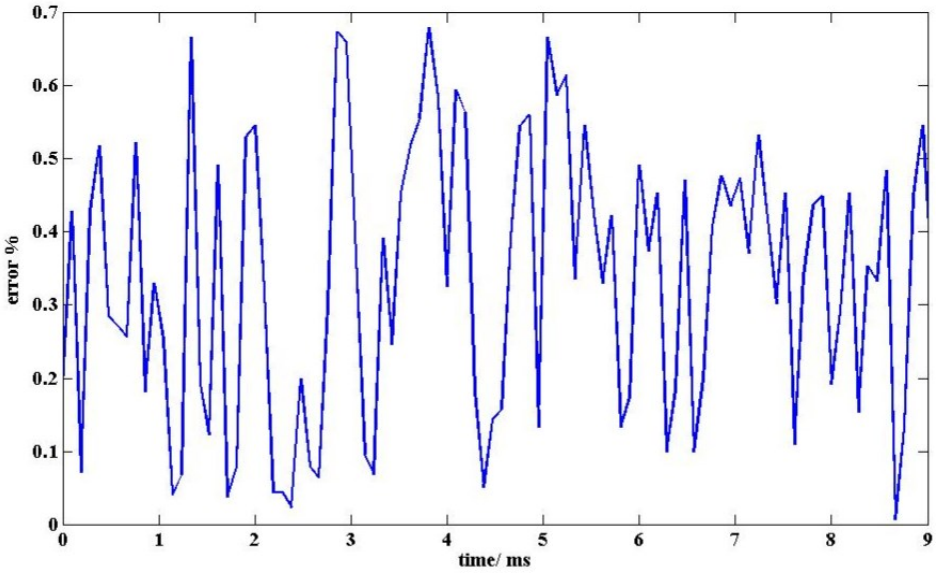


Fig. 6.23. Percentage error between the transmitted and recovered signal in Fig. 6.22

To verify the full system functionality for a range of input frequencies, a 50mv peak-peak sinusoidal sweep from 100Hz-1.5KHz was applied to the system. The transmitted packets were received by the receiver and then uploaded into MATLAB to decode and recover the data. Seven packets of data were decoded to obtain 31.5ms of data. This is shown in the blue graph in Fig. 6.24. The solid red graph represents the signal at the output of the AFE, which was digitized, formatted and then transmitted. The broken blue line represents the recovered data. A very good match can be seen between the transmitted and received data, indicating a good functionality of the full system. The percentage error between the transmitted and recovered signal is plotted in Fig. 6.25 and it shows a maximum error of less than 0.5%.

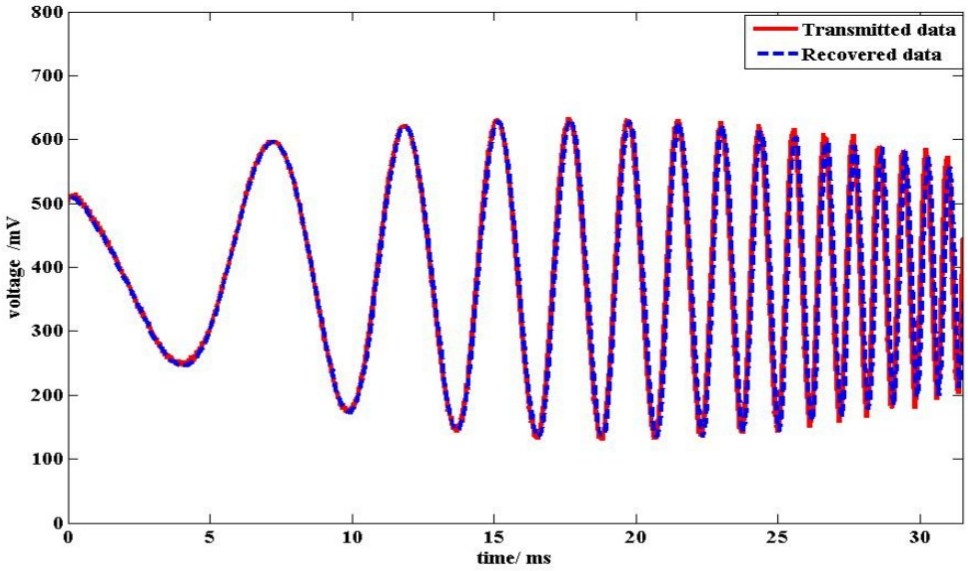


Fig. 6.24. Comparison between the transmitted and recovered sinusoidal sweep from 100 Hz-1.5KHz with 50mV peak-peak magnitude

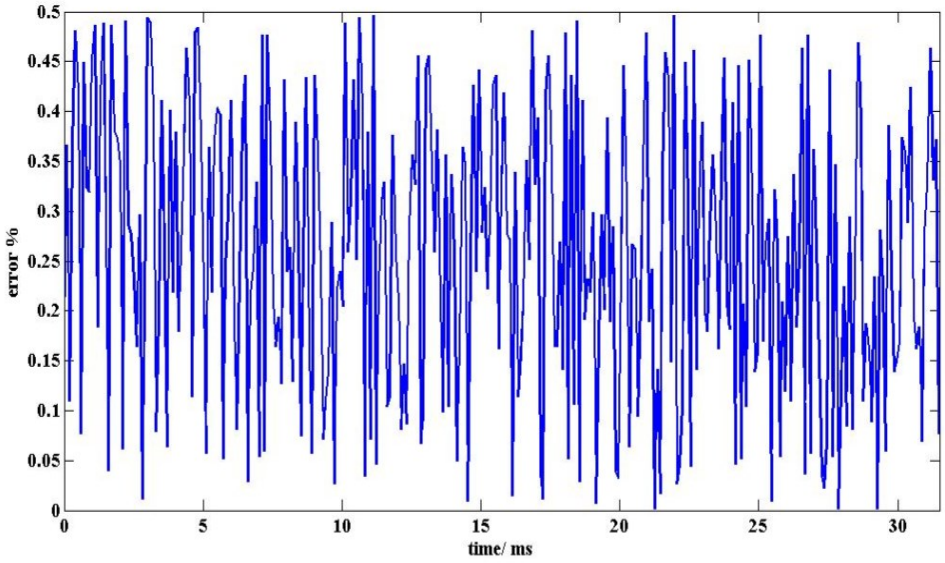


Fig. 6.25. Percentage error between the transmitted and recovered signal in in Fig. 6.24

6.5 Conclusion

This chapter has described the ADC architecture and the implementation of the transmitter, together with the measurements results of the full integrated breathing monitoring system. The final system's PCB had a diameter of 23mm, and the system and consumed 560µW of power at 1.3V supply voltage including the microphone. Lab measurements showed that the system can

operate continuously for more than two weeks with a 0.83g P13 zinc air battery. Testing the functionality of the system showed good results and great potential for realising a complete remote diagnostic process.

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Chapter 7: Conclusion and future work

7.1 Conclusions

This thesis has discussed several chronic respiratory and cardiac diseases and exposed the effects of such diseases on society and on patients. The traditional diagnosis methods for these diseases and their limitations were discussed. It was shown that there is a great demand for an affordable wearable diagnostic process that could, potentially, remotely diagnose and follow these chronic diseases. Such a remote diagnostic process would reduce the impact of the diseases on patients' lives and would decrease the diagnostic costs, which would in turn reduce the financial burden on the economy and the personal burden on individuals.

A remote diagnostic system would be composed of a wearable device to acquire physiological signals and algorithms that work on this data to extract disease related parameters that are useful in the diagnostic process. After conducting a literature research, it was found that there is a lot of work in the literature that describe the implementation of algorithms to extract disease related parameters form acoustic cardiac and respiratory signals. However there is lack of a true low-power wearable system to acquire these signals. In this thesis, the concept of a low-power wearable system that acquires cardiorespiratory sounds was proposed. The low power system is composed of two parts: a low-power wearable device mounted on the neck and an intermediate RF module that can be placed in the pocket. The wearable device transmits data to the intermediate RF module, which in turn transmits these data to a server where different algorithms can process the signals. This allows the wearable device on the neck to be designed with low power.

The majority of this thesis has presented the analysis, design, implementation and testing of a custom integrated circuit which, together with a low power microphone, form a low-power wearable device to sense and transmit signals, ideally from the neck. The full system consists of a charge pump, analogue front end, ADC, digital block and a transmitter. The system was fabricated at the transistor level in AMS 0.18µm 6M technology. The final system was wire-bonded to a custom made miniature PCB that had a diameter of 23mm and integrated with a miniature MEMS microphone that was soldered on the same PCB as well. The system consumed a total power of 560µW from a 1.3V supply. Lab measurements

showed that the system could last on continuous operation for more than 2 weeks when using a Zinc Air P13 0.83g battery with a capacity of 310mAh. Testing the functionality of the full system proved the performance at such small power consumption. These results demonstrated that the system can have great potential for realising a complete low power diagnostic and monitoring process for chronic cardiac and respiratory diseases, combining it with diagnostic algorithms.

7.2 Future work

The device created in this thesis has showed good performance and good potential to be used in a low-power remote diagnostic process. However, some more work needs to be done before this can be realised. Firstly, the CC2500 transceiver module must be programmed to receive data from the wearable device. Secondly, the second device, which is the intermediate RF module that is placed inside the pocket, must be built and the CC2500 module and MSP430 interface must be correctly programmed as described in Chapter 2. An extra useful feature to have in the device would be a rechargeable battery with a charging circuit. This would greatly increase the convenience of the device and makes it more usable for the patients.

A more challenging future work would be to transfer the conventional wearable device to a transparent “Silicon patch”. This could be achieved if the wearable system was designed in a thin flexible CMOS technology with approximately 50μm substrate thickness. At this thickness, the silicon chip would become transparent and could be used as a silicone patch mounted on the neck. This would be very desirable because it would transfer a relatively bulky and noticeable device to a completely transparent patch that feels much better to wear. However, this would also be dependent on advances in battery technologies as a flexible battery would be required to have a fully flexible system.

Appendix 5.1

The acoustic signal can be modelled by two sinusoids waveforms with different amplitudes and frequencies as shown in Fig. A.5.1.

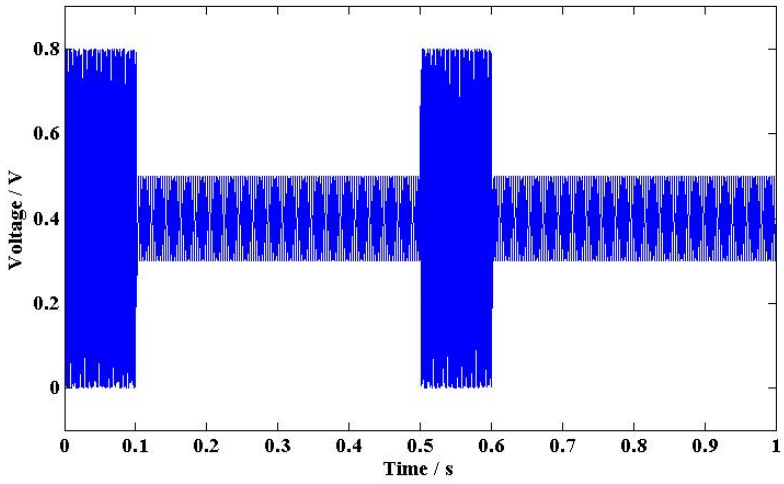


Fig. A5.1. Modeling the acoustic signal using two sinusoids with different amplitudes and frequencies

The current consumption of the envelope detector during tracking of speech is derived in the following. This result will be extended for the current consumption expression during tracking of breath signals.

Defining the speech segment in the acoustic signal as $V_S(t)$, during tracking, the output tracks the input and hence $V_S(t) = V_{out}(t)$, and a current flows through M_p to C_t and R_D. The total current that passes through M_p during the tracking of speech can be approximated as:

$$I_{Mp-S} \approx C_t \frac{dV_{out}}{dt} + \frac{V_{S_{peak}}}{R_{D_S}} \tag{A 5.1}$$

And can be averaged as:

$$I_{Mp-Avg.S} = \frac{1}{T_S}\int_0^T I_{Mp-S}\, dt = \frac{1}{T_S}\left(\left[V_{S_{peak}} - V_S(t_{start})\right] C_t + \frac{V_{S_{peak}}}{R_{D_S}} t_{0_S}\right) \tag{A 5.2}$$

Where T_S is the time between the peaks of speech signal; $V_{S_{peak}}$ is the peak voltage of speech (which is the saturated output voltage of the acoustic signal amplifier); $V_S(t_{start})$ is the voltage of speech signal when tracking starts (this is typically equal to 98% of $V_{S_{peak}}$ due to

the large RC time constant of the envelope detector); t_{0_S} is the duration of the tracking phase; and R_{D_S} is the resistance of R_D during the tracking of speech. These terms are illustrated in Fig A5.2.

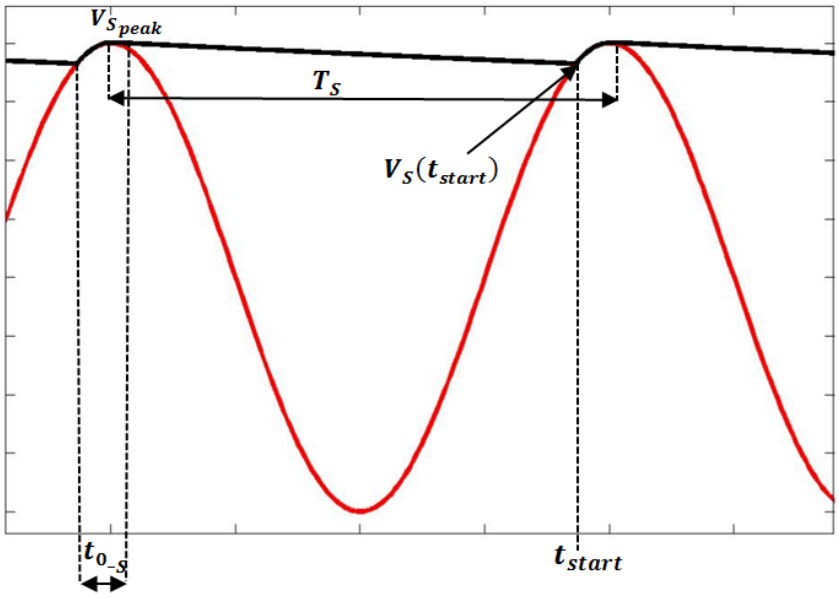


Fig. A5.2. Graph illustrating the terms in equation (A 5.2)

A similar expression can be found for the average current that passes through M_p during the tracking of breathing:

$$I_{Mp-Avg.B} = \frac{1}{T_B}\left(\left[V_{B_{peak}} - V_B(t_{start})\right] C_t + \frac{V_{B_{peak}}}{R_{D_B}} t_{0_B}\right) \quad \text{(A 5.3)}$$

The average total current that passes through M_p is:

$$I_{Mp-Avg} = K_S I_{Mp-Avg.S} + K_B I_{Mp-Avg.B} \quad \text{(A 5.4)}$$

Where K_s and K_B are the percentages of speech and breathing segments' duration in the acoustic signal respectively.

The bandwidth of the amplifier ω_a can be written as:

$$\omega_a = \frac{\lambda I_{opamp}}{4C_0} \quad \text{(A 5.5)}$$

where I_{opamp} is the opamp's biasing tail current; C_0 is the total capacitance at the opamp's output; and λ is the channel length modulation coefficient (which was assumed to be the same for P-type and N-type devices).

The Opamp's bandwidth must satisfy (5.12). Equating (5.12) with (A 5.5) and solving for I_{opamp}:

$$I_{opamp} = \frac{8C_0A_0g_m|_{max}}{\alpha\lambda C_t} \tag{A 5.6}$$

Assuming that transistor M_p operates in moderate-strong inversion with *IC>3,* its transconductance can be approximated using (5.7) as:

$$g_m|_{max} \approx \frac{I_{Mp-max}}{nV_T\sqrt{IC}} = \sqrt{C_t}\sqrt{\frac{2\beta_{Mp}\times\left(dVin/dt\right)_{max}}{n}} \tag{A 5.7}$$

Substituting (A 5.7) in (A 5.6):

$$I_{opamp} = \left(\frac{8C_0A_0}{\alpha\lambda}\sqrt{\frac{2\beta_{Mp}\left(dVin/dt\right)_{max}}{n}}\right)\sqrt{\frac{1}{C_t}} \tag{A 5.8}$$

The total power consumption of the envelope detector is:

$$P_{ED} = V_{DD}\left(I_{opamp} + I_{Mp-Avg}\right)$$

$$= V_{DD}\left\{\left(\frac{8C_0A_0}{\alpha\lambda}\sqrt{\frac{2\beta_{Mp}(dVin/dt)_{max}}{n}}\right)\sqrt{\frac{1}{C_t}} + \frac{K_S}{T_S}\left(\left[V_{S_{peak}} - V_S(t_{start})\right]\ C_t + \frac{V_{S_{peak}}}{R_{D_S}}t_{0_S}\right)\right.$$

$$\left. + \frac{K_B}{T_B}\left(\left[V_{B_{peak}} - V_B(t_{start})\right]\ C_t + \frac{V_{B_{peak}}}{R_{D_B}}t_{0_B}\right)\right\} \tag{A 5.9}$$