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A Modular Multilevel DC-DC Converter with a Compact Sub-module Stack Suited to Low Step-Ratios

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***Abstract*—The voltage ratings for dc transmission and distribution are not currently standardized because cable technology is advancing rapidly and therefore low step-ratio dc-dc converter at multi-megawatt scale is a crucial technology for combining point-to-point dc links into multi-terminal networks. This paper presents a modular multilevel dc-dc converter configuration with only a single stack of half-bridge sub-modules (SM) and a resonant tank. The power processed through the stack is a small fraction of the throughput power if the step-ratio is small ($1 - v_L/v_H$). Detailed analysis shows the required semiconductor ratings are much smaller compared to the front-to-front MMC and modular converters derived from standard dc-dc topologies. Further, the requirement for SM capacitive energy storage is also significantly less than those converters. The theoretical analysis and the operating principles have been verified by full-scale simulation examples and experiments with a down-scaled prototype. The SMs are operated with an adjustable phase-shift to create a high frequency excitation across the resonant tank for further volume reduction. The SM capacitors self-balance without the need for switching pattern adjustments and the resonant operation provides soft-switching for all power switches to increase efficiency.**

***Index Terms*—Multi-terminal dc network, medium voltage dc, modular multilevel converter, dc transformer.**

I. Introduction

THE INCREASING penetration of renewable energy in power systems has called for additional transmission and distribution and has driven the uptake of dc technology and a move from the existing point-to-point dc connections towards multi-terminal dc networks [1]–[4]. DC technology has advantages in transmission capability and footprint over traditional ac [5]–[7], but a difficulty of the dc option that must be overcome in dc networks is the size, cost and power losses incurred in the power converter needed to interface lines of unequal dc voltages. The voltage rating of dc lines are not currently standardized and technology innovation and the quest for high power transfer have led to many different voltages being used [8], [9]. Thus, there will be an essential role for dc-dc conversion equipment with a low step-ratio connected between existing dc links with similar but not identical voltages [10]–[12].

General purpose low step-ratio dc-dc conversion has been investigated for decades with the objective of increasing power efficiency and power density. The classic dual-active-bridge (DAB) converter [13] and *LLC* resonant circuits [14], [15] are the popular solutions for various power supply applications. The single full-bridge or half-bridge design and the use of high switching frequency are well suited to low voltage levels but this does not scale to medium- or high-voltage applications. The use of multiple modules in series and parallel combinations can address this limitation to an extent [16], but the approach may lead to complicated voltage and current balancing issues between the many modules needed at high-power conversion [17]. Further, the structure does not easily accommodate redundancy so fault-tolerant operation is another challenge in practice [18]. The modular multilevel converter (MMC) scales very well to medium- or high-voltage for high-power conversion and can readily include redundancy [19]. The original ac-dc MMC technology has been widely used for voltage-source-converter (VSC) dc transmission and distribution [20], but it cannot be directly used for dc-dc conversion. It needs reconfiguration and adaption to play the role of a low step-ratio dc transformer between dc terminals of different voltages.

The front-to-front configuration of two MMCs (FtF-MMC) and its extensions [21], [22] are popular solutions. Not only do they inherit all the benefits of the conventional ac-dc MMC they can also block the propagation of dc fault current from either side to the other. However, the full throughput power is processed by the stacks of two MMCs resulting in relatively high power losses. The configuration is also bulky because there are 12 sub-module (SM) stacks in the 3-phase version (two stacks in each phase of each converter) or 8 stacks in the single-phase version. Each stack requires a large volume of capacitive energy storage and needs isolation clearances to neighboring stacks and the valve hall walls. Thus, the volume density is poor and the cost will be high for installation on offshore platforms or in substations where land is expensive. The high-frequency-link dc transformers presented in [23], [24] combine the MMC and the DAB topology. They provide the fault-tolerance missing from the traditional modular DAB circuits and also avoid the single large low-frequency transformer of the FtF-MMC. However, the power losses of these converters may have some disadvantages and there are practical challenges in the isolation for the large number of module transformers. The direct chain-link modular multilevel dc converter was proposed and developed [25]–[28] to increase the power device utilization and improve the power conversion efficiency. A direct dc-dc voltage transformation is achieved without an intermediate ac stage and the SM stacks are arranged to form part of both the low-voltage and high-voltage current path. The difficulties that arise are management of dc faults [25], [26] and the practical design of the large inductances [27], [28].

The resonant dc transformer [29] developed a new direction for medium- or high-voltage dc-dc conversion. The power switches are operated at low frequency and the resonant action assists all switches to achieve soft-switching. The transformer-less configuration offers further advantages in volume reduction and power efficiency. Versions using thyristors and IGBTs were

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demonstrated experimentally [30], [31]. They are promising candidates for medium step-ratio or high step-ratio dc-dc applications but they would face either high voltage or high current stress on some of the active switches or passive capacitors, which may cause design difficulties for high-power low step-ratio conversion.

This paper presents a resonant modular multilevel dc-dc converter with compact SM stack for low step-ratio dc voltage transformation. The topology has only one SM stack and it processes only a small fraction of the power throughput. This configuration is intended to reduce the required volt-ampere rating for SM switches and the energy storage of SM capacitors, thereby substantially reducing the stack volume and cost compared to alternatives. Each SM of the stack is operated at low switching frequency but with an adjustable phase-shift to create a medium frequency excitation across the resonant tank for further volume reduction. The SM capacitors join the resonant operation in controllable sequences and soft-switching is also achieved for all power switches to increase efficiency. Considering that the SM stack itself can fulfil the low step-ratio voltage conversion in a cost-effective way, this converter also utilizes a transformer-less architecture with the benefits of conversion volume and overall efficiency as the resonant dc transformer topologies in [29]–[31], but it loses the galvanic isolation as penalty, which may limit some application area for this converter.

II. Proposed Topology and Operational Principles

The proposed low step-ratio dc-dc converter is shown in Fig. 1, with two configurations, for negative output and positive output respectively. The negative configuration is discussed in this section to illustrate the circuit operation, and the principles are the same for the positive counterpart. The arrows in Fig. 1 denote the reference of the voltages and currents in the circuit.

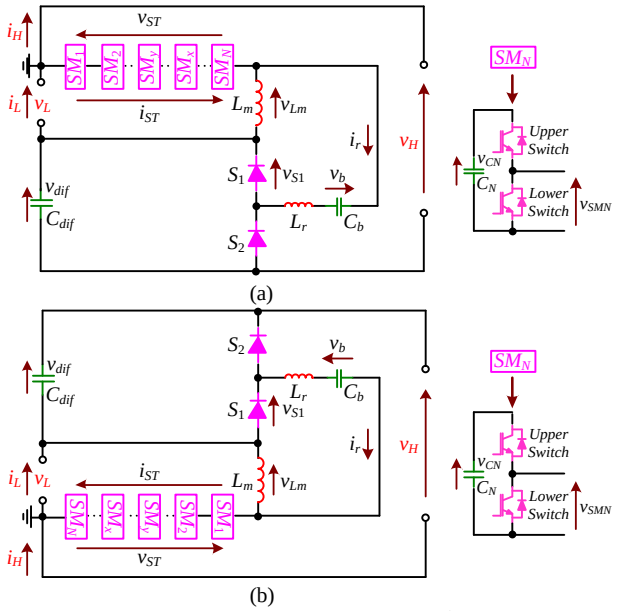


Fig. 1. Low step-ratio dc-dc converter. (a) Negative configuration (b) Positive configuration.

The step-ratio between the high-voltage terminal and low-voltage terminal is defined as $R_{ST} = v_H / v_L$, and the capacitor C_{dif} supports the voltage difference between v_H and v_L ($v_{dif} = v_H - v_L = v_L R_{ST} - v_L$). i_L and i_H are the currents passing through low-voltage terminal and high-voltage terminal, and their difference is the average stack current $\overline{i_{st}}$ ($\overline{i_{st}} = i_L - i_H = i_L - i_L/R_{ST}$).

This circuit contains only one stack of N half-bridge SMs. Since the average voltage across the magnetizing inductor L_m is zero in steady state operation, the average stack voltage $\overline{v_{st}}$ will equal the low-side dc terminal voltage v_L ($\overline{v_{st}} = v_L$) although the maximum and minimum value of stack voltage, $v_{st\text{-}max}$ and $v_{st\text{-}min}$, would depend on SM number and SM capacitor voltage. By switching either y or x SM capacitors into the circuit ($0 < y < x \leq N$) for equal durations, a symmetrical square-wave voltage v_{Lm} can be imposed across the magnetizing inductor. The positive stage is defined as y SMs switched in, the stack voltage is less than v_L and a positive voltage across L_m. In the negative stage, x SMs are switched in and the voltage across L_m is negative. This symmetrical square-wave voltage excites an energy exchange between the SM capacitors (C_1 to C_N), the capacitor C_b and resonant inductor L_r, which together constitute the resonant tank of this converter. The dc component of the stack current passes through the magnetizing inductor while the ac component of stack current flows into the resonant tank, denoted as resonant current i_r. The resonant current flows onward through S_1 when it is positive and the resonant tank is being charged. During this time the high-voltage terminal current, i_H, flows from the low-voltage terminal and differential capacitor C_{dif}. S_2 conducts when resonant current i_r is negative and the resonant tank is discharging in this period to both dc terminals and differential capacitor. The output voltage of this resonant tank as seen across S_1, v_{s1}, is a positive-biased square-wave due to the effect of the dc component voltage on capacitor C_b, noted as dc bias capacitor. For illustration, a simple half-bridge diode rectifier (S_1 and S_2) is shown in Fig. 1, connecting the resonant tank and differential capacitor. The diodes can be formed of series connected diodes appropriate to the voltage difference between v_H and v_L. Controllable devices can be used instead to accommodate bidirectional power flow. If S_1 and S_2 are configured with reverse-blocked bidirectional switches, the full capability for dc-fault management can be also obtained for this converter.

The voltage relationship in the positive stage and negative stage can be described as (1) and (2) respectively given the assumptions that all the SM capacitor voltages are balanced at their average value $\overline{v_C}$ and the voltage across L_r is negligible compared to the dc terminal voltage v_L or v_H.

$$v_L = y\overline{v_C} + v_b = v_{st-min} + v_b \quad (1)$$

$$v_H = v_L + v_{dif} = x\overline{v_C} + v_b = v_{st-max} + v_b \quad (2)$$

According to the voltage-time balance principle on inductor L_m, and considering equal durations for the positive and negative stages, the low-side terminal voltage v_L is expressed as (3).

$$v_L = \overline{v_{st}} = \frac{x+y}{2}\overline{v_C} \quad (3)$$

By substituting (3) into (1) and (2), the voltage on dc bias capacitor v_b and the voltage step-ratio are derived in (4) and (5). This converter is designed for low step-ratio conversion and its maximum step-ratio value is limited to less than 3 with this operational scheme.

$$v_b = \frac{x-y}{2}\overline{v_C} \quad (4)$$

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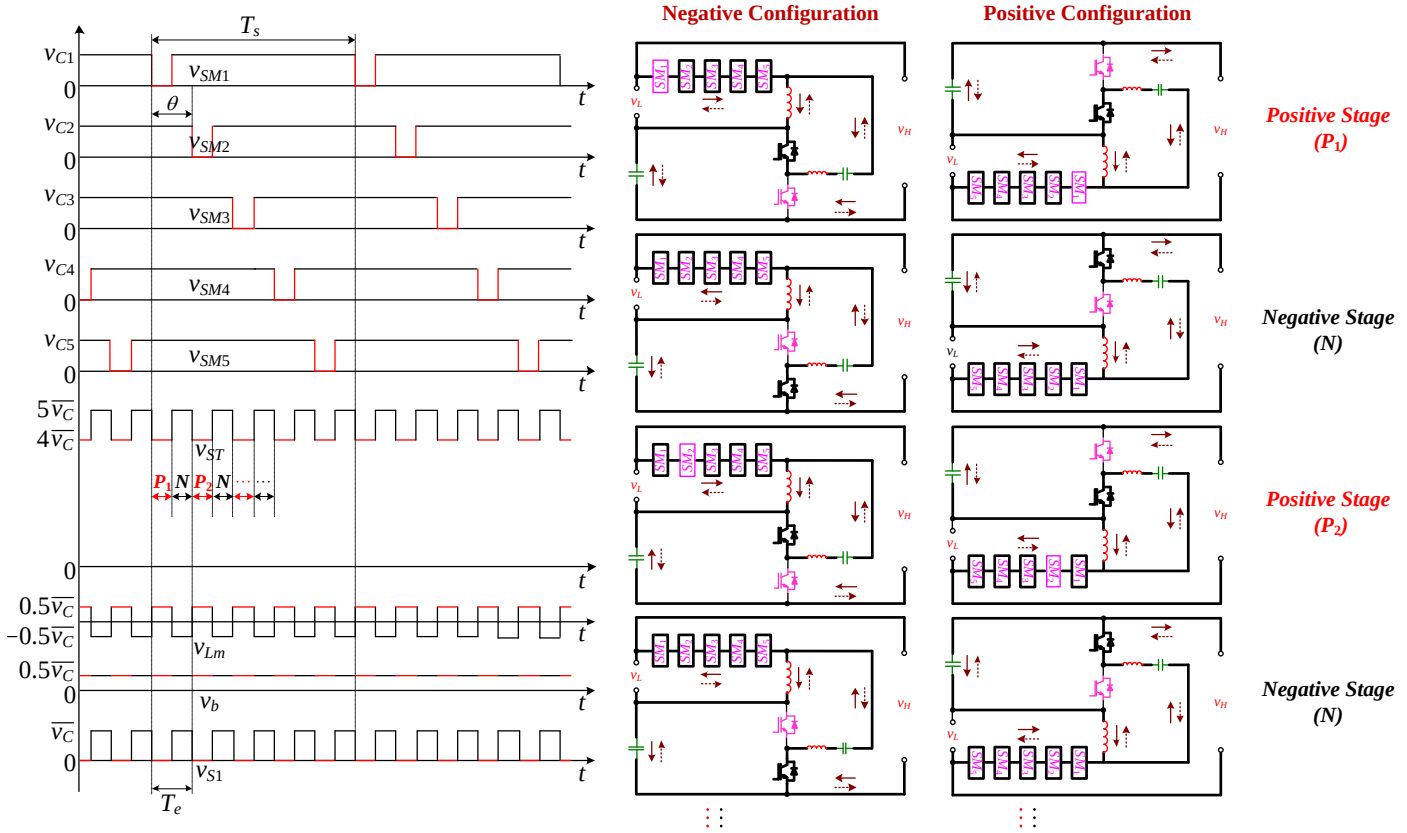


Fig. 2. Operation example waveforms of this low step-ratio dc-dc converter.

$$R_{ST} = \frac{v_H}{v_L} = \frac{3x - y}{x + y} \le R_{ST_max} = \frac{3N - 1}{N + 1} < 3 \tag{5}$$

In the positive stage, the capacitors of y SMs join a resonant circuit with capacitor C_b and inductor L_r, and its resonance assists the switches of the inserted SMs to achieve soft-switching. These inserted y capacitors are in series connection with C_b and inductor L_r, and the remaining N–y SMs are bypassed in this stage. Thus, the resonant frequency in this positive stage, f_p, is presented in (6) under the assumption that each SM capacitance equals C_{SM}. Likewise, the resonant frequency in negative stage, f_n, is given in (7), in which x SM capacitors are deployed in the stack in series with C_b and L_r and N–x SMs are bypassed in this stage.

$$f_p = \frac{\sqrt{y}}{2\pi \cdot \sqrt{L_r(C_{SM} + yC_b)}} \tag{6}$$

$$f_n = \frac{\sqrt{x}}{2\pi \cdot \sqrt{L_r(C_{SM} + xC_b)}} \tag{7}$$

The magnetizing inductor L_m is not considered in the resonant frequency calculation because the magnetizing inductor voltage is clamped by the symmetrical square-wave voltage and L_m is not in the main resonant path for both positive stage and negative stage. Moreover, the value of the magnetizing inductor L_m would be much larger than that of L_r in the circuit design and the effective frequency for resonant excitation will be set in the range of (6) and (7). The high frequency harmonics of the square-wave voltage v_{Lm} could cause some other smaller resonances between the parasite capacitors and inductors in the circuit, but their amplitudes are negligible compared to this fundamental frequency resonance between the SM capacitors, dc bias capacitor and resonant inductor.

To increase the effective frequency f_e of the square-wave v_{Lm} for converter volume reduction and also keep the low switching frequency of SMs for power losses reduction, the phase-shift modulation scheme discussed in [32] is implemented. The upper switches of the SMs are all operated with a duty-cycle value of $(x+y)/2x$ at a switching frequency f_s and each SM switching sequence keeps a phase-shift value of $2\pi/x$ with respect to the adjacent ones. With this scheme, the effective frequency f_e of the square-wave v_{Lm} is increased to xf_s which is normally chosen between f_p and f_n for the best efficiency. The specific relationships for SM duty-cycle and effective frequency in this phase-shift modulation are expressed in (8) and (9) respectively.

$$D = \frac{x + y}{2x} = \frac{2}{1 + R_{ST}} \tag{8}$$

$$f_p \le f_e = xf_s \le f_n \tag{9}$$

For further illustration of the operational principles, a detailed example of low step-ratio conversion (N = 5, y = 4, x = 5) with bidirectional power flow is given in Fig. 2, in which the voltage waveform of each SM (v_{SM1}, v_{SM2}, v_{SM3}, v_{SM4}, v_{SM5}) is colored black when the upper switch of this SM is on (SM capacitor inserted) and colored red when the lower switch is on (SM capacitor bypassed). For the stack voltage v_{ST}, magnetizing inductor voltage v_{Lm} and resonant tank output voltage v_{s1}, the waveforms are colored red for the positive stages and black for the negative ones. In the circuit operation diagrams, solid arrows indicate the current direction when power flow is from the low-voltage terminal to high-voltage terminal, and dash arrows for current flow when the power flow is reversed. For the SMs, the bold black box means this SM is inserted into the resonant path and the current passes through its capacitor while the pink box means

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this SM is bypassed. For rectifier S_1 and S_2, the bold black means this switch is in the on-state while the pink means this switch is off. From the SM voltage waveforms of Fig. 2, it can be seen that each SM capacitor is inserted into the circuit with a duty-cycle of 90% (of the switching cycle T_s), and each SM insertion is phase-shifted by 0.4π from the previous one. Substituting the individual SM capacitor voltage (v_{C1}, v_{C2}, v_{C3}, v_{C4}, v_{C5}) into the average value equations (1) and (2), the voltage relationship of each SM capacitor is derived and summarized in (10). The first five rows represent the five individual positive stages of switching cycle and in each four SMs insert their capacitor and participate in the resonant operation. The sixth row indicates the common negative stage with all the five SMs deployed. The individual SM capacitor voltage can be found from (10) and are written in (11). It means that all the SM capacitor voltages of this converter naturally balance at the value of $2v_L/9$ as an inherent feature of its operation. Using equations (4) and (5), the average voltage across the dc bias capacitor is $v_L/9$ and the step-ratio in this example is found to be 11/9.

$$\begin{bmatrix} v_L \\ v_L \\ v_L \\ v_L \\ v_L \\ v_H \end{bmatrix} = \begin{bmatrix} 0 & 1 & 1 & 1 & 1 & 1 \\ 1 & 0 & 1 & 1 & 1 & 1 \\ 1 & 1 & 0 & 1 & 1 & 1 \\ 1 & 1 & 1 & 0 & 1 & 1 \\ 1 & 1 & 1 & 1 & 0 & 1 \\ 1 & 1 & 1 & 1 & 1 & 1 \end{bmatrix} \cdot \begin{bmatrix} v_{C1} \\ v_{C2} \\ v_{C3} \\ v_{C4} \\ v_{C5} \\ v_b \end{bmatrix} \tag{10}$$

$$v_{C1} = v_{C2} = v_{C3} = v_{C4} = v_{C5} = \overline{v_C} = \frac{2v_L}{9} \tag{11}$$

This is a specific case for the lowest step-ratio conversion with $N = 5$ configuration for this converter and it is obtained with y and x selected at their maximum values they can have in this case.

In general operation of this converter, the value of y and x for the positive stage and negative stage can be flexibly chosen from their minimum to maximum values ($1 \le y \le N-1$, $y < x \le N$) in the design process to provide various choices for step-ratio value and satisfy various dc connection specifications. Also, the voltage and current of this converter are both controllable in the operation by adjusting the switching frequency and phase-shift angle [32] as the traditional scheme in classic *LLC* circuit [14], [15] and resonant dc transformers [29]–[31].

In general operation, all the SM capacitors voltage of this converter will be also self-balanced at $2v_L/(x+y)$ as long as the value of y and x are mutually prime and the voltage relationship matrix has the full rank. In this condition, all the SM capacitor voltages (v_{C1}, v_{C2}, v_{C3}, … , v_{CN}) are linearly independent in the voltage relationship equation, which guarantees the solution of all the SM capacitor voltages is unique. Also, there is no strict limitation for the total SM number N in the generalized operation, but note that when N increases to a large number for some applications, it could complicate the design process for the phase-shift modulation scheme in the SM stack. The classic Nearest Level Modulation (NLM) [19], [20] could be an easier modulation choice to accomplish the operation when a large number of SMs are implemented into the stack, but extra voltage sorting and selection process will be needed to realize the voltage balancing for all the SM capacitors. Lastly, soft-switching operation of the SM switches can be also realized in the generalized operation provided the effective frequency f_e is maintained between f_p and f_n.

It is acknowledged that it would be difficult to change the value of y and x online in practical operation if the step-ratio between two terminals changes dramatically. Fortunately, it is not very common to have a large change in terminal voltage in a power transmission or distribution grid (other than a fault), so the step-ratio will usually stay at a given value or in a small range when the converter is implemented in the operation and there will be a regular combination choice for y and x values to meet the step-ratio requirement. When the dc terminal voltage changes a lot in practical applications, it would be preferred to redesign the y-x combination and adjust the modulation scheme to satisfy the new step-ratio requirement.

III. Stack Rating Requirement

The volume and cost are important metrics for MMC-based converters in medium- or high-voltage applications and the required rating of the SM stack is the crucial factor [33], [34].

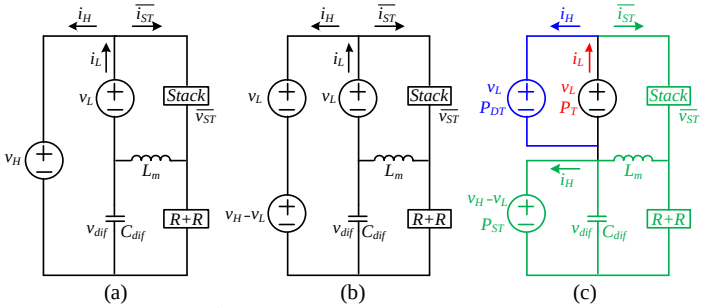


Fig. 3. Illustration of the power conversion process analysis. (a) Principal current loops. (b) Equivalent circuit. (c) Separation of power flows.

The power conversion process of the proposed low-ratio dc-dc converter is illustrated in Fig. 3. Fig. 3(a) is a representation of Fig. 1, showing the SM stack with average voltage and current ($\overline{v_{st}}$ and $\overline{i_{st}}$), and a simplified resonant tank and rectifier (R+R). As in the original, the high-side voltage v_H is the sum of the low-side voltage v_L and the voltage across differential capacitor v_{dif} ($v_H = v_L + v_{dif}$). The current from the low-voltage terminal i_L divides to flow in two loops ($i_L = i_H + \overline{i_{st}}$): that flowing via the high-voltage terminal, i_H, directly transfers power between two dc terminals; that flowing via the SM stack, $\overline{i_{st}}$, transfers power to the stack which then re-enters the circuit through ac current developed in the resonant tank. The rectifier passes power to the differential capacitor C_{dif}, which then flows to the high-voltage terminal alongside the direct transferred power. Therefore, the SM stack processes only a fraction of the power throughput as made clearly by redrawing the circuit in Fig. 3(b) and Fig. 3(c). The power directly transferred between two terminals, P_{DT}, is the blue loop in Fig. 3(c), and the power processed through the SM stack, P_{ST}, is the green loop, which sum to give the total power throughput P_T. These power are described by the relationships given in (12)–(14).

$$P_T = v_L i_L = v_H i_H = P_{DT} + P_{ST} \tag{12}$$

$$P_{DT} = v_L i_H = v_L \frac{i_L}{R_{ST}} = \frac{P_T}{R_{ST}} = \frac{v_L}{v_H} P_T \tag{13}$$

$$P_{ST} = \overline{v_{st}} \cdot \overline{i_{st}} = v_L(i_L - i_H) = P_T\left(1 - \frac{1}{R_{ST}}\right) = P_T\left(1 - \frac{v_L}{v_H}\right) \tag{14}$$

The proposed converter is more suitable for low step-ratio conversion ($1 < R_{st} \le 2$) to interface two dc terminals with similar

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but not identical voltage. It can be seen from (13) and (14) that, when the step-ratio of this converter is a little above 1 for low step-ratio conversion, then the bulk of the power passes directly between two dc terminals and only a small fraction is processed by the SM stack. If the step-ratio of this converter keeps increasing to medium ratio range ($2 < R_{st} < 3$), the majority of the power will go through the SM stack, and the requirements for stack semiconductor volt-ampere rating and stack capacitive energy storage would be both increased.

It is also important to note that there is only one stack in the circuit and the small fraction of the power throughput, P_{ST}, passes through the stack just once. Together, these features create a substantial advantage in terms of stack rating requirement compared to the front-to-front and direct-chain-link MMC in low step-ratio dc-dc applications. The analysis and comparisons in the following sections will quantify those benefits.

A. *Requirement for Stack Semiconductor Volt-ampere Rating*

For a general MMC based dc-dc converter, the normalized stack semiconductor volt-ampere rating, S_{SP}, is defined as a ratio of the sum of the semiconductor volt-ampere rating to the converter power throughput P_T, shown in (15), where v_{jk} and i_{jk} are the rated voltage and current rating of kth (half-bridge) SM power device in jth stack, N_j is the number of the SMs in jth stack and N_{ST} is the number of stacks in the circuit.

$$S_{SP} = \frac{2\sum_{j=1}^{N_{ST}}\sum_{k=1}^{N_j} v_{jk}\, i_{jk}}{P_T} = \frac{2\sum_{j=1}^{N_{ST}} i_j \sum_{k=1}^{N_j} v_{jk}}{P_T} \tag{15}$$

To keep the power devices working safely within their rated voltage and current, the sum of the v_{jk} for jth stack should be larger than the maximum value (absolute value) of jth stack voltage, $v_{STj\text{-}max}$, and i_{jk} also needs to be larger than the maximum value (absolute value) of jth stack current, $i_{STj\text{-}max}$. In this manner, S_{SP} must be larger than R_{SP}, which is defined as the maximum operation volt-ampere rating normalized to P_T and it leads to the minimum volt-ampere rating requirement for SM stack semiconductors without considering power device safety margin. The detailed relationship is presented in (16). Note that the units of numerator and denominator in (15) and (16) are both Watts, so S_{sp} and R_{sp} are both ratio values without units.

$$S_{SP} > R_{SP} = \frac{2\sum_{j=1}^{N_{ST}} i_{STj-max} v_{STj-max}}{P_T} \tag{16}$$

With the analysis in (1), (2) and (5), the stack voltage v_{ST} of this dc-dc converter is given in (17). It is a relatively square-wave voltage with a large dc offset. The stack current i_{ST} has both dc and ac components. The dc component is the average value of i_{ST} over each effective cycle and the ac component is the resonant current of this circuit. It can be described as (18) given the fact that the time difference between resonant cycle and effective cycle is short and the stack current value in this short time difference is negligible.

$$v_{ST}(t) = v_L \mp \frac{R_{ST}-1}{2} v_L = v_L - sgn\left(sin\frac{2\pi}{T_e}t\right)\cdot\frac{R_{ST}-1}{2}v_L \tag{17}$$

$$i_{ST}(t) = i_{dc}(t) + i_{ac}(t) = \frac{R_{ST}-1}{R_{ST}} i_L + I_r\, sin\frac{2\pi}{T_e}t \tag{18}$$

The amplitude of the resonant current I_r can be derived from (19) and expressed in (20) under the assumption that there is no power losses in the whole conversion process. From (18) and (20), it can be seen that the maximum current (absolute value) for SM IGBTs would occur in lowest step-ratio conversion.

$$\int_0^{T_e} v_{Lm}(t) i_r(t) dt = \frac{(R_{ST}-1)v_L}{2}\cdot 2\int_0^{\frac{T_e}{2}} I_r sin\frac{2\pi}{T_e}dt = v_L(i_L - i_H)T_e \tag{19}$$

$$I_r = \frac{\pi i_L}{R_{ST}} \tag{20}$$

Then, substituting the results of (17), (18) and (20) into (16), the maximum operation volt-ampere rating for SM stack of this low step-ratio dc-dc converter is shown in (21).

$$R_{SP-LRS} = \frac{R_{ST}^2 + \pi R_{ST} + \pi - 1}{R_{ST}} \tag{21}$$

To make a fair comparison with other MMC stack based dc-dc alternatives, the volt-ampere rating of S_1 and S_2 in this converter should be also taken into consideration. The maximum voltage and current (absolute value) of S_1 and S_2 in normal operation are expressed in (22) and (23) respectively, and their maximum operation volt-ampere rating is shown in (24).

$$v_{S1-max} = v_{S2-max} = v_H - v_L = (R_{ST}-1)v_L \tag{22}$$

$$i_{S1-max} = i_{S2-max} = I_r = \frac{\pi i_L}{R_{ST}} \tag{23}$$

$$R_{S1} = R_{S2} = \frac{\pi(R_{ST}-1)}{R_{ST}} \tag{24}$$

Then, combining the results in (21) and (24), the overall required volt-ampere rating (including both SM stack and rectifiers) of this low step-ratio converter is given in (25).

$$R_{SP-LR} = \frac{R_{ST}^2 + 3\pi R_{ST} - \pi - 1}{R_{ST}} \tag{25}$$

The stack volt-ampere rating expression for transformer-less front-to-front MMC $R_{SP\text{-}FF}$ [35], [36] and direct-chain-link MMC $R_{SP\text{-}DL}$ [25], [37] are given in (26) and (27) respectively.

$$R_{SP-FF} = \frac{4R_{ST}^2 + 18R_{ST} + 2}{R_{ST}} \tag{26}$$

$$R_{SP-DL} = \begin{cases} \dfrac{2R_{ST}^2 + 14R_{ST} - 12}{R_{ST}^2}, & 1 < R_{ST} \le 2 \\ \dfrac{4R_{ST}^2 + 10R_{ST} - 12}{R_{ST}^2}, & R_{ST} > 2 \end{cases} \tag{27}$$

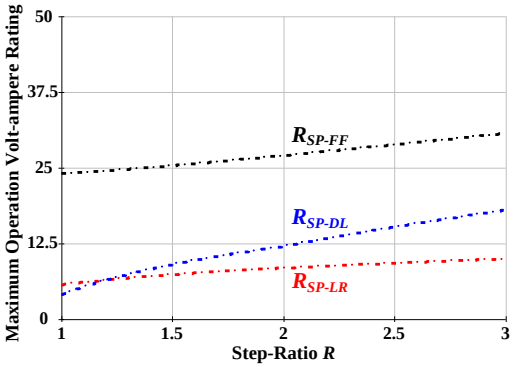


Fig. 4. Comparison for maximum operation volt-ampere rating.

The detailed comparison result among these three dc-dc converters are presented in Fig. 4. It can be seen that the value for the proposed low step-ratio converter, $R_{SP\text{-}LR}$, is below 11 in the whole step-ratio range ($1 < R_{st} < 3$), and this value is much

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smaller than $R_{SP\text{-}FF}$ and $R_{SP\text{-}DC}$ for the front-to-front and direct-chain-link MMC alternatives in this same ratio range. This results indicate that the proposed converter may save a large amount of volume and cost in its semiconductor design in the case of connection of dc terminals with similar but not identical voltages.

B. Requirement for Stack Capacitive Energy Storage

Similar to (15), the stack capacitive energy storage, normalized to the power throughput, is defined as S_{CE} and given by (28), where $v_{c\text{-}max}$ and $v_{c\text{-}min}$ are the maximum and minimum voltage expected for SM capacitors.

$$S_{CE} = \frac{\sum_{j=1}^{N_{ST}} \sum_{k=1}^{N_j} \left(\frac{1}{2} C_{SM} v_{c-max}^2 - \frac{1}{2} C_{SM} v_{c-min}^2 \right)}{P_T} \tag{28}$$

The stack capacitors need to absorb and release the energy fluctuations from the varying current flow of the stacks. To balance the SM voltages within the nominal range, S_{CE} should be larger than the operation required capacitive energy R_{CE}, which is defined as a ratio of the sum of the maximum energy deviation (absolute value) of each stack to the converter power throughput P_T, as shown in (29), where $\Delta E_{ST\,j}$ denotes the energy deviation in jth stack.

$$S_{CE} \geq R_{CE} = \frac{\sum_{j=1}^{N_{ST}} max\left|\Delta E_{ST\,j}\right|}{P_T} = \sum_{j=1}^{N_{ST}} max\left|\frac{\Delta E_{ST\,j}}{P_T}\right| \tag{29}$$

Based on the analysis in (17), (18) and (20), the stack energy deviation of the presented dc-dc converter is derived in (30).

$$\begin{aligned} R_{CE-LR} &= max\left|\frac{\Delta E_{ST-LR}}{P_T}\right| = max\left|\frac{1}{v_{LS} i_{LS}} \int_0^t v_{ST}(t) i_{ST}(t) dt\right| \\ &= max\left|\int_0^t \left[1 - sgn\left(sin\frac{2\pi x}{T_s} t\right) \cdot \frac{R_{ST}-1}{2}\right] \right. \\ &\left. \cdot \left(\frac{R_{ST}-1}{R} + \frac{\pi}{R_{ST}} sin\frac{2\pi x}{T_s} t\right) dt\right| \end{aligned} \tag{30}$$

For a transformer-less front-to-front MMC or direct-chain-link MMC, the relevant energy deviation are expressed in (31) and (32) [33], [34], [37], where ΔE_{LSST} and ΔE_{HSST} denote the stack energy deviation sum in the low-voltage side and high-voltage side of the transformer-less front-to-front MMC, ΔE_{STT} and ΔE_{STB} are the stack energy deviation sum in the top arms and bottom arms of the direct-chain-link MMC.

$$\begin{aligned} R_{CE-FF} &= max\left|\frac{\Delta E_{LSST}}{P_T}\right| + max\left|\frac{\Delta E_{HSST}}{P_T}\right| \\ &= max\left|-2\,sin^2\frac{2\pi}{T_s} t + sin\frac{2\pi}{T_s} t + 1\right| \\ &+ max\left|-2\,sin^2\frac{2\pi}{T_s} t + \frac{2R_{ST}^2 - 1}{R_{ST}} sin\frac{2\pi}{T_s} t + 1\right| \end{aligned} \tag{31}$$

$$\begin{aligned} R_{CE-DL}(1 < R_{ST} \leq 2) &= max\left|\frac{\Delta E_{STT}}{P_T}\right| + max\left|\frac{\Delta E_{STB}}{P_T}\right| \\ &= max\left|\int_0^t -\frac{2(R_{ST}-1)}{R_{ST}} sin^2\frac{2\pi}{T_s} t + \frac{R_{ST}-1}{R_{ST}} sin\frac{2\pi}{T_s} t \right. \\ &\left. + \frac{R_{ST}-1}{R_{ST}} dt\right| + max\left|\int_0^t \frac{2(R_{ST}-1)}{R_{ST}} sin^2\frac{2\pi}{T_s} t \right. \\ &\left. - \frac{R_{ST}^2 - 2R_{ST} - 1}{R_{ST}} sin\frac{2\pi}{T_s} t - \frac{R_{ST}-1}{R_{ST}} dt\right| \end{aligned} \tag{32.a}$$

$$\begin{aligned} R_{CE-DL}(R_{ST} > 2) &= max\left|\frac{\Delta E_{STT}}{P_T}\right| + max\left|\frac{\Delta E_{STB}}{P_T}\right| \\ &= max\left|\int_0^t -\frac{2(R_{ST}-1)}{R_{ST}} sin^2\frac{2\pi}{T_s} t + \frac{2R_{ST}^2 - 4R_{ST} + 1}{R_{ST}} sin\frac{2\pi}{T_s} t \right. \\ &\left. + \frac{R_{ST}-1}{R_{ST}} dt\right| + max\left|\int_0^t \frac{2(R_{ST}-1)}{R_{ST}} sin^2\frac{2\pi}{T_s} t + \frac{R_{ST}-1}{R_{ST}} sin\frac{2\pi}{T_s} t \right. \\ &\left. - \frac{R_{ST}-1}{R_{ST}} dt\right| \end{aligned} \tag{32.b}$$

Fig. 5 compares the total stack energy deviation of three converters over one switching cycle at the same switching frequency and step-ratio. The stack energy deviation of the proposed low step-ratio converter is zero over each switching cycle, which means the net dc energy and ac energy are naturally balanced in this stack without requirement for extra adjustment. In other words, the dc energy injecting to the SM stack is all converted to the ac energy going to the resonant tank. More importantly, the maximum energy deviation of this converter is less than 0.25 kJ/MVA, which is clearly a smaller value than that of the front-to-front and direct-chain-link circuits. Thus, there would be also a significant saving in stack capacitor volume and cost with the proposed converter compared to the alternatives.

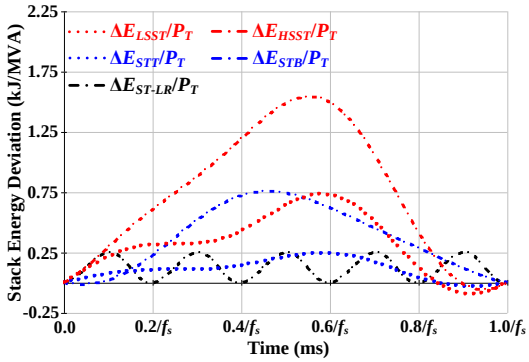


Fig. 5. Comparison for stack energy deviation and operation required capacitive energy ($f_s = 500Hz, R_{ST} = 3/2, R_{CE-LR} = max\left|\frac{\Delta E_{ST-LR}}{P_T}\right| \approx 0.25$ kJ/MVA, $R_{CE-FF} = max\left|\frac{\Delta E_{LSST}}{P_T}\right| + max\left|\frac{\Delta E_{HSST}}{P_T}\right| \approx 2.4$ kJ/MVA, $R_{CE-DL} = max\left|\frac{\Delta E_{STT}}{P_T}\right| + max\left|\frac{\Delta E_{STB}}{P_T}\right| \approx$ 1.0 kJ/MVA).

In addition, for other passive components (L_m, L_r, C_b, C_{dif}) in the circuit, this low step-ratio dc-dc converter also has some advantages in volume and cost over the passive components in front-to-front and direct-chain-link alternatives. Firstly, the required voltage ratings for these passive components are all much smaller than the dc terminal voltages ($v_{Lm_max} = \frac{x-y}{x+y} v_L, v_{Lr} \ll v_L, v_{b_max} = \frac{x-y}{x+y} v_L, v_{cdif_max} = \frac{2x-2y}{x+y} v_L$), but some of the passive components in the front-to-front and direct-chain-link MMC circuits need to withstand the whole terminal voltages. Secondly, based on the analysis in Fig. 3, the bulk of the power passes directly between two dc terminals in this converter and only a small fraction goes through these passive components, while in the front-to-front and direct-chain-link MMC, the passive components usually need to provide full capacity for the power throughput. Thirdly, the value of these passive components are very small because they only need to process the resonant voltage or current with the fast effective frequency f_e, which is x times of the SM switching frequency f_s ($f_e = xf_s$). However, the majority of the passive components in the front-to-front MMC and direct-chain-link MMC have to face the relatively low frequency voltage or current, which is normally equal or lower than the SM switching frequency, so the passive components value would be much larger than that in the proposed converter. Taking all of these three factors as a whole, the volume

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and cost of these passive components in this low step-ratio dc-dc converter could also have substantial benefits over that in front-to-front and direct-chain-link circuits.

IV. Further Configurations

For bipolar MVDC or HVDC where the two poles may need independent power processing, the positive and negative configuration of the proposed converter can be combined with a common ground. The switching sequence in the negative stack can be given a half-cycle phase-shift with respect to that in the positive counterpart to achieve a reduction in voltage ripple on bipolar dc terminal.

Alternatively, pair of converters of the same polarity can be connected in parallel and operated with a half-cycle phase-shift with respect to each other. This creates a symmetrical square-wave voltage between the mid-points of the two half-bridge rectifiers which is equivalent to use full-bridge rectifier. The current will flow through two resonant tanks (two stacks of SM capacitors, two dc bias capacitors and two resonant inductors), but the resonant frequencies still keep the same as those in single circuit operation according to (6) and (7).

These two concepts are combined and shown in Fig. 6 to create a bipolar full-bridge dc-dc converter. The rectifier sub-sections are full-bridge architecture, so the phase-shift between the positive pole and negative pole should be adjusted to a quarter of the effective cycle to achieve voltage ripple reduction. The switching sequences for the pair of the stacks of the same polarity are still operated with half-cycle phase-shift to form the symmetrical square-wave voltage for full-bridge rectifier. The operational advantages of original single circuit are preserved and the power throughput is four times that of the single circuit.

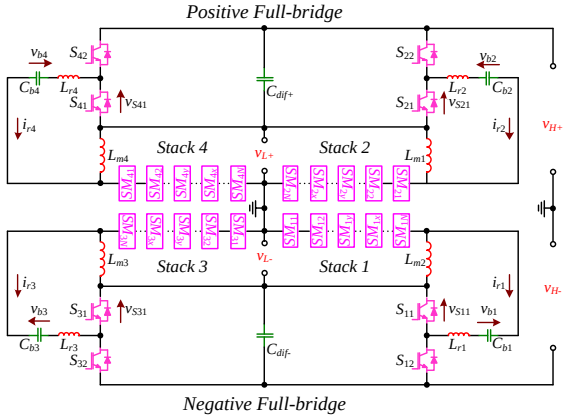


Fig. 6. Bipolar full-bridge configuration.

V. Medium Voltage Level Simulation Examples

As explained in Section II, S_1 and S_2 have to withstand the voltage difference between v_H and v_L. When v_H and v_L are in the medium voltage range, the single switch configuration or series connection with small number of devices can be utilized for S_1 and S_2. If v_H and v_L are increased to high voltage range, their difference could become larger and the press-package series connection with large number of devices would be a preferred option for S_1 and S_2 for highly reliable operation.

In this section, a trail design of a medium voltage level converter is undertaken and its simulation results for low step-ratio conversion is used to verify the theoretical analysis in Section II and III. Application examples for the proposed converter and its derivatives are also explored.

The application chosen is bidirectional dc power flow between two monopole MVDC terminals, one at 10 kV and the other variable between 10 and 20 kV. A medium power rating (4 MW < P < 5 MW) is chosen to that this can be accomplished with only 5 SMs using a presently available IGBT. The maximum current value for SM IGBTs would be below 1.5 kA in this application example based on the analysis in (18) and (20). The detailed parameters of the design are listed in Table I. From (15) and (28), it can be found this converter has implemented a highly-compact and low-cost design, in which the normalized semiconductor stack volt-ampere rating S_{SP} is 17.3 and the SM capacitive energy storage S_{CE} is only 0.46 kJ/MVA.

Table I. Simulation parameters in the full-scale applications examples

Parameter	Description	Value
P_T	*Power Throughput*	4 MW–5 MW
v_L	*Low-side Terminal Voltage*	10 kV
v_H	*High-side Terminal Voltage*	10 kV–20 kV
C_b	*DC Bias Capacitor*	750 μF
L_r	*Resonant Inductor*	25 μH
L_m	*Magnetizing Inductor*	0.98 mH
N	*SM Total Number in the Stack*	5
S	*Power Switches*	ABB 5SNA1500E330305
C_k	*SM Capacitors* (k=1,2,…,5)	750 μF with ±10% variation
δ_{SM}	*SM Capacitor Voltage Range*	5%

Simulation results are given in Fig. 7 for the same operating condition (y = 4, x = 5) as illustrated in Fig. 2, which was the lowest step-ratio conversion for this stack configuration. The switching frequency was operated at 550 Hz to create an effective frequency of 2.75 kHz for good resonance performance and conversion efficiency. The SM_1 output voltage v_{sm1} and stack current i_{ST} are shown in Fig. 7(a). They demonstrate that the capacitor of SM_1 is switched into the stack (v_{sm1} is high) for 90% of the switching cycle, during which time this capacitor forms part of the resonant circuit, assisting the SM switches to achieve soft-switching. For the remaining 10% of the switching cycle (v_{sm1} is low), SM_1 is the bypassed and the SM capacitor is not in the conduction path. This bypassed period is one of the five positive stages in the overall cycle of the converter. The stack voltage v_{ST}, presented in Fig. 7(b), is a square-wave voltage with minimum value at about 9 kV for positive stages and maximum value at about 11 kV for negative stages, which verifies the analysis in (1)–(3). The SM capacitances used in the simulation were deliberately given a ±10% variation from the nominal capacitance to reflect manufacturing tolerances. Fig. 7(c) shows that all the SM capacitor voltages self-balance at 2.2 kV without switching pattern adjustment. The SM capacitor voltage waveforms exhibit the phase-shift of 0.4π ($2\pi/x$) between adjacent SMs. The voltage across dc bias capacitor is about 1.1 kV, which is half of the SM capacitor average voltage as predicted by (4). The amplitude of resonant tank output voltage in Fig. 7(d) indicate the step-ratio is around 11/9 in this conversion as expected from (5). In addition, it can be seen that the harmonics generated from the converter are very small in this simulation operation, and they would not interfere with the telephone lines and power quality in practical applications.

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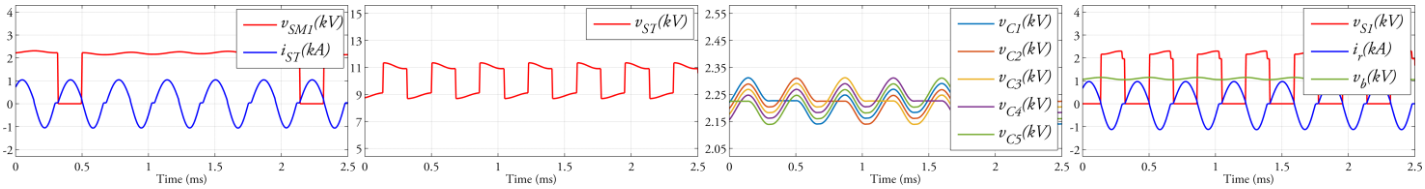


Fig. 7. Positive power flow for R_{st} = 11/9. (a) SM_1 output voltage v_{SM1} and stack current i_{ST}. (b) Stack voltage v_{ST}. (c) SM capacitor voltages v_{C1}, v_{C2}, v_{C3}, v_{C4}, v_{C5}. (d) Resonant tank output voltage v_{S1}, resonant current i_r and dc biased capacitor voltage v_b.

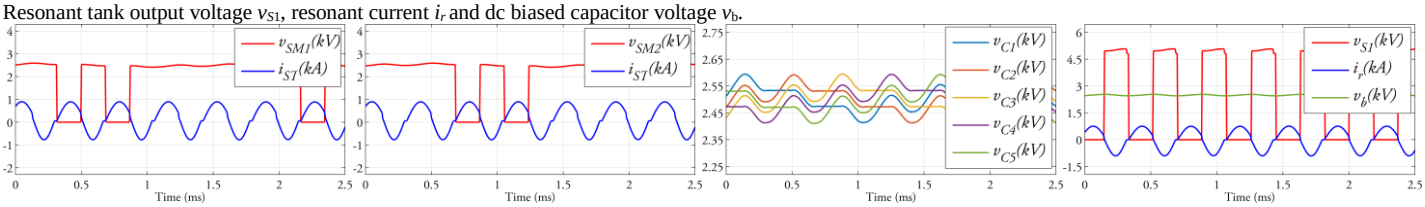


Fig. 8. Positive power flow for R_{st} = 3/2. (a) SM_1 output voltage v_{SM1} and stack current i_{ST}. (b) SM_2 output voltage v_{SM2} and stack current i_{ST}. (c) SM capacitor voltages v_{C1}, v_{C2}, v_{C3}, v_{C4}, v_{C5}. (d) Resonant tank output voltage v_{S1}, resonant current i_r and dc biased capacitor voltage v_b.

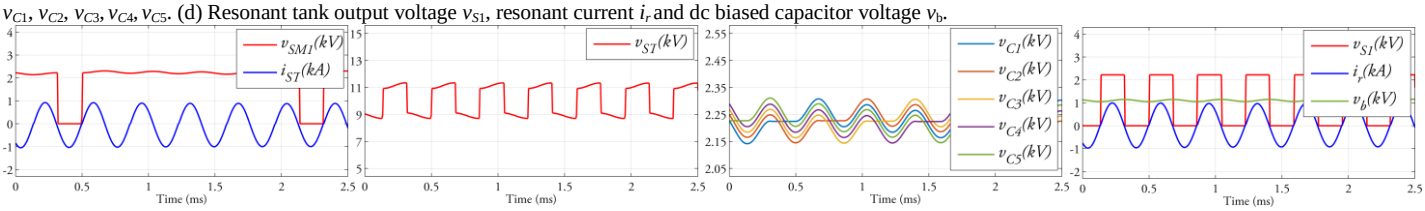


Fig. 9. Negative power flow for R_{st} = 11/9. (a) SM_1 output voltage v_{SM1} and stack current i_{ST}. (b) Stack voltage v_{ST}. (c) SM capacitor voltages v_{C1}, v_{C2}, v_{C3}, v_{C4}, v_{C5}. (d) Resonant tank output voltage v_{S1}, resonant current i_r and dc biased capacitor voltage v_b.

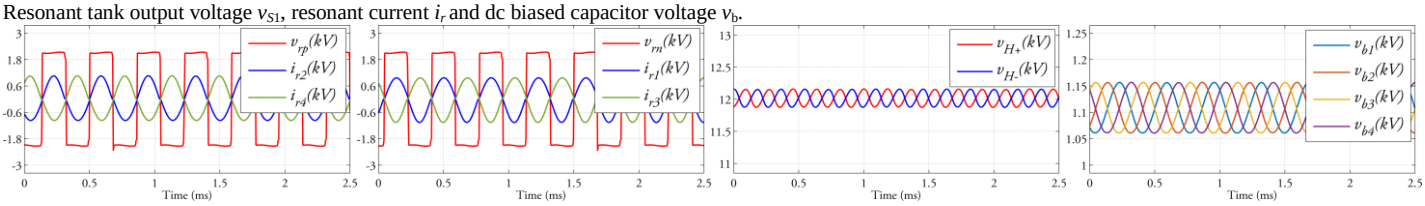


Fig. 10. Bipolar full-bridge configuration. (a) Positive full-bridge rectifier input voltage v_{rp} ($v_{rp} = v_{S21} - v_{S41}$), resonant currents i_{r2} and i_{r4}. (b) Negative full-bridge rectifier input voltage v_{rn} ($v_{rn} = v_{S31} - v_{S11}$) resonant currents i_{r1} and i_{r3}. (c) Positive and negative dc terminal voltage v_{H+} and v_{H-}. (d) DC bias capacitor voltages v_{b1}, v_{b2}, v_{b3}, v_{b4}.

To illustrate the flexibility of modulation and operation, Fig. 8 shows conversion from 10 kV to 15 kV in which the number of SMs in the positive stage is adjusted to 3 (y = 3) and the switching frequency is reduced to 525 Hz to match the range of resonant frequencies in this operation. The SM_1 and SM_2 output voltage waveforms are given in Fig. 8(a) and Fig. 8(b) respectively. Compared to Fig. 7, the phase-shift angle between the adjacent SMs is still 0.4π but the duty-cycle is decreased to 80%. It means each SM capacitor is bypassed for two positive stages and two adjacent SMs are switched out of the stack in sequence for each positive stage. Fig. 8(c) and Fig. 8(d) verify that all the SM capacitor voltages are still self-balanced in this operation and the voltage step-ratio is about 3/2. The step-ratio of this dc-dc converter can be further extended to about 7/3 in this application example within the rated operation area of the selected power devices in Table I.

Simulation results with reverse power flow (high-side to low side) is shown in Fig. 9. Operation is seen to be essentially the same as in Fig. 7, with the same voltage values and resonant frequencies but the current directions have been all reversed. The SM capacitor voltages waveform in Fig. 9(c) is very similar to that in Fig. 7(c), but it can be seen in detail that the voltage trends of each SM capacitor in one switching cycle are actually in the opposite sense due to the change of the current flow.

To demonstrate the high power rating connection between two bipolar MVDC terminals, the bipolar full-bridge topology in Fig. 6, is configured for ±10 kV to ±12 kV conversion at 15 MW.

Each of the four stacks has the same circuit parameters as Table I. The four biased dc capacitor and four resonant inductor are also subject to 10% variations to represent manufacturing tolerances. Each stack is operated with the same principles as in the single circuit operation, so the benefits of low stack rating, soft-switching and self-balancing can be all inherited.

The switching sequences for *Stack 2* (*Stack 1*) and *Stack 4* (*Stack 3*) have a half-cycle phase-shift from each other, forming a minus/plus symmetrical rectifier input voltage, given in Fig. 10(a) and Fig. 10(b), which increases the current rating twice and also suits the full-bridge rectifier architecture. In the meantime, the sequence difference between *Stack 2* (*Stack 4*) and *Stack 1* (*Stack 3*) is set with a quarter of cycle to increase the voltage rating twice and also alleviate the ripple on bipolar dc terminal, shown in Fig. 10(c). Lastly, the four dc biased capacitor voltages are also self-balanced at the theoretical value of (4), illustrated in Fig. 10(d). The voltage and current stress on each power device of this derivative converter still keeps the some value as that in original single configuration, but its power rating has been increased to four times that of the single circuit operation.

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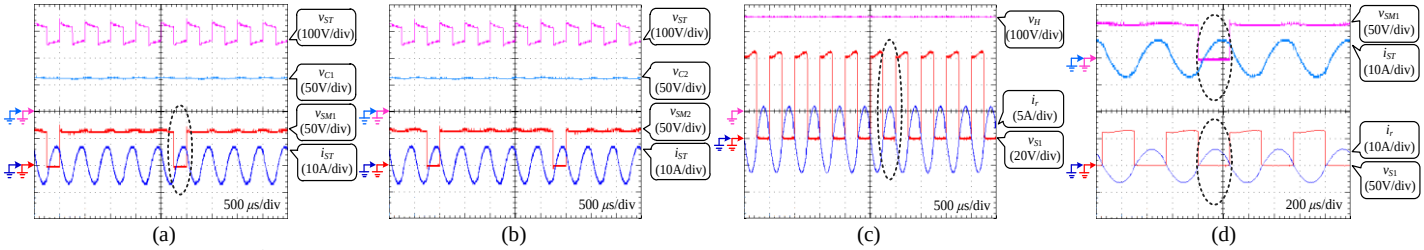


Fig. 11. Experimental results for R_{st} = 11/9. (a) Stack voltage v_{ST}, SM_1 capacitor voltage v_{C1}, SM_1 output voltage v_{SM1} and stack current i_{ST}. (b) SM_2 capacitor voltage v_{C2} and SM_2 output voltage v_{SM2}. (c) High-side voltage v_H, resonant current i_r and resonant tank output voltage v_{S1}. (d) Switching waveforms of SM_1 and rectifier S_1.

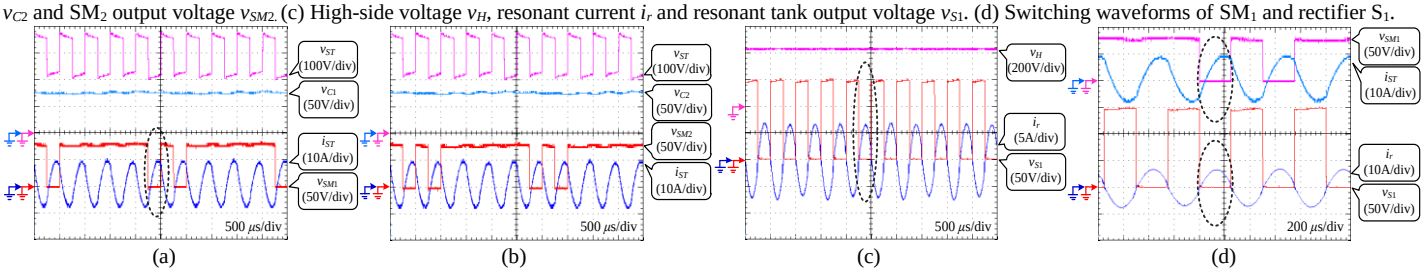


Fig. 12. Experimental results for R_{st} = 3/2. (a) Stack voltage v_{ST}, SM_1 capacitor voltage v_{C1}, stack current i_{ST} and SM_1 output voltage v_{SM1}. (b) SM_2 capacitor voltage v_{C2} and SM_2 output voltage v_{SM2}. (c) High-side voltage v_H, resonant current i_r and resonant tank output voltage v_{S1}. (d) Switching waveforms of SM_1 and rectifier S_1.

VI. Experimental Results Assessment

To further validate the theoretical analysis and simulation results for low step-ratio conversion, a down-scaled prototype was built with the parameters of Table II. The stack design also has a low rating configuration. The capacitive energy storage S_{CE} is only 0.49 kJ/MVA in the test.

Table II. Experimental parameters in the down-scaled laboratory prototype

Symbol	Description	Value
P_T	*Power Throughput*	1.5 kW–3.5 kW
v_L	*Low-side Terminal Voltage*	300 V
v_H	*High-side Terminal Voltage*	300 V–600 V
C_b	*DC Bias Capacitor*	330 μF
L_r	*Resonant Inductor*	101.7 μH
L_m	*Magnetizing Inductor*	1.65 mH
N	*SM Total Number in the Stack*	5
C_k	*kth SM Capacitor* (k=1,2,…,5)	330 μF with ±10% variation
δ_{SM}	*SM Capacitor Voltage Range*	5%

Experimental results for the lowest step-ratio operation (y = 4, x = 5) of this prototype are shown in Fig. 11. The switching frequency was chosen as 400 Hz for a 2.0 kHz effective frequency which approximates the resonant frequencies of (6) and (7), and the SM duty-cycle and phase-shift value are set with 90% and π/5 respectively. It can be seen from Fig. 11(a) and Fig. 11(b) that each SM capacitor joins the resonance for 90% of the switching cycle and their voltages are self-balanced at about 65 V. The stack current is a combination of a dc term and a sinusoidal waveform while the stack voltage contains a square-wave shape with the peak-to-peak value of 66 V, which is in good agreement with the analysis in Fig. 2. The high-voltage side waveforms are given in Fig. 11(c). The resonant tank output voltage is a positive-biased square wave with the amplitude of 64 V and the resonant current is a symmetrical sinusoidal waveform without dc offset. The high-side voltage of 364 V evident in Fig. 11(c) gives a step-ratio of 1.21 which is approximately 11/9 so in agreement with the analysis and simulation results in Fig. 7. Lastly, Fig. 11(d) shows the switching details of Fig. 11(a) and Fig. 11(b). The waveforms confirm that the SM switches achieve zero-voltage-switching (ZVS) at turn-on and the rectifiers achieve zero-current-switching (ZCS) at turn-off. It can be found that the harmonics are also very small in these experiment results.

The flexibility of modulation and operation is demonstrated by testing conversion between 300 V and 450 V with y = 3, x = 5. The duty-cycle is adjusted to 80% accordingly while the phase-shift angle remains at π/5. Fig. 12(a) and Fig. 12(b) illustrate that two SM capacitors are bypassed in each positive stage and that each SM is bypassed for two consecutive positive stages. The SM capacitor voltages settle in a balanced fashion at around 75 V and the ac stack voltage is therefore 150 V peak-to-peak. The amplitude of the resonant tank output voltage in Fig. 12(c) becomes double of the SM capacitor voltage because the voltage across bias capacitor is also 75 V. A high-side voltage of 448 V is seen in Fig. 12(c) giving a step-ratio of 1.49 which is very close to the theoretical value of 3/2 for this case. Again, soft-switching is achieved as seen in Fig. 12(d). These experimental results further validate the theoretical analysis and simulation example in Fig. 8.

The down-scaled prototype is seen to operate in close accord with the theory and simulation presented for these low step-ratio conversion examples, and it demonstrates that the proposed converter has good potentials of low stack rating, soft-switching and self-balancing for low step-ratio dc terminal interconnection.

VII. Conclusion

A modular multilevel dc-dc converter has been presented in this paper which is suited to realize the low-step ratio conversion that would allow bi-directional connection between dc terminals with similar but not identical voltage.

The converter has only one stack of SMs, shared between the low-voltage and high-voltage terminals and this stack only processes a fraction of the throughput power. This fraction is small when the voltage step-ratio is small (a little above 1). Analysis has shown that the required ratings of this stack in terms of semiconductor stack volt-ampere rating and capacitive energy storage are substantially lower than those for the alternative converters using front-to-front and direct-chain-link MMC configurations. These low rating advantages are expected to

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make significant savings in physical volume and cost for this converter in low step-ratio applications. In circuit operation, each SM of the stack is operated in low switching frequency with an adjustable phase-shift value, which creates a medium frequency voltage across the resonant tank for further volume reduction and also provides the self-balancing benefits for SM capacitors. The voltage conversion ratio can be flexibly adjusted in design process by selection of the number of SMs participating in the positive and negative stages of the switching cycle. Soft-switching operation is also achieved for all power switches to increase efficiency.

The theoretical analysis has been verified by both full-scale simulation examples and down-scaled experimental prototype. The results demonstrate that this low-step ratio dc-dc converter and its derivatives, have good potential for operation as highly-compact and low-cost dc transformers in future dc networks.

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