A Fully Passive Selectorless ReRAM Array

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***Abstract*— The memristor is a revolutionary passive device that has gained popularity in recent years as a possible contender for next-generation nonvolatile memory and analogue computing. This work presents a passive selectorless memristive memory crossbar array. It presents a 16x16 array with a one capacitor and one memristor (1C1R) core cell. The 1C1R configuration is a promising memory structure because of its high density, lower power consumption, faster speed, and more importantly the monotonic relationship between the charges on the capacitor and the memristance. Data readout in this work is carried out by an 8-bit time to digital converter. Results show that the 1C1R structure can successfully store 1-bit of information by splitting the resistance of the memristor (memristance) into two states of 10.07KΩ (bit 1) and 3.38 MΩ (bit 0). The total area of the proposed array is 0.4 mm² in a SkyWater130nm CMOS technology.**

Keywords—ReRAM, Memristor, 1C1R, SkyWater

I INTRODUCTION

In 1971, Leon Chua coined the term "memristor," which combines memory and resistance [1]. Based on a circuit-theoretic notion of symmetry and completeness, Chua proposed that a two-terminal circuit element whose operation is determined by a relationship between flux linkage and charge must exist and be the fourth fundamental circuit element. Resistive Random Access Memory (RRAM) is an emerging technology based on devices that exhibit resistive switching that has been widely implemented in a variety of applications, including multibit memory storage [2], image processing [3], logic circuits [4], and neuromorphic computing [5]. The distinctive characteristic of memristors is that their conductance is dependent on previous electrical signals, allowing them to function as nonvolatile memory. In addition, memristors may store multibit information with continuously tunable conductance, unlike the binary "0" and "1" states of conventional digital storage devices, granting them a greater bit density. Nonvolatility, rapid programming, low programming energy, and a small footprint make memristors a possible alternative for the next generation of embedded memory, which might combine the benefits of SRAM and floating-gate transistors[6].

Only ReRAM crossbar arrays is the conventional method for a memristive memory array that can minimize crossbar footprint and fabrication cost, but their size and performance are restricted by sneak path leakage current, half-select cell disturbance, switching threshold voltage uniformity, crossbar yield, crossbar line resistance, and other factors Recent breakthroughs in manufacturing technology, RRAM stack enhancements, and novel conductance mapping techniques have permitted the creation of enormous passive crossbar arrays with good uniformity, high yield (above 99 percent), and precise conductance tuning. However, the 1 Transistor 1 ReRAM (1T1R) cell configuration remains the most prevalent option for RRAM arrays [7]. The 1T1R crossbar

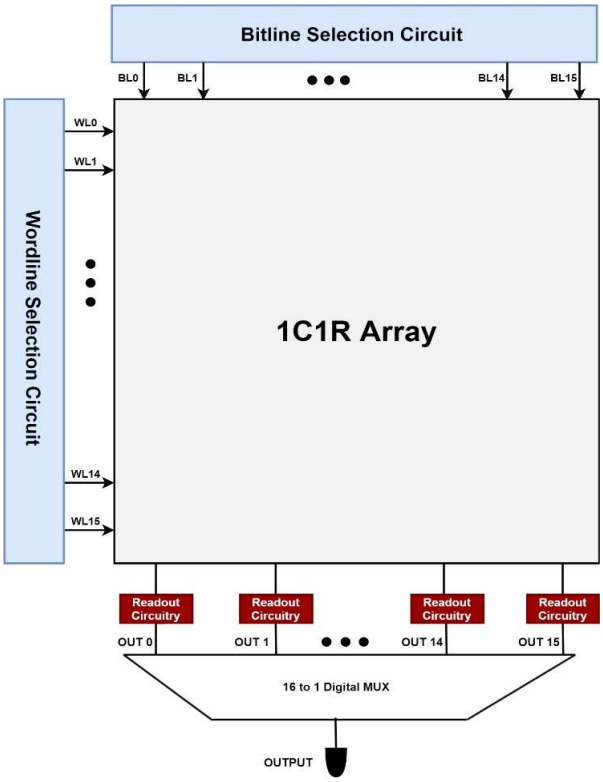


Fig. 1. The top-level architecture of proposed 1C1R array

design is highly comparable to that of DRAM. Not only does the transistor permit flexible selection of memory cells, but it also facilitates programming for systems that do computation in memory. Due to the large footprint of planar FETs, it has a relatively low device area density, and the device density is further constrained by the difficulties of integrating 1T1Rs in 3D [6]. Furthermore, active 1T1R crossbar arrays have a large area overhead due to the fact that the select transistor must be able to survive the forming/programming currents/voltages of the RRAM that is connected to their drain terminal. These currents and voltages are far greater than the typical operating currents and voltages of contemporary logic transistor technologies, hence limiting their capability for continuous scaling.

In this paper, we present a novel approach and technique for using a capacitor in conjunction with RRAM as a passive selectorless cell that can be controlled by an applied signal to either allow or prevent the passage of current. It can offer higher density and lower cost, in addition to minimizing the sneak path current compared to the standalone memristor. This paper extends the introduction of 1C1R as a memristive memory structure presented in our publication [8] by implementing a crossbar array with its peripheral circuitries in a chip and using a reverse ramp signal to program 1C1R instead of pulse signal. It covers, to the best of our knowledge, the first comprehensive study of integrating a

capacitor with RRAM (1C1R) as the core cell in an array. A fully integrated and designed 16x16 1C1R crossbar array that was designed in SkyWater 130nm CMOS technology is presented.

The remaining sections of this paper are structured as follows. Section II describes chip level architecture. Section III provides an overview of the 1C1R cell. Section IV presents the writing operation of a 1C1R. Section V provides the readout circuit and the specific implementation in this design. Section VI presents the results, and Section VII concludes the paper.

II CHIP LEVEL ARCHITECTURE

The block level CMOS chip architecture is shown in Fig.1. The array consists of (1) 16x16 1C1R cells. (2) wordline selection circuitry (3) Bitline selection circuitry (4) Readout circuit.
The selection circuit consists of 16 2-to1 analog multiplexers and a 4-16 digital decoder as illustrated in Fig.3. The digital 4-16 decoder select which multiplexer takes V1, so the remaining take V2.

The inputs to this chip are (1) digital 1.8V control signals that are level shifted on chip to 3.3V so that the applied V1 and V2 in the selection circuit can go up to 3.3V (includes the address of the DUT, pulse width and operation mode) and (2) 2-3.3V peak reverse ramp signal from an off-chip voltage source to establish the desired programming voltage across the activated ReRAM device. The outputs of the proposed system are digital signals.

III 1C1R OVERVIEW

The 1C1R structure is inherently a high pass filter (HPF) made up of a capacitor and a memristor coupled to each other in series. As can be seen in Fig. 2, 1C1R is a two-terminal arrangement in which the top plate of the capacitor is connected to wordline (WL), and the bottom electrode of the memristor is connected to bitline (BL).



Fig. 2. 1C1R cell schematic.

There is a monotonic relationship between the memristance and the charges on the capacitor. The voltage across the capacitor is proportional to the integral of the current flowing through the memristor, that is, to the memristance as in Eq.1 and Eq.2. Thus, the state of the memristor can be determined by measuring the voltage across the capacitor, potentially eliminating the need for a complex read-out circuit whilst also reducing the influence of leakage current during reading. 1C1R has an advantage of reducing the sneak path current by applying a low frequency pulse signal (>5RC) to the unselected cells, which will eventually result into a zero current following through them.

$$Vc = \frac{Q}{C} = \frac{1}{C}\int_{-\infty}^{t} i\,dt \qquad (1)$$

$$Vc = \frac{1}{Rmem\ C}\int_{-\infty}^{t} Vin\ e^{\frac{-t}{RmemC}}\,dt \qquad (2)$$

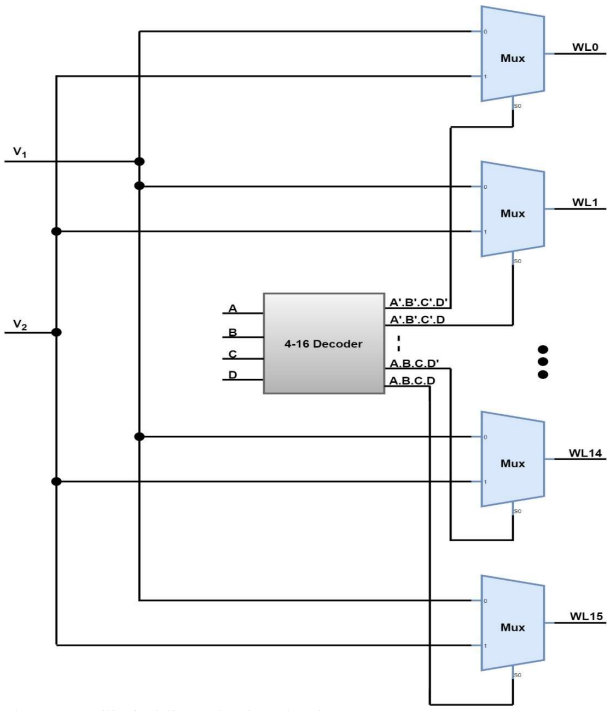


Fig. 3. Wordline\Bitline selection circuit

IV WRITING OPERATION

A. Signal type

Since 1C1R is HPF, the pulse width that is used to write onto the ReRAM in 1C1R must be much lower than RC, resulting in a very high frequency, which is hard to attain. As a result, programming a memristor needs an abrupt change in the signal applied to it in order to change its resistance state. Since the memristor switches its resistance value at the rise edge of a pulse and keeps its resistance value until the next pulse. We can apply a signal that has very rapid change in the rise time and slow change at fall time so we can keep the frequency achievable. Therefore, an alternative way to program a memristor while keeping the frequency achievable is to go for a reverse ramp signal as in Fig.4 which can be generated by a waveform generator. By setting the rise time of the reverse ramp signal to be fast and the fall time to be slow, this way the 1C1R structure can observe the rapid change at the rise time and no able to see the slow change in the fall time since it is an HPF. Fig.5 illustrates that the memristance changes at each rise edge of the reverse ramp signal and is maintained until the next signal. The simulation in Fig.5 was done using a Verilog-A ReRAM model provided by SkyWater [9].

A. Writing scheme

The write operation for the array is performed by selecting the address of the DUT, defining the rise and fall time and applying the required write voltage externally. In this paper, we used a 1/3 bias scheme to bias the unselected cells[6, 10]. The 1/3V bias scheme, depicted in Fig.6, applies full voltage to the selected word line and 0 V to the selected bitline. The unselected word lines are given a voltage of 1/3 V, whereas the unselected bit lines are given a voltage of 2/3 V. Therefore, the selected memory cell (red square) is biased at V, the half-selected memory cells (green and blue squares)

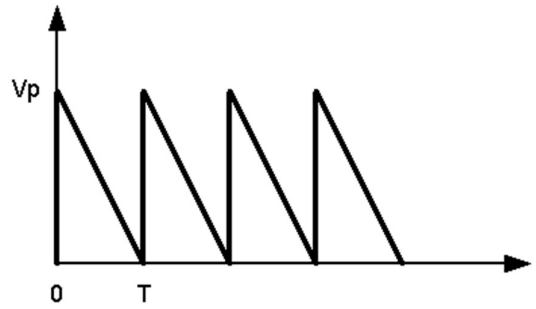


Fig. 4. A reverse ramp signal used for writing operation.

are biased at 1/3 V, and the unselected memory cells (purple square) are biased at -1/3V. In this way, all unselected cells are biased with 1/3V which is not enough to excite the memristor to cause a resistance change.

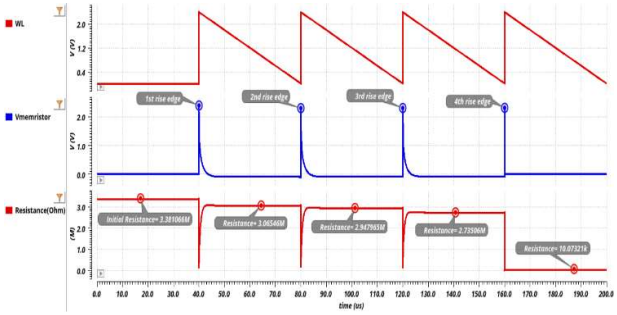


Fig. 5. Memristance changes at each rise edge of the applied signal.

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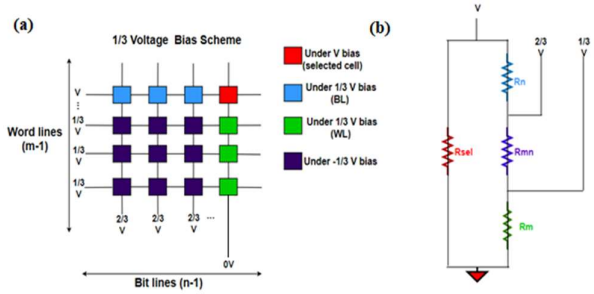


Fig. 6. (a) The one-third voltage (1/3 V) bias scheme. (b) The equivalent electric circuits.

B. Top level writing

1) SET operation

The SkyWater ReRAM device's resistance switch can range from 10.07KΩ (R_{ON}) to 3.38MΩ. (R_{OFF}). The setting operation is to write a bit 1 (R_{ON}), switching from high resistance state (HRS) to low resistance state (LRS). The set top-level writing is performed by applying a V_{DD} and $1/3V_{DD}$ at the wordline's selection circuit, and $2/3V_{DD}$ and 0V at bitline's selection circuit as illustrated in Fig.6. The decoder will select V_{DD} to be applied at the selected wordline, and $1/3V_{DD}$ at unselected ones. Similarly, at the bitline, the decoder will select $2/3V_{DD}$ at the unselected cells, and 0V at the selected one.

2) Reset operation

The reset process involves writing a bit to 0 and changing from LRS to HRS. It is implemented in same way as set

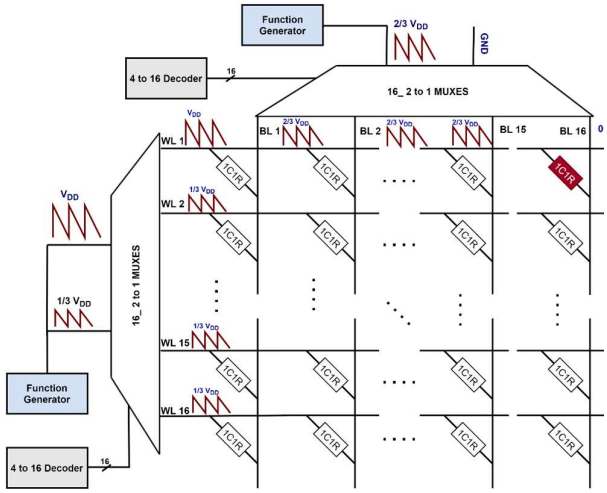


Fig. 7. The proposed array configuration for the set operation.

operation but with V_{DD} and $1/3V_{DD}$ at the selection circuit of bitline and $2/3V_{DD}$ and 0 at the wordline's selection circuit.

V READOUT OPERATION

Targeting a single cross-point element at a time and attempting to identify its resistance state is one method for reading from a multi-level crossbar array. This results in either active (leading to the target device) or inactive word- and bit-lines (not leading to the target device). Numerous circuit topologies and biassing regimes may be employed to perform a readout operation[10-12]. The readout technique we chose to implement is a time to digital converter (TDC) as shown in Fig.8.

The readout circuit consists of capacitor (C_R), two comparators, SR latch, TDC, and shift register. As our signal is encoded into time/frequency, a Time-to-Digital Converter (TDC) is used as a digitizer that converts the electrical signal into a digital code.

In the reading mode, we apply a pulse signal, at the wordline of the selected cell, with an amplitude less than writing threshold voltage (500 mV) of the memristor, thus the memristance remains unchanged. The C_R value can be any reasonable value, but for simplicity, we have it the same as the capacitor in the 1C1R so that the voltage at C_R is half of the applied signal since 1C1R capacitor and C_R are in series. Then the C_R will charge up until it reaches the half value of the applied voltage. After that, two comparators, SR latch, TDC, and PISO shift register is used to convert the time to digital code as described above.

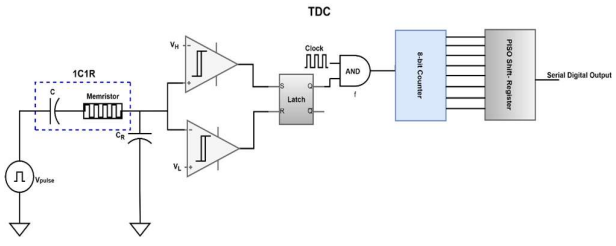


Fig. 8. 1C1R readout technique using TDC.

In the proposed readout technique, readout capacitors C_R are attached at each of the crossbar array column (BL) to covert the current flowing through the array into a voltage. Then the

sensed voltage of C_R is connected to two comparators with high and low reference voltages. The output of the comparators is then connected to the SR latch. When the C_R potential reaches one of the threshold voltages V_H or V_L, the SR latch toggles polarity, and the current flow is inverted. The charging rate is controlled by the value of the

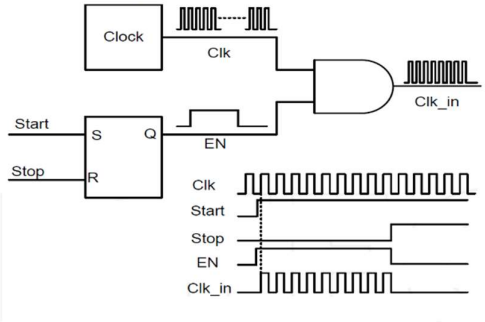


Fig. 9. Time to frequency converter circuit.

memristance value as in Eq.1 and 2. The output of the SR latch and a clock signal is connected to an AND gate to convert the signal into frequency as shown in Fig. 9. After that, a TDC is used to Convert the frequency into digital code. An 8-bit asynchronous counter is used for this purpose, as illustrated in Fig.8. After that, a parallel-in-serial-out (PISO) shift register is used to serialize the 8 digital outputs into a serial digital output thus reducing the number of pads required. The readout circuit is connected to each of the array column to perform an accurate measurement of the resistance state of a selected cell. All the digital output of the 16 readout circuits is connected to 16-1 multiplexer to select the column of the selected cell it reads. Fig. 10 illustrates the top-level array of the readout mode.

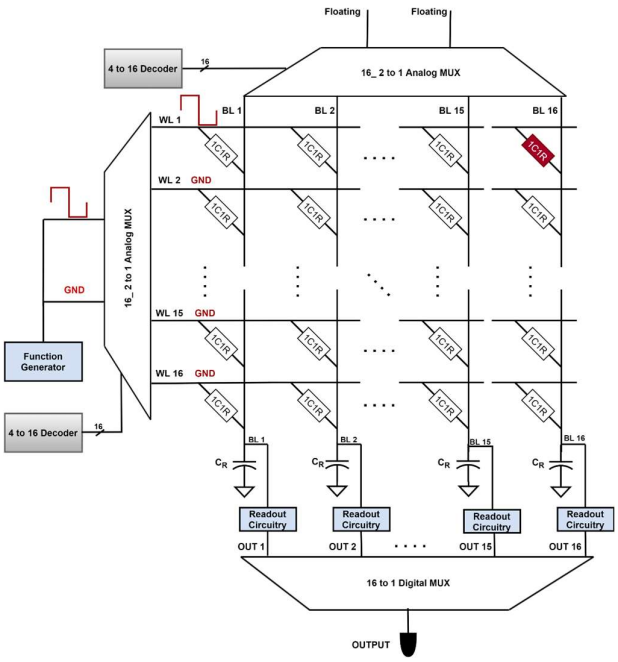


Fig. 10. 1C1R array readout mode.

VI RESULTS

The proposed circuits are designed in a SkyWater 130nm CMOS technology. The maximum programming voltage for the proposed system is set to 3.3 V. This satisfies the general requirements for the ReRAM forming conditions and achieves a good compromise between High Voltage (HV) device layout size and programming range. The HRS and LRS of SkyWater ReRAM are 3.38 MΩ and 10.07 KΩ respectively [8]. The simulation is conducted by applying an external reverse ramp signal range from 2.4-3.3 V to a pad

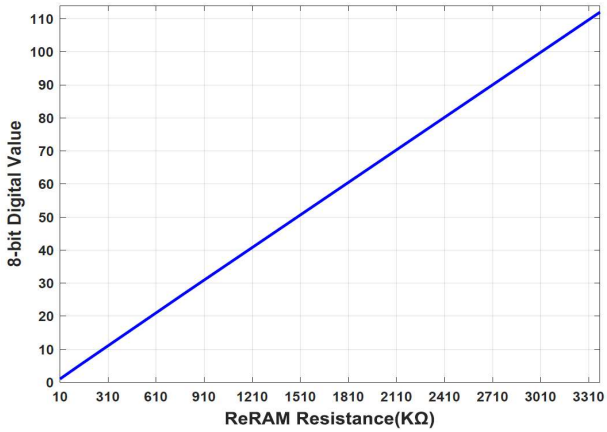


Fig. 11. Full-range conversion/digitization. It is based on 50 MHz clock speed of the readout system.

and measuring the on-chip, digitised resistance of the device through pads. Each digital value has a corresponding ReRAM resistance state as shown in Fig. 11. It can be used as a look-up table for measuring the ReRAM resistance state. This result is based on 50 MHz clock speed of the readout system. The layout of proposed system is shown in Fig.12. The layout size is 978x410um. The crucial specification of proposed array is summarized in Table I.

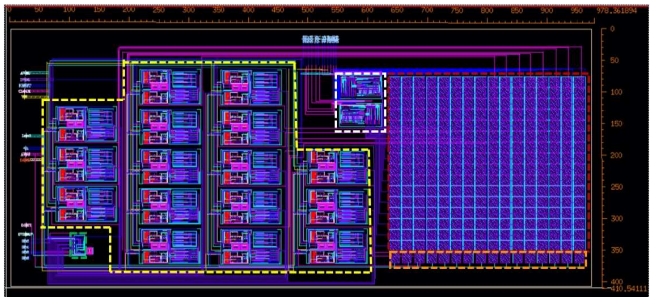


Fig. 12. The layout of designed chip. Red box:1C1R array; White box:WL and BL selection circuits; Orang box: 16 readout capacitors (C_R); Yellow box: readout circuits; Green box:16-1 multiplexer.

Table I PROPOSED ARRAY SPECIFICATIONS

Specification	Unit	Value
Programming voltage range	(V)	2.4-3.3
Minimum fall time	(μs)	8.5
Maximum rise time	(ps)	10
Reading voltage range	(mV)	100-500
Reading pulse width	(μs)	≥ 4.2
1C1R cell size	(μm)	16.3x15.9
1C1R capacitance value/C_R	(fF)	500/500
TDC resolution	(bit)	8
Clock speed	(MHz)	50
ReRAM resistance range	(Ω)	10.07K-3.38M
Average Energy consumption†	(pJ/bit)	140.10

† Writing 0 (HRS to LRS) average energy consumption

VII CONCLUSION

In this paper, a passive selectorless memristive 16x16 memory array was proposed. The design is based on a 1C1R core cell, offering high density, faster switching, and lower power consumption. A 1C1R architecture and proper programming methodology on crossbar array reduced sneak path currents and ensures reliable write and read on the selected memristor. The 1C1R system differentiates memristor into two states (R_{OFF}=3.38MΩ and R_{ON}=10.07KΩ) and can store multibit. The system was designed in SkyWater 130nm CMOS technology. A TDC readout circuitry with 8-bit resolution and 50 MHz clock has been designed to perform precise reading.

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