

Topology-Transition Control For Wide-Input-Voltage-Range Efficiency Improvement and Fast Current Regulation In Automotive LED Applications

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Abstract—Automotive LED drivers require special design considerations, which includes voltage step-up and –down function, high energy efficiency and fast current reference tracking capability. Unlike the conventional efficiency improvement methods, which is based on cumbersome circuit/component optimization and/or modification for a single operating point, this paper proposes a simple approach based on topology transition which can achieve a high efficiency for a wide input voltage range. In particular, the topology of the LED driver can change between buck, boost and buck-boost converter according to the level of the input voltage. In addition, a novel current mode controller is proposed such that (i) compatibility to different topologies (ii) seamless topology transition and (iii) fast current reference tracking can be concurrently achieved. The feasibilities of the proposed topology transition method and its control has been experimentally verified through a four-switch buck-boost converter prototype with 7 – 45 V input, 25 V/1 A LED strings output. It is shown that there is more than 5% efficiency improvement as compared to the conventional four-switch buck-boost converter. Full range (0%–100%) and precise (1% dimming precision) PWM dimming has also been demonstrated.

Index Terms—Automotive LED lighting, non-inverting four switch buck-boost converter, PWM dimming, topology transition control.

I. INTRODUCTION

Compared to the conventional lighting sources (e.g., halogen and Xenon), high-brightness light-emitting-diodes (LEDs) have become preferable solutions in the automotive

lighting industry due to their high power efficiency, compact size, long lifetime and flexible manipulation for various shapes [1]–[4].

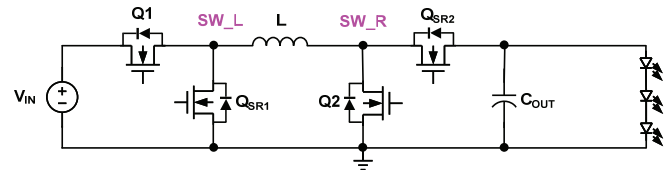


Fig. 1. Non-inverting four switch buck-boost converter.

Besides high power density, high energy efficiency, low cost, current sharing, and high reliability, which are typically needed for general lighting applications [5]–[7], the design of an automotive LED driver requires several special design considerations:

(i) The LED driver must have both voltage step-up and step-down capability [8]. This is because the input voltage of an automotive LED driver frequently varies within a wide range while the output voltage is relatively constant, despite the change of the LED current. It has been reported that the voltage of a vehicle supply line to which an LED driver is connected usually varies from 18 – 32 V for a typical 24-V system during normal driving of the vehicle. When the vehicle undergoes transient disturbances, such as a sudden stop/start, cold crank and unclamped load dump, the input voltage of the LED driver can fluctuate even more dramatically [2].

(ii) The LED driver must achieve high energy efficiency. This is helpful not only to reserve energy usage but also to relief the thermal stress on the LED devices (which directly leads to prolonged operating lifetime and a reduced maintenance cost of the automotive lighting system).

(iii) The LED driver should have fast output current regulation capability, which is necessary both for safety (e.g., the tail lights should be instantly turned on when the vehicle brakes) and dimming (e.g. in performing pulse-width-modulated (PWM) dimming, the LED current should be turned on/off with minimum delay [9]–[11]) considerations.

The first two challenges are usually addressed by selecting a proper circuit topology and then its efficiency is optimized from the circuit and/or component point of view. For instance, a non-inverting four-switch buck boost converter (as shown in Fig. 1) can be chosen due to its inherent features such as

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positive output voltage (hence simplify the control logic circuits design), minimum passive component count (thus improves the power density), low voltage stress across the power devices, and lower system order (thus easier controller design) as opposed to a Cuk and a SEPIC converter [9], [12]–[15]. Optimal efficiency is then obtained through careful selection, design and layout of the passive/active components of the LED driver, and/or modification of the original circuit in order to achieve soft-switching operation [10], [16]. With these solutions, however, an optimum efficiency can only be achieved at a certain operating point (e.g. rated input/output voltage). Further improvement of the energy efficiency for a wide input voltage range is difficult. Specifically, when high step-up or -down conversion ratio is needed, the currents in the switches will be significantly increasing which inevitably lead to an overall reduction of the system efficiency.

The third challenge is not well addressed in the prior arts. Typically, existing work focuses on fast output voltage regulation other than output current regulation. This might lead to substantial current overshoot/undershoot during PWM dimming since LEDs are sensitive to its driving voltage. To avoid undesirable transient current in the LEDs, a linear current regulator in series with the LED load are typically employed [17]–[20]. Another method is to intentionally increase the output capacitance of the LED driver to mitigate the output voltage variation. Nonetheless, due to the resulted slow system dynamics, the output current of the LED driver will have a slow slew rate, which directly limits the dimming frequency and dimming precision [21], [22].

In this paper, a method for improving system efficiency through topology transition is proposed. A four-switch buck-boost converter can be configured as a buck, boost and buck-boost converter based on the level of the input voltage. With this proposal, the number of the active switches involved is reduced during high step-up or -down conversion operations and thus the overall power losses can be reduced throughout the whole input voltage range. To facilitate the topology transition and to address the fast current regulation challenge, a novel topology-transition controller based on a unique digital adaptive constant On-time control is proposed. As will be shown, the proposed controller naturally supports accurate steady-state current regulation for all the three topologies. Moreover, due to its fast current reference tracking capability, the controller enables PWM dimming easily without the addition of lossy linear current regulators and/or large output capacitors. Experimental results from a 30 W laboratory prototype are given to demonstrate the validity and features of the proposed topology change operation and the proposed control.

II. FEASIBILITIES OF TOPOLOGY TRANSITION FOR EFFICIENCY IMPROVEMENT

A four-switch buck-boost converter (as shown in Fig. 1) is simply a cascaded formulation of a buck and a boost converter, where Q_1 and Q_{SR1} formulate a buck cell, Q_2 and Q_{SR2} formulate the boost cell. Therefore, a four-switch buck-boost converter has exactly the same function of both voltage step-up and step-down as the traditional single-switch buck-boost converter.

Unlike most single-switch buck-boost type converters, however, a four-switch buck-boost converter offers the possibility to flexibly change its topology which is helpful to achieve efficiency improvement for a wide input voltage range. The reason can be explained as follows:

Denote the duty ratios of Q_1 and Q_2 as d_1 and d_2 , respectively, and assume that the switches within a cell are switching complementarily. Based on to Fig. 1, the average voltages at the switching nodes SW_L and SW_R over one switching period T_s are therefore

$$v_{SW_L} = d_1 V_{IN} \quad (1)$$

$$v_{SW_R} = (1 - d_2) V_o. \quad (2)$$

where V_{IN} and V_o are the input voltage and output voltage, respectively. Additionally, according to the voltage-second principle, one yields

$$v_{SW_L} = v_{SW_R}. \quad (3)$$

Solutions of (1)–(3) lead to

$$V_o = \frac{d_1}{1 - d_2} V_{IN} \quad (4)$$

Equation (4) indicates that V_o can be controlled by two individual control inputs, i.e., d_1 and d_2 , which means that there are two degrees of freedom for controlling the converters. This is in contrast to all the single-switch converters where V_o can only be regulated by a single control input (which is the duty cycle of that switch).

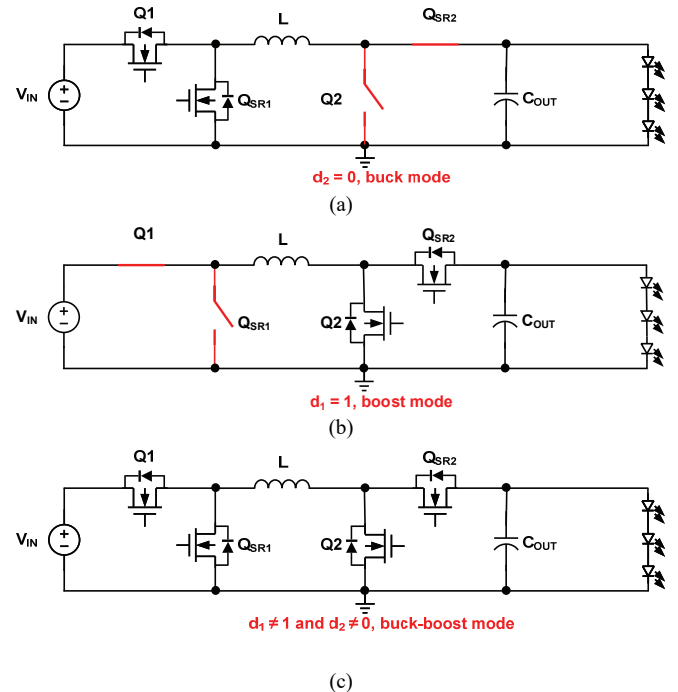


Fig. 2. Illustration of the three operation modes of a four-switch buck-boost converter.

With the enhanced control freedom, it is possible to change the topology of the four-switch buck-boost converter while still achieve output voltage regulation. For instance,

If $d_2 = 0$, which means that Q_2 is always off, and Q_{SR2} is always on, then the converter operates as a buck converter (Fig. 2 (a)). Equation (4) reduces to

$$V_o = d_1 V_{IN} \quad (5)$$

If $d_1 = 1$, which means that Q_1 is always on, and Q_2 is always off, the converter operations as a boost converter (Fig. 2 (b)). (4) then becomes

$$V_o = \frac{1}{1-d_2} V_{IN} \quad (6)$$

If $d_1 \neq 1$ and $d_2 \neq 0$, then the converter is a conventional four-switch buck-boost converter (Fig. 2 (c)).

Note that the number of active switches involved during the buck mode and the boost mode of operation is three. In particular, only two out of the three active switches are switching at high frequency while the third switch is always ON. This is in contrast to the conventional operation mode of a four-switch buck-boost converter (Fig. 2(c)) where all of the four switches are switching at high frequency. Intuitively, if the topology can change according to the level of the input voltage, i.e., in buck mode when V_{IN} is relatively high, in boost mode when V_{IN} is low and in buck-boost mode when V_{IN} is closed to V_o , then the overall system efficiency can be improved due to the reduced switching losses and conduction losses.

On the other hand, by employing the topology change scheme, the inductor core loss can also be reduced as compared to that in the conventional buck-boost type converter (including single-switch buck-boost, SEPIC, and Cuk). The reason is that the inductor in a buck-boost converter always processes (stores and releases) all the input power per switching cycle, where it only processes partial power in a buck and a boost converter.

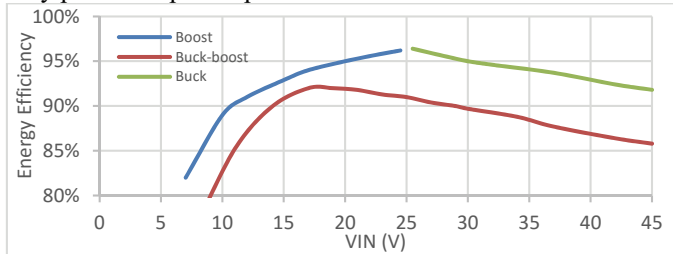


Fig. 3. Measured efficiency comparison between the buck, the buck-boost, and the boost mode of operation ($V_o = 25$ V, $I_{LED} = 1$ A).

The feasibility of energy efficiency improvement with topology transition is evaluated in Fig. 3, where energy efficiencies for the buck, the buck-boost and the boost mode of operation are compared (with $V_o = 25$ V and $I_{LED} = 1$ A). These curves are obtained from a laboratory prototype with a specification listed in Table I. It is clear that the buck-boost mode of operation has a much lower efficiency performance as compared to that of the buck and boost mode. In particular, at low V_{IN} range (e.g. below 25 V), there is at least 2% improvement in the energy efficiency; while at high V_{IN} range (e.g. higher than 25 V), there is more than 5% improvement.

Based on the above discussion, it can be concluded that energy efficiency improvement for a wide input voltage range through the change of the topology is feasible.

III. TOPOLOGY-TRANSITION CONTROL

A. Control architecture of the proposed topology-transition control

To achieve the goal of energy efficiency improvement through the proposed topology-transition process, the system controller should support (i) the three modes of operation simultaneously at the steady state, and (ii) smooth transition

between different modes during the transient of input voltage change. In addition, (iii) the controller should have fast current regulation capability for the purpose mentioned in the introduction section (e.g. PWM dimming). Fig. 4(a) illustrates the overall control architecture of the proposed topology-transition controller which consists of three major control blocks:

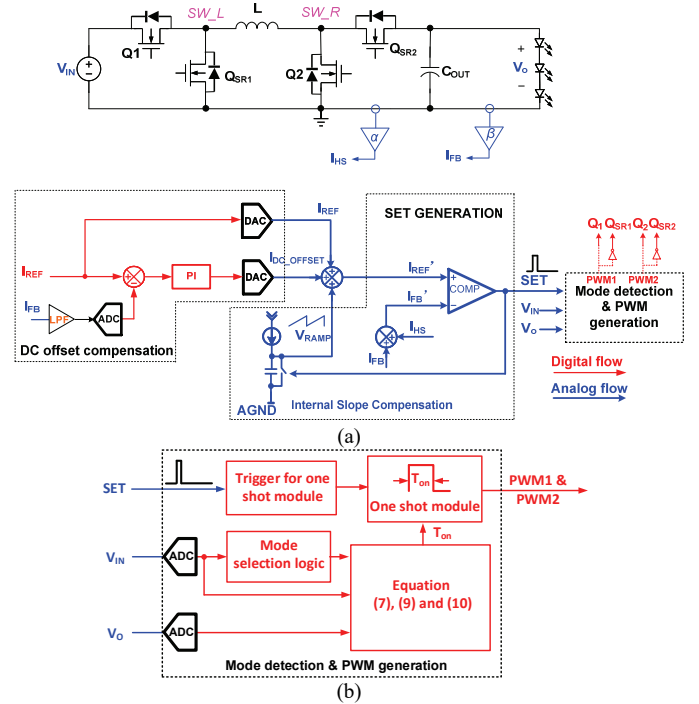


Fig. 4. (a) Simplified architecture of the proposed controller and power stage and (b) Detailed illustration of Mode detection and PWM generation block.

(i) Mode detection & PWM generation block: This block determines the operating mode of the system (and hence the topology to be selected) and generates proper gate drive signals for the active switches Q_1 , Q_{SR1} , Q_2 , and Q_{SR2} . In particular, the gate signals are generated with an adaptive ON-time such that the steady-state switching frequency of the system is constant despite the operating mode. Detailed operating principles of this block will be explained below in this and the following subsections.

(ii) SET generation block: This block enables a fast and preliminary reference tracking of the reference signal I_{REF} with the feedback signal I_{FB} (i.e., the sensed LED current). A SET signal which will be used to initiate the adaptive constant ON-time control in block (i) is generated. To enhance the stability of the inner current control loop, an internal slope compensation circuit producing a ramp signal V_{RAMP} is also augmented.

(iii) DC offset compensation block: This outer block ensures accurate reference tracking of I_{REF} with I_{FB} by generating a shifted reference signal I_{REF}' for the inner current control block to track. Modification of I_{REF} is needed due to the slight dc offset introduced in block (i) and block (iii), as will be explained in detail in IV-B.

Fig. 4(b) illustrates the detailed control logic for block (i). The block has three inputs (SET, V_{IN} , and V_o) and two outputs (PWM1 and PWM2). In particular, the SET signal triggers the one shot module; the level of V_{IN} instantaneously determines

the operating mode of the system (for instance, for $V_{IN} < 20$ V, then operating in the boost mode, and for $V_{IN} > 28$ V, then in the buck mode); Finally, the operating mode, V_{IN} and V_o signal determine the ON-time T_{ON} of the one shot module based on which the gate signals for the four active switches are generated. The process repeats whenever a new SET signal arrives.

B. Steady-state analysis

In this section, V_{RAMP} is assumed zero to simplify the analysis. With reference to Fig. 4(a), we have $I_{REF}' = I_{REF} + I_{DC_OFFSET}$, where I_{DC_OFFSET} is a compensation signal for eliminating the steady-state reference-tracking error as will be discussed below. In addition, both I_{FB} and the high-side switch Q_{SR2} current (I_{HS}) are sensed and summed up formulating a new feedback signal I_{FB}' . The incorporation of I_{HS} essentially introduces nonlinear current information into I_{FB} which enables fast output current tracking capability of the system, regardless of the operating mode.

1) Buck mode of operation

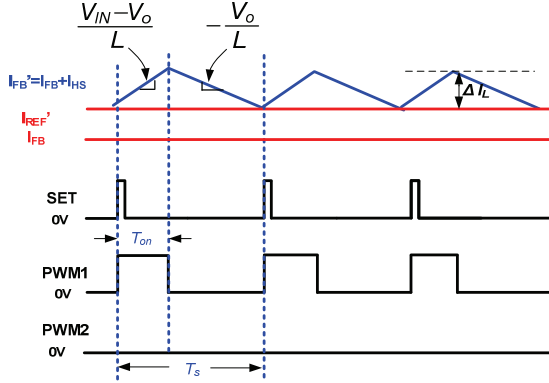


Fig. 5. Adaptive constant-ON-time Modulation in the buck mode.

Fig. 5 shows the steady-state waveforms of the system in the buck mode of operation (with PWM2 signal set to zero). Here, I_{FB} is assumed constant (the small switching ripple is neglected here), and I_{HS} (and hence I_{FB}') has a triangular waveform since I_{HS} equals the inductor current. Each switching cycle is activated by the SET signal from the output of the fast comparator COMP (see Fig. 4 (a)) in block (ii) whenever I_{FB}' falls below I_{REF}' . PWM1 signal is generated by the one shot module in block (i) and remains at high level until a period of T_{on} . Unlike the conventional constant-ON-time control, which has a fixed and preset value of T_{ON} , here T_{ON} is adaptively updated according to (7) in order to ensure a relatively fixed switching frequency $1/T_s$, despite the change of V_{IN} (and hence the name adaptive constant-ON-time control). It should be noted that T_{ON} is updated on a cycle-by-cycle manner with the sensed V_o and V_{IN} information, as described in Fig. 4(b). As a result, the proposed control enjoys both (i) fast time response as that of the conventional constant-ON-time control and (ii) fixed switching frequency at the steady state.

$$T_{ON} = \frac{V_o}{V_{IN}} T_s \quad (7)$$

Based on Fig. 5, the valley of I_{FB}' equals I_{REF}' . This yields

$$I_{FB_valley}' = I_{FB} + \left(I_L - \frac{1}{2} \Delta I_L \right) = I_{FB} + I_{DC_OFFSET} = I_{REF}' \quad (8)$$

where I_L and ΔI_L are the average inductor current (over T_s) and

its ripple, respectively, and I_{DC_OFFSET} represents the discrepancy between I_{FB} and I_{REF}' . As will be shown later, I_{DC_OFFSET} can always be accurately predicted by block (iii) at steady state. Therefore, based on (8), $I_{REF} = I_{REF}' - I_{DC_OFFSET} = (I_{FB} + I_{DC_OFFSET}) - I_{DC_OFFSET} = I_{FB}$, i.e., the steady-state I_{FB} always equals I_{REF} in the buck mode of operation.

2) Boost mode of operation

Similar to the buck mode of operation, the controller can also achieve fast and accurate reference tracking in the boost mode of operation (with PWM1 signal set to high). The detailed operating waveforms are shown in Fig. 6. Again, each switching cycle is activated by the SET signal, and PWM2 is turned OFF after T_{ON} , where

$$T_{ON} = \left(1 - \frac{V_{IN}}{V_o} \right) T_s \quad (9)$$

It can be easily verified by analyzing Fig. 6 that, (8) still holds in the boost mode of operation. Therefore, a dc offset exists between I_{REF}' and I_{FB} . Similar to the buck mode of operation, block (iii) can precisely predict I_{DC_OFFSET} in a closed-loop such that the steady-state current tracking error is zero.

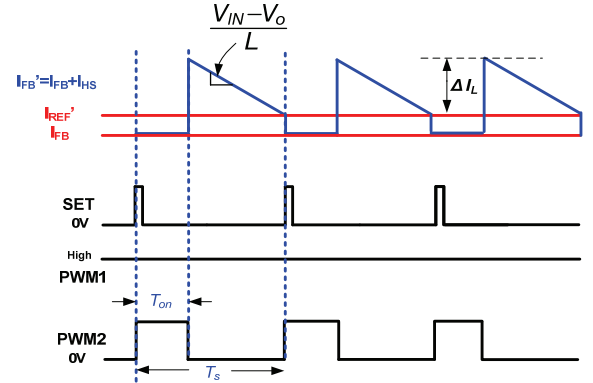


Fig. 6. Adaptive constant-ON-time modulation in the boost Mode.

3) Buck-boost mode of operation

Finally, the steady-state operating waveforms for buck-boost operation is shown in Fig. 7. Since there are two degrees of freedom of designing d_1 and d_2 , the on-time for either PWM1 or PWM2 can be firstly pre-determined to a certain value, and then the on-time for PWM2 or PWM1 can be determined in order to achieve a switching frequency of T_s . For instance, if the on-time for PWM1 is manually selected as T_1 , then T_{ON} for PWM2 can be determined as

$$T_{ON} = \left(1 - \frac{T_1}{T_s} \frac{V_{IN}}{V_o} \right) T_s \quad (10)$$

Based on Fig. 7, one can see that (8) still holds in the buck-boost mode of operation.

It can be seen from the above analysis that the incorporation of the switch current signal I_{HS} into I_{FB} introduces an extra downslope in the final feedback signal I_{FB}' regardless of the operating topologies. Since the current controller always forces the lower boundary of I_{FB}' to be equal to I_{REF} , I_{FB} is regulated indirectly through the regulation of I_{FB}' for all the three topologies.

C. Transient-state analysis

As illustrated in Section III-B, the introduction of the switch current I_{HS} actually regulates I_{FB}' and I_{FB} in a cycle-by-cycle manner. Similar to the conventional current mode control, fast reference tracking can be easily obtained. This feature can be qualitatively described in Fig. 8(a), where the topology is operating in the buck mode.

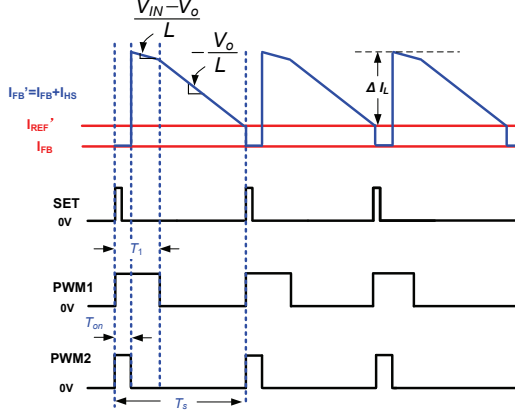


Fig. 7. Adaptive constant-ON-time modulation in the buck-boost mode.

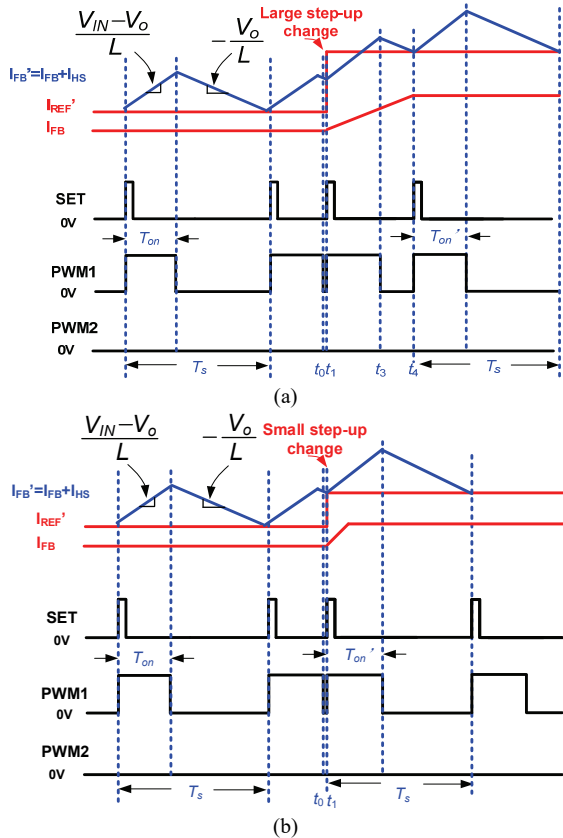


Fig. 8. Fast current reference tracking in buck mode of operation (a) when the change of I_{REF} is relatively huge (b) when the change of I_{REF} is relatively small.

Before the step change of the current reference command at t_1 , PWM1 is OFF and I_{FB}' is linearly decreasing with a slope of $-V_{LED}/L$. At t_1 when I_{REF} undergoes a step-up change (with an incremental value larger than ΔI_L), I_{FB}' is immediately smaller than I_{REF} , and a SET signal is triggered, which further turns on PWM1. The inductor current thus increases almost at the same time of the step-up change of the I_{REF} command for another period of T_{ON} (till t_4) and then decreases again. When I_{FB}' is

again lower than the new reference command at t_4 and another SET signal is triggered, the new steady-state has been reached. It is clear from the above discussions that it takes merely two switching action to track the current references changes. Similarly, when the incremental change of I_{REF} is smaller than ΔI_L , converter always reaches the new current reference in one switching cycle (Fig. 8(b)). A more general and precise small-signal model of buck, boost and buck-boost converter with constant-ON time control can be found in [22], [23].

In addition to reference tracking, seamless topology transition between buck, buck-boost, and boost is also possible with the proposed current controller. Fig. 9 illustrates the operating waveforms when the system transits from buck mode into buck-boost mode of operation as V_{IN} increases. Similar operating waveforms apply also to the cases when the system transits from buck-boost to boost and vice versa.

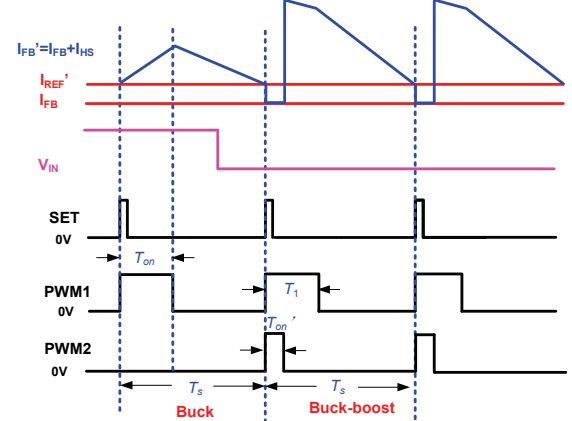


Fig. 9. Topology transition from buck mode to buck-boost mode of operation when the input voltage rises.

IV. DESIGN CONSIDERATIONS

A. Stability improvement

The discussions in Section III are only eligible when the amplitude of the I_{HS} downslope is dominating the ripple portion of I_{FB}' , that is, ΔI_L is sufficiently larger than the current ripples of I_{FB} . At light load condition, when ΔI_L is very low, the current ripples of I_{FB} is more dominant, and the system is becoming unstable (as shown in Fig. 10). This is in part because the level of I_{FB} at light load condition is also low which is susceptible to external noise disturbances. On the other hand, I_{FB} is generally proportional to V_{LED} , and thus the closed-loop control system shifts from a quasi-first-order system into a quasi-second-order system (smaller phase margin) as voltage mode control [23].

To ensure stable operation at light load condition, the proposed controller adds internal slope compensation function in control block (ii) as Fig. 4 shows. The concept is to emulate the effect of the inductor current ripple which effectively turns the control system into a virtual current feedback system. A detailed discussion and design of the external slope compensator is discussed in [23] which is out of the scope of this paper.

Fig. 11 illustrates the operating waveforms during a light load condition in the boost mode of operation. Due to the small current ripple in the inductor, the sum of I_{FB} and I_{HS} only has a small ripple dominated by the dynamics of I_{FB} . The ramp signal V_{RAMP} which is a virtual current is then added. It can be easily

verified that the resulted relationship between I_{FB} and I_{REF} is similar to that shown in (8) and hence I_{FB} can be regulated in the same manner.

The detailed implementation and generation of the V_{RAMP} signal is illustrated in Fig. 4. To achieve small PWM jitter and low cost, an analog circuit is used for the implementation of internal slope compensation instead of a digital-controlled DAC.

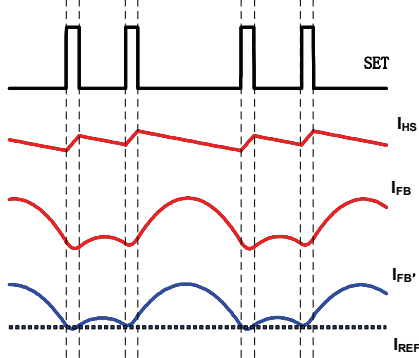


Fig. 10 Operating waveforms when the high-side switch current I_{HS} is low during the buck mode of operation.

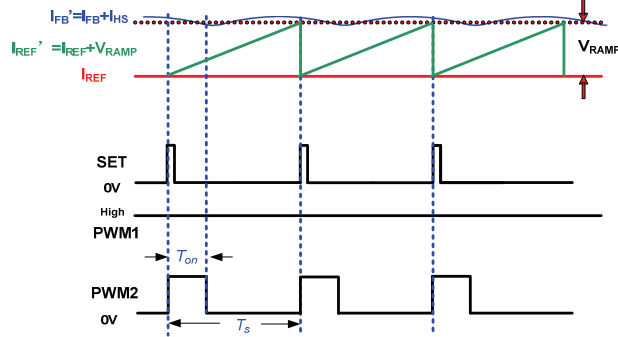


Fig. 11. Slope compensation to improve system stability in boost mode.

B. Steady-state error elimination

As the discussion in Section III-B and IV-A, due to the proposed topology-transition control scheme and the internal compensation, there is still some DC offset between I_{FB} and I_{REF} .

To solve this issue, a simple digital PI compensation loop can be incorporated to remove any steady-state residual DC offset as shown in Fig. 4. As is shown, the feedback signal I_{FB} is firstly filtered by an analog Low Power Filter (LPF). The objective of the LPF is to extract the averaged LED current and reduce the ripple of I_{FB} to improve the performance of the digital PI. To effectively suppress the switching ripple, the cut-off frequency of the LPF is designed to be 1/10 of the switching frequency, i.e., 50 kHz. One ADC then converts the filtered I_{FB} into a digital signal $I_{FB_SENSE}[n]$, which is fed back and compared to $I_{REF}[n]$ and the difference is $error[n]$. A digital proportional-integral (PI) compensator which has an infinite gain at DC is used to force the steady-state error[n] to be zero. The output of PI compensator $V_{TRIM_REF}[n]$ then formulates the true reference signal for the control block (ii) in order to compensate the DC offset. Note that the introduction of the PI compensation loop will not deteriorate the stability of the overall loop due to the inner ramp compensation in the control block (iii). Therefore, a PI compensator with bandwidth high

enough but sufficient lower than switching frequency can be selected in order to achieve fast DC error elimination.

C. Change Point Selection for Mode Transition

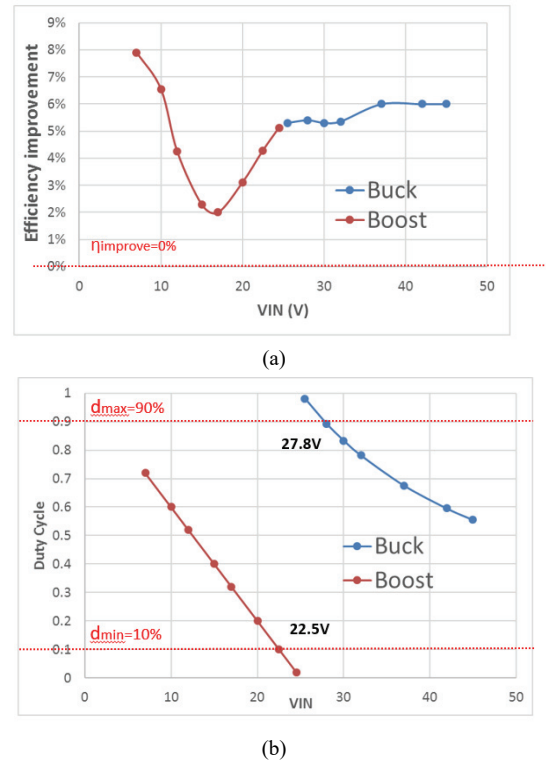


Fig. 12. (a) The measured energy efficiency improvement curve (with buck (7–24 V) and boost (24–45 V) mode of operation only versus with buck-boost mode only) and (b) the calculated duty cycle curves versus V_{IN} (with buck (7–24 V) and boost (24–45 V) mode of operation).

When designing the change points for topology transition, there are two major considerations: (i) the efficiency improvement range, and (ii) the duty cycle range of $Q1$ in the boost mode before entering the buck-boost mode and the duty cycle range of $Q2$ in the buck mode before entering the buck-boost mode. In particular, the efficiency improvement range refers to the input voltage range where the efficiency of buck and boost mode are higher than the buck-boost mode. Additionally, the duty cycle range for $Q1$ and $Q2$ in the buck and boost mode, respectively, should lie within a certain range (e.g. 10% to 90%) to ensure accurate digital implementation and secure system operation.

Fig. 12 illustrate the measured energy efficiency improvement curve and the calculated duty cycle curves versus V_{IN} . It can be seen that throughout the whole operating range of V_{IN} , the energy efficiency is always improved; while the duty cycle curves intersect with the d_{MIN} (10%) and d_{MAX} (90%) line, respectively at 22.5 V and 27.8 V. Therefore, the change point for the buck transferred to the buck-boost can be selected at 22 V, while the change point for the buck-boost transferred to the buck mode is selected at 28 V.

V. EXPERIMENTAL VERIFICATIONS

To verify the effectiveness of the proposed control scheme, a 7–45 V input, 25 V/1A LED strings output prototype is fabricated in the laboratory, as shown in Fig. 13. The prototype consists of three PCB boards, namely, a FPGA control board

(for implementing all the digital control part in Fig. 4(a)), a power stage & signal processing board (e.g. the four-switch buck-boost converter, the internal slope compensation, the generation of the SET signal, and the mode selection logic, etc.), and finally a LED board consisting of 8 CREE XLamp® XM-L LEDs in series. It should be noted that the sizes of the FPGA board and the signal processing part of the second board can be much reduced as they can be easily fabricated into a mixed-signal integrated controller (which is not shown here to prove the concept). Therefore, the overall system is expected to have a compact size. The detailed parameters of the prototype are listed as shown in Table I. Since an LED is current a driven device, its forward voltage range is narrow and almost constant. According to the V-I curve from CREE XLamp® XM-L LEDs device datasheet, the voltage range of the eight LEDs and hence the output voltage range is around 23.2–25.6 V.

TABLE I
EXPERIMENTAL SPECIFICATIONS

Parameter/Component	Specifications
Input Voltage V_{in}	7 – 45 V
Rated LED Current I_{LED}	1.0 A
Rated Output Power	25 W
Q_1 and Q_{SR1}	SQJ850EP (60 V)
Q_2 and Q_{SR2}	SQJ850EP (60 V)
Power Inductor L	10 μ H
Input Power Capacitor	100 μ F, (80 V)
Output Power Capacitor	680 μ F (50V)
FPGA	Xilinx XC6SLX25
FPGA Memory	Xilinx XCF16PVO48C
ADCs	ADS7887 and MAX4617
DACs	DAC902E and AD5308
Oscillator	20MHz and 40MHz oscillator

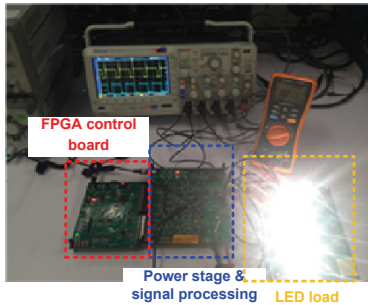


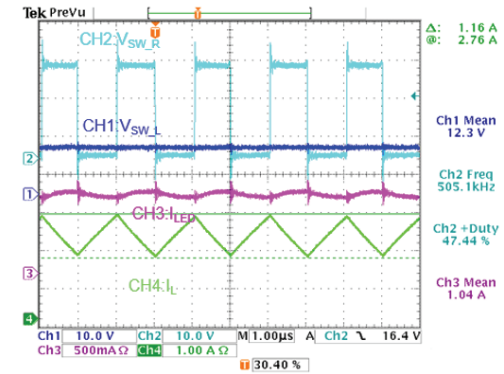
Fig. 13. Experimental hardware prototype with three separate boards.

A. Steady-state operating waveform in buck, boost, and buck-boost mode of operation

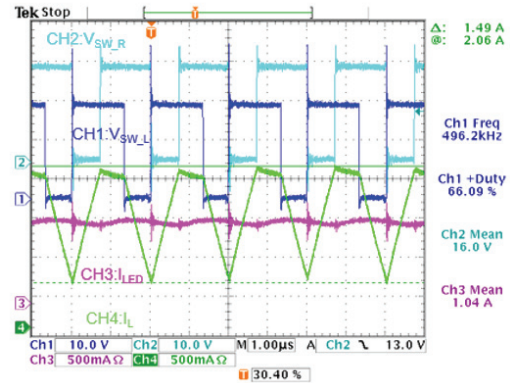
Fig. 14 shows the measured voltage waveforms of buck cell common switching point V_{SW_L} and boost cell common switching point V_{SW_R} , and the measured current waveforms for the LED string and the power inductor at different modes.

When the input voltage is 12 V (Fig. 14(a)), the proposed digital controlled buck-boost converter operates at the boost mode, with the boost cell operating at exactly 500 kHz, and the buck cell's high side switch Q_1 ON. Similarly, when the input voltage is 24 V (Fig. 14(b)), the four-switch buck-boost converter is operating in the buck-boost mode, with both the

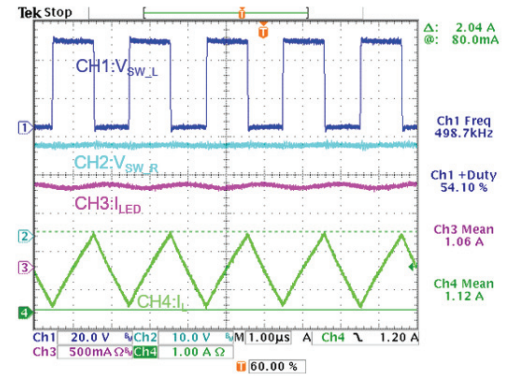
buck and boost cells operating at 500 kHz. Finally, when the input voltage is 45V (Fig. 14(c)), the converter operates in the buck mode, the buck cell is still operating at 500 kHz, with the boost cell synchronous rectifier is on. The above results show that the proposed controller supports all the three mode of operation.



(a)



(b)



(c)

Fig. 14. Operating waveforms when (a) $V_{in} = 12$ V in boost mode (b) $V_{in} = 24$ V in buck-boost mode and (c) $V_{in} = 45$ V in buck mode. I_L : operating waveform of Inductor current. I_{LED} : operating waveforms of the LED current. V_{SW_L} : voltage at the switching node SW_L. V_{SW_R} : voltage at the switching node SW_R.

B. Dynamic waveforms during topology transition

Fig. 15 shows the measured transient voltage and current waveforms of the converter during the topology transitional period among buck mode, buck-boost mode and boost mode. Due to the robustness and fast reference tracking capability of the proposed topology-transition controller, there is no overshoot/undershoot in the inductor current. Importantly, the output LED current is almost constant and disturbance-free

before, during and after the transient. Therefore, seamless topology transition between buck, boost and buck-boost mode has been demonstrated with the proposed control.

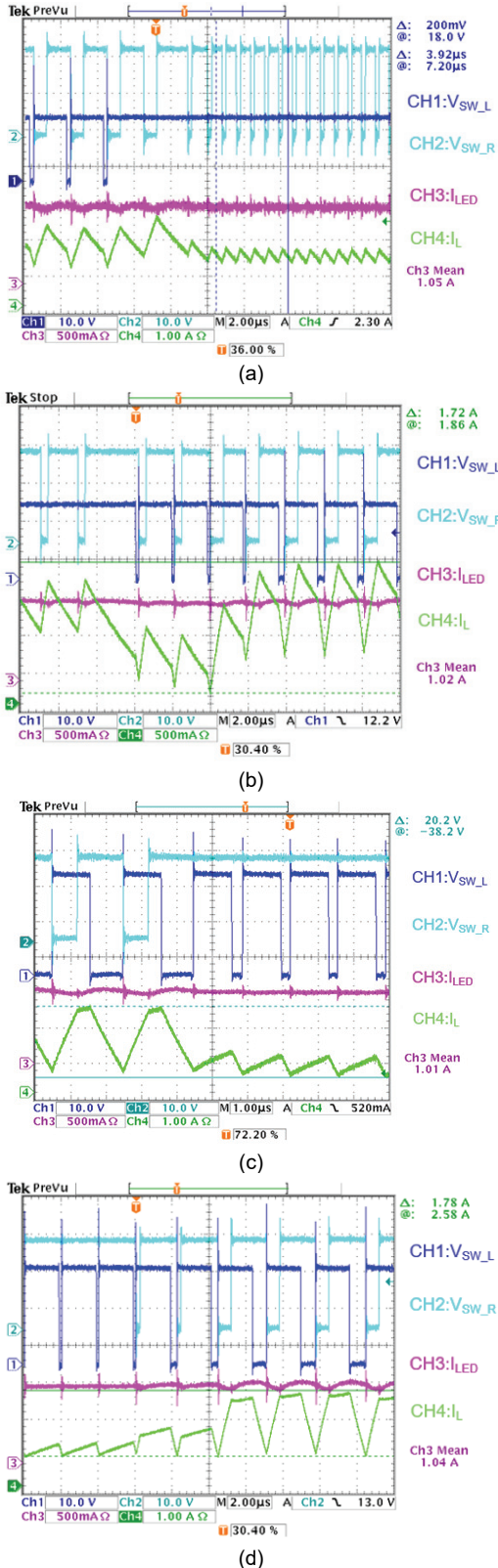


Fig. 15. Transient operating waveforms ($V_o = 24$ V, $I_{LED} = 1$ A) when (a) V_{IN} changes from 24 V to 12 V, transitional period from buck-boost to boost mode (b) V_{IN} changes from 12 V to 24 V, transitional period from boost to buck-boost mode (c) V_{IN} changes from 24 V to 30 V, transitional

period from buck-boost to buck mode and (d) V_{IN} changes from 30 V to 24 V, transitional period from buck to buck-boost mode. I_L : operating waveform of Inductor current. I_{LED} : operating waveforms of the LED current. V_{SW_L} : voltage at the switching node SW_L. V_{SW_R} : voltage at the switching node SW_R.

C. Efficiency performance

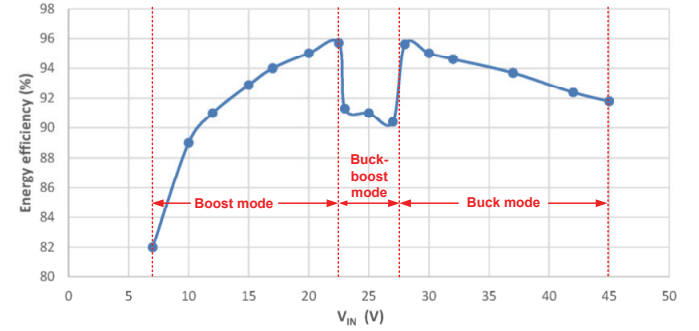


Fig. 16. Measured energy efficiency versus V_{IN} .

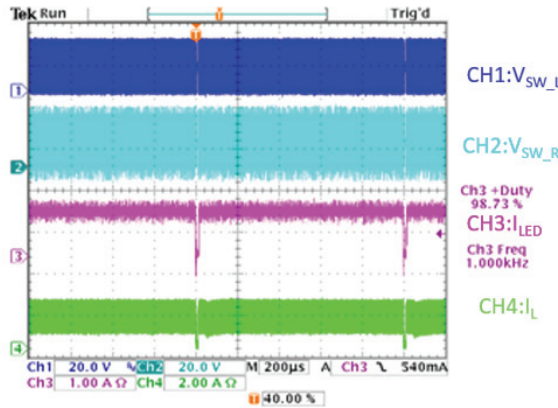
Fig. 16 shows the measured energy efficiency performance of the proposed LED system tested at different input voltage level with an LED output current of 1 A. The two topology transition voltage points are selected at $V_{IN} = 22$ V and $V_{IN} = 28$ V, as explained in Section IV-C. In Fig. 16, there is a drop of energy efficiency when the converter transits to the buck-boost mode from buck and boost mode of operation. The drop of efficiency is due to the operation in the buck-boost mode where all the four active switches are ON, which is expected according to Fig. 3. Fortunately, the input voltage range for the buck-boost mode is limited. The proposal can effectively improve the energy efficiency performance in the sense of a wide-input-voltage-range operation. Throughout the whole input voltage range, an efficiency higher than 82% has been achieved.

D. PWM dimming performance

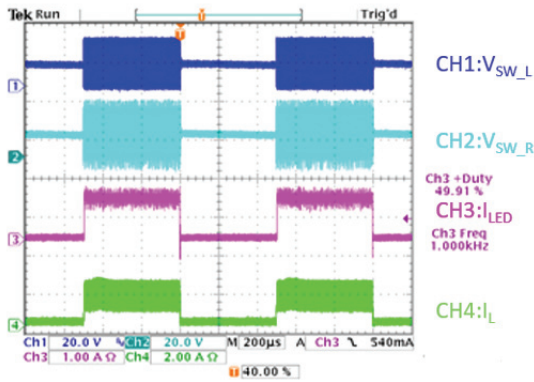
In LED lighting applications, it is highly desirable to achieve precise and full-range dimming control of the LED current. In particular, precise dimming means that the average LED current (over one dimming period) can be precisely and linearly controlled by the dimming duty cycle D_{DIM} , while full-range dimming means that the average LED current can be adjusted from 0% to 100%. PWM dimming method can easily achieve precise and full-range PWM dimming as compared to conventional analog dimming, provided that the LED current can be turned on/off with minimum rising/falling time [24]. One popular method to implement PWM dimming is to periodically change the output current reference from a high level (e.g. 1 A) to a low level (i.e., 0 A) at a fixed frequency (which is the dimming frequency). By changing the duty ratio of the high-level period over the dimming period, the averaged LED current can be precisely controlled.

Fig. 17 shows the measured transient voltage and current waveforms of the converter during PWM dimming period. With the fast reference tracking capability, the converter achieves full range (0% to 100%) and precise dimming (i.e., 1% dimming precision) easily. The transition from dimming OFF condition to ON condition is also shown in Fig. 17(d). It is evident that the transition is fast and it takes no more than two switching action to track the current references changes without any current spike. Finally, Fig. 18 illustrates the PWM

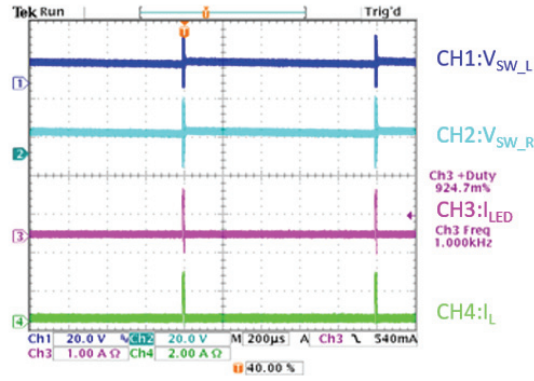
dimming curve at different input voltages. It can be seen that precise dimming performance has been achieved at all input voltage levels.



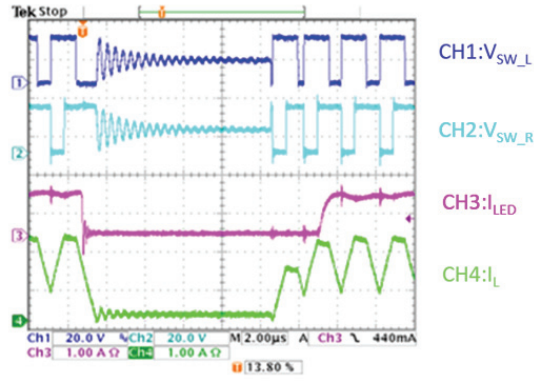
(a)



(b)



(c)



(d)

Fig. 17. Transient operating waveforms during PWM dimming (a) overview when dimming duty = 99% (b) overview when dimming duty =

50% (c) overview when dimming duty = 1% (d) close-up view of the dimming ON/OFF period. I_L : operating waveform of Inductor current. I_{LED} : operating waveforms of the LED current. V_{SW_L} : voltage at the switching node SW_L. V_{SW_R} : voltage at the switching node SW_R.

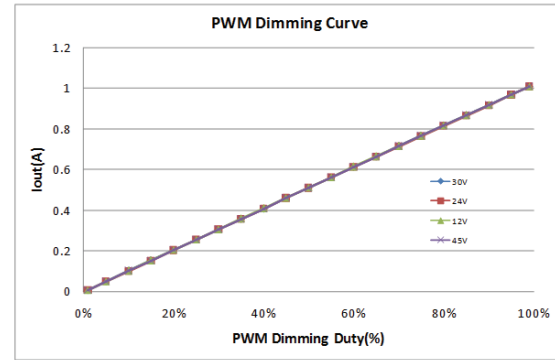


Fig. 18. Measured average LED current versus the PWM dimming duty at various input voltage levels.

VI. CONCLUSION

In this paper, a novel topology-transition controller is proposed. It can change the circuit topology according to the level of the input voltage. This leads to a significant efficiency improvement for a wide input voltage range by more than 5%, as compared to the conventional four-switch buck-boost converter without topology transition control. In addition, the controller achieves superior and robust dynamic performance. Fast reference tracking is obtainable through a single set of controller. With the proposed control, full range and high precision PWM dimming can be easily performed.

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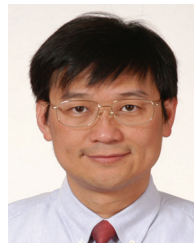
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