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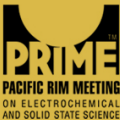
Comparison of 1T1R and 1C1R ReRAM Arrays

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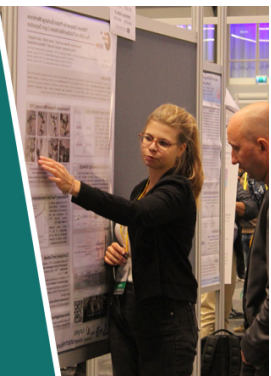
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Comparison of 1T1R and 1C1R ReRAM Arrays

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Abstract. The rise of memristors with potential applications in memory has attracted wide interests. Memristors are typically assembled in crossbar arrays with data bits encoded by the resistance of individual cells. The 1T1R cell structure is the most popular for memristive memory as it eliminates sneak path currents. The transistor not only allows for flexible selection of memory cells but also facilitates the programming for computing-in-memory applications. In this paper, we replace the selector in the 1T1R configuration with a capacitor to form a selectorless and passive combination of ReRAM structure. Moreover, we evaluate the merits of the two structures in SkyWater 130nm CMOS technology by comparing the writing technique, power consumption, switching speed, and memory density. Furthermore, we compared the complexity of the readout method between 1T1R and 1C1R for a memory application. This work shows that the 1C1R configuration is a promising memory structure that consumes less energy, switches faster, has higher density, and has a simpler readout method when compared to 1T1R.

1. Introduction

Professor Chua and researchers from the Hewlett-Packard (HP) lab conceptualized and demonstrated the memristor, which is the fourth passive electronic element [1]. Essentially, the HP memristor [2, 3] is a resistive switch consisting of a dielectric layer sandwiched between two electrodes. The distinctive characteristic of a memristor is that its conductance is dependent on previous electrical signals, allowing it to function as a Non-Volatile (NV) Resistive Random Access Memory (ReRAM). In addition, ReRAM may store multibit information with continuously tunable conductance, unlike the binary "0" and "1" states of conventional digital storage devices, granting them a greater bit density. Non-volatility, rapid programming, low programming energy, and a small footprint make memristors an attractive option for the next generation of embedded memory, which may combine the benefits of SRAM and floating-gate transistors. In addition to memory and storage, memristors intrinsically imitate the dynamic behaviors of synapses and neurons, owing to their bias-history dependent conductance, which has led to the development of numerous memristor-based artificial and spiking neural networks (SNNs) [4].

Memristors or ReRAM with their simple two-terminal metal-insulator-metal (MIM) architecture allow them to be integrated into dense crossbar arrays [5, 6]. As depicted in Figure 1(a), a conventional crossbar array comprises of parallel metal lines, referred to as word lines and bit lines, at the perpendicular top and bottom electrodes. Memristors with two terminals are formed at the intersections of word and bit lines. The red cylinder represents a selected cell during the operation to read its conductance (the black solid line). In this readout process, as depicted in Figure 1(a), an undesired current flows along multiple sneak paths, represented by the red solid line, which is analogous to parallel series resistors in Figure 1(b). Such sneak pathways would result in additional energy consumption from unselected cells, hence reducing the read margin and limiting the array size. The sneak path current could lead to a failed write operation on the targeted cell, an unwanted write action on an unselected cell, and a failed read operation [7].



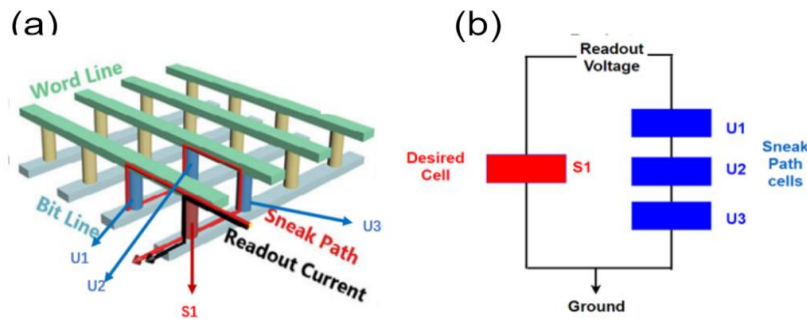


Figure 1. (a) 3D schematic of crossbar array architecture (b) The equivalent circuit.

Selector devices coupled to the memristor at each node can eliminate sneak path current. These methods involve engineering the unit cells, such as providing an access element to the 1-ReRAM (1R) cell to generate composite cells such as one-transistor-one ReRAM (1T1R), one-capacitor-one ReRAM (1C1R), one diode-one ReRAM (1D1R), and one selector-one ReRAM (1S1R), as well as self-rectifying memristors. Not only can the insertion of the access device enhance energy efficiency during array programming, but it may also help memristors achieve synaptic plasticity, hence allowing innovative analogue machine learning and neuromorphic computing.

In this paper, a comprehensive comparison between 1T1R (T: NMOS transistor) and 1C1R (C: Metal–Insulator–Metal (MIM) capacitor) is made. The objective of this comparison is to investigate the most common structure in memristive crossbar array with the new structure of the 1C1R that we have recently published [8]. In this comparison, we explore their differing writing techniques, power consumption, switching speed, memory density, and readout complexity for 1T1R and 1C1R. The remainder of this paper is organized as follows. Section 2 briefly reviews the 1T1R and 1C1R structures. Section 3 presents writing/programming technique. Section 4 introduces the switching speed comparison. Section 5 provide the power consumption comparison. Section 6 presents the memory density comparison. Section 7 provides readout complexity comparison. Finally, Section 8 concludes this paper.

2. 1T1R and 1C1R structures

2.1. 1T1R

The 1T1R crossbar architecture resembles that of DRAM in many ways. The transistor not only enables the flexible selection of memory cells, but also facilitates the development of applications that do computations in memory.

Figure 2(a) depicts a 1T1R structure. The 1T1R structure has three terminals that are connected to the memory array which are word line (WL), source line (SL), and bit line (BL). The activities of a ReRAM cell depend on the duration of the access time and the supply voltage applied to WL and SL.

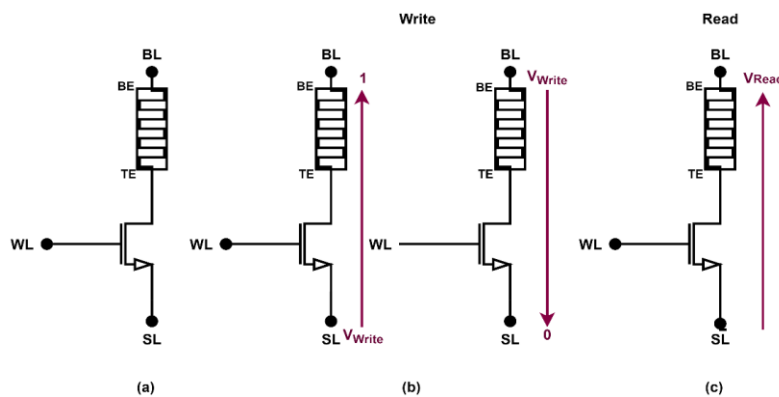


Figure 2. (a) 1T1R cell. (b) Bias conditions of write operations. (c) Bias conditions of read operation.

Figure 2(b) depicts the biased circumstances during a write operation. If a Write bit-1 operation is executed, V_{w0} is applied to SL and BL is connected to ground, resulting in a low resistance state (LRS) condition for the ReRAM. V_{w1} is applied to BL and SL is connected to ground during a Write bit-0 operation, which alters the resistance of the ReRAM to a high resistance state (HRS). To read the data from a selected cell, a small read voltage V_{read} is applied to SL and BL is connected to ground, as seen in Figure 2(c), so that the read current is less than the threshold current for changing the state of the ReRAM.

2.2. 1C1R

1C1R was recently introduced as a novel technique whose structure consists of one capacitor and one memristor coupled together in series [8]. As depicted in Figure 3, 1C1R is a two-terminal construction with the top plate of the capacitor connected to WL and the bottom plate of the ReRAM connected to BL.

The 1C1R structure is inherently a high pass filter (HPF) that makes the capacitor an access device in which the applied pulse frequency determines the selection of the cell. Consequently, by controlling the pulse frequency applied to the 1C1R, we can always use it as an open or closed switch to allow or block the flow of the current through the ReRAM.

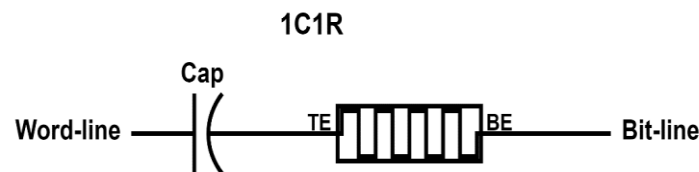


Figure 3. 1C1R structure schematic.

3. Writing/programming technique

To store bits inside the ReRAM cell, each binary bit (0 or 1) is assigned a resistance value; $R=3.38 \text{ M}\Omega$ (HRS) and $R=10.07 \text{ K}\Omega$ (LRS) correspond to bit 0 and bit 1 respectively in this technology. Programming algorithms employ programming pulses, or voltage pulses, to precisely tune the target cell resistance to the desired value; often, numerous pulses are necessary due to the unpredictability of ReRAM cells. The energy and latency of a ReRAM write operation are dependent on the number and width of the programming pulses; consequently, it is essential to reduce the number of programming pulses for quick and low-energy writes.

ReRAM needs an abrupt change in its voltage in order to change its resistance state. A pulse signal is an example of programming signals that change its value rapidly and is used widely in memory applications in 1T1R. Moreover, ReRAM switches its resistance value at the rise edge of the signal applied to it and keeps its resistance value until the next pulse. However, pulse signal suits 1T1R more than 1C1R because of the HPF structure of the 1C1R. If we were to use a pulse signal, the pulse width used to write onto the ReRAM in 1C1R would have to be significantly smaller than RC , resulting in a very high frequency pulse signal, unless a very big capacitor is used, which is difficult to achieve. Therefore, an alternative technique to program the ReRAM in 1C1R structure while keeping the frequency realizable is to use a reverse ramp signal, as depicted in Figure. 4, which has a very rapid rise time and a slow fall time so that the ReRAM can see the change in the rise time and will not be able to see the slow change in the fall time.

3.1. 1T1R

There are five factors that affect the state the programming for 1T1R:

- **Pulse Amplitude:** higher absolute bias voltage induces faster changing and less pinpointing on the memristance.

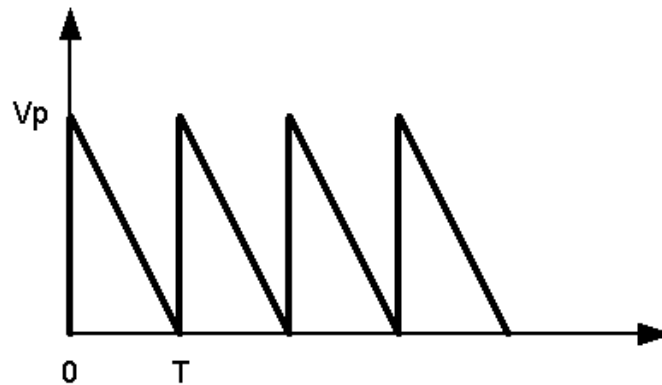


Figure 4. A reverse ramp signal used for writing operation in 1C1R.

- **Pulse Width:** a pulse with a smaller width can be applied to slow down the changing rate of the memristance. Applying a large pulse width results into a smaller number of pulses needed to switch the memristor from HRS to LRS.
- **Number of Pulses:** a specific Memristance can be achieved by increasing/decreasing the number of pulses that helps to program the device in an accurate resistive state.
- **Transistor area:** higher transistor (W/L), faster resistance switching due to higher drain current.
- **Transistor Type:** nMOS transistors offer greater mobility compared to pMOS, allowing them to be smaller while maintaining the same current-driving capacity.

3.2. IC1R

Four criteria affect the memristance switching:

- **Rise time:** less rise time, fast resistance switching. Figure.5 illustrates different rise times with their respective resistance switch.
- **Fall Time:** As we increase the fall time to be more than $5RC$, faster memrsitance changing rate, and if the fall time is close to $5RC$, slower resistance switching rate happening and this is because the capacitor will have enough time to charge and settle, hence, the memristor voltage amplitude is the same as the applied signal amplitude. In contrast, fall time that is much less than RC , switch off the memristnace changes. In this case, ReRAM reverse ramp amplitude is almost half of the applied amplitude because the capacitor will not have enough time to charge and reach its maximum value due to the short reverse ramp signal, hence, the voltage across the ReRAM decreases.
- **Capacitance Value:** given the rise and fall time is fixed, more capacitance value will cause large time constant (RC), thus slow capacitor charging, leads to large memristor spike width, which leads to fast memristance changing rate.
- **Amplitude:** higher absolute bias voltage amplitude, leads to fast resistance switching.

4. Switching speed

Switching speed is an important metric for comparing 1T1R and 1C1R. It specifies the duration over which the ReRAM changes from HRS to LRS or vice versa. Pulses with a 3V amplitude and 100ps width were applied to the 1T1R and 1C1R structures. As illustrated in Figure.6, the switching speed of the 1T1R is roughly 811 ns, but the speed of the 1C1R is merely 1.07 ns. 1C1R swaps at a rate approximately 800 times faster than 1T1R. 1T1R is slower due to the ON-resistance (R_{ON}) of the transistor, which reduces the current passing through the memristor and therefore the speed. In

addition, the 1C1R is faster because, when a very short duration pulse is applied, the structure acts as standalone memristor (1R) since the capacitor acts as a short circuit.

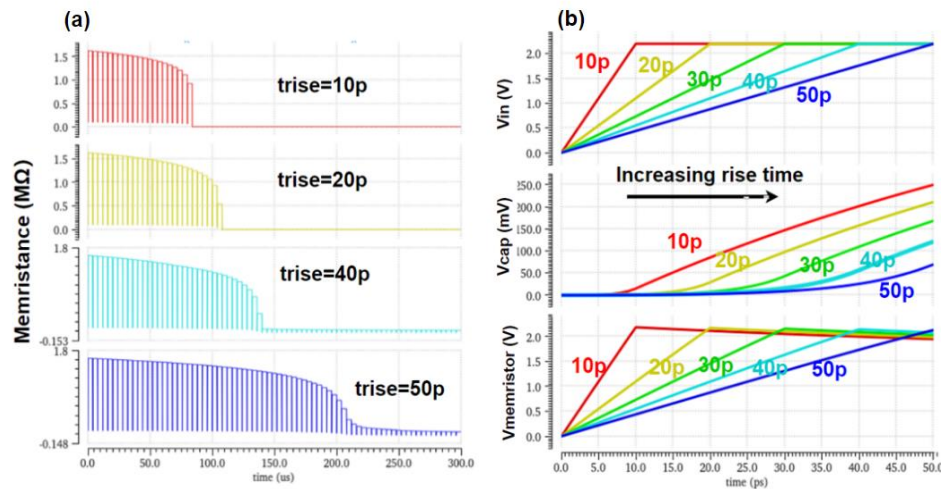


Figure 5. (a) ReRAM behaviour (b) voltage across the capacitor and the ReRAM with different rise time of ramp signal.

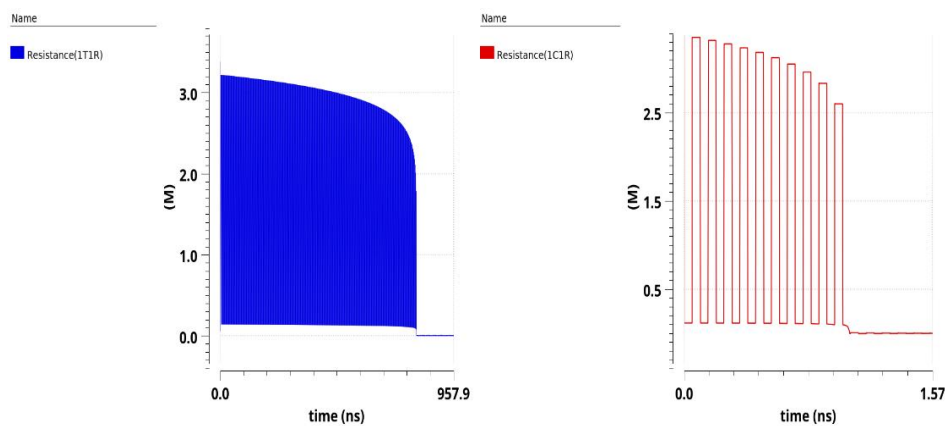


Figure 6. Switching speed comparison (a) 1T1R (b) 1C1R (pulse amp= 2.5V, pulse width=100ps).

5. Power consumption

When comparing 1T1R and 1C1R, power consumption is another crucial statistic. In this comparison, we evaluate the power consumed for the two structures to switch from HRS to LRS or LRS to HRS. With pulses of 2.5 V amplitude and 100ps width, the single 1T1R structure consumes roughly 1.06 mW of average power, whereas the 1C1R structure consumes approximately 57.75 μ W with the same pulse amplitude and width.

The power consumption of 1T1R and 1C1R can vary depending on the transistor area and capacitance value respectively. Therefore, in order to determine accurately which structure is better for switching speed and power consumption when operating at the same pulse frequency and amplitude, we compared the power consumption while maintaining the same switching speed for both structures and compared the switching speed while maintaining the same power consumption. We fixed the same power consumption and switching speed by changing the transistor area in 1T1R and capacitor value in 1C1R. Table 1 summarizes the power consumption comparison and switching energy when switching speed is the same.

1C1R consumes less power than 1T1R because of the absence of DC conductance in the capacitor, which prevents the DC bias in the 1C1R array. On the other hand, the transistor ON-resistance of the 1T1R plays a roll of increasing the power consumption. In 1T1R, the transistor functions as a switch with static power consumption, whereas in 1C1R, the capacitor serves as an energy source to power consumed by the memristor when the voltage across the capacitor is negative.

Table 1. Power consumption comparison with the same switching speed.

	1T1R	1C1R
Switching Speed	1.07ns	1.07 ns
Power Consumption	3.13 mW	1.13 mW
Switching Energy	3.34 pJ	1.20 pJ

Table 2 summarizes the switching speed and switching energy comparison and when the power consumption is the same. 1C1R has a faster switching speed when both power consumptions are the same. This is because 1C1R acts like a standalone memristor (1R) when a high frequency pulse is applied to 1C1R. In addition, the ON-resistance will slow down the switching speed in 1T1R because it will lower the amount of current that flows through the memristor.

Table 2. Switching speed comparison with the same power consumption.

	1T1R	1C1R
Power Consumption	1.16 mW	1.13 mW
Switching Speed	1.017 μ s	1.07 ns
Switching Energy	1.17 nJ	1.20 pJ

6. Memory density

Memory density is among the most critical aspects of memory technology to enable the design of multibit capacity memory cells. The memory density of a crossbar array depends mainly on the transistor and capacitor sizes for 1T1R and 1C1R respectively. There is a tradeoff between power consumption, switching speed, and transistor and capacitor areas. In 1C1R, the switching speed gets faster when the capacitor area increases, but it will consume more power and reduce the memory density. On the other hand, 1T1R consumes much power when the transistor area increases, but the switching speed gets faster. Overall, transistor area of 1T1R may be lower than capacitor area of 1C1R, hence, it has more memory density. The capacitor in 1C1R size could be reduced to be comparable to the transistor area of 1T1R but this will affect the switching speed. Figure.7 illustrates the power consumption and switching speed for difference transistor and capacitor sizes for 1T1R and 1C1R respectively.

7. Readout complexity

A crucial aspect of the design of a readout circuit is ensuring that the ReRAM state (resistance) does not change during the operation. The voltage and current ranges in which the state of a ReRAM changes might vary from device to device due to the manufacturing process, resulting in several models.

The design of readout circuits has been the subject of extensive studies due to the challenges of current solutions [9-11]. In this comparison, we compare the complexity of the most common readout solution for 1T1R, and readout technique used in 1C1R.

7.1. 1T1R

Most 1T1R structure use a Trans-Impedance Converter (TIA), and Analog to Digital Converter (ADC) for readout [9]. The TIA is used to sense the current passing through the device under test (DUT) and convert to voltage, then an ADC is followed to digitize the sensed voltage [12]. This requires feedback loops and consequently the reading time is not well bounded. Furthermore, TIA's converted voltage is too small to be read with high accuracy when the sensed current is extremely low for HRS. In contrast, the TIA cannot guarantee that the virtual ground is stable if the current is extremely high in case of LRS. ADCs and operational amplifiers are required in this readout solution, which results in the large size of the readout circuits.

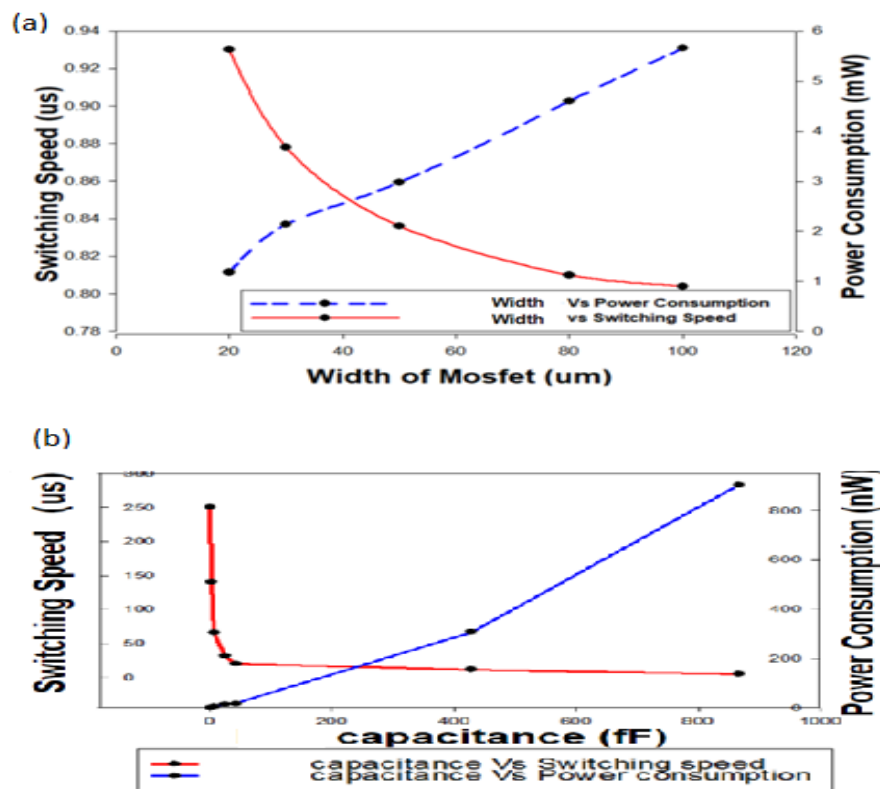


Figure 7. (a) The relationship between the transistor width, speed, and power consumption in 1T1R from HRS to LRS, (b) The relationship between the capacitance, speed, and power consumption in 1C1R from HRS to LRS.

7.2. 1C1R

Reading-out in 1C1R structure is much simpler than 1T1R. One direct method is to measure the ReRAM state by employing only one capacitor (C_R) connected from bitline to ground. Then, applying a low voltage pulse (V_{Read}) with a long duration and measuring the voltage time constant (RC) at 36.8% of the C_R voltage, then divide the time measured by the capacitance value to estimate the resistance value.

Alternatively, time domain approach can be used for more readout accuracy. To read the ReRAM state more accurately, a Time to digital Converter (TDC) is used as a digitizer to convert the electrical signal into a digital code. The idea behind this is the development of a relationship between the resistance of the ReRAM representing its state and the time it takes C_R to fully charge and reach V_{Read} . The charging rate is controlled by the value of the resistance value of the ReRAM.

8. conclusion

The most prevalent structure for memristive memory that eliminates sneak path currents is the 1T1R. Not only does the transistor permit flexible selection of memory cells, but it also facilitates programming for systems that do computation in memory. In this work, we replace the selector in the 1T1R structure with a capacitor to create a selectorless, passive ReRAM and capacitor combination (1C1R). In addition, we compare the writing process, power consumption, switching speed, and memory density of the two structures in SkyWater 130nm CMOS technology to assess their strengths. Furthermore, we investigated the readout method complexity of 1T1R and 1C1R for a memory application. This comparison demonstrates that the 1C1R configuration is a potential memory structure that consumes less energy, less than 70% of 1T1R's, switches faster (>500 times of 1T1R's), has a comparable density to 1T1R, and has a simpler reading mechanism than 1T1R.

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