FREQUENCY MULTIPLICATION USING NON-LINEAR CAPACITANCE EFFECTS OF P-N JUNCTION DIODES

A THESIS presented by David. J. Roulston

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Department of Electrical Engineering,

Imperial College of Science and Technology.

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SUMMARY

Frequency multiplication using the non-linear capacitance formed by the depletion layer of a reverse biassed p-n junction diode is studied with a view to obtaining a complete and generally applicable solution to the problem. The solution is presented for two basic circuit configurations in the form of a series which may be evaluated for any diode and for any order of harmonic. Results are included in the form of power loss and design curves for three orders of multiplication for various diode characteristics and for various diode and circuit 'Q' factors. From these curves the performance of different multipliers is compared and conclusions are drawn as to the choice of circuit and diode for maximum efficiency multipliers.

The effect of driving the diode into the forward conduction region is studied both as an extension to the depletion layer mode of operation and as a distinctly different mechanism for frequency multiplication.

A circuit analysis allows the estimation of various additional losses including the use of non-ideal filters and unwanted harmonic power being dissipated in the diode and in the load. Methods of eliminating these losses are suggested.

Problems which occur in practical circuits are discussed. These include methods of biassing the diode, behaviour when the input amplitude is not constant, matching conditions and requirements for cascading circuits.

The basic large signal theory is verified experimentally and operation of various circuits is illustrated at both low (1 Mc/s. to 10 Mc/s.) and high (300 Mc/s. to 1200 Mc/s.) frequencies.

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TABLE OF CONTENTS

	Page
Title	1
Summary	2
Acknowledgements	3
Table of contents	4
List of symbols	9
INTRODUCTION	
Definition	17
Historical survey - Methods and applications	17
Reasons leading to present work	18
Work already carried out in the field	19
Purpose of project	19
Outline of project	20
DISCUSSION OF ORIGINAL WORK	21
1. BASIC CONCEPTS AND CIRCUITS	
1.1 Introduction	23
1.2 Diode characteristics	23
1.3 Basic circuits	25
1.4 X2 Node circuit	
1.4.1 Analysis	26
1.4.2 General behaviour of circuit	30
1.4.3 Requirements for high efficiency circuits	32
1.4.4 Experimental results	34
1.4.5 Conclusions	37
1.5 X2 Mesh circuit	
1.5.1Analysis	37
1.5.2 General behaviour of circuit	40
1.5.3 Requirements for high efficiency circuits	42
1.5.4 Experimental results	43
1.5.5 Conclusions	44

1.6 General conclusions 44
Figures 46

2.LARGE SIGNAL DEPLETION LAYER ANALYSIS

2.1 Introduction 51
2.2 Basic analysis
2.2.1 Node circuit 51
2.2.2 Mesh circuit 55
2.2.3 Discussion of the series involved in the preceding analysis 59
2.2.3.1 General considerations 59
2.2.3.2 Node circuit 60
2.2.3.3 Mesh circuit 61
2.2.4 Limiting conditions of signal across the junction
2.2.4.1 Node circuit 62
2.2.4.2 Mesh circuit 63
2.3 Evaluation of power loss
2.3.1 Node circuit 65
2.3.2 Mesh circuit 66
2.4 Discussion of the theoretical results
2.4.1 Assumptions and limitations in the theory 67
2.4.2 Comparison of various circuits using the power loss curves
2.4.2.1 Node circuit 69
2.4.2.2 Mesh circuit 71
2.4.2.3 General remarks 72
2.4.3 Active behaviour of specific circuits 72
2.5 Experimental results
2.5.1 Introduction 74
2.5.2 Node circuit 74
2.5.3 Mesh circuit 75
2.6 Conclusions 76
Table I 78
Figures 79
Appendices 107

3. CONSIDERATION OF CHARGE STORAGE EFFECTS

3.1 Introduction 112

3.2 Theoretical analysis of a charge storage multiplier

3.2.1 Basic ideas 113

3.2.2 Analysis of tuned output circuit 114

3.2.3 Analysis of tuned and matched input, broadband output circuit 120

3.3 Discussion of results 122

3.4 Experimental results 125

3.5 Conclusions 127

Figures 128

Appendices 139

4. SOURCES OF DECREASED EFFICIENCY WHEN USING PRACTICAL CIRCUITS

4.1 Introduction 141

4.2 Losses due to finite resistance in circuit filters

4.2.1 Node circuit 141

4.2.2 Mesh circuit 143

4.2.3 Discussion of results for the node circuit 143

4.2.4 Discussion of results for the mesh circuit 149

4.3 Effect of finite reactance of filters

4.3.1 Introduction 150

4.3.2 Modification of power loss expression 150

4.3.3 Modification of filter 'Q' factors due to coupled losses 155

4.3.4 Conclusions 157

4.4 Harmonic losses due to finite loaded 'Q' factor of input and output circuits

4.4.1 Introduction 159

4.4.2 Analysis of node circuit losses 159

4.4.3 Illustration of node circuit losses 163

4.5 Rigorous solution of efficiency for the node circuit under lossy diode conditions 166

4.6 Harmonic losses in series resistance of diode 169

4.7 Losses due to forward conduction
4.7.1 Practical effect of driving diode into conduction 172
4.7.2 Theoretical estimation of losses 172
4.7.3 Conclusions 175
4.8 Effect of stray diode reactances
4.8.1 Lead inductance 177
4.8.2 Shunt capacitamce 178
Figures 180
Appendices 197

5. GENERAL DETAILS OF DEPLETION LAYER CIRCUITS INCLUDING CASCADING

5.1 Introduction 199
5.2 Biassing arrangements 199
5.3 Voltage relationships
5.3.1 Node circuit 201
5.3.2 Mesh circuit 205
5.3.3 General conclusions 207
5.4 Hysteresis effects 207
5.5 Effect of de-tuning a circuit 211
5.6 Input matching and power handling capabilities
5.6.1 Node circuit 214
5.6.2 Mesh circuit 216
5.7 Cascading considerations
5.7.1 Introduction 217
5.7.2 Matching conditions between adjacent stages 218
5.7.3 Estimation of efficiency using the results of previous sections 224
5.7.4 Estimation of additional losses 226
5.7.5 Conclusions 227
5.8 Conclusions 228
Figures 229

6. SOME GENERAL EXPERIMENTAL RESULTS

6.1 Introduction 233

6.2 Low frequency circuits

6.2.1 Single stage circuit 233

6.2.2 Cascaded circuit 237

6.2.3 Illustration of hysteresis effect 240

6.3 High frequency circuits

6.3.1 Description of circuit 241

6.3.2 Measurements of power loss 242

6.3.3 Behaviour when input is varied 245

6.4 Conclusions 246

Figures 247

CONCLUSIONS 254

Bibliography 257

SYMBOLS

Symbol	Definition	Page of first appearance
A_1, A_m	Fourier co-efficients given in Appendix 3.1	116
${}^mA_i$	Co-efficient of cos iθ in expansion of $\cos^m\theta$	53
B_1, B_m	Fourier co-efficient given by Appendix 3.1	116
B_1, B_n	Susceptances at ω_1, ω_n	53
B_L, B_C	Inductive and capacitive susceptances	208
b	arbitrary constant	209
C_o	Small signal capacitance of diode	24
C_1, C_n	Circuit capacitances in input and output filters	47
C_{1t}, C_{nt}	Total node or mesh capacitances (including diode capacitance) in input and output filters	142
C_{om}	C_o in the mth. stage of a cascaded multiplier	220
C_{o12},etc.	Capacitance of diode which couples nodes (or meshes) resonant at ω_1 and ω_2, etc.	233
C'_{o1},C'_{on}	Diode capacitance at ω_1, ω_n under large signal conditions	55
C''_{o1},C''_{on}	Capacitance formed by C_o in series with X_1,X_n	151
C_s	Stray shunt capacitance	178
C_a, C_b	'Additional filter' capacitances	158
C_i	Isolating capacitance for bias circuit	200
C_B	Decoupling capacitance for bias supply	200
C(v)	Non-linear capacitance, a function of v	24
${}^mC_i$	Binomial co-efficient	60
c', c_i	Taylor co-efficients	27
D_m	Fourier co-efficient given in Appendix 3.1	116
D_t,D_d,D_f	Total, diode, filter loss in dB.	147
D(m)	Part of the factor 'K' in the node circuit	54

Symbol	Definition	Page of first appearance
E_1, E_n	Equal to C_1/C_{1t}, C_n/C_{nt}	151
e	The exponential function	172
f( )	Mathematical function	116
f_1, f_n	Input and output frequencies	51
G_1, G_n	Conductances at the input and output nodes due to losses (of filters)	30
G_o	Load conductance at ω_n	29
G_{nt}	Total conductance at ω_n	29
G_{1t}	Total conductance at ω_1	
G_{in}	Input conductance of a node circuit	30
G_{eq}	Equivalent conductance appearing at ω_1 as a result of power dissipated at ω_n	30
G_g	Generator conductance	159
G_d^g	Equivalent shunt conductance of diode	79
G_{dn}	Equivalent shunt conductance of diode at ω_n	65
G'_{eq}, G'_{nt}	Values of G_{eq}, G_{nt} modified by the presence of filter reactances at alternate nodes	152
G_{in2}	Input conductance to second stage	218
G_{L2}	Loss conductance of second stage	218
G_{o1}	Load conductance of first stage	218
h	Value of harmonic	159
I	Peak value of current	
I_g	Generator current	28
I_n	Current generated at ω_n due to non-linearity	53
I_{dn}	Equal to I_n/V_b	53
I_1	Input current of a mesh circuit	38
I_1', I_n'	Mesh currents at ω_1, ω_n modified by reactances of filters in alternate meshes	153

Symbol	Definition	Page of first appearance
I_{1h}, I_{nh}	Current at $h\omega_1$ flowing in G_g, G_o respectively	159
I_{1a}, I_{na}	Current at ω_1, ω_n that would flow in charge storage circuit if diode was always conducting	115
I_B	Equal to V_B/R_d in charge storage circuit	115
I_{ms}, I_{mc}	Sine and cosine components of current at $m\omega_1$ obtained by Fourier analysis	115
i	Current, a function of time	52
$i(\omega_1)$etc.	Current at ω_1, etc.	28
i_1, i_n	Current, a function of time, at ω_1, ω_n	54
i_{dn}	Normalized current equal to i_n/V_b	53
j	$\sqrt{-1}$	28
K	Factor relating input and output quantities in a node or a mesh multiplier	29
K_h	Factor relating current at $h\omega_1$ to the input voltage of a node multiplier $^{-1}$(see (4.79))	160
K_m'	Factor relating diode capacitance to bias volts	220
L_1, L_n	Inductances of filters resonant at ω_1, ω_n	47
L_a, L_b	Inductance of 'additional filters'	79
L_i	Taylor co-efficients for mesh circuit case	56
L_d, L_f, L_t	Terms representing diode, filter and total loss respectively	147
M_d, M_f	Factors occuring in expression for L_d, L_f	147
m	A harmonic number (general)	54
N_d, N_f	Factors occuring in expression for L_d, L_f	147
n	The required output harmonic	52
P	Power	173
P_a	Power available from a generator	214
P_{in}	Power input to a circuit	31

Symbol	Definition	Page of first appearance
P_{out}	Power output from a circuit	31
P_{1d}	Power input to the diode (as distinct from power input to the circuit)	31
P_{nt}	Total power dissipated at the output frequency	30
P_{in1}, P_{o1}	Input and output powers for the first stage of a cascaded multiplier	223
p	Factor determining the power dissipated under forward conduction conditions	173
Q	Circuit or diode 'Q' factors	
Q_1, Q_n	'Q' factors of filters at ω_1, ω_n respectively	142
Q_d	Diode 'Q' factor	
Q_{dn}	Diode 'Q' factor at the output frequency	66
Q_o	Part of the charge on the diode under mesh circuit operation	56
Q_e	'Q' factor of diode modified by forward conduction losses	173
Q_{1c}, Q_{nc}	Equivalent 'Q' factor of losses coupled into the filters at ω_1 and ω_n respectively due to non-ideal filters	155
Q_{1t}, Q_{nt}	Total 'Q' factors at the input and output frequencies, including generator and load resistances respectively	143
q	Charge, a function of time	56
q_d	Normalized charge defined by q/Q_o	56
R	Value of the last term in a series	61
R_1, R_n	Loss resistances in the input and output meshes respectively	41
R_{1t}, R_{nt}	Total resistances in the input and output meshes respectively(including generator and load resistances)	41
R_n	Load resistance in a charge storage circuit	116

Symbol	Definition	Page of first appearance
R_{eq}	Equivalent resistance at the input frequency due to power being dissipated at the output frequency	40
R_s	Series resistance of diode	65
R_o	Output (load) resistance in a mesh circuit	40
R_d	Series circuit resistance in a charge storage type multiplier	115
R_g	Generator resistance	118
R_b	Bias resistance	200
R_{in}	Input resistance to a mesh circuit	41
r	Ratio of successive terms in a series	109
r	Ratio of I_{na}/I_{1a} in a charge storage circuit	117
S_R	Sum to infinity of the remainder of a series	61
T_1, T_n	The relation between V_1 and V_1'(node circuit) and I_1 and I_1'(mesh circuit) due to non-ideal filters	151
t	Time	26
t_1	Time when diode starts to conduct in a charge storage circuit	116
t_2	Time when current becomes the same value as at t_1 in a charge storage circuit	128
t_3	Time at which diode becomes open circuit in a charge storage circuit	116
V	Voltage (peak value)	
V_1, V_n	Voltages at the input and the output frequencies in a node circuit	26
V_1', V_n'	Voltages at the input and output frequencies modified by the filter reactances	151
V_n	Voltage of the equivalent series generator at the output frequency of a mesh circuit	58

Symbol	Definition	Page of first appearance
V_B	Battery voltage	23
V_b	Effective bias voltage = $V_B + \gamma_o$	38
V_b'	Maximum useable part of diode characteristic before conduction effects dominate	68
V_b''	Equal to $V_B + \gamma_c$, (see (4.98)	173
V_{eq}	The volyage across R_{eq}	41
V_{1d}, V_{2d}	Approximate voltages across the diode at ω_1, ω_2 in a mesh circuit	43
V_{d1}, V_{dn}	Normalised voltages across the diode at ω_1, ω_n in a node circuit	52
V_{11}, V_{12}	Input voltages of first and second stages of a cascaded multiplier(node type)	218
V_{n1}, V_{n2}	Output voltages of first and second stages of a cascaded multiplier (node type)	218
V_{XY}	Voltage between points X and Y (Fig.3.2,(a)) in a charge storage circuit	114
V_{bm}	Bias voltage on the mth. stage of a cascaded multiplier	220
v	Voltage, a function of time	24
$v(\omega_m)$	Voltage at ω_m	39
v_d	Normalised voltage = v/V_b	52
v_1, v_n	Voltages at ω_1, ω_n	53
v_{d1}, v_{dn}	Normalised voltages at ω_1, ω_n	57
X	Reactance.	
X_1, X_n	Reactance of input and output filters	151
X_o	Reactance of diode capacitance, C_o	151

Symbol	Definition	Page of first appearance
x	Equal to V_1/V_b, node circuit and equal to $(I_1/\omega_1 Q_o)$, mesh circuit	59
Y	Admittance	
Y_1	Admittance of filter at ω_1 (magnitude)	28
Y_n	Admittance of filter and load at ω_n (magnitude)	28
y_1	Complex form of admittance = $Y_1 \underline{/\theta_1}$	28
y_n	Complex form of admittance = $Y_n \underline{/\theta_n}$	28
Z	Impedance	
Z_n	Impedance of filter and load at ω_n	57
z_n	Complex form of impedance = $Z_n \underline{/\theta_n}$	57

Symbol	Definition	Page of first appearance
α_m	Ratio of total resonating capacitance to diode capacitance in a node circuit	142
α_m	Ratio of diode capacitance to total resonating capacitance in a mesh circuit	143
α_m'	As above but including only the filter capacitance, not the total capacitance	197
β	Ratio of output to input voltages in a node circuit	214
γ	Exponent in the depletion layer capacitance law (see (1.1))	23
γ'	Equal to $1/(1-\gamma)$	56
δ	Factor in the large signal analysis for the mesh circuit	57
δ''	The amount by which V_1/V_b'' can exceed unity before the diode 'Q' factor is seriously degraded	175
${}^m\Delta_i^n$	Equal to ${}^mA_i - {}^mA_n$	54
ϕ_1, ϕ_n	Phase angles	27
ψ_o	Barrier voltage of a p-n junction	23
ψ_c	Forward voltage at which conduction effects are assumed to suddenly occur	173
Ψ_1, Ψ_n	Phase angles between voltages in a mesh circuit	63
θ_1, θ_n	Impedance (or admittance) phase angles	28
ω_1	Equal to $2\pi f_1$	26
ω_n	Equal to $n\omega_1$	52
η	Efficiency	65
$1/\eta$	Referred to as power loss	66
	$10 \log(1/\eta)$ = power loss in dB	148

INTRODUCTION.

Definition.

Frequency multiplication may be defined as the conversion of power from a fundamental or input frequency to a higher unique harmonic frequency. This definition will be assumed in the following work. It should be noted that this does not include the generation of a band of harmonic frequencies which comes under the heading of harmonic generation. Distinction should also be made between these two mechanisms and 'mixer action' in which power may be generated at a higher or lower frequency not integrally related to the input frequency.

Historical survey - Methods and applications.

Since the early days of electronic circuits, frequency multipliers have been used in various applications. For example, in radio transmitters a small amount of power is often developed at a relatively low frequency, then multiplied in several stages before being amplified at the final output frequency. This has the advantage of facilitating frequency stability, firstly because it is often easier to construct stable oscillators at low frequencies and secondly because high power at the output frequency cannot, through poor shielding, be coupled to the oscillator thus giving rise to instability. Also in mixer circuits it is often desirable to originate the local oscillator power at a convenient low frequency and then multiply to the frequency required for mixing.

This multiplication has in the past been carried out with valves operating in class 'C'[34]. In a similar manner, transistors may be used in frequency multiplying circuits. Both these methods have the disadvantage of a low overall

efficiency, necessitated by the presence of d.c. power supplies. The upper frequency at which useful power may be developed is also limited in the above devices.

Reasons leading to present work.

With the introduction of transistors, junction diodes also became considered as useful circuit elements. At the time the present work was started, the field of frequency conversion[21,24,29] and parametric amplification [1,5,14] was beginning to arouse interest due to the usefulness of the latter device as a low noise amplifier at high frequencies. Parametric amplification depends on the presence of a non-linear reactance as a coupling element between circuits resonant at two different frequencies, the pump and the signal frequencies. A very suitable non-linear reactance was available in the depletion layer capacitance of a reverse biased p-n junction diode [5,36] although amplifiers and converters were also studied using ferrites as the non-linear element [21,34,38].

A difficulty encountered in high frequency parametric amplifiers is the fact that the pump (i.e. the input power) frequency must be greater than the signal frequency[5]. A method of overcoming this difficulty was suggested by Bloom and Chang[6], in which power is supplied at one half the theoretical pump frequency and the non-linearity of the coupling element used to generate second harmonic power at the necessary frequency. Whilst making preliminary investigations of these topics the author decided that perhaps a more efficient method of overcoming the difficulty of generating high frequency pump power would be to use a separate diode with suitable circuitry to generate the required harmonic. The present work is the outcome of this idea but as has already been pointed out, the usefulness

of the circuit is not limited to the field of parametric amplification, ~~but~~ for it may be applied ~~to~~ in any of the uses of frequency multipliers previously covered by ~~the use of~~ valve or transistor circuits.

Work already carried out in the field.

The theoretical basis for the use of non-linear reactances in frequency multiplying circuits was first put forward in 1956 by Manley and Rowe[24] when they discussed, as a special case of their 'power relations in non-linear elements', the use of a non-linear reactance as a device capable of 100% efficiency when used as a frequency multiplier. This fact is intuitively obvious, since if no losses are present in the non-linear element, no power will be dissipated and hence the power input to the device will equal the total power output. It is only necessary to use adequate lossless filters in order to realise 100% efficiency. It is of course obvious that the Manley Rowe relations are only applicable in the ideal, and non-practical, case of lossless non-linear elements and lossless filters. The behaviour of practical circuits with lossy diodes and/or lossy circuit elements cannot be predicted without recourse to a circuit analysis. This was first attempted by Chang[9] whose paper appeared at the commencement of the work described in this thesis. Prior to this, Higa[16] had suggested using ferro electric devices for frequency multiplication and several people had in fact constructed various multipliers[20,36] without attempting to relate the efficiencies they obtained with any theory.

Purpose of project.

The aim of the research is to obtain a complete understanding of the theory of frequency multiplication using

the non-linear capacitance effect of p-n junction diodes, hence to evolve a tractable theoretical approach to the solution of the problems leading to a basis for the design and evaluation of performance of various circuits. This enables a comparative study of different circuits to be made. As an extension of the depletion layer behaviour, a study is also made of operation of the diode as a charge storage device.

Outline of project.

The work divides into the following basic headings:

Section 1, Basic concepts and circuits,
Section 2, Large signal depletion layer analysis,
Section 3, Consideration of charge storage effects,
Section 4, Sources of decreased efficiency when using practical circuits,
Section 5, General details of depletion layer circuits including cascading,
Section 6, S ome general experimental results.

All the work described is believed to be original except where specifically stated to be otherwise. However, since the research was started, a number of papers have been published in the field which overlapped the author's work. In order to clarify the points which the author considers to be original, a discussion of these points follows.

DISCUSSION OF ORIGINAL WORK.

At the time this work on frequency multiplication was started, the only relevant theoretical papers to have been published were by Manley and Rowe[24] in June, 1956, and by Chang[9] in September, 1958. Chang's paper which is essentially an extension of that on parametric amplifiers[5] gives an approximate theoretical solution for a doubler and a tripler for a specific circuit. After most of the basic work on the two circuit configurations discussed in sect.1 had been completed, Leeson and Weinreb[23] published a paper which overlapped the author's work and lead to the same basic small signal circuit equations for a doubler as had already been obtained by the author (refer to sect.1). This paper does not however consider in any detail the effect of circuit and diode losses, nor the problem of optimizing a specific circuit for minimum power loss.

In September, 1960, after some large signal theory for low order multipliers had been evolved, Johnson[19] published a paper which considers large signal behaviour. This paper does not, however, give any general results which may be readily used to indicate the efficiencies obtained under specific conditions nor does it discuss the choice of circuits. The method described for tackling the large signal problem is different from the author's method.

Although some thought had been given to operation of the diode in the forward region, it was not until after the publication in October, 1959, of a paper by Leenov and Uhlir[22] that serious consideration was given to multiplication using the charge storage effect. The work described in sect.3 uses this paper as a starting point and is essentially concerned with predicting the efficiencies obtainable when filters are introduced into the circuit and hence with determining the behaviour of a depletion layer circuit when driven into the forward conduction region.

Apart from the points mentioned, all the work may be taken to be original to the best of the author's knowledge unless explicitly stated otherwise. A summary of the most important points of the work is given below:-

Complete approach to the large signal solution of the diode behaviour in the depletion layer mode of operation for the two basic circuit configurations.

Extension of the work of Leenov and Uhlir[22] on the charge storage mode of operation to cover the case of circuits with filters, thus increasing the efficiency, and hence to predict the behaviour of a depletion layer circuit when driven into the forward conduction region.

Circuit analysis and discussion of the two basic circuits, leading to expressions for power loss due to both lossy diodes and lossy filters.

Design data and curves of power loss for various cases.

Cascading considerations including discussion of matching conditions between adjacent stages.

Comparative study of various circuits and combinations to obtain a given order of multiplication.

General topics including a qualitative study of hysteresis effects and behaviour of a circuit when it is de-tuned.

SECTION 1

BASIC CONCEPTS AND CIRCUITS.

1.1 Introduction.

The present section is intended to give a general outline of the theory and operation of the frequency multiplying circuits under investigation. The essential properties of the non-linear element, the p-njunction,are discussed and methods of utilising the diode in practical circuits are given. Two basic circuits for a X2 multiplier are analysed on the basis of a small signal approximation. The results of the theory indicate the requirements for high efficiency operation. Some experimental results are included, and from these conclusions are drawn as to the limitations of the small signal theory and extensions necessary to the theory in order to predict accurately the behaviour of any multiplier.

1.2 Diode characteristics.

A p-n junction diode operating with a small amount of reverse bias may be represented essentially by its depletion layer capacitance which is a function of the applied bias. This capacitance obeys the well known law:

$$C = k(V_B + \psi_o)^{-\gamma} \qquad (1.1)$$

where V_B is the applied reverse bias voltage, ψ_o is the barrier voltage and k is a constant which depends upon the geometry of the diode. The value of γ depends on the doping of the diode: for an abrupt junction, $\gamma = 1/2$ and

for a linearly graded junction, $\gamma = 1/3$. It is important to note that the above capacitance is the small signal 'a.c. capacitance'; i.e. it is the capacitance which would appear if the diode, together with its bias, were connected across an impedance through which a small a.c. current was flowing. If the alternating voltage across the diode is not negligibly small we have the following relationship:

$$C(v) = k(V_B + v + \psi_o)^{-\gamma} \qquad (1.2)$$

where v is the alternating voltage across the diode. This may be expressed in the form:

$$C(v) = C_o\left[1 + v/(V_B + \psi_o)\right]^{-\gamma} \qquad (1.3)$$

where C_o is the small signal capacitance given by (1.1).

The other important property of the diode which must be considered is the loss introduced by the finite resistance of the material. This becomes particularly significant at high frequencies, i.e. when the reactance of the capacitance C_o, becomes comparable to the series loss resistance. This resistance is, to a good approximation, constant and the equivalent circuit of the diode under a given bias may be represented as a non-linear capacitance, C(v), whose small signal capacitance is C_o, in series with a loss resistance R_s. In fact both C_o and R_s are frequency dependent to a slight extent but since the frequency 'gain' of the multipliers to be considered is small, this variation may be safely neglected. At very low frequencies the shunt or leakage resistance may also be significant but since the main application of the circuits is at high frequencies, this may generally be neglected.

For the present discussion it will be assumed that the diode is operating solely in the depletion layer region. The effect of driving the diode into the forward conduction

region will be discussed later.

Obviously, two main requirements in choosing a diode for frequency multipliers are:

(a) A suitable non-linearity

(b) A low value of series loss resistance.

The precise effect of these properties is not, however, obvious and in the following work a detailed study is made of the behaviour of the diode as a circuit element in frequency multipliers.

1.3 Basic circuits.

Given a non-linear element, the first problem is to choose a circuit in which it may be incorporated to generate harmonics and in which a particular harmonic may be filtered so that power may be extracted at a given frequency. Two basic possibilities exist for utilising the non-linear properties of the diode. The diode may be connected either in series or in shunt with the generator and load. (Henceforth it will be assumed that a suitable bias supply is included: a discussion of biasing arrangements will be found in sect.5.2). The two alternatives are shown in Fig. 1.1 for a circuit without filters. We are, however, interested in generating a particular harmonic and for this reason it is obviously necessary to employ filters to prevent power from being dissipated at unwanted frequencies. Thus we have the two possibilities as shown in Fig.1.2. in which the generator with its associated resistance is fed through a filter to the diode which in turn feeds power to a filtered load at the required harmonic frequency: loss conductances G_1, G_2 or resistances R_1, R_2, are shown; their exact nature will be discussed later.

These are the two basic circuits to be considered in the following work. In order to gain an understanding of the essential properties of the circuits, a study will first of all be made of their behaviour as X2 multipliers, using only a first order approximation to the non-linear characteristic of the diode. In subsequent sections a more detailed analysis of the behaviour will be given, valid for all orders of multiplication and including high order non-linear effects. Henceforth the circuit shown in Fig.1.2,(a) will be referred to as a node circuit since it consists essentially of two nodal points coupled together by the non-linear capacitance; likewise the circuit of Fig.1.2,(b) will be referred to as a mesh circuit since the diode forms the non-linear coupling element between two meshes. Note that these two circuits are <u>not</u> duals; if this were to be the case the coupling element in the second circuit would have to be a non-linear inductance with suitable characteristics. For this reason a separate analysis is required for each circuit.

1.4 <u>X2 node circuit</u>.

1.4.1. <u>Analysis</u>.

Consider the circuit shown in Fig.1.2,(a). It is assumed that the losses at the input and output frequencies may be represented by the conductances G_1 and G_2 respectively Thus each conductance represents a combination of diode and circuit losses. The filters are assumed to be perfect short circuits at frequencies other than their resonant frequencies.

Let a generated voltage v_1 exist at the input node where;

$$v_1 = V_1 \sin \omega_1 t \qquad (1.4)$$

This voltage will cause a current to flow through the diode and due to the non-linearity, a second harmonic current, i_2, will produce a voltage, v_2, at the output node. Thus the voltage across the diode, v, is given by:

$$v = V_1 \sin \omega_1 t + V_2 \sin \overline{\omega_2 t + \phi_2} \qquad (1.5)$$

where $\omega_2 = 2\omega_1$

The current through the diode, i, is then given by:

$$i = C(v) \frac{dv}{dt} \qquad (1.6)$$

where C(v) is defined by (1.3). This follows since C(v) is the incremental capacitance, i.e.

$$C(v) = \frac{dq}{dv} \qquad (1.7)$$

The expression for C(v) as given by (1.3) is not suitable for evaluating (1.6) directly. A first order approximation to the non-linear law may be made, however, by letting

$$C(v) = C_o + c'v \qquad (1.8)$$

The complete expansion of C(v) will of course be an infinite series but the capacitance with the first order non-linearity given by (1.8) will generate second harmonic current and will thus serve as an indication to the probable behaviour of the circuit. Note that c' is simply the slope of the 'a.c. capacitance' versus voltage characteristic at the operating point determined by the bias. It is thus the first term of the Taylor expansion of C(v) about the operating point; i.e.

$$c' = -\gamma C_o/(V_B + \psi_o) \qquad (1.9)$$

Combining (1.6) and (1.8) and substituting for v from (1.5) leads to the result:

$$i = i(\omega_1) + i(\omega_2) + i(\omega_3) + i(\omega_4) \qquad (1.10)$$

where:

$$i(\omega_1) = \omega_1 C_o V_1 \cos\omega_1 t - (1/2)c'\omega_1 V_1 V_2 \sin\overline{\omega_1 t + \phi_2} \qquad (1.11)$$

$$i(\omega_2) = \omega_2 C_o V_2 \cos\overline{\omega_2 t + \phi_2} + (1/2)c'\omega_1 V_1^2 \sin 2\omega_1 t \qquad (1.12)$$

We are not interested in currents at other frequencies since, due to the filters, power can not be dissipated at these frequencies. The equations for current at the input and output frequencies may be written in exponential form thus:

$$i_1 = j\omega_1 C_o V_1 - (1/2)c'\omega_1 V_1 V_2 \exp j\phi_2 \qquad (1.13)$$

$$i_2 = j\omega_2 C_o V_2 \exp j\phi_2 + (1/2)c'\omega_1 V_1^2 \qquad (1.14)$$

The mode equations at the two frequencies may be written thus:

$$i_g = v_1 y_1 + i_1 \qquad (1.15)$$

$$0 = v_2 y_2 + i_2 \qquad (1.16)$$

where
$$\left.\begin{aligned} y_1 &= Y_1 \angle\theta_1 \\ y_2 &= Y_2 \angle\theta_2 \end{aligned}\right\} \qquad (1.17)$$

$$i_g = I_g \exp j(-\phi_1) \qquad (1.18)$$

Substituting in (1.15) and (1.16) for the various quantities gives:

$$I_g \exp j(-\phi_1) = V_1 Y_1 \exp j\theta_1 + j\omega_1 C_o V_1 - (1/2)c'\omega_1 V_1 V_2 \exp j\phi_2 \qquad (1.19)$$

$$0 = V_2 Y_2 \exp j(\phi_2+\theta_2) = j\omega_2 C_o V_2 \exp j\phi_2 + (1/2)c'\omega_1 V_1^2 \quad (1.20)$$

These two equations are essentially the same as those derived by Chang[9].
We may rewrite (1.20) in the following way:

$$V_2 \exp j\phi_2 \left[Y_2 \exp j\theta_2 + j\,\omega_2 C_o + (1/2)c'\omega_1 (V_1^2/V_2) \exp j(-\phi_2) \right] = 0 \quad (1.21)$$

i.e. in general:

$$Y_2 \exp j\theta_2 + j\,\omega_2 C_o + (1/2)c'\,\omega_1 (V_1^2/V_2) \exp j(-\phi_2) = 0 \quad (1.22)$$

which, equating real terms, gives:

$$V_2 G_{2t} + (1/2)c'\omega_1 V_1^2 \cos \phi_2 = 0 \quad (1.23)$$

where: $$G_{2t} = G_2 + G_o \quad (1.24)$$

G_o being the load conductance and G_2 the loss conductance at ω_2. Since c' is negative, it follows that for the output voltage and hence the output power to be maximum,

$$\phi_2 = 0 \quad (1.25)$$

whence (1.23) may be rewritten:

$$V_2 G_{2t} = K \omega_1 C_o V_1 \quad (1.26)$$

where

$$K = (1/2)\,\gamma\, V_1/(V_B + \psi_o) \quad (1.27)$$

(This is obtained by substituting from (1.9) for c').
(1.19) may now be evaluated to give:

$$I_g \exp j(-\phi_1) = V_1 Y_1 \exp j\theta_1 + j\omega_1 C_o V_1 - (1/2)c'\omega_1 V_1 V_2 \quad (1.28)$$

If the susceptance at the input node is zero at the input frequency, i.e. if the input is resonated,

$$\phi_1 = 0 \tag{1.29}$$

and

$$I_g = V_1 G_1 - (1/2) c' \omega_1 V_1 V_2 \tag{1.30}$$

$$= V_1 G_1 + (1/2) |c'| \omega_1 V_1 V_2 \tag{1.31}$$

$$= V_1 G_1 + K \omega_1 C_o V_2 \tag{1.32}$$

1.4.2 General behaviour of circuit.

We are now in a position to discuss the general behaviour of the circuit. Firstly let us consider the relation between the input and the output voltages. This is given by (1.23) or (1.26) and it is seen that the output voltage varies as the square of the voltage at the input node. We also see from the same equations that the power P_{2t}, in the conductance G_{2t}, at the output node is:

$$P_{2t} = (1/2) c' \omega_1 V_1^2 V_2 \tag{1.33}$$

$$= K \omega_1 C_o V_1 V_2 \tag{1.34}$$

From (1.30) to (1.32) we see that the input conductance, G_{in}, is made up of two parts thus:

$$G_{in} = G_1 + G_{eq} \tag{1.35}$$

where

$$G_{eq} = (1/2) c' \omega_1 V_2 \tag{1.36}$$

$$= K \omega_1 C_o (V_2/V_1) \tag{1.37}$$

or, using (1.26), G_{eq} may be expressed thus:

$$G_{eq} = K^2 (\omega_1 C_o)^2 / G_{2t} \tag{1.38}$$

The equivalent circuit at the input frequency may now be represented as shown in Fig.1.3,(a), where, under normal operation, the total susceptance will be zero (this condition is given by (1.28) and (1.29)). Note that the input power to the diode, P_{1d}, obtained from (1.32) is:

$$\left.\begin{aligned} P_{1d} &= V_1 I_g - V_1^2 G_1 \\ &= K \omega_1 C_o V_1 V_2 \end{aligned}\right\} \qquad (1.39)$$

which, as must logically be the case, is the same as (1.34) since no power exists at frequencies other than the fundamental and second harmonic.

Let us now consider the efficiency of the multiplier. Defining the efficiency, η , by:

$$\frac{1}{\eta} = \frac{\text{Power available from generator}}{\text{Power output}} \qquad (1.40)$$

we may write:

$$\frac{1}{\eta} = \frac{P_{in}}{P_{out}} \qquad (1.41)$$

where P_{in} is the power input to the circuit under matched input conditions: i.e.

$$P_{in} = I_g^2/(8G_g) \qquad (1.42)$$

This condition is met when:

$$G_g = G_1 + G_{eq} \qquad (1.43)$$

Writing (1.41) in terms of the circuit parameters gives:

$$\frac{1}{\eta} = \frac{V_1^2 (G_1 + G_{eq})}{V_2^2 G_o} \qquad (1.44)$$

where G_o is the load conductance as in (1.24). Using the fact that the input power to the diode, P_{1d}, is equal to

the total power at the output frequency, the result obtained by comparing (1.34) and (1.39), we may write:

$$V_1^2 G_{eq} = V_2^2 G_{2t} \qquad (1.45)$$

Substituting this in (1.44) gives:

$$\frac{1}{\eta} = \left[\frac{G_2 + G_o}{G_o} \right] \left[\frac{G_1 + G_{eq}}{G_{eq}} \right] \qquad (1.46)$$

This expression shows simply the attenuation at the input and output nodes due to the loss conductances and is obvious. If we substitute for G_{eq} we obtain the more interesting expression:

$$\frac{1}{\eta} = \frac{G_{2t}}{G_o} \left[1 + \frac{G_1 G_{2t}}{K^2 (\omega_1 C_o)^2} \right] \qquad (1.47)$$

This shows clearly the dependence of η on the factor K, defined by (1.27).

1.4.3 Requirements for high efficiency circuits.

As a result of the above analysis we are now in a position to summarise the requirements necessary for high efficiency operation of a X2 node multiplier. Referring to (1.47) these are as follows:

(a) G_o should approach G_{2t} in value. This simply implies that the loss conductance in (1.24) should be as small as possible; alternatively, for a given loss conductance, the load conductance G_o and hence the total conductance G_{2t}, should be large.

(b) The product $G_1 G_{2t}$ should be small. Obviously G_1 must be made as small as possible; however we now have

two conflicting conditions when the loss conductance G_1 and G_2 are fixed since (a) implies a large value of G_{2t} whilst the present requirement is for a small value of G_{2t}.

(c) $\omega_1 C_o$ should be large. This means that the diode ~~capacitance~~ susceptance at the operating point must be comparable in magnitude to the node conductance G_{in} and G_{2t} which, for given circuit 'Q' factors, are related to the circuit resonating capacitances.

(d) The factor K must be large as possible.

Of the above conditions, (d) is the only condition relating directly to the diode. The other conditions affect the circuit parameters but for a given circuit and a diode with a given capacitance at the operating point, it is apparent that the efficiency is a variable quantity being a function of K. Referring to (1.27) it is seen that this implies in addition to the diode having a large input voltage, a diode with a large value of γ. Since in general the choice of values for γ is strictly limited the main point of interest in the factor K is the maximum value of V_1. It is obvious that V_1 cannot exceed $(V_B + \psi_o)$; in fact the limiting condition is given by

$$v_{min} = -(V_B + \psi_o) \qquad (1.48)$$

where v is defined by (1.5). Due to forward conduction effects this limit may not in fact be reached. It is important to remember in discussing the value of K that the approximation involved in (1.8) will cause the practical operation to differ from that predicted from the above theory. This is illustrated by the experimental results.

1.4.4 Experimental results.

The purpose of the experiment was to see how closely the above approximate theory holds in a practical circuit. The circuit used was essentially that of Fig.1.2,(a) with the current generator replaced by a voltage generator of low internal resistance connected to the input node via a resistance of known value. The voltages at the nodes were measured on a wave analyser with a high impedance probe, calibrated at both the input and output frequencies. The input frequency was 2.6 Mc/s and the diode used was a Pacific Semiconductor type V20. The capacitance characteristic was plotted by measuring the capacitance for various values of applied bias under conditions of small input voltage across the diode. This gave a capacitance of 24 pF at the operating bias of -4 volts and a slope at the operating point of -2.24 pF/volt. The value of ψ_o was estimated by plotting the inverse square of the capacitance versus the bias voltage, including small values of forward bias, and measuring the intercept on the voltage axis corresponding to the point of infinite capacitance. This gave a value of $\psi_o = 0.6$ volts. Substituting the above values in (1.9) gives $\gamma = 0.43$. Since the simple filters used were not ideal ~~filters~~, the measured nodal voltages were corrected to obtain the actual diode voltages, by taking into account the voltage drop between the alternate node and the common earth point. At the frequency used it was found that the diode loss was small compared to the inductor loss; the values of G_1 and G_2 were therefore determined by the inductor 'Q' factors.

It was decided that, since the input and output voltages were readily measurable quantities, the validity of the theory could be checked by plotting the voltage gain, V_2/V_1, versus the normalized input voltage, $V_1/(V_B + \psi_o)$. The theoretical relationship between these quantities is given by (1.26) and (1.27) which gives:

$$V_2/V_1 = (1/2)\,\gamma\,(\omega_1 C_o/G_{2t})V_1/(V_B + \psi_o) \qquad (1.49)$$

The value of G_{2t} was determined by measuring the loss of L_2 on a bridge. The value of G_{2t} was altered by suitable loading.

The results obtained are given in Fig.1.4 for two values of the parameter $\omega_1 C_o/G_{2t}$, together with the results predicted by the preceding theory. It is seen that at low values of input voltage the agreement with theory is reasonably good. Possible sources of error are: measuring and correcting the voltages, estimating ψ_o, C_o and γ, measuring the circuit conductances. The main interest in the results is, however, the deviation from the above theory under conditions of large input. Referring to Fig.1.4,(a) it is seen that before V_1 becomes equal to $(V_B + \psi_o)$, the voltage gaim starts to increase more rapidly than the theory predicts. This increase continues for values of normalised input voltage greater than unity. Note that this seemingly impossible condition may arise due to the fact that current flows through the finite resistance of the bias supply and the effective bias voltage may be more than that of the battery under forward drive conditions. The bias was actually supplied through a potentiometer of value 1K. to the bottom end of the combination L_2G_{2t}, a suitable capacitor forming the necessary r.f. bypass. It was observed that as V_1 was increased, the voltage gain reached a maximum value and then started to decrease. The maximum value of V_2/V_1 corresponds to a maximum value of K (see (1.26) and thus to maximum efficiency (see (1.47)). It was noticed that for large values of V_1, it was sometimes possible to obtain two possible values for V_2 depending on the method of tuning the circuit and altering the input voltage. This is illustrated in Fig.1.4,(b) for which case the voltage gain, for a given value of input voltage, is larger than for the case

plotted in Fig.1.4,(a) (corresponding to a larger value of $\omega_1 C_o/G_{2e}$). This corresponds to a hysteresis effect and manifested itself in practice by a sudden jump in output voltage as either the input voltage or the circuit tuning was varied over a small range. The region over which the effect was observed is indicated in Fig.1.4,(b) by the shaded area.

The above measurements suffice to indicate how the practical operation is related to the small signal theory. However, a further set of measurements were made to verify the behaviour of G_{eq} with respect to the input voltage. As was pointed out above the practical circuit consisted of a voltage generator connected to the input node via a known resistance. The value of G_{eq} was determined for a given value of input voltage by replacing the diode by an equivalent (linear) capacitance and connecting a variable conductance across L_1C_1 and adjusting it until (keeping the generator voltage constant) the voltage at the input node returned to its original value; the value of G_{eq} is then equal to the value of inserted conductance. The values of G_{eq} determined in this way agreed with the theoretical relationship given by (1.38) for small input voltages and departed from the theory in the same manner as V_2/V_1 in the above examples, as one would expect. Note that in estimating G_{eq} it was found necessary to make C_1 comparable to C_o ; otherwise it was found that G_1 'swamped' G_{eq}, corresponding to low efficiency operation. This is due to the fact that since the 'Q' factor of an inductor is approximately constant over a wide range of values of inductance, the shunt conductance varies as the resonating capacitance for a given resonant frequency. The minimum value of C_1 is, however, limited by the fact that L_1C_1 must present a low impedance path at the second harmonic frequency.

1.4.5 Conclusions.

From the above results it is apparent that the behaviour of the circuit under large signal conditions is not accurately explainable on a basis of the small signal theory already presented. Since this large signal region corresponds to optimum efficiency operation it is necessary to extend the theory in order to predict efficiencies using various diodes and circuits. It is also desirable to be able to predict how the circuit behaves when the diode is driven into the region of heavy forward conduction. Apart from the operation directly related to the diode it is obviously necessary to perform a circuit analysis in order to determine the choice of parameters for maximum efficiency and to allow for the fact that the simple filters as used above are not ideal.

1.5 X2 mesh circuit.

1.5.1 Analysis.

Consider the circuit shown in Fig.1.2,(b). It is assumed that the losses at the input and output frequencies may be represented by the resistances R_1 and R_2 respectively. As in the case of the mode circuit these losses may in fact be a combination of diode and circuit losses. It is further assumed, as in the mode circuit, that the filters are ideal and only allow currents at their resonant frequencies to flow.

Let a current i_1 generated by v_g flow in the input mesh where:

$$i_1 = I_1 \sin \overline{\omega_1 t + \phi_1} \qquad (1.50)$$

This current will cause a second harmonic current i_2 to flow through the diode. Thus the total current through the diode, i, is given by:

$$i = I_1 \sin \overline{\omega_1 t + \phi_1} + I_2 \sin \overline{\omega_2 t + \phi_2} \qquad (1.51)$$

The relationship between the current, i, and the voltage across the diode may be found by rewriting (1.6) in such a way that upon integrating we obtain the charge on the diode.

$$\int i dt = \int C(v) dv \qquad (1.52)$$

The definition for C(v) given by (1.3) may be used. Substituting for i and C(v) in (1.52) and integrating gives:

$$-(I_1/\omega_1)\cos\overline{\omega_1 t+\phi_1} - (I_2/\omega_2)\cos\overline{\omega_2 t+\phi_2} + f(C_o, V_b)$$

$$+ f(I_1/\omega_1, I_2/\omega_2) = \frac{V_b C_o}{1-\gamma}(1 + v/V_b)^{1-\gamma} \qquad (1.53)$$

where $V_b = V_B + \psi_o \qquad (1.54)$

The integration constants may be found as follows: when I_1 and I_2 are zero, the voltage, v, must also be zero; hence:

$$f(C_o, V_b) = V_b C_o/(1-\gamma) \qquad (1.55)$$

the second integration constant may be determined by using the fact that since there is no direct current flowing through the diode, the direct voltage across the diode must always be equal to V_b. It is now required to expand the right hand side of (1.53). However it is seen that for the special case of $\gamma = 1/2$, a complete solution is possible without using a series expansion. Squaring each side and

equating 'd.c.' terms (due to terms of the form $\cos^2 \omega t$) gives:

$$f(I_1/\omega_1, I_2/\omega_2) = -2C_o V_b + \sqrt{4C_o^2 V_b^2 - (1/2)\left[(I_1/\omega_1)^2 + (I_2/\omega_2)^2\right]} \qquad (1.56)$$

It is seen that for small values of I_1 and I_2 this factor tends to zero; it will therefore be neglected in the following preliminary analysis. Substituting (1.55) into (1.53) and taking the case of $\gamma = 1/2$ enables us to solve for v. This gives (by squaring both sides):

$$v = v(\omega_1) + v(\omega_2) + v(\omega_3) + v(\omega_4) \qquad (1.57)$$

Since the filters are assumed to present open circuits to all unwanted currents, we need not consider the third and fourth harmonic voltages. The relevant voltages are as follows:

$$v(\omega_1) = \left[-I_1/(\omega_1 C_o)\right]\cos\overline{\omega_1 t + \phi_1} + \left[I_1 I_2/(4C_o^2 \omega_1 \omega_2 V_b)\right]\cos\overline{\omega_1 t + \phi_2 - \phi_1} \qquad (1.58)$$

$$v(\omega_2) = \left[-I_2/(\omega_2 C_o)\right]\cos\overline{\omega_2 t + \phi_2} + \left[(1/8) I_1^2/(\omega_1^2 C_o^2 V_b)\right]\cos^2\overline{\omega_1 t + 2\phi_1} \qquad (1.59)$$

These equations may be compared with the results for the node circuit given by (1.11) and (1.12)

Following a procedure similar to that for the node circuit gives the following results:

$$\left.\begin{aligned} \phi_1 &= 0 \\ \phi_2 &= -\pi/2 \end{aligned}\right\} \text{for optimum conditions,} \qquad (1.60)$$

$$I_2 R_{2t} = (1/8)\left[I_1/(\omega_1 C_o) \right]^2 (1/V_b) \qquad (1.61)$$

$$V_g = I_1 R_1 + I_1 I_2/(4C_o^2 \omega_1 \omega_2 V_b) \qquad (1.62)$$

where

$$R_{2t} = R_2 + R_o \qquad (1.63)$$

The similarity between the two circuits may again be seen by comparing the above equations to those for the node circuit.

1.5.2. General behaviour of circuit.

As would be expected, the mesh circuit behaves in a similar manner to the node circuit. For this reason only a brief summary of the operation will be given here. Firstly let us consider the power relationships. The total power at the output frequency, P_{2t} is obtained from (1.61):

$$P_{2t} = (1/8) I_1^2 I_2/(\omega_1^2 C_o^2 V_b) \qquad (1.64)$$

The total power input to the diode is obtained from the second part of (1.62) and gives:

$$P_{1d} = (1/4) I_1^2 I_2/(\omega_1 \omega_2 C_o^2 V_b) \qquad (1.65)$$

It is at once apparent that these two expressions are the same as must logically be the case (as in the node circuit). Note that we may define a resistance R_{eq} where

$$R_{eq} = I_2/(4C_o^2 \omega_1 \omega_2 V_b) \qquad (1.66)$$

which corresponds to G_{eq} in the node circuit and enables us to write the total input resistance of the circuit at ω_1 as

$$R_{in} = R_1 + R_{eq} \tag{1.67}$$

Note that the voltage, V_{eq} , across R_{eq} is obtained from (1.66) and (1.61), thus:

$$\frac{V_{eq}}{V_b} = \left[\frac{1}{32}\right]\left[\frac{I_1}{\omega_1 C_o V_b}\right]^3\left[\frac{1}{\omega_2 C_o R_{2t}}\right] \tag{1.68}$$

This voltage is of interest since it is (in the case where losses are negligible) the voltage input to the multiplier. Substituting (1.68) into (1.66) gives an alternative expression for R_{eq}, thus:

$$R_{eq} = \left[\frac{1}{2}\right]^{5/3}\left[\frac{V_{eq}}{V_b}\right]^{2/3}\left[\frac{1}{\omega_2 C_o R_{2t}}\right]^{1/3} \tag{1.69}$$

Note that this is the same as the result given by Leeson and Weinreb[23].

The efficiency may be expressed in the form:

$$\frac{1}{\eta} = \frac{R_2 + R_o}{R_o}\quad\frac{R_1 + R_{eq}}{R_{eq}} \tag{1.70}$$

or in the more useful form:

$$\frac{1}{\eta} = \frac{R_{2t}}{R_o}\left[1 + \frac{64 R_1 R_{2t}(\omega_1 C_o)^2}{\{I_1/(\omega_1 C_o V_b)\}^2}\right] \tag{1.71}$$

Note that $I_1/(\omega_1 C_o V_b)$ is approximately the normalized voltage across the diode at the input frequency; the approximation is negligible in the case where R_{eq} is small compared with $1/(\omega_1 C_o)$.

It is apparent from the above analysis that the X2 mesh multiplier behaves in a very similar manner to the X2 node multiplier. There is however one important difference

between the two circuits when considering higher order multiplication. It may be seen by referring to (1.53) that if the terms in ω_2 are replaced by higher harmonic terms the circuit will cease to function, considering as before the case of $\gamma = 1/2$. This implies that if the circuit is tuned to, for example, the third harmonic instead of the second, no output will be obtained. Note that the additional higher frequency terms in (1.57) are due to mixing action and only exist when current flows at the second harmonic frequency. The behaviour when $\gamma \neq 1/2$ will be treated in subsequent sections.

1.5.3 Requirements for high efficiency circuits.

Since the requirements for high efficiency operation have already been mentioned for the node circuit it is not necessary to enumerate them in detail for the present case. Referring to sect.1.4.3 the duals of conditions (a) and (b) obviously apply, with the conductances being replaced by the resistances of the mesh circuit. Referring to (1.71) it is apparent that the factor $\omega_1 C_o$ must now be small, i.e. of a magnitude comparable to R_{in} and R_{2t}. Also from (1.71) we get the obvious condition that I_1 must be as large as possible. Since this is limited by the voltage across the diode we have essentially the same conditions as for the node circuit. Note that to determine the limiting value of I_1, it is necessary to consider the total voltage across the diode, which will be a function of the second harmonic circuit and hence dependent on the load.

1.5.4. Experimental results.

A circuit was set up with the purpose of checking the behaviour of a X2 mesh circuit. The arrangement used was essentially that of Fig.1.2,(b), the voltages across the diode being measured as before on a calibrated wave analyser. The diode used was a Pacific Semiconductor type V56,with a bias of -2 volts,which gave an operating point capacitance of 75 pf. The capacitances in the input and output meshes were approximately 30 pf and 15 pf respectively and the input frequency was 3 Mc/s. The value of γ was estimated by plotting the capacitance versus voltage characteristic on a log/log scale, using an estimated value of $\psi_o = 0.6$ volts; the value for γ thus obtained was 0.45.

The relationship between the voltages at the input and output frequencies across the diode ~~are~~ [16] given approximately by re-arrangeing (1.61). This gives:

$$V_{2d}/V_{1d} = (1/8)(V_{1d}/V_b)/(\omega_2 C_o R_{2t}) \qquad (1.72)$$

where the approximation has been made that the voltage at the input frequency across the diode, V_{1d}, is given by:

$$V_{1d} = I_1/(\omega_1 C_o) \qquad (1.73)$$

and the voltage at the output frequency across the diode, V_{2d}, is given by:

$$V_{2d} = I_2/(\omega_2 C_o) \qquad (1.74)$$

It is of course obvious that the above two equations are approximations to (1.58) and (1.59) but it may be readily checked that in the cases considered, the error involved is small. (From (1.68) it is seen that V_{eq}/V_b is considerably less than unity).

The results obtained are shown in Fig.1.5. The discrepancy between the theoretical and the measured curves under conditions of low input may be due largely to the fact that the value of γ is considerably less than 1/2. Again it should be noted that the diode was biased through a resistance of 20K (connected to the 'top' of the diode in Fig. 1.?.(b)) and for values of V_{ld}/V_b greater than unity, current was flowing, thus increasing the actual bias across the diode. As in the case of the node circuit, hysteresis effects were sometimes observed under conditions where the input voltage was large.

1.5.5 Conclusions.

It may be concluded from the above results that the small signal theory is valid under most conditions but further investigation is required of operation under forward conduction conditions. Note that the theory for the mesh circuit for $\gamma = 1/2$ may be made accurate under large s ignal conditions by including (1.56) in the solution. It would appear that this addition will only have a second order effect on the result. The solution when $\gamma \neq 1/2$ requires a series solution to (1.53) which will also enable the solution for higher order multipliers to be obtained.

1.6 General conclusions.

A theory has been presented for the operation of X2 node and mesh type multipliers. The limitations of this theory have been observed, partly as a result of experimental work. It is apparent that the method for solving the node circuit may be equally well applied to higher order multi-

pliers, simply by determining the appropriate co-efficient (refer to (1.8)) to generate the required harmonic current. It would be expected that any error involved in the small signal approximation may become more significant in the case of higher order multipliers. This was in fact observed to be so, since a X10 node multiplier was constructed and gave an output several times that predicted by the small signal approach (using the 9th. Taylor co-efficient), before the diode was driven into the region where current started to flow.

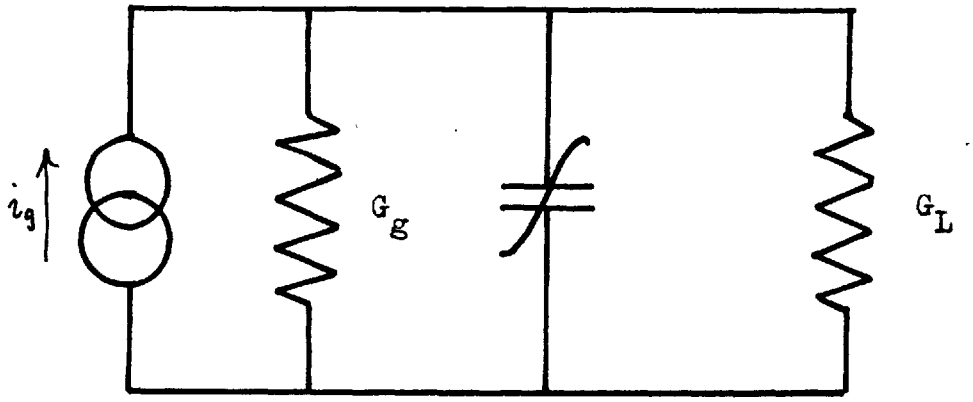
On the basis of the above theoretical and practical results it is apparent that three main points require to be studied in order to predict the behaviour of any multiplier and to design a multiplier with maximum efficiency.

(a) It is necessary to evolve a 'large signal' analysis with which the exact behaviour of a node or mesh circuit may be predicted in the depletion layer region.

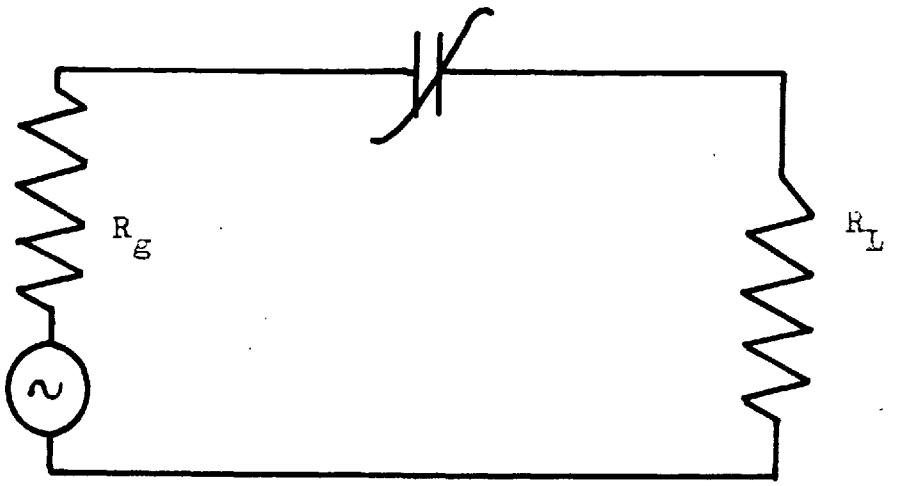
(b) It is necessary to know what happens when the diode is driven into the conduction region.

(c) A circuit analysis is required so that the circuit parameters for maximum efficiency conditions may be determined.

These requirements form the basis of the following sections.

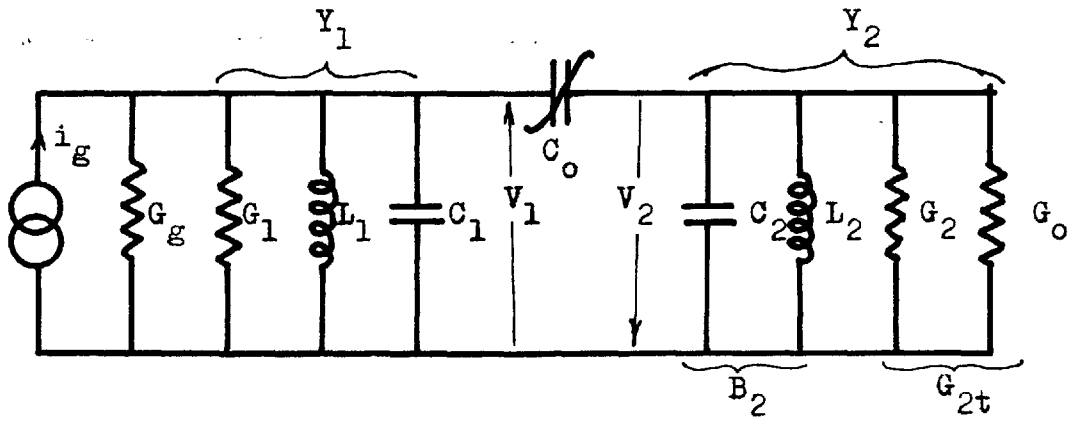


(a) Diode shunting generator and load

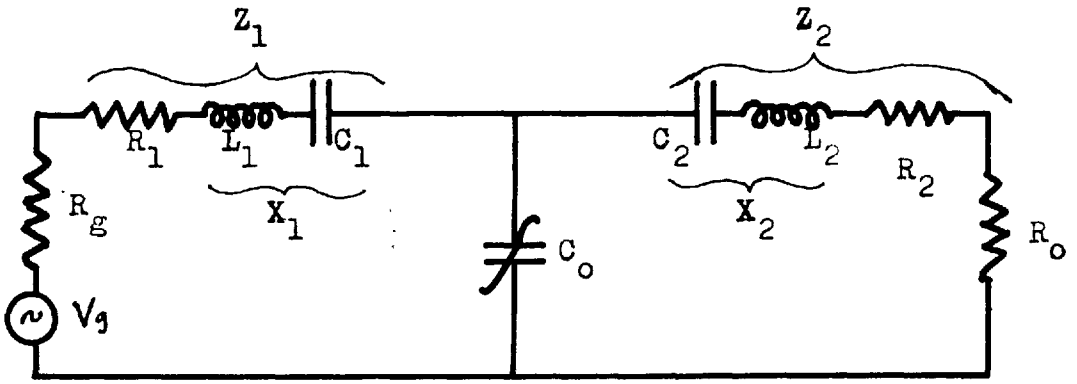


(b) Diode in series with generator and load

Fig.1.1 Basic methods of utilizing diode as a harmonic generator.

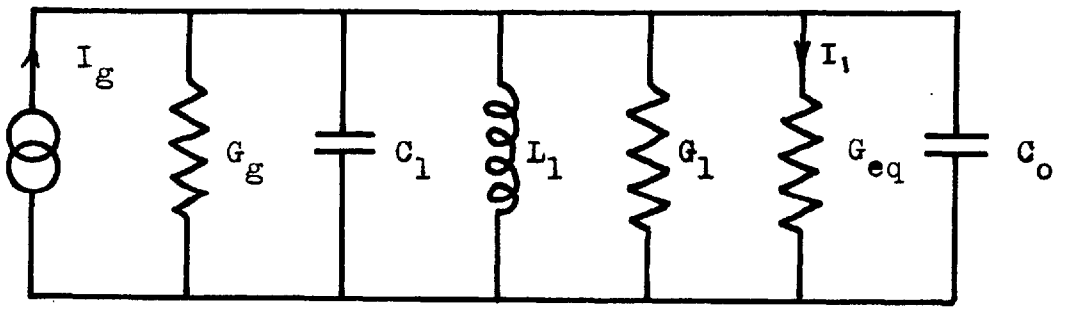


(a) X2 node circuit

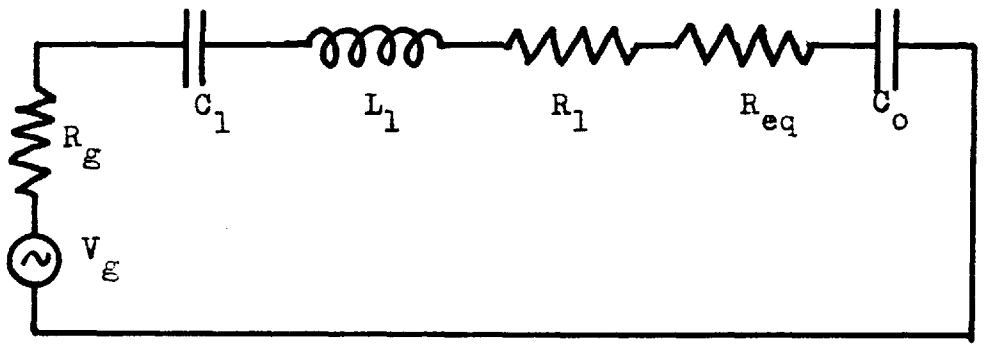


(b) X2 mesh circuit

Fig.1.2 Basic frequency multiplying circuits.

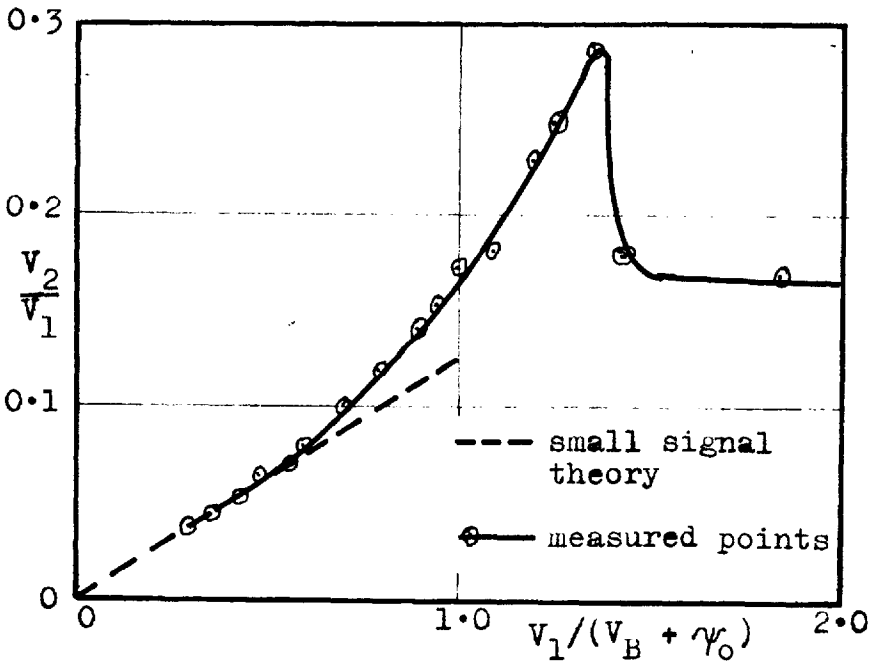


(a)Node input equivalent circuit

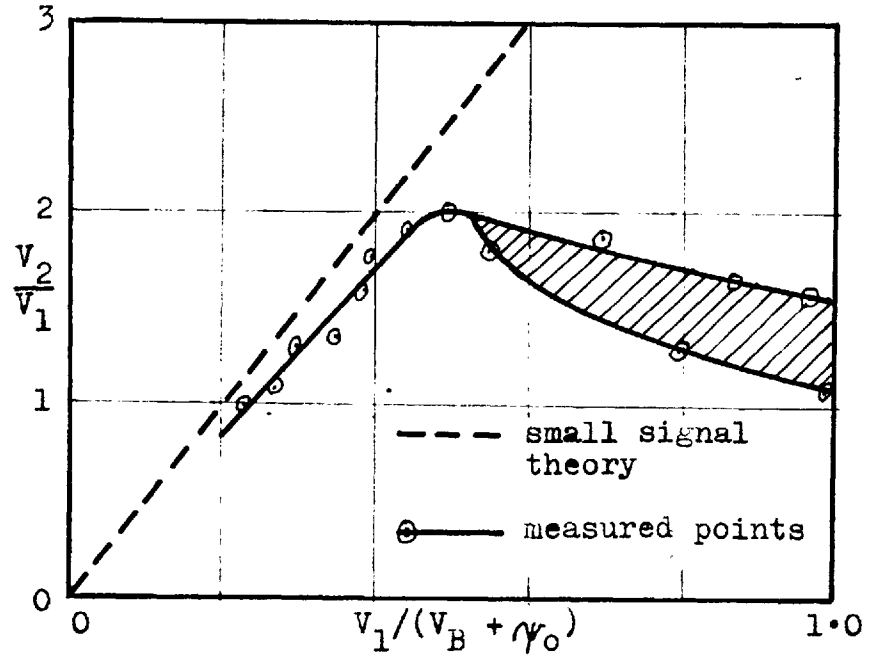


(b) Mesh input equivalent circuit

Fig.1.3 Equivalent circuits at the input frequency.

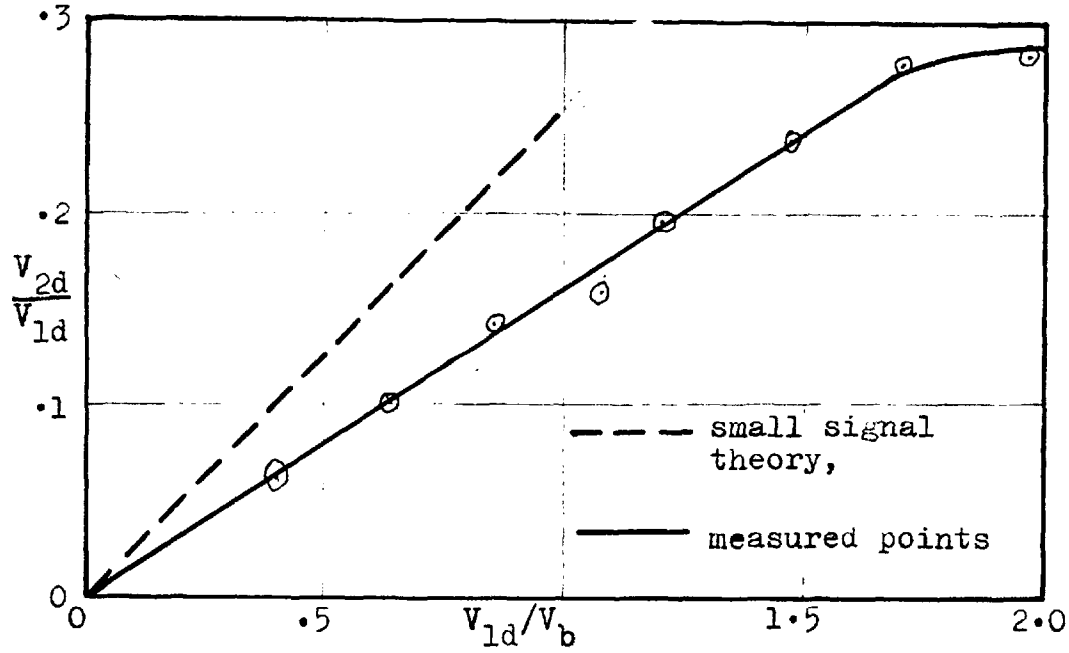


(a) $\omega_1 C_o/G_{2t} = 0{\cdot}58$

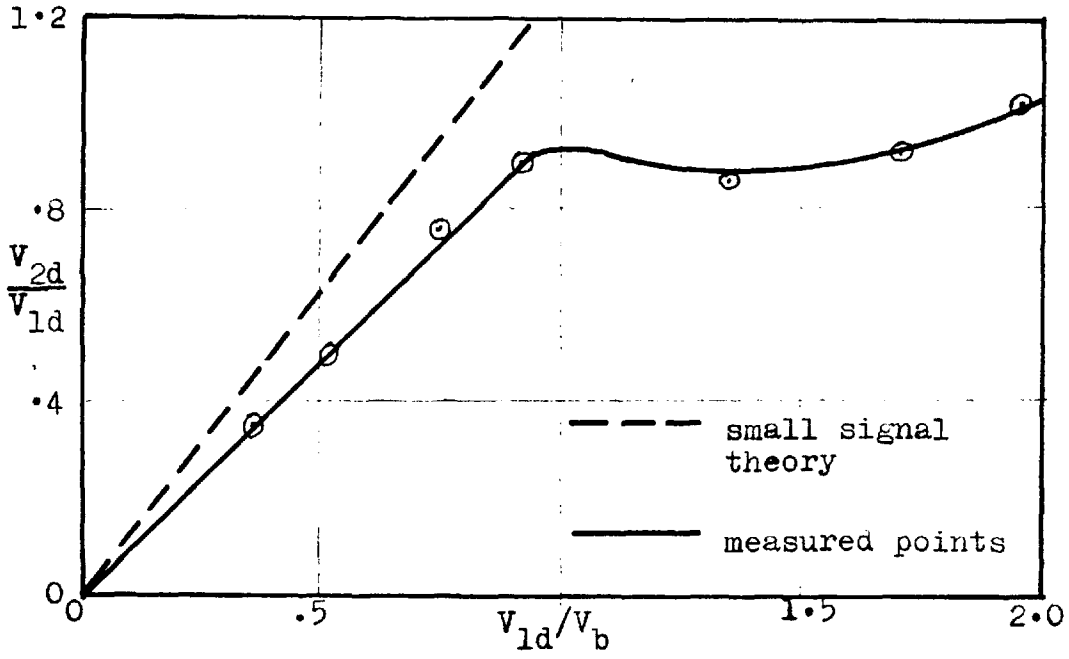


(b) $\omega_1 C_o/G_{2t} = 23{\cdot}0$

Fig.1.4 X2 node multiplier, voltage gain versus normalized input voltage.



(a) $(\omega_2 C_o R_{2t})^{-1} = 2{\cdot}1$



(b) $(\omega_2 C_o R_{2t})^{-1} = 10{\cdot}0$

Fig.1.5 X2 mesh multiplier, voltage gain versus normalized input voltage.

SECTION 2

LARGE SIGNAL DEPLETION LAYER ANALYSIS.

2.1 Introduction.

In the preceding section multipliers have been considered on the basis of a first order approximation to the non-linear depletion layer characteristics. The limitations of this method have been pointed out and it is the purpose of this section to derive a general and accurate large signal analysis. This is used to predict the optimum power loss for X2, X3 and X10 multipliers for various diodes, using the two basic circuits previously mentioned. This enables some useful conclusions to be drawn regarding the usefulness of various arrangements to obtain a given order of multiplication.

2.2 Basic analysis.

2.2.1 Node circuit.

For the purpose of the analysis the circuit shown in Fig.2.1 will be used. It is assumed that only a voltage V_1 at frequency f_1 exists across Y_1 and only a voltage V_n at the output frequency f_n exists across Y_n. This assumption implies that a short circuit path exists for currents at all other frequencies. It is further assumed that the series loss resistance of the diode may be considered as lumped as

an equivalent conductance at the input and output frequencies. The implication of these assumptions is discussed later and where necessary additional theory is derived for cases where the assumptionsbecome invalidated. It should be noted, however, that no additions or modifications to the actual non-linear analysis will be required, any additional theory being concerned solely with linear circuit analysis.

Let the voltage across the junction be

$$v = V_1 \sin\omega_1 t + V_n \sin \overline{\omega_n t + \phi_n} \qquad (2.1)$$

where $\omega_n = n\omega_1$.

The current through the junction, i, is given by:

$$i = C(v)\frac{dv}{dt} \qquad (2.2)$$

where $C(v) = C_o(1 + v/V_b)^{-\gamma}$ (2.3)

and can be expanded about the operating point in a Taylor series.

Note that $V_b = V_B + \psi_o$ (2.4)

where V_B is the applied bias and ψ_o is the barrier voltage. Let us now use normalized quantities and denote them by the subscript 'd', i.e. we write:

$$v_d = v/V_b, \quad V_{dn} = V_n/V_b, \quad \text{etc.} \qquad (2.5)$$

Now expand C(v) thus:

$$C(v) = C_o(1 + c_1 v_d + c_2 v_d^2 + ... + c_i v_d^i + ...) \qquad (2.6)$$

where $C_i = (-1)^i \lfloor(\gamma + i - 1) \Big/ \{\lfloor i \ \lfloor(\gamma - 1)\}$ (2.7)

(2.7) is plotted in Fig. 2.3 versus i for $\gamma = 0.5$ and $\gamma = 0.33$.

Consider the lowest order term leading to current i_n at $n\omega_1 t$:

$$i'_{dn} = C_o c_{n-1} v_d^{n-1} \frac{dv}{dt} \qquad (2.8)$$

which, after substituting for v from (2.1) gives

$$i_{dn} = \omega_n C_o V_{dn} \cos \overline{\omega_n t + \phi_n} + I_{dn} \sin \overline{\omega_n t + n\pi/2} \qquad (2.9)$$

where $$I_{dn} = \omega_1 C_o \left|c_{n-1}\right| V_{d1}^{\,n} \left\{{}^{n-1}A_{n-1}\right\}^{\frac{1}{2}} \qquad (2.10)$$

and ${}^{m}A_i$ is the coefficient of cos iθ in the expansion of $\cos^m\theta$, i.e.

$$\cos^m\theta = \sum_i {}^{m}A_i \cos i\theta \qquad (2.11)$$

At ω_n we may write the node equation at the output node thus:

$$0 = v_n y_n + i_n \qquad (2.12)$$

Letting $y_n = Y_n \angle\theta_n$ and writing (2.12) in exponential form gives:

$$0 = V_n Y_n \exp j(\phi_n + \theta_n) + j\omega_n C_o V_n \exp j\phi_n + I_n \exp jn\pi/2 \qquad (2.13)$$

Hence $$G_{nt} + (I_n/V_n) \cos \overline{n\pi/2 - \phi_n} = 0 \qquad (2.14)$$

where G_{nt} is the total conductance at the output frequency, — i.e. the sum of the load conductance and the diode conductance.

Also ~~and~~ $$B_n + \omega_n C_o + (I_n/V_n) \sin \overline{n\pi/2 - \phi_n} = 0 \qquad (2.15)$$

where B_n is the susceptance of the filter at the output frequency; i.e. for maximum output power in G_n, the phase is determined from (2.14):

$$\phi_n = n\pi/2 - \pi \tag{2.16}$$

under which condition I_n is the current at the desired harmonic frequency flowing in G_{nt}. We may now write (2.1) thus:

$$v = V_1 \sin \omega_1 t - V_n \sin n(\omega_1 t + \pi/2) \tag{2.17}$$

We are now in a position to evaluate the general series for i_n obtained by selecting the terms contributing to power in G_{nt} at $n\omega_1 t$ from the series:

$$i_n = C_o \sum c_m v_d^m \frac{dv}{dt} \tag{2.18}$$

The required terms are obtained by expanding

$$\left\{V_1 \sin \omega_1 t - V_n \sin n(\omega_1 t + \pi/2)\right\}^m \tag{2.19}$$

and combining appropriate terms with $\frac{dv}{dt}$ to yield real components of current at $n\omega_1 t$. This leads to the result:

$$I_n = K \omega_1 C_o V_1 \tag{2.20}$$

where
$$K = \sum_{m=n-1}^{\infty} \left\{ B(m) + D(m) \right\} \tag{2.21}$$

$$B(m) = \frac{1}{2} \left| {}^m\Delta_{n+1}^{n-1} \right| \left| c_m \right| V_{d1}^m \tag{2.22}$$

$$D(m) = \frac{m}{4} \left[\frac{V_n}{V_1} \right]^2 \left\{ \frac{m-1}{4} \left[3 \left| {}^{m-2}\Delta_{n+1}^{n-1} \right| - \left| {}^{m-2}\Delta_{3n+1}^{3n-1} \right| \right] - n \left| {}^{m-1}\Delta_{3n}^{n} \right| \right\} \left| c_m \right| V_{d1}^m \tag{2.23}$$

where
$$\left| {}^m\Delta_i^n \right| = \left| {}^mA_i - {}^mA_n \right| \tag{2.24}$$

${}^mA_i$ is defined by (2.11).

The derivation of the above result is given in Appendix 2.1.1.

Note that (2.21) is of course incomplete since the full series will contain powers of (V_n/V_1) which increase indefinitely.

However, since this quantity is considerably less than unity for values of V_{d1} approaching unity (corresponding to operation in the region of optimum efficiency) only the terms shown need be considered in a practical case. This argument is justified by the results obtained : it may be seen from the theoretical curves that in fact it is often sufficient to consider only the term B(m,n).

So far only terms leading to power at the output frequency have been considered. A similar approach following from (2.18) and (2.19) leads to an expression for the reactive current flowing at the input and output frequencies. This reactive current may be considered as modifying the capacitance of the diode at the operating point to a new value C'_{o1} at ω_1 and C'_{on} at ω_n. These values may be expressed by the following two series:

$$\frac{C'_{o1}}{C_o} = \sum_m |c_m| V_{d1}{}^m \left\{ \left| {}^m\Delta^0_{\frac{1}{2},2} \right| + \left[\frac{V_n}{V_1} \right]^2 \frac{1}{2} \left| {}^{m-2}\Delta^0_{\frac{1}{2},2} \right| \right\} \quad (2.25)$$

$$\frac{C'_{on}}{C_o} = \sum_m |c_m| V_{d1}{}^m \left\{ \left| {}^m\Delta^0_{-} \right| + \left[\frac{V_n}{V_1} \right]^2 \frac{1}{4} \left| {}^{m-2}\Delta^0_{-} \right| \right\} \quad (2.26)$$

where $\frac{1}{2},2$ as a subscript is taken to mean $\frac{1}{2}A_2$, and $-$ is taken to mean 'no-coefficient'.

2.22 Mesh circuit.

The following analysis refers to the basic circuit shown in Fig.2.2. Note that a completely separate analysis is required since the circuit is not a dual of that analysed in section 2.2.1. The initial assumptions are similar : it is assumed that only a current I_1 at the input frequency f_1 passes through Z_1 and only a current at the output frequency f_n passes through Z_n. This implies that no other currents

are flowing through the diode. The implications of these assumptions are discussed later but it is again pointed out that any additions or modifications required will be concerned solely with a linear circuit analysis.

Let the current through the junction be:

$$i = I_1 \sin \omega_1 t + I_n \sin \overline{n \omega_1 t + \phi_n} \tag{2.27}$$

The charge is expressed as a function of time thus:

$$q(t) = \int i \, dt$$

$$= \int C(v) \, dv \tag{2.28}$$

where $C(v)$ is defined by (2.3)

Let $q(t) = q + Q_o$ (2.29)

where $$q = -\frac{I_1}{\omega_1} \cos \omega_1 t - \frac{I_n}{\omega_n} \cos \overline{\omega_n t + \phi_n} \tag{2.30}$$

Then $$q + Q_o = \frac{C_o V_b}{1-\gamma} (1 + v_d)^{1-\gamma} \tag{2.31}$$

or thus: $$v_d = -1 + \left[\frac{Q_o (1-\gamma)}{C_o V_b} \right]^{\frac{1}{1-\gamma}} (1 + L_1 q_d^{\,1} + \ldots + L_i q_d^{\,i} + \ldots) \tag{2.32}$$

where letting $\gamma' = 1/(1-\gamma)$ (2.33)

L_i is defined thus:

$$L_i = \frac{\gamma' !}{(\gamma' - i)! i!} \tag{2.34}$$

and $$q_d = q/Q_o \tag{2.35}$$

Other quantities are as previously defined.

Q_o is found by equating the 'd.c.' terms of (2.32) using (2.30) and leads to the result:

$$Q_o = C_o V_b \Big/ \left\{ (1-\gamma)(1+\delta)^{1-\gamma} \right\} \tag{2.36}$$

where $\delta =$

$$\sum_{m=2} I_1^{\,m} \cdot L_m \cdot \left[\omega_1^{\,m} Q_o^{\,m}\right]^{-1} \left\{ {}^{m}A_o + \frac{m(m-1)}{24}\left[\frac{I_n}{I_1 n}\right]^2 \left| {}^{m-2}A_o - \tfrac{1}{2}{}^{m-2}A_{2n} \right| \right\}$$

summed over all even values of m. (2.37)

From (2.32) and (2.30) we may write the lowest order term leading to a voltage v_n at ω_n :

$$v_{dn} =$$

$$-(I_n/n\omega_1 Q_o)\cos\overline{\omega_n t + \phi_n} + (-1)^n (I_1/\omega_1 Q_o)^n L_n{}^n A_n \cos \omega_n t \quad (2.38)$$

The mesh equation at ω_n is :

$$0 = i_n z_n + v_n \quad (2.39)$$

or, rewriting in exponential form :

$$0 = (I_n Z_n / V_b) \exp j(\phi_n + \theta_n) - j(I_n/\omega_n Q_o) \exp j\phi_n$$

$$+ (I_1/\omega_1 Q_o)^n {}^n A_n L_n \exp j(\pi/2 + n\pi) \quad (2.40)$$

hence $I_{dn} R_{nt} + (I_1/\omega_1 Q_o)^n A_n L_n \cos\overline{\pi/2 + n\pi - \phi_n} = 0$ (2.41)

where R_{nt} is the total resistance in the output mesh, and

$$j\, I_{dn} X_n - j\, I_n/\omega_n Q_o + j(I_1/\omega_1 Q_o)^n L_n{}^n A_n \sin\overline{\pi/2 + n\pi - \phi_n} = 0$$

where X_n is the reactance of the filter in the output mesh. (2.42)

Hence from (2.41), taking into account the fact that

$$L_n = (-1)^n |L_n| \quad \text{for} \quad 0 < \gamma \leq 1/2 \quad (2.43)$$

we obtain the condition for maximum output:

$$\phi_n = -\pi/2 \quad (2.44)$$

Hence (2.27) may be re-written:

$$i = I_1 \sin \omega_1 t - I_n \cos n\omega_1 t \quad (2.45)$$

Consider now the general series for v_n given by (2.32). As in the case of the node circuit this can be evaluated using the Binomial series to find the terms of

$$\left\{I_1 \cos \omega_1 t + (I_n/n) \sin \omega_n t\right\}^m$$

leading to current in R_n at ω_n. This yields the result:

$$V_n = K I_1/(\omega_1 C_o) \qquad (2.46)$$

where $V_n = I_n R_n$ and is the voltage contributing to power at ω_n

and $K =$

$$\frac{(1-\gamma)}{(1+\delta)\gamma} \sum_{m=n}^{\infty} |L_m| (I_1/\omega_1 Q_o)^{m-1} \left\{ {}^{m}A_n + \left| \frac{I_n}{nI_1} \right|^2 \frac{m(m-1)}{8} \left|{}^{m-2}\Delta_{3n}\right| \right\} \qquad (2.47)$$

The above result is derived in Appendix 2.1.2.
The complete series will contain higher powers of I_n/nI_1 but since this quantity is less than unity, (2.47) gives a very good approximation to the full series. In fact (as in the node circuit) it will often be sufficient to consider only the first term in the above expression. This will be seen clearly later when the series is evaluated.

The effective capacitance changes at the input and output frequencies are as follows :

$$\frac{C_o}{C'_{on}} = \frac{C_o V_b}{Q_o} \sum \left[\frac{I_1}{\omega_1 Q_o}\right]^{m-1} |L_m| \, m \left[\left|{}^{m-1}A_o\right| - \frac{1}{2} \left|{}^{m-1}A_{2n}\right| \right] \qquad (2.48)$$

$$\frac{C_o}{C'_{o1}} = \frac{C_o V_b}{Q_o} \sum \left[\frac{I_1}{\omega_1 Q_o}\right]^{m-1} |L_m| \left\{ \left|{}^{m}A_1\right| + \frac{m(m-1)}{4} \left[\frac{I_m}{nI_1}\right]^2 \left[\left|{}^{m-2}A_1\right| - \left|\frac{1}{2}\,{}^{m-2}A_{2n-1}\right| - \left|\frac{1}{2}\,{}^{m-2}A_{2n+1}\right| \right] \right\} \qquad (2.49)$$

2.2.3 Discussion of the series involved in the preceding analysis.

2.2.3.1 General considerations.

Having evolved expressions for the currents and voltages generated by the non-linearity, it is necessary to consider the series expansions involved. Each result is given in a form containing the co-efficients ${}^{m}A_{i}$ as defined by (2.11). These coefficients are given in Table 1 for a useful range of values up to i = 10 amd m =101. It is seen that for a given m, the co-efficients decrease for i increasing (omitting the case where i = 0) and for a given i, the co-efficients eventually decrease for m increasing. Since the series for 'K' in both the node and mesh circuits contains a multiplying factor of the form x^{m} where x is constant for a given summation (see (2.21) and (2.47) from whence it is seen that for the node circuit $x = V_{d1}$ and for the mesh circuit $x = I_1/\omega_1 C_0$) and less than unity, it is apparent that if sufficient terms are taken the series may be summed to any degree of accuracy and the remainder evaluated. This convergence is obvious in the case of (2.22) and the first term of (2.47), (i.e. the ${}^{m}A_{n}$ term) but requires some further examination for the other terms. Note that in any practical evaluation the convergence will become apparent as successive terms are calculated and is quite rapid in the case of low order multipliers (e.g. X2 and X3), a dozen terms being normally ample for the remainder to be negligible. Note that in any particular summation only odd or even values of i are involved. For this reason the given table has been divided into two sections.

Let us now consider the mathematical expressions for the co-efficients.* These may be written thus:

---

* The author is grateful to Mr. P. Apaydin (of Imperial College) for drawing attention to the fact that the co-efficients of the $\cos^{m}\theta$ series are related to Pascal's triangle.

$$ {}^{m}A_i = 2^{1-m} \cdot {}^{m}C_{\frac{m+i}{2}} \quad , \qquad \text{for m odd} \tag{2.50} $$

$$ \left.\begin{aligned} {}^{m}A_i &= 2^{1-m} \cdot {}^{m}C_{\frac{m+i}{2}} \quad , \quad i \neq 0 \\ &= 2^{-m} \cdot {}^{m}C_{m/2} \quad , \quad i = 0 \end{aligned}\right\} \quad \text{for m even} \tag{2.51} $$

The point at which the coefficients start to decrease is found by comparing two adjacent terms thus:

$$ \frac{{}^{m+2}A_i}{{}^{m}A_i} = 1 + \frac{i^2 - m - 2}{m^2 + 4m + 4 - i^2} \tag{2.52} $$

which, for $i < m$, gives the condition:

$$ m > i^2 - 2 \tag{2.53} $$

for the co-efficients to start to decrease. Thus by evaluating the series for $\cos^{(i^2-2)}\theta$ we can find the maximum value which ${}^{m}A_i$ attains. In practice it is found to be sufficient to consider only the terms as far as $m = n^2$ for a particular multiplier. The particular cases which occur will now be considered.

2.2.3.2. Node circuit.

The condition for convergence of (2.22) can be shown to be a good approximation:

$$ 2^{\frac{1-\gamma}{m}} + \frac{2}{m+n} > \left[\frac{n}{m}\right]^2 - \left[1 - (V_{dl})^2\right] \tag{2.54} $$

which gives for $\gamma = 1/2$ and $V_{dl} \approx 1$, this being the 'worst' case;

$$ m > n^2/3 \quad , \quad \text{(accurately true for } m \gg n\text{)} \tag{2.55} $$

Thus when (2.55) holds, the first part of (2.21) may be evaluated to any desired degree of accuracy since the ratio of successive terms is less than unity and the remainder after

summing to m/2 terms is:

$$S_R < R/(1-x^2) \qquad (2.56)$$

where R is the value of the last term, and $x = V_{dl}$.

It can be shown that the condition for (2.23) to start to decrease is:

$$(1 - 2\gamma/m) > x^2 , \quad \text{(accurately true for } m \gg n) \qquad (2.57)$$

which gives for $\gamma = 1/2$:

$$1/m < 1 - x^2 \qquad (2.58)$$

It may appear at first sight that this will be tedious to compute, but since it involves $(V_n/V_1)^2$ and since this quantity is small for x having values near unity, (which, from (2.58) indicates large values of m) a very rough approximation will usually suffice. This is made clear by referring to the curves for 'K' (Figs.2.6 to Fig.2.11.) from which itis seen that the effect of including (2.23) is slight as V_{dl} tends to unity.

2.2.3.3. Mesh circuit.

When $I_n \ll nI_1$, successive terms of (2.47) can be shown to converge when:

$$m > (n^2 - 2)/3 \qquad (2.59)$$

In fact, since $I_1/\omega_1 Q_o$ is always considerably less than unity (unlike the node case) it is only necessary to sum the first few terms in most cases.

The second part of (2.47) may be shown to converge when

$$(m + n^2)/m^2 < 1 - (I_1/\omega_1 Q_o)^2 \qquad (2.60)$$

Again since $I_1/\omega_1 Q_o$ is less than unity the series converges very rapidly.

It will be found that the summation involved in (2.37)

is quite simple and the second term can always be neglected in practice. A curve for δ is given in Fig.2.19.

2.2.4. Limiting conditions of signal across the junction.

2.2.4.1 Node circuit

We have obtained expressions for the output harmonic voltage or current in terms of the input to the diode and containing in some cases implicitly the voltage or current gain of the stage. In order to determine the complete solution it is necessary to fix another set of conditions: this is done by considering the limitation imposed by the fact that the maximum voltage across the junction is restricted to a value equal to or less than the voltage V_b defined by (2.4). Thus using (2.17) we may write the limiting condition thus:

$$v_{min} = -V_b \tag{2.61}$$

$$\text{i.e.} \quad V_b = -\left[V_1 \sin \omega_1 t - V_n \sin n(\omega_1 t + \pi/2)\right]_{min} \tag{2.62}$$

This gives:

$$\frac{V_n}{V_1} = \frac{\cos \omega_1 t}{n \cos n(\omega_1 t + \pi/2)} \tag{2.63}$$

$$\text{and} \quad (V_1/V_b)^{-1} = -\left[\sin \omega_1 t - \frac{1}{n} \cos \omega_1 t . \tan n(\omega_1 t + \pi/2)\right] \tag{2.64}$$

This solution (obtained by evaluating (2.63) and (2.64) for specific values of $\omega_1 t$) is plotted in the form V_n/V_1 versus V_1/V_b in Fig.2.4 for a X2, X3 and X10 multiplier. Also shown is the solution obtained by solving

$$V_1 + V_n = -V_b \tag{2.65}$$

which is the limiting case for high order multipliers. In Fig.2.5 is shown the result obtained when the peak voltage is limited to $0.95\ V_b$, corresponding to the case where the forward conduction characteristic is such that only this fraction of

the characteristic can be effectively used before conduction losses become severe. This effect will be discussed in more detail in section.4.7. These two sets of curves may now be used to solve (2.21). The results obtained are plotted in Figs.2.6 to Fig.2.11 for γ = 0.5 and 0.33, for X2, X3 and X10 multipliers. Note that the values of 'K' obtained when the peak voltage is limited to 0.95 V_b are not significantly different from those plotted. The main effect of this limitation will become apparent when the power loss is considered in sect.2.3.

2.2.4.2. Mesh circuit.

The mesh circuit is, of course, also restricted by the voltage across the junction. However, since the diode is being used as a current operated device the limiting conditions are not directly related to the parameters used in the preceding analysis and in order to find the voltage across the junction it is necessary to extend the theory.

Let the voltage across the junction be

$$v = V_{1t} \sin \overline{\omega_1 t + \psi_1} - V_{nt} \sin \overline{\omega_n t + \psi_n} \qquad (2.66)$$

Consider the voltage at the input frequency:

$$v_1 = -I_1/(\omega_1 C_{o1}') \cos \omega_1 t + I_1 R_{eq} \sin \omega_1 t \qquad (2.67)$$

In this equation C_{o1}' is the 'effective' capacitance at the input frequency as defined by (2.49) and R_{eq} is the 'effective' resistance, being a function of the input and output currents and related thus:

$$I_1^2 \cdot R_{eq} = I_n^2 \cdot R_{nt} \qquad (2.68)$$

since all the input power is converted to power at the output frequency. Using this equation and (2.46) enables us to solve

for V_{1t} and ψ_1.

$$V_{1t} = \left[\frac{I_1}{\omega_1 C_{o1}'}\right] \sqrt{1+K^4.n^2.\left[\frac{1}{\omega_n C_o R_{nt}}\right]^2 \left[\frac{C_{o1}'}{C_o}\right]^2} \qquad (2.69)$$

$$\tan \psi_1 = -\left[\frac{1}{\omega_n C_o R_{nt}}\right]\left[\frac{1}{n K^2}\right]\left[\frac{C_o}{C_{o1}'}\right] \qquad (2.70)$$

The voltage at the output frequency is

$$v_n = -\left[I_n/\omega_n C_{on}'\right] \cos \overline{\omega_n t - \pi/2} + V_n \cos \omega_n t \qquad (2.71)$$

which gives:

$$V_{nt} = \left[\frac{I_1}{\omega_1 C_o}\right] K \sqrt{1 + \left[\frac{1}{\omega_n C_{on}' R_{nt}}\right]^2} \qquad (2.72)$$

and $$\tan \psi_n = -\omega_m C_{on}' R_{nt} \qquad (2.73)$$

Thus although an explicit solution for the limiting conditions is not possible, we are now in a position to solve, by a relatively simple trial and error process, the condition

$$v_{min} = -V_b \qquad (2.74)$$

where v is found from (2.66), (2.69), (2.70), (2.72) and (2.73). This solution is plotted in Figs. 2.21 to Fig. 2.23 for a X2 circuit, γ = 0.5 and 0.33 and for a X3 circuit γ = 0.33, with $\omega_n C_o R_{nt}$ as a dependent variable.

2.3 Evaluation of power loss

2.3.1 Node circuit

Having found a relation between the input and output voltages of the multiplier we are now in a position to find the efficiency of a stage for a given diode. Define the efficiency η_1 by

$$\frac{1}{\eta} = \frac{\text{Power available from generator}}{\text{Power delivered to load}} \qquad (2.75)$$

$$= \frac{P_{in}}{P_{out}} \quad \text{under matched conditions}$$

where P_{in} is the power input to the circuit at ω_1

P_{out} is the useful power output at $n\,\omega_1$

Since we are interested in computing the maximum efficiency obtainable with a given diode the filters will be assumed lossless. The circuit may be represented in nodal form as in Fig. 2.1, (C), where the series loss resistance of the diode has been replaced by an equivalent shunt conductance. It is assumed for the purpose of this analysis that the 'Q' factor of the diode is sufficiently high for the equivalent shunt conductance, G, to be given by

$$G = (\omega C)^2 \cdot R_s \qquad (2.76)$$

where C is the capacitance of the diode and R_s its series resistance. G_{eq} is defined as the conductance seen at the input frequency due to the power generated at the harmonic frequency i.e.

$$V_1^2 \cdot G_{eq} = V_n^2 \cdot G_{nt} \qquad (2.77)$$

where G_{nt} is the total conductance at the output frequency i.e.

$$G_{nt} = G_o + G_{dn} \qquad (2.78)$$

where G_o is the load conductance and G_{dn} is the equivalent shunt conductance of the diode at ω_n, i.e.

$$G_{dn} = (\omega_n C_{on}')^2 \cdot R_s$$

$$= \left[(\omega_n C_{on}') / Q_{dn}\right] \cdot \left[C_{on}' / C_o\right] \qquad (2.79)$$

where Q_{dn} is the diode 'Q' factor at ω_n, defined by

$$Q_{dn} = 1/\omega_n C_o R_s \qquad (2.80)$$

$$P_{in} = V_1^2 (G_{dl} + G_{eq}) \qquad (2.81)$$

$$P_{out} = V_m^2 G_o \qquad (2.82)$$

Using (2.77) to (2.82) and (2.20) gives the power loss:

$$\frac{1}{\eta} = \left\{1+\frac{1}{K^2 Q_{dn}}\left[\frac{G_{to}}{\omega_n C_o}\right]\left[\frac{C_{ol}'}{C_{ol}}\right]^2\right\} \Big/ \left\{1-\frac{1}{Q_{dn}}\left[\frac{\omega_n C_o}{G_{to}}\right]\left[\frac{C_{on}'}{C_{on}}\right]^2\right\} \qquad (2.83)$$

Note the presence of C_{on}' and C_{ol}' (defined by (2.25) and (2.26)). These functions are plotted on Fig.2.12. It is apparent that the presence of these factors has a degrading effect on the efficiency. (2.75) may be evaluated using the curves of Fig.2.4, to Fig.2.12. The results thus obtained are given for various cases in Figs. 2.14 to Fig.2.18.

2.32 Mesh circuit

The efficiency for the mesh circuit may be evaluated in a similar manner, the basic circuit being given in Fig.2.2 (C). The resulting expression for power loss is:

$$\frac{1}{\eta} = \left\{1 + \frac{\omega_n C_o R_{nt}}{n^2 K^2 Q_n}\right\} \Big/ \left\{1 - \frac{1}{Q_n} \frac{1}{\omega_n C_o R_{nt}}\right\} \qquad (2.84)$$

where R_{nt} is the total resistance at the output frequency, including the diode resistance.

This power loss has been calculated using the values of 'K' and $\omega_n C_o R_{nt}$ plotted in Figs.2.21 to Fig.2.23 and curves are given in Figs. 2.24 to Fig.2.26 for a X2 and X3 multiplier.

2.4 Discussion of the theoretical results

2.4.1. Assumptions and limitations in the theory

The preceding analysis assumes that the following conditions hold:

(a) The filters present short circuit paths (in the node circuit) or open circuit paths (in the mesh circuit) at all frequencies other than their resonant frequencies.

(b) No losses are introduced by the filters.

(c) The diode 'Q' factor is sufficiently high for the series loss resistance to be replaced by an equivalent shunt conductance at both input and output frequencies in the node circuit.

(d) The diode capacitance law is given accurately by substituting the appropriate value of γ in the relevant expansion.

(e) The effect of stray reactances is negligible.

(f) The effect of forward conduction may be allowed for by limiting the peak value of voltage to a certain fraction of V_b.

The condition specified in (a) may not always hold in a simple circuit of the type shown in Fig.2.1(a). It is,

however, possible to obtain the condition by the use of additional filters as shown in Fig.2.1,(b). The effect of not including these filters is considered in detail in section 4.3.

Filter losses may be accounted for by a separate analysis using the 'K' curves obtained above. This is treated in section 4.2.

For the purpose of estimating losses there is virtually no error involved in replacing the series resistance by an equivalent shunt conductance as in (2.79), for diode 'Q' factors greater than 10. The effect of the voltage drop across the series resistance does not seriously affect the performance, since the analysis is based on the voltage across the junction and any drop in voltage may be compensated by increasing the input voltage by a small amount(see sect.4.5).

In practice it is found that the capacitance law is as predicted by the theoretical expressions used above (2.7) even for values of bias approaching the barrier voltage. As a rough guide the diode may be driven to within 0.1 volt of the barrier voltage before conductance effects become appreciable with silicon diodes. This means that for a bias of 2.0 volts a value of $V_b' = 0.95\ V_b$ is a reasonable value to take for the limiting conditions of peak voltage.* The limit of operation in the reverse direction is caused either by avalanching or by stray shunt capacitance; the former generally predominates at low frequencies, the latter at high frequencies. Neither of these effects presents a serious limitation in practice since it is usually convenient to operate at small values of reverse bias. Further consideration is given to stray reactances in section 4.8.

It is thus apparent that the preceding analysis gives a basis for the design and comparison of various circuits. When

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* See sect.4.7 for further treatment of this point.

any of the above assumptions become invalidated, errors likely to be introduced may be separately accounted for.

2.4.2. Comparison of various circuits using the power loss curves.

2.4.2.1. Node circuit.

A study of the power loss curves for optimized circuits given in Fig.2.18 and Fig.2.26 enables some useful conclusions to be made about the relative merits of various types of multipliers. Let us consider the Power Loss versus Q_{dn} curves given in Fig.2.18 for a node circuit. An ideal diode is defined to be one in which the forward conduction characteristic is such that the diode may be driven to the point where the depletion layer capacitance is theoretically infinite before conduction effects dominate the behaviour. In fact, for low order multipliers, the error involved in assuming this property is very small: it may be seen from the relevant curves that the increase in loss in a X3 circuit is about 1dB and in a X2 circuit about 0.3dB when the peak applied voltage is limited to $0.95V_b$ instead of $1.0V_b$, for a Q_{dn} of 10, and for an optimized circuit. By referring to the 'K' versus V_1/V_b curves given in Fig.2.6 to Fig.2.11 where K is defined by (2.20) it is apparent that as the order of multiplication is increased K becomes increasingly dependent upon V_1/V_b. This is predicted immediately by the first order approximation for K which gives $K \propto (V_1/V_b)^{n-1}$. Thus we would expect the power loss to become increasingly dependent upon V_b' where we define V_b' as the maximum 'useful' voltage swing, i.e. the maximum voltage that may be superimposed on the bias voltage before conduction effects dominate. This effect is clearly shown by comparing the curves for a X10 multiplier with those for a X2 and X3 multiplier given in Fig.2.18. The

respective differences in losses for X2, X3 and X10 circuits are, for a diode Q_{dn} of 10, 0.3 dB, 1.0 dB and 11.0 dB, for $V_b' = 0.95\ V_b$.

Consider now the problem of generating a high harmonic given a particular diode. Let us take as an illustration a diode with $Q_{dn} = 10$. Consider first of all the case of an ideal diode, with $\gamma = 1/2$.

Three X2 stages cascaded together give an overall loss of 6.0 dB.

Two X3 stages cascaded together give an overall loss of 8.5 dB.

One X10 stage gives a loss of 16.0 dB.

In estimating the above losses it must be remembered that the diode 'Q' factor is inversely proportional to frequency and hence the Q_{dn} for successive stages decreases in proportion to the order of multiplication of the stage. This has been taken into account in the above examples.

The above three examples have been chosen to give approximately the same order of multiplication (X8, X9, and X10). It is thus apparent that for maximum efficiency the best method is to use X2 circuits cascaded to give the required output frequency. (For an accurate comparison, note that the above losses should be corrected to allow for the differences in overall frequency 'gain': the error involved is, however, small, the corrected values of loss being:- 6.7 dB, 8.9 dB and 16 dB, taking X10 as a basis for comparison).

If the case of a diode with non ideal conduction characteristics is considered it is at once apparent from the curves for $V_b' = 0.95 V_b$ that the superior performance of the low order multipliers is enhanced since the X2 losses are increased by only a factor of 1.09 compared with a factor of 1.7 for the X10 losses.

The case of $\gamma = 0.5$ has been considered since this gives the most efficient multiplication. By referring to Fig.2.3 the effect of using a diode with $\gamma = 0.333$ can be seen. It is apparent that the higher order co-efficients in the Taylor expansion are reduced by a larger factor than the lower order co-efficients. Thus the efficiency of higher order multipliers will be reduced by a greater amount than for lower order multipliers. (The values of 'Y' may be found from Fig.2.6 to Fig.2.11. Thus the above conclusions concerning the relative merits of the three orders of multiplier still hold, the differences being in fact more pronounced.

2.4.2.2. Mesh Circuit.

Consider now the results for the mesh type multiplier given in Fig.2.26. Using this circuit with $\gamma = 0.5$ it is only possible to multiply by two since all terms in the expansion for v_d (2.32) above the first are zero. It is seen that the power loss is the same as that for a X2 node circuit for $Q_{dn} \geqslant 10$, and approximately the same for $Q_{dn} < 10$; (note that the analysis is only approximately valid for low values of 'Q' factor : this is discussed in sect.4.5.) it may thus be concluded that the two circuits give essentially the same power loss for various diode 'Q' factors. Also shown in Fig.2.26 is the curve for $\gamma = 0.333$ which, as expected, gives a slightly poorer efficiency.

Since no harmonics higher than the second are generated using this circuit with $\gamma = 0.5$, one would not expect very great efficiencies for $\gamma = 0.333$, due to the fact that the Taylor co-efficients decrease rapidly in value after the first, (see (2.34)). This is confirmed by the curve for a X3 multiplier (Fig.2.26), which shows, for a 'Q' of 10, a loss five times that of a X2 multiplier. It may therefore be concluded that this circuit is not of any practical value for

multiplication other than by two.

2.4.2.3. General Remarks.

Figs.2.14 to Fig.2.17 and Figs.2.24 to Fig.2.25 give design curves for the node and mesh circuits respectively. It is apparent that to obtain the optimum efficiency a particular value of the parameter $G_{nt}/\omega_n C_o$ for a node circuit and $\omega_n C_o R_{nt}$ for the mesh circuit, must be chosen. In practice these parameters may be determined by other requirements (e.g. availability of suitable diodes); in this case it is possible to determine from the curves how far off optimum the circuit is operating. Note that for high 'Q' diodes the optimum is broad with respect to the above parameters; conversely for low 'Q' diodes the value of the parameters must be more accurately set to obtain the optimum conditions. The value of $G_{nt}/\omega_n C_o$ or $\omega_n C_o R_{nt}$ having been determined it remains to know what drive must be applied to the circuit in order to operate under optimum conditions. This may be found by referring to Fig.2.13 for the node circuit and Fig.2.21 to Fig.2.23 for the mesh circuit. Of interest also is the voltage or current gain of the node or mesh circuits, particularly when cascading circuits together. These quantities may be found from Fig.2.4 and Fig.2.5 for the node circuit and calculated from Fig.2.21 to Fig.2.23 for the mesh circuit.

2.4.3. Active behaviour of specific circuits.

The preceding theory may also be used to predict the behaviour of a circuit under practical operating conditions. Of particular interest is the effect of varying the drive. This may be estimated by referring to the appropriate 'K' curves for the circuit in question. The value of 'K' for a given drive below the optimum value will lie somewhere between the optimum 'K' curve and that plotted for $V_n \ll V_1$ (node

circuit) or $I_n \ll nI_1$ (mesh circuit). Since these two curves are quite close to each other it is possible to estimate simply the variation in 'K' (which, for a particular circuit is proportional to the voltage or current gains) with variation in input voltage (or current).

Note also the variation of input conductance or resistance obtainable from the 'K' curves using (2.77) or (2.68). This of course determines the matching condition at the input.

Fig.2.12 and Fig.2.20 are also of interest since they show the change in diode capacitance as the input is varied. In a practical circuit this of course means that as the input is varied the capacitances forming the resonant circuits must be altered to obtain maximum output. Note that in the analysis for the node circuit these capacitances occur in the expression for power loss given by (2.75), but in the mesh circuit analysis the power loss equation is independent of capacitance changes due to reactance terms introduced by the non-linearity. This comes from the fact that in the mesh circuit the series loss resistance of the diode is constant and directly related to the 'Q' factor defined by (2.80) whereas in the node circuit the equivalent shunt conductance is a function of the actual diode capacitance as given by (2.79).

2.5. Experimental results.

2.5.1. Introduction.

Experiments were carried out in order to verify the preceding large signal theory. No measurements on power loss are included at this stage since a complete analysis of the losses introduced in a practical circuit has not yet been presented: this is dealt with in section 4. Since only a verification of the non-linear operation of the circuit was required, the circuits were not optimized. This enabled values of parameters to be chosen which facilitated direct measurement of the quantities concerned in the large signal analysis.

2.5.2. Node Circuit.

The circuit for the node type multiplier is given in Fig.2.27. The output circuit is designed so that the output voltage is small compared ~~to~~ with the input voltage over the greater part of the range of V_1/V_b. This enables the non-linear operation to be verified up to values of V_1/V_b approaching unity. The results obtained in this way should lie between the two large signal curves of Figs.2.6 to Fig. 2.11. tending towards the lower one at low values of V_1/V_b and the upper one as V_1/V_b tends to unity. The input circuit is designed so that its resonating capacitance is large compared ~~to~~ with the diode capacitance so that only a small fraction of the voltage at the second harmonic frequency appears across the input tank.

The diode capacitance characteristics were measured under small signal conditions and a value for γ estimated. This was found to be 0.39 and the results of the experiment are shown together with the theoretical curves of Fig.2.7, Fig.2.9

and Fig.2.11. In comparing the results with the theoretical curves it must, therefore, be remembered that the measured points should lie slightly above the (b) curves, i.e. in between the theoretical curves for $\gamma = 0.5$ and $\gamma = 0.333$ tending towards the latter. In fact the measured results fall slightly short of the expected values: possible sources of error are :

(a) Measurement of 'Q' factor of output circuit.
(b) Measurement of circuit capacitances.
(c) Voltage measurements.
(d) Measurement of γ .

Any one of these could give rise to an error in 'K' corresponding to a constant (approximately constant in the case of (d)) multiplying factor over the range of V_1/V_b. The important point to notice is that the large signal law is accurately verified. Note that the experiments were restricted to verifying the preceding theory and no attempt is made to measure the performance under conditions where the diode is driven into forward conduction. The readings are taken up to values of V_1/V_b which cause a small (0.1 mA.) current to flow through the bias resistance.

The capacitance variation shown in Fig.2.12 was checked in the X10 circuit. Since the change is small it is difficult (and not very useful) to obtain accurate measurements. The results show however that the theoretical trend is realised in practice and it is seen that the order of magnitude of the change agrees with the theory.

2.5.3. Mesh Circuit.

The arrangement used for the mesh type multiplier is shown in Fig.2.28. Again, the output circuit is designed so that the output current is small compared to the input

current through the diode so that measurements may be made up to values of $I_1 / \omega_1 C_o V_b$ approaching unity. Also, C_1 and C_n are made much less than C_o so that the two meshes act as effective filters to their respective currents. This necessitated making C_o large and for this reason the diode was operated at zero bias. The measured value of γ was 0.33 and the measured points are shown on Fig. 2.22 and Fig. 2.23. In the case of the X10 circuit the output was too small to be measured for $I_1 / \omega_1 C_o V_b$ less than unity. Approaching this value with bias current of 1.0 μ A. gave a value of 'K' less than 5×10^{-6}. Theory gives a value of 1.0×10^{-6} at $I_1 / \omega_1 C_o V_b = 1.0$. As the input was increased causing large current to flow the measured output rose sharply. This is due to a mechanism other than that under investigation and will be dealt with in section 3. Similar, though less pronounced, effects were observed in the X3 circuit under forward current conditions. It has already been concluded that these two circuits are not of much practical importance and the measurements confirm the theoretical predictions. The X2 results are seen to agree closely with theory: the main sources of error are:

(a) estimation of ψ_o.
(b) estimation of $I_1 / \omega_1 C_o V_b$.

both of these quantities being particularly susceptible to error due to the difficulty in performing measurements in the region of zero bias.

2.6. Conclusions.

In this section an accurate large signal theory has been evolved for the depletion layer operation of two basic circuits, the node and the mesh types, and the theory has been

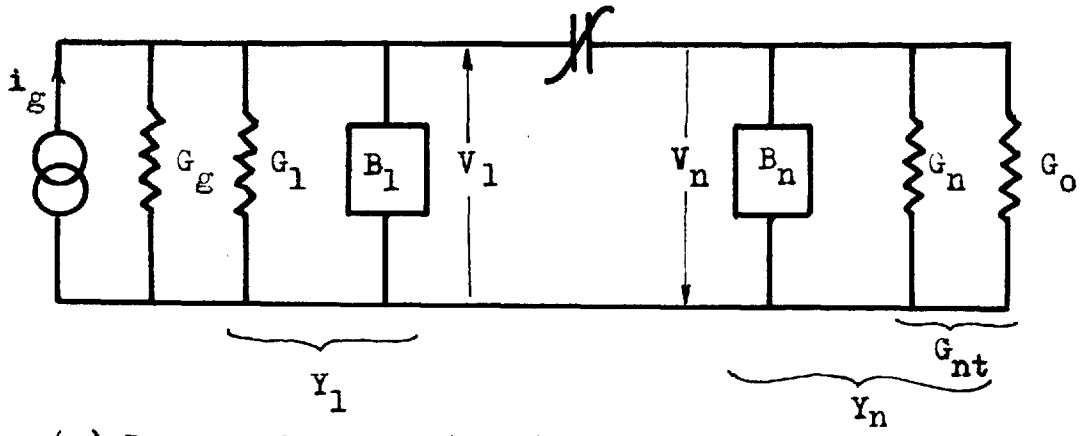
verified experimentally. Curves have been produced which show the minimum power loss obtainable with various diodes together with the circuit conditions to obtain this minimum loss. A comparison is now possible between various circuits and combinations of circuits, assuming the realizeability of the optimum efficiency. Indications have been given as to possible additional losses: these will be treated in detail in section 4.

m↓ i→	0	2	4	6	8	10
0	1·000					
2	5000	5000				
4	3750	5000	1250			
6	3125	4690	1875	312		
8	2738	4370	2185	625	78	
10	2460	4100	2341	880	195	19
12	2260	3870	2420	1072	322	59
14	2095	3665	2441	1221	444	111
16	1960	3495	2441	1331	555	171
18	1859	3338	2425	1417	653	233
20	1763	3203	2400	1477	739	295
22	1684	3085	2370	1523	812	356
..	....	....	....	....	....	....
46	1170	2242	1974	1595	1180	801
..	....	....	....	....	....	....
100	791	1553	1465	1325	1151	966

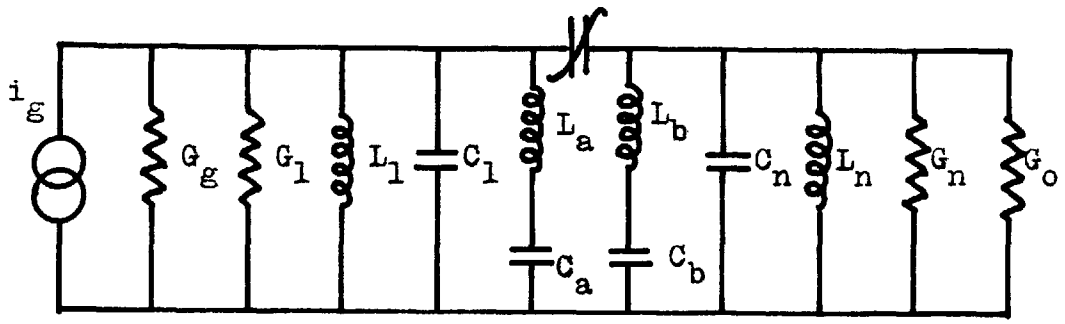
m↓ i→	1	3	5	7	9	11
1	1·000					
3	7500	2500				
5	·6250	3125	625			
7	5470	3280	1094	156		
9	4920	3280	1406	352	39	
11	4510	3220	1610	536	107	10
13	4190	3140	1742	697	190	32
15	3921	3055	1831	831	278	64
17	3700	2965	1889	944	363	104
19	3520	2880	1920	1034	443	147
21	3368	2801	1939	1108	517	194
23	3226	2727	1947	1168	584	241
..	....	....	....	....	....	....
47	2291	2108	1784	1387	991	650
..	....	....	....	....	....	....
101	1570	1510	1398	1240	1062	872

$$\cos^m\theta = \sum_i A_i \cos i\theta$$

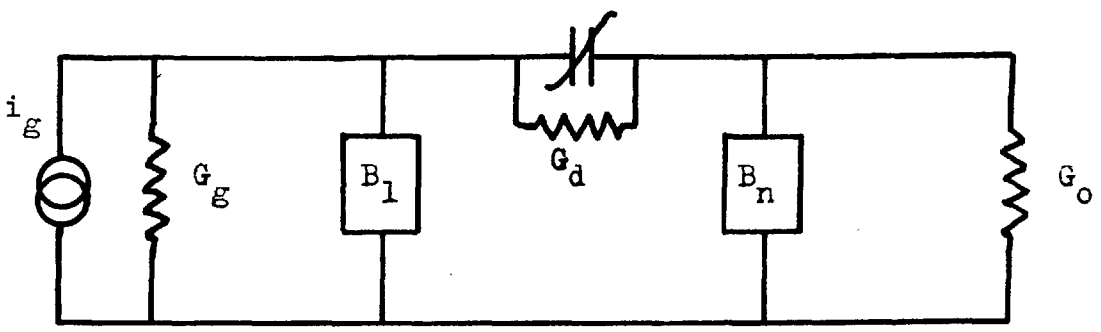
Table I Series used in large signal analysis



(a) Basic node circuit

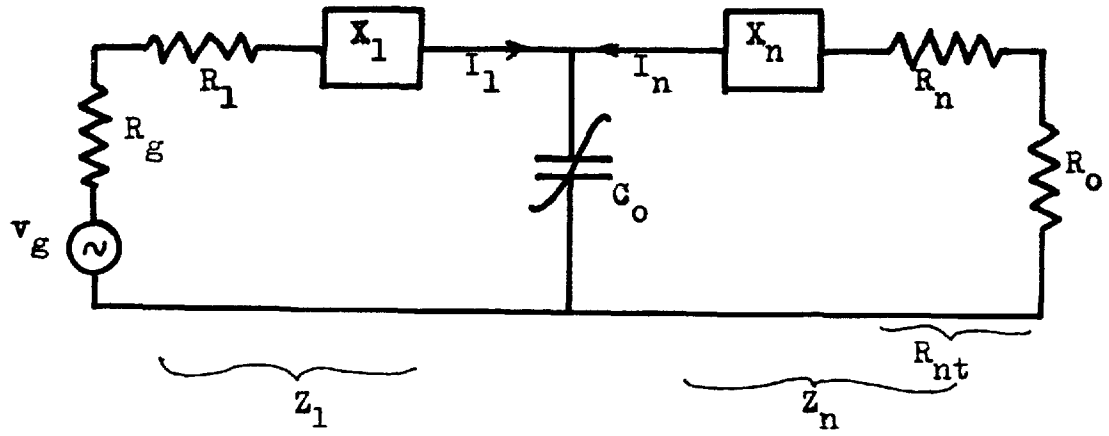


(b) Practical realization of above circuit

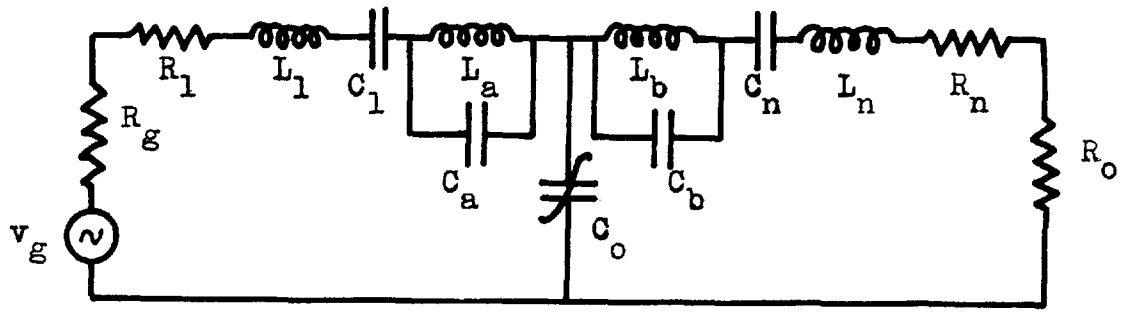


(c) Circuit used in estimating power loss due to diode

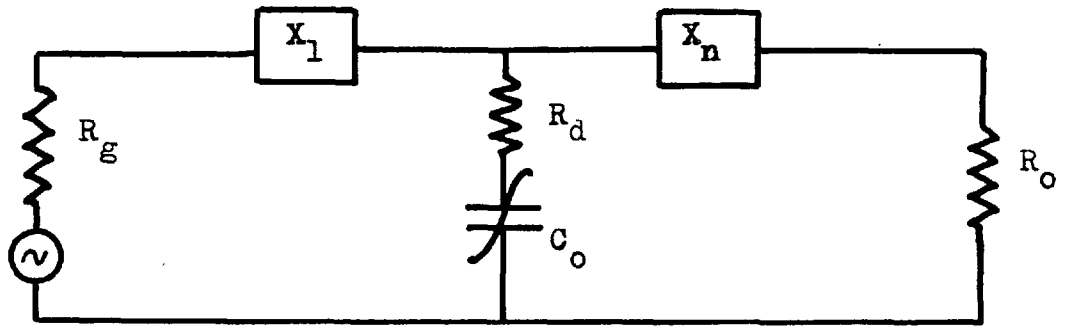
Fig.2.1 Node circuits used in the analysis



(a) Basic mesh circuit



(b) Practical realization of above circuit



(c) Circuit used in estimating power loss due to diode

Fig.2.2 Mesh circuits used in the analysis

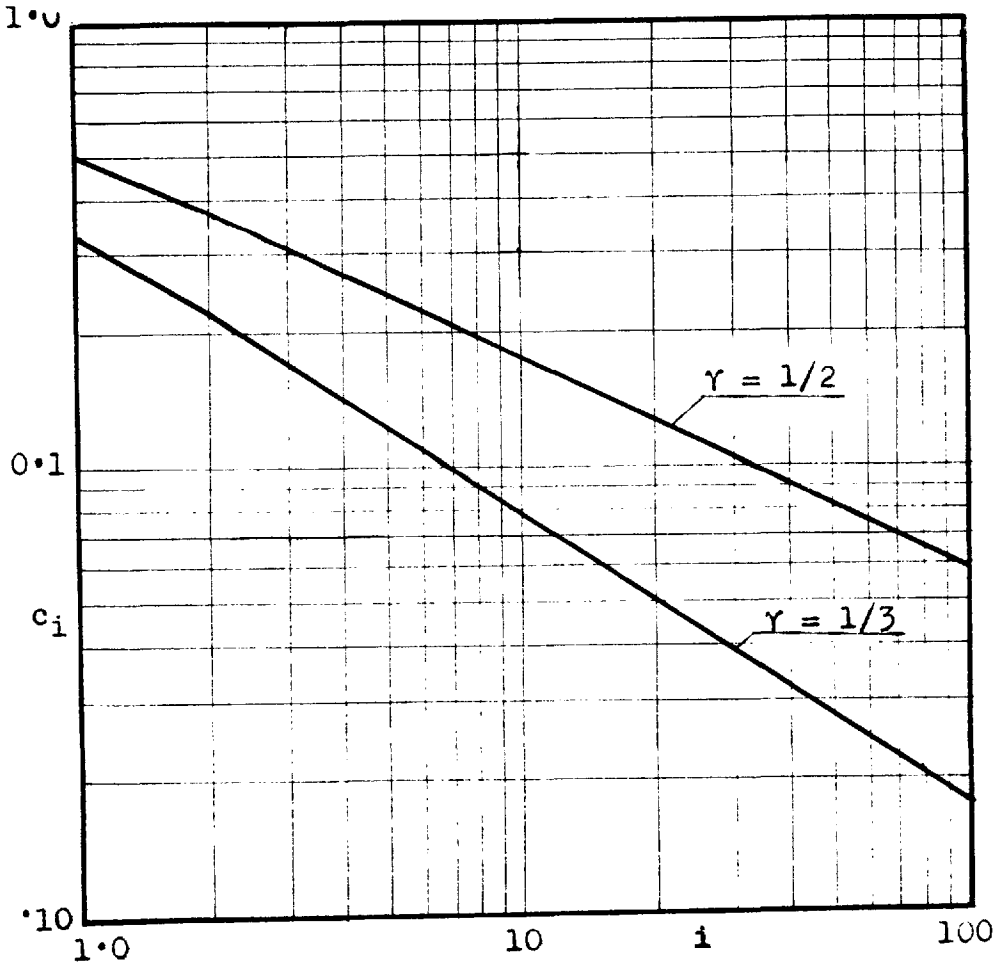


Fig.2.3 Taylor co-efficients, c_i, plotted versus i

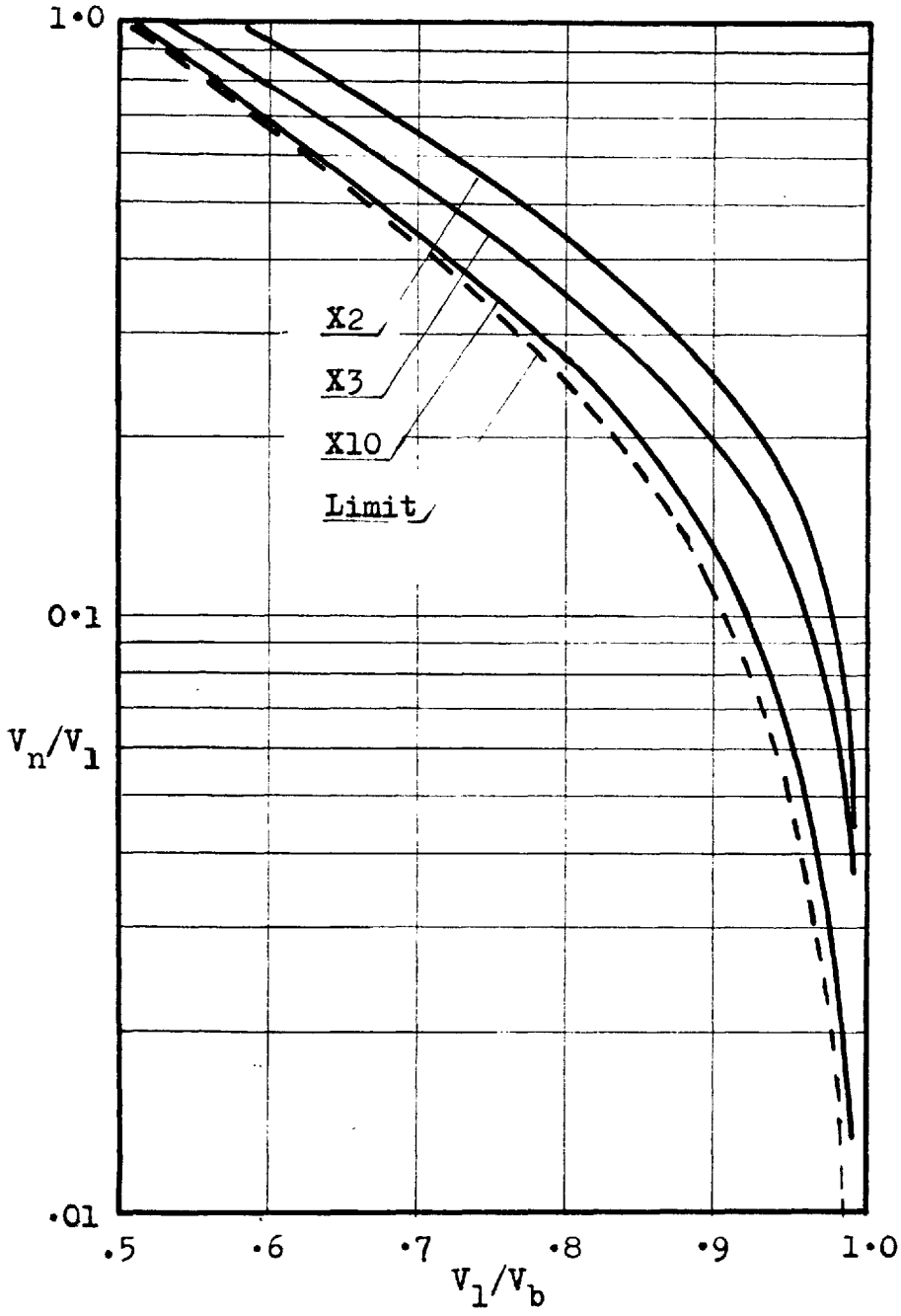


Fig.2.4 Relationship between voltage gain and input voltage for a node multiplier under optimized conditions using an ideal diode

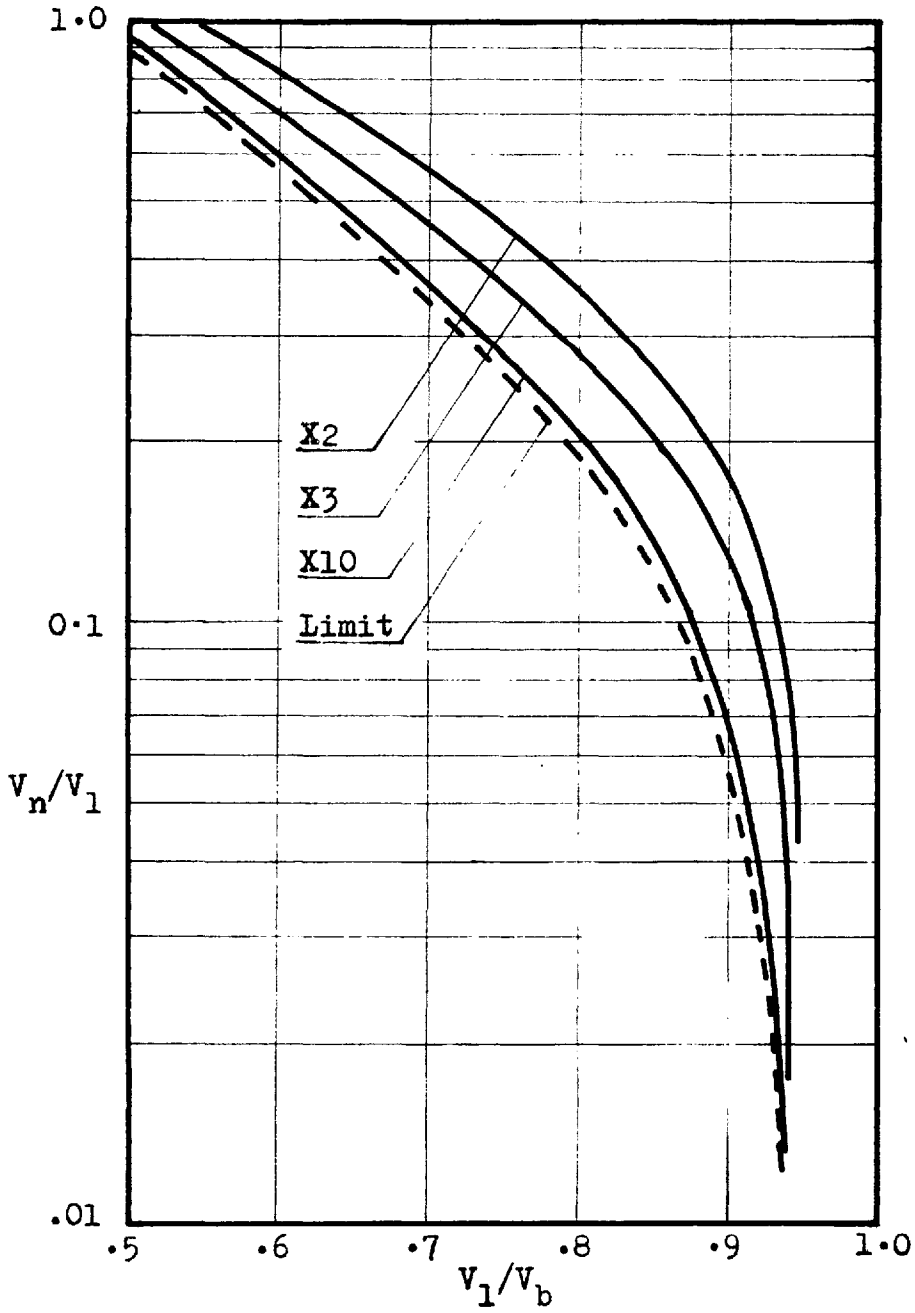


Fig.2.5 Relationship between voltage gain and input voltage for a node multiplier under optimized conditions using a diode where $V_b' = \cdot 95V_b$

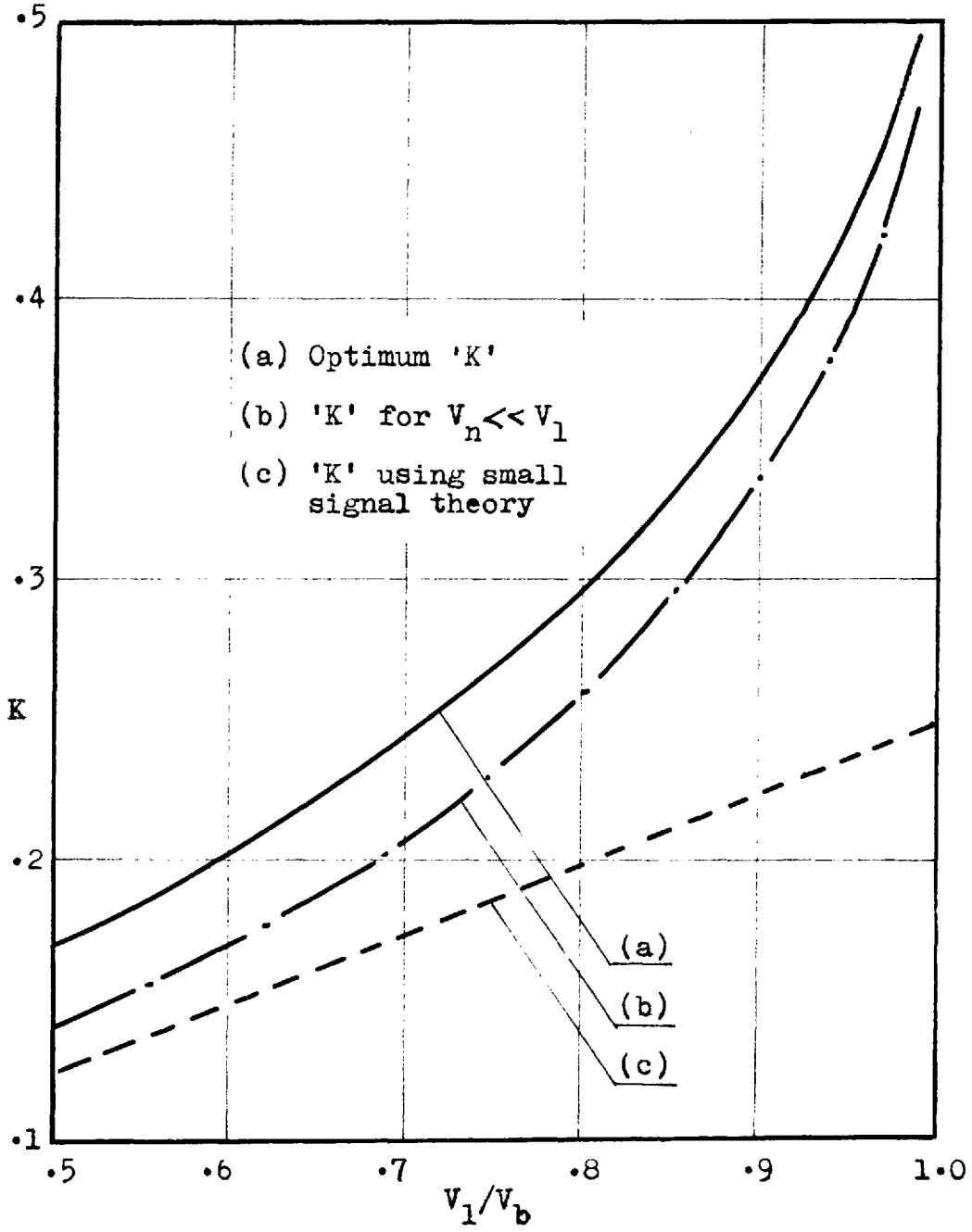


Fig.2.6 'K' curves for a X2 node multiplier, $\gamma = 1/2$.

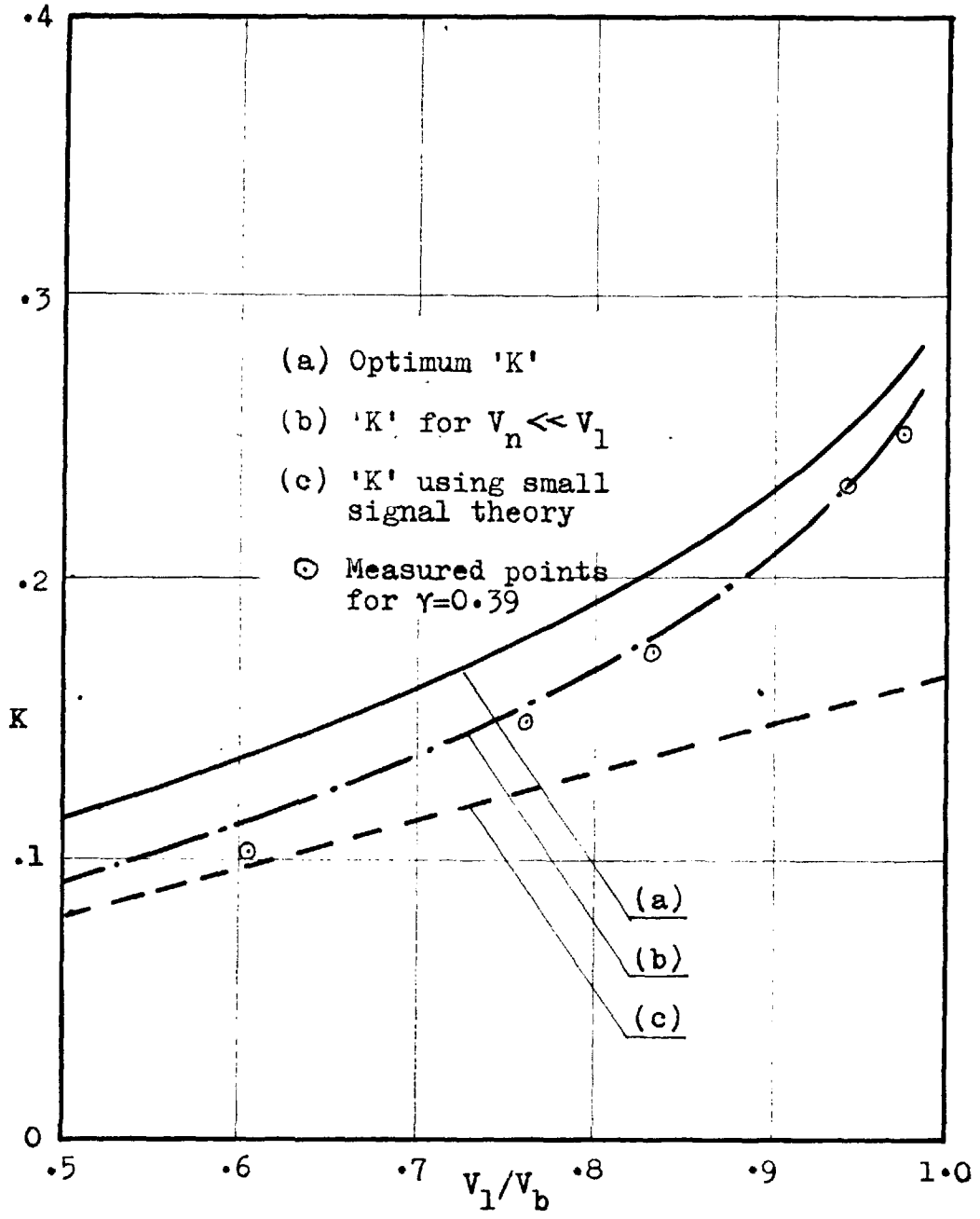


Fig.2.7 'K' curves for a X2 node multiplier, $\gamma = 1/3$.

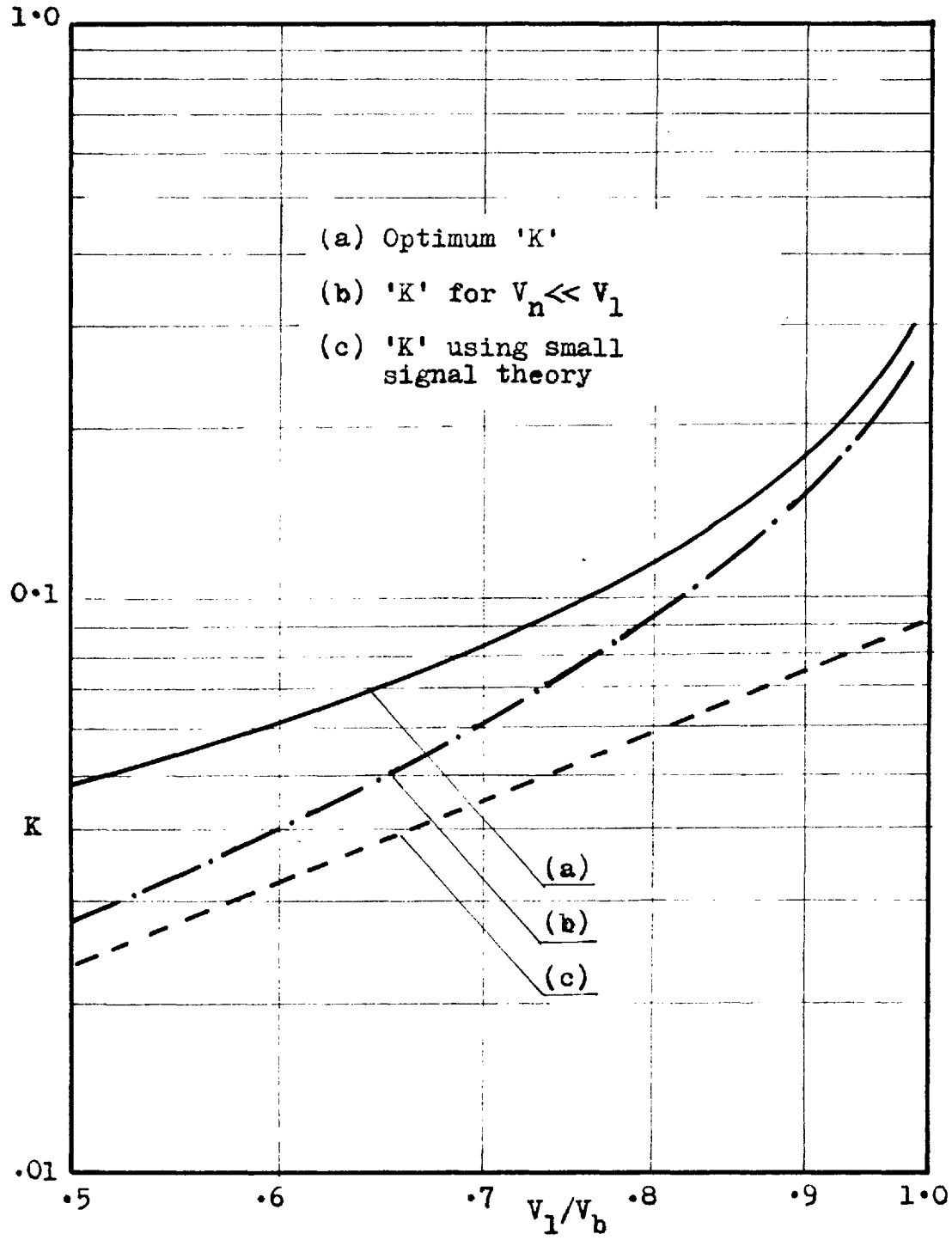


Fig.2.8 'K' curves for a X3 node multiplier, $\gamma = 1/2$.

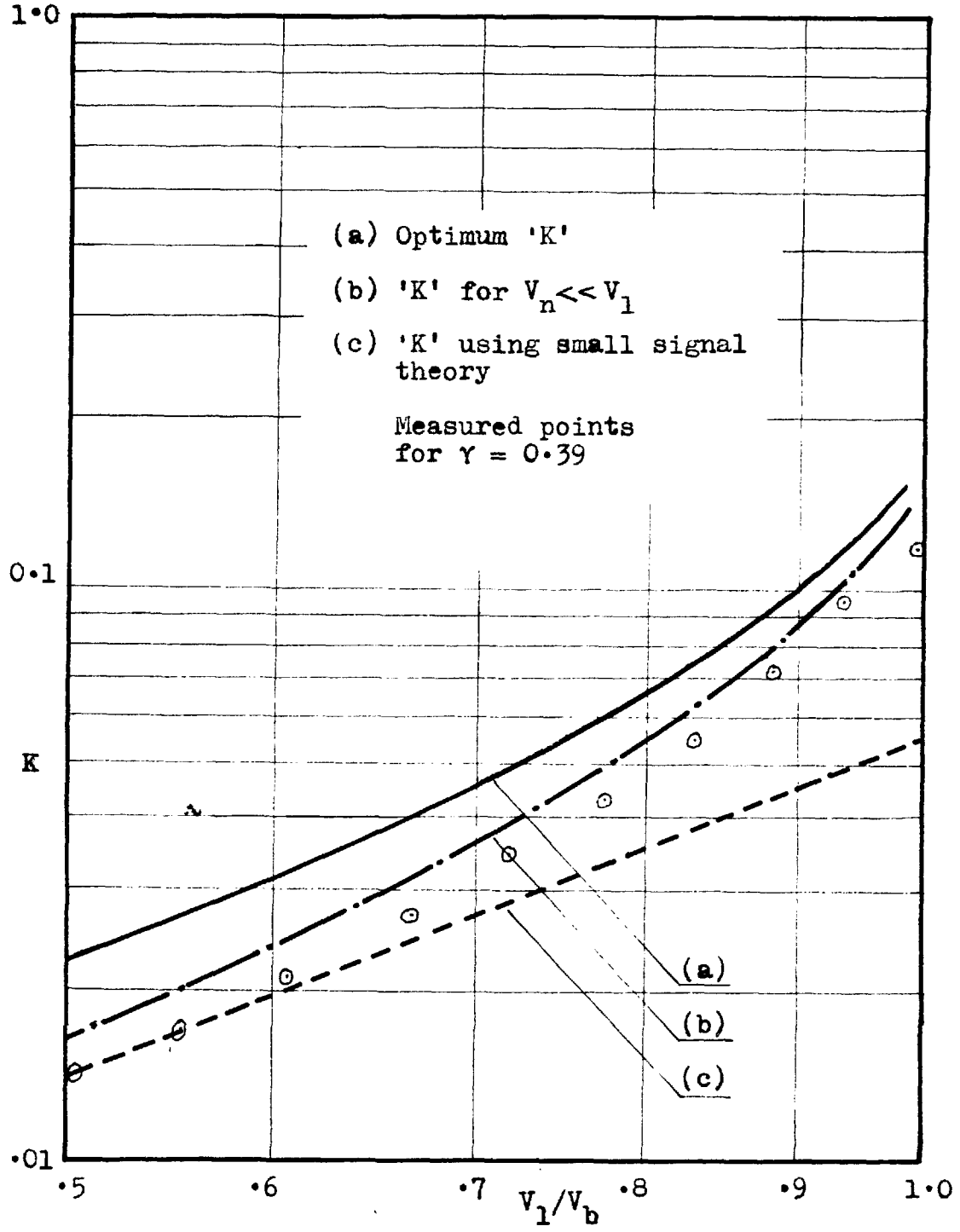


Fig.2.9 'K' curves for a X3 node multiplier, $\gamma = 1/3$.

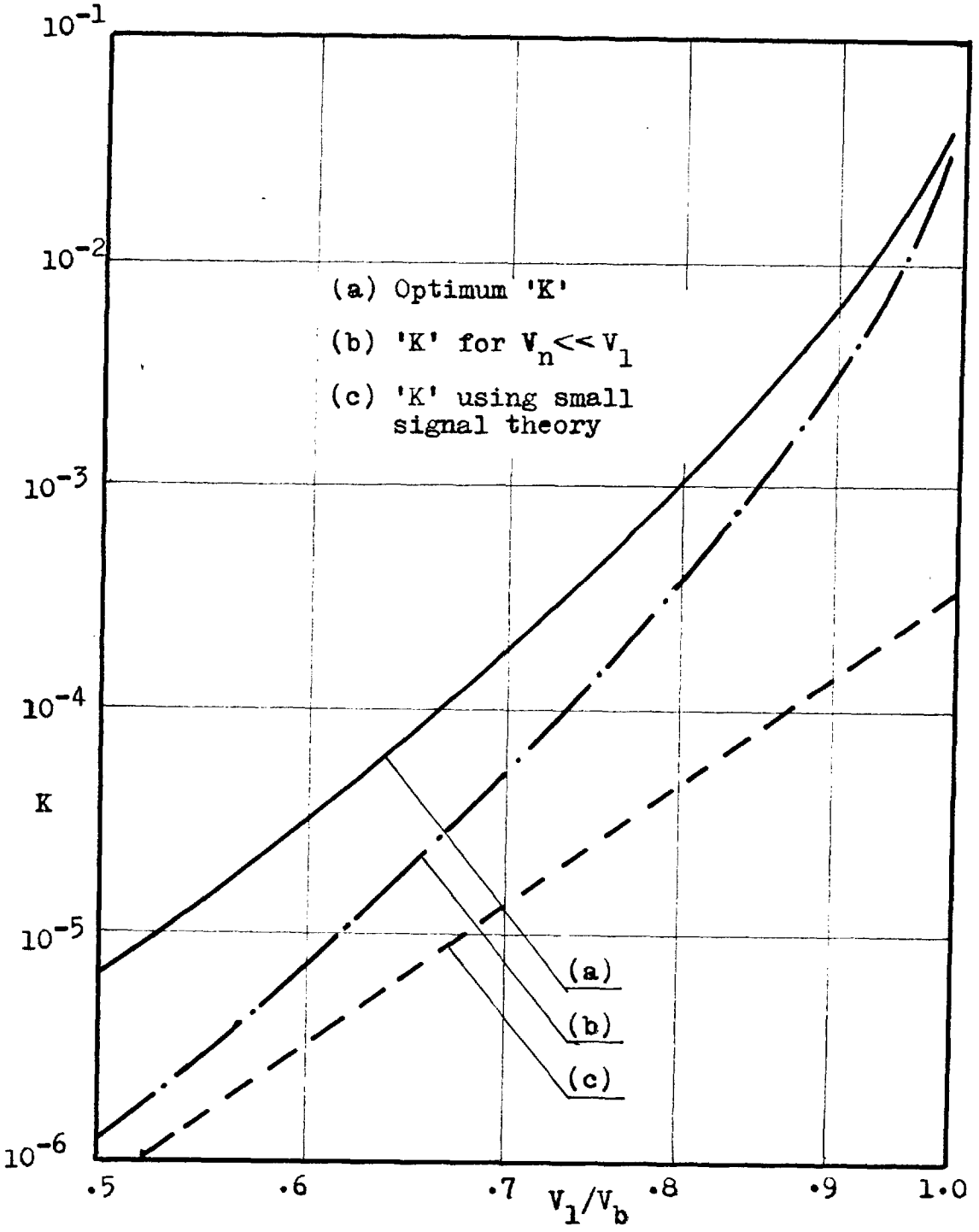


Fig.2.10 'K' curves for a X10 node multiplier, $\gamma = 1/2$.

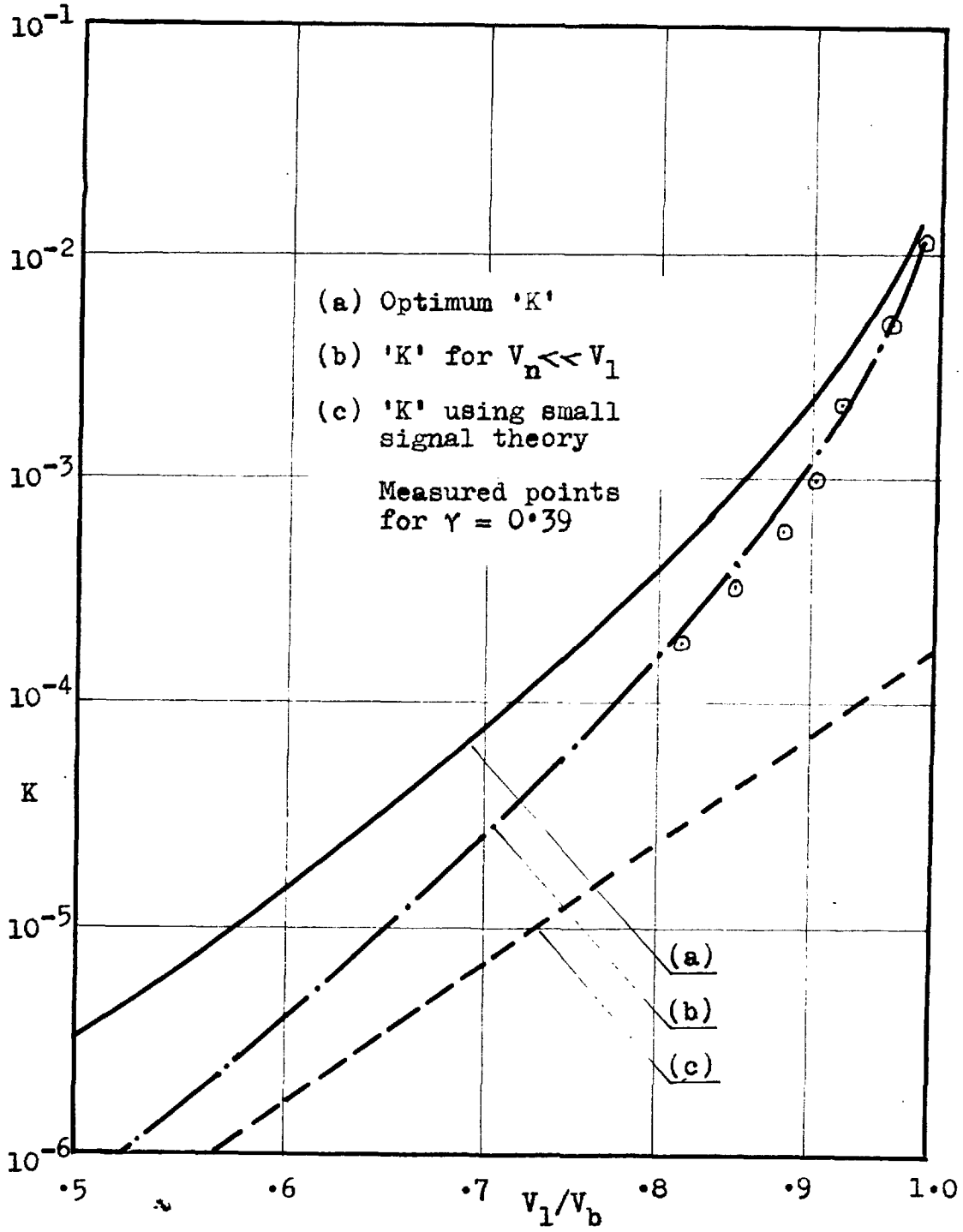


Fig.2.11 'K' curves for a X10 node multiplier, $\gamma = 1/3$.

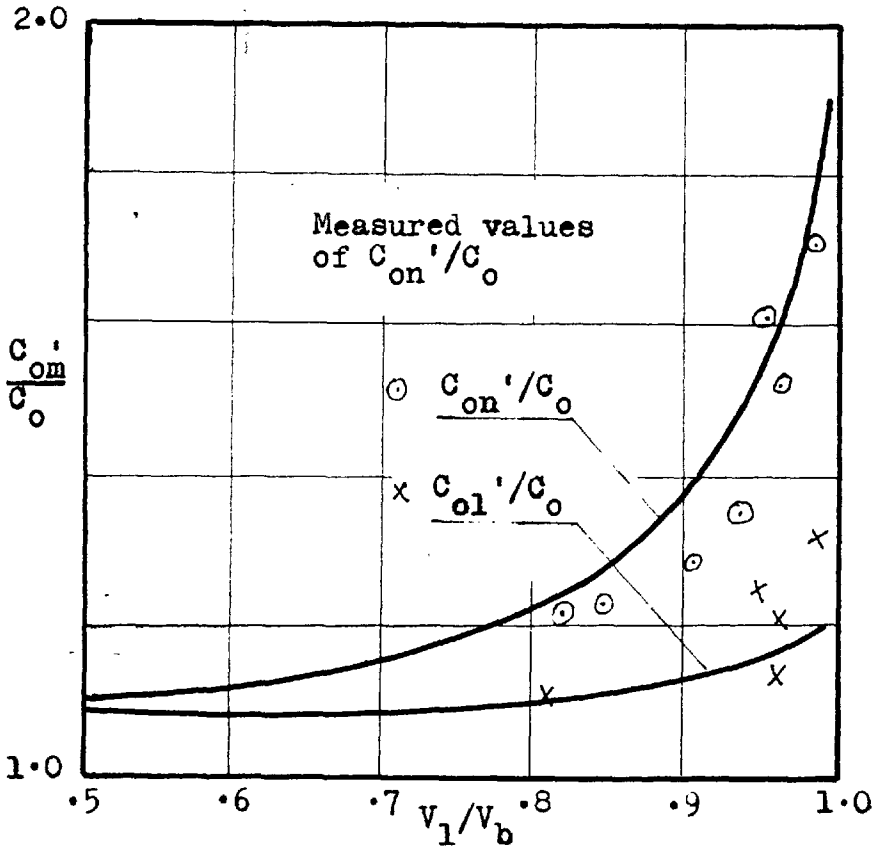


Fig.2.12 Variation of diode 'capacitance' with input voltage for a node multiplier.

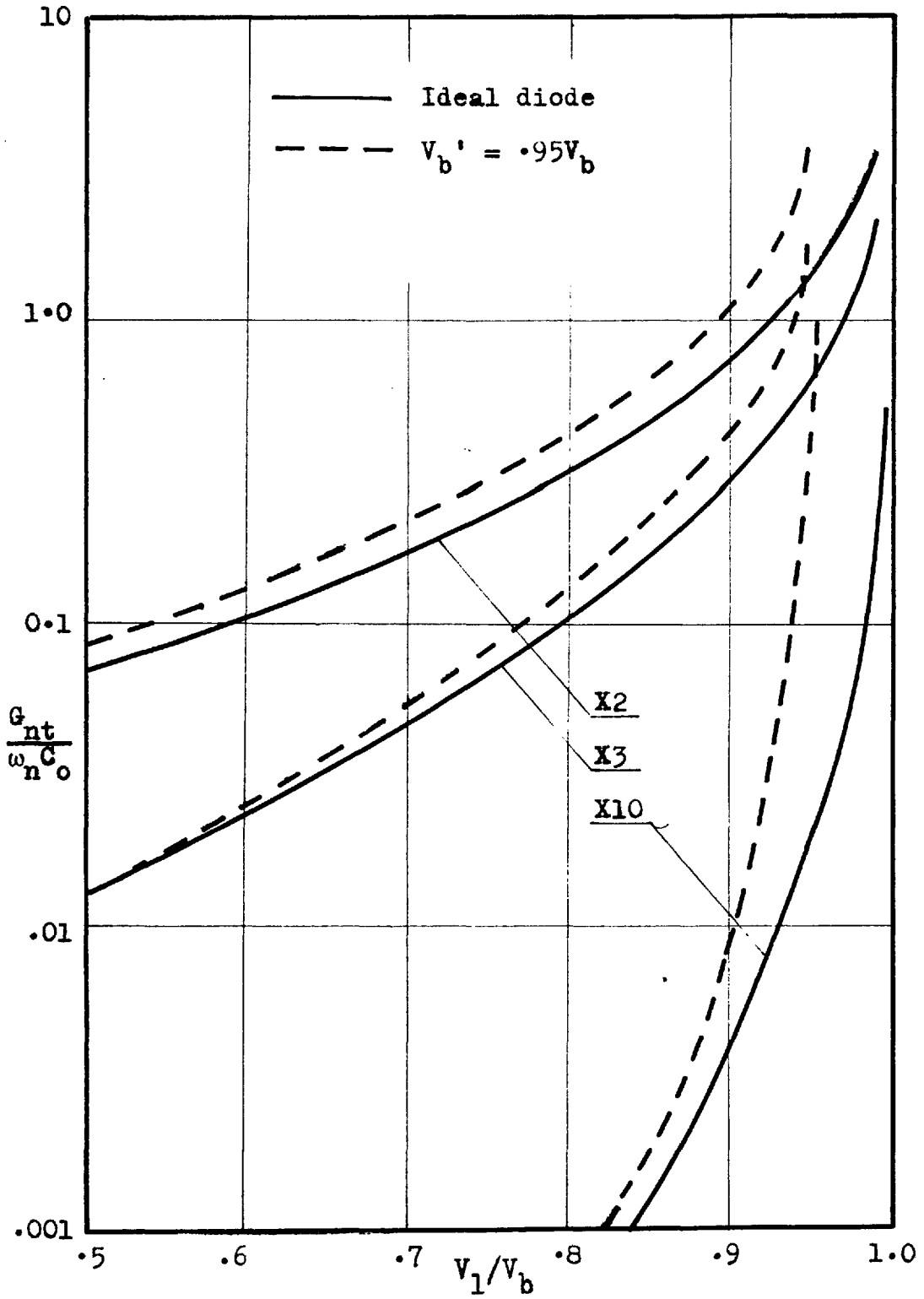


Fig.2.13 $G_{nt}/\omega_n C_o$ plotted versus V_1/V_b for optimized node multipliers where $\gamma = 1/2$.

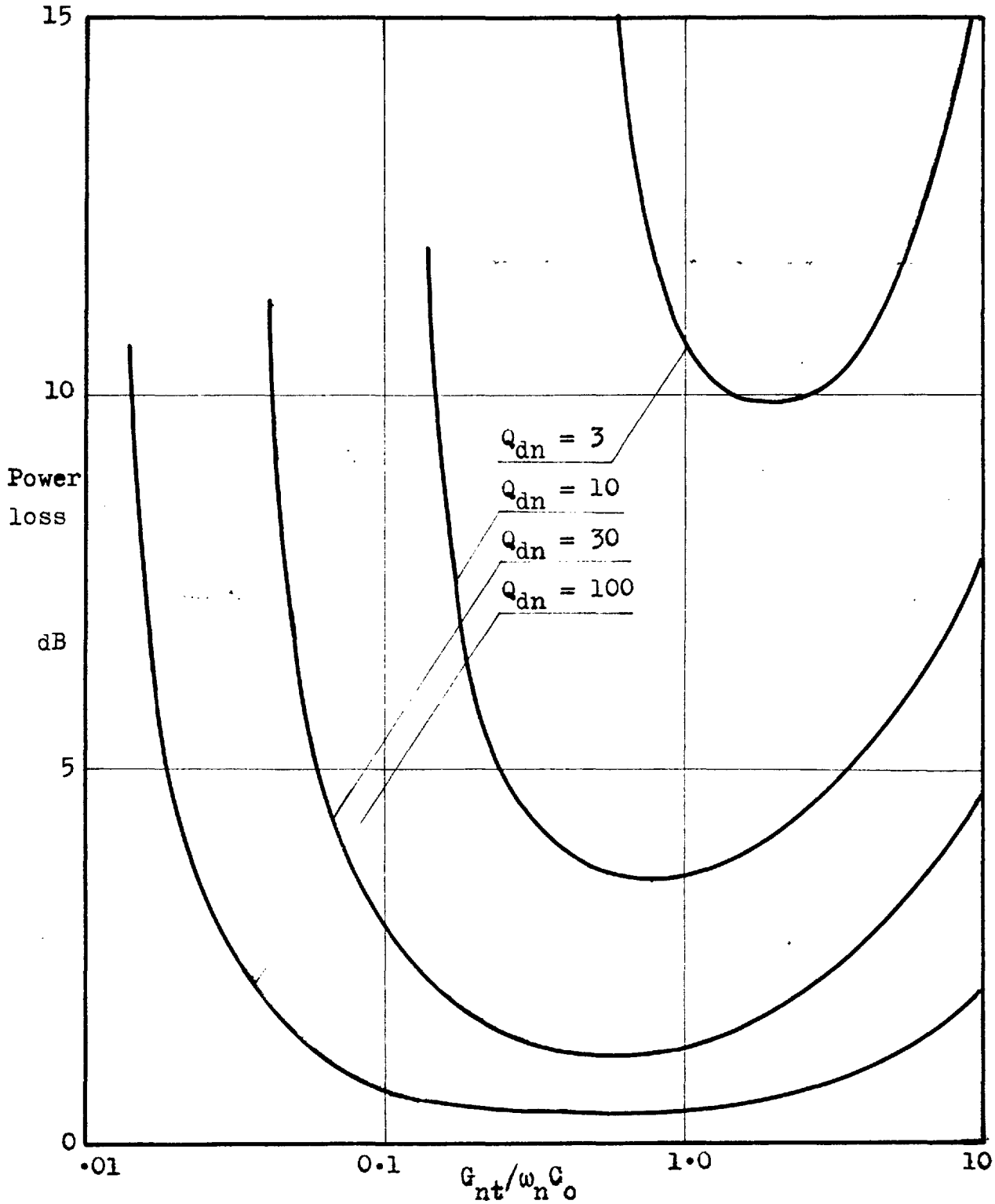


Fig.2.14 Power loss curves for a X2 node multiplier, $\gamma = 1/2$.

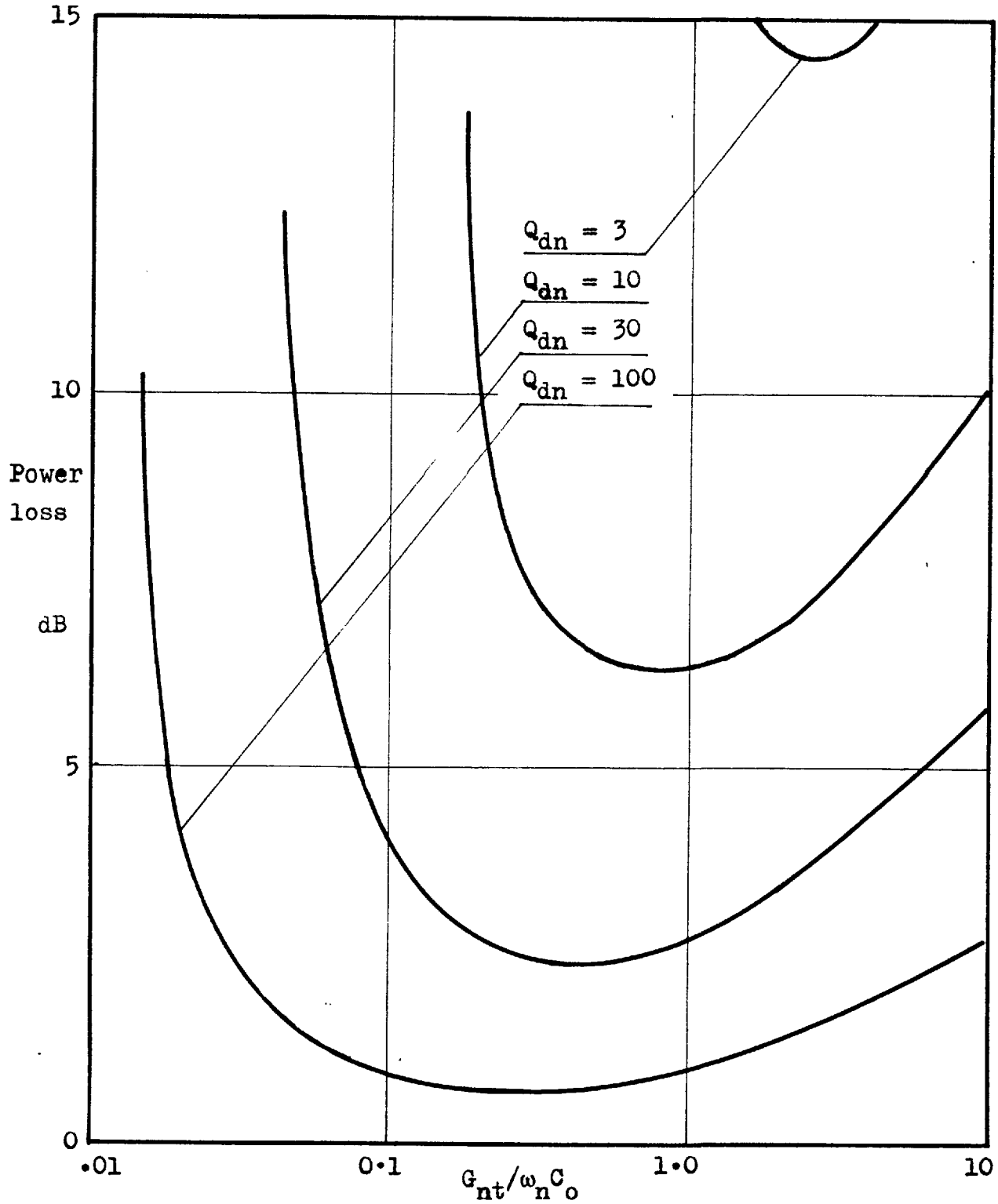


Fig.2.15 Power loss curves for a X3 node multiplier, $\gamma = 1/2$.

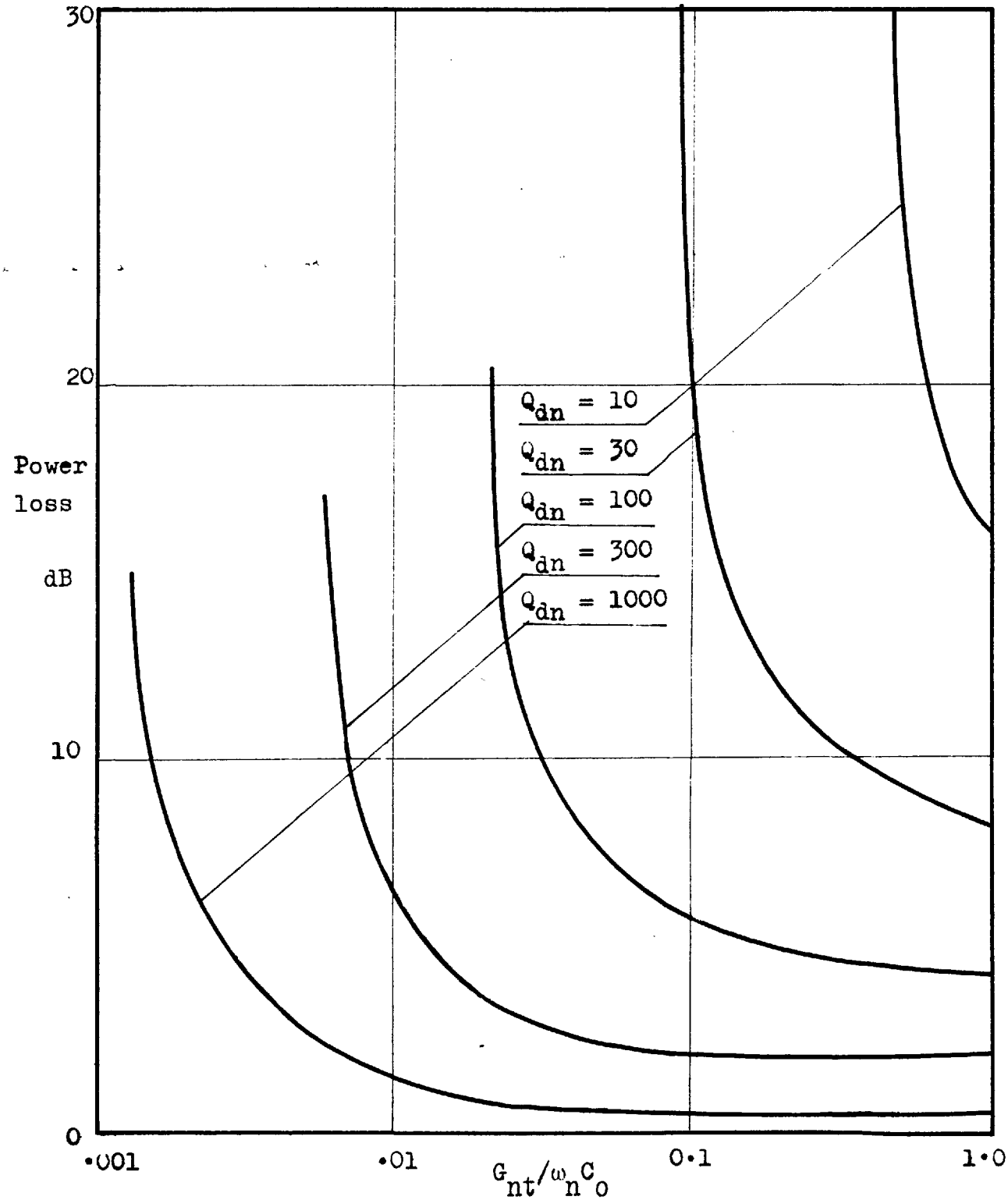


Fig.2.16 Power loss curves for a X10 node multiplier, $\gamma = 1/2$.

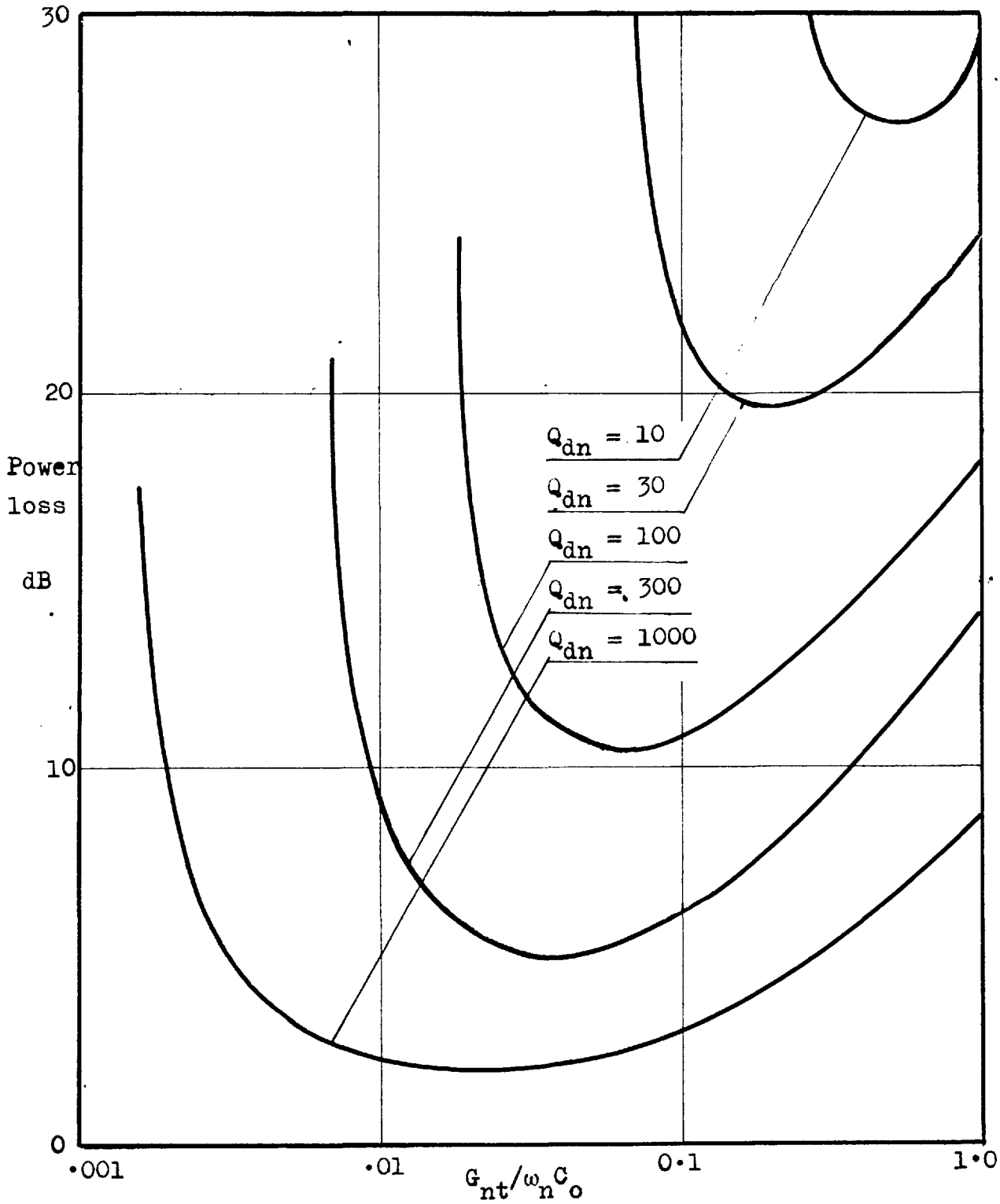


Fig.2.17 Power loss curves for a X10 node multiplier where $\gamma = 1/2$ and $V_b' = \cdot 95 V_b$.

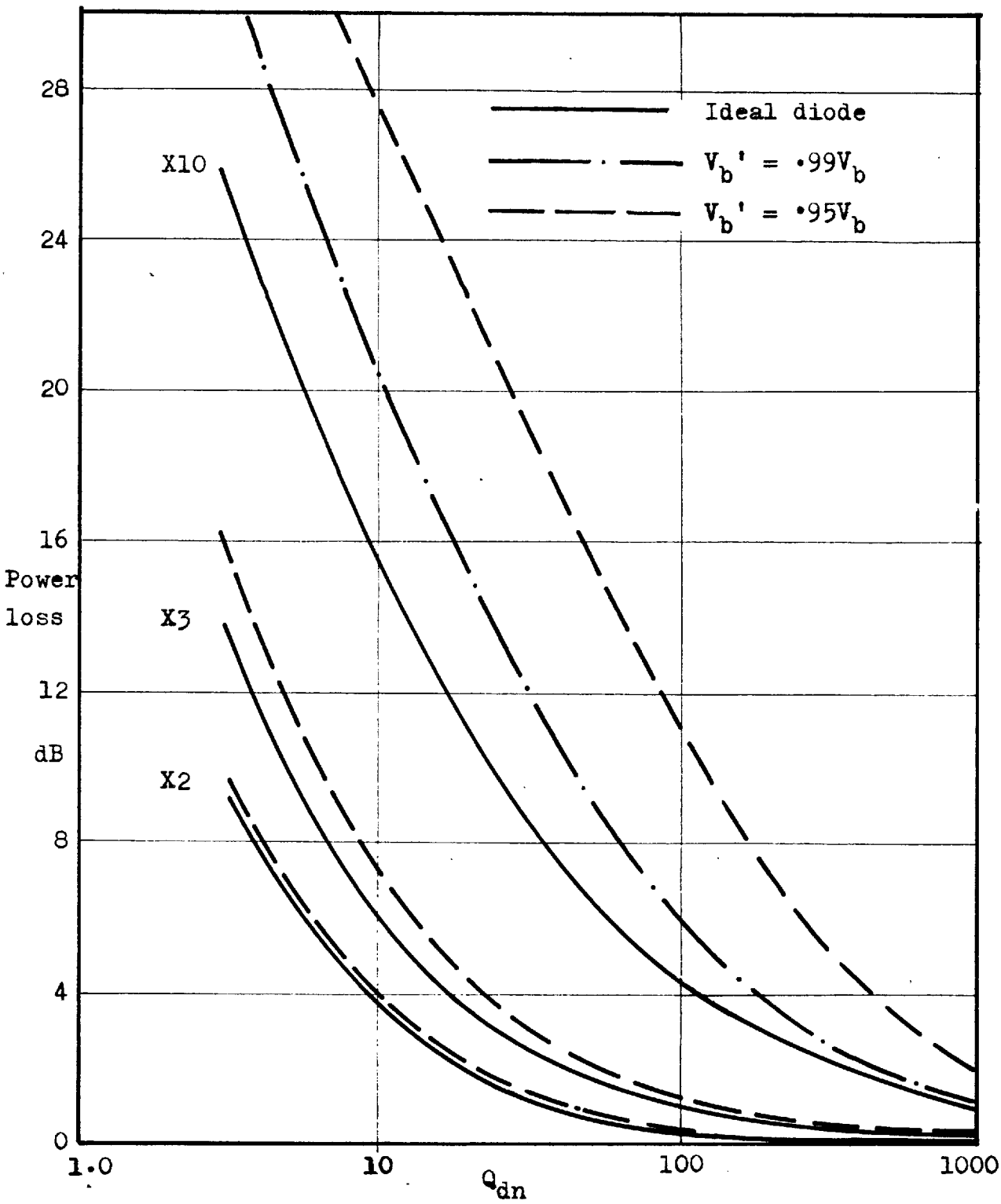


Fig.2.18 Minimum power loss versus diode 'Q' factor for various node multipliers.

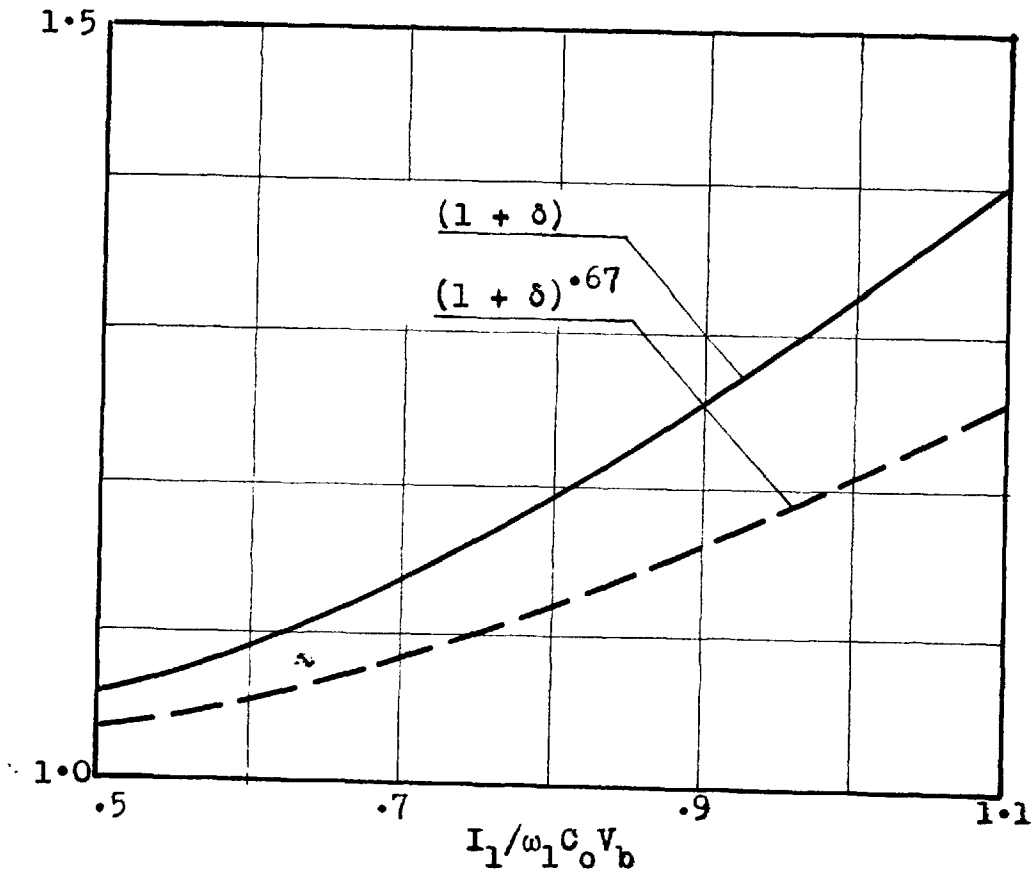


Fig.2.19 'δ' curves for a mesh multiplier.

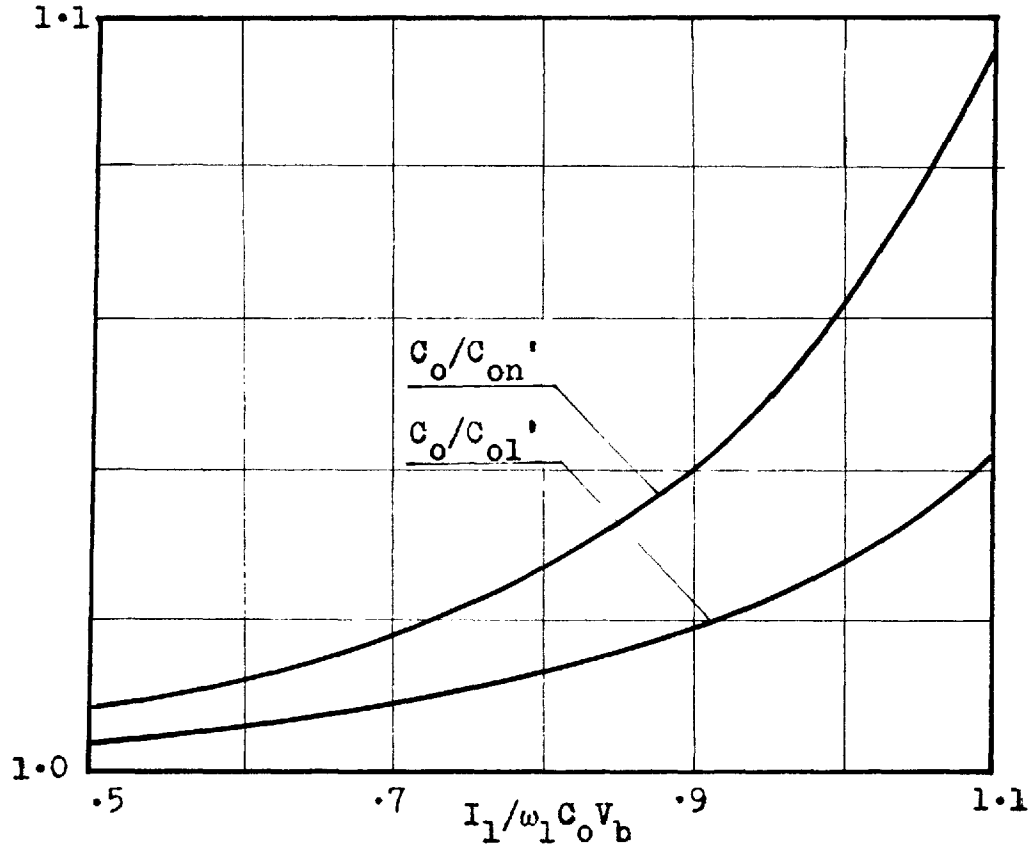


Fig.2.20 Variation of diode 'capacitance' with input current for a mesh multiplier.

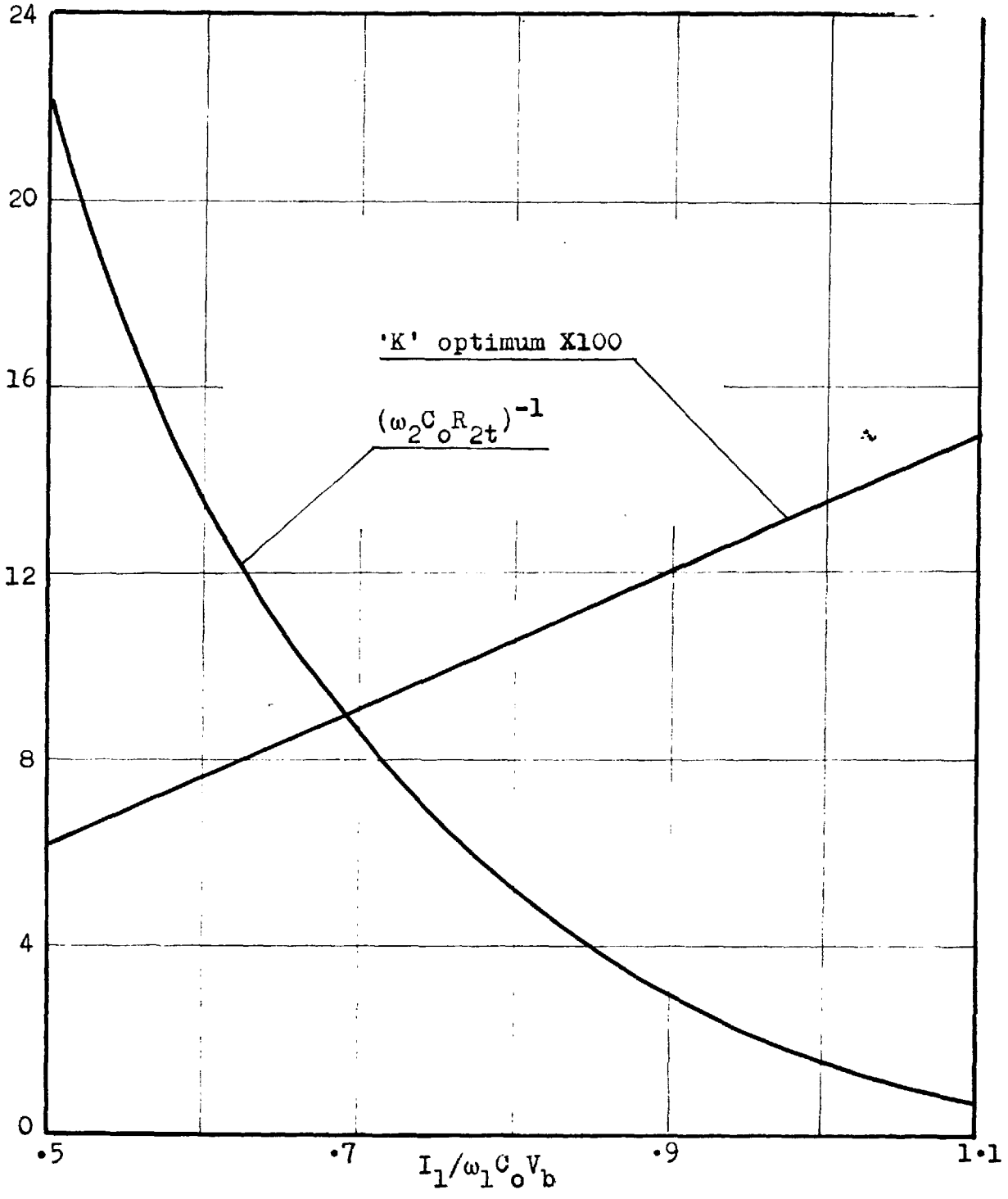


Fig.2.21 'K' and $(\omega_2 C_o R_{2t})^{-1}$ curves for a X2 mesh multiplier where $\gamma = 1/2$.

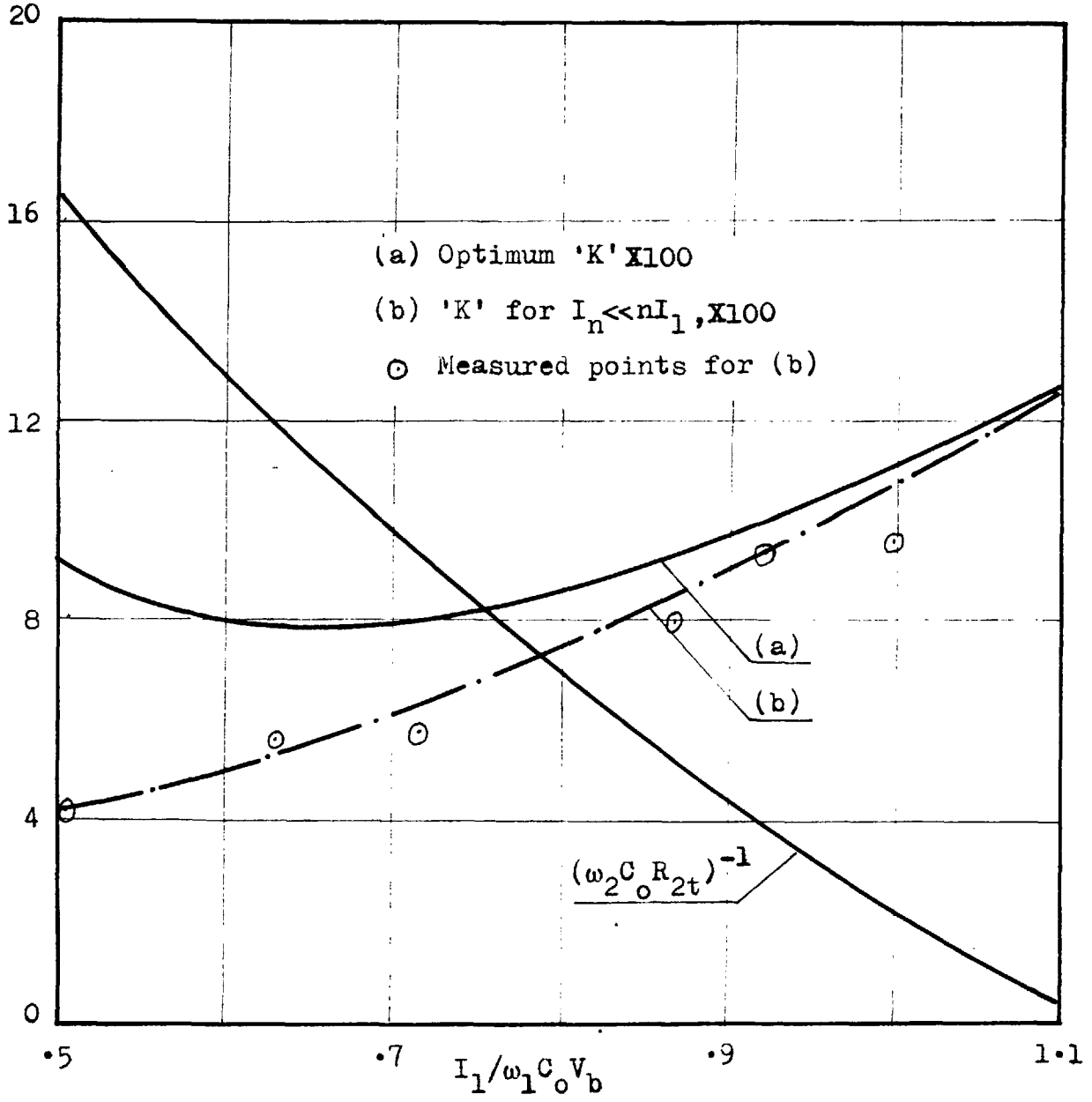


Fig.2.22 'K' and $(\omega_2 C_o R_{2t})^{-1}$ curves for a X2 mesh multiplier where $\gamma = 1/3$.

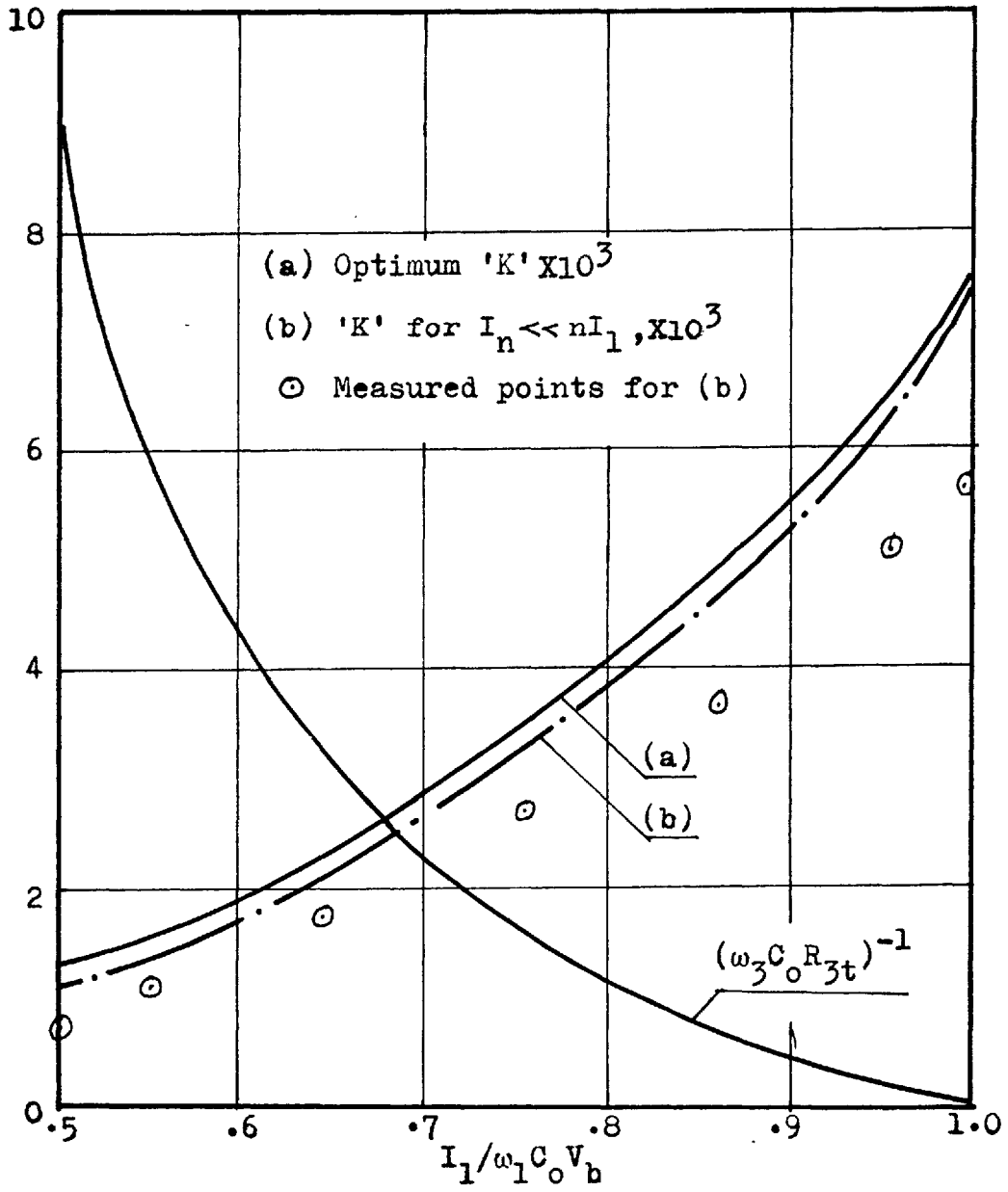


Fig.2.23 'K' and $(\omega_3 C_o R_{3t})^{-1}$ curves for a X3 mesh multiplier, $\gamma = 1/3$.

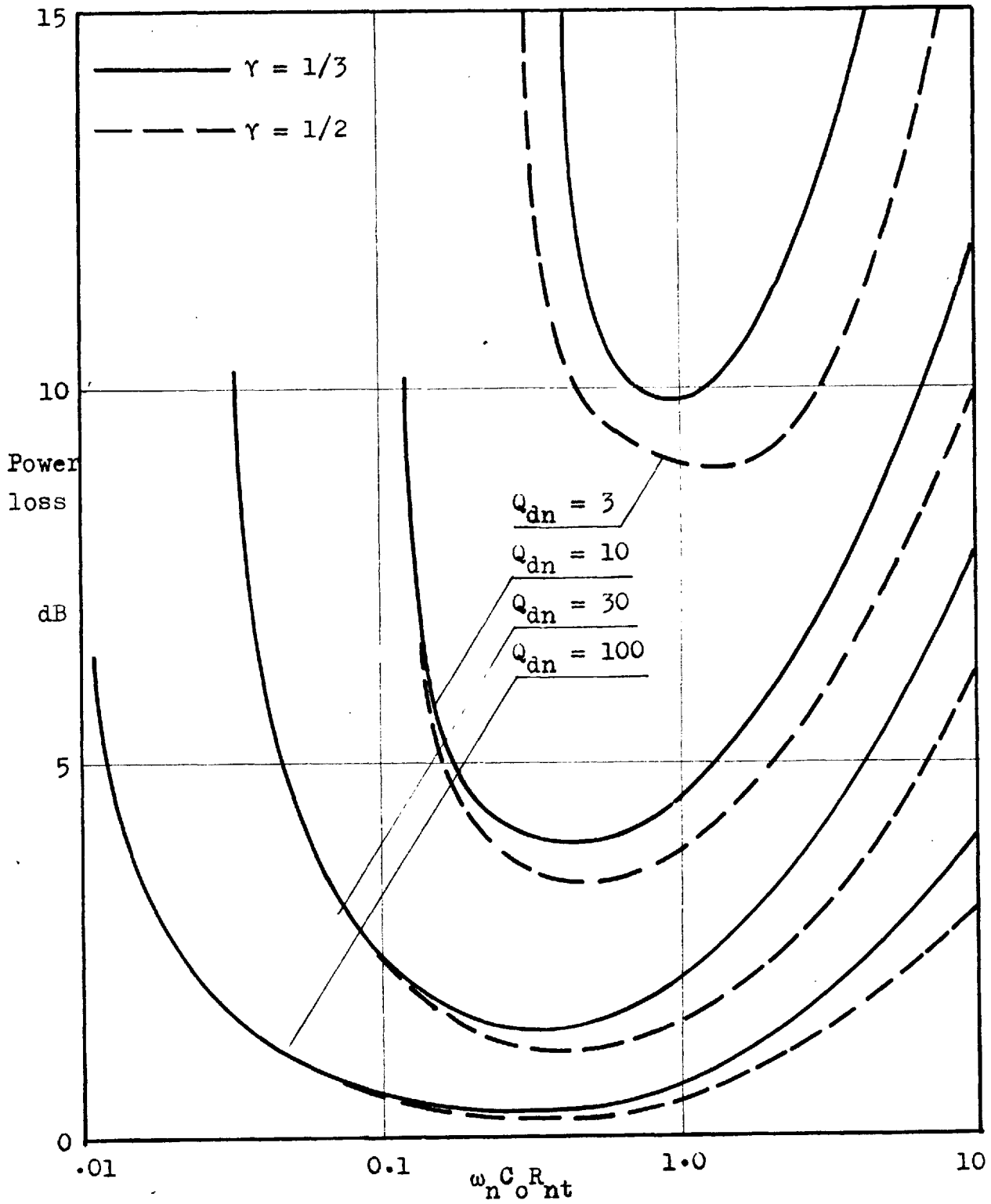


Fig.2.24 Power loss curves for a X2 mesh multiplier.

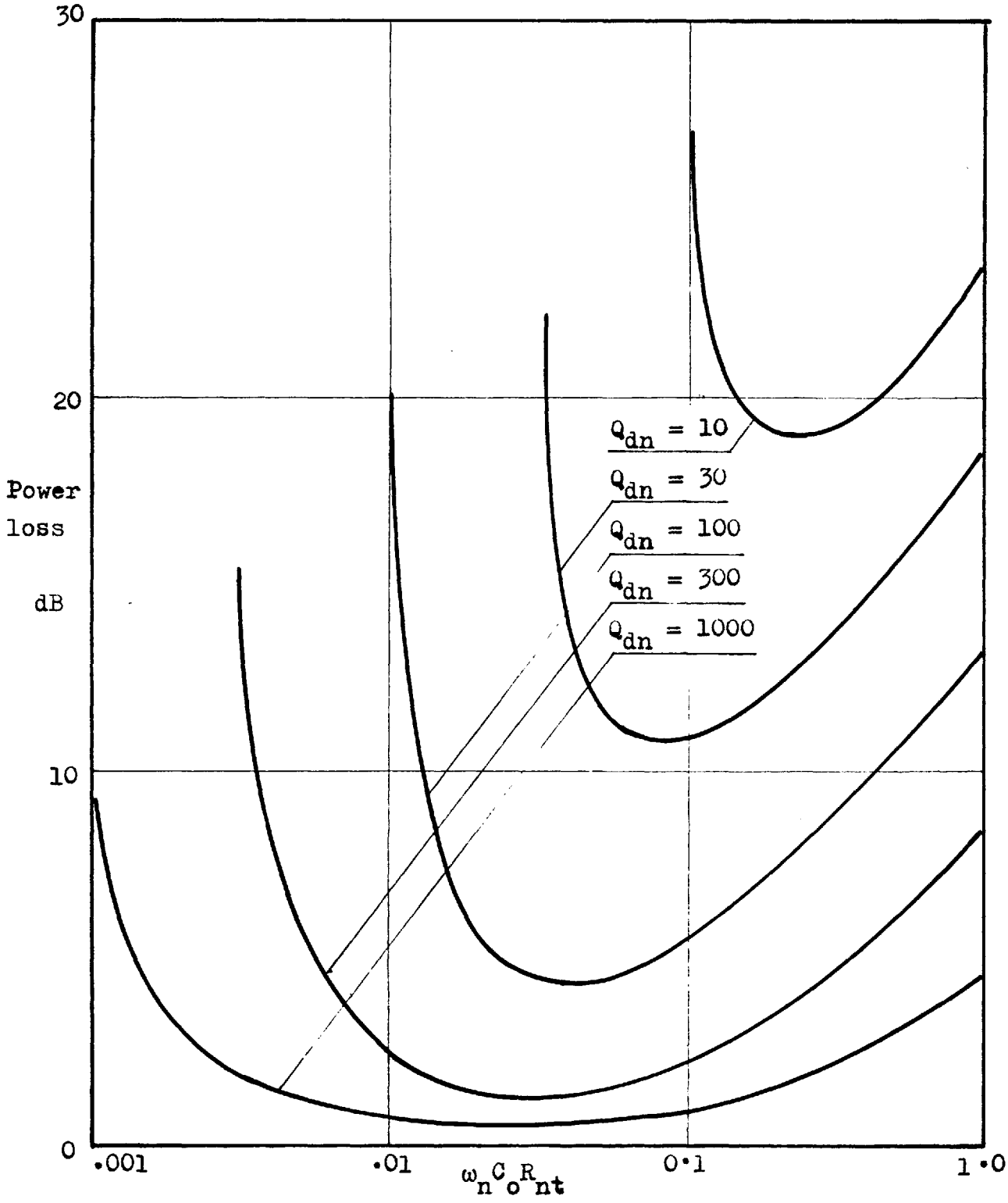


Fig.2.25 Power loss curves for a X3 mesh multiplier, $\gamma = 1/3$.

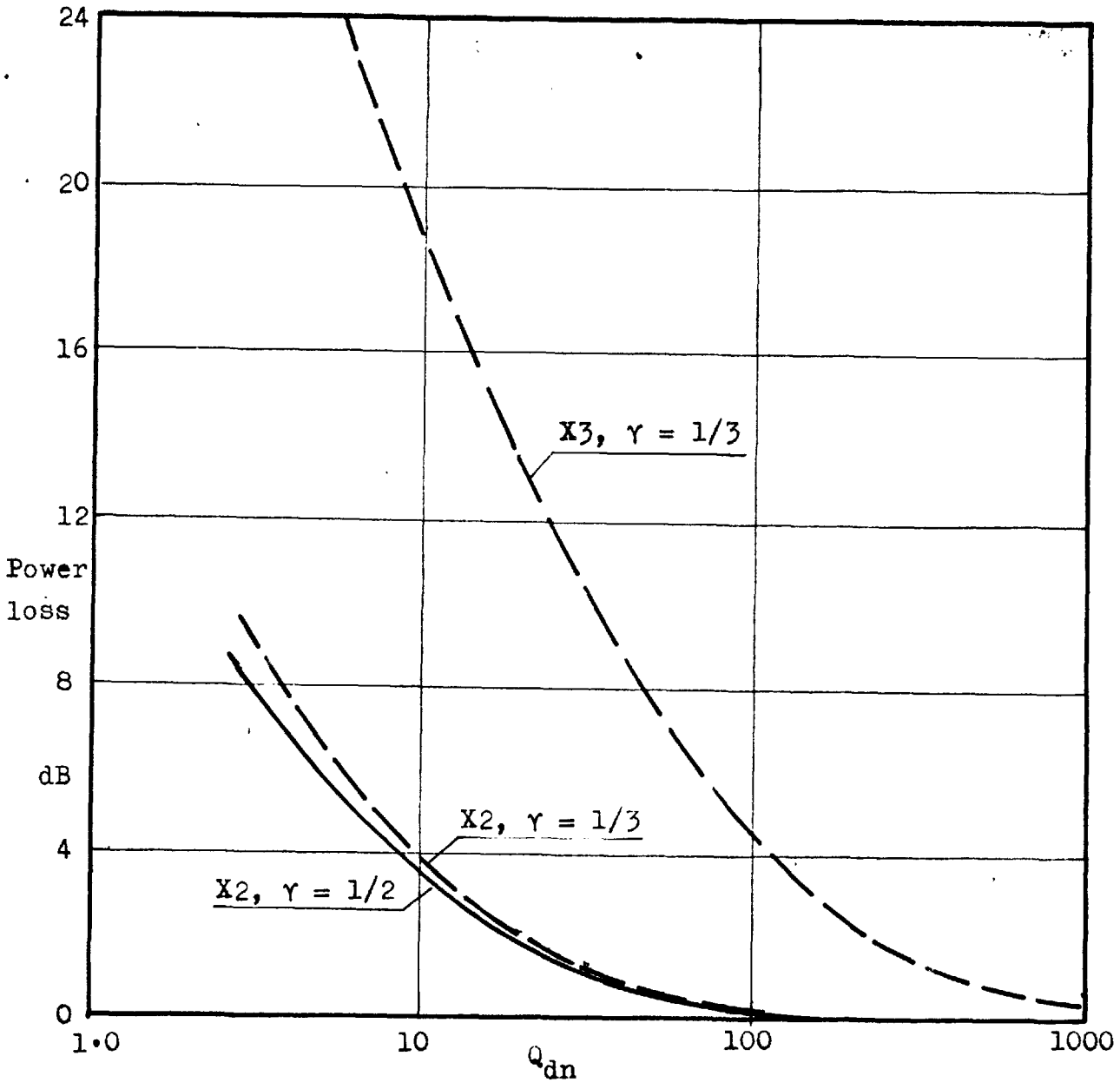
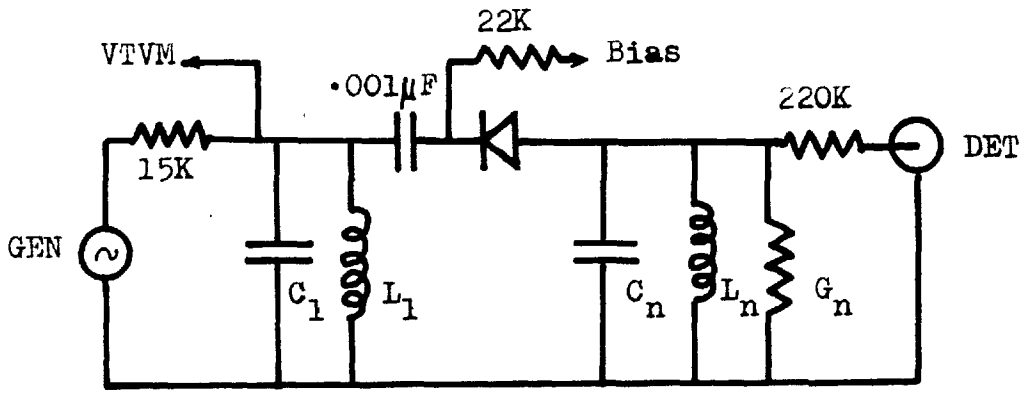


Fig.2.26 Minimum power loss versus diode 'Q' factor for various mesh multipliers.



Diode: G.E.C. SVC3

C_o (at 4·4V bias) = 6·2pf.

R_s = 6·0 ohm.

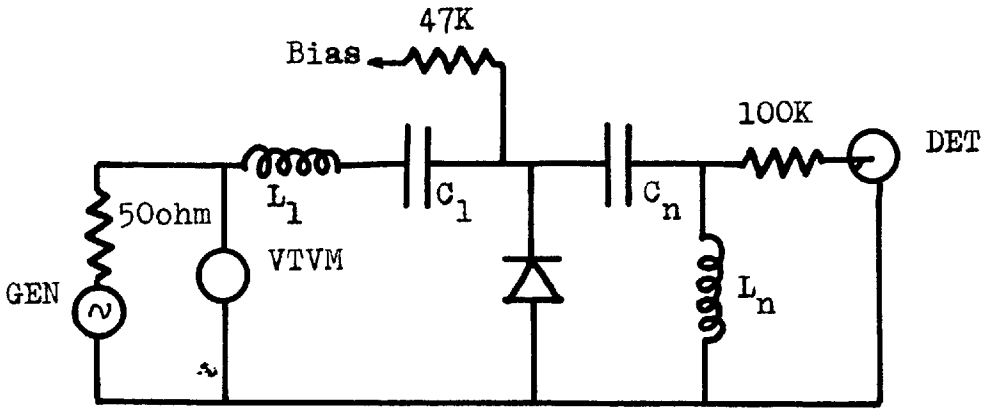
γ = 0·39

Circuit constants:

f_1 = 5·75Mc/s., C_{1t} = 110pf.

X2	C_{2t} = 295pf.,	Q_{2t} = 43,	$G_{2t}/\omega_2 C_o$ = 1·11,
X3	C_{3t} = 130pf.,	Q_{3t} = 26,	$G_{3t}/\omega_3 C_o$ = 0·73,
X10	C_{10t}= 110pf.,	Q_{10t}= 48,	$G_{10t}/\omega_{10} C_o$= 0·37.

Fig.2.27 Experimental node circuit.



Diode: 8X G.E.C. SVC3 in parallel operating at zero volts applied bias.

C_o = 115pf.,

R_s = 0·55 ohm

γ = 0·33.

Circuit constants:

X2 circuit: f_1 = 50Mc/s., C_{1t} = 10pf., C_{2t} = 10pf., Q_{2t} = 13·5,

X3 circuit: f_1 = 50Mc/s., C_{1t} = 10pf., C_{3t} = 5·3pf., Q_{3t} = 42,

X10 circuit: f_1 = 18Mc/s., C_{1t} = 10pf., C_{10t} = 11pf., Q_{10t} = 91.

Fig.2.28 Experimental mesh circuit.

Appendix 2.1 Derivation of the series for 'K'.

Appendix 2.1.1. Node circuit.

We wish to obtain the terms of (2.18) leading to current in phase with the I_{dn} component of (2.9). Consider the mth term of the general series and substitute for v from (2.17).

$$i=C_o c_m\left[V_1 \sin \omega_1 t - V_n \sin n(\omega_1 t+\frac{\pi}{2})\right]^m \left[\omega_1 V_1 \cos\omega_1 t - \omega_n V_n \cos(\omega_n t + n\frac{\pi}{2})\right]$$

The terms leading to current at $\omega_n t$ are given by terms in v^m of frequency, 0, $2n\omega_1 t$, $(n-1)\omega_1 t$, $(n+1)\omega_1 t$ and it is only the last two that contribute to current in phase with I_{dn} (this can be checked by inspection): Thus the required terms are:

$$i = (\omega_1 C_o V_1) c_m V_{d1}^m \left\{A_{n-1}\cos\overline{n\theta-(n-1)\frac{\pi}{2}} + A_{n+1}\cos\overline{n\theta-(n+1)\frac{\pi}{2}}\right\}$$

(obtained by using the fact that $\sin^m\theta = \sum_{i=0}^{m}{}' A_i \cos i(\theta - \frac{\pi}{2})$

Putting $c_m = |c_m|\ (-1)^m$, (see (2.7)), gives:

$$i = (\omega_1 C_o V_1)\,|c_m|\,V_{d1}{}^m (-1)^m \left|{}^m\triangle_{n-1}^{n+1}\right| \cos\overline{n\theta - (n+1)\pi/2}$$

$$= (\omega_1 C_o V_1)\,|c_m|\,V_{d1}{}^m \left|{}^m\triangle_{n-1}^{n+1}\right| \sin n(\theta+\pi/2)$$

which is in phase with the I_{dn} component of (2.9).

Thus B(m) in (2.21) is obtained:

$$B(m) = \frac{1}{2}\left|{}^m\triangle_{n+1}^{n-1}\right|\ |c_m|\ V_{d1}{}^m$$

which is the result given in (2.22).

The method for determining D(m) is similar but instead of

taking terms of v^m, terms of v^{m-1} and v^{m-2} must be combined with $\frac{dv}{dt}$.

Appendix 2.1.2. Mesh circuit.

In this case we wish to obtain the terms of (2.32) leading to voltage in phase with that defined by (2.41) and (2.46). This is obtained simply from the mth term of (2.32) thus:

$$v_d = \left\{\frac{Q_o(1-\gamma)}{C_o V_b}\right\}^{\frac{1}{1-\gamma}} \left[\frac{I_1}{\omega_1 Q_o}\right]^m |L_m| \left\{\cos\omega_1 t + (I_n/nI_1)\sin n\omega_1 t\right\}^m$$

gives; for the term containing $I_1{}^m$:

$$V_n = V_b \left\{\frac{Q_o(1-\gamma)}{C_o V_b}\right\}^{\frac{1}{1-\gamma}} \left[\frac{I_1}{\omega_1 Q_n}\right]^m |L_m|^m A_n$$

whence:

$$'K'_m = \frac{1-\gamma}{(1+\delta)^\gamma} |L_m| \left[\frac{I_1}{\omega_1 Q_o}\right]^{m-1} {}^m A_n$$

This is the result given in (2.47).

The second part is obtained in a similar manner.

Appendix 2.2. Convergence of series involved in the large signal analysis.

Appendix 2.2.1. Node circuit.

(2.22) may be written thus:

$$C_m V_{d1}^m \left| {}^m\Delta_{n+1}^{n-i} \right| = \frac{c_m \cdot \lfloor m \cdot n \cdot (V_{d1})^m}{2^{m-2} \cdot (m+n+1) \cdot \lfloor (m+n+1)/2 \cdot \lfloor (m-n+1)/2}$$

The ratio of successive terms is thus:

$$r = \frac{c_m}{c_{m+2}} \left[1 + \frac{n-1}{m+2}\right]\left[1 + \frac{2}{m+n+1}\right]\left[1 - \frac{n-2}{m+1}\right](V_{d1})^{-2}$$

Since the Taylor co-efficients are as given by (2.7) it follows that:

$$\frac{c_m}{c_{m+2}} = \left[1 - \gamma/(\gamma+m+1)\right]\left[1 + (2-\gamma)/(\gamma+m)\right]$$

$$\approx 1 + 2(1-\gamma)/m, \quad \text{for} \quad n \gg 1.$$

Hence r becomes:

$$\left[1 + \frac{n-1}{m+2}\right]\left[1 + \frac{2}{m+n+1}\right]\left[1 - \frac{n-2}{m+1}\right]\left[1 - \frac{\gamma}{\gamma+m+1}\right]\left[1 + \frac{2-\gamma}{m+\gamma}\right](V_{d1})^{-2}$$

which simplifies to :

$$r = \left[1 + 2\frac{1-\gamma}{m} + \frac{2}{m+n} - \left(\frac{n}{m}\right)^2\right]\left[(V_{d1})\right]^{-2}$$

for $m \gg n > 1$

Thus r is greater than unity when,

$$\left[2\frac{1-\gamma}{m} + \frac{2}{m+n} - \left(\frac{n}{m}\right)^2\right] > \left[(V_{d1})\right]^{-2} - 1$$

which is the result used in (2.54).

Similarly (2.23) may be written thus:

$$D(m) = \frac{n \cdot \lfloor m-1 \cdot m \cdot c_m \cdot (V_{d1})^m \cdot (V_n/V_1)^2}{2^{m-2} \cdot \lfloor (m-n-1)/2 \cdot \lfloor (m+n-3)/2 \cdot (m+n-1) \cdot 4}$$

and the ratio of successive terms becomes:

$$r = \left[1 + \frac{1+m}{m}\right]\left[1 - \frac{n}{m+1}\right]\left[1 - \frac{2}{m+2}\right]\left[1 + 2\,\frac{1-\gamma}{m}\right] (V_{d1})^{-2}$$

which simplifies to :

$$r = \left[1 - \left(\frac{n}{m}\right)^2 - 2\,\frac{\gamma}{m}\right] (V_{d1})^{-2} \quad , \quad \text{for } m \gg n > 1$$

Hence, for $r > 1$ we obtain the result:

$$\left[1 - 2\,\gamma/m\right] > (V_{d1})^2 \quad \text{neglecting} \quad \left(\frac{n}{m}\right)^2$$

This is the result used in (2.57).

Appendix 2.2.2. Mesh Circuit.

Consider the ratio of successive terms of (2.47) where $I_n \ll nI_1$.

$$r = \frac{L_m}{L_{m+2}} \left[\frac{I_1}{\omega_1 Q_o}\right]^{-2} \left[1 + \frac{m+2-m^2}{m^2+3m+2}\right]$$

L_m is defined by (2.34) and hence

$$\frac{L_m}{L_{m+2}} = \left[1 + \frac{\gamma'+2}{m-\gamma'}\right]\left[1 - \frac{\gamma'}{m+\gamma'+1}\right]$$

$$\approx 1 + 2/m \quad , \text{ for } m \gg \gamma'$$

Hence

$$r = \left[1 + \frac{2}{m} + \frac{m+2-m^2}{m^2}\right]\left[\frac{I_1}{\omega_1 Q_o}\right]^{-2}$$

which converges when $m > (n^2-2)/3$ irrespective of the value of $I_1/\omega_1 Q_o$. This condition gives (2.59).

The ratio of successive terms for the second factor of (2.47) is:

$$r = \left[1 - \frac{2}{m}\right]\left[1 + \frac{m-n^2}{m^2-m}\right]\left[\frac{I_1}{\omega_1 Q_o}\right]^{-2}, \text{ for } m \gg n > 1.$$

$$\approx \left[1 - \frac{m+n^2}{m^2}\right]\left[\frac{I_1}{\omega_1 Q_o}\right]^{-2}$$

It follows that for $r > 1$,

$$(m + n^2)/m^2 < 1 - (I_1/\omega_1 Q_o)^2$$

which is the condition stated in (2.60).

SECTION 3

CONSIDERATION OF CHARGE STORAGE EFFECTS.

3.1 Introduction.

In the previous two sections a behaviour has been observed under conditions of forward conduction which does not appear to fit the depletion layer analysis, even taking into account large signal effects. It is the purpose of this section to examine the operation of the diode under conditions where the applied signal voltage exceeds the bias voltage and hence to draw conclusions about the behaviour of a circuit operating under these conditions as a frequency multiplier. Of particular interest is the behaviour of a circuit designed for depletion layer operation but actually operating in the forward conduction mode. The following theory will be concerned only with the diode functioning as a charge storage device, i.e. the case of an ideal resistive rectifier will not be considered, since it has already been shown[29] that this type of frequency multiplier has inherently low efficiencies. The following work takes as a starting point, the theory presented by Leenov and Uhlir[22], for a diode operating as a broadband harmonic generator.

The theory will assume an ideal charge storage device, i.e. the voltage and current waveforms are as shown in Fig. 3.1 where the following two conditions apply:

(a) All the charge stored during the portion of the cycle where the applied voltage exceeds the bias voltage is recovered.

(b) At the time when the total charge becomes zero the diode changes instantaneously from a short circuit to an open circuit.

In practice the recovery time will of course be finite. This, as one would expect, causes the practical results to be worse (in terms of efficiency) than the theory predicts.

3.2 Theoretical analysis of a charge storage multiplier.

3.2.1 Basic ideas.

The circuit analysed by Leenov and Uhlir is that shown in Fig.3.1,(a); note that no filters are included. The diode is negatively biased by the voltage V_B. Harmonics are generated by the transient which occurs when the diode switches off after all the charge has been recovered, as shown in Fig.3.1(c) (assuming the diode behaves as described in 3.1). Power flows in both the generator and load resistors at all harmonic frequencies and the conversion efficiency of power from the fundamental to a particular harmonic is therefore inherently low. If one tries to restrict power in the circuit to only the fundamental and one harmonic by incorporating suitable filters, (e.g. a high 'Q' parallel resonant circuit across R_n tuned to the required harmonic and a similar circuit shunting the generator tuned to the input frequency) the circuit will cease to function. This may be seen by the following simple argument: Assume the waveform across the junction to consist of two sinusoids,(this implies ideal filters or infinite 'Q' circuits). This means that the 'flat top' in the voltage waveform shown in Fig.3.1,(b) is made infinitesimally short in duration (corresponding to a peak of the voltage waveform) and therefore the time during which the diode conducts is reduced to zero, making charge storage operation impossible. It may therefore be concluded that it is necessary to have some series resistance in the circuit for such a mode to exist..

Two basic arrangements will be investigated; firstly the circuit shown in Fig.3.2(a) where the output is filtered to contain only the required frequency, secondly the circuit of Fig.3.3(a) where the output is taken across a load which is resistive at all frequencies. Note the resemblance of the circuit of Fig.3.2(b) to the node circuit for depletion layer operation where R_d is the series loss resistance of the diode.

3.2.2 Analysis of tuned output circuit.

It will be assumed for the purpose of the analysis that the filters are ideal. Two possibilities exist for the tuned output case: firstly that shown in Fig.3.2(a) where the generator is connected directly in series with the diode as shown, the generator resistance R_g being the necessary series resistance, and secondly that shown in Fig. 3.2(b), where the generator is coupled to the circuit via a matching transformer and filter, in which case the filter prevents harmonic currents from flowing in the generator and an additional resistance R_d is added in series with the diode to allow the necessary conditions discussed in section 3.2.1 to exist. Note that the operation of the two circuits is identical if we replace V_g and R_g in Fig.3.2,(a) by V_1 and R_d respectively of Fig.3.2.(b). The following analysis will apply to the circuit of Fig.3.2.(b) but efficiency expressions will be derived for both circuits.

A typical waveform of the current through the diode is shown in Fig.3.2.(c). It is assumed that the voltage across points X, Y, consists of the input and output frequencies only. We may write the voltage across the points X, Y thus:

$$v_{XY} = V_1 \sin \omega_1 t + V_n \sin \overline{n \omega_1 t + \phi_n} \qquad (3.1)$$

Now define currents thus:

$$I_{1a} = V_1/R_d \quad \text{and} \quad I_{na} = V_n/R_d \tag{3.2}$$

and

$$i = I_{1a} \sin \omega_1 t + I_{na} \sin \overline{n\,\omega_1 t + \phi_n} - I_B \tag{3.3}$$

This is the current that would flow if the above voltages were present and the diode were conducting all the time: it corresponds to the dotted curve of Fig.3.2.(c). The actual current flowing is given by the solid curve and it starts to flow at a time t_1 corresponding to the point when the voltage v_{XY} causes the diode to be driven positive. We can thus write:

$$I_B = I_{1a} \sin \omega_1 t_1 + I_{na} \sin \overline{n\,\omega_1 t_1 + \phi_n} \tag{3.4}$$

where $$I_B = V_B/R_d \tag{3.5}$$

The time t_3, corresponding to the point where the current stops flowing due to the diode becoming open circuit, is given by the condition that the total charge is zero. Thus:

$$\int_{t_1}^{t_3} i \, dt = 0 \tag{3.6}$$

This gives the result:

$$\frac{I_{1a}}{I_B}\left[\cos \omega_1 t_1 - \cos \omega_1 t_3\right] + \frac{I_{na}}{I_B n}\left[\cos \overline{n\omega_1 t + \phi_n} - \cos \overline{n\,\omega_1 t_3 + \phi_n}\right]$$
$$= \omega_1 (t_3 - t_1) \tag{3.7}$$

The actual currents flowing at any harmonic frequency may be found by Fourier analysis. Thus the current i_m at $m\omega_1 t$ is:

$$i_m = I_{ms} \sin m\,\omega_1 t + I_{mc} \cos m\,\omega_1 t \tag{3.8}$$

where I_{ms} and I_{mc} are determined in the usual manner, thus:

$$\begin{matrix} I_{ms} \\ I_{mc} \end{matrix} = \frac{\omega}{\pi} \int_{0}^{2\pi/\omega} f(t) \begin{matrix} \sin \\ \cos \end{matrix} m \omega_1 t \, dt \qquad (3.9)$$

$$\left.\begin{aligned} \text{where} \quad & f(t) = 0 \;, \; 0 < t < t_1 \\ & f(t) = i \;, \; t_1 < t < t_3 \\ & f(t) = 0 \;, \; t_3 < t < 2\pi/\omega \end{aligned}\right\} \qquad (3.10)$$

Solving (3.9) and (3.10) and substituting from (3.7) and (3.4) gives the following results:

$$I_{ms} = A_m I_{1a} + B_m I_{na} \qquad (3.11)$$

$$I_{mc} = C_m I_{1a} + D_m I_{na} \qquad (3.12)$$

where A, B, C, D, are each functions of n, t_1, t_3, and ϕ_n and correspond to the Fourier co-efficients. They are given in appendix 3.1.

The equations can now be solved in the following manner: Choose I_{1a}/I_B as a variable; this is related directly to the imput from the generator. Define a second variable $r = I_{na}/I_{1a}$; this will be dependent upon the value of the load resistor R_n. Now take an arbitrary value of ϕ_n; substitute these three quantities in (3.4) and obtain t_1, hence obtain t_3 from (3.7). Now (3.11) and (3.12) can be evaluated and the value of ϕ_n checked.

$$\text{since} \quad \phi_n = \pi + \tan^{-1} (I_{nc}/I_{ns}) \qquad (3.13)$$

The above procedure is repeated until the value of ϕ_n obtained from (3.13) is the same as the value originally chosen. Although somewhat tedious, the process is quite tractable once an initial value of ϕ_n has been determined.

(this initial value may be found by letting $r \to 0$). The value of R_d/R_n to give the above conditions may be found thus:

$$V_n = I_n R_n \qquad (3.14)$$

where $$I_n^2 = I_{ns}^2 + I_{nc}^2 \qquad (3.15)$$

Combining (3.14) with (3.2) gives:

$$R_d/R_n = I_n/I_{na} \qquad (3.16)$$

Substituting this in (3.15) and using (3.11) and (3.12) gives:

$$(R_d/R_n)^2 = (B_n^2 + D_n^2) + 2(A_n B_n + C_n D_n)/r + (A_n^2 + C_n^2)/r^2 \qquad (3.17)$$

where $$r = I_{na}/I_{1a} \qquad (3.18)$$

We are now in a position to determine the efficiency of the circuit. Consider the circuit of Fig.3.2.(b) and assume that the reactive part of the input current is 'tuned out' and that the transformer is used to match the generator resistance to the imput <u>resistance</u> of the circuit: the efficiency, η, may be expressed thus:

$$\frac{1}{\eta} = \frac{P_{in}}{P_{out}} = \frac{V_1 I_{1s}}{I_n^2 R_n} \qquad (3.19)$$

$$= \frac{R_n}{R_d} \left[\frac{A_1}{r^2} + \frac{B_1}{r} \right] \qquad (3.20)$$

Note that if the input filter consists of a simple resonant circuit tuned to the input frequency, it may not be possible to 'tune out' the reactive part of the current at this frequency. In this case the generator resistance

may be simply matched to the input impedance of the circuit. The efficiency under this 'impedance matched' condition is given by:

$$\frac{1}{\eta} = \frac{R_n}{R_d}\left[\frac{A_1}{r^2} + \frac{B_1}{r}\right]\sqrt{1 + \frac{C_1^2 + D_1^2 r^2 + 2C_1 D_1 r}{A_1^2 + B_1^2 r^2 + 2A_1 B_1 r}} \qquad (3.21)$$

Alternatively using the circuit of Fig.3.2.(a) and replacing the resistance R_d by the generator resistance R_g, the efficiency is defined thus:

$$\frac{1}{\eta} = \frac{P_{available}}{P_{out}} = \frac{V_1^2/4R_d}{I_n^2 R_n} \qquad (3.22)$$

$$= \frac{R_n}{R_g}\ \frac{1}{4}\ \frac{1}{r^2} \qquad (3.23)$$

Comparing (3.20) and (3.23) for the same output power (i.e. the same value of 'r') gives:

$$\frac{P_{in}}{P_{available}} = 4(A_1 + B_1 r) \qquad (3.24)$$

The performance of a X2 and a X10 multiplier, evaluated using the above theory, ~~are~~ is given in Fig.3.4 to Fig.3.6 for a range of values of R_n/R_d. A value of drive is chosen which corresponds with the region of maximum efficiency for the basic broadband circuit, (refer to Fig.3.7(a) or to the results of Leemov and Uhlir), the actual chosen condition being $V_1/V_B = 2$. Since the variation of power loss with angle of forward conduction is small in this region it was thought that this value would give a useful indication of the behaviour under tuned conditions. Experimental results confirm the soundness of this choice.

For large values of drive note that A_1 is large and hence the efficiency obtained with the circuit of Fig.3.2(b) is not much different from that obtained using the circuit of Fig.3.2(a). This can be seen from (3.24) ~~from~~ whence, for the condition $(A_1+B_1 r) = 0.25$ the two efficiencies are the same. This is approximately the case for the results shown in Fig.3.4 and Fig.3.5 which are actually plotted for the circuit of Fig.3.2(a). The maximum difference in power loss between the two circuits under the conditions considered is less than 1.0 dB.

The comparable behaviour of the two circuits can be explained simply by the following reasoning: in the circuit of Fig.3.2.(a) power loss at all harmonic frequencies occurs in the generator resistance R_g, also, since the fundamental component of current is large, the power input to the circuit is comparable ~~to~~ with the power available from the generator; in the circuit of Fig.3.2(b) power is dissipated in R_g only at the fundamental frequency, but since a resistance R_d is added in series with the diode the total power loss remains of the same order and the gain due to matching is small.

The advantage of the circuit of Fig.3.2.(b) only becomes apparent at low values of drive since the fundamental component of current is then small and using the circuit of Fig. 3.2.(a) the available power is very much greater than the input power. In general low values of drive are not of interest since under these conditions the harmonic current generated by the charge storage effect is small and the depletion layer effect will tend to dominate the behaviour. In order to predict the behaviour of depletion layer circuits operating under charge storage conditions the parameter 'r' is of interest. This is plotted in Fig.3.6 for the conditions considered above.

3.2.3 Analysis of tuned and matched input, broadband output circuit.

We have considered in the previous section the operation of the circuit with the output taken from a load, filtered to allow only the desired harmonic to flow. We will now treat the case where the output is taken from a load which is resistive at all frequencies but, unlike the circuit treated by Leenov and Uhlir, where the input from the generator is both filtered and matched. The purpose of the filter is to prevent harmonics flowing in R_g; it can be seen by referring to Fig.3.1(a) that in the optimized case of $R_n = R_g$, half the power at the output frequency is dissipated in the generator resistance when no filter is used. Note that the existence of all the harmonics in R_n does not preclude the output at the required frequency from being filtered, provided a resistive load still exists at all other frequencies. The circuit is given in Fig.3.3(a).

For the purpose of the analysis consider the circuit of Fig.3.3(a) re-drawn as in Fig.3.3.(b): the generator and associated filter and transformer have been replaced by an equivalent voltage generator of zero internal resistance. This is justified, since at all harmonic frequencies the filter presents a short circuit across points W, Y.

The components of current at the input and output frequencies may be found as before by a Fourier analysis. The conditions and equations are as in section 3.2.2, with $I_{na} = 0$.

The efficiency is given by:

$$\frac{1}{\eta} = \frac{V_1 I_{1s}}{I_n^2 R_n} \qquad (3.25)$$

$$= \frac{A_1}{A_n^2 + C_n^2} \qquad (3.26)$$

Compare this efficiency with that of the circuit shown in Fig.3.1.(a) where, under matched conditions,

$$\frac{1}{\eta} = \frac{1}{A_n^2 + C_n^2} \qquad (3.27)$$

This is the efficiency derived by Leenov and Uhlir and it is apparent that the addition of a filtered and matched input improves the efficiency by a factor $1/A_1$.

The matching conditions are determined simply as follows:

$$\text{Input resistance } R_{in} = V_1/I_{1s} \qquad (3.28)$$

$$= R_n/A_1 \qquad (3.29)$$

Hence for a turns ratio 1 : n as shown in Fig.3.3.(a) optimum conditions exist when

$$n = \sqrt{\frac{1}{A_1}\left[\frac{R_n}{R_g}\right]} \qquad (3.30)$$

It is assumed in the above considerations of efficiency that the reactive term in the input impedance is 'tuned out'. If this is not the case, the above equations will be modified thus:

$$\frac{1}{\eta} = \frac{\sqrt{A_1^2 + C_1^2}}{A_n^2 + C_n^2} \qquad (3.31)$$

$$\text{and,} \quad n = \sqrt{\frac{1}{\sqrt{A_1^2 + C_1^2}}\left[\frac{R_n}{R_g}\right]} \qquad (3.32)$$

This condition gives a slightly poorer efficiency, but since both A_1 and C_1 are less than unity, the circuit always gives

an efficiency which is better than if no input filter were used.

Results are plotted for a X2 circuit in Fig.3.7. Curve (a) for the untuned case, is shown for purposes of comparison. Curves (d) and (e) show the improvement obtained by addition of the input filter and are the same for any order of harmonic.

3.3 Discussion of results.

In the preceding section a theory has been evolved for two specific types of charge storage circuit, and results evaluated for some particular cases. Let us consider firstly the results for the tuned input circuit of section 3.2.3 which are given in Fig.3.7. for a X2 multiplier. As one would expect, the behaviour is similar to that of the basic broadband circuit in which the power loss becomes large at small values of drive and at values of drive which cause the diode to conduct for most of the cycle. It is seen that when the input is matched to the input impedance of the circuit the optimum efficiency is improved by about 5 dB. When conjugate matching is used the improvement is about 6.5 dB, corresponding to an overall maximum efficiency of-3.5 dB Curves (d) and (e) show the improvement due to matching and are applicable to any order of multiplier. Obviously since the input impedance is high for small values of drive the improvement due to matching is greater under these conditions as shown by the curves. It is apparent that this circuit, although giving a moderate efficiency for a X2 multiplier, does not give very good results for high order multiplication.

Consider now the circuit analysed in section 3.2.2. Power loss is plotted versus R_n/R_d in Fig.3.4 for a value of drive corresponding to $V_1/V_B = 2$. It is seen that the effect of tuning the output causes the maximum efficiency to be -7dB compared with -10dB for the basic untuned case. It may be seen from the experimental results of Fig.3.8 (obtained using the collector-base junction of an OC44 transistor at an input frequency of 350 Kc/s.) that the value of drive chosen for the curves of Fig.3.4 is not the optimum value and a further improvement of about 1.5 dB may be obtained by increasing the drive to a value corresponding to about 140°. This gives an overall optimum efficiency of -5.5dB.

The results for a X10 circuit are given in Fig.3.5 for the same value of drive ($V_1/V_B = 2$) It is seen that the improvement due to tuning the output is about 4 dB giving a maximum efficiency of -25 dB. Referring to the practical results given in Fig.3.9 it is seen that a further improvement of 4dB can be obtained by increasing the drive slightly. It may thus be concluded that the maximum efficiency obtainable with this circuit is about -21 dB for a X10 multiplier. This compares with an estimated efficiency of -23 dB obtainable with the circuit of Fig.3.3.(a), (tuned input case).

It has already been pointed out (section 3.2.2) that under conditions of large forward drive the circuit of Fig. 3.2.(b) gives results which are not much different from those using the circuit of Fig.3.2,(a). The circuit of Fig.3.2, (b) is of interest since it is essentially the same as the node type depletion layer circuit. It is thus possible to predict the behaviour that may be expected when a circuit designed for depletion layer operation is driven into charge storage operation. The curves of Fig.3.6 are of interest in this respect since they show the 'voltage gain' defined by (3.18), as a function of R_n/R_d. It is seen that as

R_n/R_d increases, the voltage gain, r, tends to a limit for a given value of drive. For the case considered the limiting value of 'r' is about 0.5 for a X2 circuit and 0.07 for a X10 circuit. This implies that if a depletion layer circuit has been designed with circuit parameters which give a voltage gain less than these values when the diode is just on the point of conduction, the gain will continue to increase as the input is increased. Note that whether or not the efficiency increases as the diode is driven into conduction depends upon the case in question. For low order multipliers it is possible to obtain high efficiencies using the depletion layer effect with only moderate 'Q' factors and generally the losses due to conduction will cause the efficiency to drop as the diode is driven into conduction. On the other hand it is possible that in the case of a high order multiplier with a low 'Q' diode the efficiency will increase as the diode is driven into conduction. By comparing the results of section 2 and section 3 it is possible to determine, for the cases studied, the relative merits of the two types of multiplier.

Note that the circuits considered in this section have each a dual. The duals are given in Fig.3.11. It is apparent that the operation of the basic untuned circuit of Fig.3.11,(a) is essentially the same as that of Fig.3.1,(a): when the voltage across G_g due to the generator current i_g reaches the value of the bias voltage, the diode starts to conduct; conduction continues until charge equilibrium again occurs, at which time the diode becomes open circuit and the diode current becomes zero. The diode voltage and current waveforms are thus the same as for the case already considered. Similarly if one considers the dual shown in Fig. 3.11,(b) it is seen that the operation is essentially the same as that of Fig.3.2,(a) and likewise Fig.3.11,(c) corresponds to Fig.3.2,(b). The theoretical analysis of section 3.2 may

thus be applied to the dual cases. Note however that the circuit shown in Fig.3.11,(d) is not directly suitable for charge storage operation since, following the argument of section 3.2.1, it is necessary to have a current path at all frequencies and if the series filters in each mesh are ideal this condition is not fulfilled.

3.4 Experimental results.

Experiments were performed to verify the preceding theory. The diode used was the collector-base junction of an OC44 transistor which gives reasonable charge storage characteristics between 100 kc/s and 10 Mc/s. The results for the tuned output case are given together with the theoretical curves in Fig.3.4 and Fig.3.5, the input frequency used being 350 kc/s. It is seen that the efficiencies obtained in practice are worse than the theoretical efficiencies, the difference being about 3 dB for the X2 circuit and 7 dB for the X10 circuit. Referring to the waveforms shown in Fig.3.10 it is seen that the pessimistic performance may be accounted for by the fact that charge recovery is not complete, (it was observed that considerable current flowed under forward conduction): when the frequency was increased from 350 kc/s to 2 Mc/s, approximately the same efficiency was obtained but in this case the poor performance may be explained by the fact that, although charge recovery was nearly complete the recovery time was long compared with the time for one cycle. The important point to note in the results is the fact that the difference in power loss between the tuned and untuned circuits is very close to that predicted by the theory (5 dB for the X2 circuit and 6 dB for the X10 circuit). The circuit parameters were chosen to minimise

the effect of the depletion layer capacitance. The value of R_g was 1.4 K.

The operation of filtered and matched input operation was verified for a X2 and a X10 circuit with an angle of drive of 120°. For the X2 case the following results were obtained:

Power loss under untuned conditions	=	12.6 dB
Power loss under tuned conditions	=	9.5 dB
Improvement due to matching	=	3.1 dB

For the X10 case the following results were obtained:

Power loss under untuned conditions	=	39 dB
Power loss under tuned conditions	=	33.5 dB
Improvement due to matching	=	5.5 dB

The theoretical improvement (given in Fig.3.7) is for an angle of drive of 120°, 5 dB for matching to the input impedance and 6.5 dB for conjugate matching, the latter being the condition in the experiment performed.

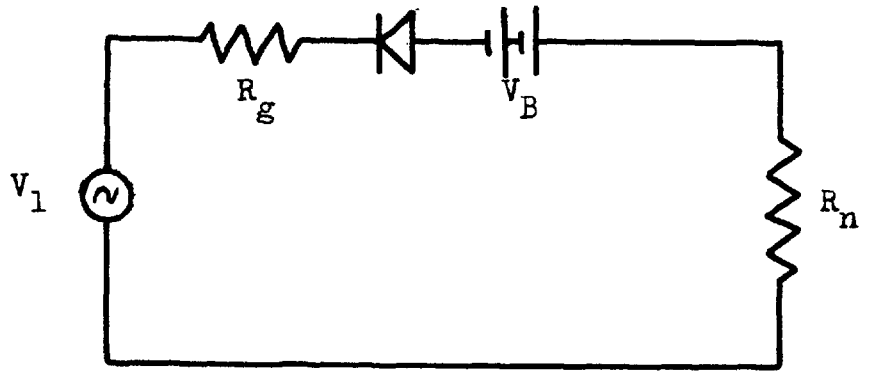
In order to check the performance of the tuned output circuit for various angles of drive the results given in Fig. 3.8 and Fig.3.9 were obtained. It is seen that in both cases the maximum efficiency occurs at an angle of about 140° giving a slight improvement compared with the efficiency at 120°.

The waveforms shown in Fig.3.10 show that for the X2 multiplier the assumption of the output voltage being sinusoidal (see section 3.2.2) is valid. However for the X10 case it is apparent from Fig.3.10,(h) that the waveform departs considerably from a sinusoid: this is a further possible reason for the departure from theory of the results for a X10 circuit.

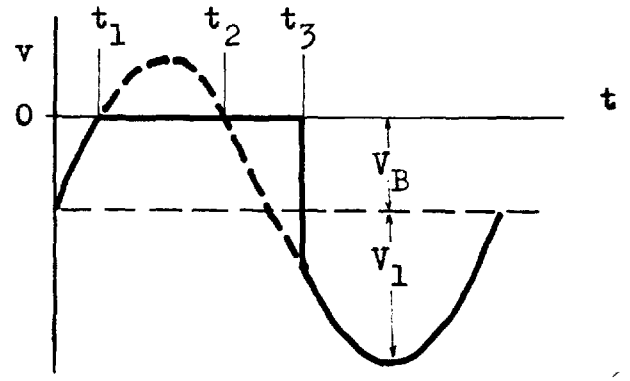
3.5 Conclusions.

A theory has been evolved for operation of a multiplier using the charge storage effect under tuned output and/or tuned input conditions. Some specific results have been obtained which enable the general behaviour to be predicted. In particular it is possible to draw certain conclusions as to the operation of a depletion layer circuit operating in the charge storage mode. The discrepancies between the experimental and the theoretical results may be accounted for by the fact that the diode used only approximated to an ideal charge storage diode.

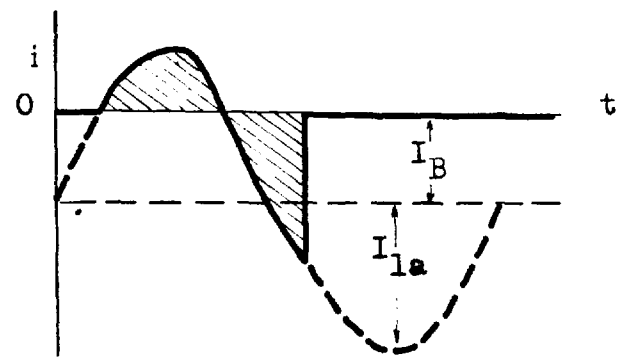
A set of general results has not been obtained for the tuned output case. This could most readily be done using a computer to solve the equations of section 3.?.? and appendix 3.1. Of particular interest is the solution for low values of drive for the circuit of Fig.3.?, (b) from whence it s hould be possible to evaluate completely the performance of a circuit operating under a combination of depletion layer and charge storage conditions.



(a) Basic broadband circuit

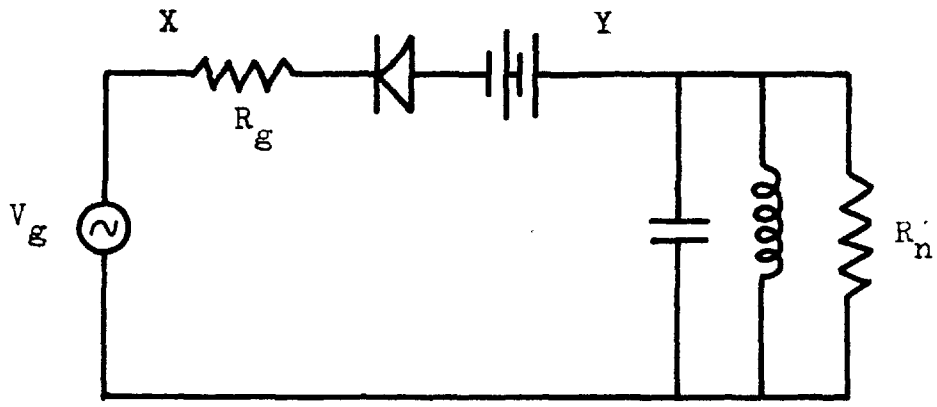


(b) Voltage waveform

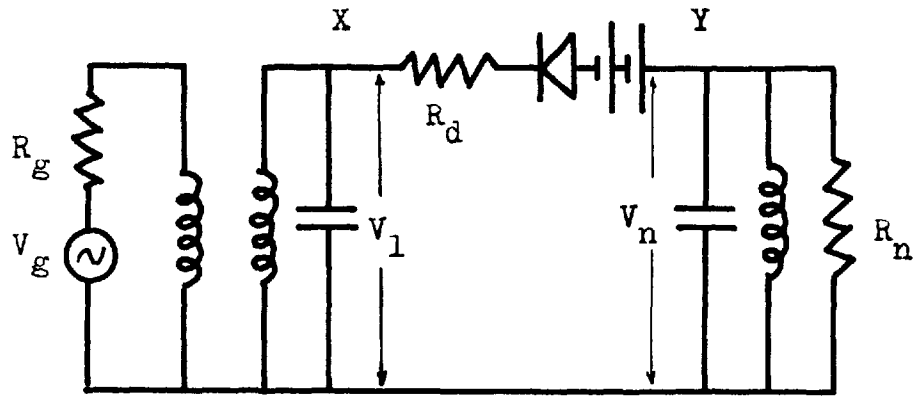


(c) Current waveform

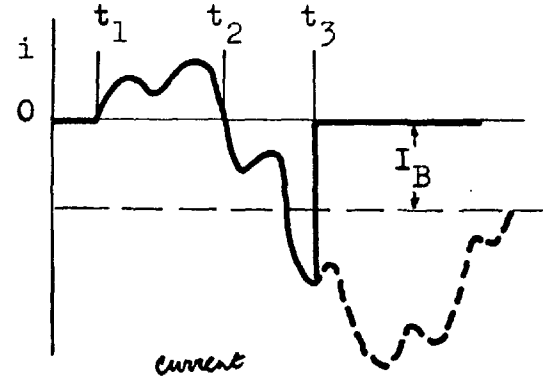
Fig.3.1 Basic broadband circuit and waveforms.



(a) Basic tuned output circuit

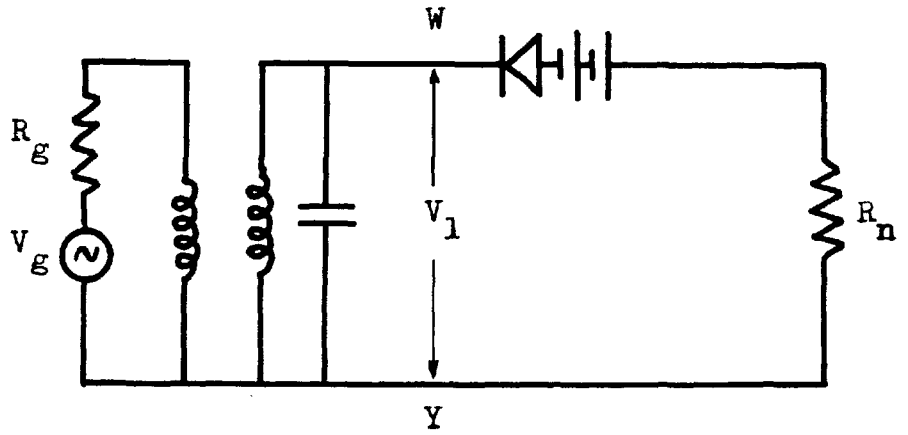


(b) Tuned output circuit with filtered and matched input

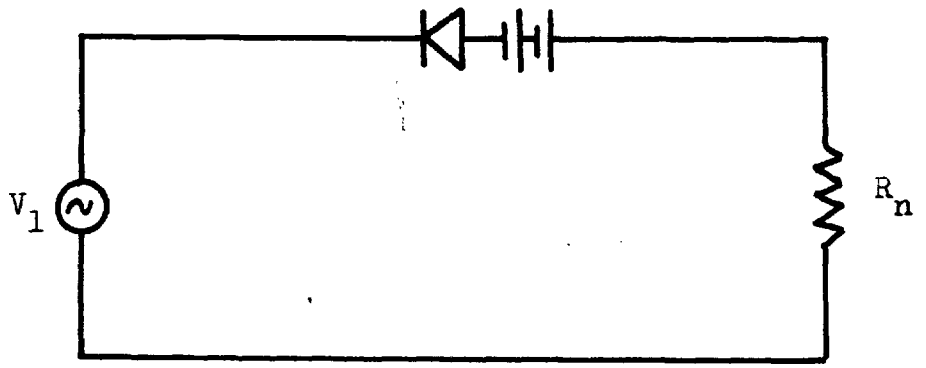


(c) Typical current waveform for tuned output ~~waveform~~

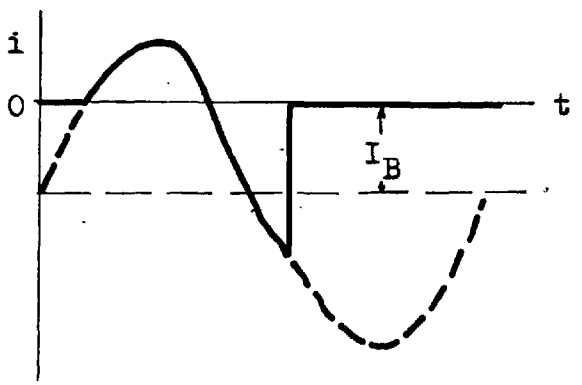
Fig.3.2 Tuned output circuits and waveforms.



(a) Filtered and matched input circuit



(b) Equivalent circuit of (a) used in the analysis



(c) Current waveform

Fig.3.3 Circuits and waveform for the case where the input is filtered and matched and the output is broadband.

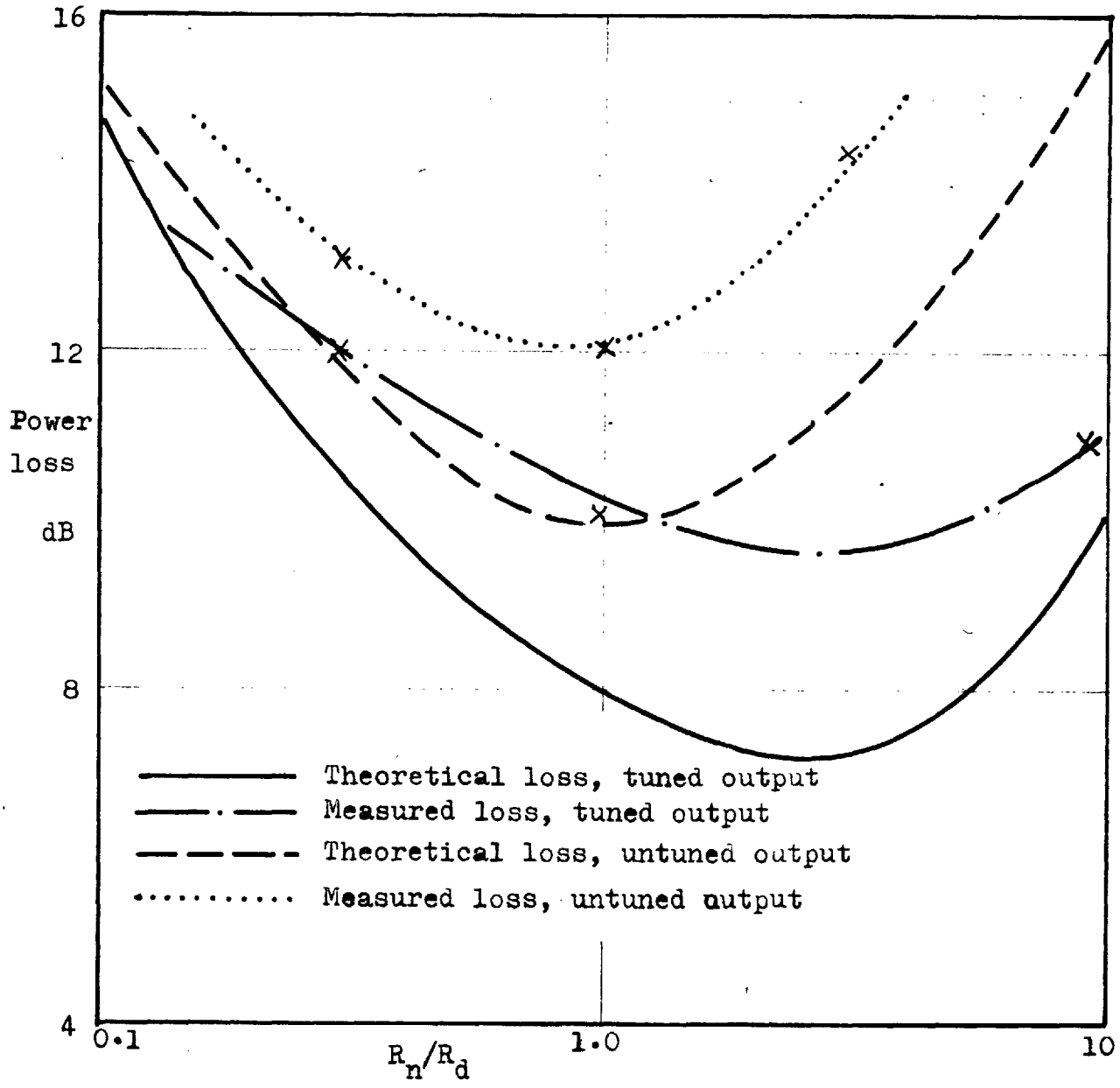


Fig.3.4 Power loss curves for a X2 tuned output charge storage multiplier for $V_1/V_B = 2$, plotted versus R_n/R_d, using the circuit of Fig.3.2,(a).

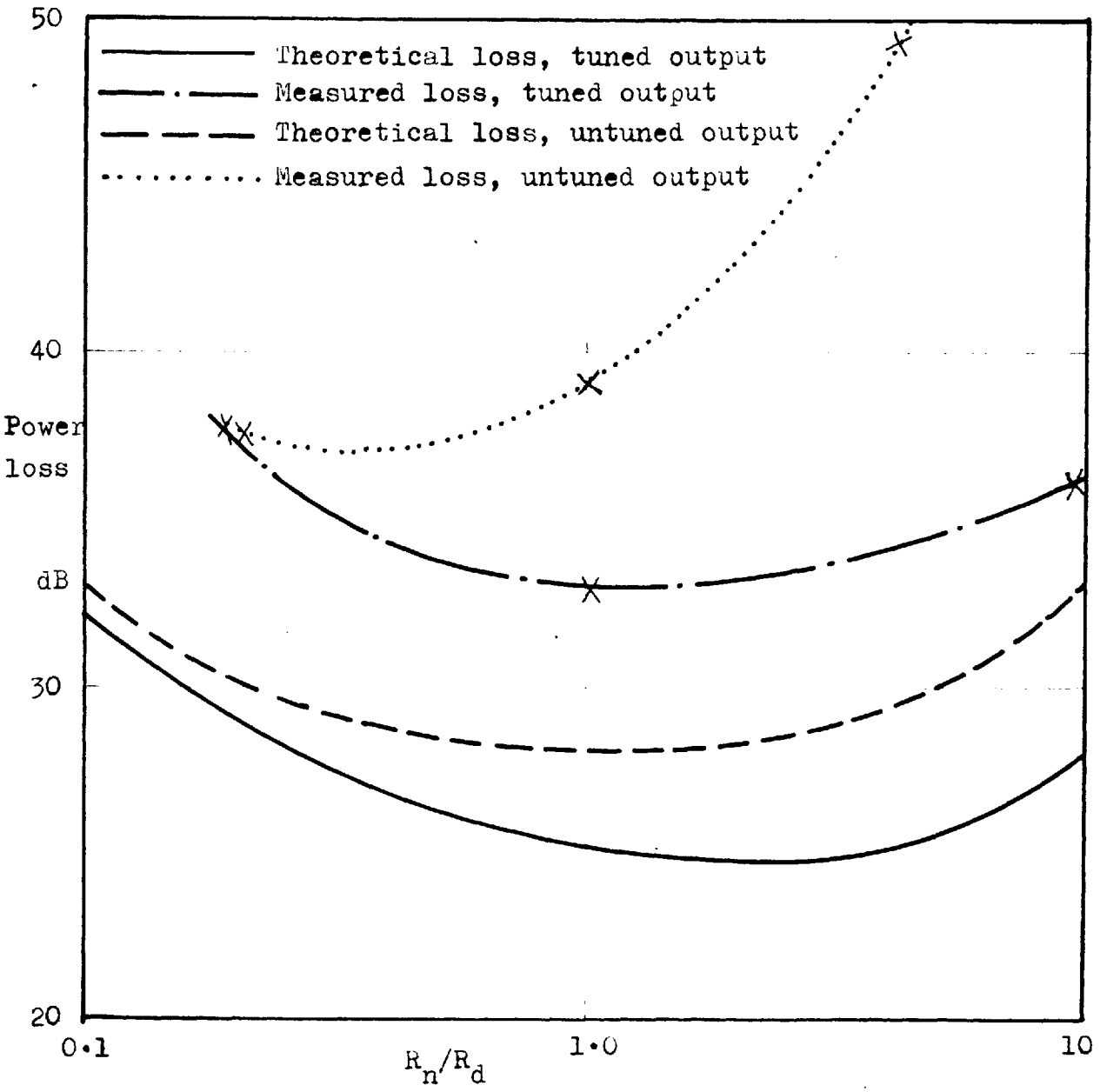


Fig.3.5 Power loss curves for a X10 tuned output charge storage multiplier for $V_1/V_B = 2$, plotted versus R_n/R_d, using the circuit of Fig.3.2,(a).

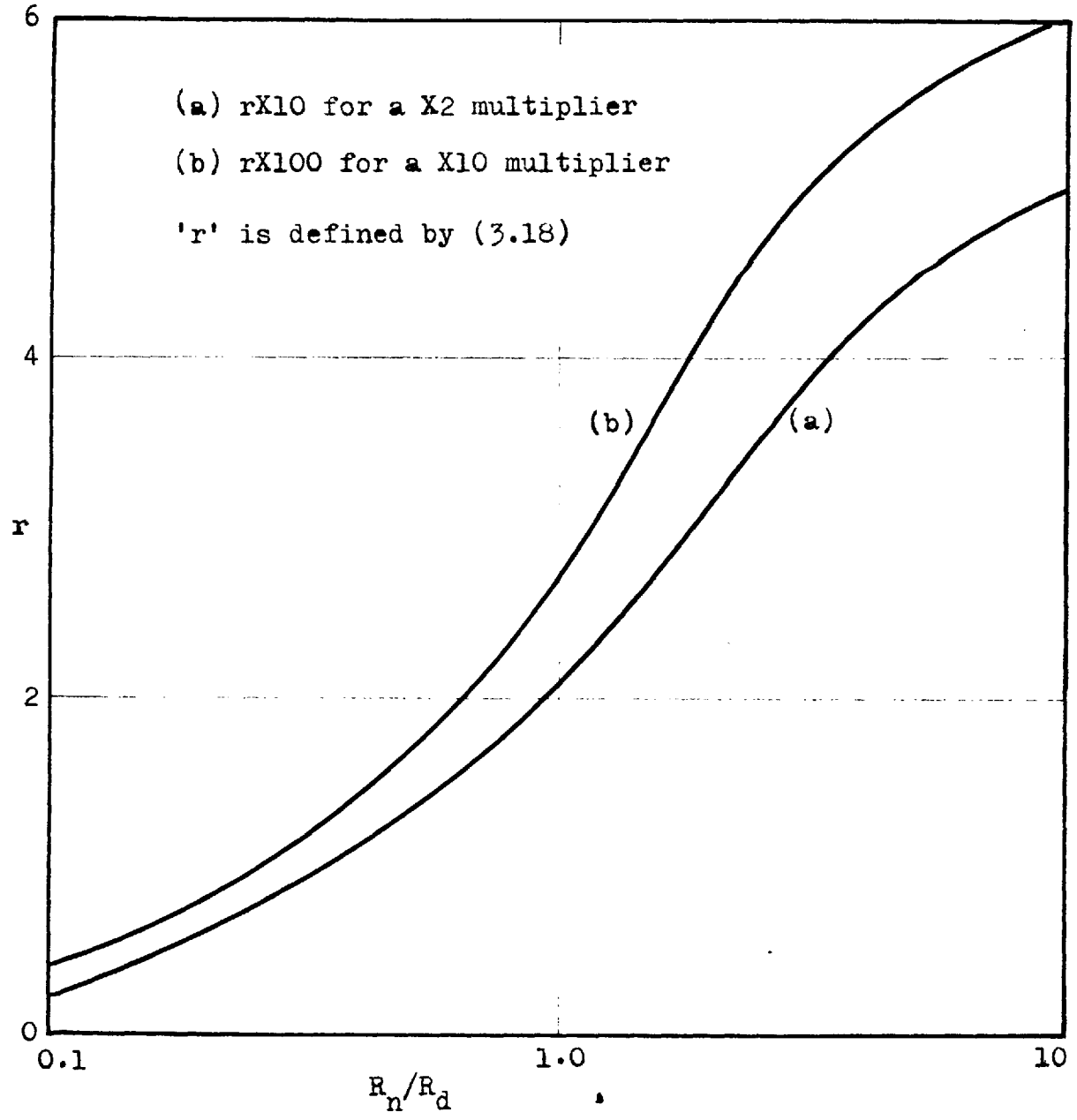


Fig.3.6 'r' curves for a X2 and a X10 tuned output charge storage multiplier, $V_1/V_B = 2$, plotted versus R_n/R_d.

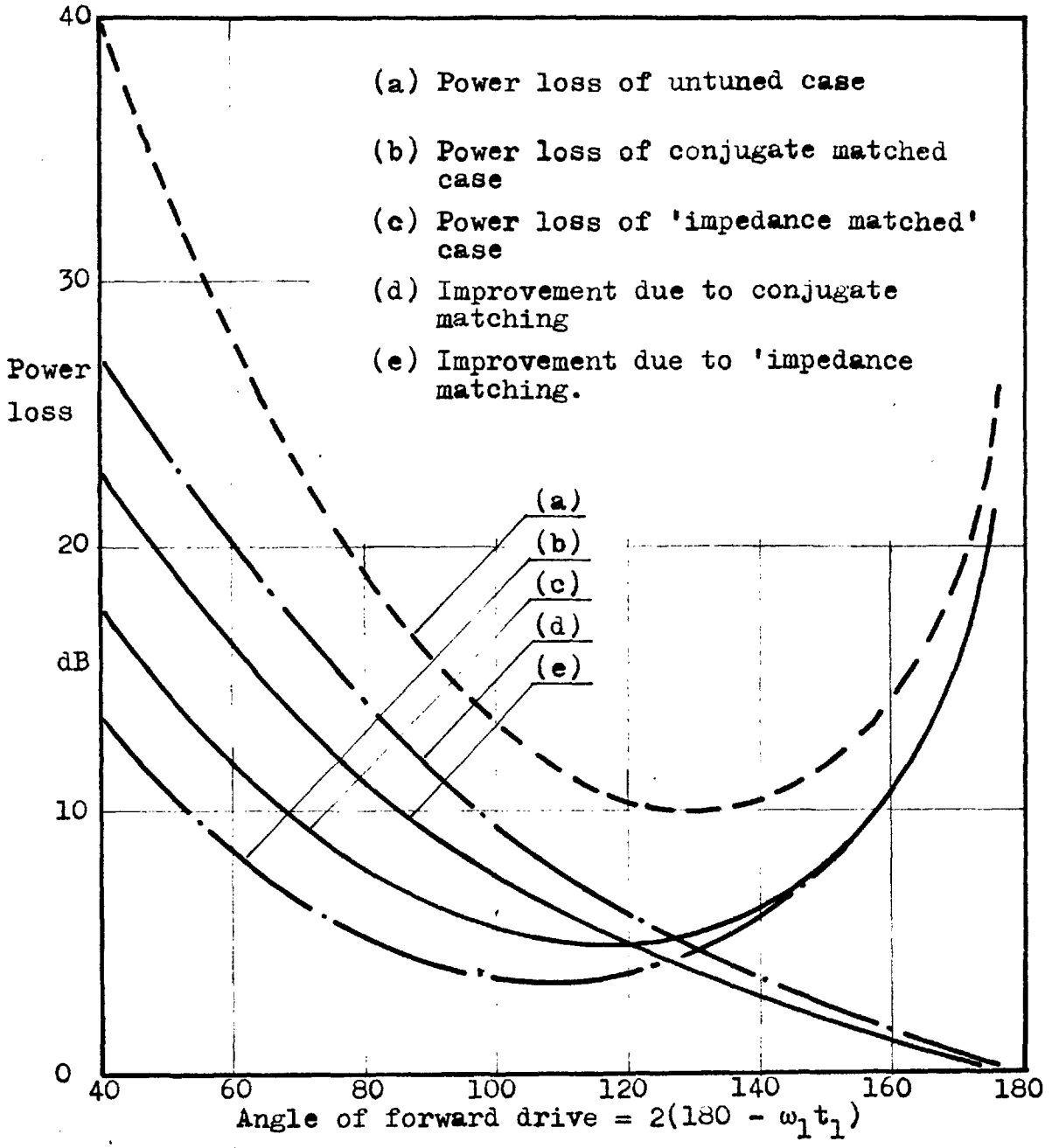


Fig.3.7 Power loss curves for a X2 tuned input charge storage multiplier.

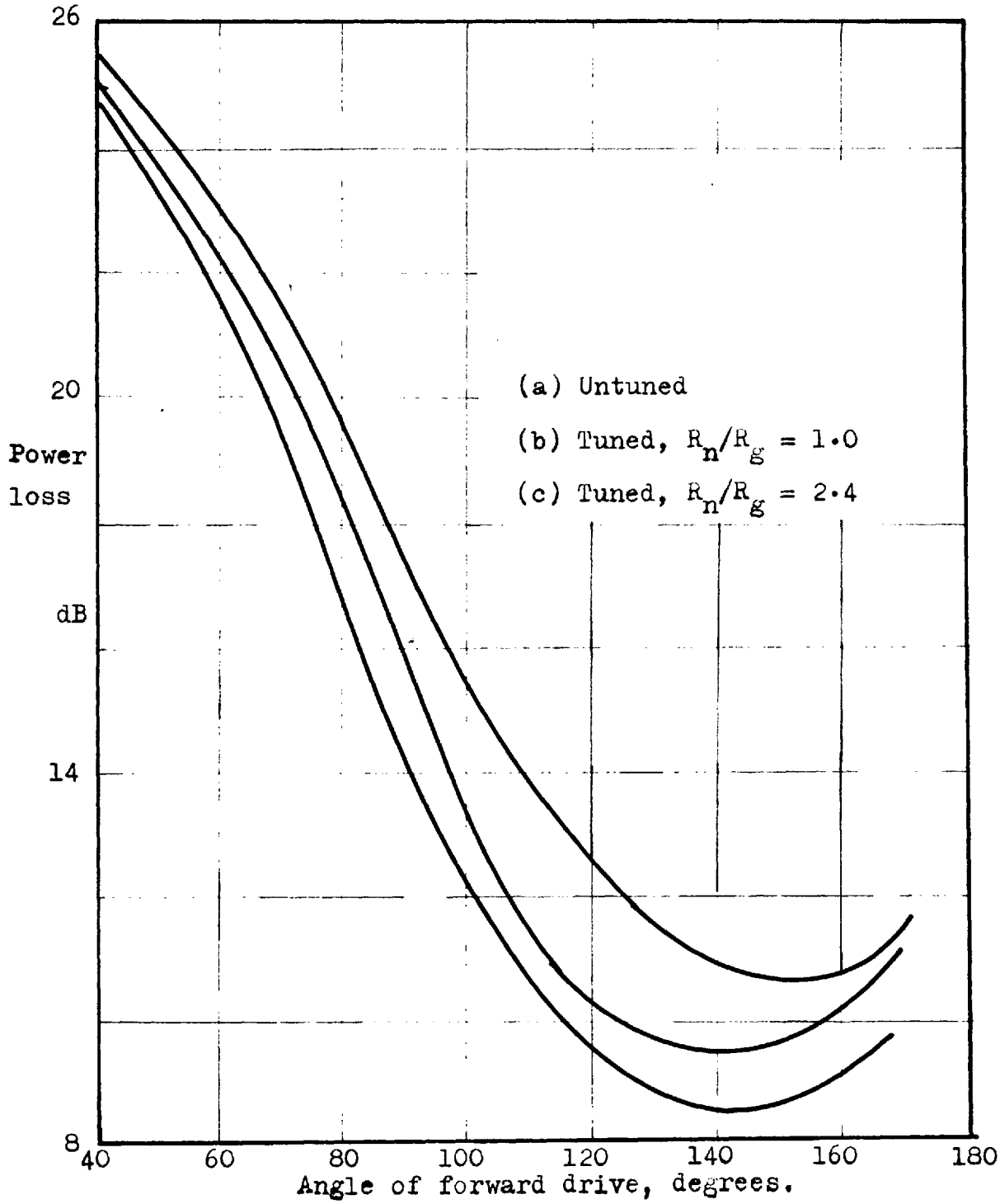


Fig.3.8 Measurements of power loss versus angle of forward drive for a X2 charge storage multiplier using the circuit of Fig.3.2,(a).

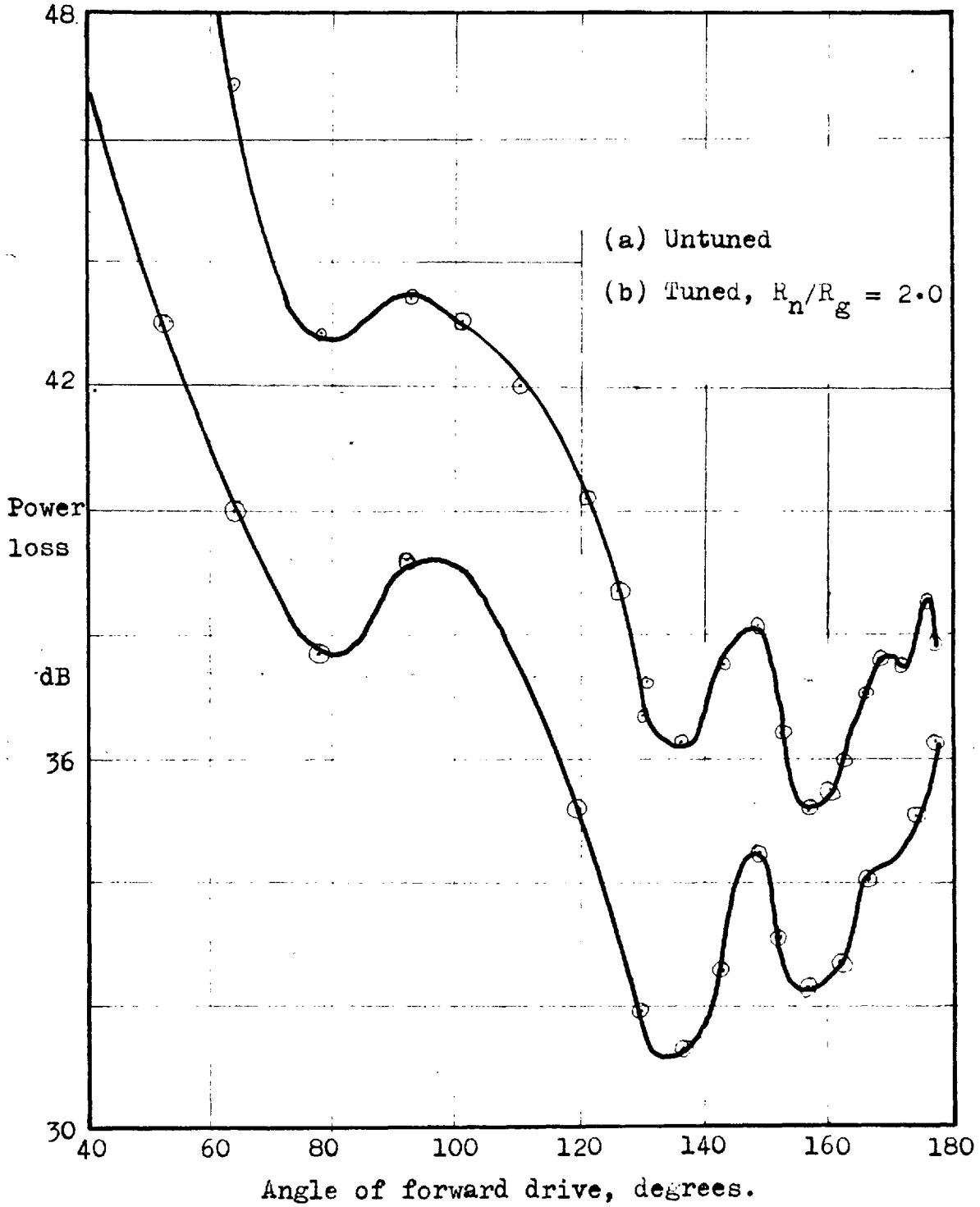
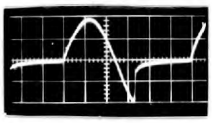
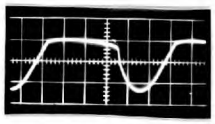


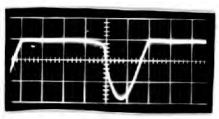
Fig.3.9 Measurements of power loss versus angle of forward drive for a X10 charge storage multiplier using the circuit of Fig.3.2,(a).



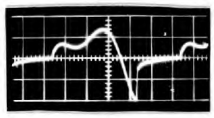
(a) Basic current waveform



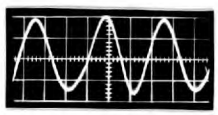
(b) Basic voltage waveform



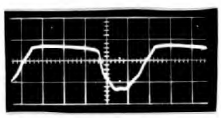
(c) X2 voltage waveform



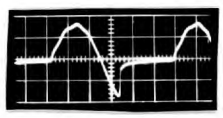
(d) X2 current waveform



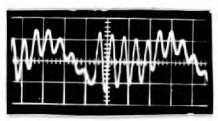
(e) X2 output waveform



(f) X10 voltage waveform

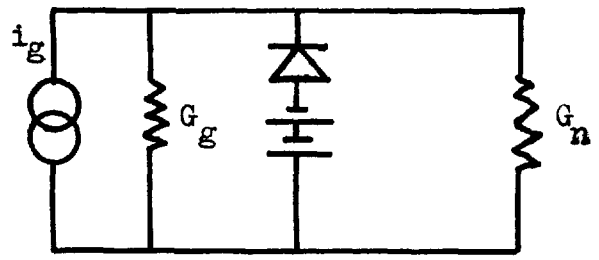


(g) X10 current waveform

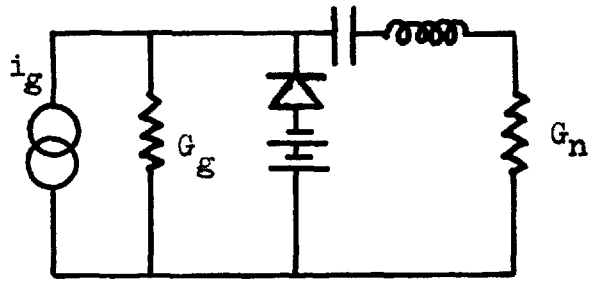


(h) X10 output waveform

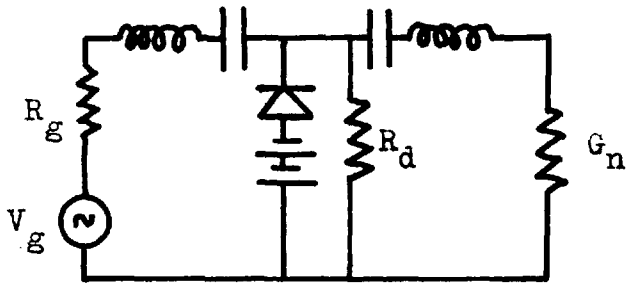
Fig.3.10 Waveforms obtained in experimental circuits.



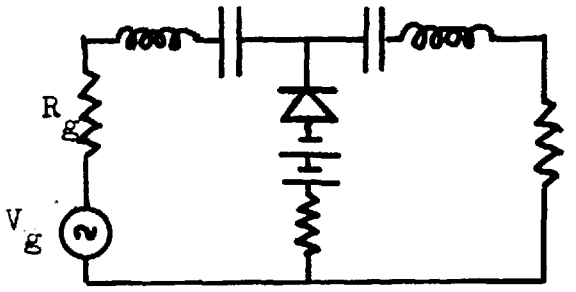
(a) Untuned, dual of Fig.3.1,(a)



(b) Tuned output, dual of Fig.3.2,(a)



(c) Tuned input and output, essentially a dual of Fig.3.2,(b)



(d) Basic depletion layer mesh type circuit.

Fig.3.11 Dual circuits

APPENDIX 3.1 RESULTS OBTAINED FROM FOURIER ANALYSIS.

The following are the equations for the variables A, B, C, D, of (3.11) and (3.12) obtained by a Fourier analysis as described by (3.9).

$$A_1 = \frac{1}{2\pi}\left[\omega_1(t_3-t_1) - \frac{1}{2}(\sin 2\omega_1 t_3 - \sin 2\omega_1 t_1) + 2\sin\omega_1 t_1(\cos\omega_1 t_3 - \cos\omega_1 t_1)\right]$$

$$B_1 = \frac{1}{2\pi}\left[\frac{1}{(n-1)}\left(\sin\overline{(n-1)\omega_1 t_3+\phi_n} - \sin\overline{(n-1)\omega_1 t_1+\phi_n}\right) - \frac{1}{(n+1)}\left(\sin\overline{(n+1)\omega_1 t_3+\phi_n} - \sin\overline{(n+1)\omega_1 t_1+\phi_n}\right) + 2\left(\sin\overline{n\omega_1 t_1+\phi_n}\right)(\cos\omega_1 t_3 - \cos\omega_1 t_1)\right]$$

$$C_1 = \frac{1}{2\pi}\left[\frac{1}{2}\left(\cos 2\omega_1 t_1 - \cos 2\omega_1 t_3\right) - 2\sin\omega_1 t_1\left(\sin\omega_1 t_3 - \sin\omega_1 t_1\right)\right]$$

$$D_1 = \frac{1}{2\pi}\left[\frac{1}{(n-1)}\left(\cos\overline{(n-1)\omega_1 t_1+\phi_n} - \cos\overline{(n-1)\omega_1 t_3+\phi_n}\right) + \frac{1}{(n+1)}\left(\cos\overline{(n+1)\omega_1 t_1+\phi_n} - \cos\overline{(n+1)\omega_1 t_3+\phi_n}\right) - 2\left(\sin\overline{n\omega_1 t_1+\phi_n}\right)\left(\sin\omega_1 t_3 - \sin\omega_1 t_1\right)\right]$$

$$A_n = \frac{1}{2\pi}\left[\frac{1}{(n-1)}\left(\sin(n-1)\omega_1 t_3 - \sin(n-1)\omega_1 t_1\right) - \frac{1}{(n+1)}\left(\sin(n+1)\omega_1 t_3 - \sin(n+1)\omega_1 t_1\right) + \frac{2}{n}\sin\omega_1 t_1\left(\cos n\omega_1 t_3 - \cos n\omega_1 t_1\right)\right]$$

$$B_n = \frac{1}{2\pi}\left[(\cos \phi_n)(\omega_1 t_3 - \omega_1 t_1)\right.$$

$$- \frac{1}{2n}\left(\sin \overline{2n\omega_1 t_3 + \phi_n} - \sin \overline{2n\omega_1 t_1 + \phi_n}\right)$$

$$\left. + \frac{2}{n}\left(\sin \overline{n\omega_1 t_1 + \phi_n}\right)\left(\cos n\omega_1 t_3 - \cos n\omega_1 t_1\right)\right]$$

$$C_n = \frac{1}{2\pi}\left[\frac{1}{(n-1)}\left(\cos (n-1)\omega_1 t_3 - \cos(n-1)\omega_1 t_1\right)\right.$$

$$- \frac{1}{(n+1)}\left(\cos (n+1)\omega_1 t_3 - \cos (n+1)\omega_1 t_1\right)$$

$$\left. - \frac{2}{n}\sin \omega_1 t_1 \left(\sin n\omega_1 t_3 - \sin n\omega_1 t_1\right)\right]$$

$$D_n = \frac{1}{2\pi}\left[\frac{1}{2n}\left(\cos \overline{2n\omega_1 t_1 + \phi_n} - \cos \overline{2n\omega_1 t_3 + \phi_n}\right)\right.$$

$$+ (\sin \phi_n)\left(\omega_1 t_3 - \omega_1 t_1\right)$$

$$\left. - \frac{2}{n}\left(\sin \overline{n\omega_1 t_1 + \phi_n}\right)\left(\sin n\omega_1 t_3 - \sin n\omega_1 t_1\right)\right]$$

SECTION 4.

SOURCES OF DECREASED EFFICIENCY WHEN USING PRACTICAL CIRCUITS.

4.1 Introduction.

In sect. 2 power loss curves were derived from a large signal analysis for a depletion layer multiplier, assuming the only losses which occurred were due to the series loss resistance of the diode. In a simple practical circuit the efficiency will in general be less than that predicted from the above results. The present section will analyse the various sources of additional power loss and, where necessary, modifications to the efficiency expression given in sect.2 will be introduced to take into account conditions encountered in practical circuits.

Note in particular the case treated in 4.2 which deals with the losses caused by the presence of finite resistance in the filters. In some cases, specially at low frequencies, this may be the dominating source of loss in a multiplier and thus merits special attention. The remaining sources of decreased efficiency can generally be eliminated, often by the use of additional filtering. This will be discussed in the relevant sections.

4.2 Losses due to finite resistance in circuit filters.

4.2.1. Node circuit.

Losses due to the filters may be taken into account by deriving a new expression for the efficiency, similar to that of sect. 2.3 but replacing the diode conductance by filter conductance G_1 and G_n at the input and output frequencies

respectively. The circuit under these conditions is shown in Fig.4.1,(a). The total conductance at the output frequency is now given by:

$$G_{mt} = G_o + G_n \tag{4.1}$$

The input and output power are now as follows:

$$P_{in} = V_1^2(G_1 + G_{eq}) \tag{4.2}$$

$$P_{out} = V_n^2 G_o \tag{4.3}$$

using the same nomenclature as in sect.2.3. The resulting expression for efficiency is, (following the method given in sect.2.3.1):

$$\frac{1}{\eta} = \left\{ 1 + \frac{n}{K^2} \left[\frac{G_1}{\omega_1 C_o} \right] \left[\frac{G_n}{\omega_n C_o} \right] \frac{G_{nt}}{G_n} \right\} \Big/ \left\{ 1 - \frac{G_n}{G_{nt}} \right\} \tag{4.4}$$

If C_{mt} is the total resonating capacitance at a node at frequency $\omega/2\pi$ and we define Q_m and α_m as follows:

$$Q_m = \omega_m C_{mt}/G_m \tag{4.5}$$

$$\alpha_m = C_{mt}/C_o \tag{4.6}$$

the resulting expression for efficiency becomes:

$$\frac{1}{\eta} = \left\{ 1 + \frac{n}{K^2} \left[\frac{\alpha_n}{Q_n} \right] \left[\frac{\alpha_1}{Q_1} \right] \left[\frac{Q_n}{Q_{nt}} \right] \right\} \Big/ \left\{ 1 - \frac{Q_{nt}}{Q_n} \right\} \tag{4.7}$$

where Q_{nt} is the loaded 'Q' factor of the output node. This form is particularly convenient at low frequencies where the 'Q' factors of circuits are readily measurable quantities. Power loss curves are plotted for X2, X3 and X10 multipliers in Figs.4.2 to Fig.4.6 for various values of α_n/Q_n.

4.2.2. Mesh circuit.

The efficiency for the mesh circuit under conditions where all the losses are concentrated in the filters may be evaluated in a similar manner. Defining R_1 and R_n as the filter loss resistances in the input and output meshes respectively (see Fig.4.1, (c) for the circuit under these conditions), the resulting expression is:

$$\frac{1}{\eta} = \left\{1 + \frac{1}{K^2_n}(\omega_n C_o R_n)(\omega_1 C_o R_1)\left[\frac{R_{nt}}{R_n}\right]\right\} \Big/ \left\{1 - \frac{R_n}{R_{nt}}\right\} \qquad (4.8)$$

where R_{nt} is the total resistance at the output frequency.

As before we can obtain an alternative expression by letting:

$$Q_m = 1/\omega_m C_{mt} R_m \qquad (4.9)$$

$$\alpha_m = C_o/C_{mt} \qquad (4.10)$$

where C_{mt} is the total resonating capacitance in a mesh at frequency $\omega/2\pi$. This gives:

$$\frac{1}{\eta} = \left\{1 + \frac{1}{K^2_n}\left[\frac{\alpha_n}{Q_n}\right]\left[\frac{\alpha_1}{Q_1}\right]\left[\frac{Q_n}{Q_{nt}}\right]\right\} \Big/ \left\{1 - \frac{Q_{nt}}{Q_n}\right\} \qquad (4.11)$$

where Q_{nt} is the loaded 'Q' factor of the output mesh.

Power loss curves using the above result are given in Fig.4.7 to Fig.4.9 for a X2 ($\gamma = 1/2$ and $\gamma = 1/3$) and a X3 ($\gamma = 1/3$) multiplier.

4.2.3 Discussion of results for the node circuit.

The assumptions on which the preceding estimation of efficiency is based are essentially those outlined in sect.2.4.1, condition (b) being that treated in this section. As has

already been pointed out, conditions (a) and (c) can be realised by the addition of suitable filters as shown in Fig.2.1, (b). It will therefore be assumed in the following discussion that these additional filters are included or that they are not required. The behaviour of the circuit without such filters is treated in sect.4.3. In either case the power loss given by (4.4) or (4.7) represents a basic loss for a given circuit, i.e., it is not possible to eliminate it by introducing additional circuitry. It is therefore important to be able to estimate the loss in a given case to see how it compares with the diode loss derived in sect.2. Three possibilities exist:

(a) the filter loss is negligible compared ~~to~~ with the diode loss,

(b) the filter loss is much greater than the diode loss,

(c) the two losses are comparable.

Case (a) is trivial and the efficiency of a multiplier may be estimated using only the results of sect.2. Of the remaining two possibilities let us consider firstly the case where the filter losses dominate the behaviour.

It often happens at low frequencies (i.e. of the order 1Mc/s to 100Mc/s), where the diode 'Q' factor is high and the 'Q' factors of the circuit components relatively low, that the efficiency of a multiplier is determined solely by the filter losses. It is thus worth considering in some detail the behaviour of the circuit under these conditions. Take, as an example, the results for a X2 node multiplier given in Fig.4.2. The power loss is plotted versus α_n/Q_{nt}, which from (4.5) and (4.6) is the same as $G_{nt}/\omega_n C_o$, the parameter used in sect.2. The curves shown are for the case where $\alpha_1/Q_1 = \alpha_n/Q_n$. Since in general the 'Q' factors at the input and output nodes will be approximately equal this implies that the curves plotted pertain to the case where the total capacitances at each node are the same. In the circuit

of Fig.4.1,(a) it may often be convenient in practice, particularly when several stages are cascaded together, to make $\alpha_1 = 2\alpha_2$. In this case the loss may be estimated by interpolating between the two values of α (cascading will be discussed in detail in sect.5). It is apparent from the curves that the power loss (for a given 'Q' factor) decreases as the value of α is decreased. This is intuitively obvious by looking at the basic circuit of Fig.4.1,(a), since for large values of α the coupling between the two nodes is small and hence any non-linear effect due to the diode will be small, i.e. G_{eq} of (4.2) will be small compared to G_1, the filter loss at the input node. Note that this is not the case when diode losses predominate (see sect.2) since under these conditions the corresponding 'Q' factor is a function of the diode series resistance and therefore is not constant but dependent on α .

Fig.4.2 may be used to find the minimum possible loss for a given value of filter 'Q' factor. This occurs when $\alpha_1 = \alpha_2 = 1.0$, under which condition additional series filters are essential to form the necessary short circuit paths at each node as shown in Fig.4.1,(b) with $C_1 = C_2 = 0$. For example, for a filter 'Q' factor of 100 the appropriate curve shows that the minimum loss is about 0.4 dB, occurring at a value of Q_{nt} equal to approximately 3.0. If the value of α is increased to 10 the minimum loss becomes 3.6 dB. Note, however, that for high values of α additional filters do not substantially alter the performance (see sect.4.3 for further treatment of this point) and it may sometimes be preferable to operate under conditions of reduced efficiency for the sake of less complicated circuitry. Also for simplicity in circuitry it may be desirable to operate at values of Q_{nt} which do not correspond to minimum power loss. For example, to avoid the use of extra filters (see sect.4.3.4) it may be desirable to make Q_{nt} fairly high, thus making α_n/Q_{nt} less than

the optimum value.

Comparison of the results shown in Fig.4.6 for the minimum loss for X2, X3 and X10 multipliers enables some conclusions to be drawn about the best arrangement of circuits for a high order of multiplication. Consider for example the efficiency obtained with a value of $\alpha / Q = 0.01$:

The X2 circuit gives a minimum loss of 0.46 dB.
The X3 circuit gives a minimum loss of 1.2 dB.
The X10 circuit gives a minimum loss of 11.0 dB.

If several stages are cascaded together it is apparent that for similar values of 'frequency gain' a multiplier based on X2 stages is considerably better than other combinations. The following example makes this clear:

X8 multiplication using 3 X2 stages gives a loss of 1.38dB.
X9 multiplication using 2 X3 stages gives a loss of 2.4 dB.
X10 multiplication using one stage gives a loss of 11.0 dB.

The superiority of the X2 method is enhanced when utilisation of the characteristic is limited by forward conduction effects; this is apparent from Fig.4.6. which shows minimum power loss curves for three values of V_b'/V_b. The conclusions are thus the same as for the case where the diode losses predominate and in fact the advantage of cascading X2 circuits is greater for the lossy filter case than for the lossy diode case. Further discussion on cascading will be found in sect.5.

It may happen at intermediate frequencies that the two losses (diode and filter) are of the same order. It is thus necessary to know how they combine. Using the nomenclature of sect.2.3.1. and sect.4.2.1. we can define the power loss thus:

$$\frac{1}{\eta} = \frac{P_{in}}{P_{out}} = \frac{V_1^2 (G_1 + G_{d1} + G_{eq})}{V_n^2 G_o} \qquad (4.12)$$

(This is in effect equivalent to combining (2.73) with (4.2)).

Since $V_1^2 G_{eq} = V_n^2 G_{nt}$ (2.70)

where $G_{nt} = G_o + G_{dn} + G_n$ (4.13)

we may re-write (4.12) as follows:

$$\frac{1}{\eta} = \left\{ 1 + \left[\frac{V_1}{V_n}\right]^2 \left[\frac{G_1 + G_{d1}}{G_{nt}}\right] \right\} \Big/ \left\{ 1 - \left[\frac{G_n + G_{dn}}{G_{nt}}\right] \right\} \quad (4.14)$$

This is equivalent to saying that if we represent the diode loss by:

$$L_d = (1 + N_d) / (1 - M_d) \quad (4.15)$$

and the filter loss by:

$$L_f = (1 + N_f) / (1 - M_f) \quad (4.16)$$

where N and M are the appropriate terms of (2.75) and (4.4) or (4.7), the total loss is given by:

$$L_t = (1 + N_d + N_f) / (1 - M_d - M_f) \quad (4.17)$$

which is an intuitively obvious result.

If N_d, M_d, N_f, M_f are each much less than unity, the total loss will be:

$$L_t = 1 + N_d + N_f + M_d + M_f \quad (4.18)$$

In this case the total power loss in dB given by,

$$D_t = \left[10 \log L_t\right] \text{ dB} \quad (4.19)$$

will be simply the sum of the individual losses given by the respective power loss curves of sect. 2.3.1. and sect. 4.2.1. The overall performance of a multiplier can thus be readily estimated from the results already obtained, the limiting individual loss being about 1.0 dB for reasonable accuracy.

In the case of large losses it is not possible to use directly the two sets of results already obtained. In particular if 'M' is a quantity approaching unity, the addition of a second term may cause $M_d + M_f$ to become greater than unity. This implies an impossible situation and in fact means that the operating point must be altered; i.e., that G_{nt} must be increased so that a finite value of G_o remains. A good approximation to the overall efficiency can be obtained, however, if a sufficiently large value of G_{nt} is chosen, i.e. one which makes both M_d and M_f much less than unity. This will in fact generally be the case, since even in a low efficiency multiplier the load conductance will normally comprise the greater part of the total conductance at the output node: i.e., G_{nt} will usually be considerably greater than either G_n or G_{dn} (see (4.14)). Referring to the power loss curves this implies an operating point considerably removed from the point where the power loss becomes infinite. From Fig.2.13 it is apparent that large values of G_{nt} imply values of V_l/V_b near to unity or (see Fig.2.4 and Fig.2.5) small values of V_n/V_l. It is thus seen from (4.14) that the case of N_d and/or N_f being much greater than unity and M_d and M_f much less than unity, is a case often encountered in practice. Under these conditions the losses are as follows:

$$L_d = N_d \tag{4.20}$$

$$L_f = N_f \tag{4.21}$$

$$L_t = N_d + N_f \tag{4.22}$$

and

$$D_t = \left[10 \log N_d + 10 \log (1+N_f/N_d) \right] \text{dB} \tag{4.23}$$

This shows clearly that the total loss is much less than the sum of the individual losses in low efficiency circuits. Note that if D_d and D_f are the diode and filter losses respectively (obtained from the appropriate curves), (4.23) can be found since:

$$10 \log (N_f/N_d) = D_f - D_d \tag{4.24}$$

4.2.4. Discussion of results for mesh circuits.

The general remarks referring to the X2 node circuit also apply to the X2 mesh circuit and will not be repeated. The efficiencies of the two circuits are substantially the same as can be seen by comparing Fig.4.2 and Fig.4.7. Note that since the circuit parameters are different it is not possible to relate directly the values of α_m and Q_m for the two cases. The choice between a mesh and a node circuit (for a X2 multiplier) will therefore be dictated by practical circuit considerations rather than on a basis of theoretical efficiency (bearing in mind the fact that the two circuits also give similar resultsunder conditions where the diode losses predominate). As expected the mesh circuit gives poor efficiencies for other than X2 multiplication. Curves for a X3 mesh multiplier are given in Fig.4.8 for the sake of completness but it is clear from Fig.4.9 that a vastly inferior performance is obtained compared to that of an X2 circuit.

4.3. Effect of finite reactance of filters.

4.3.1. Introduction.

Referring to the basic node and mesh circuits shown in Fig.4.1,(a) and Fig.4.1,(c) it is obvious that the simple filters shown formed by L_1C_1 and L_nC_n do not present zero (or infinite) impedance paths at frequencies other than their resonant frequencies. This may in some cases seriously affect the performance of a multiplier if not taken into account in the theory or eliminated by using additional filters. It is thus necessary to examine the effects of finite reactances of the filters. Consider the node circuit: L_1C_1 and L_nC_n will possess some finite reactance at ω_n and ω_1 respectively. This gives rise to two effects:

(a) The voltage and conductances at the two nodes are not the same as those appearing across the diode.

(b) The load and generator conductances are not by-passed at the input and output frequencies respectively.

Because of (a) it is necessary to modify the Power loss expressions obtained in sect.2.3 and sect.4.2. Effect (b) can be taken into account by modifying the values of the 'Q' factors of the filters used in sect.4.2. The two effects will be treated separately, with special attention being paid to the case of the X2 multiplier.

4.3.2. Modification of power loss expression.

In order to find the voltages at the input and output frequencies appearing across the diode it will be assumed that the admittance at the input mode at the output frequency is susceptive as is the admittance at the output node at the input frequency. The circuit can thus be represented as

shown in Fig.4.10,(a) for the node circuit and Fig.4.10,(b) for the mesh circuit. Let us consider the node circuit.

Using V_1 and V_n to represent the voltage across the diode, define V_1' and V_n' as the corresponding voltages at each node. Let the voltages be related thus:

$$V_1/V_1' = T_1 \tag{4.25}$$

$$V_n/V_n' = T_n \tag{4.26}$$

These quantities can be evaluated in terms of the circuit constants on the assumption that the diode impedance is that of the linear capacitance C_o, i.e. the non-linear part of the impedance is neglected. Since the effect under investigation is in general a second order one, this approximation is justified.

Let $$\omega_1^2 L_1 C_{1t} = 1 \tag{4.27}$$

and $$\omega_1^2 L_1 C_1 = E_1 \tag{4.28}$$

where $$C_{1t} = C_1 + C_{o1}'' \tag{4.29}$$

and C_{o1}'' is the capacitance formed by C_o in series with X_n at ω_1.

Then $$T_1 = X_o(\text{at } \omega_1)/\left[X_o \text{ (at } \omega_1) + X_n(\text{at } \omega_1)\right] \tag{4.30}$$

$$= C_{o1}''/C_o \tag{4.31}$$

$$= \alpha_1(1 - E_1) \tag{4.32}$$

where α_1 is defined by (4.6).

Similarly where:

$$\omega_n^2 L_n C_{nt} = 1 \tag{4.33}$$

$$\omega_n^2 L_n C_n = E_n \tag{4.34}$$

and $$C_{nt} = C_n + C_{on}'' \tag{4.35}$$

$$T_n = C_{on}''/C_o \tag{4.36}$$

$$= \alpha_n(1 - E_n) \tag{4.37}$$

where α_n is defined by (4.6)

Note that α_1, α_n are functions of E_1, E_n. These functions are evaluated in Appendix 4.1 and the results for a X2 mode circuit are given in Fig.4.11. It is seen that for values of α_1 greater than 10 the values of E are such as to make T_1 and T_n very close to unity, i.e. the effect of the filter reactances may be neglected if α_1 is greater than 10.

The load conductance seen by the diode will be altered (for cases where $T_n \neq 1.0$) to a modified value G_{nt}' where :

$$V_n^2 G_{nt}' = V_n'^2 G_{nt} \tag{4.38}$$

i.e. $$G_{nt}' = G_{nt}/T_n^2 \tag{4.39}$$

Similarly the input conductance G_{eq} defined by (2.70) is related to the conductance seen across the diode G_{eq}' thus:

$$V_1^2 G_{eq} = V_1'^2 G_{eq}' \tag{4.40}$$

i.e. $$G_{eq}' = G_{eq} T_1^2 \tag{4.41}$$

Substituting the above results in the derivation of the power loss expression of sect. 2.3.1 gives:

$$\frac{1}{\eta} = \left\{ 1 + \frac{1}{K^2 Q_{dn}} \left[\frac{G_{nt}}{\omega_n C_o}\right] \left[\frac{C_{ol}'}{C_{ol}}\right]^2 \left[\frac{1}{T_n}\right]^2 \right\} \Bigg/ \left\{ 1 - \frac{1}{Q_{dn}} \left[\frac{\omega_n C_o}{G_{nt}}\right] \left[\frac{C_{on}'}{C_{on}}\right]^2 T_n^2 \right\} \tag{4.42}$$

Note that this modified expression contains only the factor T_n, a not unexpected result since the input filter is assumed lossless and therefore its relation to the diode (given by α_1) should not have any effect on the performance, i.e. T_1 should not appear in the loss. Note also that equations (4.29) onwards do not take into account the variation of C_o due to the non-linear effect, given by (2.25) and (2.26) and hence the results obtained are subject to slight approximation, inasmuch as T_n is a function of C_{on}'. Since, however, this is a second order effect the above results may be considered as being substantially correct. It is seen from (4.42) that the presence of T_n may be considered as altering the factor $G_{nt}/\omega_n C_o$; thus the effect of T_n not being equal to unity is to shift the curves of Fig. 2.14 to Fig. 2.17 horizontally, the minimum power loss remaining the same.

The modified loss, in the case where only the filter losses exist, is found by using (4.25) to (4.41) in the derivation of sect. 4.2.1. The resulting expression is:

$$\frac{1}{\eta} = \left\{1 + \frac{n}{K^2}\left[\frac{\alpha_n}{Q_n}\right]\left[\frac{\alpha_1}{Q_1}\right]\left[\frac{Q_n}{Q_{nt}}\right]\left[\frac{1}{T_1^2 T_n^2}\right]\right\} \Bigg/ \left\{1 - \frac{Q_{nt}}{Q_n}\right\} \qquad (4.43)$$

It may be seen by inspection, using the results given in Fig. 4.11, that for values of α_1 less than 4.0 the power loss may be increased considerably. For example consider the case of $\alpha_1 = \alpha_2 = 3.0$: $E_1 = 0.64$, $E_2 = 0.83$, hence $T_1 = 1.08$ and $T_2 = 0.51$. Thus the product $T_1^2 T_n^2 = 0.35$, which will seriously degrade the performance, as can be seen from (4.43).

The above results have been obtained for a node multiplier. In a similar manner the mesh circuit can be treated. In this case we define:

$$I_1/I_1' = T_1 \qquad (4.44)$$

and $$I_n/I_n' = T_n \qquad (4.45)$$

As before $$\omega_1^2 L_1 C_{1t} = 1 \qquad (4.46)$$

and $$\omega_1^2 L_1 C_1 = E_1 \qquad (4.47)$$

where C_{1t} = C_1 in series with C_{o1}", the latter being the capacitance formed by C_o shunted by X_n at ω_1.

Similar equations apply at ω_n. The parameters are now given by:

$$T_1 = \alpha_1(1 - 1/E_1) \qquad (4.48)$$

$$T_n = \alpha_n(1 - 1/E_n) \qquad (4.49)$$

E_1 and E_n are given for the case of an X2 multiplier in Appendix 4.2 as functions of C_o/C_1 and C_o/C_n. The two power loss expressions are as follows:

Lossy diode case,

$$\frac{1}{\eta} = \left[1 + \frac{\alpha_n C_o R_{nt}}{n^2 K^2 Q_{dn}} \frac{1}{T_n^2}\right] \Bigg/ \left[1 - \frac{1}{Q_{nd}} \frac{1}{\alpha_n C_o R_{nt}} T_n^2\right] \qquad (4.50)$$

Lossy filter case,

$$\frac{1}{\eta} = \left[1 + \frac{1}{K^2 n}\left[\frac{\alpha n}{Q_n}\right]\left[\frac{\alpha_1}{Q_1}\right]\left[\frac{Q_n}{Q_{nt}}\right]\frac{1}{T_1^2 T_n^2}\right] \Bigg/ \left[1 - \frac{Q_{nt}}{Q_n}\right] \qquad (4.51)$$

It is apparent that these expressions are modified in exactly the same way as those for the node circuit, and, as one would expect, the general behaviour for an X2 stage is the same.

4.3.3. Modification of filter 'Q' factors due to coupled losses.

It is apparent from the basic node and mesh circuits shown in Fig.4.1, (a) and Fig.4.1, (c) that if C_n is of the same order as C_o and G_o (or R_o) is of the same order as the reactance of L_nC_n at ω_1 then G_o (or R_o) will effectively constitute a loss at the input frequency. This effect also occurs due to the generator conductance G_g (or resistance R_g) causing a loss at the output frequency. For a given circuit these additional losses may be taken into account by defining at ω_1 a 'Q' factor Q_{1c} and at ω_n a 'Q' factor Q_{nc} where Q_{1c} and Q_{nc} are due to the conductances (or resistances) at the alternate nodes (or meshes). These quantities may be simply evaluated in terms of the circuit parameters α_1, α_n, E_1, E_n and the loaded input and output 'Q' factors, Q_{1t} and Q_{nt} (where Q_{1t} is the 'Q' factor obtained by including the effect of the generator conductance (or resistance) at ω_1. The node circuit may be treated as follows:

The impedance Z seen at the input node looking towards the output node may be written thus:

$$Z = \frac{1}{j\omega_1 C_o} + \frac{j\omega_1 L_n/G_{nt}}{j\omega_1 L_n + (1 - E_n/n^2)/G_{nt}} \qquad (4.52)$$

This gives the effective conductance G, at the input node,

$$\text{i.e.} \quad G = \frac{Q_{nt}/\alpha_n n^3}{Q_{nt}^2(1 - E_n/n^2 - 1/\alpha_n n^2)} \qquad (4.53)$$

$$\text{hence } \frac{Q_{1c}}{Q_{nt}} = \alpha_1 \alpha_n n^3 \left[(1-E_n/n^2-1/\alpha_n n^2)^2 + 1/n^2 Q_{nt}^2\right] \qquad (4.54)$$

Similarly

$$Q_{nc}/Q_{1t} = \left[\alpha_1 \alpha_n/n^3\right]\left[(1-n^2E_1-n^2/\alpha_1)^2 + n^2/Q_{1t}^2\right] \qquad (4.55)$$

These two quantities are plotted in Fig.4.12 for the case of $\alpha_1 = 2\alpha_2$ for an X2 node multiplier.

The results for an X2 mesh multiplier are similarly obtained and are as follows:

$$Q_{1c}/Q_{2t} = \left[2\alpha_1/\alpha_2\right]\left\{\left[1+\alpha_2'(1-E_2/4)\right]^2+(\alpha_2/2Q_{2t})^2\right\} \quad (4.56)$$

$$Q_{2c}/Q_{1t} = \left[\tfrac{1}{2}\alpha_2/\alpha_1\right]\left\{\left[1+\alpha_1'(1-4E_1)\right]^2+(2\alpha_1/Q_{1t})^2\right\} \quad (4.57)$$

Let us now consider the effect of these coupled losses in a node circuit. It is apparent from Fig.4.12 that the performance is affected most seriously at low values of α_1 and α_n. This is of course what one would expect since the two nodes are in effect tightly coupled under conditions where the capacitance of the diode is comparable to the node capacitance. Consider for example the case of $\alpha_1 = 4$: $Q_{2c}/Q_{1t} = 7.5$; this means that if the value of Q_{1t} is 10, the effective 'Q' factor of the output filter will be, at the most, 75. To determine the actual value of Q_2 to be used in the power loss expression, (4.7) , it is necessary to take the combined value of the filter 'Q' factor Q_2 'in parallel' with Q_{2c}. Since in general the loaded values of 'Q' factor will be quite low if the filters are lossy (since it is necessary for reasonable efficiency to 'swamp' the filter losses) it is apparent that the efficiency may in some cases be seriously limited. Note also that the efficiency is reduced by another effect for the case of lossy filters as mentioned in sect.4.2.3, when the value of α is increased. When using the simple circuit there is therefore an optimum value of α under these conditions. Note however that when the filters are lossless (i.e. the diode losses dominate the behaviour) the above coupled losses , although still present, can be made negligible by using sufficiently high values of α .

It is apparent that the mesh circuit will behave in a very similar manner. Note that under conditions where α_1 and α_n are large, the expressions for both types of circuit become simplified as follows (comparing the X2 circuits):

Node circuit.

$$Q_{1c}/Q_{2t} = (9/2)\,\alpha_1\,\alpha_2 \tag{4.58}$$

$$Q_{2c}/Q_{1t} = (9/8)\,\alpha_1\,\alpha_2 \tag{4.59}$$

Mesh circuit:

$$Q_{1c}/Q_{2t} = (9/8)\,\alpha_1\,\alpha_2 \tag{4.60}$$

$$Q_{2c}/Q_{1t} = (9/2)\,\alpha_1\,\alpha_2 \tag{4.61}$$

The above equations are approximately valid for $\alpha_1 = \alpha_n = 5$ and the error becomes negligible for values of $\alpha \gg 10$. Using the above forms it is possible to see whether the coupled losses are comparable to the filter losses, i.e. whether or not they must be considered in a particular case.

4.3.4. Conclusions.

It has been shown above that the finite reactance of the filters may cause severe restrictions to the efficiency that may be obtained using the basic circuits. As has already been mentioned in sect. 2.4.1 and sect. 4.2.3 it is always possible to overcome these effects by the use of additional filters as in Fig.4.1 ,(b) and Fig.4.1,(d). Whether or not the extra circuitry is necessary may be decided from the above results. As an example of the operation with and without the additional filters refer to the results for an X2 multiplier given in Fig.4.13. Curve (b) corresponds to the case where the filters are lossless and shows that under this

condition it is desirable to make α_1 and α_n large. As pointed out in sect.4.2.3. the efficiency decreases for large values of α, whilst at low values of α the efficiency decreases due to the effects discussed in sect.4.3.2 and sect. 4.3.3. As is clearly seen from curve (c) the maximum efficiency can be greatly improved (in this case of $Q_1=Q_2=100$) by the use of additional filters. It must of course be remembered that these filters will possibly introduce losses themselves and their use therefore is most advantageous when the circuit is designed with low values of α. Note also that the minimum value of α_1 will be limited by C_a (referring to Fig.4.1,(b)) and it is therefore necessary to make $C_a \ll C_1$. It has been assumed in calculating curve (c) that the additional filters are lossless and that the reactance requirements can be satisfied.

4.4 Harmonic losses due to finite loaded 'Q' factor of input and output circuits.

4.4.1 Introduction.

So far we have only considered losses which occur at either the input or the output frequencies. The 'Q' factors of both the input and the output circuits are finite under practical conditions, due to the presence of the generator and the load conductances. This means that harmonic power will be dissipated in both the generator and the load conductances (referring to the basic circuit of Fig.4.1,(a)). Note that this loss could come under the heading of sect.4.3 since the 'Q' factor is related to the reactance present in the circuit. The loss is however directly related to the 'Q' factor as such and is thus more readily treated by a separate analysis. Since all the harmonics in the mesh circuit other than the second are small compared to the fundamental, the present loss need not be considered as serious in the X2 mesh multiplier. The following analysis will therefore only be carried out for the mode multiplier.

4.4.2 Analysis of mode circuit losses.

Refer to Fig.4.1,(a) and define I_{nh} as the current at a frequency $h\,\omega_1/2\pi$ flowing in G_o and I_{1h} as the current at the same frequency flowing in G_g. I_h is defined as the harmonic current flowing through the diode. In estimating the following losses it will be assumed that the filters are lossless, i.e. both G_1 and G_n are neglected.

The fraction of the diode harmonic current which flows in each conductance may be found simply by considering the susceptance at each node. Thus the susceptance at the input node Y_1 is given by :

$$Y_1 = G_g \left[1 + jhQ_{1t}E_1(1 - 1/h^2E_1) \right] \tag{4.62}$$

whence $I_h/I_{1h} \doteq hQ_{1t}E_1(1 - 1/h^2E_1)$ (4.63)

Similarly $Y_n = G_o \left[1 + j(h/n)Q_{nt}E_n(1 - n^2/h^2E_n) \right]$ (4.64)

whence $I_h/I_{nh} \doteq (h/n)Q_{nt}E_n(1 - n^2/h^2E_n)$ (4.65)

In the above equations E_1 and E_n are the parameters defined by (4.28) and (4.34) and Q_{1t} is due to the generator conductance as in sect.4.3.3.

The harmonic current through the diode is given by an expression similar to (2.18). Thus:

$$i_h = C_o \sum_{m=h-1}^{\infty} c_m v_d^m \frac{dv}{dt} \tag{4.66}$$

where the summation extends over all terms contributing to current at $h\omega_1$. I_h is the modulus of i_h and may be expressed in a form similar to (2.20) thus:

$$I_h = K_h \omega_1 C_o V_1 \tag{4.67}$$

The power loss due to the harmonic currents may now be evaluated. Consider the loss at the output node due to a harmonic at $h\omega_1$:

$$P_{out} = I_n^2/G_o \tag{4.68}$$

$$P_{dis} = I_{nh}^2/G_o \tag{4.69}$$

where P_{dis} is the power dissipated at the harmonic frequency. The power loss given by (Total power/Output power) is thus:

$$1/\eta_o = 1 + (I_{nh}/I_n)^2 \qquad (4.70)$$

(I_n is the current defined by (2.20)).

The loss at the input mode may be expressed in a similar form as follows: Assume that the input matching conditions are given by $G_g = G_{eq}$ (see (4.2)), i.e. the harmonic losses are neglected when matching the input (this approximation is generally justifiable since, as will be shown, the harmonic losses are small). Under these conditions the total input power P_{in} is:

$$P_{in} = V_1^2 G_g + I_{1h}^2/G_g \qquad (4.71)$$

and the 'useful' input power P_{in}' is:

$$P_{in}' = V_1^2 G_g \qquad (4.72)$$

the power loss is thus given by:

$$1/\eta_1 = 1 + (I_{1h}/V_1 G_g)^2 \qquad (4.73)$$

Combining the power loss at both modes, we get the total power loss for a given harmonic, $1/\eta_t$:

$$1/\eta_t = \left[1 + (I_{1h}/V_1 G_g)^2\right]\left[1 + (I_{nh}/I_n)^2\right] \qquad (4.74)$$

or, assuming that the losses are small, we get:

$$(1/\eta_t) = 1 + (I_{1h}/V_1 G_g)^2 + (I_{nh}/I_n)^2 \qquad (4.75)$$

The total loss due to all harmonics is:

$$\sum (1/\eta_t) = 1 + \sum_h \left[(I_{1h}/V_1 G_g)^2 + (I_{nh}/I_n)^2\right] \qquad (4.76)$$

summed over values of 'h' other than h=1 and h=n.

Using (2.20), (2.77) and (4.5) this loss may be expressed in the form:

$$\frac{1}{\eta t} = 1 + \sum_{h} \left[\frac{I_h}{I_n} \frac{n}{h} \frac{1}{Q_{nt}} \right]^2 \left\{ \left[\frac{(V_n/V_1)(\alpha_n/\alpha_1)}{E_1(1-1/h^2 E_1)} \right]^2 + \left[\frac{1}{E_n(1-n^2/h^2 E_n)} \right]^2 \right\} \tag{4.77}$$

It is thus possible to evaluate the harmonic losses for any particular circuit. Direct comparison of different multipliers is difficult using (4.77) due to the presence of several independent parameters. It is possible however to compare various multipliers on a simple basis for the case where $V_n \ll V_1$, since under this condition the loss expression simplifies to:

$$\frac{1}{\eta t} = 1 + \sum_{h} \left[\frac{K_h}{K} \frac{n}{h} \frac{1}{Q_{nt}} \right]^2 \left[\frac{1}{E_n(1 - n^2/h^2 E_n)} \right]^2 \tag{4.78}$$

Note that this is simply the loss at the output node, this being the dominating harmonic loss when $V_n \ll V_1$. It is worth noting that this condition generally holds for an optimized circuit where the diode losses dominate (see Figs. 2.13 to Fig. 2.17 and Fig. 2.4); it is thus of particular interest. Note that in (4.78), 'K' is given by (2.22) and

$$K_h = \sum_{m} \frac{1}{2}\, {}^{m}\triangle_{h+1}^{h-1}\, c_m\, V_{dl}{}^{m} \tag{4.79}$$

which is the expression for K (where h = n) obtained in sect. 2, for $V_n \ll V_1$.

4.4.3 Illustration of node circuit losses.

To illustrate the effect of these harmonic losses, consider the case of a circuit designed for optimum operation using a diode with $Q_{dm} = 100$. The values of the parameter $G_{nt}/\omega_n C_o$ may be found from Fig.2.14 for an X2 multiplier ($\gamma = 1/2$) and it is seen that a value of 0.8 gives optimum efficiency. The value of V_1/V_b is thus determined from Fig.2.13 and V_n/V_1 from Fig.2.4 or Fig.2.5. On the assumption that $V_n \ll V_1$ the value of K may be found from Fig.2.6 and the value of K_h for h = 3 and h = 10 are given by the relevant 'K' curves for the X3 and X10 multipliers. A good approximation to K_h for other values of h may be obtained by interpolation. On this basis the loss given by (4.78) may be evaluated as a function of Q_{nt}, assuming that α_n is large enough to make E_n constant and equal to unity. The loss evaluated in this manner is given in Fig.4.14 for a diode in which $V_b' = 0.95V_b$, and $\gamma = 1/2$ for the three orders of multiplier previously considered.

As is to be expected, the losses at frequencies lower than the output frequency dominate due to the fact that the co-efficients c_m in (4.79) increase with decreasing harmonic number; i.e. for harmonics between the 1st. and the nth. the factor K_h/K is greater than unity., This accounts for the fact that the losses for the X2 multiplier are small compared to those for the X3 multiplier, since in the latter case it is mainly the second harmonic which causes the loss. In fact the calculation of the losses is made very simple by the rapid decrease in loss from harmonics higher than the nth., and values of h greater than (n+3) were not considered in estimating the losses given in Fig.4.14.

It is important to note that the results given by the solid curves are based on the assumption that the losses dealt with in sect.4.3 have been eliminated by the inclusion

of additional filters as discussed in sect.4.3.4. and as shown in Fig.4.1,(b). The effects of these filters at frequencies other than their resonant frequency has been neglected on the basis that they are of necessity high 'Q' circuits and that they were designed to have minimum 'secondary' effects on the basic circuit, i.e. for the output node, C_b will be small compared to C_n. For the case where α_1 and α_n are large and the additional filters of Fig.4.1,(b) are omitted, there will be the loss of sect. 4.3.3. to take into account. Under these conditions this loss may be treated alternatively by the present analysis using the first term of (4.77) for h = n and the second term for h = 1. Including this loss (as before, only the loss due to fundamental current in the output circuit need be considered in most cases) gives the broken curve of Fig.4.14. As would be expected, the effect is most pronounced in the X2 multiplier, the loss being increased by a factor of about 15, whereas in the X3 case the loss is approximately doubled.

Let us now consider the effect of the harmonic losses relative to the diode losses of sect.2. For the case considered in Fig.4.14 of $Q_{dm} = 100$, the diode losses (obtained from Fig.2.18) are as follows:

X2 multiplier diode loss = 0.4 dB
X3 multiplier diode loss = 0.9 dB
X10 multiplier diode loss = 10.5 dB

The respective harmonic losses for the case of Q_{nt}=10,using the basic circuit (given by the broken curve of Fig.4.14) are:

X2 multiplier harmonic loss = 0.24 dB
X3 multiplier harmonic loss = 0.66 dB.
X10 multiplier harmonic loss = 8.60 dB

It is thus apparent that in this case the harmonic loss will seriously degrade the performance of a multiplier.

For values of Q_{nt} greater than 10, (note that the upper limit is determined by the filter losses) and values of Q_{dm} less than 100 the effect of the harmonic losses becomes increasingly negligible. The respective harmonic losses for the case of Q_{nt}=10, using the circuit of Fig.4.1,(b), (given by the solid curve of Fig.4.14) are:

X2 multiplier harmonic loss = 0.015 dB
X3 multiplier harmonic loss = 0.34 dB
X10 multiplier harmonic loss = 6.50 dB

In this case the results for the X3 and the X10 multipliers are slightly improved. The loss for the X2 circuit is greatly reduced and for the case under discussion is negligible compared to the diode loss.

The above results show that the losses due to the finite 'Q' factor of the input and output circuits are in some cases serious and will restrict the maximum obtainable efficiency unless eliminated by additional filtering. It has been shown that the loss may be almost completely eliminated in a X2 multiplier by the addition of the filters shown in Fig.4.1,(b). Note that since it is often the loss at the output node (at the fundamental frequency) which dominates, the addition of only one series filter (i.e. the one at the output node) may be sufficient to make the loss negligible. It is worth noting that the loss in higher order multipliers may be eliminated by the addition of series filters resonant at each harmonic but in practice the number of circuits would probably become prohibitive. It should also be noted that the above loss will generally be negligible in intermediate stages of a cascaded multiplier since no 'real' load will exist. This will be discussed further in sect.5.

4.5 Rigorous solution of efficiency for the node circuit under lossy diode conditions.

The derivation of the efficiency expression in sect. 2.3.1 is based on the fact that the diode loss resistance may be replaced by an equivalent shunt conductance at both the input and output frequencies as mentioned in sect. 2.4.1. The approximations involved are not immediately obvious and it is the purpose of the present section to derive an exact solution for power loss. It will be shown that, in fact, the original expression is sufficiently accurate for all practical purposes.

Refer to Fig.1.1.(a), in which the diode is shown in its basic form (with a series resistance R_s) coupling the two nodes. Let the voltage across the diode at ω_n be V_n' and the voltage across the junction (i.e. effectively across the non-linear capacitance) be V_n. The relationship between these two voltages is given by the definition of the 'Q' factor:

$$(V_n'/V_n)^2 = 1 + (1/Q_{dn})^2 \qquad (4.80)$$

The current through the diode at the input frequency consists of a capacitive component and a 'power' component. Using the nomenclature of sect.2, the power loss at the input frequency may be expressed thus:

$$P_{loss}(\omega_1) = I_{1d}^2 R_s$$

$$= (\omega_1 C_{o1}' V_1)^2 R_s + (V_1 G_{eq})^2 R_s \qquad (4.81)$$

By using (2.20) and (2.77) this loss may be written:

$$P_{loss}(\omega_1)=(\omega_m C_o V_n')^2\left\{\frac{1}{K^2}\left[\frac{G_{nt}}{\omega_n C_o}\right]^2\left[\frac{C_{o1}'}{C_o}\right]^2+\left(\frac{K}{n}\right)^2\right\}R_s \quad (4.82)$$

Similarly at the output frequency, the capacitive and the 'power' components of current combine to give a power loss:

$$P_{loss}(\omega_n) = I_{nd}^2 R_s$$

$$P_{loss}(\omega_n) = (\omega_n C_{on}' V_n)^2 R_s + I_n^2 R_s \quad (4.83)$$

This may be expressed thus:

$$P_{loss}(\omega_n) = (\omega_n C_o V_n')^2\left\{\left[\frac{V_n}{V_n'}\right]^2\left[\frac{C_{on}'}{C_o}\right]^2+\left[\frac{G_{nt}}{\omega_n C_o}\right]^2\right\}R_s \quad (4.84)$$

The output power, P_o, may be written thus:

$$P_o = V_n'^2 G_o$$

$$= V_n'^2(G_{nt} - G_{dn}) \quad (4.85)$$

The equivalent conductance of the diode at the output frequency may be expressed thus:

$$G_{dn} = \frac{(\omega_n C_{on}')^2 R_s}{1 + (1/Q_{dn})^2} \quad (4.86)$$

where $Q_{dn} = 1/\omega_n C_o R_s \quad (4.87)$

(4.85) may thus be written in the following form:

$$P_o = (\omega_n C_o V_n')^2\left\{\left[\frac{G_{nt}}{\omega_n C_o}\right]Q_{dn} - \left[\frac{1}{1+(1/Q_{dn})^2}\right]\left[\frac{C_{on}'}{C_{on}}\right]^2\right\}R_s \quad (4.88)$$

The efficiency is thus given as follows:

$$1/\eta = 1 + \left[P_{loss}(\omega_1) + P_{loss}(\omega_n)\right] / P_o \quad (4.89)$$

which, after substituting the above results, gives:

$$\frac{1}{\eta} = \frac{1+\left[\frac{1}{K^2 Q_{dn}}\right]\left[\frac{G_{nt}}{\omega_n C_o}\right]\left[\frac{C_{o1}'}{C_o}\right]^2\left\{1+K^2\left[\frac{C_o}{C_{o1}'}\right]^2\left[1+\left(\frac{K}{n}\right)^2\left(\frac{\omega_n C_o}{G_{nt}}\right)^2\right]\right\}}{1-\left[\frac{\omega_n C_o}{G_{nt}}\right]\left[\frac{1}{Q_{dn}}\right]\left[\frac{C_{on}'}{C_o}\right]^2\left[\frac{1}{1+(1/Q_{dn}^2)}\right]} \qquad (4.90)$$

It is seen that this is in fact similar to the expression given in (2.83) but with some additional terms in both the numerator and the denominator. Let us examine the effect of these additional terms.

The only term to be considered in the denominator is the factor involving $1/Q_{dn}^2$. It is immediately obvious that this factor will have negligible effect until the value of Q_{dn} becomes much less than 10. For $Q_{dn}=3$, the total value of the variable factor in the denominator is decreased by about 10%. This will have the effect of increasing the efficiency slightly compared to the value given by (2.83). In general however it is obvious that this effect can be neglected.

The presence of the new term in the numerator is due to the fact that it is not strictly accurate to replace the diode loss resistance by an equivalent shunt conductance as in sect. 2.3.1. It is seen that the new term involves essentially the factor K^2. Since 'K' is generally considerably less than unity the effect of this factor will be second order. The 'worst' case is the X2 multiplier with $\gamma = 1/2$. Consider the optimum conditions for $Q_{dn}=10$: Fig. 2.14 gives $G_{nt}/\omega_n C_o = 1.0$, which from Fig. 2.13 and Fig. 2.6, gives $K = 0.4$. The value of C_o/C_{o1}' is given by Fig. 2.12. It is seen that the overall effect is to increase the factor in the numerator by about 10%. Remembering that

this is the 'worst' case, (the effect in higher order multipliers will be quite negligible) it is apparent that the results obtained in sect.2 are substantially correct and that the diode series loss resistance may be replaced by an equivalent shunt conductance at both the input and output frequencies without introducing appreciable errors.

4.6. Harmonic loss in series resistance of diode.

In the previous analysis of the diode losses, only the losses at the input and output frequencies were considered. In the node multiplier, current will flow at all harmonic frequencies due to the fact that a short circuit path exists through the filters. This does not occur in the basic mesh circuit since the filters present open circuit paths to all harmonics. The loss due to the harmonic current flowing in the series resistance of the diode will cause the efficiency to be worse than that predicted by (?.83). It is the purpose of this section to estimate this loss and shows how it may be taken into account in determining the efficiency.

The current at a particular harmonic frequency, I_h, is defined by (4.66) and (4.67). The power loss due to this current is given by:

$$P_{loss}(\omega_h) = I_h^2 R_s \qquad (4.91)$$

It may be seen by considering (4.82) and (4.84) that, to a good approximation, the power loss at the input and output frequencies may be expressed thus:

$$P_{loss}(\omega_1)+P_{loss}(\omega_n) = (\omega_1 C_o V_1)^2 R_s + (\omega_n C_o V_n)^2 R_s \qquad (4.92)$$

(second order effects being neglected). This is of course

the loss obtained by considering only the capacitive currents due to V_1 and V_n. Let us consider the ratio of the two losses and call it F_h. Thus:

$$F_h = \frac{P_{loss}(\omega_h)}{P_{loss}(\omega_1) + P_{loss}(\omega_n)} \qquad (4.93)$$

i.e. $$F_h = \frac{K_h^2}{1 + (nV_n/V_1)^2} \qquad (4.94)$$

The evaluation of I_h from (4.66) is tedious for the general case. A good approximation may be obtained as before by taking the case of $V_n \ll V_1$, under which condition K_h is given by (4.79). The ratio of the total power loss at all harmonic frequencies to the basic loss is found by summing F_h over all values of 'h' other than h = 1 and h = n. As mentioned in sect.4.4.3, the values of K_h may in this case be found from the curves of sect.2. for any particular operating condition. Let us consider some typical cases. Take first of all the example considered in sect.4.4.3 of a circuit optimized on the basis of sect.2 for a diode with Q_{dn} = 100.

X2 multiplier, sum of all F_h = 0.024
X3 multiplier, sum of all F_h = 0.097
X10 multiplier, sum of all F_h = 0.114

In calculating the above summations it is only necessary to consider values of 'h' up to about 4 due to the rapid convergence of the series. These results show that for the X2 multiplier the increase in loss is completely negligible and in the case of the X3 and the X10 multipliers the basic loss is increased by about 10%.

Consider now the case of a multiplier designed to

operate under the comdition $V_1/V_b = 0.99$. Since the value of 'K' increases with V_1/V_b increasing, this represents a case where the harmonic losses will be severe. In practice it may not be possible to operate at such a high value of V_1/V_b, due to forward conduction effects; this case may therefore be considered as a limiting 'worst' case. The results are as follows:

X2 multiplier, sum of all F_h = 0.19
X3 multiplier, sum of all F_h = 0.34
X10 multiplier, sum of all F_h = 0.43

These results show that the harmonic losses can be serious, particularly in high order multipliers.

The above results again illustrate the superiority of the X2 multiplier over all others. Note that any particular harmonic loss may be eliminated by the inclusion of a parallel resonant circuit in series with the diode. It is doubtful if this would be worthwhile in practice, however, due to the increase in circuit complexity for a relatively small increase in efficiency.

4.7 Losses due to forward conduction.

4.7.1 Practical effect of driving diode into conduction.

Consider the case of a diode biased for operation in the depletion layer region with a voltage at a single frequency applied across the terminals. It has been assumed in sect.1 and sect.2 that losses due to the diode may be taken into account by defining the 'Q' factor thus:

$$Q = 1/\omega C_D R_S$$

This neglects the losses which occur when current flows in R_S due to conduction when the peak applied voltage exceeds the applied bias voltage. It has already been shown in sect.2 that it is desirable to operate under these conditions, i.e. under conditions where the peak applied voltage is equal to the sum of the applied bias plus the barrier voltage, ψ_D. It is therefore necessary to determine the additional losses which occur and either to incorporate them in the expressions for efficiency (this is most easily done by defining a new expression for the 'Q' factor) or to limit the applied voltage on the basis of the results of the following analysis so that the extra losses are negligible.

4.7.2 Theoretical estimation of losses.

The current through the diode due to an applied voltage V is given by the standard expression:

$$i = I_s (e^{qV/kT} - 1) \qquad (4.95)$$

where I_s is the reverse saturation current

and $kT/q \doteq 26$ mV at room temperature.

For the case shown in Fig.4.15 (a) where a voltage V sinωt

causes the diode to be conducting in the forward direction from time t_1 to time t_2, the current during forward conduction is given by:

$$i = I_s \left(e^{(qV \sin \omega t)/kT} - 1\right) \Big|_{t_2}^{t_1} \qquad (4.96)$$

In general I_s is small: for a silicon diode as used in the experiments described in the preceding sections $I_s \ll 1\,\mu A$. This means that forward current will be small until the applied voltage v is considerably greater than kT/q. A fair approximation to practical conditions can thus be made by assuming an abrupt characteristic as shown in Fig.4.15,(b) where current starts to flow at a point ψ_c somewhere between 0 and ψ_o, (the value of ψ_c being determined by the value of I_s for a particular diode) and assuming that the series resistance R_s is external to the actual junction.

The power loss may now be found as follows:

Power dissipated in R_s = P

where
$$P = \frac{1}{2\pi} \int_{t_1}^{t_2} (V \sin \omega t - V_b'')^2 / R_s \qquad (4.97)$$

where
$$V_b'' = V_B + \psi_c \qquad (4.98)$$

i.e.
$$P = \frac{1}{2\pi} \frac{V^2}{R_s} \left[(1/2+\sin^2 \omega t_1)(\omega t_2 - \omega t_1) - (3/2)\sin 2\omega_1 t_1\right]$$

$$= (V^2/2R_s)p, \text{ say.} \qquad (4.99)$$

The power dissipated in R_s may also be expressed in terms of the effective 'Q' factor, Q_e thus:

$$P = (V/Q_e)^2/2R_s \qquad (4.100)$$

or,
$$Q_e^2 = (V^2/2R_s)/P \qquad (4.101)$$

i.e.
$$Q_e^2 = 1/p \qquad (4.102)$$

Note that this expression for 'Q' is only valid for relatively small excursions of forward drive since it assumes that the diode has still an impedance which is mainly capacitive. An error will also occur due to the fact that R_s is not completely external to the junction and will thus vary as the junction current varies.

At high frequencies it is possible that the diode will exhibit charge storage characteristics. In this case it is probably a closer approximation to assume an abrupt increase in capacitance as shown in Fig.4.15(c). The value for 'p' may now be found as in sect.3 from the equation for I_{ls}(3.11). The above analysis therefore represents an approximation to the actual conditions but it is found to be sufficiently accurate for the purposes of the present investigation.

Values of 'Q' factor for both the low and high frequency cases are plotted in Fig.4.16 for values of V/V_b'' up to 1.3 The experimental results were obtained using a G.E.C.SVC 3 diode at 20 Mc/s. ψ_c was estimated from the measured d.c. conduction characteristic to be 0.5 volts; the applied bias was 1.5 volts thus making $V_b'' = 2.0$ volts. The practical circuit is shown in Fig.4.17. The impedance across R_1 was found by measuring the attenuation across R_g and using the measured value of R_g. It was thus possible to calculate the effective 'Q' factor of the diode under varying conditions of forward conduction. It is seen that although the practical results differ somewhat from the theory, the measure of agreement is sufficient for the above analysis to be used as a first approximation for estimating the 'Q' factor under forward conduction conditions.

4.7.3 Conclusions.

From the preceeding results it is possible to determine the effective 'Q' factor of a diode under given amounts of forward conduction. It is thus possible to estimate the efficiency for a particular depletion layer type multiplier under forward conduction by replacing the original value for 'Q' factor by the value obtained from Fig.4.16. Since, however, the value of Q_e drops rapidly, the effects of increasing V_1/V_b'' above a certain value will be to cause the efficiency due to the depletion layer effect to decrease (this follows since the 'expected' increase due to greater utilization of the depletion layer characteristic is nullified by the decrease in efficiency due to the decreased 'Q' factor). The actual point at which the efficiency will start to decrease depends upon the value of Q_{dn}, since the effect of conduction will not dominate until Q_e is less than Q_{dn}. In most cases it will be possible to accurately predict the performance by limiting the maximum drive to the point where $V_1/V_b'' = (1 + \delta'')$ where δ'' is such that Q_e is still greater than Q_{dn}. In the above discussion the effect of the output harmonic voltage has been neglected. It may be assumed that the conclusions are essentially the same, i.e. that due to the abrupt nature of the decrease in Q_e shown in Fig.4.16 the peak voltage across the junction should be restricted to a value equal to $V_b'' (1 + \delta'')$. Results obtained in practice justify this assumption.

Errors involved in the above theory will be small for circuits in which the power loss due to the diode is small since this implies high values of diode 'Q' factor, Q_{dn}, and hence small values of δ''. Note that the relationship between the parameter V_b' used in preceding sections and the parameters introduced in the above theory is given by:

$$V_b' = (1 + \delta'')(V_B + \psi_c) \qquad (4.103)$$

Prediction of depletion layer efficiency using low 'Q' diodes will be subject to error due to the estimation of δ''. This error will generally be insignificant for low order circuits since the exact value of V_b' is not critical. In high order multipliers the error will become increasingly serious but since, as has already been pointed out, high order depletion layer multipliers become very inefficient when using low 'Q' diodes, this case will not be of interest in practice. If a high 'Q' diode is not available one would normally use a charge storage type multiplier or else a cascaded depletion layer multiplier.

4.8 Effect of stray diode reactances.

4.8.1 Lead inductance.

At very high frequencies the leads of the diode may possess an inductive reactance which is comparable with the diode capacitive reactance at the operating point. The effect of this inductance may be taken into account in the following manner;

Consider first of all the node circuit. Using the nomenclature of (4.25) and (4.26) where V_1, V_n are the junction voltages and V_1', V_n' are the voltages at each mode (for the purpose of this analysis, assume that the filters are ideal, i.e. any reactance presented by the filters will be neglected), we can write the relationships between the voltages as follows:

$$V_1/V_1' = T_1$$
$$= (1 - \omega_1/\omega_o)^{-1} \qquad (4.104)$$

where ω_o is the self resonant frequency of the diode capacitance and lead inductance. Similarly,

$$V_n/V_n' = T_n$$
$$= (1 - \omega_n/\omega_o)^{-1} \qquad (4.105)$$

The efficiency expressions incorporating the factors T_1 and T_n are given by (4.42) and (4.43). Thus the effect when diode losses predominate is to alter the efficiency for any particular case but to leave the maximum obtainable efficiency unaltered. When the filter losses predominate the efficiency would appear to be increased by the presence of series inductance. It must be remembered however that the inductance will be lossy and it is doubtful whether any

improvement would be realised in practice. If one considers the addition of artificial series inductance it is obvious that the efficiency would be increased by the above effect, were it not for the presence of additional loss in the inductance itself. The mechanism involved may be seen as follows: keeping the diode operating conditions the same, the first effect of the added inductance is to let the input voltage be decreased, i.e. the input conductance is increased thus becoming much greater than the loss conductance in the input filter; the limiting condition is when the input consists of a series resonant circuit fed from a low impedance generator in which case the input circuit is the same as for the basic mesh type multiplier. It is thus apparent that the efficiency is again limited, this time by the equivalent series resistance of the inductance.

The presence of stray lead inductance has virtually no effect in the case of the basic mesh type multiplier due to the fact that each mesh is series resonated by the filters and any inductive reactance is automatically tuned out.

4.8.2. Shunt capacitance.

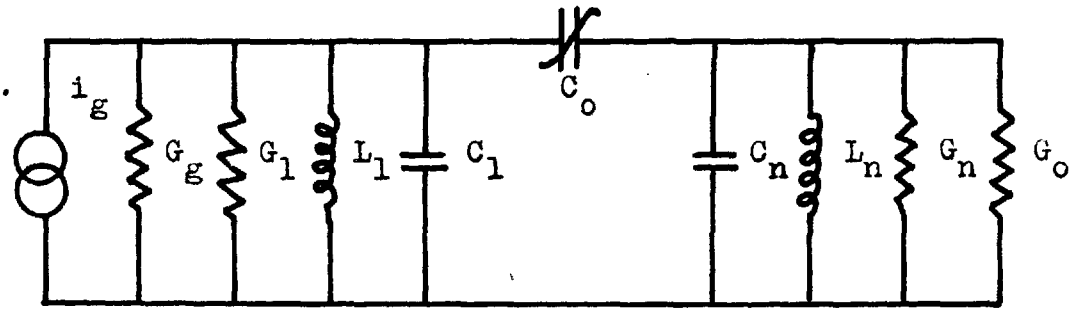
Consider first of all the mesh circuit. Using the same nomenclature as in (4.44) and (4.45), we can write:

$$T_n = T_1 = (1 + C_s/C_o)^{-1} \qquad (4.106)$$

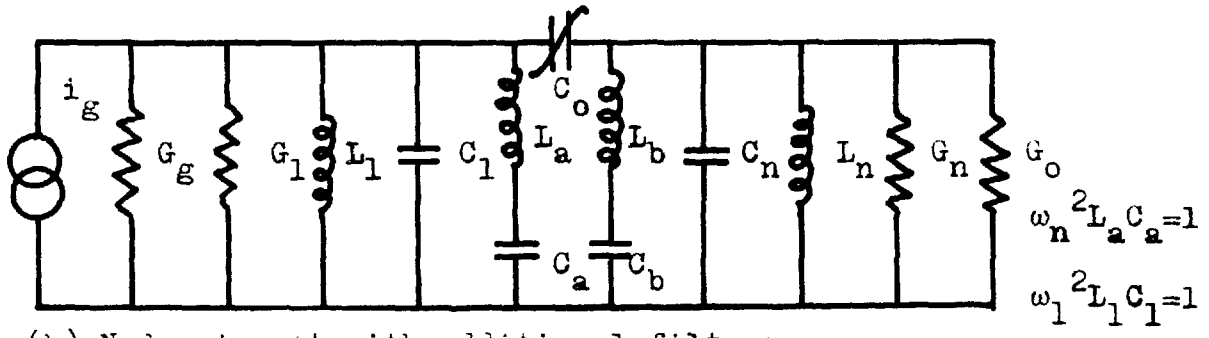
where C_s is the stray shunt capacitance. The conclusions for a lossy diode circuit are as before as can be seen from (4.50). Since T_1 and T_n are in this case less than unity, the efficiency of a multiplier in which filter losses predominate is decreased by the presence of stray shunt capacitance. The effect for any particular value of C_s/C_o may be found from (4.51).

In the case of the node circuit, any stray capacitance is tuned out by the filters and therefore may be neglected in estimating the efficiency.

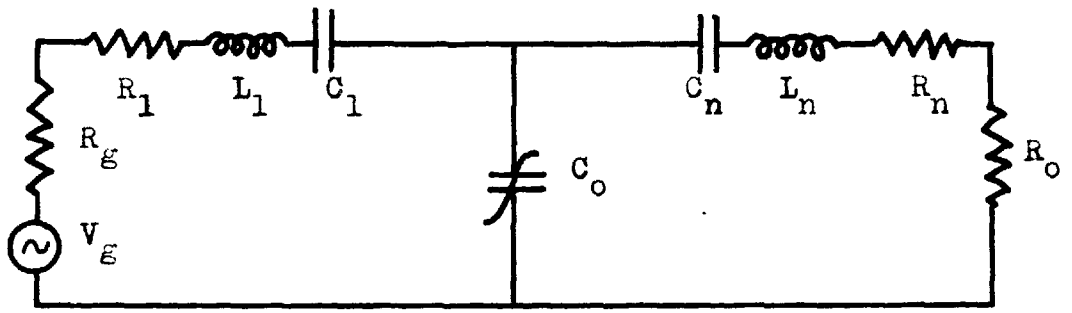
The above theory is based on the same assumption as that made in sect.4.3.2, i.e. that the voltage (in the node circuit) and the currents (in the mesh circuit) divide as if the diode presents an impedance corresponding to its capacitive reactance at the operating point. Since the effect under investigation is normally a second order one, the results obtained should be sufficiently accurate for most purposes.



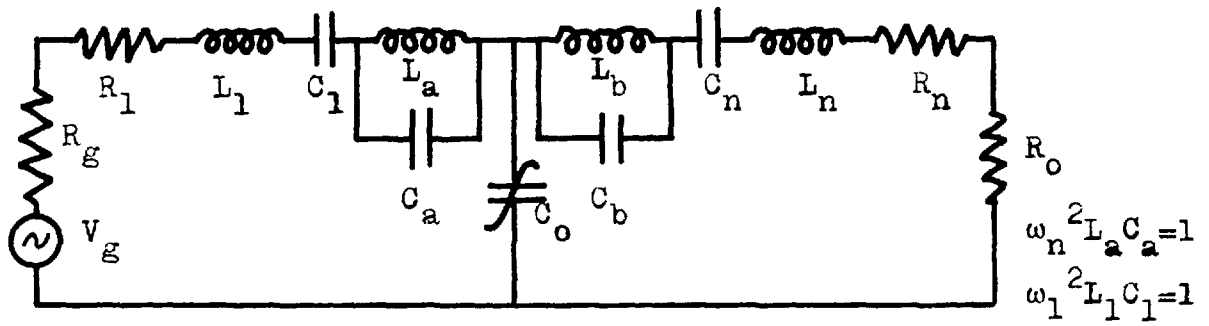
(a) Basic node circuit



(b) Node circuit with additional filters



(c) Basic mesh circuit



(d) Mesh circuit with additional filters.

Fig.4.1 Depletion layer multiplier circuits with lossy filters.

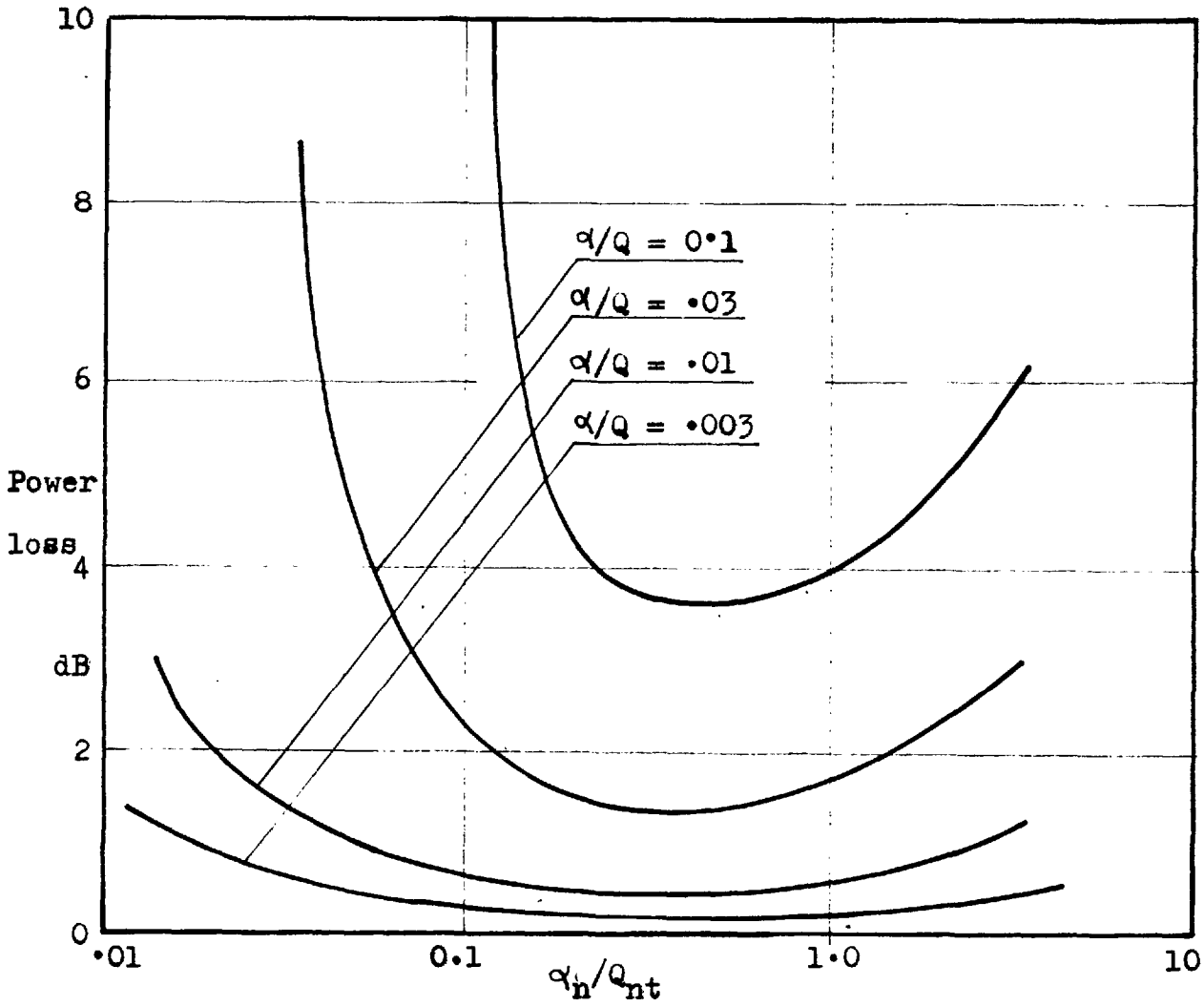


Fig.4.2 Filter loss curves for a X2 node multiplier where $\gamma = 1/2$ and $\alpha_1/Q_1 = \alpha_n/Q_n = \alpha/Q$.

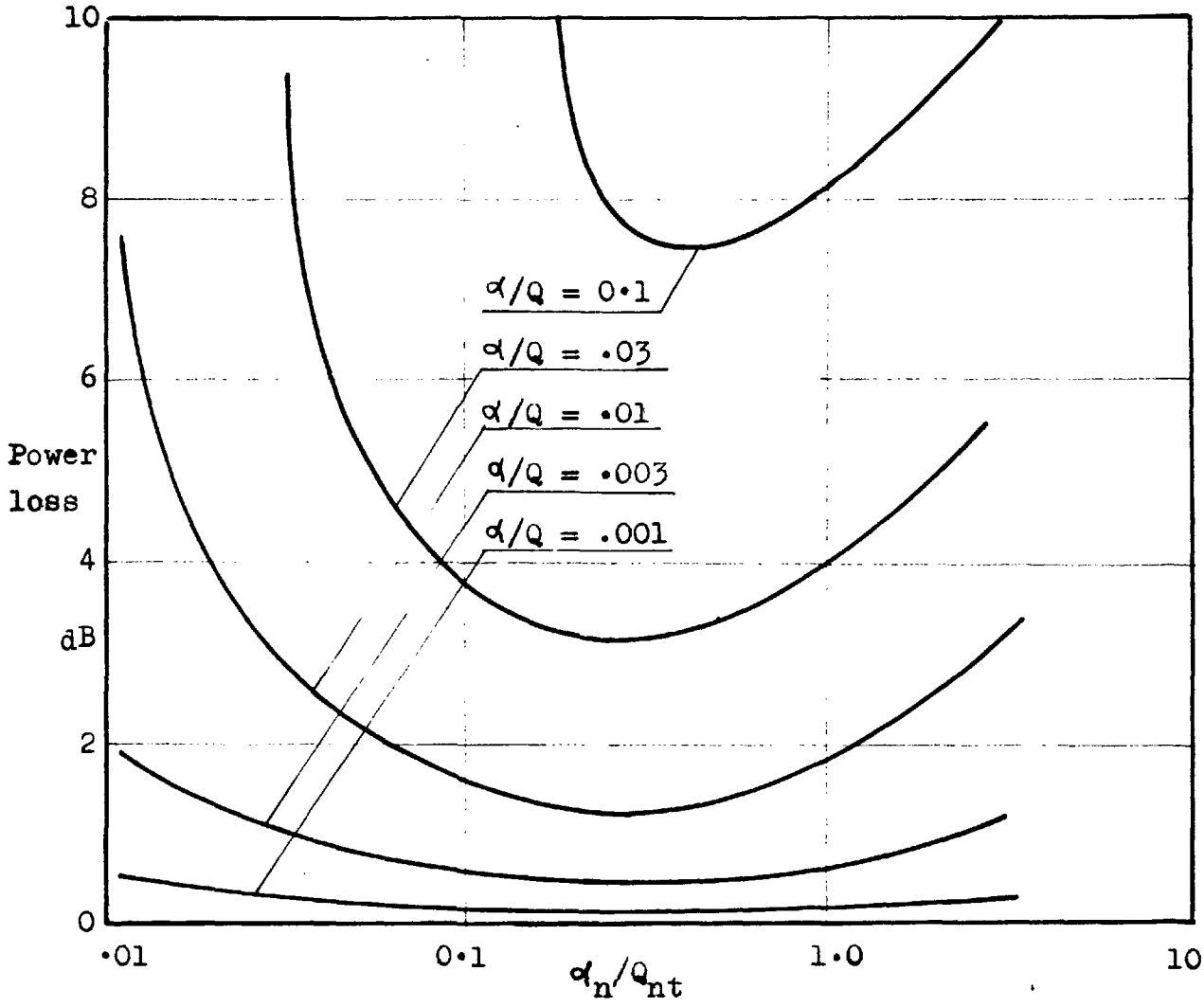


Fig.4.3 Filter loss curves for a X3 node multiplier where $\gamma = 1/2$ and $\alpha_1/Q_1 = \alpha_n/Q_n = \alpha/Q$.

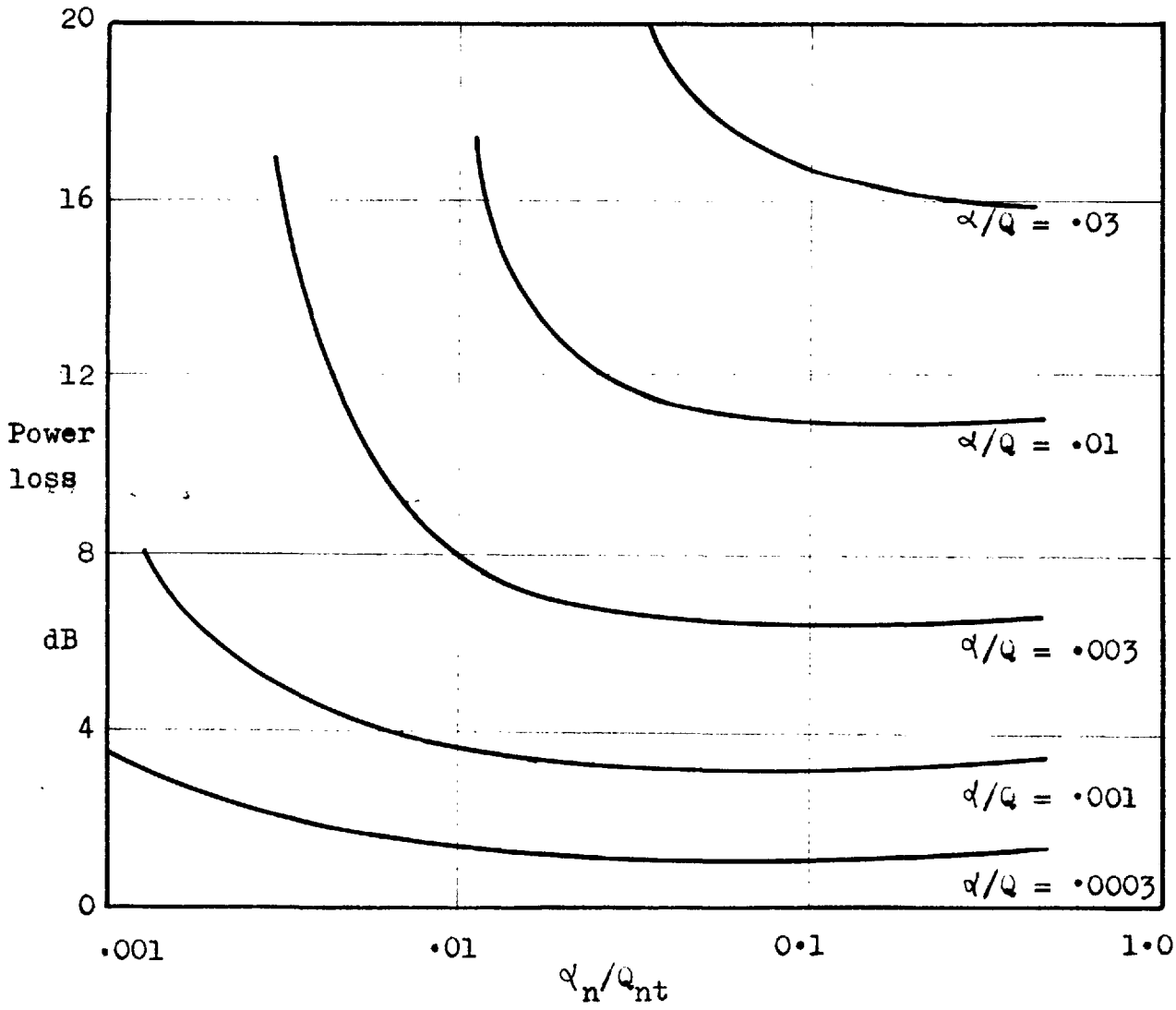


Fig.4.4 Filter loss curves for a X10 node multiplier, $\gamma = 1/2$, $\alpha_1/Q_1 = \alpha_n/Q_n = \alpha/Q$.

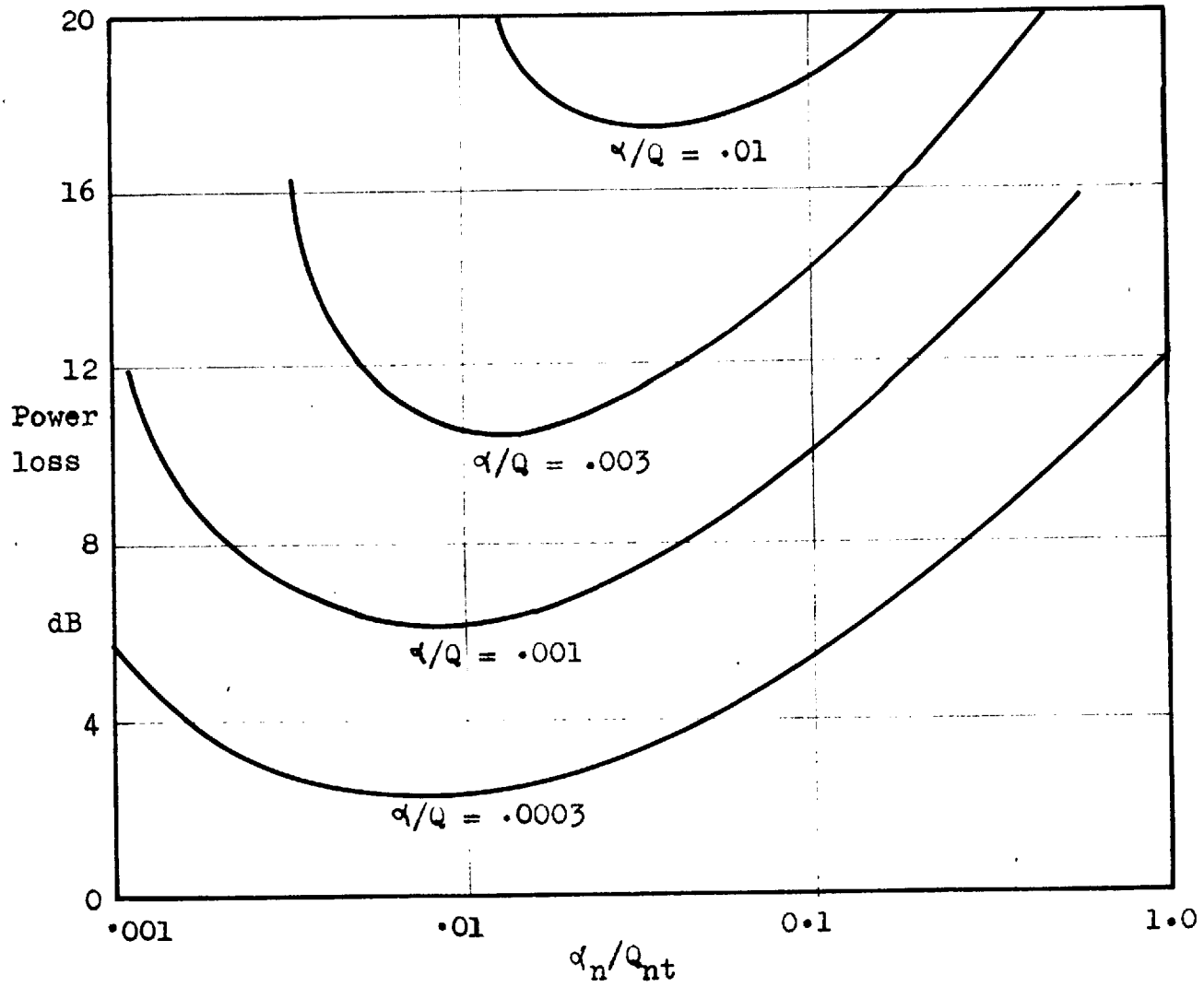


Fig.4.5 Filter loss curves for a X10 node multiplier, $\gamma = 1/2$, $V_b' = \cdot 95 V_b$, $\alpha_1/Q_1 = \alpha_n/Q_n = \alpha/Q$.

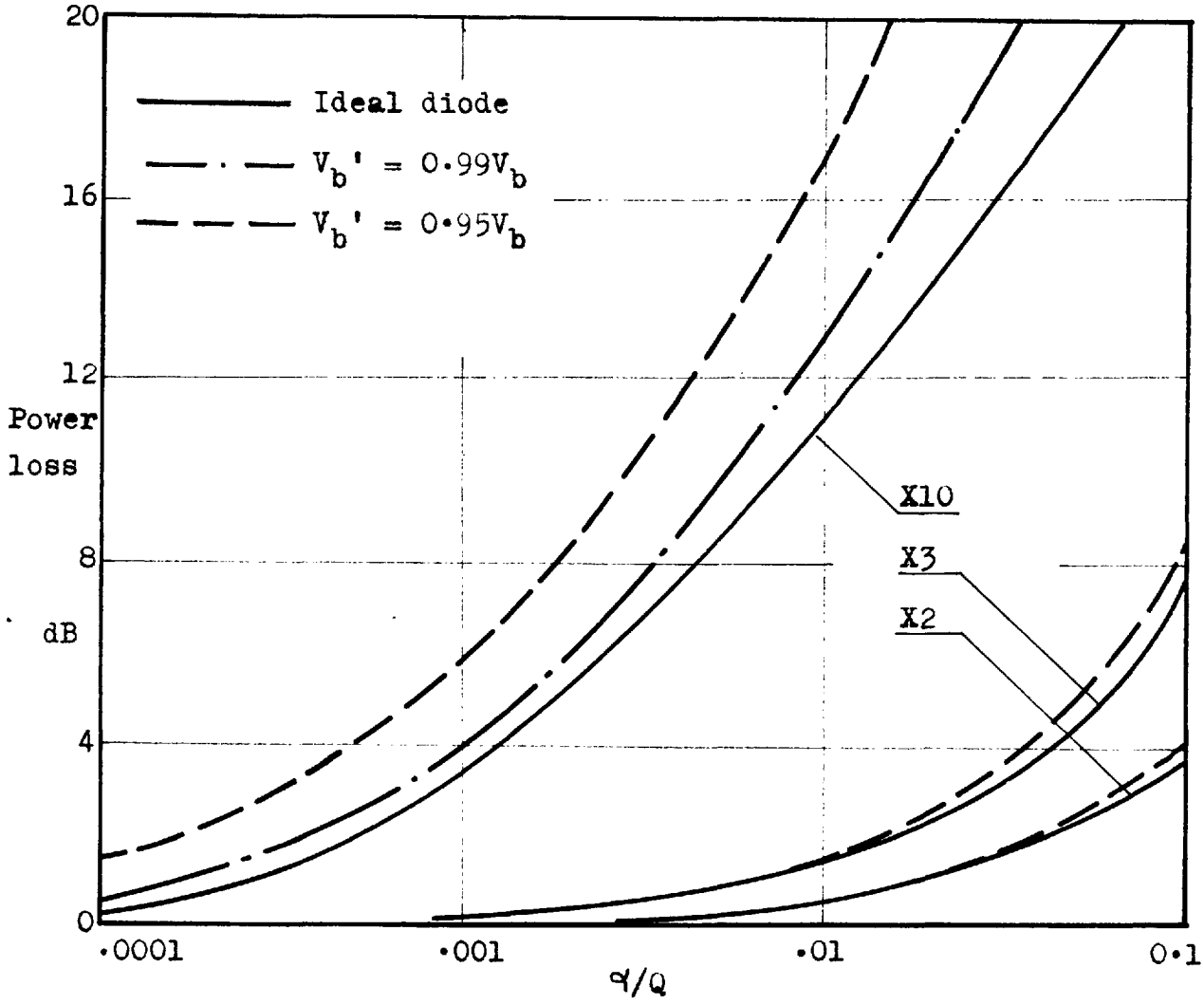


Fig.4.6 Node multiplier curves of minimum power loss for the case where only filter losses exist, evaluated for the case of $q_1/Q_1 = q_n/Q_n = q/Q$ and $\gamma = 1/2$.

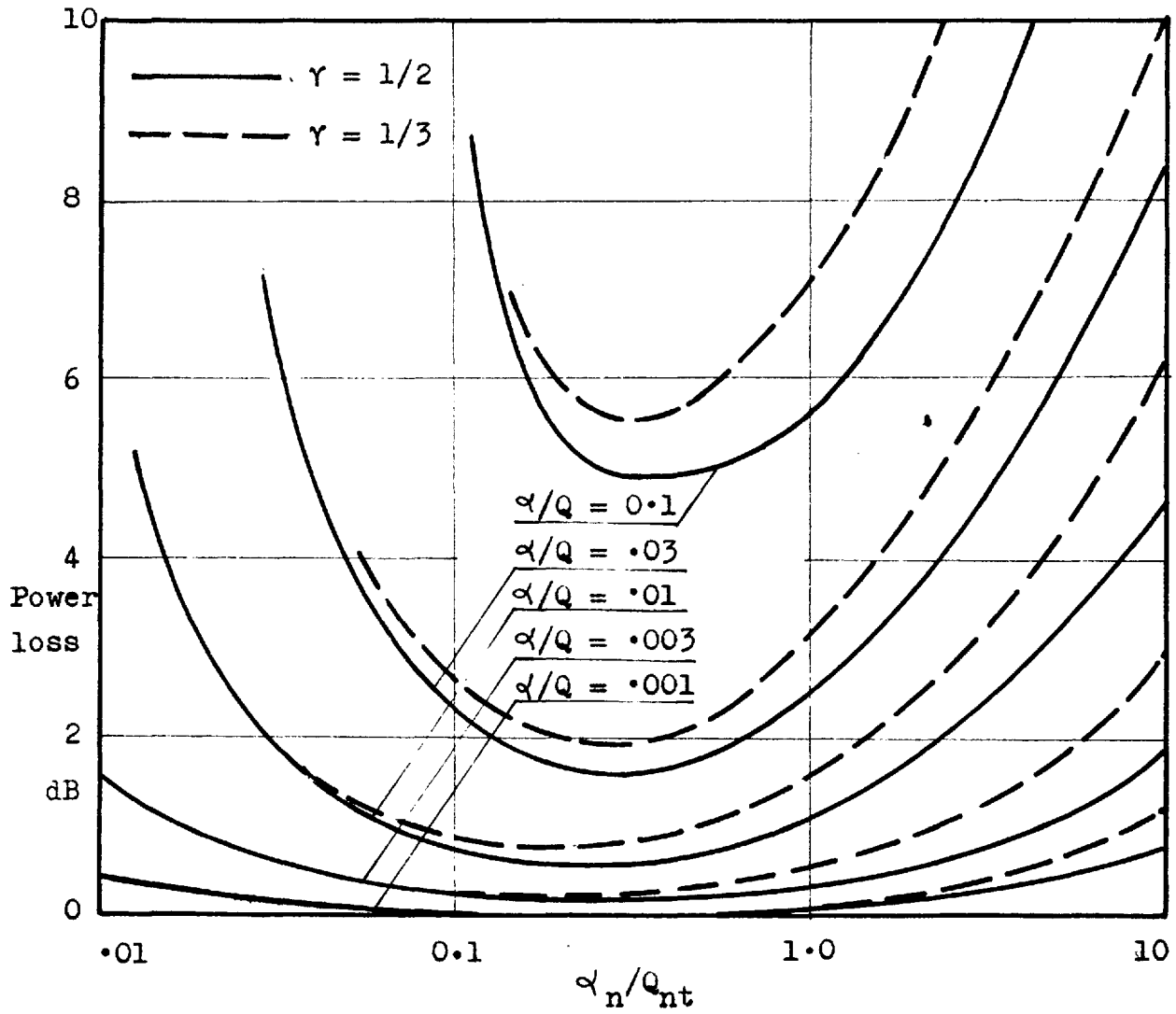


Fig.4.7 Filter loss curves for a X2 mesh multiplier where $\alpha_1/Q_1 = \alpha_n/Q_n = \alpha/Q$.

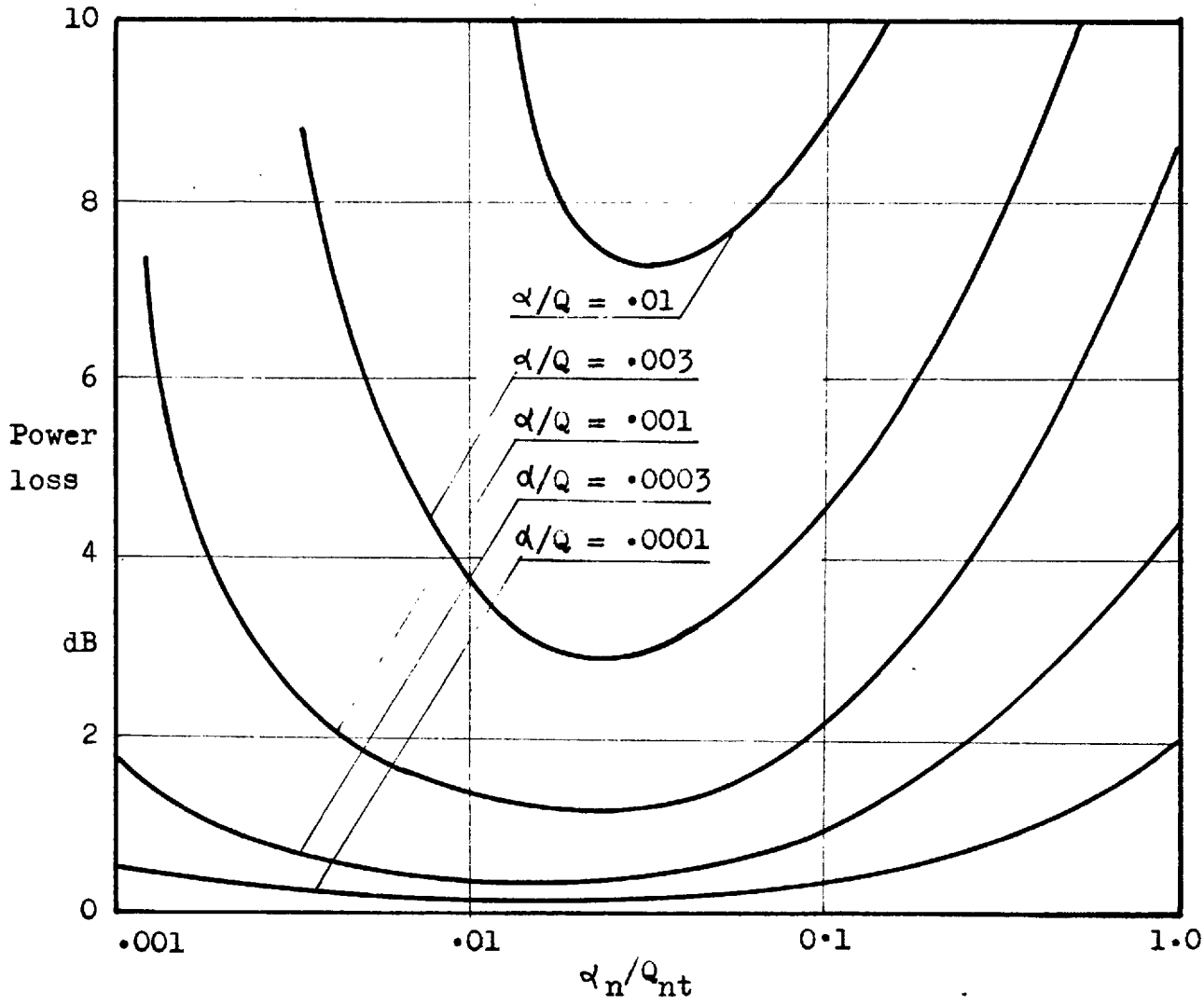


Fig.4.8 Filter loss curves for a X3 mesh multiplier where $\gamma = 1/3$ and $\alpha_1/Q_1 = \alpha_n/Q_n = \alpha/Q$.

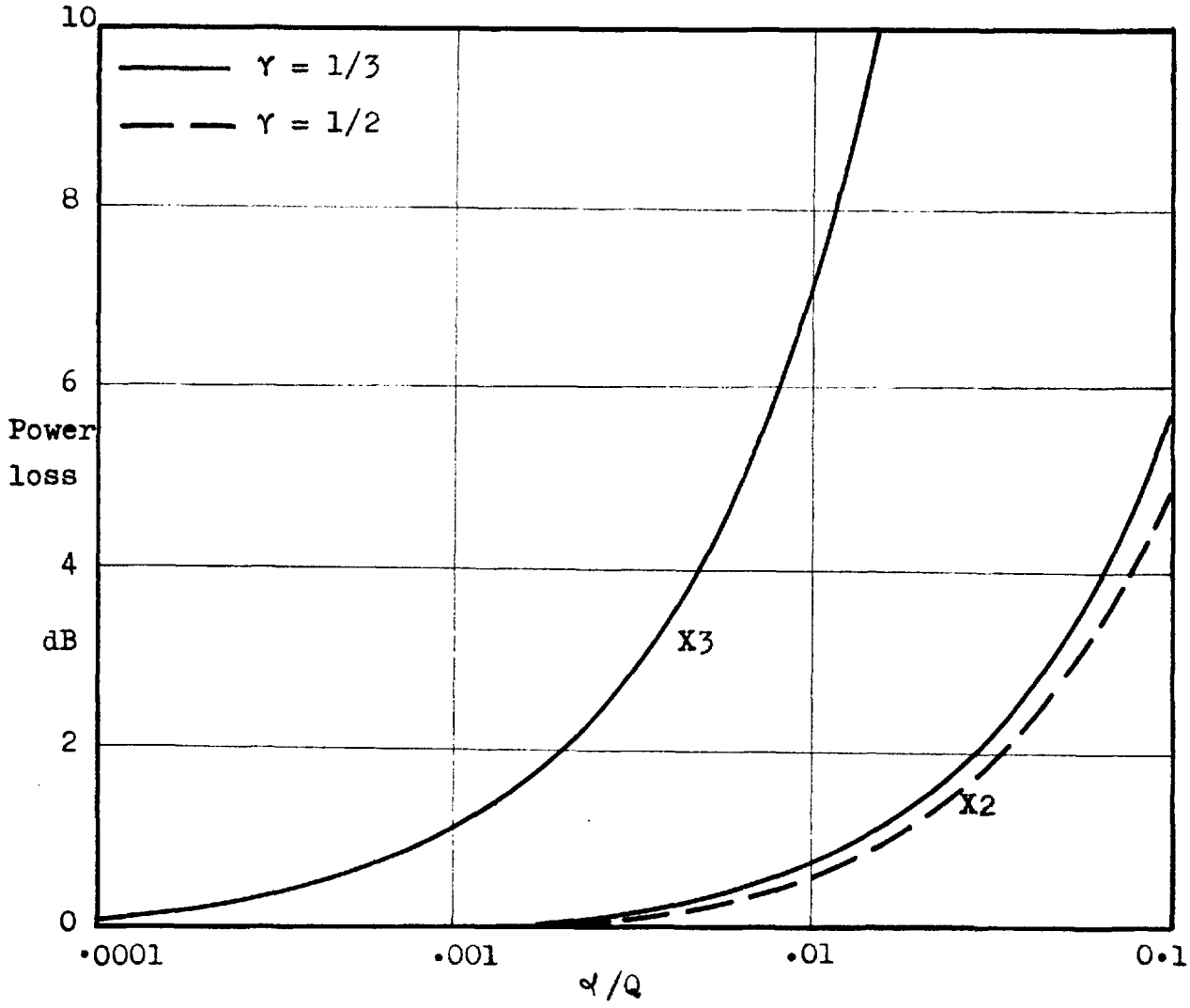
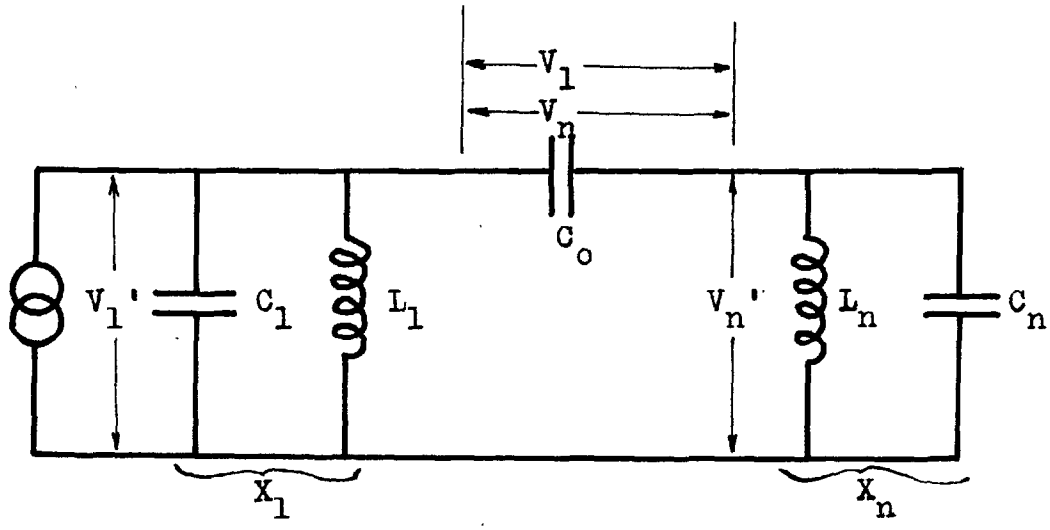
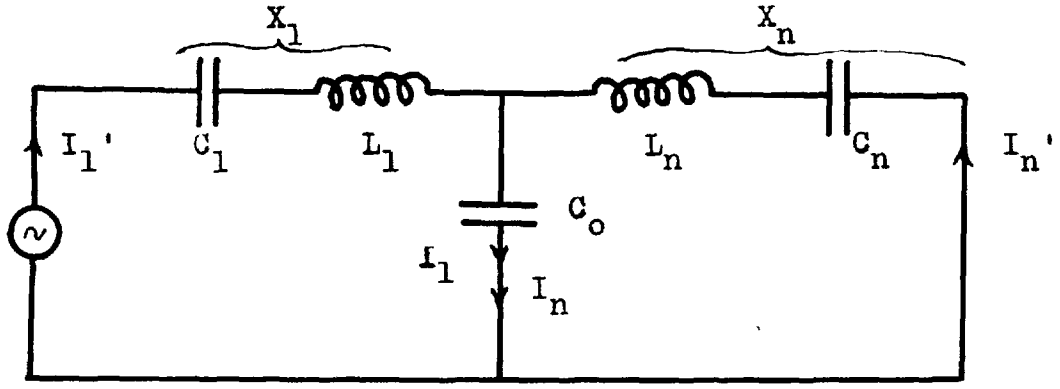


Fig.4.9 Mesh circuit curves of minimum power loss for the case where only filter losses exist, evaluated for the case of $\alpha_1/Q_1 = \alpha_n/Q_n = \alpha/Q$.



(a) Node circuit



(b) Mesh circuit

Fig.4.10 Simplified circuits used to allow for the finite reactance of the filters.

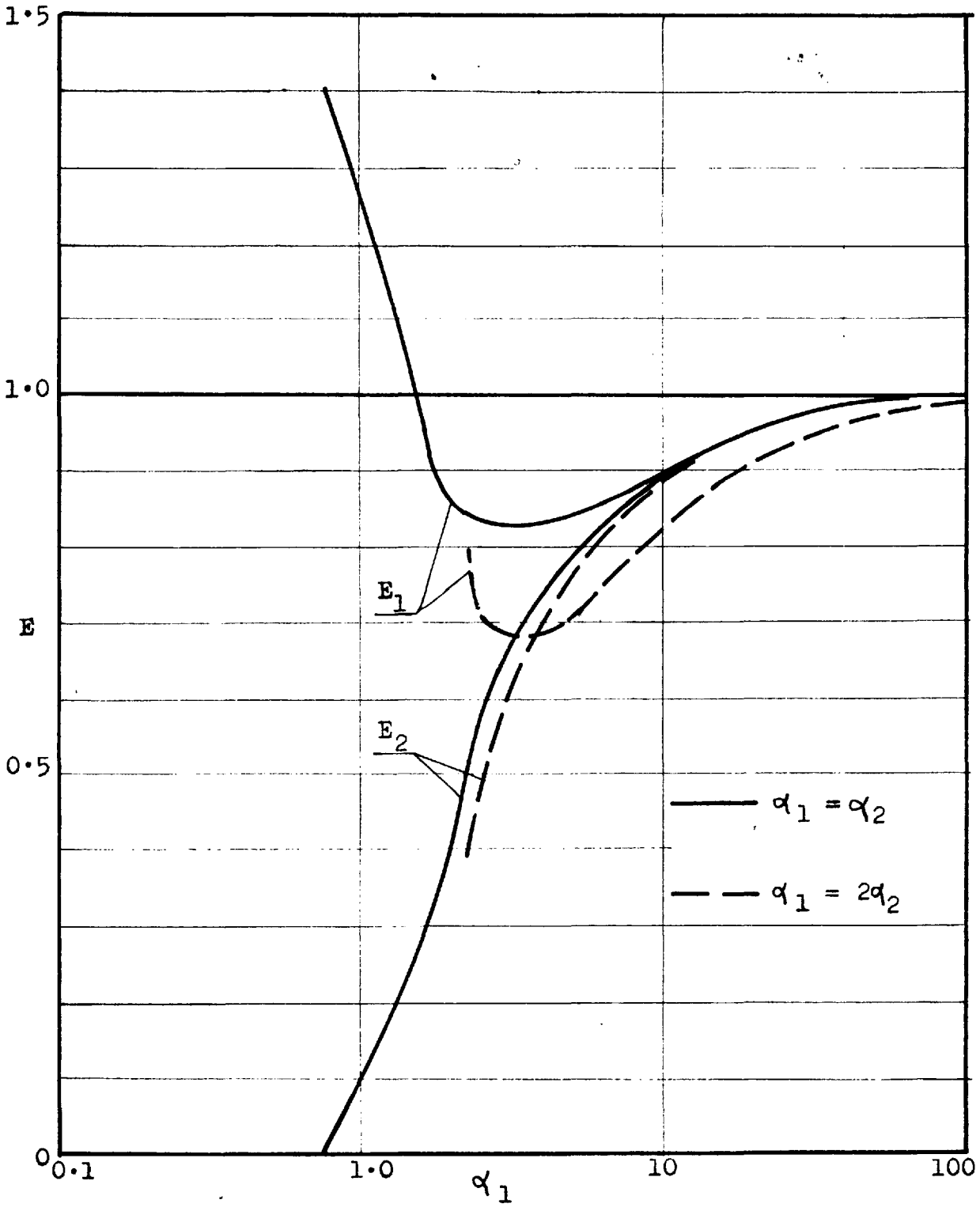


Fig.4.11 'E' curves for a X2 node multiplier circuit.

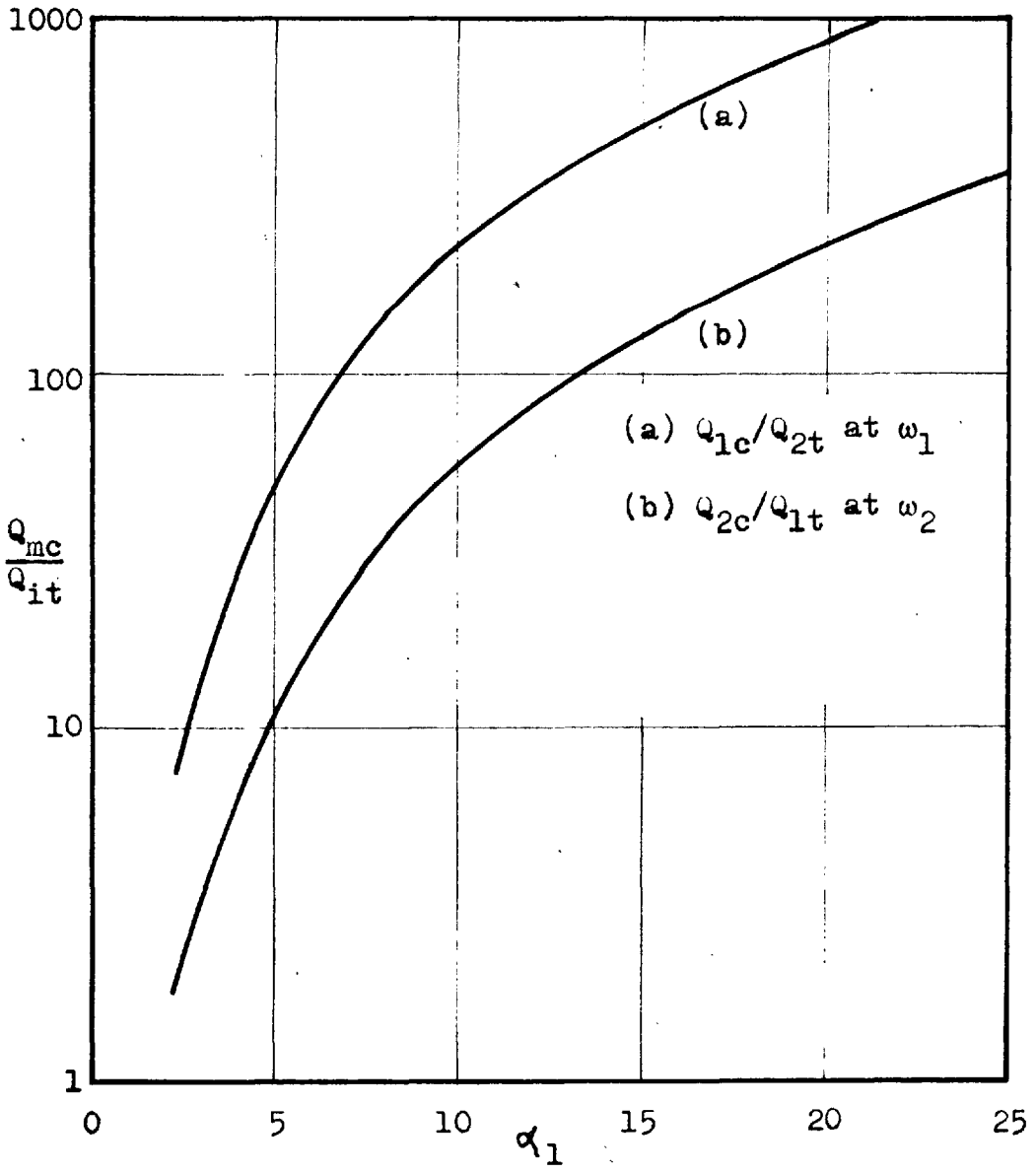


Fig.4.12 Variation of coupled losses in a X2 node multiplier where $\alpha_1 = 2\alpha_2$.

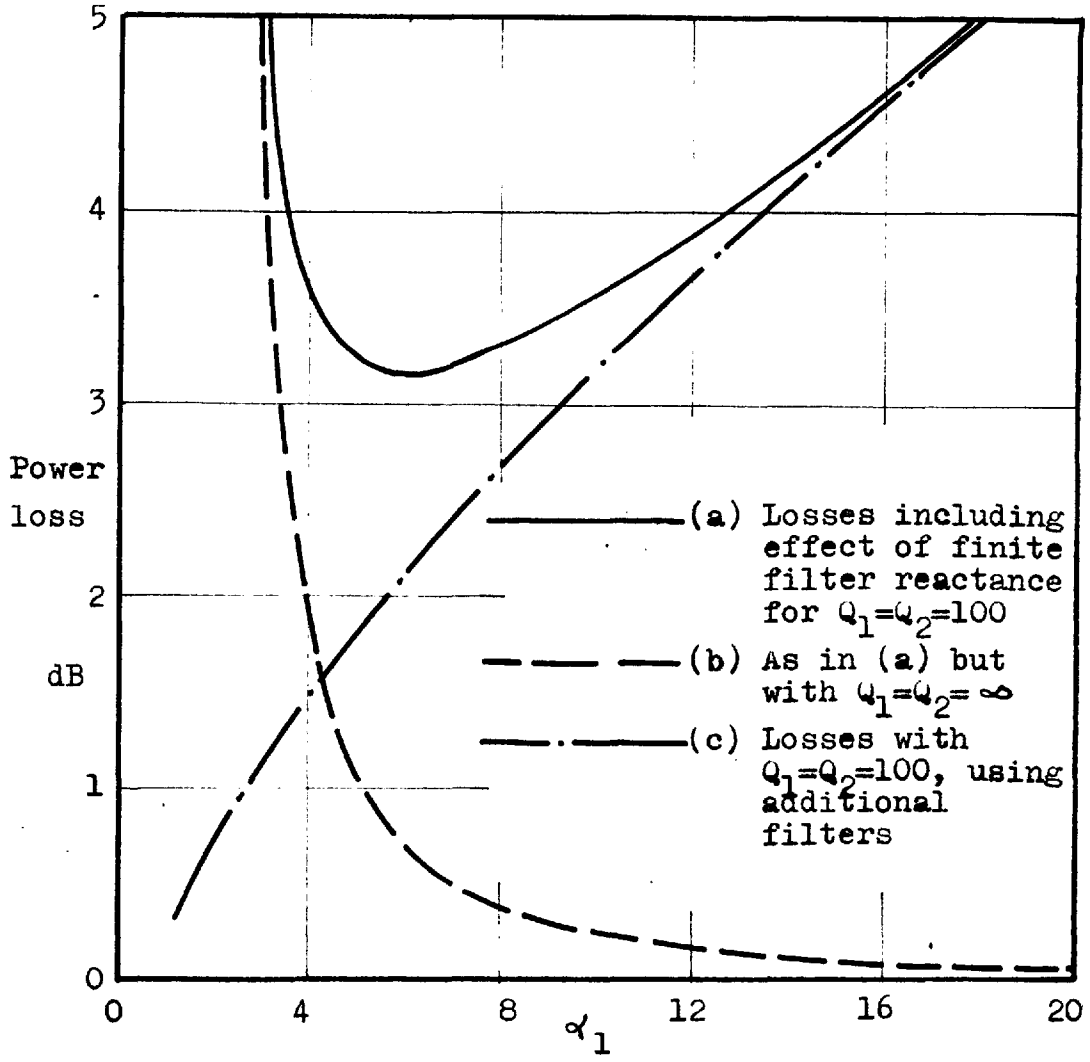


Fig.4.13 Illustration of behaviour of losses with respect to α_1 where $\alpha_1 = 2\alpha_2$, for a X2 node multiplier.

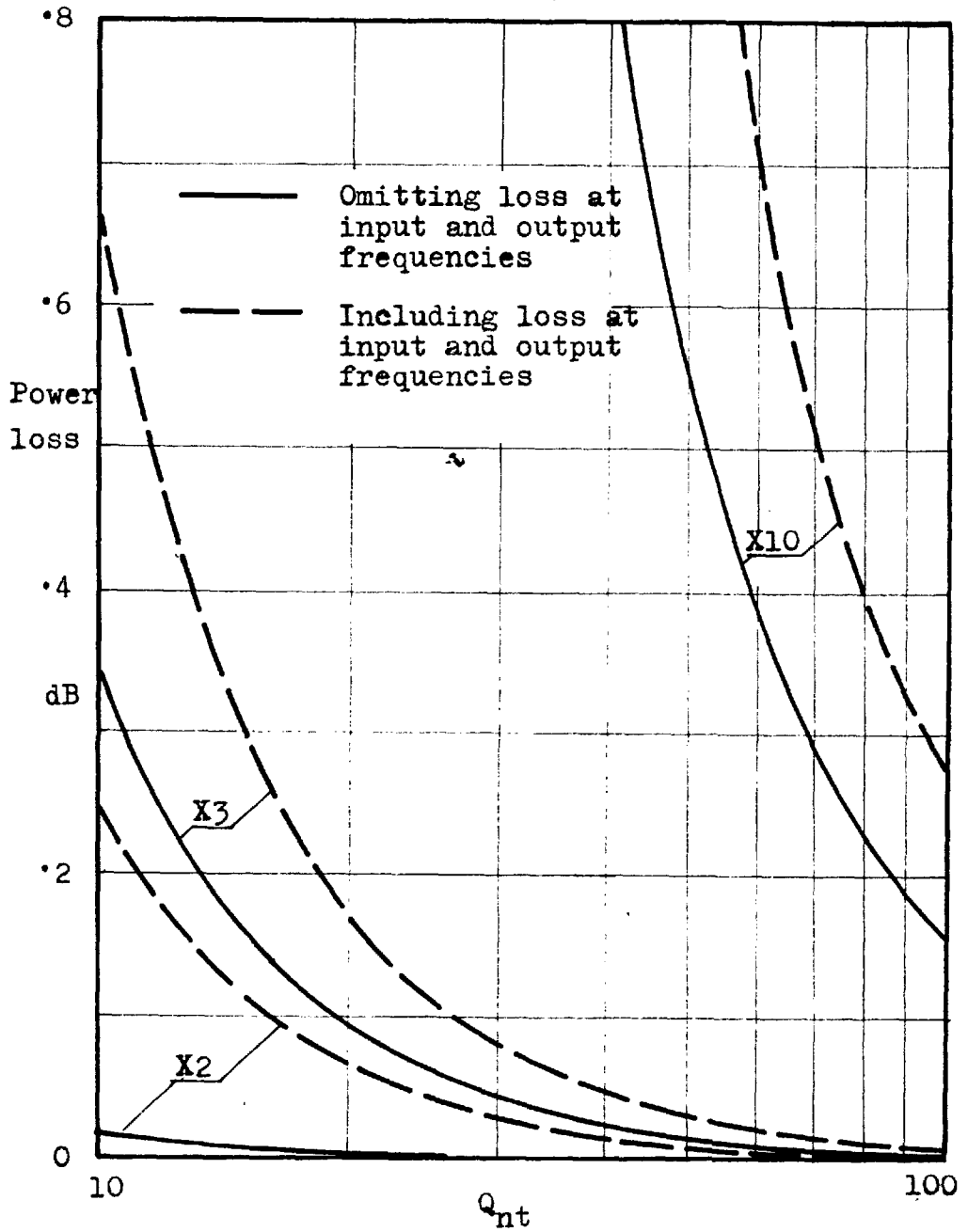
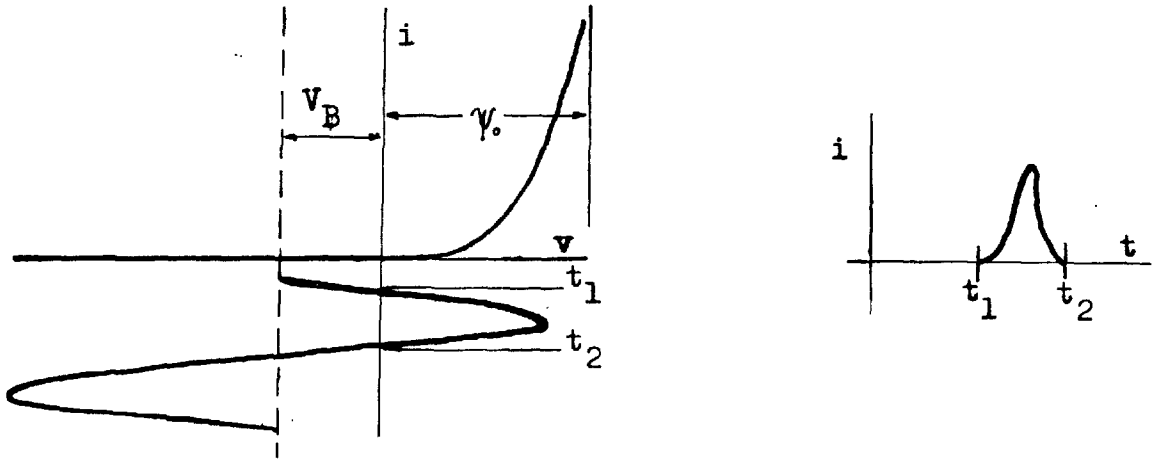
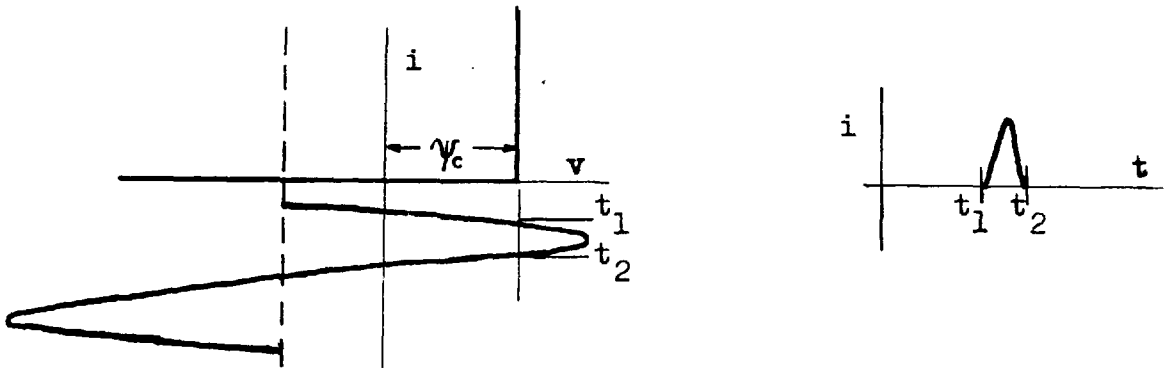


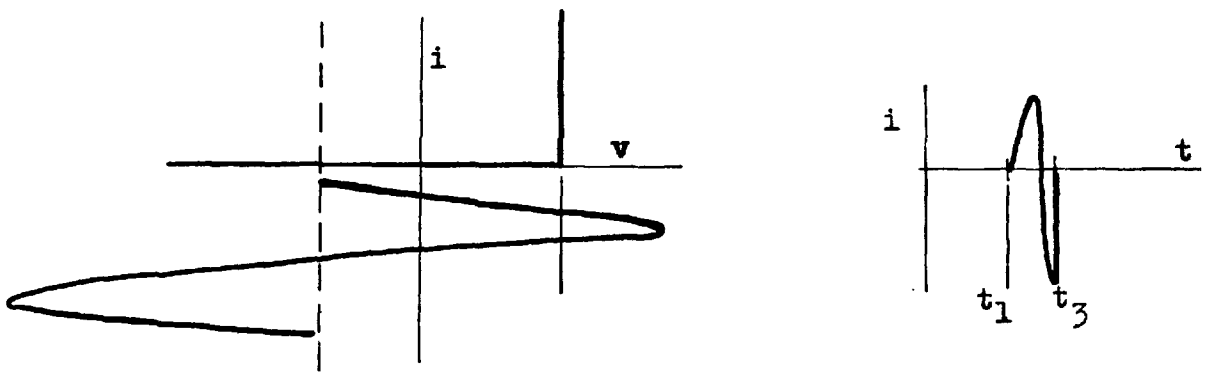
Fig.4.14 Illustration of harmonic losses in load conductance when circuit is designed for optimum operation with a diode $Q_{dn} = 100$, $V_b' = \cdot 95 V_b$ and $\gamma = 1/2$.



(a) Diode characteristic and current waveforms



(b) Approximation to (a) assuming abrupt characteristic



(c) Waveform obtained under charge storage conditions

Fig.4.15 Diode characteristics and current waveforms due to forward conduction.

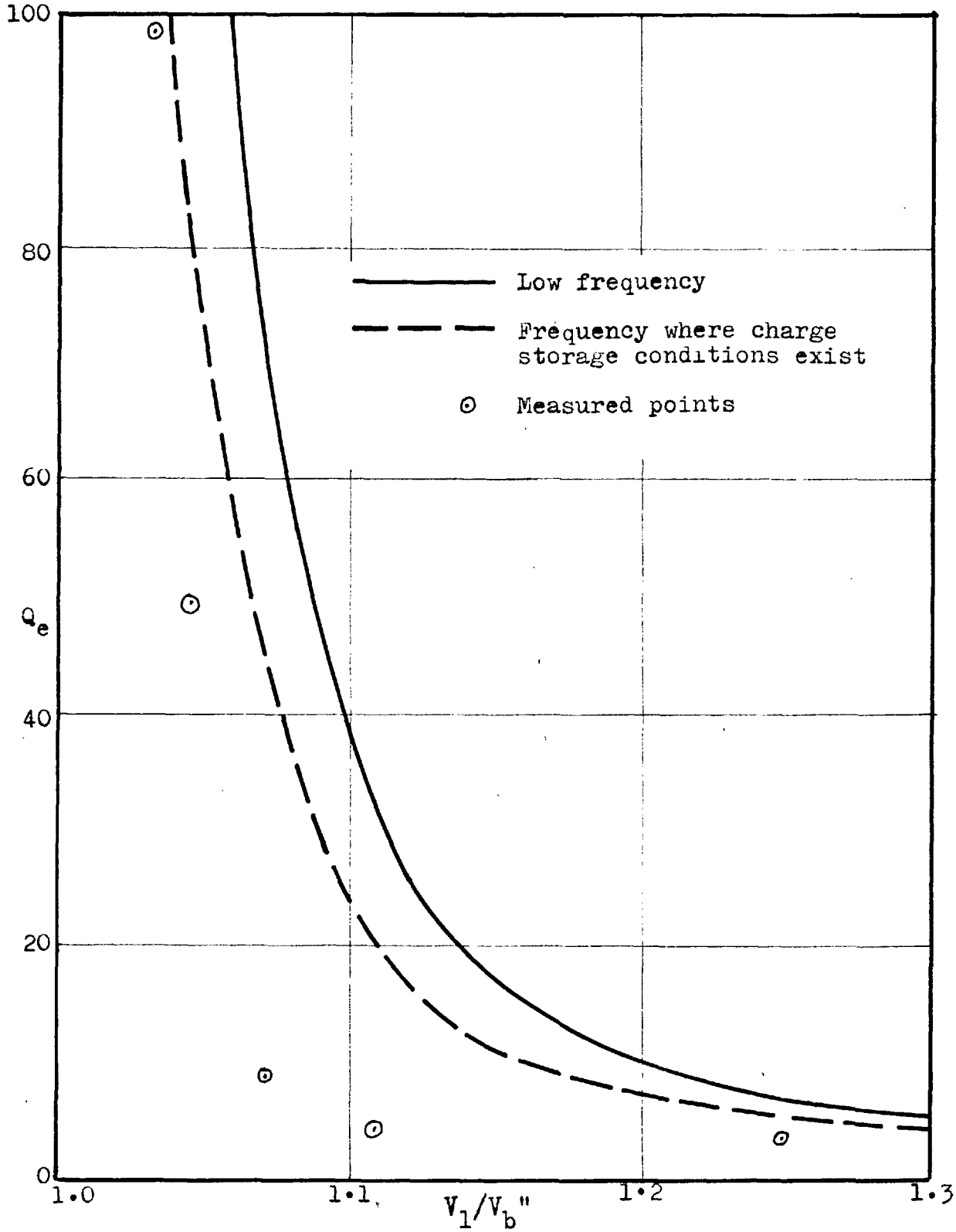


Fig.4.16 Variation of 'Q' factor, Q_e, as diode is driven into forward conduction.

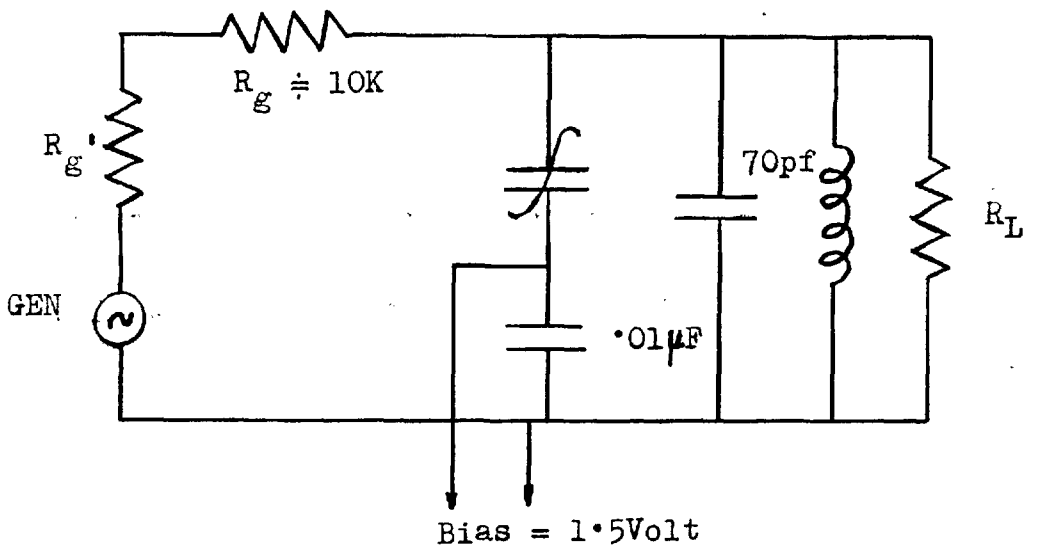


Fig.4.17 Experimental circuit used for verifying 'Q' factor under forward conduction conditions.

Appendix 4.1. Circuit relationships for node circuit.

Refer to the circuit shown in Fig.4.10(a). Using the nomenclature of (4.25) to (4.41) we can write the following equations:

$$X_n(\text{at } \omega_1) = \frac{j\omega_1 L_n}{1 - (1/n)^2 E_n}$$

hence, $$\frac{1}{j\omega_1 C_{o1}''} = \frac{1}{j\omega_1 C_o} + \frac{j\omega_1 L_n}{1 - (1/n)^2 E_n}$$

i.e. $$C_{o1}'' = C_o \Big/ \left\{1 - E_n / \left[\alpha_n' n^2 (1 - E_n/n^2)\right]\right\}$$

where $$\alpha_n' = C_n/C_o = \alpha_n E_n$$

Thus applying (4.29) gives:

$$\frac{1}{E_1} = 1 + \frac{\alpha_n'(1 - E_n/n^2)}{\alpha_1'\alpha_n' - \alpha_1'\alpha_n' E_n/n^2 - \alpha_1' E_n/n^2}.$$

Similarly,

$$\frac{1}{E_m} = 1 + \frac{\alpha_1'(1 - E_1 n^2)}{\alpha_1'\alpha_n' - \alpha_1'\alpha_n' E_1 n^2 - \alpha_m' E_1 n^2}$$

Solving these two equations for E_1 and E_n gives:

$$E_1 = \frac{\alpha_1'}{1+\alpha_1'} \frac{n^2+1}{2n^2} \left[1 + \frac{1}{n^2+1} \sqrt{(n^2-1)^2 - \frac{4n^2}{\alpha_1' + \alpha_n' + \alpha_1'\alpha_n'}}\right]$$

$$E_n = \frac{\alpha_n'}{1+\alpha_n'} \frac{n^2+1}{2} \left[1 - \frac{1}{n^2+1} \sqrt{(n^2-1)^2 - \frac{4n^2}{\alpha_1' + \alpha_n' + \alpha_1'\alpha_n'}}\right]$$

this solution can be used directly to evaluate E_1 and E_n in terms of α_1' and α_n'. Note that for the type of solution used to plot the curves in Fig.4.11 a trial and error solution is necessary since α_1 and α_n are specified and these are functions of E_1 and E_n, as given above.

Appendix 4.2. Circuit relationships for mesh circuit.

Since only the X2 mesh circuit is of practical interest the results will be restricted to this case. Using the nomenclature of (4.44) to (4.49) and proceeding as in Appendix 4.1 gives the following result:

$$E_1 = \frac{5}{8}\left[1 + \frac{\alpha_2'}{\alpha_1'(1+\alpha_2')}\right]\left[1 + \frac{1}{5}\sqrt{9 - \frac{16}{\alpha_1' + \alpha_2' + \alpha_1'\alpha_2'}}\right]$$

$$E_2 = \frac{5}{2}\left[1 + \frac{\alpha_1'}{\alpha_2'(1+\alpha_1')}\right]\left[1 - \frac{1}{5}\sqrt{9 - \frac{16}{\alpha_1' + \alpha_2' + \alpha_1'\alpha_2'}}\right]$$

SECTION 5.

GENERAL DETAILS OF DEPLETION LAYER CIRCUITS INCLUDING CASCADING.

5.1 Introduction.

In preceding sections depletion layer multiplying circuits have been analysed from the point of view of power loss. Methods have been derived for choosing optimum circuit parameters and a detailed study of circuit losses has been made. It is the purpose of the present section to discuss the circuits in a more general manner and particular attention will be paid to problems encountered in setting up practical circuits such as methods of biasing the diode. Methods of cascading stages will also be considered, using the results already obtained and bearing in mind requirements and limitations of practical circuits. A brief discussion will also be given of the behaviour of circuits under conditions where the input is not constant.

5.2 Biassing arrangements.

In the theoretical analysis of sect. 2 and sect. 4 it has been assumed that the diode is biased from a battery of negligible internal impedance. For a given operating condition in which the diode characteristic is being fully utilized, implying a small amount of forward conduction current, the battery may be replaced by a resistance of such a value that the reverse bias developed across it is equal to the value of bias previously supplied by the battery. Under these conditions the steady state operation of a multiplier will be the same whether the bias is derived from a

battery or from an automatic bias circuit, provided that the bias circuit is so designed that it does not introduce any additional loss. Some basic arrangements for the node and mesh circuits are shown in Fig.5.1.

The choice of biasing circuit constants in the case of fixed bias operation (when the forward current is negligible) is relatively simple. In the circuits shown in Fig.5.1,(a) and Fig.5,1,(c) R_b may have any value provided that the decoupling elements C_β and L_β are sufficiently large. In general it is convenient in this case to make R_b equal to zero. When using the arrangement shown in Fig.5.1,(b) or Fig.5.1,(d) where no decoupling element is used (C_i is merely an isolating capacitor which must be much greater than the diode capacitance at the operating point), the only restriction placed on R_b is that it must be large enough so as not to introduce any losses into the circuit.

In the case of automatic bias where the battery voltage is zero (the battery being replaced by a short circuit), some additional restrictions are placed on the choice of R_b. Firstly, if the value of R_b is too high, the bias voltage will be large for a small value of current. This may make optimum utilization of the depletion layer characteristic impossible since the peak alternating voltage across the diode will be approximately equal to the bias developed across R_b and (because the bias is developed by a small current) will thus never approach the region of the barrier voltage (at which point the current is very high). On the other hand the value of R_b must not be so low that the diode losses (due to conduction) become severe before a suitable bias is developed across R_b. Since the current varies rapidly with small changes in forward voltage, the range of values at which R_b may be fixed (between the limits governed by the above restrictions) is very great. A further restri-

ction on the value of R_b occurs when the multiplier is used with an amplitude modulated input. In this case it is necessary to ensure that the time constant formed by R_b and the relevant reactance is such that the developed bias follows any change in the input. In the circuits of Fig. 5.1,(b) and Fig.5.1,(d) the minimum value of R_b is limited as before by the fact that it must not introduce any losses into the circuit.

The choice between fixed bias and automatic bias is in practice often dictated by ~~practical~~ convenience rather than by theoretical considerations. There is, however, an important difference between the two methods in the case where the input signal is amplitude modulated; i.e. the relation between the input voltage and output voltage of a multiplier depends on whether the circuit is operated with fixed or automatic bias.

5.3. Voltage relationships.

5.3.1 Node circuit.

The relationship between the input and output voltages of a node circuit is given by (2.20), since I_n is directly proportional to V_n. Under fixed bias conditions this gives:

$$V_n = K(\omega_1 C_o/G_{nt})V_1 \qquad (5.1)$$

where 'K' is given by (2.21). The behaviour of the circuits may be illustrated by considering only the small signal approximation. Since K is then proportional to $(V_1/V_h)^{n-1}$, this gives:

$$V_n = kV_1^n \qquad (5.2)$$

where 'k' is independent of V_1, i.e. 'k' is constant for a given circuit. For a X2 multiplier this gives:

$$V_2 = kV_1^2 \qquad (5.3)$$

The behaviour under automatic bias conditions may be illustrated by considering the case where $V_n \ll V_1$. Under this condition the bias voltage will be approximately equal to the input voltage. In fact the ratio V_1/V_b will be practically constant at a value somewhat less than unity, the actual value being determined by the forward conduction characteristic and the value of bias resistance. This means that 'K' is dependent only on $C_o \propto V_b^{-1/2}$, for a given circuit and the output voltage is now related to the input voltage as follows:

$$V_n = k'V_1^{1/2} \qquad (5.4)$$

where k' is independent of V_1.

It is thus seen that the output voltage is less dependent on the input voltage under automatic bias than under fixed bias conditions. This may be a considerable advantage in practice in the case where input stability is a problem; it is evident that in this case a circuit operating under fixed bias conditions is inferior, particularly in high order multipliers as can be seen by comparing (5.2) and (5.4).

Note that if the circuit is being driven from a practical generator as in Fig.1.3,(a) the generator current I_g, is perhaps a more interesting parameter than the voltage at the input node, V_1. The relationship between these two quantities depends on the input loading conditions. For example, if the generator conductance G_g (or the loss conductance at the input node) is much greater than the conduc-

tance G_{eq} (see (2.77)), the generator current will be proportional to the voltage at the input mode and the above discussion may be directly applied. On the other hand, if $G_{eq} \gg G_g$ and the loss conductance at the input mode is negligible, the input voltage is not necessarily proportional to the generator current; the actual relationship may be found as follows:

From (2.77) and (2.20) we get:

$$G = K^2(\omega_1 C_o/G_{nt})^2 G_{nt} \tag{5.5}$$

Also, $$V_1 = I_1/G_{eq} \tag{5.6}$$

where I_1 is the input current, as distinct from the generator current. Thus:

$$V_1 = I_1/\left[K^2(\omega_1 C_o/G_{nt})^2 G_{nt}\right] \tag{5.7}$$

In the case of fixed bias this gives (again using the small signal approximation):

$$I_1 \propto V_1^{2n-1} \tag{5.8}$$

which gives, using (5.2):

$$V_n \propto I_1^{(n/2n-1)} \tag{5.9}$$

For the X2 multiplier this reduces to:

$$V_2 \propto I_1^{2/3} \tag{5.10}$$

Thus in a practical X2 multiplier where G_{eq} is comparable to G_g the variation of output voltage with generator current will lie somewhere between

$$V_2 \propto I_g^{2/3} \tag{5.11}$$

and

$$V_2 \propto I_g^{2} \tag{5.12}$$

In the case of automatic bias, referring to (5.7) and remembering that $C_o \propto V_b^{-(1/2)}$, we get:

$$I_1 \propto (V_1/V_b)^{2n-1} \tag{5.13}$$

Assuming again that $V_n \ll V_1$, we see that I_1 is, within the limits of the approximations, independent of V_1. This implies that $G_{eq} \propto V_1^{-1}$, which is the result given by (5.5) when $V_1 = V_b$.

The behaviour of the circuit as I_g is varied may be seen from the following example: Let the circuit be operating in such a way that $G_{eq} \gg G_g$ and neglect G_1; since I_1 is constant (see Fig.1.3,(a)) a slight increase in I_g will cause the current through G_g to increase rapidly, causing a consequent rapid increase in V_1, corresponding to a proportional decrease in G_{eq}; when G_{eq} is comparable to G_g, V_1 increases less rapidly for a given increase in I_g, (e.g. starting from the condition where $G_{eq} = G_g$ and increasing I_g by 10% causes V_1 to increase by 20% and G_{eq} to decrease by 20%; the upper limit is reached when G_{eq} becomes much less than G_g in which case, as has already been pointed out, V_1 is directly proportional to I_g.

Note that since, in a practical multiplier, the input will be matched, V_1 will be roughly proportional to I_g^2 (from the above example) and hence V_n will be directly proportional to I_g for small variations about the operating point.

It must be noted that the above discussion is only approximate in view of the fact that only the small signal

behaviour has been used. A further approximation occurs due to the fact that the circuit is assumed to be correctly 'tuned'; since the capacitance of the diode changes with bias voltage, the circuit will not remain in this condition if the bias voltage is changed, as happens under automatic bias conditions. The errors involved due to 'mis-tuning' will be small for small departures from the operating point but for large variations of input under automatic bias conditions the 'mis-tuning' due to the change in diode capacitance may eventually cause the output to fall as the input is increased. A similar effect may occur under fixed bias conditions due to the presence of the reactances given by (2.25) and (2.26) but since these reactance changes are relatively small it is unlikely that they will have much effect unless the circuit 'Q' factors are particularly high.

5.3.2 Mesh circuit.

The mesh circuit may be treated in a similar manner. Referring to (2.46) the second harmonic voltage, V_2 is given by:

$$V_2 = K I_1/(\omega_1 C_o) \qquad (5.14)$$

where 'K' is given by (2.47) and (2.36). Considering again the small signal case, gives:

$$V_2 = k I_1^2/(V_b C_o^2) \qquad (5.15)$$

Thus for fixed bias operation,

$$V_2 \propto I_1^2 \qquad (5.16)$$

Under automatic bias conditions, since $C_o^2 \propto V_b^{-1}$, we get:

$$V_2 \propto I_1^2$$

i.e. within the limits of the approximations the behaviour is the same under both fixed and automatic bias conditions.

The relationship between the generator voltage and the input current may be found as follows (refer to Fig.5.2,(b)):

If $R_g \gg R_{eq}$ then $I_1 \propto V_g$ and the relationship between generator voltage and output voltage is:

$$V_2 \propto V_g^2 \tag{5.17}$$

If $R_{eq} \gg R_g$, the relationship between the generator voltage and the input current may be found as follows:

$$I_1^2 R_{eq} = I_n^2 R_{nt} \tag{5.18}$$

(This is the basic power equation for the multiplier and is the mesh circuit equivalent of (2.77)).
Combining (5.18) with (5.15) and using the fact that $V_2 \propto I_2$ gives:

$$R_{eq} \propto I_1^2 \tag{5.19}$$

Thus since $V_g = I_1 R_{eq}$ (5.20)

it follows that: $$V_g \propto I_1^3 \tag{5.21}$$

Combining this result with (5.16) gives:

$$V_2 \propto V_g^{2/3} \tag{5.22}$$

It must be remembered that the above results are, as in the case of the node circuit, only approximate. They

indicate, however, the general behaviour which may be expected when the input amplitude is not constant. It is seem that (within the limitations of the assumptions) the mesh circuit behaves in the same way whether fixed or automatic bias is used. The input/output relationships correspond to those obtained in the node circuit using fixed bias as may be seen by comparing (5.22) with (5.11) and (5.16) with (5.12).

5.3.3 General conclusions.

The detailed behaviour of a multiplier under large signal optimized conditions with varying input amplitude is not simple. Any particular circuit may be analysed if the exact behaviour is required to be determined and the above results may be used as a basis for predicting the performance although it must be borne in mind that their derivation involves two basic approximations (i.e. small signal and no 'mis-tuning'). The results also of course indicate the essential difference between operation under fixed and automatic bias conditions.

5.4 Hysteresis effects.

It was observed (see sect.1 and also sect.6) that under certain conditions as the input amplitude or frequency was varied, the output, instead of varying regularly, 'jumped' to a new value; the same effect was also observed when the output or input reactances were altered. It was noted that when this effect occurred the diode was being operated under

conditions in which the input and/or the output voltage was comparable with the bias voltage. It is the purpose of the present section to give a theoretical solution to account for this behaviour, which is a form of hysteresis. It is not intended to give a complete theory which may be verified experimentally but merely to give a qualitative explanation of the effect, which is generally of secondary importance since it may only occur when 'setting up' a circuit or when the input is otherwise varied.

Let a susceptance $B(V_1, V_n)$ be introduced at the output node of a node type multiplier. This may arise from two different causes:

(a) It may be due to the 'large signal' reactance given by (2.26)

(b) It may be due to the change in the operating point capacitance caused by conduction current flowing in the bias resistance.

The total susceptance at the output node B_n is the sum of the inductive susceptance, B_L, the circuit capacitive susceptance plus the diode capacitive susceptance, B_C and the above 'generated' susceptance.

i.e. $$B_n = B_L - B_C - B(V_1, V_n) \qquad (5.23)$$

At the chosen operating point, B_n will be zero, (c.f.(2.15)). The admittance, magnitude at the output node, Y_n is given by:

$$Y_n = \left[G_n^2 + (B_L - B_C - B(V_1, V_n))^2\right]^{1/2} \qquad (5.24)$$

The output voltage V_n is given by:

$$V_n = I_n Y_n^{-1} \qquad (5.25)$$

where I_n is (to a first approximation) the current given by (2.20). For the sake of this analysis, let I_n be a simple

function of V_1; e.g. let

$$I_n = kV_1^m \tag{5.26}$$

Combining (5.24), (5.25) and (5.26) gives:

$$kV_1^m = V_n\left[G_n^2 + (B_L - B_C - B(V_1, V_n))^2\right]^{1/2} \tag{5.27}$$

Let us consider first of all the simple case of $m = 1$ and

$$B(V_1, V_n) = bV_n \tag{5.28}$$

where b is a constant.

Referring to case (a) above, (5.28) represents an approximation to the condition given by (5.26) i.e. we are saying in effect that:

$$bV_n/B_o = (C_{on}' - C_o)/C_o \tag{5.29}$$

where B_o is the susceptance of C_o. In fact, of course, C_{on}'/C_o is a polynomial in both V_1 and V_n. The simplification inherent in (5.28) is justified only on the grounds that the present exercise aims at producing a qualitative explanation of the hysteresis effect and is not intended to give a rigorous quantitative solution. It will be seen later that the approximation is valid for this purpose.

Referring to case (b) above, the susceptance in (5.28) corresponds to the change in operating point capacitance due to V_n, causing forward conduction current to flow in the bias resistor thus altering the effective bias voltage. It is again, of course, an approximation and only serves to illustrate an observed effect.

Substituting (5.28) into (5.27) gives:

$$kV_1^2 = V_n^2\left[G_n^2 + (B_L - B_C - bV_n)^2\right] \tag{5.30}$$

This function has been plotted in Fig.5.2 for the case of $k = 1$, $(B_L - B_C) = 10$, $b = 100$ and for three values of G_n^2. It is apparent that, depending on the value of G_n relative to the susceptance term, the function may or may not exhibit hysteresis effects. Obviously if G_n is large compared ~~to~~ with $(B_L - B_C)$ hysteresis will not occur since the function will be single valued at all times with respect to V_1. Note that $(B_L - B_C)$ is determined by the magnitude of $B(V_1, V_n)$ at the chosen operating point (i.e. when B_n (see (5.23) is zero). Since $B(V_1, V_n)$ is related to the diode capacitance, it follows that hysteresis is most likely to occur when the diode capacitance forms a large part of the total node capacitance. This is equivalent to saying that α_n, defined by (4.6) must be less than a certain value for the effect to occur.

The conditions under which hysteresis effects are most likely to occur may be summarised as follows:

(1) Low value of G_{nt}, i.e. high circuit 'Q' factors

(2) High value of $B(V_1, V_n)$, implying diode capacitance large compared to circuit capacitances.

(3) High value of $B(V_1, V_n)$, implying large signal operation.

It is apparent that if $B(V_1, V_n)$ is a higher order function of V_n, the general behaviour will remain unchanged and the form of hysteresis illustrated in Fig.5.3 may still occur. If however the susceptance term is a polynomial in V_1 and V_n one would expect other, more complicated, forms of hysteresis to occur. Take for example, the curve shown in Fig.5.3,(b). Since this is triple valued in both V_1 and V_n, its equation is a cubic in both these quantities and this condition could arise if the large signal polynomial expression for I_n and $B(V_1, V_n)$ ~~are~~ is used to obtain the equivalent of (5.27).

In a practical multiplier, the hysteresis effect will manifest itself as a sudden jump in output as the input is slowly varied. For example, refer to Fig.5.3,(a). As the input voltage reaches point 'Y' the output voltage will jump from a value V_{nY} to a value V_{nZ}. Note that if the theoretical operating point coincides with a minimum value of V_1, for instance the point 'X', the theoretical operating conditions will be unobtainable in practice, since on reducing V_1 towards 'X', the output voltage will jump from a value V_{nX} to a value V_{nW}. The closeness to which one can reach the theoretical conditions will in this case be determined by the stability of the input.

Note that since the hysteresis effect is due to a 'generated' reactance it also occurs as the circuit is tuned, i.e. as the node capacitance or inductance is altered in the region of the optimum value. Similarly, as the frequency is varied, hysteresis may occur.

Since the properties which give rise to hysteresis in the above discussion are also present in the mesh circuit, it is to be expected that the effects would be similar. This is borne out by the experimental results (see sect. 6.3.3).

5.5 Effect of de-tuning a circuit.

The analysis in preceding sections has been based on the assumption that the circuits were tuned for optimum conditions. The effect of de-tuning will now be considered; to illustrate the behaviour, let us consider the X2 node multiplier.

The relationship between the output voltage and current are given by (2.14) and the theory has been based on

the assumption that $\phi_n = 0$. The effect of de-tuning is to alter the value of ϕ_2, in which case (2.14) becomes:

$$V_2 G_2 = I_2 \cos\phi_2 \tag{5.31}$$

Combining this with (2.20) gives:

$$V_2 G_2 = K \omega_1 C_o V_1 \cos \phi_2 \tag{5.32}$$

Note that (2.22) still holds since it does not involve V_2; this is not the case in (2.23) and the modified form of (2.23) will involve ϕ_2. Since (2.23) is of secondary importance in the evaluation of K, we will neglect, for the purpose of the present analysis, this change.

The efficiency may be evaluated using (5.32) and it is apparent that the new expression for efficiency will be as before (refer to (2.83)) with K replaced by K' where:

$$K' = K\cos\phi_2 \tag{5.33}$$

It is apparent that any deviation in ϕ_2 from its original value of zero will cause K' to be less than K and hence cause a decrease in efficiency, as one would expect.

It must be remembered however that changing ϕ_2 from its original value will alter the limiting conditions of voltage across the diode, given by (2.62). By considering specific values of V_2/V_1 it is possible to plot $\omega_1 t$ versus ϕ_2 from the relationship:

$$\frac{V_2}{V_1} = - \frac{\cos \omega_1 t}{2\cos(\omega_2 t + \phi_2)} \tag{5.34}$$

which is a modified version of (2.63) including ϕ_2. It is then possible to solve the conditions:

$$V_1 \sin \omega_1 t + V_2 \sin \overline{\omega_2 t + \phi_2} = -V_b \tag{5.35}$$

These conditions have been evaluated for $V_2/V_1 = 1$ and $V_2/V_1 = 0.5$. The results thus obtained are shown in Fig. 5.4 in the form V_1/V_b versus ϕ_2. As one would expect, it is possible to increase the maximum value of V_1/V_b considerably by altering ϕ_2 (this is of course because the peak value of the waveform may be made less by suitably adjusting the phase relation between the two voltages across the diode).

Also shown in the same figure is the value of K'/K, evaluated by letting V_1/V_b assume its increased value, using the small signal expression for K.

The slight increase in the value of K'/K above unity is insignificant. The main interest in the results lies in the fact that the input voltage can be considerably increased if the output node is de-tuned, without seriously affecting the efficiency. Note that for a circuit in which the losses at the input are very large, a value of K'/K = 0.5 corresponds to a decrease in efficiency of 6dB. For a circuit in which the losses are small this value of K'/K corresponds to a X4 increase in power loss. It is thus apparent that in a circuit in which the losses are small it is possible to increase the input voltage and hence the input power considerably by de-tuning from the original conditions. It must be remembered that the above results involve two basic approximations: (a) only a small signal expansion for K has been used, (b) a circuit designed initially for operation with $V_2/V_1 = 1.0$ will, when de-tuned, no longer satisfy this condition; due to ϕ_2 changing V_2 will tend to drop in value. These two approximations will not however, affect the essential conclusions of the above analysis.

5.6. Input matching and power handling capabilities.

5.6.1 Node circuit.

The operation of individual circuits has already been considered in detail but the exact requirements for matching a circuit to a given source have not yet been dealt with. Let us consider the problem of driving a single stage node multiplier from a generator which is capable of supplying a given amount of power P_a at a peak voltage V_g'. In the case of a current generator whose peak value of current is I_g and whose internal conductance is G_g, V_g' is given by:

$$V_g' = I_g/(2G_g) \tag{5.36}$$

and

$$P_a = I_g^2/(8G_g) \tag{5.37}$$

Under matched input conditions the input power to the circuit is equal to P_a, hence:

$$P_a = V_1^2(G_{eq} + G_L)/2 \tag{5.38}$$

where G_L is the equivalent loss conductance at the input node (which may be either due to diode loss or circuit loss). G_{eq} may be expressed in terms of parameters relating only to the diode as follows:

from (2.20) we get:

$$G_{nt} = K\omega_1 C_o/\beta \tag{5.39}$$

where

$$\beta = V_n/V_1 \tag{5.40}$$

hence (5.5) may be rewritten thus:

$$G_{eq} = K\beta\omega_1 C_o \tag{5.41}$$

Substituting this expression for G_{eq} into (5.38) gives:

$$P_a = V_1^2(K\beta\omega_1 C_o + G_L)/2 \qquad (5.42)$$

Consider the case of a circuit in which diode losses predominate. For a given diode, the operating point (chosen to fully utilise the non-linear characteristic) and hence the 'Q' factor, will be fixed. Thus for an optimised circuit the parameters K, β and V_1 will be determined (from the results of sect.2) and for a given C_o, the value of P_a is fixed. If however several identical diodes are connected in parallel the value of P_a may be increased to correspond to the greater power (note that G_L will also increase), whilst keeping the parameters K, β and V_1 constant. If the value of V_g' given by (5.36) is not equal to V_1 a transformer will be necessary to couple the circuit to the generator. The above conditions also apply in the case of a circuit in which inductor losses predominate since for a given 'Q' factor the operating conditions are fixed (in this case however G_L will be independent of the number of diodes).

If it is desired to connect the generator directly to the multiplier without using a transformer it will generally be necessary to vary one of the other parameters. Referring to (5.42) it is seen that in this case both P_a and V_1 are fixed. In order to let K and β attain their optimum values it will therefore be necessary to alter the bias voltage, V_B (this will of course only be possible over a limited range of values and implies that the diode characteristic will not be fully utilised). The number of diodes in parallel may then be varied until C_o is of a value such that (5.42) is satisfied. It should be noted, however, that in the case where the losses are determined by the diode, alteration of V_B automatically causes the 'Q' factor (used in the power loss curves of sect.2) to change, thus causing the

optimum values of K and β to change. The exact solution for V_B (for P_a and V_1 fixed) may not, therefore, be simply obtained but it is apparent that sufficient degrees of freedom exist (by letting V_B vary) for the circuit to be matched.

A third possibility exists to fulfill the matching conditions if only one diode is available. In this case a transformer may be used together with an adjustment of the bias voltage; this gives sufficient degrees of freedom for (5.42) to be satisfied, since C_o is a function of the bias voltage.

The power 'handled' by the diode, P_{1d} , i.e. the power converted from the input frequency to the desired harmonic frequency, is the input power to the multiplier less the power loss at the input node (due to diode or circuit losses). Thus

$$P_{1d} = V_1^2 K \beta \omega_1 C_o/2 \qquad (5.43)$$

P_{1d} will be maximum when the diode characteristic is being fully utilised, i.e. when it is biased so that negative voltage swings drive it nearly to the point where avalanching occurs and positive voltage swings drive it into the forward conduction region. The values of K and β may be found from Fig.?.6 to Fig.?.11 and Fig.?.4 and Fig.?.5 for various operating conditions.

5.6.2 Mesh circuit.

The mesh circuit may be treated in a similar manner. Thus the power input P_a is given by:

$$P_a = I_1^2 (K \beta /(\omega_1 C_o) + R_L)/2 \qquad (5.44)$$

where in this case K is defined by (2.46) and

$$\beta = I_n/I_1 \tag{5.45}$$

R_L is the loss resistance in the input mesh. As before, if the diode operating conditions are fixed, P_a may be altered by altering the number of diodes in parallel and the available power may thus be extracted from a given generator, a transformer being used to adjust I_1 to the required value. Also as in the case of the node circuit, it is possible to alter the value of I_1 (whilst keeping the diode conditions optimum) by adjusting the bias voltage suitably.

The power handled by the diode is given by:

$$P_{1d} = I_1^2 K \beta /(\omega_1 C_o) \tag{5.46}$$

where from Fig.2.21 to Fig.2.23 K may be obtained directly and

$$\beta = nK/(\omega_n C_o R_{nt}) \tag{5.47}$$

5.7. Cascading considerations.

5.7.1 Introduction.

It has already been pointed out in sect.2 and sect.4 that it is often advantageous to use several low order multipliers cascaded together instead of using one stage of high order multiplication. In this section some of the requirements and problems encountered in designing a cascaded multiplier will be discussed. These concern essentially the matching conditions to be fulfilled between adjacent stages and the estimation of overall efficiency using the results obtained in preceding sections. For the sake of illustrating the behaviour, node circuits will be considered.

5.7.2 Matching conditions between adjacent stages.

Let us consider the problem of cascading two node type multiplier stages together. Let the first stage be designed to give an output voltage V_{n1} across a load conductance G_{o1} and the second stage to be designed to operate with an input voltage V_{12} and to have a total input conductance G_{in2} where

$$G_{in2} = G_{L2} + G_{eq2} \qquad (5.48)$$

G_{L2} being the input loss conductance. If it happens that $V_{n1} = V_{12}$ and $G_{o1} = G_{in2}$ then the two stages may be connected directly together with G_{o1} being replaced by G_{in2}. In this case the load of the first stage is formed partly by the loss conductance of the second stage and partly by the 'active' input conductance of the second stage, this 'active' conductance being of course a function of the output voltage and load of the second stage. Note that the fact that the load conductance of the first stage is no longer a 'real' conductance in no way affects the operation of the stage; ~~the fact still exists that~~, under steady state conditions, the output voltage and current of the first stage behave in exactly the same way as if a 'real' load existed.

In practice of course it would be extremely unlikely that two stages taken at random would fulfill the above voltage and load conditions. Sect.5.6 may be taken as a basis for obtaining the necessary matching conditions between two stages. Let us consider the problem of designing the second of two stages on the assumption that the first one has been already designed for maximum output. Assuming that the parameters K and β are determined by the design curves of sect.2 or sect.4, three variables remain for adjusting the matching conditions:

(a) The impedance transformation (turns ratio) between the stages may be altered.

(b) The diode in the second stage may be altered, or the number of diodes of the same type in a parallel combination may be altered.

(c) The bias voltage in the second stage may be altered.

As has already been pointed out, any one of the above three variables may be fixed and sufficient degrees of freedom will still exist for the matching conditions to be satisfied.

It will be necessary to consider each case on its merits bearing in mind the practical aspects, for example whether it is more convenient to use transformer coupling or to obtain different diodes or a different number of the same diode for the second stage. Some examples may however serve to illustrate the general nature of the problems involved in cascading two adjacent stages. Let us consider for the sake of simplicity the case of a low loss circuit, i.e. one in which we may assume that the power loss is small enough for the input and output loss conductances to be neglected (compared to the conductances G_{eq} and G_o respectively in a particular stage) where the voltage relationships are concerned. This assumption implies that since the power loss is finite (but small) the values of the parameters K and β (see (5.42)) are determined for minimum loss by the results of preceding sections; the present problem is to examine the matching conditions between adjacent stages and to compare the changes necessary between two stages for these conditions to be fulfilled. Let the parameters of the first and second stages be denoted by the subscripts 1 and 2 respectively: thus the input voltages of the two stages will be V_{11} and V_{12}. Referring to (5.42) the value of P_a will be the same for both stages; thus:

$$\left.\begin{aligned} P_a &= V_{11}^2 K_1 \beta_1 \omega_1 C_{o1} \\ &= V_{12}^2 K_2 \beta_2^2 \omega_1 C_{o2} \end{aligned}\right\} \qquad (5.49)$$

Now define the following quantities:

$$C_{om} = K_m' V_{bm}^{-(1/2)} \qquad (5.50)$$

$$V_{1m} = D_m V_{bm} \qquad (5.51)$$

where m refers to stage 1 or stage 2.
Substituting these relationships into (5.49) gives:

$$\left[\frac{V_{11}}{V_{12}}\right]^{3/2} = 2 \frac{K_2 \beta_2}{K_1 \beta_1} \sqrt{\frac{D_2}{D_1}} \frac{K_2'}{K_1'} \qquad (5.52)$$

For the sake of this illustration let us assume that the optimum operating conditions for each stage are the same i.e. that $K_2 \beta_2 = K_1 \beta_1$ and that $D_2 = D_1$. In practice this may well be approximately true as may be seen by referring to the appropriate design curves (for a X2 multiplier refer to Fig.2.4 and Fig.2.6). We now have:

$$\left[\frac{V_{11}}{V_{12}}\right]^{3/2} = 2 \frac{K_2'}{K_1'} \qquad (5.53)$$

Three possibilities now exist for fulfilling the matching conditions.

(a) No coupling transformer used. In this case the input voltage to the second stage will be equal to the output voltage of the first stage. This gives:

$$V_{12} = \beta_1 V_{11} \qquad (5.54)$$

Substituting this into (5.53) gives:

$$K_2'/K_1' = (1/2)\beta_1^{-3/2} \qquad (5.55)$$

This gives the necessary relationship between the diode capacitances (at a given bias, refer to (5.50)) of the two stages. Note the special case of the first stage having a voltage gain of unity whence (5.55) shows that the diode in the second stage must have a capacitance at a given bias which is half that of the preceding stage; this could be accomplished in practice by using two diodes in parallel for the first stage and only one in the second stage; alternatively of course a different diode could be used in each stage. Note that the bias relationship between the two stages is given by (5.54) and (5.51):

$$V_{b2}/V_{b1} = \beta_1 \qquad (5.56)$$

It is seen that in the case when no coupling transformer is used, the relationships between the diode capacitances and the bias voltages of adjacent stages depends on the voltage gain of the first stage. Note that if β is small compared to unity, the diodes must increase in capacitance with each successive stage and the bias must similarly decrease. It is apparent that this would usually be impracticable for more than a small number of consecutive stages since the diode capacitance would rapidly become very large and the bias very small. It may therefore be concluded that a coupling transformer is advantageous in practice, whence two possibilities remain.

(b) Same diodes used.

Assuming the same conditions as above, and letting the turns ratio of the transformer be T, where

$$T = V_{12}/V_{n1} \qquad (5.57)$$

we may rewrite (5.53) thus:

$$(\beta T)^{-3/2} = 2K_2'/K_1 \qquad (5.58)$$

and from (5.51) and (5.40) we get the bias relationship:

$$V_{b2}/V_{b1} = \beta T \qquad (5.59)$$

From (5.58) we see that if the same diodes are used in each stage the turns ratio is given by:

$$T = (1/\beta)(1/2)^{2/3} \qquad (5.60)$$

and

$$V_{b2}/V_{b1} = (1/2)^{2/3} \qquad (5.61)$$
$$= 0.63$$

It is apparent that this condition may offer considerable advantages over the previous one since for small values of β, the decrease in bias per stage is less than that indicated by (5.56) The remaining possibility is for the bias to be the same per stage.

(c) Same bias per stage.

In this case from (5.59) we get:

$$\beta T = 1 \qquad (5.62)$$

and from (5.58)

$$K_2'/K_1' = 1/2 \qquad (5.63)$$

This would seem to be a very reasonable condition for a practical multiplier since it enables the bias to be maintained at a constant value for each stage, thus allowing the diode characteristic to be fully utilised in each stage. At the same time the condition that the diode capacitance decreases by half for a doubling in frequency fits in well with the properties of most diodes, since to keep the 'Q' factor constant, it is necessary to construct diodes whose capacitance decreases with increasing frequency (the series loss resistance being approximately the same at all frequencies)

Although the above examples have assumed low loss circuits, they nevertheless give an idea of the general behaviour and matching requirements applicable to any cascaded multiplier. The introduction of losses into the circuit will alter the quantitative relationships but the general conclusions will usually remain the same. Take for example the case of a cascaded multiplier designed without a coupling transformer in which the voltage gain of a stage is unity. This implies that the stages are not optimized for minimum power loss but it is possible that in some cases a sacrifice in efficiency may be acceptable if it enables a saving in circuit complexity (in this case, the fact that a transformer is not used). Since the voltage gain of each stage is unity the bias will normally be made the same and the operating conditions of the diode, i.e. the values of K and β , in each stage will be the same. The output power from the first stage P_{o1} may be written thus (referring to (5.41)):

$$P_{o1} = V^2(K\beta\omega_1 C_{o1} - G_{L12}) \qquad (5.64)$$

where G_{L12} is the total loss conductance at the output node of the first stage and input node of the second stage. This may also be expressed as the power converted in the second stage; thus

$$P_{o1} = V^2 K\beta\omega_2 C_{o2} \qquad (5.65)$$

Equating these two expressions for P_{o1} gives:

$$C_{o2} = (1/2)C_{o1} - G_{L12}/(K\beta\omega_2) \qquad (5.66)$$

Comparing this with (5.55) shows that the effect of including the losses is to make C_{o2} less than half C_{o1}.

In the above discussions all the spurious effects dealt with in sect.4 have been neglected on the basis that

they may be eliminated in any particular case by the use of additional filtering.

5.7.3 Estimation of basic efficiency using the results of previous sections.

It is always possible to determine the power loss of a specific circuit with known parameters, simply by referring to the appropriate curves of preceding sections. The estimation of the overall power loss of a series of cascaded stages by summing the individual losses is straightforward. The more interesting problem of determining the maximum obtainable efficiency with given diodes and circuit components is not as simple, however, and it is necessary to bear in mind some relevant points when using the curves for losses in a single stage to estimate the combined losses of a number of stages.

Considering the case where diode losses predominate, the first point to remember is that if the bias is not the same for each stage the 'Q' factor as used in the curves of sect.? will not be a directly available quantity. It will therefore be necessary to decide on the method of matching the stages and to arrive at an estimation of the relevant design parameters before the 'Q' factor and hence the power loss, may be found. On the other hand, if the bias is the same for each stage, the 'Q' factor will be a known quantity and the efficiency may be readily evaluated for each stage (remembering that if the same diode is used in different stages the 'Q' factor will be inversely proportional to frequency) and the overall efficiency determined in a straightforward manner. This was the method used in the example given in sect.?.4.?.

It is interesting to consider the problem of cascading two stages of different 'frequency gain' together. Let us take the case of two stages of equal bias using a suitable arrangement of the same diodes in each stage. The minimum loss may be found from Fig.?.18. Let the diode 'Q' factor at the final output frequency be 10 and let the desired output frequency be obtained by a combination of a X3 and a X2 circuit. The following results are obtained:

(a) 1st stage X3, Q_{d3} = 20, Power loss = 3.3 dB.
2nd stage X2, Q_{d2} = 10, Power loss = 3.4 dB.

(b) 1st stage X2, Q_{d2} = 30, Power loss = 1.2 dB.
2nd stage X3, Q_{d3} = 10, Power loss = 6.2 dB.

It is seen that arrangement (a) gives a total loss of 6.7 dB. compared to a total loss of 7.4 dB for arrangement (b). Let us now take the example of the output being obtained by a combination of a X2 and a X10 circuit. This gives the following results:

(a) 1st stage X10, Q_{d10} = 20, Power loss = 11.0 dB.
2nd stage X2, Q_{d2} = 10, Power loss = 3.4 dB.

(b) 1st stage X2, Q_{d2} =100, Power loss = 0.4 dB.
2nd stage X10, Q_{d10} = 10, Power loss = 16.0 dB.

Arrangement (a) gives an overall loss of 14.4 dB. compared to 16.4 dB for arrangement (b). From the above two examples it would seem that there is a slight advantage to be gained by putting the stage with the highest 'frequency gain' first.

The efficiency in the case where circuit losses predominate is considered as a 'basic' efficiency since it may not be improved by additional circuitry. The losses may be estimated directly once the circuit parameters have been determined. If the circuit is optimized with respect to

circuit losses then the overall efficiency for a number of stages may be found from a knowledge of the circuit 'Q' factors using the results of sect.4. Note however that if the stages are connected directly together it will normally be possible to elimimate one of the node loss conductances since one of the two parallel resonant circuits will be superfluous. Thus if a large number of stages were cascaded together the effective 'Q' factor per stage would be almost double that for a single stage multiplier.

5.7.4 Estimation of additional losses.

The results obtained in sect.4 for various additional losses may be applied to cascaded multipliers. Some special points should be noted however and these will be outlined below.

In sect.4.3 the effect of finite filter reactances is studied. The essential results may be applied to any specific cascaded stage; however in estimating the coupled loss of sect.4.3.3 it must be remembered that the values of Q_{1t} and Q_{nt} for intermediate stages are simply the loss 'Q' factors; i.e. since the load is not a real conductance it does not constitute a loss at any frequency. In general this effect may therefore be neglected in all but the first and last stages where real conductances exist.

In sect.4.4 the effect of the finite 'Q' factor of the input and output circuits is considered with respect to harmonic losses. Again this problem only becomes serious in the first and last stages of a cascaded multiplier. It is interesting to note however that the presence of harmonic losses in the output load may determine the best arrangement in the case where two stages of different 'frequency gain'

are cascaded. Referring to the example given in sect. 4.4.3 of $Q_{nt} = 10$ it is seen that if a X2 and a X3 circuit are cascaded and the X3 stage is the high frequency one, the harmonic losses will be 0.66 dB; if the X2 stage is the output one, the corresponding loss is 0.24 dB. If these losses are the dominating losses it would obviously be preferable to use the second arrangement and place the X3 stage on the 'input side'. Remembering the conclusions drawn from the example in sect.5.7.3 we see that it is doubly advantageous to place the stage with the highest 'frequency gain' at the input side.

5.7.5 . Conclusions.

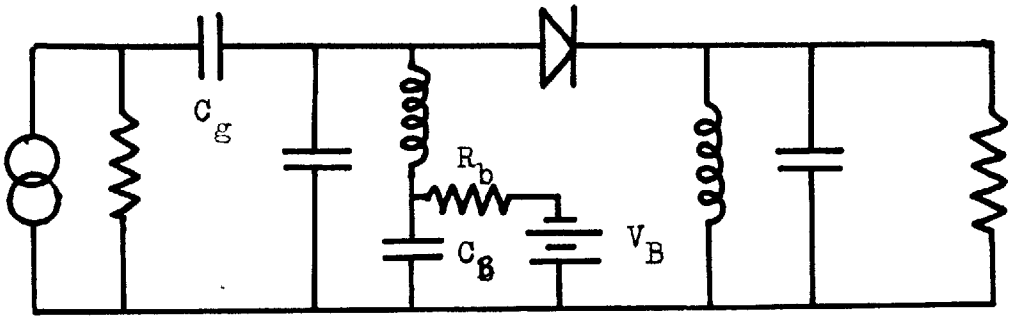
It is apparent from the above examination of cascaded multipliers that their design does not present any undue difficulties. Problems likely to be encountered have been discussed and different methods of cascading have been compared. It has been shown that it is desirable to cascade low order stages if high efficiency is required (refer to sect.2.4.2.1 and sect.4.2.3.) Evaluation of efficiencies using the results of preceding sections has been dealt with.

It is interesting to study the predictions of Johnson[19] with reference to cascading. He takes as an example a specific diode and predicts the efficiency for various orders of multiplication. On the basis of his results it would appear that direct high order multiplication may be more efficient than cascading low order stages. It should be noted however that he assumes a constant filter loss; in most practical cases the filter loss will increase with increasing harmonic number (refer to sect.4.2.3) and therefore must be evaluated for each case. The omission of this

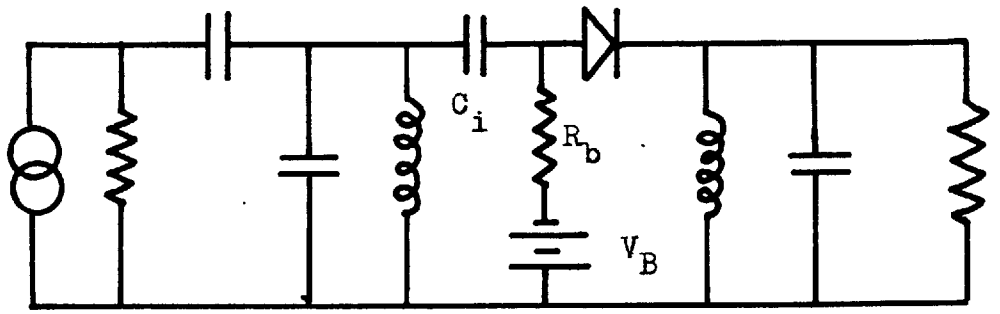
point may account for the fact that he was unable to obtain his predicted efficiencies in practice.

5.8 Conclusions.

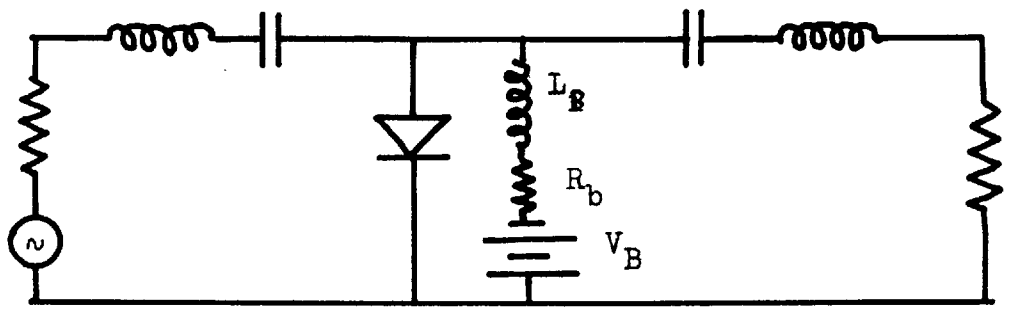
In the present section we have mentioned some of the properties relating to the general behaviour of multipliers. It is obvious that the theory could be extended in most cases but the outline of the effects discussed will normally be sufficient to indicate, in any practical case, the qualitative behaviour to be expected, together with an approximate solution of the magnitude of these effects. In any particular case it would be a simple matter to determine the exact behaviour of a circuit and it is doubtful if a complete and rigorous general solution to the problems discussed above would yield any useful information.



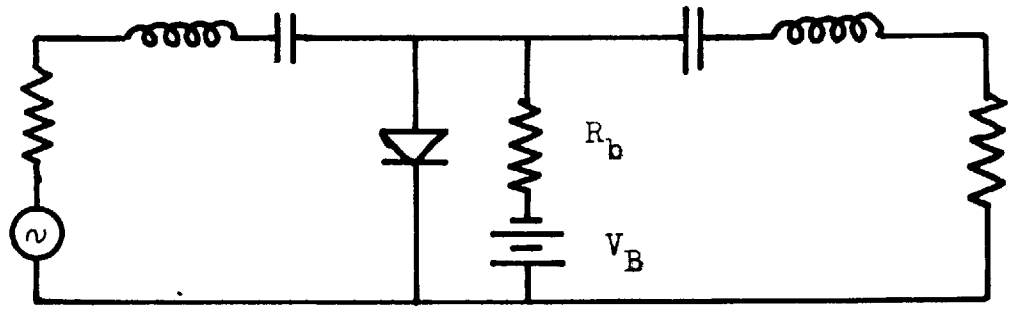
(a)



(b)



(c)



(d)

Fig.5.1 Biasing arrangements.

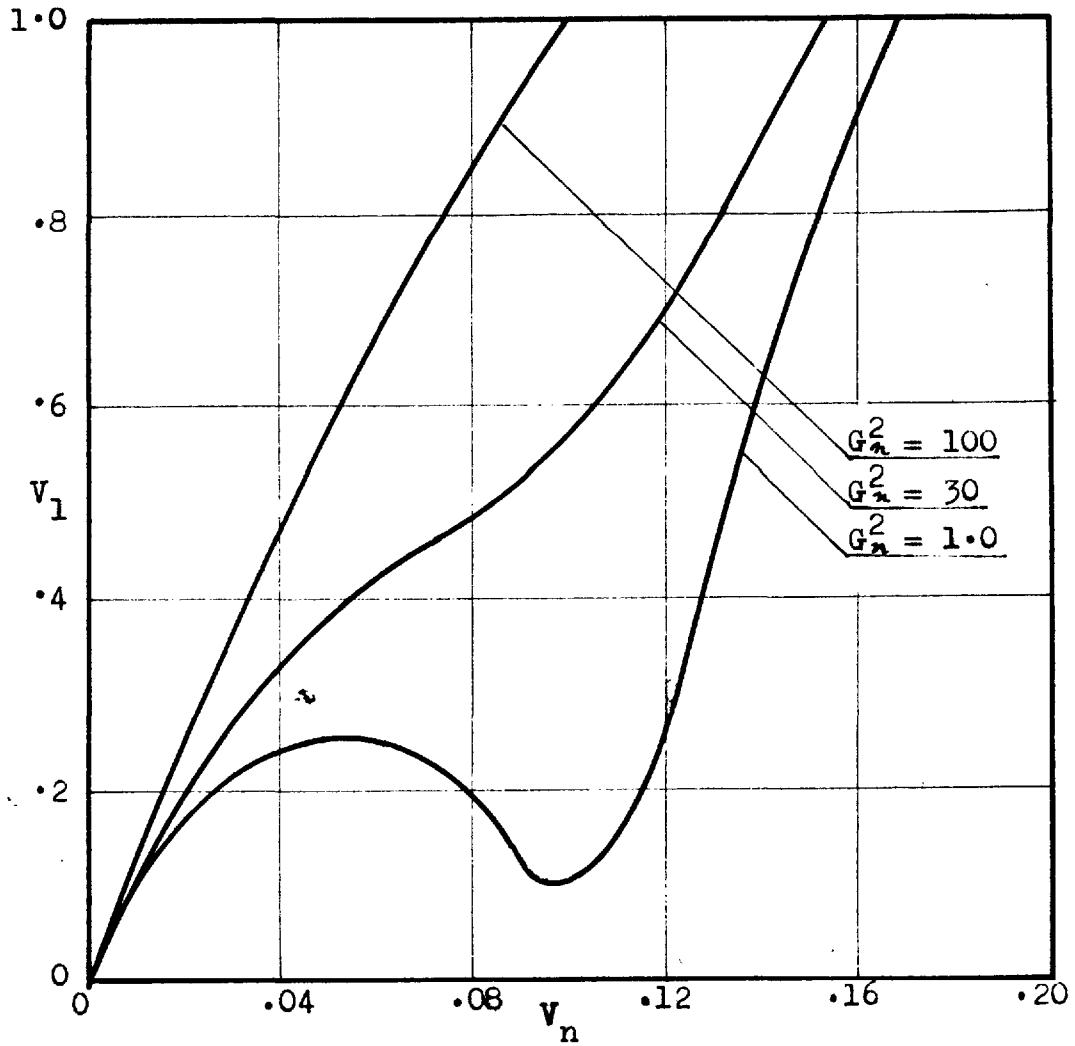
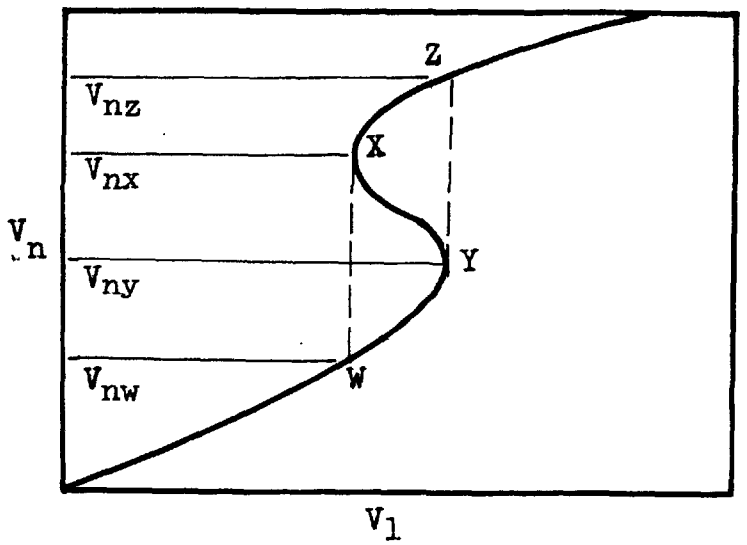
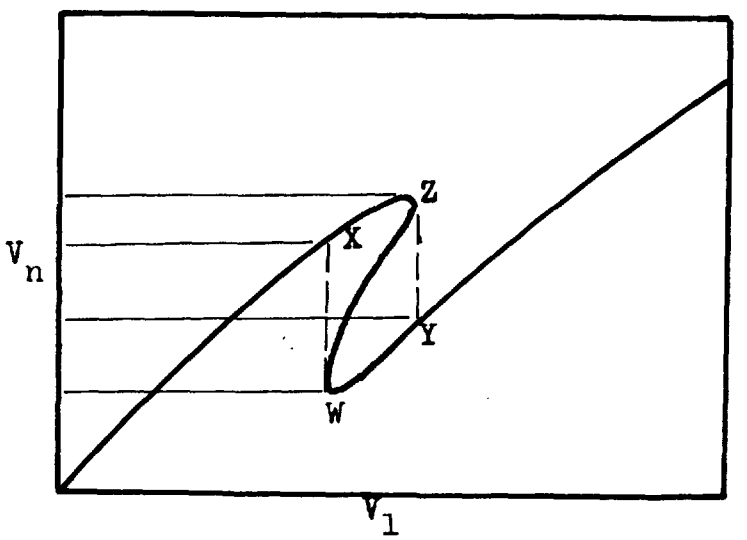


Fig.5.2 Illustration of simple hysteresis effect.



(a) 'Low order' hysteresis



(b) 'High order' hysteresis

Fig.5.3 Two basic forms of hysteresis likely to be encountered.

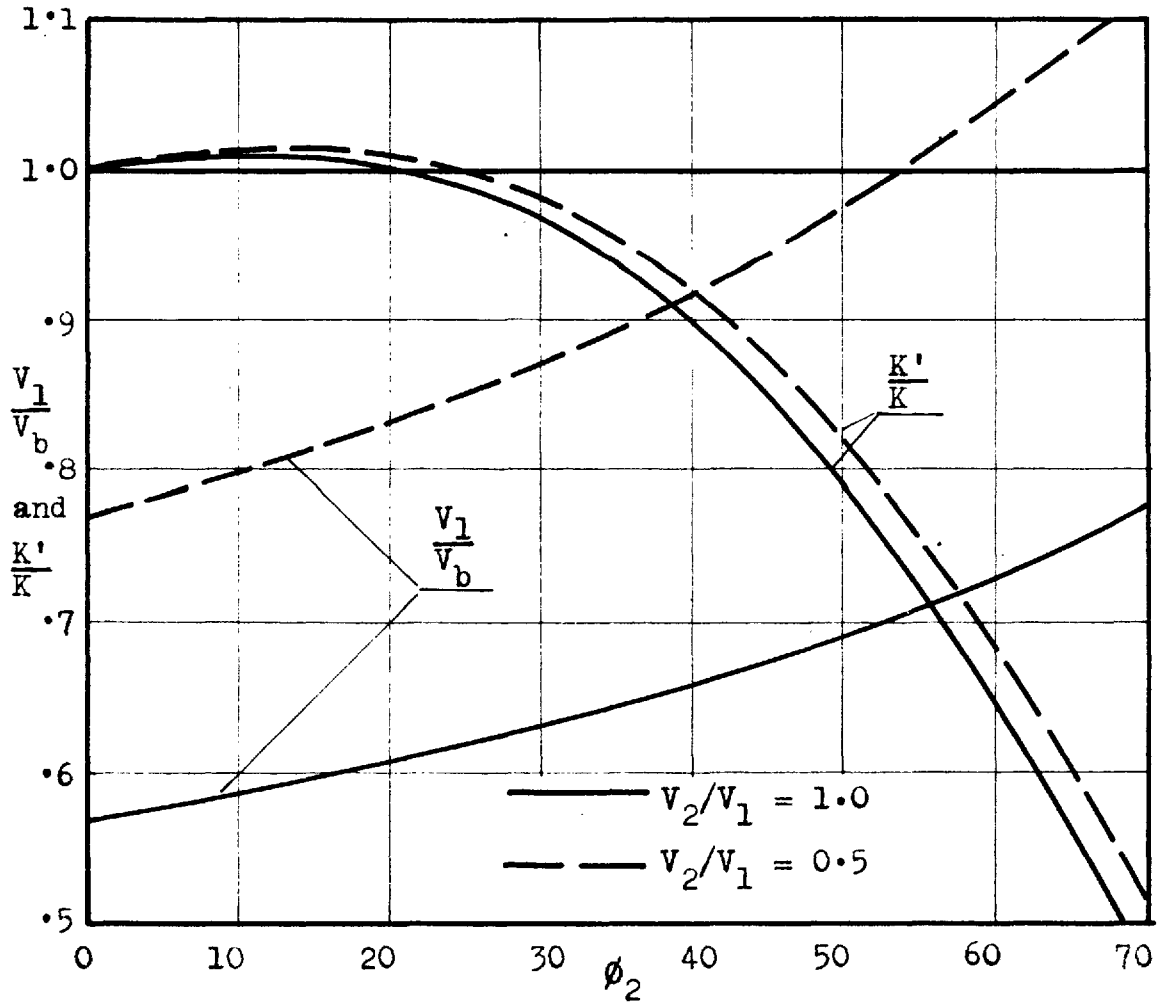


Fig.5.4 V_1/V_b and K'/K curves for a X2 node multiplier related to phase angle ϕ_2.

SECTION 6.

SOME GENERAL EXPERIMENTAL RESULTS.

6.1 Introduction.

In the preceding sections the experimental work has been aimed at verifying specific parts of the theory. The experiments described in sect. 2 were intended to verify the large signal behaviour and were consequently devised to facilitate voltage and current measurements; for this reason the circuits were not optimized for maximum efficiency. It is the purpose of the present section to illustrate the theory with several typical circuits, particular attention being given to power loss; thus the circuits to be described will generally be operating under optimum conditions. The experiments to be described fall into two main categories: (a) low frequency circuits, (b) high frequency circuits. As well as giving results for power loss, mention will also be made of practical difficulties encountered in setting up multipliers, particularly when several stages are cascaded.

6.2. Low frequency circuits.

6.2.1 Single stage circuit.

A single stage circuit was constructed with the purpose of verifying the power loss obtainable, particularly under lossy diode conditions. A node circuit as shown in Fig. 6.1,(a) was used. A non-linear capacitance consisted of two Pacific Semiconductor Type V 20 diodes and five G.E.C. Type S.V.C. 3 diodes all connected in parallel and operated with an applied bias of 1.5 volts; the total capacitance was

120 pF. and the 'Q' factor at 6 Mc/s . was measured to be 100. From the values shown in Fig.6.1 the following information is obtained:

$$\alpha_1' = 3.33, \qquad \alpha_2' = 2.5$$

where these parameters are defined in Appendix 4.1. Using the results of Appendix 4.1 we obtain the values of the parameters used in sect.4.3.2, thus:

$$E_1 = 0.75, \qquad E_2 = 0.785$$

whence,

$$\alpha_1 = 4.45, \qquad \alpha_2 = 3.19$$

and

$$T_1 = 1.11, \qquad T_2 = 0.687$$

In order that the circuit operated under conditions where the power loss was small, the value of Q_{2t} was chosen so that the value of α_2/Q_{2t} corresponds to a minimum of the power loss curves of Fig.?.14 and Fig.4.2. In fact Q_{2t} was made equal to 17 which gives

$$\alpha_2/Q_{2t} = 0.188$$

which, referring to (4.39), (4.5) and (4.6) gives an 'effective' value (for the diode operating conditions) of

$$(\alpha_2/Q_{2t})_{eff} = 0.188/T_2^2 = 0.40$$

It is seen that this corresponds to a region of minimum power loss on both sets of curves.

The effective 'Q' factors of the inductors may be found by including the coupled loss given in sect.4.3.3. Using (4.58) and (4.59) gives:

$$Q_{1c}/Q_{2t} = 63.5, \quad Q_{2c}/Q_{1t} = 16.0$$

Q_{2t} as mentioned above is equal to 17 and Q_{1t} may be calculated from the value of the generator resistance and the inductor 'Q' factor to be 68. This gives:

$$Q_{1c} = 1080, \quad Q_{2c} = 1100$$

This causes approximately a 10 % reduction in the effective inductor 'Q' factors, i.e.

$$Q_1 = 100, \quad Q_2 = 140$$

The power loss may now be evaluated using (4.43). The value of K may be found for $\gamma = 0.45$ by interpolating between the curves of Fig.2.6 and Fig.2.7, having first of all obtained the value of V_1/V_b corresponding to the value of $(\alpha_2/Q_{2t})_{eff}$ given above from Fig.2.13. Thus:

$$V_1/V_b = 0.81 \text{ and } K = 0.26$$

The resulting calculated value of power loss is 2.1 dB (from (4.7)). Note that Fig.4.6 gives a very good approximation to this loss by taking the average effective value of α_1/Q_1 and α_2/Q_2.

From Fig.2.15 it is seen that the power loss due to the diode ($Q_{dn} = 100$) is about 0.7 dB. From Fig.4.6 it is seen that a loss of 0.1 dB occurs due to harmonic currents flowing in the load. The total power loss is thus 2.9 dB (assuming that the losses may be added; this will not involve significant error since the losses are small, as may be seen by referring to sect.4.2.3)

The input was adjusted until current just started to flow ($\doteq$ 10 μA). Under these conditions the following quantities were measured:

$V_{in} = 1.5$ V, $V_{out} = 0.575$ V.

The value of output conductance added to give the required value of Q_{2t} was 0.715 mmhos. The input conductance was measured by noting the attentuation across R_g and using the measured value of R_g. This gave $G_{in} = 0.242$ m mhos. The actual power loss was thus 3.6 dB. The discrepancy of 0.7 dB between the predicted and the measured power loss may be due largely to errors in the measurements of voltages and resistances.

In order to verify the power loss under conditions where the diode losses predominate, the 'Q' factor of the diode was lowered by adding a series resistance. In order to keep the operating conditions the same, the load was reduced to keep the value of α_2/Q_{2t} the same for each condition, the generator voltage being correspondingly adjusted. The following results were obtained:

With 10 ohm resistance added, diode $Q_{dn} = 18.5$, power loss increased by 1.7 dB.

With 20 ohm resistance added, diode $Q_{dn} = 11.0$, power loss increased by a further 2.1 dB.

Subtracting the loss of 2.2 dB which is not due to the diode gives the following results for diode loss:

$Q_{d2} = 100$, power loss due to diode = 0.7 dB(assume)
$Q_{d2} = 18.5$ power loss due to diode = 2.4 dB
$Q_{d2} = 11.0$ power loss due to diode = 3.9 dB

It is seen that these losses agree closely with the results shown in Fig. 2.14 for various diode 'Q' factors.

6.2.2. Cascaded circuit.

It was decided to construct a cascaded multiplier in order to study the general behaviour and to verify the conditions for this type of circuit already discussed in sect. 5.7. The circuit used is shown in Fig.6.1,(b). It was decided to use values of α which were sufficiently high for the use of additional filtering to be unnecessary. It was also decided to make the voltage gain of each stage approximately equal to unity so that no inter-stage transformers were required whilst at the same time allowing the diodes in each stage to have the same bias voltage (refer to sect.5.7). On the assumption that the losses are small (5.55) gives the condition that the diodes must decrease in capacitance by one half per stage. Since the voltage gain of each stage is unity the conductances at each node will be approximately equal (exactly equal when the losses are zero) and the stages must be all similar. The actual conditions chosen were:

$$C_{o12} = 2C_{o24} = 4C_{048} = 60\text{pF}.$$

$$C_{1t} = 2C_{2t} = 4C_{4t} = 8C_{8t} = 360\text{pF}.$$

whence,

$$\left.\begin{aligned} \alpha_1 &= 6.0, \quad \alpha_2 = 3.0 \\ \text{and} \quad T_1 &= 1.12, \quad T_2 = 0.816 \end{aligned}\right\} \quad \text{for each stage}$$

The inductors used had a nominal 'Q' factor of 200 but the additional losses due to decoupling capacitances and coupling between stages reduced the 'Q' at each node to a measured value of 120.

For the voltage gain of a stage to be unity we have

$$V_2'/V_1' = 1.0$$

which, using (4.25) and (4.26) gives

$$V_2/V_1 = 0.73$$

This corresponds to $V_1/V_b = 0.66$ (from Fig. 2.5)

and $(\alpha_2/Q_{2t})_{eff} = 0.12$ (from Fig. 2.13).

This gives a value of $\alpha_2/Q_{2t} = 0.12(0.816)^2 = 0.08$

Since $\alpha_2 = 3.0$ this gives $Q_{2t} = 37.5$.

This corresponds to a loss at each node of

$$10 \log \left[1/(1 - Q_{2t}/Q_1)\right] \quad \text{dB}$$

$$= 1.6 \text{ dB}.$$

The overall efficiency of the three stages (four nodes) is therefore 6.4 dB. It is obvious that the above method of evaluating the loss is only approximate since the losses are not completely negligible and the voltage gain will therefore not be exactly unity. In practice the following results were obtained:

$V_{in} = 3.1$ Volts, $G_{in} = 0.092$ m mhos,

$V_{out} = 2.0$ Volts, $G_{out} = 0.059$ m mhos.

which corresponds to power loss of 5.7 dB. The voltages at each node were as follows:

$V_{in} = 3.1$, $V_2 = 2.75$, $V_4 = 2.65$, $V_{out} = 2.0$ Volts.

It is thus seen that the approximate method used to estimate the power loss in this case gives reasonably good accuracy. Note also that the curves of Fig. 4.2 may be used to estimate the approximate efficiency very quickly:

$$\alpha_1/Q_1 = 6/120 = 0.05, \quad \alpha_2/Q_2 = 3/120 = 0.025$$

thus the power loss for a single stage is obtained by taking the average value of $\alpha/Q = 0.035$, corresponding to a power loss (at $\alpha_2/Q_{2t} = 0.12$) of about 2.2 dB. In fact since two of the nodes are common the overall loss will lie somewhere between the loss for $\alpha/Q = 0.035$ and $\alpha/Q = 0.035/2 = 0.017$ the latter being (from Fig.4.2) about 1.2dB. The total loss for three stages therefore lies between 6.6 dB and 3.6 dB. The mean of these two values is 5.1 dB which is seen to be close to the loss obtained in practice. Note that if the multiplier consisted of a large number of stages the overall loss would correspond to the lower value since most of the nodes would be common and the effective 'Q' factor of the inductors would be doubled (this has been pointed out in sect.5.7.3).

Regarding the setting up of the multiplier described above, no undue difficulty was experienced. Each stage was constructed and 'tuned' with a load equal to that calculated for the output circuit. On connecting the three stages together (with the loads on the first two stages disconnected) it was found that only slight re-adjustment was required for the optimum operating conditions to be obtained. The bias supplies were each formed by a battery fed through a 1K resistor and the input was increased until a small amount of current(of the order of 0.5 mA.) flowed in each stage. This ensured that each stage was operating under optimum conditions (as far as utilisation of the diode characteristic is concerned) and allowed small variations in voltage drive per stage to be 'compensated for' by the small amount of automatic bias developed across the bias resistors.

6.2.3 Illustration of hysteresis effect.

It was decided to construct a circuit to study the hysteresis behaviour in a single stage. To present favourable conditions for the effect to occur a circuit with a high 'Q' output was constructed. This is shown in Fig.6.2. together with the variation in output voltage as the input was varied. The current flowing through the bias resistance was measured to be less than 0.01 mA. Since the bias resistance was 15K, the maximum voltage developed across it was 0.15 Volts. This corresponds to a change in the bias of 2.3% which, since $C_o \propto V_b^{-1/2}$, corresponds to a change in operating point capacitance of 1.2%. Since the change in capacitance due to the non-linear effect is (from Fig. 2.12) about 20% (at the point where the output rises abruptly, the voltage across the diode at the input frequency was 5.5 volts, i.e. $V_1/V_b = 0.8$) it may be concluded that the hysteresis is in this case being caused by the 'non-linear' capacitance as distinct from being caused by a shift in the operating point (see sect.5.4).

It is apparent that the curve shown in Fig.6.2 corresponds to the form of hysteresis of Fig.5.3. It was possible to eliminate the effect by altering the tuning of the output circuit but only at a sacrifice in maximum efficiency. In general it was found that hysteresis did not present a serious problem at low frequencies probably because of the fact that the circuit 'Q' factors are not sufficiently high for the effect to occur. Some other forms of hysteresis will be illustrated in the high freqency experiments to follow.

6.3 High frequency circuits.

6.3.1 Description of circuit.

The main purpose of constructing a high frequency multiplier was to investigate the general behaviour and to verify that the preceding theory could be applied to the case of a circuit with distributed constants. It was decided to limit the upper frequency to about 1000 Mc/s. and thus to use co-axial lines as basic circuit elements. After some consideration had been given to the problem* it was decided to use G.R. components as a basis for the experiment. The diode available was a G.E.C. Type SVC12. To enable this to be used with the standard G.R. equipment a special mount was constructed, details of which are given in Fig.6.3. A single stage circuit is shown in Fig.6.4. It consists essentially of a generator (whose voltage V_g was monitored by a meter built into the equipment) driving the diode via a slotted line, low pass filter, and matching network consisting of one shorting stub and one variable length line; the output at the second harmonic frequency was fed via a second matching network to a receiver. Both the generator and load resistances were 50 ohm. The bias was fed into the system via $\lambda/2$ line at the output frequency, as shown in Fig.6.4. Since the bias was supplied via a 10K resistance, the arrangement used had no loading effect at the second harmonic frequency and provided an effective short for any fundamental current at the output end of the system. Isolating capacitors were included as shown. With the exception of the diode holder, the circuit consisted of standard G.R.50 ohm equipment.

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* The author is indebted to Mr. F.J. Hyde of the Department of Electronic Engineering, University College of North Wales, for some useful advice on this matter.

6.3.2 Measurements of power loss.

The diode was biased at -3Volts and the input adjusted until a small current flowed through the bias resistance. The input and output matching networks were then adjusted until the output at the second harmonic frequency was a maximum. The output power was obtained by calibrating the receiver with the meter incorporated in the generator (the VSWR under calibrating conditions was checked and found to be substantially unity); the available power was found directly from the voltage read on the same meter at the input frequency. A voltmeter detector was also used as a check to measure the voltage at the output end of the line. ~~agreement between~~ The two readings of load voltage always gave good agreement under optimally tuned conditions. The following results were obtained:

V_g = 5.1 Volts, V_o = 1.59 Volts

I_B = 0.05 mA, hence total applied bias = 3.5 Volts

Input VSWR = 2.0 : 1

The power loss under these conditions is 4.1 dB. By careful trial and error adjustment of the matching networks it was possible to reduce the VSWR to 1.1 : 1 but the overall power loss remained the same. Increasing the bias to 4.5 Volts and re-adjusting the circuit gave a slight improvement in efficiency, the minimum power loss obtained being 3.9 dB.

The manufacturers data for the SVC12 diode gives a nominal series loss resistance of 5.8 ohms. Taking a nominal capacitance of 1pF gives an estimated 'Q' factor of 47 at 600 Mc/s. Referring to Fig.2.18 we should thus expect a power loss of about 2.0 dB (since K is to a good approximation proportional to γ (Fig.2.6 and Fig.2.7), the

power loss for a diode with $\gamma = 1/3$ is approximately double that for $\gamma = 1/2$, for small losses; this may be checked by referring to (2.83)). In fact the measured loss is about double this value. Measurement of circuit losses including the loss due to the bias supply accounted for 0.2 dB. It was therefore concluded that the additional losses were caused by the diode holder; to check this point measurements were made on a G.R., V.H.F. bridge of the 'Q' factor of the diode in its holder at 760 Kc/s. The resulting estimation of 'Q' factor lay between 12 and 4 depending on the side of the holder on which the impedance was measured. It was also found that the 'Q' factor was substantially independent of the bias voltage. This confirmed the conclusion already reached that the losses were mainly in the actual holder.

Since the exact nature of these losses is not known, it is not possible to predict accurately the power loss which they introduce into the circuit. It should, however, be possible to obtain an overall loss which approaches that due to the diode only, by obtaining a suitable mount for the diode. It must be remembered that the impedance level at the diode terminal is generally much higher than 50 ohms (for example referring to Fig.2.14, if the optimum value of $G_{2t}/\omega_2 C_o$ is 0.5 and the diode has a capacitance of 1pF. at 600 Mc/s., the equivalent load resistance is 550 ohms and the equivalent resistance at the input frequency is 3.4 K, this value being evaluated by using Fig.2.13, Fig.2.4 and (2.77)). For this reason it is essential to keep the shunt losses at a low value.

Note that in the above multiplier the optimum operating conditions are automatically obtained by adjusting both the input and output matching networks. The minimum power loss curves of Fig.2.18 are thus directly applicable in the

case where only diode losses exist; this is equivalent to saying that operation is automatically adjusted to be at a minimum of the curves shown in Fig.2.14 etc.

In order to study the performance of a cascaded multiplier, two X2 stages were connected together. The layout of the apparatus can be seen in Fig.6.5. The second stage was similar to the one described above. It was set up independently and when tuning the circuit the input voltage was held at a value corresponding to the output voltage of the first stage. When optimum conditions had been established the output of the first stage was connected directly to the input of the second stage. It was found that slight adjustment of the matching networks was required to give maximum output. Since a degree of automatic bias existed in both stages, the value of applied bias was not critical. The actual ratio of total bias in the two stages was

$$V_{b2}/V_{b1} = 0.8$$

which is somewhat less than unity as predicted by the approximate theory leading to (5.61)(the difference between the above value and the theoretical figure of 0.63 simply implies that the approximations made in deriving (5.53) from (5.52) are not accurately valid). The following results for power loss were obtained:

First stage, 300 Mc/s. to 600 Mc/s.

V_g = 5.2 Volts, V_o = 1.6Volts, V_b = 4.9 Volts

Power loss = 4.2 dB.

Second stage, 600 Mc/s. to 1200 Mc/s.

V_g = 3.2 Volts, V_o = 0.725 Volts, V_b = 3.9 Volts.

Power loss = 6.9 dB.

Two stages cascaded, 300 Mc/s. to 1200 Mc/s.

V_g = 5.5 Volts, V_o = 0.725 Volts

Power loss = 11.6 dB.

The theoretical diode loss for the second stage (assuming Q_{dn} = 23 at 1200 Mc/s.) is obtained from Fig.2.18 (and correctingfor the fact that γ = 1/3 instead of 1/2): this gives a loss of approximately 3.5 dB. The overall loss for the two stages should thus be 5.5 dB, if the diodes were the only cause of power loss.

Some measurements were also made with the diode connected across the line instead of in series as was the case in the above experiments. The results obtained were substantially the same as those given above. This is what one would expect in view of the fact that the 'equivalent' 'Q' factor of the diode is reduced by the external losses.

6.3.3 Behaviour when input is varied.

There are two main points of interest to study when the input is varied in amplitude: (a) the input/output voltage or power relationships, (b) the nature of any hysteresis effects.

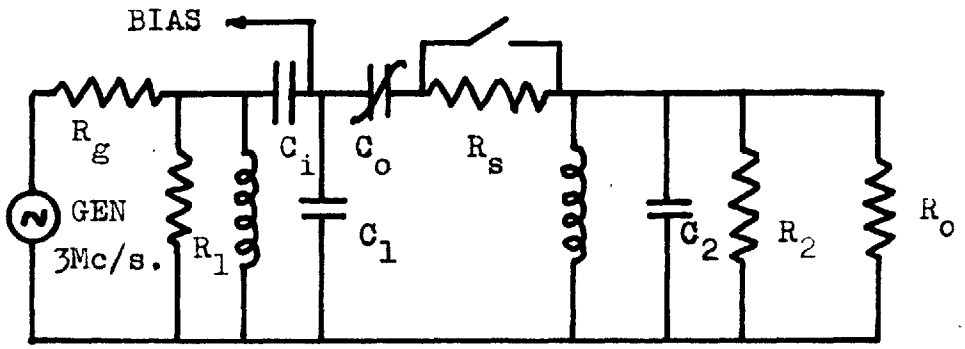
The input/output relationships for the circuit in which the diode is series connected (described above) are shown in Fig.6.6. It is seen that in the case of both the single stage and the cascaded multiplier the variation of output voltage with input voltage is greater when using fixed bias than when using automatic bias. This is the behaviour one would expect by comparing (5.3) and (5.4) although as has been pointed out in sect.5.3.1, the exact

relationships depend on the loading conditions at the input. In the case of the cascaded multiplier, the change in output for a given change in input is much greater than was the case for a single stage. This is again what one would expect, since any non-linear relationship between the input and the output quantities will be emphasised when two stages are connected together.

No hysteresis effects were observed in the above circuit under normal conditions. In the case where the diode was connected across the line, however, marked hysteresis occured. This is illustrated in Fig.6.7 for both a single and a two stage circuit. It corresponds to the type shown in Fig.5.4,(b). Of particular interest is the hysteresis for the cascaded multiplier. It was found that the optimum operating point, X, could only be reached by adjustment of the circuit tuning. Once point Y or point Z had been passed it was impossible to attain point X again without re-tuning the circuit. This illustrates the fact that these effects can present undesirable problems and may make the setting up of the circuits very difficult.

6.4 Conclusions

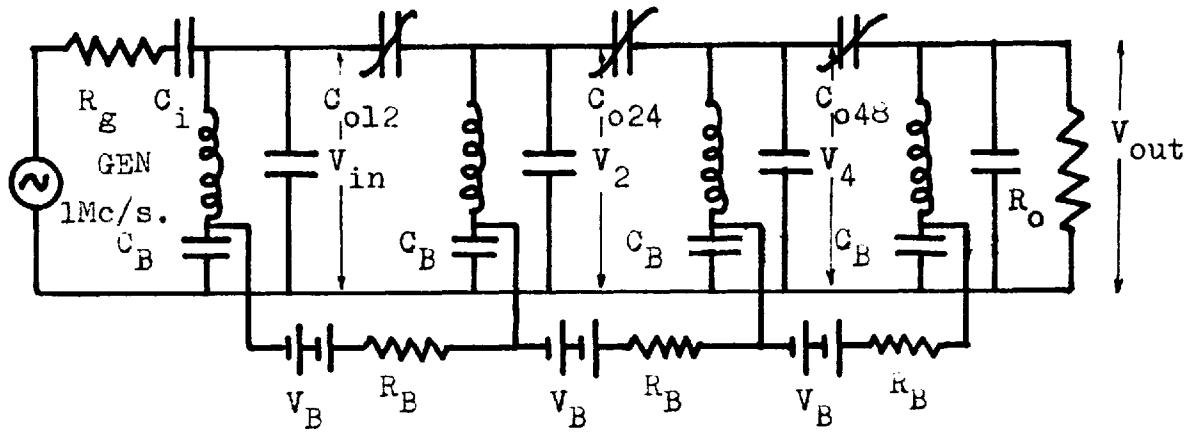
The performance of typical multipliers has been illustrated at both low and high frequencies. The agreement with the theoretically predicted efficiencies was reasonably good in the former case. When using co-axial line circuits in the range 300 Mc/s. to 1200 Mc/s., it was found that the minimum diode loss was not obtainable, due to losses occuring in the diode holder. This illustrates the fact that to obtain maximum efficiencies using this type of circuit, it is essential to design the diode holder in such a way that all spurious losses are kept at a low level. Behaviour of the circuits when the input was varied was as predicted by the qualitative theory. It was concluded that hysteresis effects may present undesirable problems in V.H.F. circuits.



$Q_1 = 110$ $\qquad$ $Q_2 = 160$

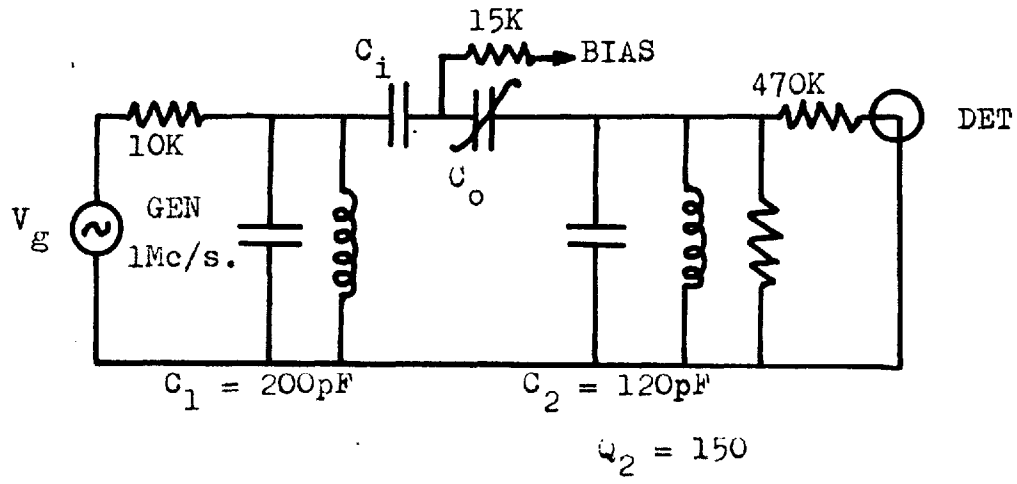
$C_1 = 400$ pF. $\qquad$ $C_2 = 300$ pF.

(a) Circuit used for single stage power measurements

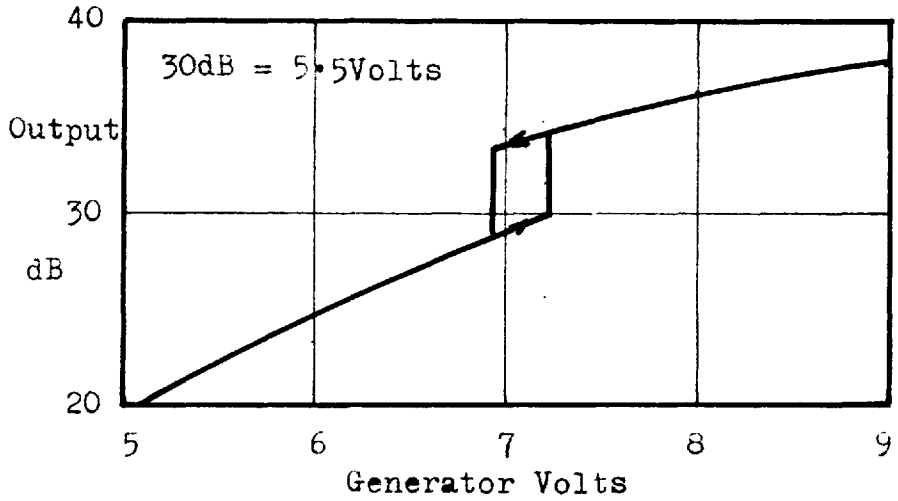


(b) Cascaded multiplier

Fig.6.1 Circuits used for low frequency power loss measurements.



(a) Circuit used to illustrate hysteresis effect.



(b) Variation of output as input is varied (experimental).

Fig.6.2 Illustration of low frequency hysteresis effect.

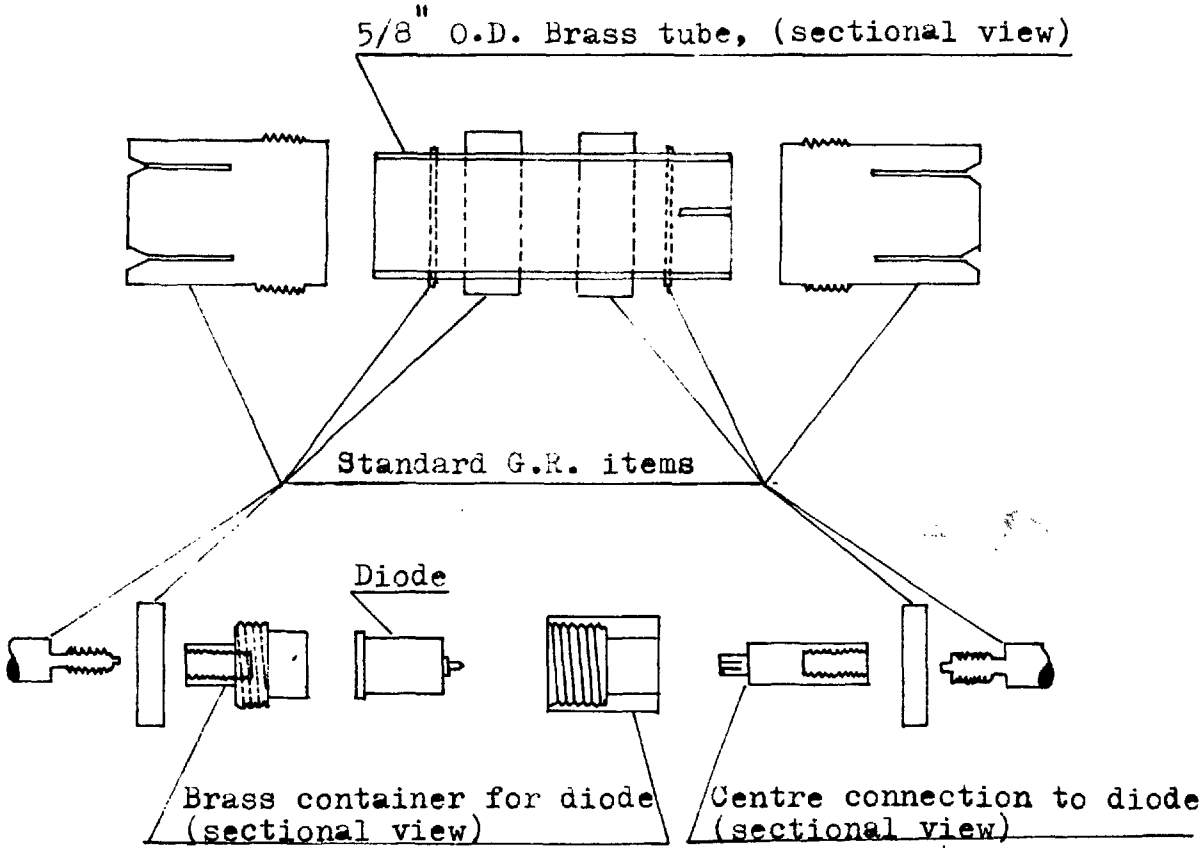


Fig.6.3 Detailed sketch of diode holder assembly.

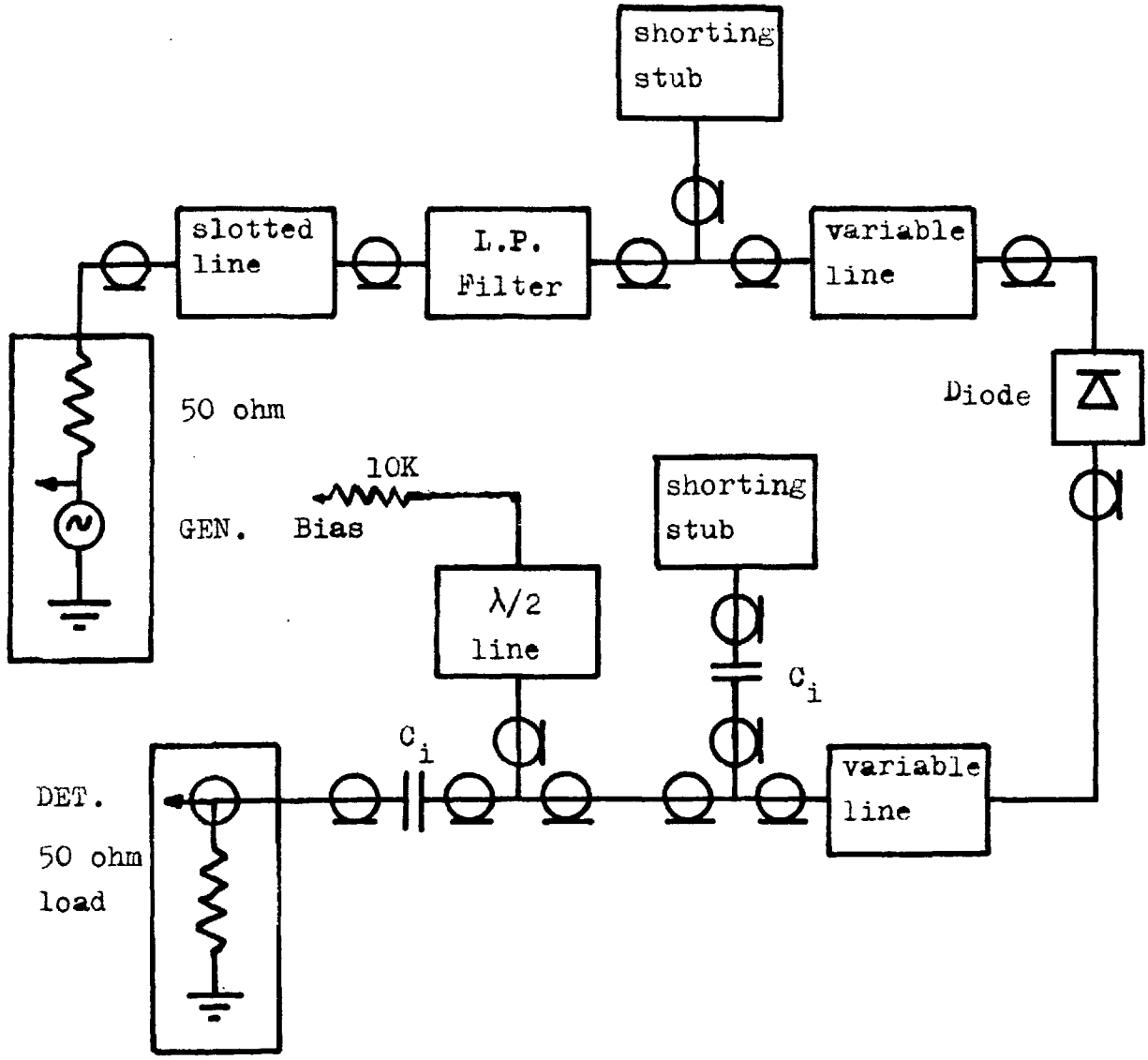


Fig.6.4 Circuit arrangement for single stage V.H.F. multiplier.

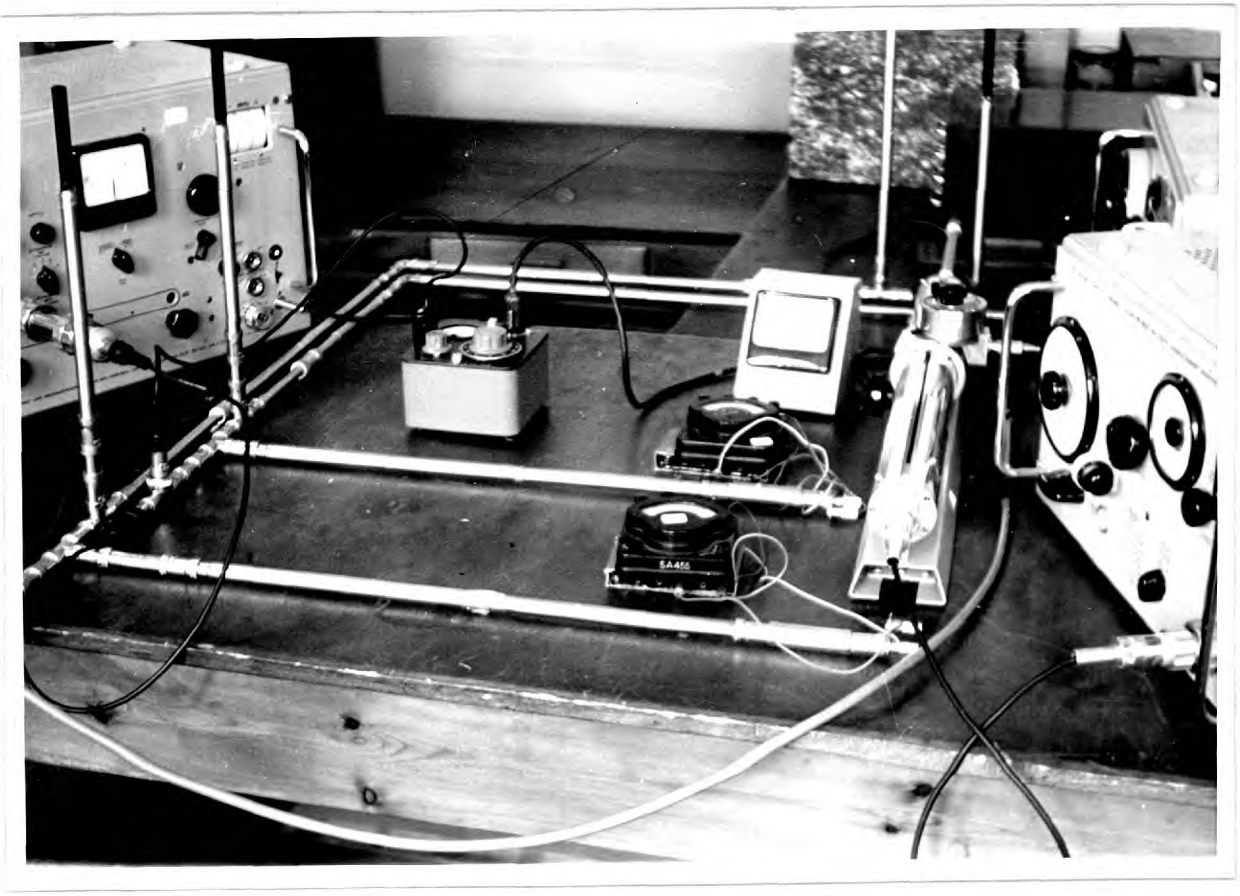
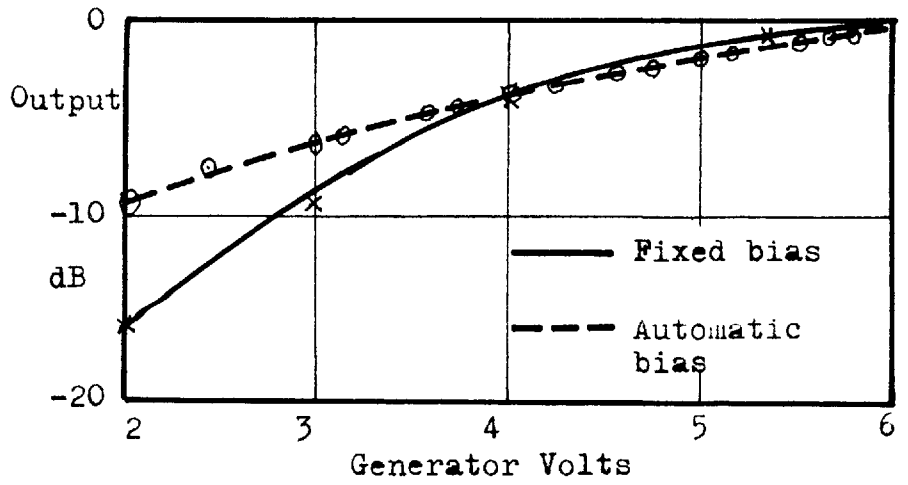
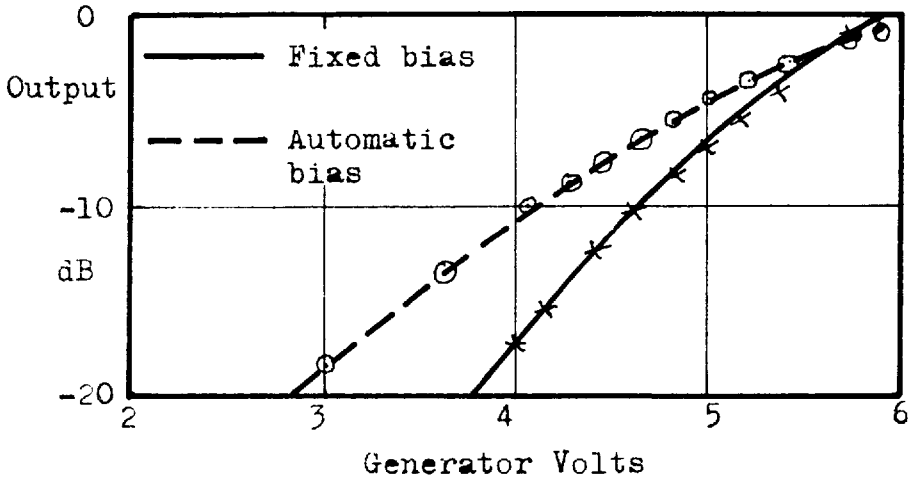


Fig.6.5 Illustration of arrangement of apparatus for a X4 two stage V.H.F. multiplier.

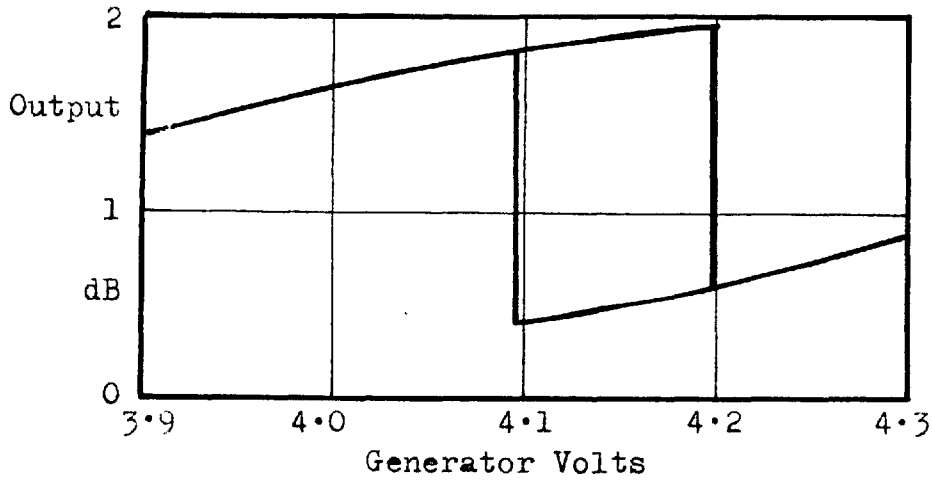


(a) Single stage input/output relationships (measured). OdB corresponds to maximum output.

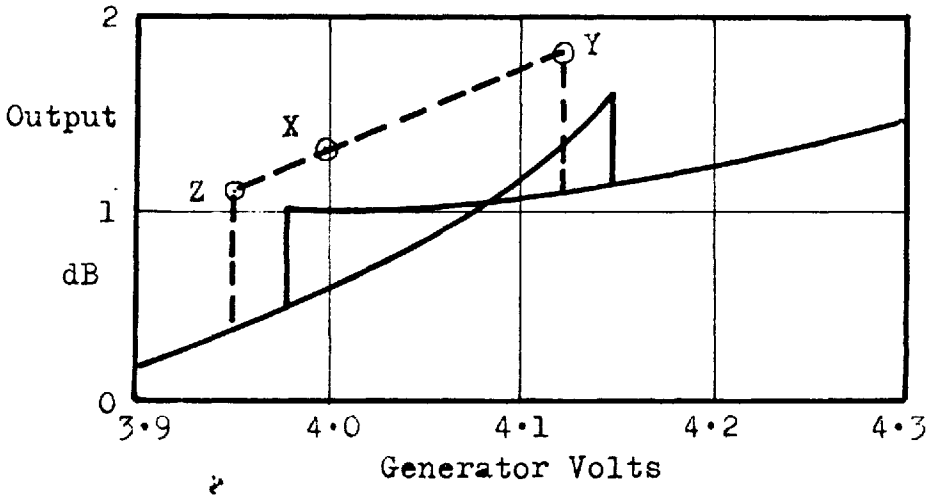


(b) Two cascaded stages, input/output relationships, (measured), OdB corresponds to maximum output.

Fig.6.6 Measured input/output relationships for single and two stage multipliers.



(a) Single stage hysteresis.; 1·9dB corresponds to the output for maximum efficiency.



(b) Single stage hysteresis; 1·3dB at point X corresponds to the output for maximum efficiency.

Fig.6.7 Hysteresis effects obtained with V.H.F. multiplier with the diode shunt connected.

CONCLUSIONS

In the preceding work a complete study has been made of two basic frequency multiplying circuits, using the non-linear depletion layer capacitance of a p-n junction diode.

A large signal analysis has been evolved which is rigorous and generally applicable. The non-linear relation between the input and the output quantities is expressed by the factor 'K'. This factor has been plotted for the specific cases of $\gamma = 1/2$ and $1/3$ for three orders of multiplication ; X2, X3 and X10, for the node circuit and X2 and X3 (the latter only for $\gamma = 1/3$) for the mesh circuit. The results of the analysis are presented in a form which permits the evaluation of 'K' for any order of multiplication and any non-linearity which can be expressed in terms of a series expansion.

Expressions for basic power loss due to both lossy diodes and lossy filters were derived and using the 'K' curves, efficiencies were evaluated for various diode and circuit 'Q' factors. Using these results a comparison of various circuits was made. It was shown that the mesh circuit is only suitable for X2 multiplication and for this order gives the same basic power loss as the node circuit. It was also shown that if a high order of multiplication is required the most efficient method is generally to cascade low order stages; the advantage of this method is enhanced if utilisation of the depletion layer characteristic is limited by forward conduction effects.

A study was also made of sources of additional loss, such as that due to the use of non-ideal filters and that due to unwanted harmonic power being dissipated in the diode resistance or in the load.

The effect of the diode being driven into the region where conduction losses become appreciable was examined by

deriving an approximate expression for the modified 'Q' factor of the diode under these conditions. A separate analysis was performed to determine the ultimate efficiency obtainable when the diode is driven into the region where the forward conduction current is large and where it is operating under charge storage conditions. The optimum circuit conditions were found to be widely different from those for depletion layer operation but as a result of the analysis it is possible to predict the performance of a depletion layer circuit when driven heavily into the forward conduction region.

Some problems which occur in practical circuits were investigated including the following: methods of biassing the diode, effect of de-tuning the output circuit, input/output relationships when the input is varied, qualitative study of hysteresis effects, requirements for matching a circuit to a generator, requirements for cascading stages.

Apart from the basic theory for each stage of the work being verified experimentally, some general experimental work was carried out to illustrate the general performance of the circuits studied. Agreement with the theory was good in low frequency circuits (with the exception of the results for charge storage operation due to the fact that the diode used did not exhibit ideal characteristics). Results on multipliers in the range 300 Mc/s. to 1200 Mc/s. indicate the necessity of limiting spurious losses by suitably connecting the diode to the associated equipment.

As an outcome of the results obtained in the above studies, a sound basis exists for the design and comparison of maximum efficiency circuits using the depletion layer mode of operation for the two basic circuit configurations.

Some problems for further study which derive from the above work are:

Extension of the charge storage theory to cover the case of small forward drive and thus to derive a complete solution for operation in the region between that where the depletion layer effect dominates and that where the charge storage effect dominates. This could most readily be carried out with the aid of a computer to solve the mathematical solution presented in sect.3.

Extension of the study of hysteresis effects to include the case of high order hysteresis and to relate this to practical circuits.

Complete study of input/output relations when the input is modulated.

Study of other modes of multiplication. This has already been attempted by Utsunomiya and Yuan[37] using more than two resonant circuits. A complete large signal analysis of this type of circuit would undoubtedly present an interesting theoretical study.

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