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Memristor Enabled Reconfigurable Analogue Systems

by

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Abstract

The following thesis re-investigates the idea of performing analogue reconfiguration using gyrator-based blocks. By employing memristors, basic impedance synthesis is achieved, allowing to realise PCB-based tunable inductors and capacitors with values as high as 50H and 2nF respectively. Clear limitations of the proposed approach - instability, high noise and limited bandwidth are thoroughly investigated through the use of test circuits such as filters and waveform generators. Accurate mathematical models are then proposed, which describe the behaviour seen in experiments and simulations. The thesis describes the advantages and drawbacks of using memristors in conventional analogue circuits. As the technology is still relatively young, current state-of-the-art devices lend themselves perfectly well in DC application, while high-frequency such as RF still need time. To contrast the use of synthetic inductors and capacitors, other methods are proposed which highlight the particular difficulties in realising true analogue computing machines. Notwithstanding, a generic analogue platform design is proposed which leverages the memristive tuning behaviour and enables systematic reconfigurability on chip. To complement the platform design, several computational methodologies are put forward, which leverage the use of component physics as means of computation, contrary to current digital architectures which are based on logic, commonly characterised by large areal and power overheads. While, the proposed methods do not give a clear answer as to whether field programmable analogue arrays can be realistically designed and used to perform complex tasks, the argument leaves the reader with clearly stated research questions which ought be answered in order to fully understand the scope into which FPAAs can be employed. The work concludes with a description of areas which will benefit from analogue reconfigurable systems, such as space exploration and IoT.

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"I am working on a great invention! It is about confirming the percentage of sugar in sugar depending on the underground radiation in the area. For example, in one store on the shelves, after lying down for a year, sugar has 80 percent sugar in sugar, and in another store, it has 90 percent sugar in sugar, and saccharine has a total of 500 percent sugar in sugar. And thanks to my invention, it will come to the point that you will not have to plant sugar beets at all, that's how much sugar in sugar there will be."

Stanisław Sylwester Bareja, Man – Woman Wanted (orig. Poszukiwany, Poszukiwana)

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Chapter 1

Introduction

The key take away from the introduction chapter is the motivation behind the work carried out in this thesis. The problem description begins with the underlying industry-wide drives: technology, performance and application. Following from the grand motives a relatively minuscule area of research is carved out and presented as the problem to be tackled in this work. Nonetheless its importance and puzzle-like fit in the overall solution is highlighted. The chapter concludes with an overview of the whole thesis.

1.1 Motivation

The pursuit of new solutions nowadays can be attributed to three key drives: technological, performance and application. These are all inter-dependent and stimulate one another. The three drives are explained below. It is their collective impact that motivates the work carried out in this thesis. This will be highlighted at the very end.

1.1.1 Technological Drive

As Yuval Noah Harari writes in his book *Homo Deus* [1], when scientists and engineers mention periods of time, the duration they mean is often made relative to the duration of their grant or fellowship. He argues that *long time* often means fewer than 20 years and *never* rarely exceeds 50 years. There is indeed something to it, as it was just around 30 years ago, that the world saw the World Wide Web for the first time. If 30 years was enough to globalise and unify the world virtually, to a point where anyone in the deepest rain forests of the Amazon, thanks to Elon Musk's Starlink project, can connect to the International Space Station and see the Earth live from the orbit, we can only imagine what the next 30 years will bring.

This rapid development has been summarised by Robert Bryce, an American writer and journalist for a number of prominent newspapers and journals, as *Smaller Faster Lighter Denser Cheaper*¹. Over the years, the scientific community has begun to establish bodies to guide the researchers and set out new challenges in an attempt to sustain the growth. The vast electronic industry is led primarily by the Institute of Electrical and Electronic Engineers. The IEEE every so often releases a set of key scientific questions and problems that the community then tries to address. These sets of problems are referred to as *roadmaps*. Depending on the specific group within the IEEE a different roadmap will be published, to name a few:

1. International Roadmap for Devices and Systems (IRDS)
2. International Technology Roadmap for Semiconductors (ITRS)
3. International Network Generations Roadmap (INGR)
4. International Technology Roadmap on Wide Bandgap Semiconductors (ITRW)

It should be pointed out that ITRS has been replaced by IRDS in 2016. Quite interestingly, the first semiconductor roadmap was proposed before the industry even existed [2], and it is famously known as Moore's Law [3] that has since become a techno-economic model for performance scaling. In short, Moore observed that number of transistors on dense integrated circuit doubles every year. He later revised this observation to a more conservative doubling every two years. It was clear from the beginning that exponential growths cannot be sustained indefinitely; as Moore said it in a 2005 interview at Harvard University: "*the nature of exponentials is that you push them out and eventually disaster happens*". Back then he predicted that the trend will be sustained for at most 20 more years. The technology reaches atomic limits - limits which cannot be overcome in similar fashion as it was done so far; the physical principles governing the behaviour of the new devices significantly change, as the technology enters quantum realm. As of 2021, the law still appears to be holding with AMD leading the industry with their EPYC family of microprocessors, which pack nearly 50 billion transistors each (Rome edition). The industry may expect at least two more years of continued growth as AMD made plans to release further two EPYC chips - Milan and Genoa.

Quantum effects are not the only cause for concern. For a long time Moore's law was accompanied by Dennard scaling. Dennard claimed that performance per Watt would follow the same exponential law. As new technology node would reduce by 30%, the clock frequency would rise by 40% and power consumption would decrease by 50%. This more or less held up until 2010, when leakage currents became too large to be negligible. Hence the reduction in power decrease with each new generation means that as density of transistors increases, so does that power

¹The book focuses around energy generation and one may or may not agree with the statements and views expressed by the author. However the title of the book quite accurately describes the effects of the technological progress to-date.

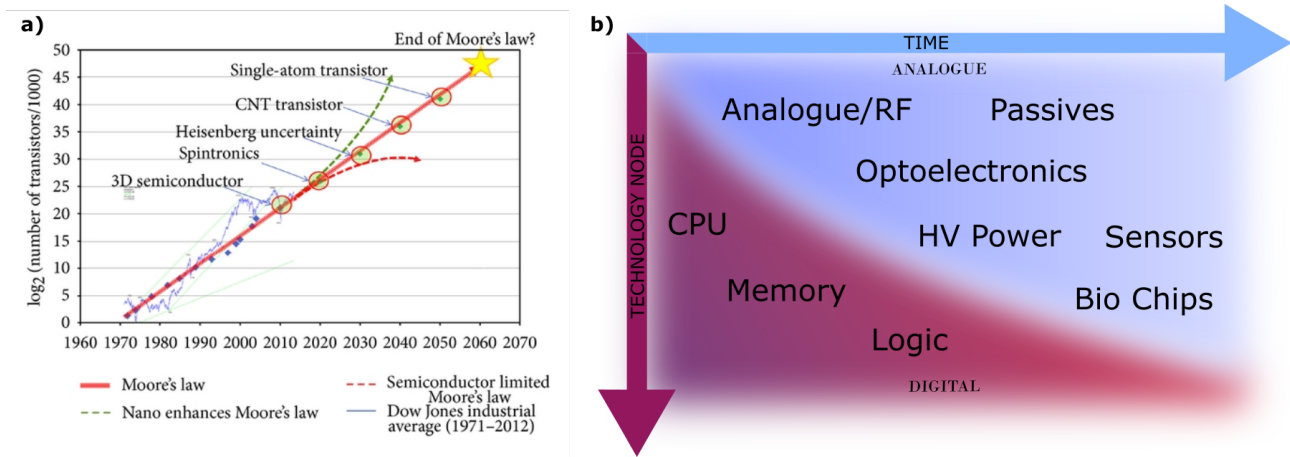


Figure 1.1: Technological drive propelling the electronic miniaturisation and scaling performance. **a)** Forecast of the Moore's Law. Pursuing pure semiconductor approach will reach the Heisenberg's Uncertainty limits and will effectively halt the progress. Nano-enhancements may prolong the continued scaling with a currently projected end date around 2060s. Figure reproduced from [5] under Creative Commons Attribution 3.0 Unported license. **b)** Moore's Law has only applied to digital units. The analogue world, arguably with exceedingly higher value of systems, relies on older technologies. Figure adapted from [6].

density, and as a result things get hotter [4]. Cooling is one of the key challenges currently facing the designers.

It is primarily for those reasons that ITRS has been replaced by a much wider IRDS. It is generally accepted that the scaling will halt in about 4 years in 2025 and alternatives are needed. Some focus in the 2016 ITRS/IRDS roadmap has been reserved to identifying and developing alternatives for Moore's Law. The two International Focus Teams (IFTs) are aptly named More Moore and More than Moore.

More Moore: As there is still some room for further scaling, this IFT is dedicated to finding the last improvements in the performance margins and seeing the Moore's Law come to an end as predicted. One aspect is further dimensional reduction, another is taking advantage of the third dimension and packing more transistors vertically - 3D IC.

More than Moore: This is used interchangeably with *Beyond CMOS*. The IFT is tasked with exploring different ideas outside of CMOS which may maintain the scaling of the performance metrics. Key areas include spintronics, memristors, carbon nanotubes or quantum-dot transistors, collectively called the emerging technologies and materials. More than Moore often broadens the horizon to entail the analogue domain. Moore's Law while it held, only represented the scaling of digital processors. Domains such as analogue, radio frequency (RF) electronics, sensors or optoelectronics benefited from the rapid scaling but did not follow it. Many modern day designs still use technologies as large as 35nm and even 180nm to develop application specific integrated circuits (ASIC).

1.1.2 Performance Drive

Area scaling and increasingly cheaper fabrication is however not the only drive of the industry. Continued Moore's Law expansion is perhaps the result of the pursuit of the improvement in various performance metrics, such as power dissipation, execution of instructions per second or per Watt or any other ones.

Many, such as Mead [7] or Hasler [8] target biological efficiency as the *Holy Grail* of computation. Mead in his seminal paper in 1990 explains the limitations of transistor technology compared to a neural system of our brains. He claimed that our bodies do not use *a mysterious fluid* or rely on some unknown *phenomenon that is more effective than we can ever imagine*. Mead proposes that the solution is simple, and it is the way we perform computation must change, *along* with continued technology scaling. In 1990 the disparity between state-of-the-art and biological efficiency was a factor of 1 million - neurons required energy packets 6 order of magnitude smaller than the best processors, to switch. These days this number may have gone down by one or two orders of magnitude. The main losses come from: architecture, i.e. gate capacitance is only a fraction of the total node capacitance, and from the way we compute - a single operation requires thousands of transistors, as opposed to a single neuron/synapse combination. Mead proposed that we can address this disparity by moving away from discrete logic gates and utilise device physics instead to count. The community needed 14 years to prove this claim - in 2004 Chwala et al. showed huge power savings of analogue versus digital approach [9].

Hasler discusses this issue referring to a different metric - number of multiply-accumulate operations (MAC) per unit power. MAC operation is the fundamental activity of a neural systems. Neurons effectively sum together weighted inputs from their synapses and pass it forward. Therefore, it makes sense to target this metric provided the architecture in question is designed for such operations. Hasler gives an overview of the progress over the decades from the first digital signal processor (DSP) released in late 1970s, which was estimated to perform at 10 MMAC/s/W - 10 million MAC operations per second per Watt. Hasler argues that modern day smartphones have reached the digital limit - the energy efficiency wall, performing at 10 GMAC/s/W - a thousandfold improvement. She claims that further scaling is only possible with analogue approaches. This claim is backed up with a demonstration of an analogue classifier inherently based on MAC operations - a Vector Matrix Multiplication, showing 10 TMAC/s/W, a further 3 order of magnitude improvement over modern day smartphones. A further factor of 1000 is achieved with ASIC analogue neuromorphic realisation in 350nm process of a distinctly bio-inspired algorithm (10 PMAC/s/W) - the dendritic classifier. It is estimated that today's state-of-the-art analogue technology only trails 2 orders of magnitude behind the biological world. Of course, these comparisons are biased, as they consider one problem at a time. The dendritic classifier performs just one operation over and over again, whereas the brain is capable of much more. Considering the versatility of biological systems, the best modern day digital

and analogue systems lack the expressive power and adaptive capabilities and therefore are limited in their scope of applicability compared to our brains.

1.1.3 Application Drive

The ultimate drive that fuels the innovation is the application space. The demand to develop new ideas, to scale down entire systems comes from pure need of creating new devices - human-like machines, intravenous robots, precision instrumentation, deep space and radiation hard solutions, faster communication devices and so on. Potentially the *hottest* topic in modern day engineering is realising artificial intelligence on chip. The domain so far reserved to digital architectures has seen a huge increase in popularity among the analogue community as will be discussed in the next chapter. The vast improvements in performance metrics mentioned earlier, together with the understanding of digital and technological limits, has propelled analogue concepts forward once again.

Harari writes that in the pursuit of god-like features, the Homo Deus² will be prepared to modify or otherwise enhance their body through genetic reprogramming and electronics embedded deep into themselves. While engineers and health practitioners already enable life-changing surgeries, by restoring hearing or replacing a pancreas with electronic modules, there is still a lot to be done before we can comfortably embed powerful electronics. These issues have already been highlighted earlier. From the application perspective, heat generation is a big worry when inserting chips into tissue as they will likely lead to irreversible damage to the host. Area is a big limitation, as well as the performance. However, more importantly one often repeated argument is that our bodies are inherently analogue, and therefore digital solutions may not necessarily be optimal.

1.1.4 Problem Statement

These are all very grand problems, that will require generations of engineers and scientist to tackle. Each researcher adds a brick to the city of knowledge. Looking from the perspective of analogue computation: while it was performed and heavily analysed at the break of the 19th and 20th centuries, the digital methods took over. Nowadays, as we seek to return to analogue solutions, or more accurately *hybrid* or *digilogue*, we need to understand how we can perform computation in this non-binary world. Taking previous models developed by the early electronic engineers and giving them a modern technology twist may just prove ever so more useful.

A key problem that can comfortably be tackled on the scale of this thesis is reconfiguration of analogue systems. Hasler's opinion [10] is that the general public still sees analogue as

²Homo Deus - Human God, the species that Yuval Noah Harari argues will supersede Homo Sapiens.

the backwards and dated systems, while strings of 0's and 1's are the future. This view, perhaps ignorant, is however partially justified. Analogue circuits have often been designed for a single application and purpose. An amplifier always amplifies the same band of frequencies by the predetermined factor, an oscillator produces constant frequency and duty cycle signal, an analogue to digital converter always samples with the same precision and speed. This view needs to change, and what that means is that analogues ought to follow the path of ubiquitous digital systems - registers, flip-flops, look up tables and so on.

In this thesis, research is focused around examining the memristor's and other memory-devices' usefulness in promoting efficient, simple and non-volatile analogue reconfiguration. As memristors are dubbed to be an increasingly important emerging technology, the research has matured enough to allow first circuit applications. This work therefore dives into and looks at systems whose performance is broadened and enhanced through the use of memristors. The applications that are enabled through the technology revitalisation are then scrutinised. It is the possibility of any research that the answer will in fact be negative, therefore no bias towards the end result should be assumed throughout. Memristors may be the answer, but there is no guarantee, as other emerging technologies are competing.

1.2 Objectives

Following from the arguments presented earlier, it was the objective of this research to address the issue of versatile, large-scale and practical tunability. Subsequently, this work attempts to provide some insight into answering the following questions:

- Is the state-of-the-art memristor technology mature enough to be used in conventional analogue circuits?
- Is tuning feasibly realisable with memristors?
- If so, does it enable system level reconfiguration?
- What is the application horizon of the memristor tuned analogue systems and circuits?

1.3 Thesis Organisation

Chapter 1: Chapter 1 introduces motivation behind this project. The problem description begins with the underlying industry-wide drives: technology, performance and application. Following from the grand motives a relatively minuscule area of research is carved out and

presented as the problem to be tackled in this work. Nonetheless its importance and puzzle-like fit in the overall solution is highlighted. The chapter concludes with an overview of the whole thesis.

Chapter 2: This chapter traces the history of analogue memory and system reconfigurability, from early forays into hardware realisations of neural networks, through independent discoveries of resistive switching phenomena all the way to modern day system-on-chip (SoC) embodiment of tunable analogue arrays. The discussion begins with dated methods, that have since gone out of fashion. Present day approaches follow with memristive devices at the heart of the discussion. Digital systematic reconfigurability is then introduced and its long dominance is explained. It is followed by the resurrection of analogue methods - their history and future impact are presented.

Chapter 3: Discussion begins with a theoretical overview of gyrators. Their usefulness in the context of creating variable components is explained. Using bilayered memristors and a PCB test platform measurements of tunable gyrator, inductor and capacitor are presented and discussed. Furthermore, the chapter sheds some light on complex gyrator structures: a formally defined upper bound of the gyrator's performance circuits is presented. Following from gyrator's non-idealities, frequency dependent negative resistors are shown to be realisable. The original contributions of this chapter are: universal impedance scaling circuit; memristive current control; memristor tuned inductor, capacitor and gyrator; theoretical derivation of performance limitations stemming from CMOS processes.

Chapter 4: The chapter's purpose is to present versatility of the building blocks demonstrated in the previous Chapter. Their use as direct drop-in replacement for standard passive elements is shown through low-level applications such as: filters, resonators, oscillators and compensators. The measured results presented in those areas show exciting opportunities for reconfigurable systems. The discussion then continues with simulated memristor amplifiers and an investigation of the consequences of recently reported memcapacitive switching on memristive devices. The novel contributions of this Chapter are: first ever analogue reconfigurable passive systems exhibiting continuity in both time and value, which are not based on redundant design utilising banks of components or data converters, and theoretical and simulated investigation of a memcapacitance read out technique.

Chapter 5: Chapter 5 conducts a theoretical feasibility study of using reconfigurable blocks on large arrays such as field programmable analogue arrays. An architecture is first proposed which would be able to host such large numbers of analogue components. Following that, noise analysis of a CMOS gyrator candidate is presented showing the true nature of these analogue blocks. Assuming that in fact it is possible to realise a platform like that, the chapter discusses in detail one particular application, namely differential equation solving, as it is very ubiquitous in computational methods. Finally, the chapter is concluded with an overview of potential applications of such FPAA and ones that are already being pursued.

Chapter 6: Chapter 6 concludes the thesis by bringing all the main points together. It then puts forward some suggestions for future work which builds upon the results of this thesis.

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Chapter 2

Nature of Reconfigurability

This chapter traces the history of analogue memory and system reconfigurability, from early forays into hardware realisations of neural networks, through independent discoveries of resistive switching phenomena all the way to modern day system-on-chip (SoC) embodiment of tunable analogue arrays. The discussion begins with dated methods, that have since gone out of fashion. Present day approaches follow with memristive devices at the heart of the discussion. Digital systematic reconfigurability is then introduced and its long dominance is explained. It is followed by the resurrection of analogue methods - their history and future impact are presented.

2.1 Introduction

Configurability in its broadest sense refers to one's ability to arrange oneself in a desired pattern. The prefix *re-* that often precedes the word, has a Latin origin, roughly meaning "again" or "again and again". System reconfigurability should therefore be understood as the ability to change the functionality repeatedly. An example of configurable but not reconfigurable system is read-only memory (ROM); the data is *burnt* into the hardware once, and cannot be erased.

To do full justice to the reconfigurable's domain, and to give the reader the broadest picture, two closely linked areas of research are presented in this background material. Reconfigurability (a term heavily used throughout this chapter) owes its success to standalone devices performing the hardware changes. Simultaneously, a single tuning element is not sufficient to realise anything useful or exciting - a whole array of those elements is required. Tuning element choice, architecture and low-level system design play pivotal roles in determining the applicability of a given platform. It therefore seems appropriate that the concept of reconfigurable systems should also be touched upon.

2.2 History of Analogue Tuning Elements

Electromechanical

Analogue reconfigurable platforms heavily depend on continuously tunable non-volatile memory cells. These elements have been researched for at least 70 years. In 1958 an artificial intelligence (AI) algorithm known as perceptron was developed at Cornell University [1]. Although it was first realised as a software, a hardware implementation quickly followed - Mark 1 Perceptron. The AI was used for image recognition with a grid of 20 by 20 photosensitive cells connected to neurons [2]. The continuous value of each neural weight was stored with a rotary potentiometer mounted on a shaft. The weights were automatically updated with electric motors. Since then electromechanical systems went out of favour for a number of reasons: they do not scale very well for larger systems, the mechanical systems are prone to failure, they are power-hungry, are quite inaccurate, take up tremendous amounts of space and are extremely expensive.

Thermistor

Some work has been done in utilising thermistors as interconnects between individual neurons. As current passes through a thermistor its temperature increases through Ohmic dissipation. This in turn increases the resistance, which forms a negative feedback loop allowing it to settle at an equilibrium point. This method however has a drawback, in that thermistors are subject to the laws of thermodynamics making their resistive states time-dependent and the time constants are neither large nor small. A relatively long stimulus is required to bring the devices resistance into desired state, but once the stimulus is removed, the temperature of the thermistor falls relatively quickly. It was estimated that the so-called "half-memory" of such analogue cell was just three to four minutes [3]. However the benefit of this approach was a greatly reduced size over the electromechanical systems.

Optochemical

Optochemical solutions have also been researched in the late 1950's [4]. Photochromic or phototropic films were exposed to flashes of light composed of different wavelengths. Depending on the intensity and the spectral composition of the incident light, the transmittance of the films would change. For example, when yellow light shone on the photochromic film, the film would become nearly 90% transmissive within the majority of the visible light spectrum. However, when the film was exposed to blue light, the transmittance would drop. The transmittance was read-out with low intensity green light, as it was found to affect the film the least. It was however observed that the film undergoes a relaxation process and is therefore volatile. The time

constant for the restorative process is a few hours. The characteristics of optochemical analogue memory cells are presented in Figure 2.1a). As with electromechanical systems, optochemical solutions did not make a significant impact, because of the complexity they introduce into the system design.

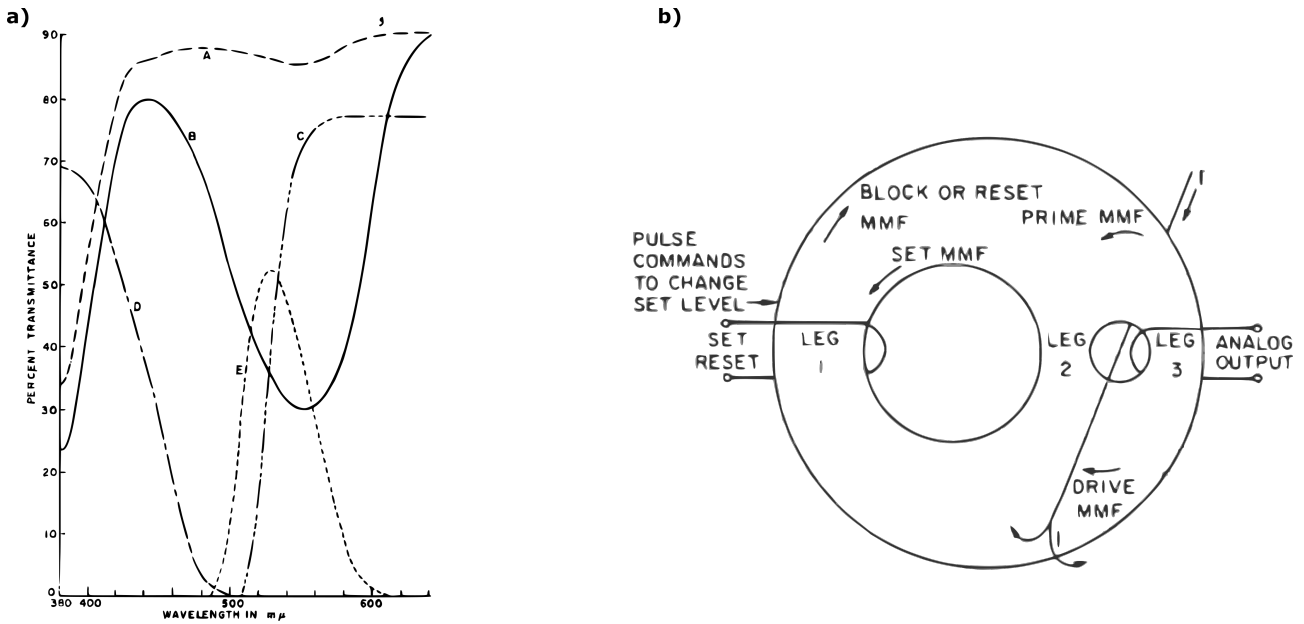


Figure 2.1: Analogue memory technologies. **a)** Characteristics of optochemical memory cells. Curve A represents the transmittance of the film after it was flashed with light whose spectral composition is represented by curve C (yellow light). Curve B shows the transmittance after the film was exposed to light with spectrum represented by curve D. Curve E shows the filter used to "read" the state of the cell, as it interferes least with the optochemical properties of the film. Figure adapted from [3]. **b)** Simple model of a transfluxor. Figure adapted from [5].

Solions

In the early 1960's, solions were considered for memory applications. These are electronic amplifying components used to sense properties of electrochemical reduction-oxidation (redox) reactions. They owe their functionality to a controlled flow of ions through an electrolytic solution. They were briefly used as timers, integrators, transducers and memory elements [6], [7]. They have since become obsolete, with inventions such as the ion-sensitive field-effect-transistor (ISFET) proving more useful.

A solion tetrode memory unit is based around an integrator. It is configured with four electrodes immersed in an electrolyte: an input electrode, shield electrode, read-out electrode and ground electrode. In addition, there are three compartments in a solion: reservoir, barrier space and integral [7]. Reactions taking place in the cell are the decomposition of iodine into iodide ions at shield and readout electrodes, and the reverse at the input and common electrodes. Through careful biasing, barrier is free of charges and the read-out electrode current only depends on

the current flowing from input to common electrodes. The quantity of charge which diffuses from the reservoir into the integral compartment due to the input current is proportional to the integral of that current.

As the authors of the solion tetrode integrator suggest, solions in general have unreliable long-term stability, which was the primary reason for their lack of success. The group reported that based on the fifteen samples they prepared, the memory drift was on average less than 0.5% in a 24 hour period.

Various forms of electrolytic memories have been proposed over time [8], [9], however none of them significantly impacted the field of analogue computing, due to their size, finite life-span (electrolyte would eventually evaporate) and non-trivial integration into larger systems (e.g. orientation of the cells must remain constant).

Transfluxor

The transfluxor was invented in 1956 by J. A. Rajchman and A. W. Lo [10]. The authors presented a novel method of switching and storing information with multi-aperture ferro-magnetic cores. The benefit of having multiple apertures as opposed to single aperture magnetic circuits such as the transformer, is the increased number of flux paths through the legs of the core. This in turn, allows to "program" the core.

A basic realisation is presented in Figure 2.1b). A high power pulse is sent through the winding on leg 1, such that anticlockwise flux flow is produced which saturates the paths 2 and 3. This is indeed possible as leg 1 offers higher flux flow than legs 2 and 3 combined. The two smaller paths will remain saturated after the pulse is terminated. By applying an energising AC signal on the wire passing straight through the aperture, the state of the core is read out through winding denoted as analogue output. When the AC signal induces a flux flow in the clockwise direction around the legs 2 and 3, the flux magnitude in increases leg 3 and decreases in leg 2. However, as both legs were previously saturated, no net change in flux density occurs. When the phase of the AC signal causes the flux to flow anti-clockwise around the legs 2 and 3 path, again no net change is observed as leg 2 was already saturated. Therefore there is no induced voltage on the read-out winding. More details are presented in Figure 2.2.

By careful application of a setting pulse through the input winding, it is possible to reverse the direction of the saturation in leg 2, while keeping original saturation in leg 3. This means that flux along the path 2 flows maximally upwards, while in path 3 it flows maximally downwards. This configuration allows the flux to flow around the smaller aperture as a result of the energising signal on the straight wire. Consequently, the voltage across the output winding is developed.

The scenarios shown represent two extremes - from nearly zero voltage on analogue output winding all the way to some maximum. It is however possible to apply setting pulses such that

path 2 remains unsaturated, thus allowing to create continuous voltages in the given range.

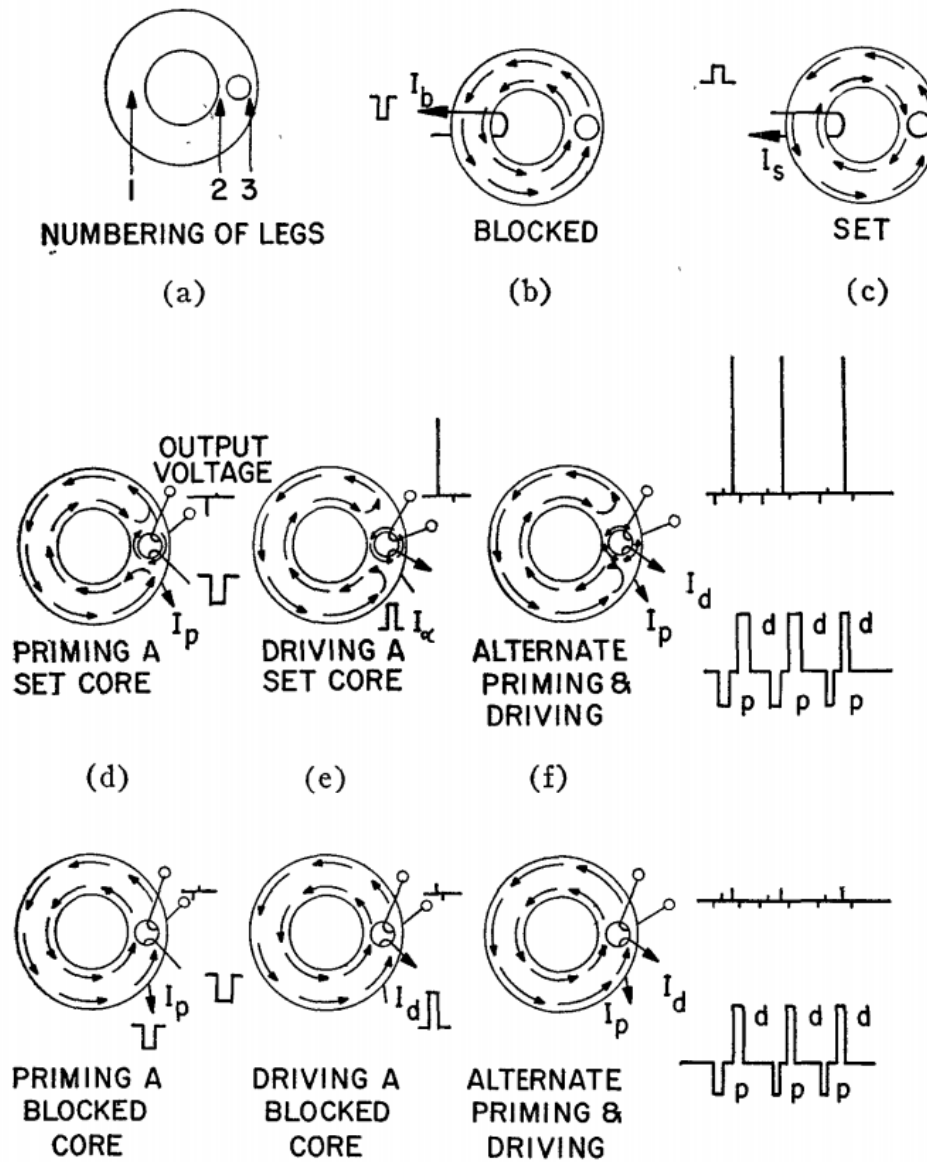


Figure 2.2: Operation Modes of Transfluxor. Figure adapted from [11]. Large aperture is used for writing, whereas small one for reading out data. Each write operation is made up of two pulses - block followed by set. Block pulse (large in magnitude) saturates the flux, whereas the set pulse (smaller than block and opposite polarity) partially unblocks the core, thus storing information. The transfluxor is read out by sending an AC signal through the small aperture to sense the magnitude of the set condition. Subsequently a respective pulse is observed on the read out coil through the same aperture depending on the state of the set condition (high pulses for when larger set pulse occurred as shown in top d), e) and f) subfigures. Bottom subfigures show a blocked condition, i.e. almost no induced output voltage.). For further detail a reader is invited to read the publication by Hammel et al. [11]. *Copyright 1959 Association for Computing Machinery*

At the time the writing process was relatively fast, allowing to store information in just a few millisecond [5]. The stored data could be read-out non-destructively and indefinitely. It had

a reported accuracy of 0.1% at all scale positions. However, non-linearity of the magnetic flux and magnetic field characteristics (B-H curve) made programming rather challenging. Finally it requires high current and relatively high frequency programming pulses, which can make this architecture a source of noise for surrounding systems.

Transpolarizer

The late 1950's saw the development of practical ferroelectrics with nearly rectangular B-H hysteresis loop such as tri-glycine sulfate (TGS) or tri-glycine fluoberyllate (TGFB) [12], [13]. The new materials were used to develop, for example, chopper amplifiers or bistable multivibrators. The common denominator among those systems was a ferroelectric filled capacitor. When multiple such capacitors are used in a circuit and polarisation of the ferroelectric can be individually controlled new circuit possibilities arise.

An application of the newly proposed materials was the transpolarizer, as a method of storing analogue data [14]. The transpolarizer requires two ferroelectric capacitors connected in series to operate. Polarization of one capacitor is held constant with DC bias. By varying the polarization level of the second capacitor it is possible to configure the equivalent impedance of the system. For instance when the second capacitor has the same polarization vector as the first one, the two devices behave as one ferroelectric component and offer a path of low impedance to an AC sensing signal. On the other extreme, if the second capacitor is polarized in the opposite direction, the overall impedance is maximised. Intermediate states are also possible, allowing continuous storage of information. The transpolarizer can be viewed as a small-scale version of the transfluxor presented earlier.

Pulvari in his research of the transpolarizer reported that the impedance ratio of two extreme states (blocked and unblocked) can be anything between 300:1 and 1000:1, depending on the material used. He doesn't however specify the number of feasibly achievable memory states. Nagy in his review paper claims that 30 to 300 discrete values were possible [3]. Finally, the transpolarizer was a voltage-mode device, as it benefited from relatively high input impedance and low output impedance. It may therefore seem surprising, that literature offers no reported use of the device in any practical circuit realisation. However, the idea of using ferroelectric capacitors later picked up, which led to development of ferroelectric random access memory (FeRAM), which will be discussed later.

Charge Integration

Electric charge integration is a method more familiar for electrical engineers and circuit designers. It solely relies on capacitors holding set amounts of charge. This simple idea presents

two problems to the designer: the writing process can be quite slow and reading the device is non-trivial.

Babcock in his PhD thesis in 1960 proposed a solution by designing a "facilitator" [15]. This system was one of the first to simulate neural properties such as spatial and temporal summation, latency and others. However, the design was too complex for any practical use and remained in the research stage.

Since then other capacitor based integrators were proposed [16]. The simplest and most intuitive one is shown in Figure 2.3. Switches S_1 and S_2 control charge or discharge function. When both switches are closed the transistor M_1 acts as a transimpedance amplifier converting the input current I_{In} into voltage V_C . Once the voltage across the capacitor has reached steady state, the switches are opened. Transistor M_2 performs the opposite function of M_1 and converts voltage V_C back to the output current. Based on the relative geometries of the two MOSFETs the output current is a linearly scaled copy of the input. Ideally, after the switch S_2 has been opened, the charge accumulated on the plate of the capacitor C will remain there. However, due to leakage currents caused by dielectric loss tangent, as well as current leakage through the switch and the gate of the transistor, the capacitor will slowly discharge over time, rendering this approach volatile.

Some work has been done to mitigate the drift [17], however it greatly increases the complexity of the cells. A more complex realisation of this circuit is used in analogue to digital (ADC) conversion and is commonly known as sample and hold circuit. This topology works well with ADCs as the hold times are generally quite short, and therefore the leakage currents do not play a significant role.

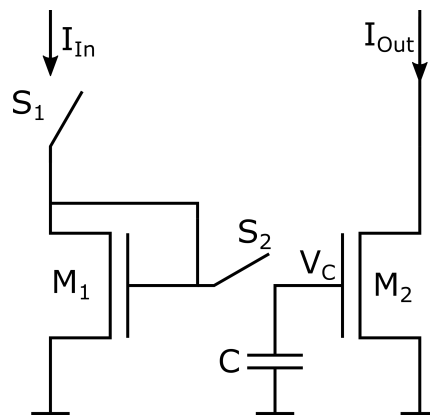


Figure 2.3: Simple current-mode memory cell based on charge integration.

Switched Current Memory

The idea of charge integration has been developed further to allow for high frequency switched operation. Switched current memory, often referred to as SI memory, is effectively an extension

of charge integration, where the charge stored on a capacitor determines the magnitude of the analogue current flowing through the FET device. Since the idea at one point gathered momentum, many different classes of SI memory have been developed, which are briefly discussed here.

The issue with charge integration scheme presented above was charge injection. Every time a switch opens or closes a small quantity of charge flows in and out of the channel. In small signal and fine analogue applications this quantity suffices to make considerable difference. For that reason a Class A S²I analogue memory was introduced. This scheme employs two transistors and four switches. The error due to charge injection is reduced due to the effectively differential nature of the cell.

Naturally the problem with this kind of approach is that it requires constant current flow during write and read operations, even when the input current is zero. Additionally, it was quickly found that the bandwidth of the Class A S²I was in part subject to modulation from input signal. The incoming signals were found to shift the operation point of the FETs, and with that their transconductance - g_m/C bandwidth was found to decrease with low amplitude input signals.

To address the above class AB S²I was introduced. Class AB utilises 4 transistors, which further allows to cancel out error terms leaving minimal error due to charge injection. Its primary advantages over class A cells are constant bandwidth and larger swing of input currents.

Many further classes and little enhancements have been developed. Simple examples includes active removal of charge injection, e.g. when one switch closes and distributes the charge stored in its channel across both its drain and source nodes, another transistor is activated which fills its channel with the injected charge, thus removing any current/voltage fluctuations on that particular node. Further methods aim to reduce the effect of channel length modulation, which often leads to different write and read voltages, due to non-infinite output conductance.

Summary of Outdated Methods

The list of methods presented above is not exhaustive. Throughout the years many other approaches have been proposed such as magnetic flux integration in multi-aperture devices (MAD) [18] or magnetic tapes such those used in VHS cassettes [19]. Magnetic tapes saw possibly the biggest expansion as an analogue memory, being actively used up until the 2000's, when optical systems such as CD-ROM took over. Some derivative systems based on magnetic tapes were developed such as the carousel memory [20], which divided the tape into smaller segments, which were placed on a rotary mechanism. It allowed faster access of information, as it eliminated the need to roll through the full length of the tape to reach the required data.

Nagy [3] conducted a thorough review of analogue memory devices developed and researched up

Method	Levels	Stability	Writing Method	Writing Time
Electromechanical	500	infinite	2 A _{DC}	0.1 s
Thermistor	continuous	5 min	40 mA _{DC}	5 s
Optochemical	2	6 h	High energy flash	-
Solion	continuous	30 days	50 μ A _{DC}	1 s
Electrolytic	2-200	<6 mos	1 mA pulse	10 ms
Ferrite	20-200	infinite	1 A pulse	3-80 μ s
Transpolarizer	30-300	infinite	Voltage pulses	1 μ s
Charge Integration	continuous	6 h	1 ms - 1 s pulses	1 ms - 1 s

Table 2.1: Summary of historic analogue memory devices. Table partly adapted from [3]. Some information from the reference has been updated to reflect developments since 1962.

1962. Although the list above is loosely based on his findings, he discusses also other techniques. Table 2.1 presents the summary of the methods discussed in this section.

In general most of the presented analogue memories did not make it to present day, as the semiconductor technology progression offered much cheaper, much denser and more reliable digital systems.

2.3 Current Approaches

While historically interesting, the old methods are generally inferior to the current methods in many ways: size, power, ease of implementation, scalability and tuning performance. Here, a brief overview of some of the presently used tuning methods is presented.

2.3.1 Micro and Nano Electro-Mechanical Systems

Micro Electro-Mechanical Systems, commonly called MEMS, and the emerging nanoscale technology (NEMS) have enabled microscopic devices with movable components, which can be actuated or reconfigured electronically. The devices are fabricated with two sets of processes. Electronic interface follows classic integrated circuit design and fabrication, whereas mechanical fabrication requires different forms of micro-machining. MEMS is deemed by some communities as one of the most promising technologies of the 21st century.

MEMS devices can be categorized into four subgroups, depending on their application - microactuators and microsensors. Some wish to add third category of microstructures, however by definition all MEMS devices are considered to be microstructures. Both sensors and actuators can theoretically be adapted to respond to different stimuli.

There is indeed a strong case for using MEMS/NEMS devices. The devices inherently yield extremely high-Q filters and resonators, because the mechanical structure is characterised by a sharp resonant peak. Rebeiz [21], [22] shows that MEMS devices exhibit very low losses often below 0.2dB and impressive linearity surpassing GaAs or CMOS devices by 20 to 50dB. The quality factor (Q) is extremely high, due to low series resistance ($0.1\text{-}2\Omega$) - it is often greater than 50, and even surpassing 400 at 2-100GHz.

These qualities allowed the devices to find their way into a growing number of radio frequency (RF) applications, particularly tunable antennas, filters, wideband true-time delay lines and matching networks. A great review of applications and capabilities is available in [23].

However, as with any technology nothing comes for free. MEMS is not a *panacea* - it requires large die area. The device geometry often starts at micron level and can be as large as 1mm for simple components (e.g. variable capacitor) and vastly greater for whole systems. The fabrication is more expensive, as it requires new and specialised processes, e.g. hermetic packaging of MEMS. Finally, the devices are volatile, e.g. a piezoelectric cantilever realising variable capacitance requires constant electric potential [24]. Once the voltage is removed the cantilever relaxes; MEMS therefore can't easily act as non-volatile memory devices.

2.3.2 PIN and Varactor Diodes

Positive-Intrinsic-Negative (PIN) diodes and varactor (also known as varicap) diodes emulate respectively variable resistors and variable capacitors. In the case of PIN diodes, the variable resistance behaviour is observed at high frequencies. Due to its long intrinsic region, which was previously flooded with carriers, the diode operates at high enough frequencies doesn't turn on and off like a standard PN junction. Low frequency operation closely follows that of a standard PN junction. Therefore, for a given PIN device a minimum usable frequency is defined by the mean recovery time, i.e. the time required to fully sweep all the charges from the intrinsic region. The emulated resistance was found to be inversely proportional to the DC bias current through the device - hence a PIN diode forms a current controlled resistor. The emulated resistance can be tuned over 5 decades.

Varicap as the name suggests forms a variable capacitance. This property arises in reversely biased PN junctions, where the magnitude of the reverse bias determines the length of the depletion region. This in turn determines the capacitance of the junction.

These two effects are often exploited in RF filter design - independently [25], [26] and simultaneously [27]. Their advantage is the relatively low size compared to the area of a distributed RF circuit. On top of that, PIN diodes are capable of sub 100ns switching times, can handle high power ($>2\text{kV}$, $>25\text{A}$ continuous) and are an ideal solid state replacement for a mechanical relay [28].

PIN devices are however not suitable for low frequency applications - the resistive behaviour of the PIN diode disappears below certain frequency. Varactors, on the other hand, can switch their capacitance from DC to RF without problems. That is not to say that varicaps are great capacitance emulators. Since the value of the capacitance formed across the depletion region is dependent on the voltage bias, any low frequency signal will effectively modulate that capacitance.

Finally, both types of diode require external DC bias network to be operational, which creates two further issues. The devices constantly require power to be operational and subsequently they are not suitable for non-volatile memory usage: any reconfiguration takes an effect for as long the system is powered on, and must be actively held in its new reconfigured state.

2.3.3 Floating Gate Field Effect Transistors

Floating gate metal oxide semiconductor field effect transistors or FGFETs form an extremely interesting class of transistors. They effectively expand on the functionality of standard MOSFETs by introducing the element of persistent and non-volatile charge storage.

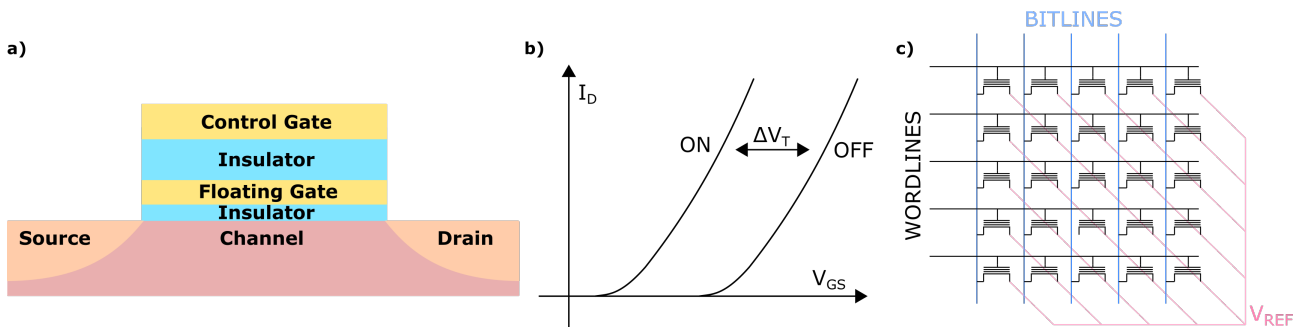


Figure 2.4: Floating Gate transistor technology. **a)** Cross-sectional view of a standard floating gate MOSFET. **b)** Effect of programming the device onto its current carrying capabilities. **c)** An example application - a non-volatile memory crossbar array.

Floating gate transistors owe their name to the physical structure of the device shown in Figure 2.4a. Similarly to standard MOS devices, FGFETs feature a control gate. However a second gate, completely immersed in the insulator is also present. This gate is left *floating*. In fact there could be multiple floating gates in a stack.

While under normal working conditions the inner gates are floating in DC, they are susceptible to AC currents. However, due to the use of thin film insulators between the channel and the gate it is possible to inject some charges onto it. One way of charging the floating gate is to apply a large potential across the drain and the source. As the carriers gain enough energy they avalanche through the channel. Some carriers become 'hot' enough to enter the conduction band of the insulator and deposit themselves on the gate. This process is known as hot-carrier injection or HCI.

Another method of depositing the carriers onto the gate is to apply a large potential difference across source/drain and the control gate. This bias gives rise to Fowler–Nordheim tunneling effect, which is illustrated in section 2.5.1. As the potential difference across the semiconductor-insulator barrier is increased, carriers increase their *probability* of overcoming some of the contact’s energy and tunnel through the band gap.

A rather interesting, however not at all surprising, method of programming the device is exposing it to ultra-violet (UV) light. UV illumination provides photons with sufficient energy in order to excite trapped electrons and allow them to traverse the oxide barrier. However, as Rodriguez-Villegas [29] discusses, the passivation layers in a standard CMOS process are not transparent to UV light. The protective layers must not therefore be deposited during the CMOS fabrication process. This however reduces the longevity of the silicon device.

The charge stored on the floating gate influences the current carrying and switching capabilities of the FGFET. According to [30] the voltage of the floating gate in the presence of gate-source (V_{GS}) and drain-source (V_{DS}) voltages can be estimated as:

$$V_F = \frac{C_{FG}V_{GS} + C_{FD}V_{DS}}{C_{FG} + C_{FD} + C_{FS} + C_{FSub}} \quad (2.1)$$

The subscripts represent the origin of the capacitance: FG - between the floating gate and control gate, FD - to drain, FS - to source and $FSub$ to substrate. Storing charge on the floating gate changes all four capacitive terms and therefore influences the potential of the gate itself. Intuitively, the floating gate voltage is responsible for modulating the current in the channel, similarly to gate-source potential in a standard MOS device. In practice this results in threshold voltage shift as seen in Figure 2.4b. This effect is commonly used to store information in EEPROM or FLASH technologies - as charges, e.g electrons, are injected into the floating gate a larger gate voltage is required to overcome the negatively charged floating gate - thus the device can be in an OFF or ‘1’ state. Removal of the charges results in lower threshold voltage - the device is ON storing ‘0’.

The usage of the devices can be broadly classified into two classes - static and dynamic. In static applications the charge on the floating gate remains constant, thus the operation of the device is determined by the set of capacitances in equation 2.1. Dynamic applications involve the tunneling and injection currents to and from the floating gate.

The capabilities of the technology were showcased in 1989 by Intel [31] with a chip realisation of an electronically trainable analogue artificial neural network (ETANN). The group designed the chip with 10240 synapses realised with floating gate technology. Each synapse cell followed the Gilbert Cell multiplier design [32]: an incoming signal was scaled by the respective weight of the neuron. The network was used to calculate a 64 by 64 dot product - that is it performed in parallel a number of multiply and accumulate operations. The chip was designed with $1\mu\text{m}$

process and it reportedly dissipated 1.5W on average, with peak dissipation of just 2W.

It is not difficult to imagine other applications such as crossbar arrays, representing either a switch matrix or perhaps even memory unit, e.g. Figure 2.4c. In a crossbar architecture individual devices can be accessed by appropriate selection of the word- and bitlines. The device can then be interfaced or programmed to perform specific function, e.g. Hasler *et al.* [33] use the FGFET crossbar as a programmable switch matrix in a Manhattan-style routing fabric.

As with any technology there is a certain price to be paid. As the technology node scales down, floating gate devices are reported to become more volatile. Park *et al.* [34] have shown that a read operation causes the threshold voltage of the FGFET to drift, as the inter-poly dielectric, the dielectric separating various gates of the transistor, becomes thinner.

Programming of the devices is also not as straight-forward. As discussed UV compatibility requires sacrificing the quality of CMOS process, whereas the Fowler–Nordheim tunneling effect requires strong electric fields, and therefore comparably large potential difference across the terminals and/or minimised dimensions. Source [29] estimates that for an oxide thickness of 10nm, 15V stimulus is required, and it grows larger with increasing thickness.

By far the most feasible approach is to program the FGFETs with hot carrier injection, as the voltages involved are a lot smaller. The number of carriers deposited on the floating gate is proportional to the current flow through the drain. As such a fine control of the current source is required and it adds to the chip’s real estate. Furthermore, modelling of the two phenomena - hot carrier injection and Fowler-Nordheim tunneling, requires precise modelling, which is not readily available to circuit designers.

2.3.4 Other

Dynamic Element Matching

The dynamic element matching (DEM) technique became quite successful in the area of high speed, low noise DAC design [35]. DEM is effectively a dynamic averaging of 2 or more components or systems; through the use of fast switching signals with varying duty cycles two resistors of different values can be made to behave as one of an intermediate value. This concept scales of course to higher order systems and becomes more complex as distortion, harmonics and other artifacts need to be addressed with accordingly.

Multi level cells

Standard NAND FLASH memory stores a single bit of information. There exists a notion of multi level cells able to store two, three and even four bits of information, called MLC, TLC and QLC respectively. However, this technology is not fundamentally different to FGFETs presented earlier. In fact, the storage unit is the floating gate device, however the instrumentation around it is the novel contribution allowing to store 8 or 16 distinct, non-overlapping states [36], [37]. As discussed earlier, the challenge in realising more states is the precision in charge deposition on the floating gate. It isn't as straightforward, because it requires very precise models of quantum effects. The pioneers of this technology are Toshiba, SanDisk and Samsung.

2.4 Resistive Switching

Resistive switching devices are currently used in many commercial systems. From the standpoint of chapter organisation, this method is equal to approaches listed in section 2.3. However, since the field is much broader and the effect is used heavily in this work, resistive switching is singled out and discussed separately.

2.4.1 Definition

The resistive switching (RS) mechanism differs from the previously discussed methods, in that RS makes use of natural material properties. Methods such as charge integration, solions or MEMS require whole systems, circuits and instrumentation to store analogue data. RS is often based on nanoscale devices, which alter their characteristics to reflect the magnitude of applied stimuli.

Resistive switching is frequently treated separately to phase change, magnetic and ferroelectric effects. There is some debate, whether these phenomena are in fact dissimilar or that generalisation under a single term RS is justified [38].

This section will follow the majority of the research community and treat the effects separately. This allows a more rigorous definition of the resistive switching mechanism. RS refers to changes in dielectric material properties, which are induced by external electric fields. The material changes result in controlled modulation of the internal resistance of the dielectric film. This is distinct from phase change, magnetic and ferroelectric phenomena and the particular differences will be highlighted in the following sections.

It must be clarified that dielectric breakdown does not constitute a controlled resistance modulation, because it is irreversible. The generally accepted definition of resistive switching requires

that the material changes should be reversible and repeatable. Often a good indication of a device exhibiting RS is an current-voltage dependency (I-V curve) in the shape of a pinched hysteresis.

2.4.2 History

Hickmott [39] first reported an observation of the resistive switching phenomenon in 1962. He used aluminum oxide films, as at the time they were relatively easy to manufacture and presented excellent dielectric properties. The dielectric was sandwiched between two metal electrodes and electric field was applied as shown in Figure 2.5 until conductance was established. As voltage across the dielectric was increased to about 4.1 V there was a sudden increase in the current flow through the film. Upon lowering the voltage Hickmott discovered a region of pronounced negative differential resistance ¹. This irreversible breakdown of an oxide film is however different from a complete dielectric breakdown, and Hickmott termed this phenomenon "forming".

Following Hickmott's revelation the idea of modulating resistance in oxide films was quickly adopted by other research communities. In 1963 Bashara and Nielsen [41] discussed the applicability of thin film sandwich structures containing a dielectric layer of silicon monoxide for memory storage purposes. They were the first to observe and report that these devices exhibit a *memory effect*, because the device "remembered" the most recent voltage stimulus. Furthermore, the group has shown the retentive properties of the structure, claiming that up to 48 hours of storage was possible. Bashara and Nielsen followed their results with 1964 publication [40] where they discussed the relationship of voltage amplitude and the resistance of the device.

In 1967 Simmons and Verderber [42] presented a new thin-film device demonstrating its data storing capability. Notably, they have shown that their device made of silicon monoxide sandwiched between gold and aluminum electrodes has what is called a threshold voltage (V_T). The group demonstrated that the devices can be switched into a resistive state, which can then be non-destructively read-out with voltages whose magnitude lies below V_T . They were also one of the first to attempt explaining the physical phenomena in a qualitative and technical manner. They hypothesised that analogue memory is a result of the device trapping charge between two potential walls.

The most thorough, at the time, investigation of the underlying physical phenomena was conducted by Dearnaley *et al.* [43]. The discussion solely focused on four structures based on thin oxide films - SiO_x , Ta_2O_5 , Nb_2O_5 and Al_2O_3 . However, following the initial excitement, 1980's and 1990's brought little advancement to this technology. This can be attributed to

¹This was later deemed an inaccuracy in analysis. The differential resistance of a device may be defined with reference to its DC current-voltage characteristic only. So the conclusion drawn by Hickmott from the AC measurements was misleading.

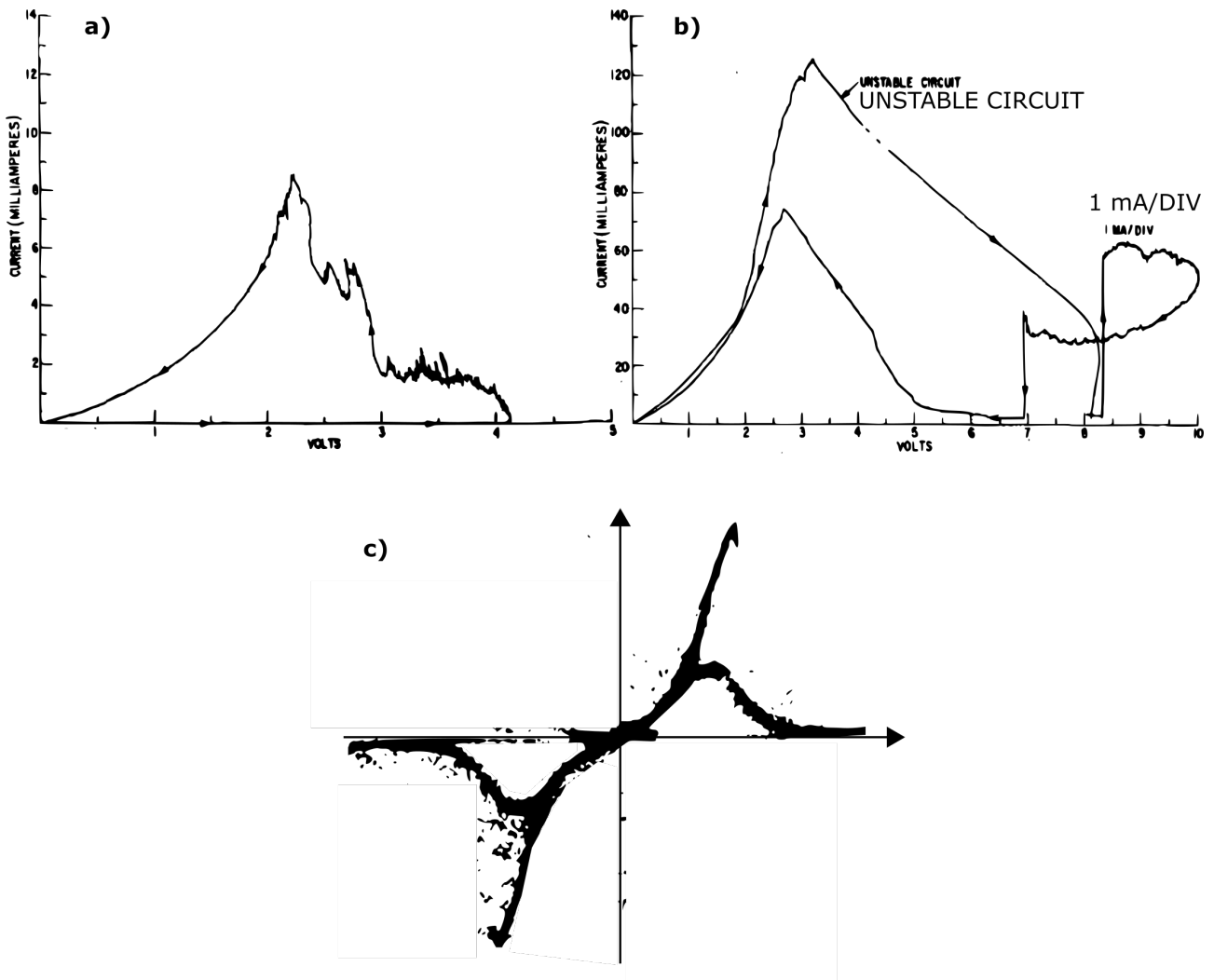


Figure 2.5: Early evidence of resistive switching. Plots a) and b) present results from Hickmott's seminal paper [39]. Plot c) has been extracted from Bashara and Nielsen [40]. Plot a) shows the process of forming the device. Large voltage is applied until conductance is established. Notice small arrows along the curve indicating the progression of the curve is from high voltage to low. Plot b) shows the I-V characteristic after the device was formed. It was estimated that dielectric breakdown voltage of this particular sample was about 15 V. A hysteresis inclusive of the origin is a strong indication that this device exhibits RS. *Copyright 1962 AIP Publishing* Plot c) shows what was first thought to be the first bipolar pinched hysteresis showing initial high resistance and negative resistance. This was later proved to be a misunderstanding of data. *Copyright 1964 IEEE*

two factors. Firstly, the governing physics was still unclear and subsequently control of the RS mechanism was often a hit-or-miss procedure. Secondly, the period before the turn of the centuries has seen significant developments in the silicon-based electronics. Transistor integration and miniaturisation together with immense speed improvements dwarfed the initial interest in the thin-film switching technologies. Notably, this period in electronics was described by Gordon Moore in two of his papers. In 1965 he first proposed based on his observations that the number of transistors doubles every year [44]. 10 years later he refined it to doubling every two years [45]. As a result, the RS technology had been partially abandoned for a number of

years.

Nonetheless, there was some progress, albeit for different reasons. Thin film metal oxides saw an expansion of interest when superconductive effects were discovered in high-temperature cuprates [46]. This led to an improvement in fabrication processes, later allowing the analogue memories to take an advantage of this.

The interest in analogue memory devices once again soared at the turn of the millennia. Two reasons among many should be highlighted. Firstly, the scaling down of silicon devices was incredibly quick (Figure 2.6), leading researchers to realise that this rate of progress would not continue for long. To maintain the continued rise in processing power other solutions would need to be found. Simultaneously the effective device scaling led to decreased drop in performance per power density, meaning that areal savings of the smaller technologies were not met by a comparable decrease in power consumption [47]. In fact, following this metric peak performance happened in 2003 when 90 nm technology was introduced. Therefore, as more processing power is packed into smaller areas, silicon becomes hotter and requires bulky heatsinks. One can argue, that further scaling has a net effect of increased areal consumption.

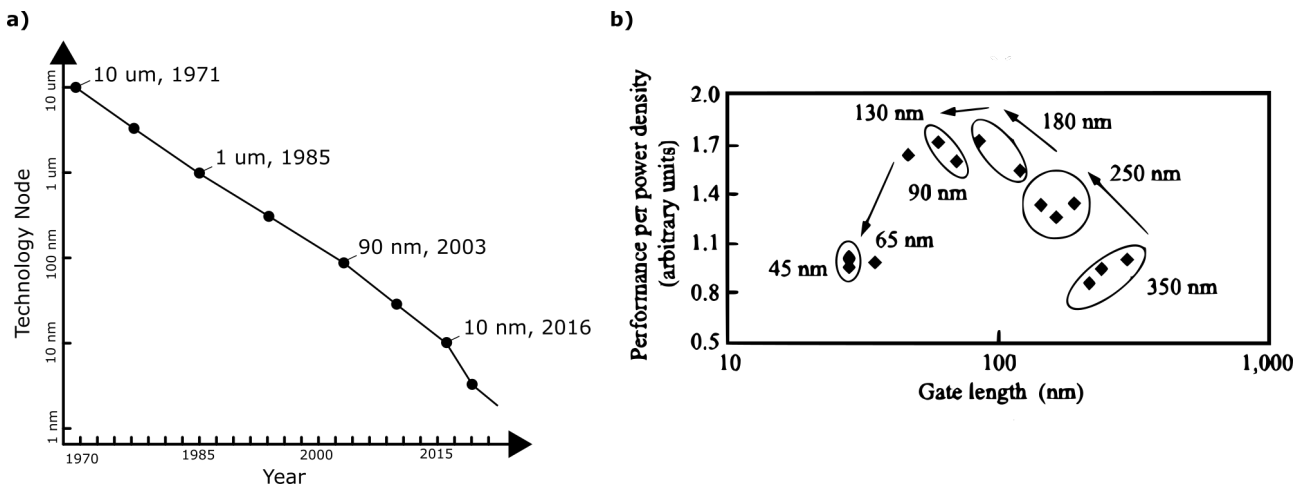


Figure 2.6: Limitations of technology node scaling. **a)** Progression of transistor fabrication technology. At the turn of the century the transistor gate size shrunk to 90 nm. **b)** Peak in relative power performance was achieved around the year 2000, with the 90 nm technology. Further investigation leads to realise that energy required to perform switching operation drastically increases below 10 nm technology node size. Figure reproduced from [47]. Copyright 2006 IBM

As a result, the discoveries reported in 2000 by independent groups led by Bednorz [48] and Igantiev [49] were of paramount importance. Igantiev's group investigated the phenomenon of colossal magnetoresistance (CMR) in manganites of the form of $Pr_{1-x}Ca_xMnO_3$. At room temperature these structures are electrically insulating even with large magnetic and electric fields applied to them. The group however discovered that in thin film structures of this type it is possible to realise gradual changes in resistance through electric pulsing (electric-pulse-induced resistance, EPIR), without applied magnetic fields. They showed that this form of RS is also non-volatile (NV) and report a resistance ratio ($R_R = R_{Max}/R_{Min}$) of around 19.

Bednorz *et al.* demonstrate similar RS effects with oxides - $SrZrO_3$ between two platinum or one platinum and one gold electrodes. In their findings they report 4 levels of switching. Although, it is not explicitly mentioned in their work, the data they present allows to estimate that their structure has an R_R of 15.

In the past, lot of research has been conducted with various materials - amorphous chalcogenides [50], [51], oxides [52]–[56], nitrides [57], semiconductors [58], conducting polymers [59], exotic heterostructures [60] and even organic materials [61], [62]. However, most exciting results are still dominated by the metal oxide groups. Most notably, it is titanium dioxide that is presently at the forefront of many research works concerned with producing feasible memory elements [63], [64]. Table 2.2 shows a summary of some of the work carried out to date.

The resistive switching effect in titanium dioxide has first been observed in 1968 by Argall [52]. He studied temperature and frequency dependent properties of the structures, however the comprehension of the results was limited by the general lack of understanding of the physical phenomena. The study however laid foundations for other works. Notably in 2008, Stanley Williams' research team at HP Labs announced the discovery of a memristor based on a metal-insulator-metal (MIM) structure, with TiO_2 as the insulator [65]. This announcement once again reignited the interest in analogue memory elements.

Oxide	Electrodes (TE-BE)	R_R	Retention (s)	Endurance
HfO_x/TiO_x [66]	$TiN-TiN$	10^3	10^4 in 200 °C	10^5
TaO_x [67]	$Pt-Pt$	10^1	10^7 in 150 °C	10^9
TiO_2 [68]	$Pt-TiN$	10^3	10^6 in 85 °C	10^6
WO_x [69]	$TiN-W$	4	10^7 in 100 °C	10^7
$Cr : Ba_{0.7}Sr_{0.3}TiO_3$ [70]	$Pt-SrRuO_3$	4	10^4 in 27 °C	10^4
$Pr_{0.7}Ca_{0.3}MnO_3$ [71]	$Ag-YBa_2Cu_3O_{7-x}$	10^2	N/A	10^5
$Cr : SrTiO_3$ [72]	$Au-Au$	10	8×10^4 in 27 °C	10^3
$Nb : SrTiO_3$ [73]	$Pt-Pt$	10^2	10^8 in 125 °C	10^7

Table 2.2: A summary of analogue memory properties of the more promising materials. Each of those materials have been shown to exhibit multibit properties, i.e. more than two states. TE and BE represent the material composition of top and bottom electrodes respectively. Endurance represents the number of switching cycles before the device undergoes irreversible changes. A comprehensive review of these and other materials exhibiting resistive switching can be found in [74].

2.4.3 Classification

There is a variety of resistive switching mechanisms documented in scientific journals. As the main interest lies in non-volatile random access memory devices (NVRAM), the main focus of this classification are the enabling phenomena for NV switching. They can be categorized into six main groups. Each group represents a physically different phenomenon behind the RS:

1. Oxygen ion migration
2. Cation migration
3. Electronic effects
4. Phase change effects
5. Magnetic effects
6. Ferroelectric effects

It has become customary to group the first three effects (oxygen ion and cation migration, and electronic effects) together under a unified name of resistive random access memory (ReRAM or RRAM) devices. While other mechanisms can also exhibit resistance modulation, they tend to be treated separately.

A brief discussion of the latter four mechanisms is presented. Following that, the focus will shift towards the ion migration mechanisms presented in section 2.5.

Electronic Effects

Electronic switching mechanisms include metal-insulator transition (MIT) and charge trapping. MIT is also known as Mott transition, named after Nevill Mott, who was the first to investigate the phenomenon of insulating conductors [75]. The devices exhibiting this phenomenon are called Mott insulators.

Under conventional band theory some structures are thought to be conductive, however upon measurement they show insulating properties. This discrepancy of theoretical and practical results arises due to electron-electron interaction, which is not covered by the electronic band theory. Insulators are characterised by a large energy separation of valence and conductive bands. That means, in order for an electron to become available for conduction it must be brought up from the valence band and therefore a large potential energy has to be applied to allow this. In conductors, there is no concept of a band-gap as the two bands overlap in terms of energy, and thus the electrons are naturally available. However band theory is considered a one particle quantum mechanics as it deals with each electron individually. To explain the Mott transition multi-body quantum effects must be considered such as electron-electron interactions.

In practice this means that compounds such as *NiO* [76] are expected to be conductive, given that it has a partially filled 3d-band. However, due to strong Coulomb repulsion between the electrons (correlation effect) *NiO* at rest behaves as an insulator. Having said that, it is possible to control or switch Mott insulators between the two states [77], by varying external parameters such as pressure, temperature, magnetic or electric field.

Charge trapping is altogether a different form of switching. In short some MIM structures form Schottky barriers at the interfaces between the layers. Schottky contacts feature a rectifying effect, meaning they allow unipolar current flow through the device. The potential barrier developed at metal-insulator interface dictates the minimum required external bias to allow the charge to flow freely. Charge trapping and detrapping mechanism is based on controlling the magnitude of the Schottky barrier [78], thus modulating the minimum external electric field required to establish conduction. However, as the contact isn't lossless, parasitic resistance will develop whose magnitude will be directly determined by the charge trapping effect.

Phase Change Effects

Phase change memory (PCM, PCRAM) devices make use of chalcogenide alloys, whose lattice can be rearranged. Along with atomic structure variations, the material alters its electric characteristics, including conductivity. The idea was first presented and patented in 1966. Notably, in 1970 Moore, known mainly for the Moore's Law, along with his colleagues presented 256 bit *read-mostly memory*² based on the phase change effect [79]. Although from the perspective of the functionality the idea seemed perfect, there were some key issues, such as high switching energy, which led to expansion of the rivaling FGFET flash memory.

The phase change occurs when a material switches for highly resistive, disordered or amorphous state to a highly conductive, ordered or crystalline state. Intermediate states are also possible, thus enabling the multibit property of PCM. State change in materials such as germanium-antimony-tellurium (GST) alloys occurs when the material is heated. This can be either induced externally or a self-heating scheme can be employed. An adequately long current pulse with low amplitude can heat a GST alloy up to a temperature of 200 °C, where the device switches into low resistance state (LRS). Conversely, a short, high-amplitude current pulse can melt the material, bring the atomic structure into an amorphous state. Due to the temperature based events, the phenomenon is highly power inefficient compared to modern day technologies, and workarounds are heavily researched. A comprehensive review of the PCM technology can be found in [80].

Magnetic Effects

Magnetic or magnetoresistive RAM (MRAM) arises as a result of spin-transfer torque (STT), spin-orbit torque (SOT) or domain-wall (DW) motion in magnetic materials.

STT-MRAM device is made of tunneling layer interposed between fixed and free magnetic layers. The whole magnetic tunnel junction (MTJ) is placed between top and bottom electrodes.

²Read-mostly memory (RMM) is a form of read-write memory. However, the writing process is usually long or inefficient, so the devices are mostly used to store one set of information, e.g. some EEPROM.

While the magnetic moment of the fixed layer cannot be altered, the free layer can be reversibly changed. The tunneling layer is made of a non-magnetic insulator such as Al_2O_3 , which acts as a spin polarizing filter for the tunneling electrons, resulting in a spin-polarized current [81]. The magnitude of the current flowing through such a structure is modulated by the tunnel magnetoresistance (TMR). The direction of the moment in the free layer is controlled by the polarized current, giving the effect its name. STT-MRAM is in LRS when the magnetic moments of both layers are parallel. When the moments are anti-parallel MJT exhibits HRS [82]. This is analogous to light passing through two sets of polarised filters. If the filters polarize the light along the same dimension, some light passes through. However when the filters are misaligned, most of the light is scattered.

Spin-orbit torque memory (SOT-MRAM) is seen as a competitor of the STT version, as it is faster, denser and more power efficient. As opposed to STT devices where switching occurs through the injection of a current perpendicular to the stack of layers, SOT devices operate by injecting an in-plane current to another free layer positioned adjacent to the one in the stack. With this method, separation of current paths for write and read operations is achieved, which is highly beneficial [83].

The domain-wall memory (DW-MRAM) is based on altogether different architectures. It is composed on nanowires made of permalloys. Magnetic domains are moved along the wire using spin-polarized current. As the leading research group at IBM puts it: the DW-MRAM "*is fundamentally a shift register*", where the movement of bits (individual domains) is controlled by the electric current [84]. Along the wire are positioned magnetic heads performing read and write operations. As the idea is still being researched, it is thought that the final working prototype would offer data density higher than conventional digital memories, and the write and read operation would be much shorter.

Ferroelectric Effects

Most commonly ferroelectric RAM (FeRAM) takes advantage of dipole arrangement within the structure. From the design perspective FeRAM is similar in construction to a dynamic RAM (DRAM), where information is stored as charge. However FeRAM is NV, as it replaces dielectric with ferroelectric layer in a capacitor, allowing them to retain the data for over 10 years. The ferroelectric layer is typically made of lead zirconate titanate (PZT) or lead titanate ($PbTiO_3$) [85]. Electric fields force alignment of semi-permanent dipoles within the ferroelectric layer, and after removal of the external bias, they retain their polarization state. This is however a binary storage element, so it cannot be considered truly analogue. It also cannot be considered a resistive switching device, as the information is stored in form of polarisation.

RS FeRAM devices are based on ferroelectric tunnel junctions (FTJ), and in principle share similar architecture to capacitor-based FeRAM. Thin layer of ferroelectric material is interposed

between two different metal electrodes and the structure of this type is known as MFM. The resistance modulation is achieved by switching the ferroelectric polarization of the tunneling barrier [86]. However this technology hasn't been fully developed, as the endurance of FTJ-based devices is 8 order of magnitude smaller than the competing DRAM [86].

2.5 ReRAM Devices

Resistive RAM devices can be categorised in two ways: based on the underlying physical phenomena or based on the switching characteristics. When looking from the perspective of physics there are three distinct categories [82], [87]:

1. Electrochemical metallisation switching
2. Valence change switching
3. Thermochemical switching

From the perspective of switching behaviour, there also three main groups, namely:

1. Unipolar switching
2. Bipolar switching
3. Threshold switching

2.5.1 Atomic Perspective

Electrochemical Metallisation

Most ReRAM effects are thought to be filament based, and it is those effects that are most heavily researched for practical applications. The non-filament effects in ReRAM and other RS devices were discussed in the previous sections. Filament effects arise in one of three ways: through valence changes, thermochemically or electrochemically.

Electrochemical metallisation is the dominant mechanism in so-called conductive bridge RAM (CBRAM) [58]. Over the years the concept was called programmable metalisation cell (PMC) [88] and electrochemical memory (ECM) [87]. A basic CBRAM cell is composed of one electrochemically active electrode such as *Ag* and one inert electrode, e.g. *W*, *Pt* or *TaN*. The material sandwiched between them acts as a solid state electrolyte for the positively charged

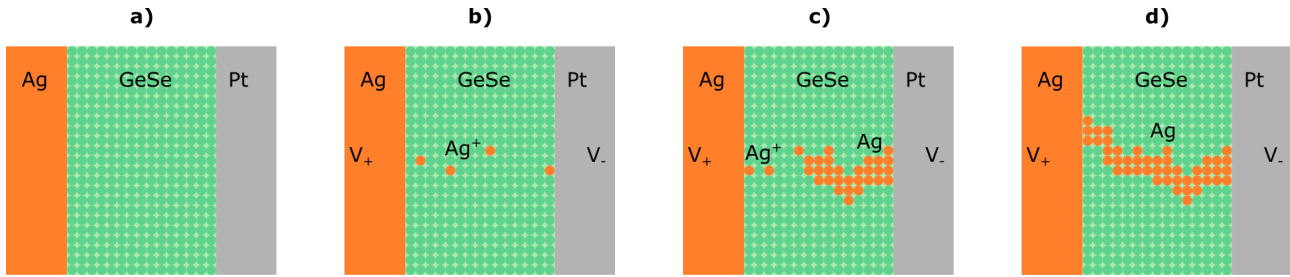


Figure 2.7: Visual representation of CBRAM behaviour. Formation of the conductive bridge resulting in the device switching from HRS to LRS. **a)** The initial resistance of the device is high as the electrodes are separated by an insulating layer. Small flow of current can be observed due to tunneling effects and dielectric loss of the material. **b)** As positive potential is applied to the active electrode with respect to the inert one, anodic dissolution of active material occurs and the ions begin to flow through the electrolyte. Current at this point is predominantly determined by the ionic flow. **c)** As the ions reach the inert electrode, they once again crystallize forming a metallic, conductive path. As the gap between the bridge and the active electrode becomes smaller, more of the current is determined by the tunneling of electrons, which has the effect of modulating the effective resistance of the structure. **d)** Eventually the bridge connects both electrodes, at which point full resistive switching occurs and the device enters LRS. The current is limited by conductivity of the path.

silver ions [82]. The electrolyte is often made of germanium selenide ($GeSe$) or germanium monosulfide (GeS) [87].

The device is initially in a high resistance state (HRS). As positive voltage is applied to the active electrode, above certain threshold potential the metal atoms become ionised, i.e. anodic dissolution of Ag occurs: $Ag \rightarrow Ag^+ + e^-$. The applied external electric field allows the ions to drift through the solid electrolyte, which then accumulate at the inert electrode. The ions then recombine with electrons, forming a conductive bridge of silver atoms between the two electrodes. This process gives rise to the name of this resistive switching mechanism. The current flow at the beginning is limited to the flow of silver cations through the electrolyte, therefore the device can be considered to have a relatively low conductivity. However, once complete bridging occurs, electron flow becomes fully established, dominating the charge flow, and the device exhibits high conductivity (Figure 2.7).

To switch the device back to HRS a opposite polarity is applied across the device, such that silver atoms clustered at the inert electrode ionise and drift back to the active electrode. More importantly, it is possible to achieve multibit functionality by carefully modulating the conductive bridge [89]. This can be achieved by controlling the input (also called compliance) current. Nearly six decades of resistance modulation has been observed using this method [90].

The CBRAM devices benefit from fast switching times, greatly surpassing those of NAND and NOR flash cells [87]. Moreover, the setting speed is directly determined by the magnitude of the applied field. It has been observed that above the ionising threshold, the switching speed is exponentially related to the voltage [91].

However, as the read and write operations share the same current path, this raises a concern regarding destructive reading of the cells. A study conducted by Gopalan *et al.* [92] has shown, that CBRAM cells are relatively resilient to short read pulses. In particular, the group has shown that out of 1344 bits of information nearly none were perturbed by 100 ns long pulses with amplitude up to 1 V.

Valence Change

The valence change mechanism (VCM) arises in some transition metal oxides (TMO, e.g. a bilayer Ta_2O_{5-x} / TaO_{2-x} structure [56]) and manifests itself with a drift of oxygen vacancies, resulting in build up or rupture of conductive filaments (CF). The filament-based behaviour of VCM devices was first directly observed by Kwon *et al.* in 2010 [93]. In general, VCM is conjectured to be triggered by the movement of oxygen vacancies (V_O) [94], [95], which act as donors in some metal oxides. The distribution of the conductive vacancies strongly determines the device resistivity, with CF showing the largest range of effective resistances. Under large external field, soft dielectric breakdown occurs, resulting in the generation of pairs of V_O and O^{2-} . The resulting vacancies and anions drift towards the cathode and anode respectively. The interface of anode and oxide accumulates the oxygen anions as either neutral non-lattice oxygen or in the form interfacial oxide depending on the electrode material [95]. This effect leads to localised deficiency of oxygen inside the oxide, which in turn promotes the build up of CFs. This is known as the SET process where the device is brought from HRS to LRS.

During RESET process the vacancies and oxygen anion recombine to form once again insulating oxide. The CF therefore no longer bridges the two electrodes, this is called rupture. This process can therefore be compared to CBRAM effect, however the conductive material is generated within the oxide, as opposed to being deposited by the active electrode.

The effective width of the insulating layer is dictated by the number and length of CFs. Even though, the CFs don't always bridge both electrodes, there is a number of phenomena that contribute to MIM structure conduction [94]–[96] (Figure 2.8):

1. **Schottky Emission:** also called thermionic emission, occurs when thermally excited carriers overcome the energy barrier E_B and enter the conduction band of the insulator. The current is given as:

$$I = I_{SE} e^{A\sqrt{V}} \quad (2.2)$$

, where I_{SE} and A are material and geometry dependent parameters [97]. In an ideal scenario, the interface at which the Schottky barrier is located is free of traps, very few electrons are conducted in this way in the reverse bias. However impurities, resulting

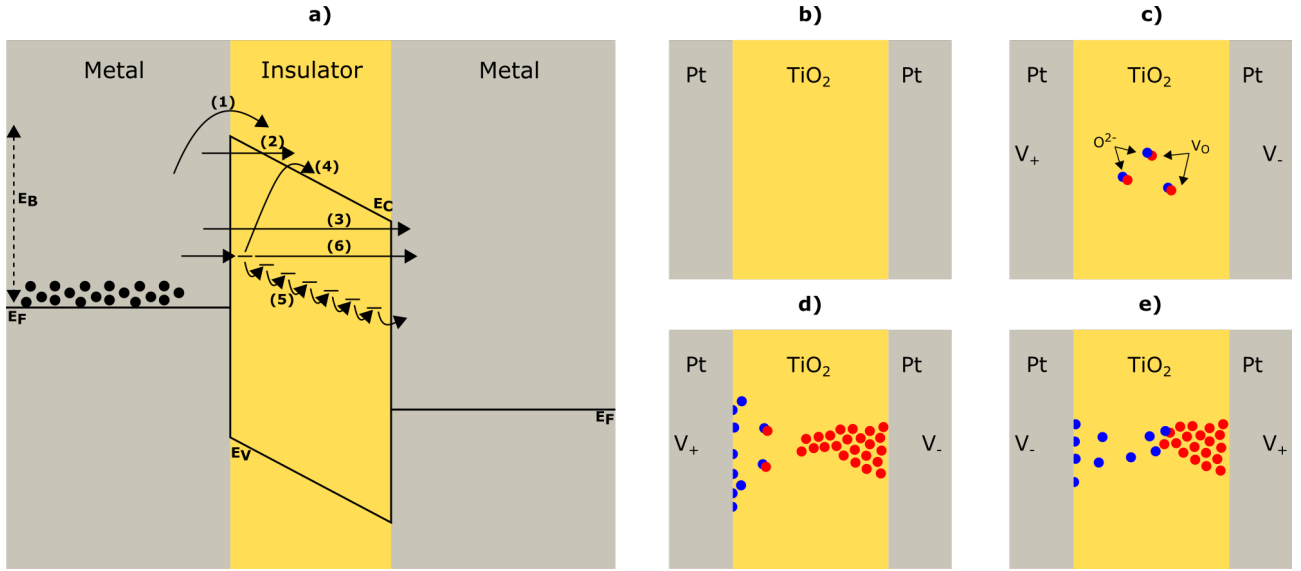


Figure 2.8: Resistive mechanism in VCM, MIM structures. **a)** Visual summary in the form of energy band diagram of the first six conduction phenomena listed earlier. E_F on both metals represents the Fermi energy level, E_C and E_V are the conduction and valence band energies respectively and E_B is the barrier energy required to bring an electron from E_F into E_C . **(1)** Schottky emission, **(2)** F-N tunneling, **(3)** Direct tunneling, **(4)** P-F emission, **(5)** hopping and **(6)** TAT. **b)** MIM cell in pristine state. **c)** Applying bias, stimulates generation of oxygen anion and vacancies, which are then pulled to the respective electrodes. **d)** SET: Over time, the vacancies accumulate forming a conductive path for electrons, while oxygen anions are discharged. **e)** RESET: Upon reversal of the bias, oxygen anions recombine with the vacancies, thus modulating the geometry of the CF.

in considerable amount of electron traps, effectively decrease the rectifying effect of the barrier in reverse bias.

2. **Fowler-Nordheim Tunneling:** Electron tunneling over the triangular region of the insulating bandgap. This tunneling phenomenon is more often observed in thicker insulators. This conduction mechanism results in a vastly different I-V characteristic:

$$I = I_{FN} V^2 e^{B/V} \quad (2.3)$$

, where once again I_{FN} and B are sample specific parameters. The current is highly non-deterministic as conduction is derived from electrons' escape probability. F-N tunneling can co-exist with other forms of conduction, in particular, there exists a special case commonly referred to as Schottky-Nordheim barrier, where the ideal triangular barrier is decreased by certain amount. In this case the F-N defined current is scaled by a correction factor defined by the field-induced barrier change [98].

3. **Direct Tunneling:** Direct electron tunneling is the dominant tunneling effect in oxides thinner than 3 nm. The electrons tunnel across the full width of the oxide in the bandgap region. In general however, direct tunneling often encapsulates other tunneling

phenomena such as F-N. A general description of tunneling current is given by [99]:

$$I = \frac{\alpha e^{-\beta(V)}}{(\gamma(V)K_B T)^2} (\text{sinc}(\pi\gamma(V)K_B T))^{-1} (1 - e^{-\gamma(V)eV}) \quad (2.4)$$

, where α and K_B are Richardson and Boltzmann constants respectively. β and γ are field dependent parameters, representing varying behaviour at positive and negative biases.

4. **Poole-Frenkel Emission:** Due to impurities in oxides, there may exist discrete energy levels within the bandgap available for electrons to occupy. These electrons can be thermally excited into conduction band, similar to Schottky emission. However the energy required do so is dictated by the depth of the trap. The current that is established through Poole-Frenkel emission takes the form [97]:

$$I = I_{PF} V e^{C\sqrt{V}} \quad (2.5)$$

5. **Hopping Conduction:** Electrons can also tunnel from traps with higher energy to ones with lower energy across the width of the insulator. This was observed for example in bilayer devices used in this work, reported by another group [100]. Interestingly, nearest neighbour hopping (NNH) mechanism is used to explain the temperature dependent current through the device. It has been shown that conductance of bilayer devices based on Al_2O_3 and TiO_2 is:

$$G(T) = G_0 e^{(-T_0/T)^\alpha} \quad (2.6)$$

, where G_0 is reference conductance at temperature T_0 . The group found that α is approximately 1.

6. **Trap-Assisted Tunneling:** TAT mechanism is similar to direct tunneling, however the electrons first tunnel to the nearest trap (e.g. V_O) before continuing to the metal. This is a two-step process and forms yet another disambiguation of the general tunneling process.
7. **Ohmic Conduction:** Some electrons are thermally generated at energy levels high enough to allow free movement. This process is different to Schottky emission, because the carriers aren't excited into higher energy states to overcome the barrier. Additionally, Ohmic conduction may be established when oxygen vacancies form continuous conductive filament, i.e. bridge the bandgap barrier. Standard Ohmic relationship is then observed:

$$I = \frac{n(T)\mu_v e V}{D} \quad (2.7)$$

, where $n(T)$ is the temperature defined carrier concentration

8. **Ionic Conduction:** It is possible to observe ionic current under the influence of strong electric field. This process is similar to diffusion through the oxide.

Thermochemical

The thermochemical mechanism (TMC) is also based on redox reactions within the MIM structure. However, as opposed to the electrochemical stimulation, the generation of CF is attributed to thermal effects. The MIM device (NbO_2 or NiO is often used [101]) in its pristine state, will have some parasitic conduction, as listed earlier. As the current density rises, the device undergoes Joule heating. This leads to increased conductivity of NiO . One has to be careful however, not to exceed certain heating point, called thermal runaway. Beyond that point thermal induced irreversible dielectric breakdown occurs and the device is damaged.

As with VCM, appearance of CFs in TMC devices is thought to arise as a result of generation of charges. In NbO_2 it is thought that the oxide splits into niobium cations and oxygen anion which are then pulled apart. While oxygen discharges on one electrode, niobium filament builds up on the other electrode [102]. Once the current compliance is reached, the voltage across the device drops, the filament cools down and its structure is frozen in place.

The RESET operation is performed without the compliance current, such that the current through the device can rise above the value during the SET process. This activates an abrupt change of the resistive state, turning the device off. It is thought that the heating of the CF causes a sudden rupture of the filament thus breaking the conductive path and increasing the resistance. This process can be repeated. Because of its behaviour, TMC is often called fuse-antifuse mechanism [82]. Importantly, TMC does not require opposite polarities for the SET/RESET operations, as the process is purely thermal.

2.5.2 Behavioural Perspective

In the previous section, we discussed differences between different ReRAM devices and their mechanisms on an atomic level. While it is important to understand the physical phenomena controlling the switching mechanism, circuit and systems engineering is a phenomenological or behavioural study of applications of such mechanisms. The devices can therefore be classified based on their electrical characteristics. Three main categories of devices can be identified, namely: bipolar, unipolar and threshold switching devices. They can be easily identified based on the I-V characteristics (Figure 2.9).

Unipolar Switching

Unipolar switching occurs when SET and RESET operation take place with potentials of the same polarity, e.g. in some TMC devices where the switching behaviour is controlled by Joule's heating, rather than direction of current flow. When the device is in LRS and potential is applied its terminals, current begins to flow. In TMC ReRAM devices this causes heating up of

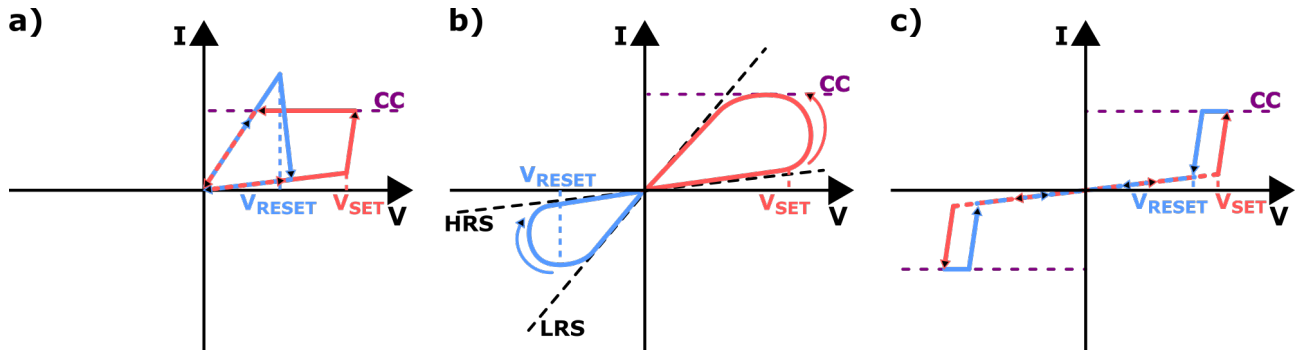


Figure 2.9: Various IV switching mechanisms. **a)** Unipolar switching mechanism, with both V_{SET} and V_{RESET} polarities the same. **b)** Bipolar F8 switching mechanism, with $V_{RESET} < 0 < V_{SET}$. cF8 switching would have $V_{SET} < 0 < V_{RESET}$. **c)** Monostable threshold switching mechanism.

the filament and at a certain current density, the filament ruptures resulting in abrupt increase in resistance (blue curve in Figure 2.9a). When the voltage is removed, the device cools and it remains in the HRS. Upon reintroduction of the voltage, the filament begins to build up again when V_{SET} is reached resulting in gradual decrease in resistance (red curve). The heating process must be limited by the compliance current (CC, purple dotted line) to avoid thermal dielectric breakdown as discussed earlier.

It is typical to observe higher SET than RESET voltage [103], with the exception of SiO_x dielectrics [104]. Additionally, the I-V characteristic is roughly symmetrical about the origin, as the effect is often thermal. It is observed in materials such as TiO_2 [68], [93], WO_x [69], but by far the most exemplary behaviour is noted in NiO [101], [105] devices.

For completeness it ought to be mentioned that recently NbO_2 based devices have been shown to exhibit threshold switching, as well as unipolar switching. Ascoli[106] has shown that in the low current regime, this device is a volatile threshold switch, and, as a result, its switching behaviour is better captured by the I-V locus in shown in Figure 2.9c rather than a. In fact one may have all these phenomena (threshold and unipolar) in the NbO_2 material. However the idea of using a NbO_2 nanostructure as data storage unit is no longer widely pursued by the researchers given that its endurance is poor.

Bipolar Switching

Bipolar switching is observed when SET and RESET operations occur at opposite voltage polarities. This behaviour can be studied in CBRAM or in VCM devices. As the device is formed it enters LRS. Cycling the voltage initially in the polarity of the SET voltage, will not induce any changes on the device, up to a point where either thermal or electric dielectric breakdown occurs, at which point the structure is irreversibly damaged.

However, as the voltage is cycled in the direction of V_{RESET} the CFs inside the structure begin to

retreat, slowly raising the device conductivity. At a certain point the device reaches maximum resistance, at which point further increase in voltage could lead to electrically induced dielectric breakdown of the material. Note that the pinched hysteresis shape doesn't necessarily have to be symmetric about the origin.

Such behaviour results in regions of negative differential resistance, which is observed in DC measurements (not AC as first proposed by Hickmott). During the SET operation the process can be stopped before reaching CC limit. Although the differential resistance will be negative, the AC resistance will be positive and the I-V curve of a high frequency AC measurement will intersect the hysteresis. This will be discussed in greater detail in the next section.

Bipolar switching can in fact co-exist with unipolar mechanisms as shown by Yoshida *et al.* [68]. The group doesn't however discuss methods to control or affect the selection of the dominant switching behaviour. Bipolar switching has been observed in materials such as TiO_2 [65], [68], TaO_x [67] or $Ba_{0.7}Sr_{0.3}TiO_3$ [70].

Finally, two types of bipolar switching have been reported called figure-of-eight (F8) and counter-figure-of-eight (cF8) [103]. The plot in Figure 2.9b shows the F8 mechanism, with V_{SET} positive and V_{RESET} negative. cF8 rather intuitively features the opposite - $V_{SET} < V_{RESET}$.

Threshold Switching

As opposed to the previous two RS mechanisms, threshold switching is monostable and therefore doesn't fall into NVRAM category. However, out of completeness it should be mentioned.

Arguably, more than two resistive states can be observed in threshold devices, when external bias is supplied. However, upon withdrawal of electric biasing, the device returns to HRS as demonstrated in Figure 2.9c.

Threshold switching, similarly to unipolar mechanism, features an I-V curve symmetric about the origin. Although, the device is not suitable for NVRAM it can find many other applications, such as electronic momentary buttons.

Comment

The discussion about the physical and electrical properties could continue, as there are many interesting phenomena, which overall contribute to the formation of analogue memory devices. However, detailed exploration of the quantum and chemical realms is beyond the scope of this work. A keen reader is invited to read publications by Lee *et al.* [103], Slesazeck *et al.* [82] or Ha *et al.* [74] to gain further insight into the material science of RS analogue memory devices.

2.6 The Memristor

2.6.1 Historical Note

Memristor is a passive, two terminal, non-linear circuit element. In 1971 Leon Chua at the University of California, postulated the existence of the fourth fundamental element alongside of resistor (R), inductor (L) and capacitor (C) [107]. Based on the argument of symmetry, whereby resistor links electric current (I) and electric potential (V), inductor links I and magnetic flux (Φ) and capacitor links V and electric charge (q), Chua hypothesised that an element connecting Φ and q should exist.

Due to its predicted behaviour of *memorising* its resistive state, it has been named a memristor - a portmanteau of memory resistor. A characteristic of the memristor is its non-volatility, making it a good candidate for analogue NVRAM.

In his seminal paper, Chua demonstrated the uniqueness of the memristor and proved that no combination of passive R , L , C components would yield the same behaviour [107]. He went on to propose an active realisation of the circuit (Figure 2.10), as he claimed that no passive realisation had been discovered. In retrospect, it is now generally accepted, that the memristive behaviour had been observed before. The first to realise that the VCM resistive switching phenomenon is the passive realisation of Chua's theory were Stanley Williams *et al.* at the HP Labs in 2008 [65]. This prompted Chua to generalise his theory to all RS devices, claiming that any effect resulting in a bipolar, pinched hysteresis shape in the I - V measurement can be seen as memristive [108].

This view is seen by some as radical, and a number of opponents of have come forward claiming that the presented memristive devices aren't in fact true realisations of the 1971 postulate [109]–[111]. While sources [109], [110] remain professional and scientific in their nature, Mouttet [111] conducts a personal attack claiming it was done as a PR stunt. Despite the few publications arguing against the memristor theory, it can be agreed that in fact no true realisation of a memristor has been observed, on the same basis as no real resistors, capacitors and inductors exist. On a technological level, all components are limited and deviate from the governing equations, e.g. resistors are power-limited and exhibit both capacitive and inductive behaviour. The case with memristor is that the technology is much younger and hence the deviations such as non-volatility or endurance are much bigger than the theory suggests.

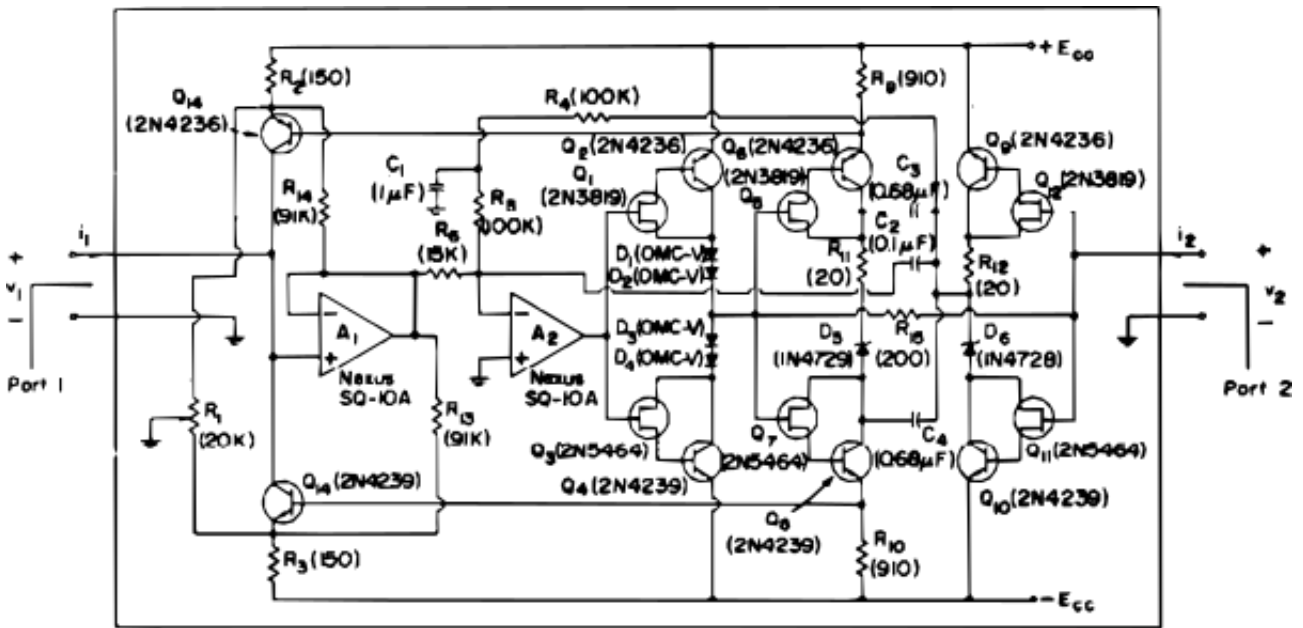


Figure 2.10: Active memristor emulator first proposed by Chua [107]. At the time the phenomenon present in thin-film structures was not yet discovered and associated with memory-like behaviour.

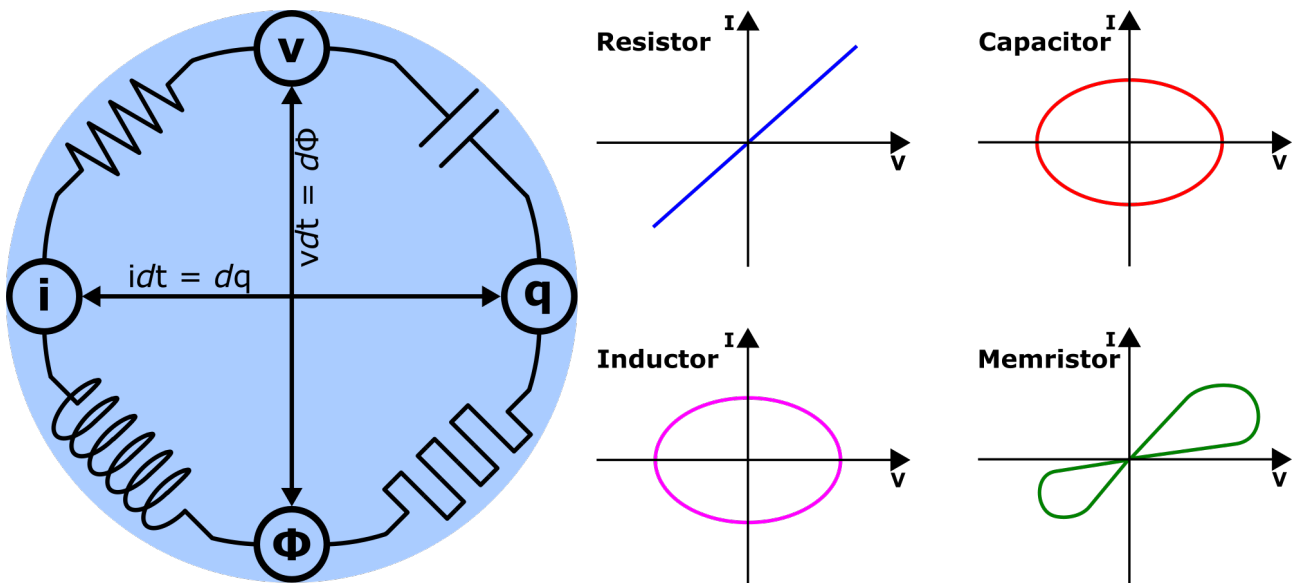


Figure 2.11: Linkage between four electrical parameters - current (i), voltage (v), magnetic flux or temporal integral of the potential across the device (Φ) and electric charge (q). 5 out of the six relationships were known in 1971. Based on this Chua postulated the missing element. Alongside are presented typical I-V responses for all component. Only resistor shows linearity as its defining equation lives in the I-V dimensions, as opposed to other components.

2.6.2 Model

Chua's Theory

To explain where the memristor lies in relation to other three fundamental elements, Figure 2.11 has been successfully adopted. Firstly, resistors link current and voltage as:

$$R = \frac{dV}{dI} \quad (2.8)$$

This is the more general form and is known as differential resistance. While in real, linear and passive resistors the following is true:

$$\frac{dV}{dI} = \frac{V}{I} \quad (2.9)$$

the measurement of resistance isn't reserved to just resistors as it was already demonstrated in this chapter.

Secondly, the capacitor forms a link between electric charge and voltage, such that capacitance is the measure of charge storing capability under applied electric field:

$$C = \frac{dq}{dV}. \quad (2.10)$$

The I-V characteristic forms an oval shape centred at but not crossing the origin. This is indicative of some device inertia, in this case charge movement. Thirdly, the inductor relates magnetic flux to the applied electric current:

$$L = \frac{d\Phi}{dI}. \quad (2.11)$$

The I-V curve also forms a loop around the origin, indicating energy storage. Hence finally, it isn't inconceivable to imagine that a link of the form of:

$$M = \frac{d\Phi}{dq} \quad (2.12)$$

should exist. The resulting quantity has the units of Ohms (Ω). Chua and Kang [112] presented a generalised model for memristive systems. As opposed to the first three fundamental components, memristive devices cannot be described by a single equation:

$$v(t) = R(x, i, t)i(t) \quad (2.13)$$

$$\frac{dx}{dt} = f(x, i, t) \quad (2.14)$$

, where x represents a state variable of the device. Chua called it this a *Memristor Lesson 2*: "memristor is defined as a state-dependent Ohm's Law" [108]. In other words the behaviour of the device is controlled by the function f . In standard resistors this is a zero function, resulting in $R(x, i, t) = R_{static}$, with fully independent value of static resistance. A non-zero function f results in the Lissajous-shape curve shown in Figure 2.11.

HP Model

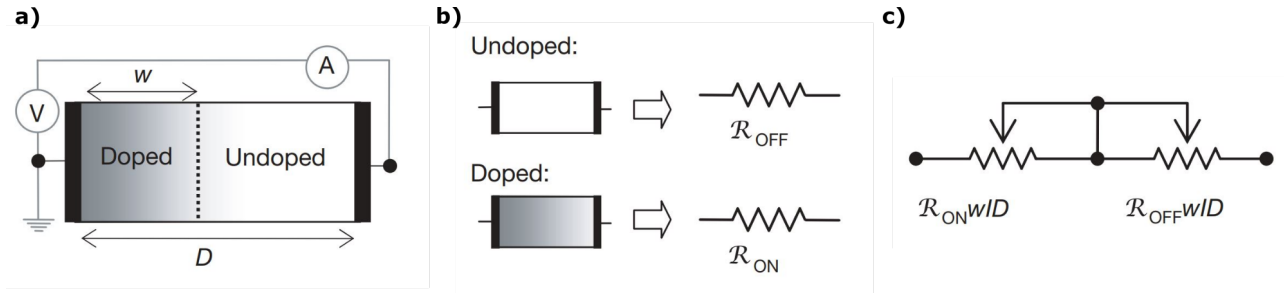


Figure 2.12: Phenomenological memristor model presented by Stanley Williams *et al.* [65]. Figures adapted from their paper. **a)** Varying material conductivity as a function of applied bias. The conductive region denoted as *Doped* has the length of w , while the *Undoped* region has the length of $D - w$. **b)** When $w = 0$, the whole device is in HRS and the resistance is denoted as R_{OFF} . Conversely, when $w = D$ the device is in LRS (R_{ON}). **c)** Simplified equivalent circuit of the switching phenomenon. Copyright 2008 Nature Publishing Group

In their seminal paper [65], the HP Labs team proposed a phenomenological model based on the material changes within the MIM structure. They conjectured that application of external bias would change the relative lengths of doped and undoped regions (Figure 2.12). Switching the device completely off would mean that the undoped region spans the whole length of the device. Conversely, switching the device fully on would imply the whole region is doped. It is therefore clear that the presented system can be rewritten in terms of Chua's original equations, with length of the doped region w as the state variable:

$$v(t) = \left(R_{ON} \frac{w(t)}{D} + R_{OFF} \left(1 - \frac{w(t)}{D} \right) \right) i(t) \quad (2.15)$$

$$\frac{dw}{dt} = \mu_V \frac{R_{ON}}{D} i(t) \quad (2.16)$$

where μ_V represents average ionic mobility under uniform electric field. Equation 2.15 is simply Ohm's law with resistance calculated as the weighted average of R_{ON} and R_{OFF} , where the weight is determined by state variable w . Equation 2.16 represents the change in the length w when charge $q(t)$ flows through it. This equation demonstrates the memory property very well. Once external bias is removed ($i(t) = 0$), the state variable becomes time-invariant with $dw/dt = 0$. Furthermore, by integrating equation 2.16 with respect to time, formula for state variable surfaces such that at $t = 0$ induced charge is $q(0) = 0$ as no current flow occurred and therefore the state variable should also be zero $w(0) = 0$:

$$w(t) = \mu_V \frac{R_{ON}}{D} q(t) \quad (2.17)$$

This in turn allows to find the memristance:

$$M = \frac{\mu_V R_{ON} (R_{ON} - R_{OFF})}{D^2} q(t) + R_{OFF} \quad (2.18)$$

This can be approximated and simplified provided that $R_{OFF} \gg R_{ON}$:

$$M = R_{OFF} \left(1 - \frac{\mu_V R_{ON}}{D^2} q(t) \right) \quad (2.19)$$

Window Function

The HP model however lacks an important parameter, namely a function which controls that the state variable stays between 0 and D . From the phenomenological point of view, this makes sense, as the doped region cannot be negative in length and it cannot exceed the length of the device. Under the current HP model a uniform DC current results in constant and linear change of the state variable w . A purpose of the window function is to ensure that at $w = 0$ and at $w = D$: $dw/dt = 0$.

Therefore, some groups proposed different window functions $p(w)$ such that:

$$\frac{dw}{dt} = \mu_V \frac{R_{ON}}{D} i(t) p(w) \quad (2.20)$$

$$0 < w(t) < D \quad (2.21)$$

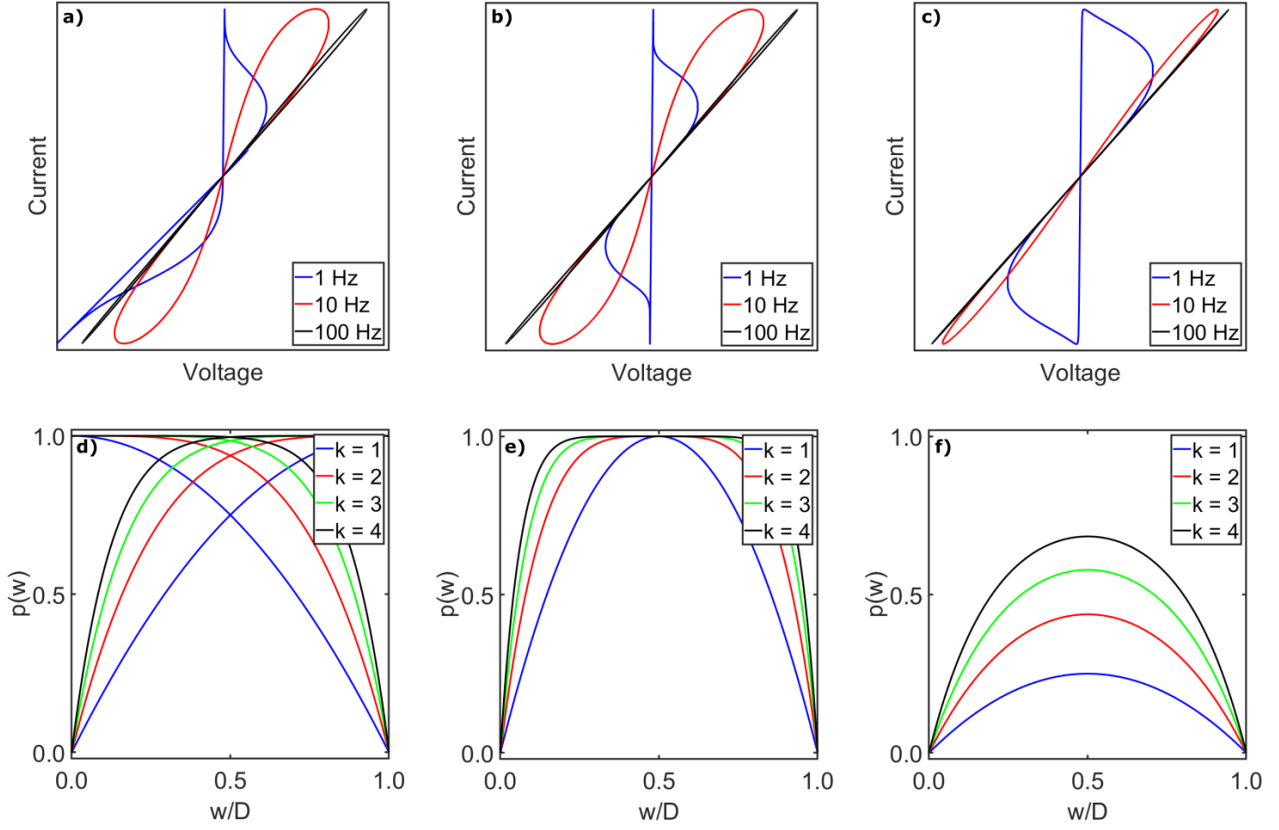


Figure 2.13: Effect of window function choice on the model performance of a Memristor. The same model of a device was used and the same excitation waveform was applied. Different results are solely attributed to change in frequency of the driving bipolar current and varying window functions. I-V of a memristor with: **a)** Biolek Window Function with $k = 2$. **b)** Joglekar Window Function with $k = 2$. **c)** Prodromakis Window Function with $k = 2$. **d)** Family of Biolek window functions. Note the discontinuity at $w = 0$ and $w = D$. **e)** Family of Joglekar window functions. **f)** Family of Prodromakis window functions.

Among the many functions most often cited ones are Joglekar [113], Biolek [114] or Prodromakis [115]. Joglekar was among the first to observe that the state variable, effectively representing the dopant drift, is in fact non linear. He proposed an observation-based window function which reduces to zero at $w = 0$ and $w = D$ and peaks in the middle at $w = D/2$. Joglekar's function is independent of the direction of the current, i.e. symmetrical about the $w = D/2$ line:

$$p(w) = 1 - \left(2\frac{w}{D} - 1\right)^{2k} \quad (2.22)$$

Biolek's window is a family of discontinuous functions, which depend on the direction of the applied current (i). The group noted that the practical memristor, particularly near the end points of w , is easier to program away from the endpoint than towards it. As such, the group proposed direction dependent function:

$$p(w) = 1 - \left(\frac{w}{D} - \text{stp}(-i)\right)^{2k} \quad (2.23)$$

$$\text{stp}(i) = \begin{cases} 1, & \text{if } i \geq 0 \\ 0, & \text{if } i < 0 \end{cases} \quad (2.24)$$

Finally, the Prodromakis window function is a physics-informed model of Joglekar function, where the physical nature of the non-linear dopant effects is derived:

$$p(w) = 1 - \left(\left(\frac{w}{D} - 0.5\right)^2 + 0.75\right)^k \quad (2.25)$$

Parameter k present in all equations is a device dependent positive integer. The window functions and the resulting Lissajous-type I-V characteristics of these models are shown in Figure 2.13. Notice the frequency dependence of the curves. In principle, the theoretical memristor approaches a linear resistor as the frequency of the I-V measurement is increased. In practice, this is not always true, e.g. at high frequencies the memristor begins to behave as voltage or current controlled nonlinear resistor. The static resistance it approaches is directly determined by the value of state variable, such that non-destructive readout is possible. An empirical Verilog-A model has also been proposed to allow circuit simulations [116]. A further discussion on the implications of the window function choice can be found in [117], [118].

Higher Order Models

One of the most widely used models nowadays is TEAM or threshold adaptive memristor model [119]. This model combines the simplicity of the previously proposed solutions and higher degree of phenomenon reproduction - the threshold behaviour of the device is accounted for. Kvatinsky proposed a piece-wise continuous definition of the state variable differential equation. The state variable describes the effective electric tunnel width:

$$\frac{dx(t)}{dt} = \begin{cases} k_{off} \times \left(\frac{i(t)}{i_{off}-1}\right)^{\alpha_{off}} \times f_{off}(x), & \text{if } 0 < i_{off} < i \\ 0, & \text{if } i_{on} < i < i_{off} \\ k_{on} \times \left(\frac{i(t)}{i_{on}-1}\right)^{\alpha_{on}} \times f_{on}(x), & \text{if } i < i_{on} < 0 \end{cases} \quad (2.26)$$

k_{off} , k_{on} , α_{off} and α_{on} are device dependent constants. i_{off} and i_{on} are the current switching thresholds. Finally functions f_{on} and f_{off} behave like window functions. The window function

much like Biolek's model is polarity dependent.

Serb proposes a data verified phenomenological model [120], incorporating voltage-dependent exponential switching behaviour, often observed in the I-V characterisation of the device. The state variable is the resistance itself. Quite notably the switching is not symmetrical as the fitting coefficients a_p , a_n , b_p and b_n vary.

$$i(R, v) = \begin{cases} a_p R^{-1} \sinh(b_p v), & \text{if } v \geq 0 \\ a_n R^{-1} \sinh(b_n v), & \text{if } v < 0 \end{cases} \quad (2.27)$$

$$\frac{dR}{dt} = g(R, v) = s(v) \times f(R, v) \quad (2.28)$$

This model introduces a new concept, namely a switching sensitivity function $s(v)$, also exponential, incorporating the $e^{|v|}$ term. Finally, the $f(v, R)$ is the voltage and resistance dependent window function. Overall, equation 2.28 while similar to equation 2.20, proposes a more complex and more accurate description of the polarity and magnitude dependence. The HP model was comparably quite static, assuming uniform mobility and was agnostic towards signal properties.

2.6.3 Memory Circuit Elements

In 2009 Di Ventra *et al.* proposed an extension of memristive systems to include memory inductors (meminductor) and memory capacitors (memcapacitor) [121]. The pinched hysteresis behaviour is theoretically predicted to occur in the I- Φ measurement for meminductor and Q-V measurement for memcapacitor. Di Ventra [121] and Chua [112] argued that that equations 2.13 and 2.14 could be generalised to any system, not only resistive. Di Ventra proposes that by replacing $v(t)$ with $q(t)$ and $i(t)$ with $v(t)$ the equations would describe a memcapacitive behaviour. Similarly $\Phi(t)$ and $i(t)$ describe meminductive properties. A detailed mathematical analysis can be found in [121], [122].

Chua's Table

The original argument for existence of a memristor was the missing link between charge and magnetic flux. However, this argument may seem incomplete, as it doesn't account for higher order terms of voltage and charge as shown in Figure 2.14a. The argument can be extended, and looking at that form of the diagram, one can also observe a repeating pattern. More importantly, in this pattern all the memory components including the memristor belong to the

second iteration, implying that memristor may not one of the *fundamental* elements³. Putting this argument aside, the connection between magnetic flux Φ (or lower capital ϕ depending on notation) and temporal integral of charge (σ) gives rise to memory capacitance. In general, this diagram shows that circuit elements only arise as a connection between α derivative of voltage and β derivative of current. This notation defines negative values of α and β as integrals.

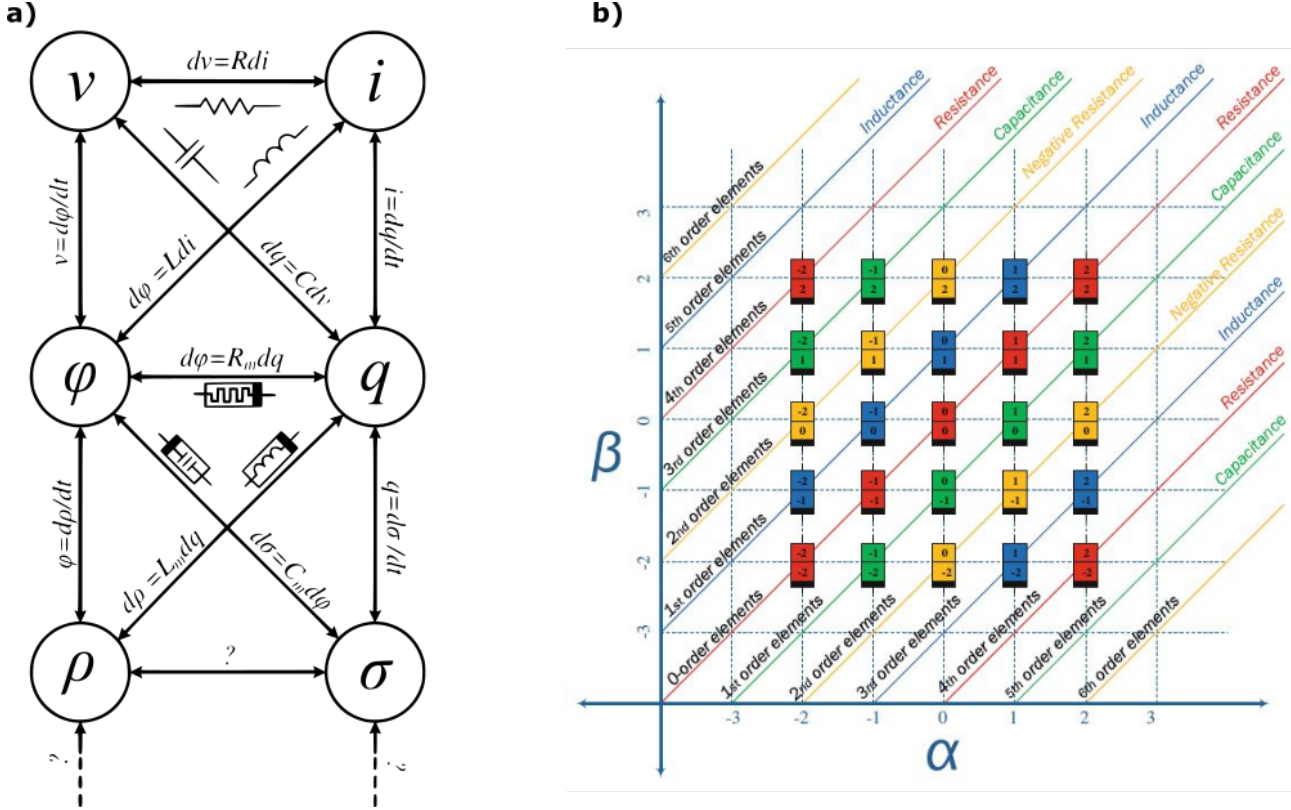


Figure 2.14: Generalisation of all fundamental passive components. Figures adapted from [123]. **a)** Extended symmetry table, showing potentially infinite number of electrical components based on higher order integrals of voltage and current. **b)** Chua's Table, showing classification of electrical components based on the order of the temporal derivatives of voltage and current, which define the elements. Copyright Springer International Publishing Switzerland 2015

$$v^\alpha = \frac{d^\alpha v}{dt^\alpha} \quad (2.29)$$

$$i^\beta = \frac{d^\beta i}{dt^\beta} \quad (2.30)$$

Using the above notation, elements can now be identified based on their respective position in the Cartesian plane - an element defined by $v^\alpha - i^\beta$ has the coordinates of (α, β) . For example,

³Many however such as Alon Ascoli hold this as unquestionable scientific fact. The ideal memristor, proposed by Chua in 1971, i.e. the one-port unequivocally defined by a nonlinear charge-flux constitutive relation of the form $f(q, \phi) = 0$, is the fourth fundamental two-terminal circuit-theoretic element. According to him there is no doubt and no question about this point. No combination of the other fundamental one-ports (inductor, capacitor, and resistor) may reproduce the behaviour of an ideal memristor, hence the latter is fundamental.

a resistor is a $(0,0)$ element, while $(-1,0)$ defines the location of an inductor.

Apart from the generalisation of passive elements, this table provides two practical functions:

1. It gives mathematical insight into theoretical higher order, non-linear, elements, e.g. the component behaviour repeats every 4 orders.
2. It allows to analyse highly non-linear memory-circuits in terms of linear memory-less components by using Biolek's transform [124], [125].

Biolek *et al.* [126] concluded using the two above implications, that every non-linear component (α, β) has a pinched hysteresis loop in $\alpha + 1$ and $\beta + 1$ plane. E.g. memristor $(-1,-1)$ exhibits a Lissajous-like behaviour in a $0 - 0$ plane, i.e. voltage and current space. Following that argument, he has shown that a resistor $(0,0)$ in parallel with a diode shows similar behaviour in $1 - 1$ space, i.e. $dv/dt - di/dt$ plane [124]. He concluded that the pinched hysteresis is not a sign of memory capability but merely a consequence of constituent non-linear relationship. Memory-devices can be then thought of as a subset of all non-linear elements. In fact Biolek goes on to explain this behaviour in more detail in his subsequent publications [127], [128].

It must be pointed out that while mathematically possible, physically there is no real proof that such higher order passive components may in fact exist. Nonetheless, Chua's table is an interesting tool which allows building and analysis of active systems conforming to Biolek's proposition.

However, most importantly, Chua's Table opens up the possibility for existence of a whole class of memcapacitive systems. It is therefore worth spending some time to look at them as well, as they may directly affect the field of reconfigurability, as it will be shown.

Memcapacitor

Since Di Ventra's paper in 2009 first theoretical and later practical realisations of memcapacitors have been proposed with various degree of optimism stemming from the overall results.

Firstly, it is still very rare that an isolated capacitance switching effect is observed. It is very often accompanied by a simultaneous memristive effect [129]–[134]. This is often attributed to one of two factors, when the underlying phenomenon is the resistance switching. It can be either capacitance modulation due to growth of conductive filaments, effectively changing the capacitance as a function of distance separating the two metal contacts, e.g. Qingjiang *et al.* [129]. It can also be attributed to change of effective dielectric of the medium, e.g. Romaacuten Acevedo *et al.* [130]. Quite interestingly Romaacuten Acevedo theorises that the effective dielectric constant change can stem from Maxwell-Wagner polarization - interface charge trapping

mechanism heavily used to slow down electromagnetic waves beyond the capabilities dictated by the dielectric constant of the material used [135]. Irrespective of the physics behind the joint memristive and memcapacitive behaviour, resistive switching often dominates at very low to relatively high (even hundreds of kHz) frequencies, since the capacitances involved are very small indeed. Figures 2.15c and d illustrate a typical DC and AC model of one of such devices.

Secondly, low switching ratios are often realised and as a result mostly binary, ternary and quaternary devices are reported. Yang *et al.* [136] reported a metal-oxide-semiconductor (MOS) stack exhibiting some degree of capacitive switching. The capacitance change represented less than 15% of the nominal value. Moreover, the process was not reversible. The group deemed this device suitable for write-once-read-many-times type of memory. However, the problems halting the desired behaviour were identified and new results were published two years later [137]. The researchers hypothesised and then proved that choice of metal plays a pivotal role in reversibility of the process. By replacing aluminium electrode with an oxygen-reactive indium-tin-oxide (ITO), Yoon *et al.* not only managed to sweep the capacitance up and down with different polarity signals, but vastly enhanced the switching ratio with 'on' capacitance of nearly 15pF and 'off' of around 2pF.

Thirdly, many of the reported devices require extreme voltage levels in order to be programmed with values reaching as high as $\pm 30\text{V}$ [138]. This is impractical for low power, small technology node application specific integrated circuit design (ASIC), since the voltage levels involved are an order of magnitude above the dielectric breakdown limit of some of the components. Wang *et al.* successfully demonstrated reversible nonvolatile memcapacitive switching, but have produced only around 10% of capacitance change, reducing the device to binary applications. This can be attributed to the nature of the switching mechanism - where a single thin film layer of the 4-layer stack is switched on and off. The large voltages required stem from the fact that the switchable layer has to accumulate carriers or be depleted of them. The injection barrier of the materials used directly dictates the magnitude of programming signals.

There are nonetheless very promising results. Qian *et al.* [139] presented a quaternary device, based on a perovskite material. The authors draw a phenomenological analogy to a PIN diode (discussed in section 2.3.2). It is shown that the migration of bromide ions modulates the intrinsic (middle) layer of the PIN structure. In the OFF state neutral bromide could be found in abundance uniformly distributed throughout the active layer. In the ON state, bromide ions accumulated on the gold anode. Capacitive switching ratio of over 200 is reported, as the group claims no conduction in the OFF state - 0pF, though its likely the results were limited by the instrumentation. Most impressively from the stand point of circuit application results shown in Figure 2.15a) are presented, showing 2 bit programmability of the device. The group provides a mathematical model for the memcapacitive behaviour completing one of more promising works to date.

The work by Qian *et al.* spurred other groups to present other quaternary devices. Shi *et al.*

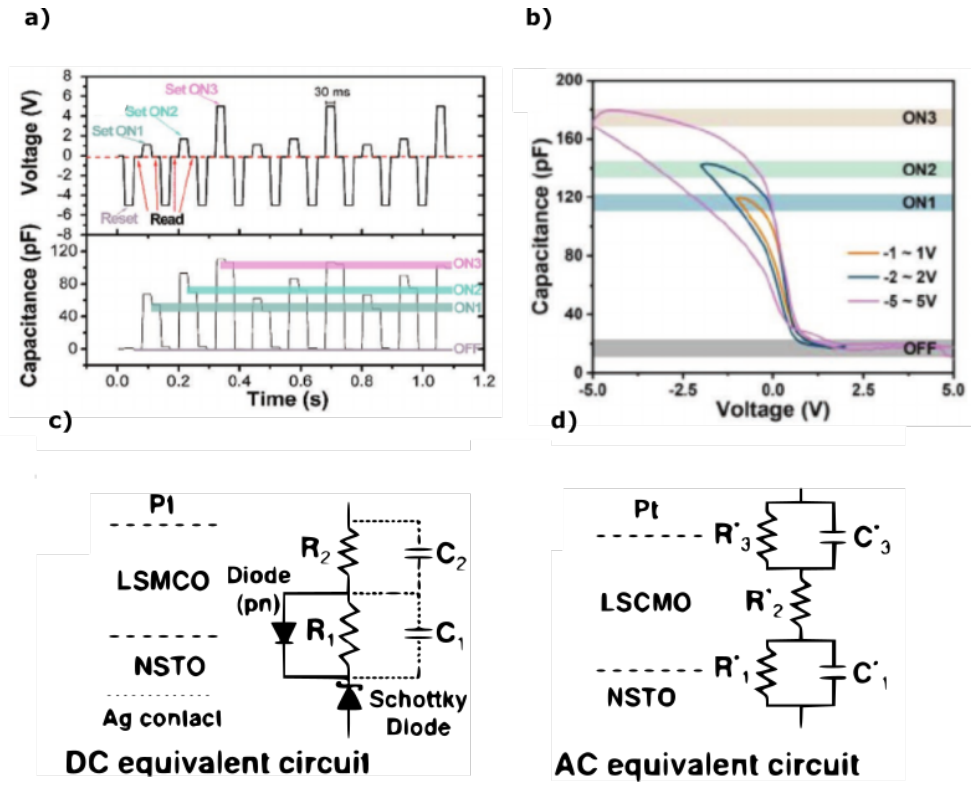


Figure 2.15: Nonvolatile memcapacitive devices. **a)** Figure adapted from [139]. Quaternary memcapacitive device exhibiting repeatable and reversible reconfiguration. A single OFF state and three ON states are described by the authors. **b)** Figure adapted from [140]. Results from subfigure a) motivated the research and other quaternary devices were soon after reported. Graphene based devices exhibited higher ON capacitances. **c)** Figure adapted from [130] DC model of a typical joint memristive and memcapacitive device. **d)** Figure adapted from [130]. Complementary AC model. Copyright 2019 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim and Copyright AIP Publishing 2020

[140] presented an organic device based on a graphene oxide and a protein (silk fibroin). Their device as opposed to other reported results is a fully flexible memcapacitor, ideal for biomedical and wearable electronics. However the group found that the magnitude of memcapacitance was frequency dependent, and the capacitance - voltage curve would collapse at frequencies above 40kHz. At 10kHz they obtained 4 capacitive states shown in Figure 2.15b), with great retention properties (reported over 30mins). The memcapacitive effect is attributed to interfacial charge build-up upon applying electric field.

The work on memcapacitors is often motivated by the development of low-power analogue neuromorphic circuits. Similar to memristors they offer reconfigurability, information storage as well as signal processing. However, memcapacitors are deemed to excel in terms of power consumption in the same way that resistors are dissipative and reactive components are not. Of course, the act of reconfiguration dissipates power, or in other words reduction of entropy requires energy input.

2.6.4 Derivatives

Memistor

A memistor (note the lack of r) is an extension of the definition of the memristor to three terminals. As with transistor, where the instantaneous gate voltage determines the current flow through the channel, memistor employs a time integrated signal as a control mechanism. The theoretical definition of a memistor precedes that of a memristor, as it was first proposed in 1960 by Widrow [141]. The original device was of course rather large and CMOS incompatible, as it used a bath and electroplating mechanisms to function. Since the invention coincided with the discovery of the integrated circuit process, the electroplating method was abandoned in favour of solid-state options.

Presently, memistors are rarely used as they are essentially too difficult to characterise. While memristors are very non-linear, it is now considered straightforward to predict its behaviour in a larger circuit. Despite over 60 years of memistor existence, the devices continue to escape full academic understanding. A keen reader is invited to read the *Handbook of Memristor Networks* to gain further appreciation of the difficulties of the design and applications of memistors [142].

Memtransistor

Many justify the existence of memory transistor by drawing a comparison to a neuron-synapse configuration. Two terminal memristors do not reflect the complexity of the basic biological structure, and as such researchers try to come up a multi-terminal model of a memristor. This definition is nearly identical to that of a memistor, with the exception that the count of terminals in the memtransistor is unrestricted. That is to say: memistor is a special case of memtransistor.

Some groups managed to develop such structures [143]. Notably the geometry of the device is planar, as opposed to current memristor stacks of metal-active material-metal. This allows for easier extension to higher number of terminals, and allows easier CMOS integration of more closely resembling neural architectures.

Furthermore, memtransistors may in fact address the issues which are currently encountered with memristors on crossbar arrays - problem of sneak paths and device selection. Due to the high number of parallel devices, selecting a single device on a purely memristive crossbar array is impossible. Some current will always flow through other paths leading to significant error in measurements. This motivates the need to use 1T1R (1 transistor in series with 1 resistor) cells as building blocks for those arrays, where the additional transistors acts as a select switch for the particular memristor. However this method greatly compromises the areal savings, which would otherwise be achieved with purely memristive architecture. Very recently a group

at the Institute of Materials Research and Engineering of A*STAR in Singapore, proposed an architecture of a crossbar based on memtransistor devices, which are 'self-selectable' [144]. The measured sneak paths are of the order of 10^{-10} A. However ultra low voltage switching is also realised, with potentials as low as 420mV, which in high noise environments may lead to undesirable behaviour.

Notwithstanding, memtransistors may prove very exciting in the years to come, as they seem to offer functionality of memristors, with resilience of transistors at a marginal areal increase over memristors.

2.6.5 Demonstrated Applications

The application space of memory devices is vast. This section presents just a sample of many of the interesting and promising use cases of memristors. A visual representation of memristive applications is shown in Figure 2.16 [145].

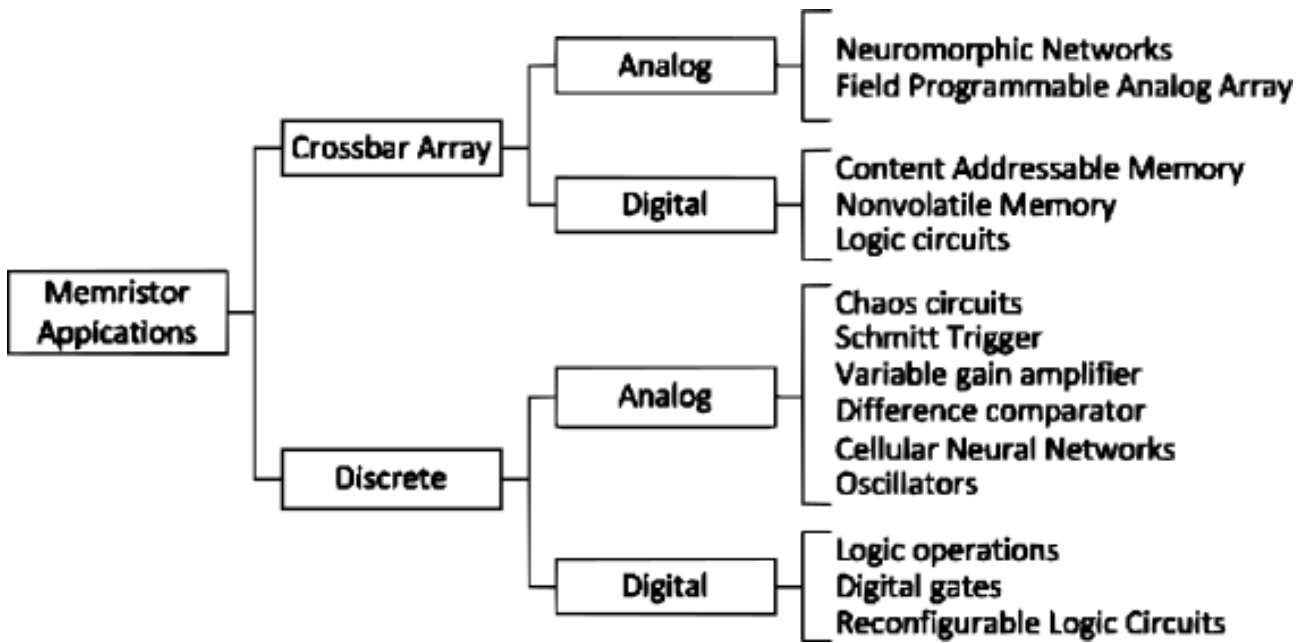


Figure 2.16: Taxonomy of memristive devices' applications. Representation of the application is divided into the two forms in which memristors are often used - as standalone device and on crossbar arrays. Diagram adapted from [145]. Copyright IEEE 2021

Programmable Gain Amplifiers

The low hanging fruits of memristor domain are simple analogue reconfigurable circuits which currently are limited in their performance due to discretisation of their range or large areal consumption. Programmable gain amplifiers (PGA) are easily realised with classic inverting and non-inverting amplifier topologies. One of the resistors determining the gain is replaced

with a memristor whose value can be controlled. In an inverting amplifier, it is preferable to replace the input resistor, that is the resistor not in feedback, as large voltage potentials across the device will quickly lead to an unwanted reconfiguration of the device, whereas the input resistor features one virtually grounded node. This allows to keep the potential difference across the device small, as it is primarily determined by the input signal.

Automatic Gain Control

When using PGAs for variable gain control, the location of the memristor is changed - it is placed in feedback with the amplifier. This is because the memristor must be able to sense and react to the output voltage. This therefore makes the design task more challenging, since the memristor must be protected from being damaged. Nonetheless theoretical and practical results have been successfully presented in literature [146], [147]

Sequence Detectors

Many of the memory devices exhibit some form of relaxations, which is often compared to short-term plasticity (STP) of biological synapses. STP demonstrates itself through modulation of the synaptic weight, or strength of connection, which is induced by the recent history of signals.

Berdan [147] demonstrates the use of volatile memristors as sequence discriminators. In his study, he proposed a circuit which determines the sequence order either AB or BA. Preliminary results suggested that the memristor based approach built with discrete components was able to successfully determine the correct order 67.5% of the time. He goes on to elaborate on use of redundancy to enable unreliable systems to behave predictably.

Image Edge Detection

Image processing is known to be computationally expensive, particularly on CPUs. Many image processing functions are often moved to a graphical processing unit (GPU), which is designed to handle matrix based computations more efficiently. Despite that, functions such as edge detection still requires relatively large number of resources. A more intuitive way based on the human retina has been proposed. A rectangular grid, where each set of nodes is connected with a memristor, has been developed [148]. The image is mapped to the new grid, and a voltage corresponding to a given pixel is applied at each node, giving rise to current flow and resistive switching. The two nodes corresponding to an edge in the image, will produce a larger current flow, thus resulting in a higher resistive change. The resistances are then read-out and a high pass filtered image is produced [149].

Fuzzy Logic

Fuzzy logic is based on continuous decision making, as opposed to binary true/false decision at a fixed boundary threshold. This area was previously developed as infinite-valued logic primarily by Lukasiewicz [150]. This concept measures the degree to which a given element belongs to one set or another. It is one of the building blocks towards realising fully autonomous artificial intelligence which capabilities of generalising knowledge. As such it attracts research, however the systems have to be developed from the fundamental principles as demonstrated by Papandroulidakis *et al.* [151], [152].

In-Memory Computing

Since 1945 computers have been designed using the von Neumann architecture, where memory and processing units are separated [153]. As technology progresses, the CPU speeds far surpass those of DRAM. This is a performance bottleneck, because computing speed-up no longer guarantees overall performance improvement. A simple addition operation of two numbers requires three read-from-memory operations, one write-to-memory operation and one arithmetic operation. Therefore execution speed is limited by the memory access times which are usually quite slow.

Work done by Kvatsinsky and his team, shows that integration of memory and CPU is in fact possible and they have demonstrated some results [154]. Computation is performed directly in the memory. For example the group proposed a MAGIC NOR gate [155], based on three memristive devices. The devices are used as binary switches, and the logic is determined by the final state (ON/OFF) of the output memristor.

2.6.6 2D Materials

Following the discovery of graphene, various structures consisting of just a single layer of atoms attracted a lot of attention. The success of 2D structures such as graphene is attributed to their thickness as well as excellent electrical, thermal and optical properties. More importantly graphene has been widely used as an active layer in memristor structures [156]–[158]. Some groups have used planar graphene or graphene oxide (GO) as electrodes. Graphene, due to its 2D structure, is extremely flexible [159]. Furthermore low cost production and its versatility render the device increasingly more researched. Most recent results show the use of G/GO devices as neural synapses, demonstrating 4 bits of data storage [156]. Furthermore due its high conductivity, G/GO based devices (electrodes) improve electrical characteristics by minimising the effective series resistance of the memristors, thus increasing the tunability range to lower values.

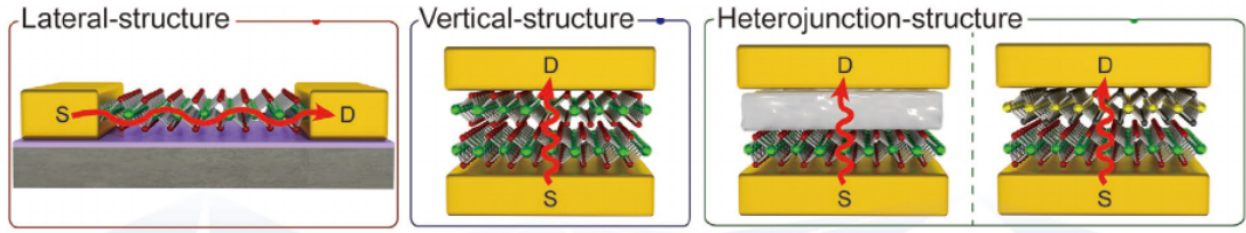


Figure 2.17: Structural taxonomy of memristive devices based on 2D materials [160]. Copyright 2020 Wiley-VCH GmbH

In terms of structure memristors based on 2D structures can be categorised into 3 groups: lateral, vertical and heterojunction [160] (Figure 2.17). Laterally oriented devices can be best compared to CMOS transistors, with electrodes on either side of the active material. Commonly, to realise truly planar 2D lateral devices, tantalum sulfide (TaS_2) or molybdenum sulfide (MoS_2) are used. The usual mechanisms contributing towards resistive tuning of the device are often reported to be local phases transitions [161] or defect migration [162]. Defect migration is however reported to require relatively large voltages to induce changes, in excess of 80V. Phase transition on the other hand requires a more manageable 3V to set the device.

Since the devices are deposited on a dielectric substrate, often silicon and silicon oxide, the devices can be viewed as memtransistors, with third terminal (i.e. the gate) controlling various active layer properties [143]. The 2D structure of the proposed memtransistor benefits from ease of multi-terminal implementation, thus allowing to simulate neural-synaptic properties more accurately.

Vertical structure devices consist of layered 2D crystalline materials. It is thought that stacked 2D materials can help control the electrical properties of the device more. In standard 3D materials, local imperfections and defects can only be statistically controlled, that is the precise location and number of imperfections cannot be controlled. Technology behind 2D materials enables thickness uniformity and an atomic precision of the structure [160].

The structure of vertical devices closely follows that of conventional oxide based devices - metal, active layer, metal stack. Typical switching phenomena of 2D layered materials overlap those of classic memristors - phase transition [163], filament growth [164] and vacancy migration [165]. The 2D structures often used to realise vertical devices include MoS_2 , MoTe_2 , WS_2 to name a few. Commonly reported optimal voltages are in the range from 0.5V to 3V, which is what is observed for standard oxide memristors.

Finally, heterojunction-structure devices present possibly most desirable characteristics. By mixing various different layers, new and potentially better electrical characteristics can be engineered. It is not uncommon nowadays to stack together the usual 3D bulk materials with 2D layers of different material to realise new properties. Such attempts have led researchers to realise ultra low power FET devices [166].

For example devices based on zirconium oxide and tungsten sulfide have been shown to switch with voltages as low as 160mV and reset voltages as low as 60mV [167]. At the same time they are very robust and can withstand 10^9 switching cycles. The group behind those results have demonstrated additionally over 11 hours of data retention. In principle the same switching mechanisms are observed in heterojunction based structures as in conventional oxide memristors.

2.7 Reconfigurable Systems

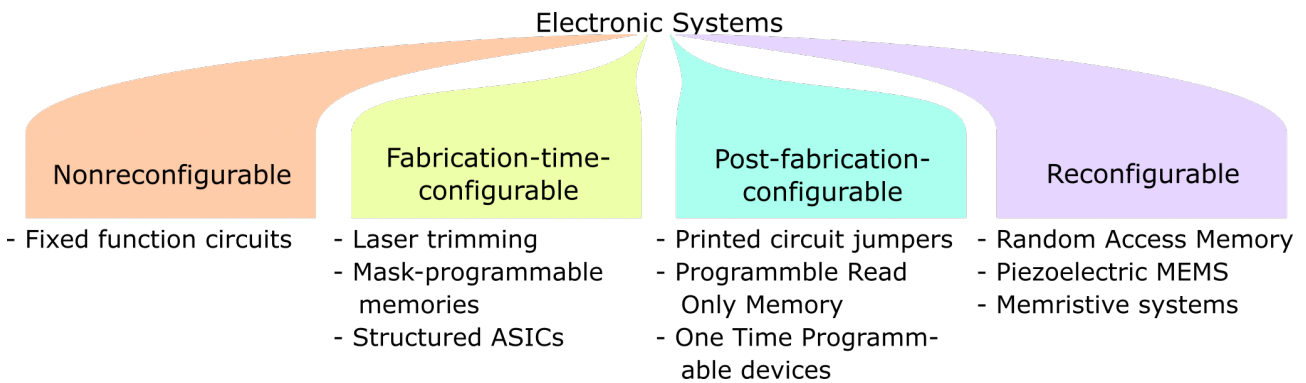


Figure 2.18: Taxonomy of electronic systems based on their ability to change their functionality. Information for this graphic was sourced from Lyke *et al.* [168].

The individual elements discussed so far enable systematic reconfigurability, however on their own they are rather limited. A reconfigurable platform will often be made up of thousands or perhaps even millions of such elements aiding the multi-functionality. It is important that the duality of reconfigurability is briefly addressed here: designing *for* and designing *with* reconfigurability. This chapter until now has dealt with the design for reconfigurability: various control and tuning methods were discussed. These methods, when implemented on a fabric of many such elements, could then be employed to design systems with reconfigurability. Though the semantic difference seems trivial, their meanings refer to two separate processes.

One further linguistic differentiation should be made, as pointed out by Lyke *et al.* [168]; adaptivness is often confused with reconfigurability. The author describes that adaptivness is a characteristic of some reconfigurable systems - those that have the ability to evolve on their own as a response to the input stimuli. The authors argue that adaptivness directly relates to systems autonomy in controlling its own degrees of freedom. As such they propose an "adaptivness hierarchy": fixed, reconfigurable and evolvable systems exhibit increasing levels of adaptivness respectively.

Hasler [169] further notes that programmability should not be confused with configurability. The act of changing parameters in an algorithm should be seen as an example of programming, whereas changing dataflow, topology or the order of operations is an act of configuring.

Reconfigurable systems can be generally thought of as those that can be altered at will, often through software. This has led to a number of *software defined* solutions such as radios, networks or computing. It also allowed to develop general purpose platforms allowing rapid prototyping such as now ubiquitous field programmable gate arrays (FPGAs). In this section a brief overview of current state-of-the-art of reconfigurable systems is presented.

2.7.1 Digital Platforms

Historical Note

Field programmable gate arrays are now considered the flagship of digital electronics. At their core they are extremely simple platforms - banks of logic elements, look-up tables (LUTs), memory and I/O all neatly positioned on a fabric of transistors, which determine the signal flow from one element to another. The concept of FPGA can be traced back to early 1980s. However, digital reconfigurability was explored earlier with many other programmable logic devices (PLD) and programmable read only memory (PROM).

Programmable logic devices are a superset of all digital configurable systems. The early forays into digital logic synthesis took place in 1969 with mask-programmable gate arrays, first developed by Motorola: XC157 Multi-Gate Array. These platforms were designed for final product delivery: transistor arrays were connected together through metallisation in the final stages of fabrication [170]. These were so-called fabrication-time configurable devices (Figure 2.18) - they allowed for customisation only once, before deployment. As the original wafer with the transistor array is a generic one, the chips rarely reach high resource efficiency. Source [170] reports that small arrays (100'000 gates back in 1995) were utilised up to 90%, however large designs would only use around 60% of bigger arrays' real estate.

In short, first configurable platforms were not reconfigurable. This status quo has changed in 1971 [171], when General Electric utilized Intel's programmable read only memory. The very first reconfigurable digital platform was based on floating-gate transistors (discussed in section 2.3.3), and reconfigurability was enabled through equalisation of charge through UV light.

Classification

Nowadays, PLDs can be divided into three sets, based on their comparative complexity: simple programmable logic devices (SPLDs), complex programmable logic devices (CPLDs) and FPGAs. Within each set there are different variants, however they all effectively do the same tasks - synthesise logic on hardware. The main difference between the three categories is the complexity of the synthesised problem. SPLDs are often made up of low-level elements, such as flip-flops or gates often collectively called macrocells. As a result they are used to perform

simple combinatorial logic. CPLDs can be viewed as an array of many SPLD-like elements. These devices as opposed to SPLD often have their own on-chip memory and can be viewed as standalone units.

FPGAs take one step further, by combining many functional blocks and moving away from individual logic gates by replacing them with LUTs, they are able to perform a whole spectrum of tasks: computing, signal processing, communication and simulation. The very first FPGA [172], Xilinx's XC2064 released in 1985, was a grid of 64 configurable logic blocks (CLBs). This was a massive breakthrough - until 1985 if any company wanted to realise logic, they had two options: use the limited SPLDs/CPLDs or own a fabrication plant, where they could develop their own ICs. The former often resulted in poor performance, while the latter was expensive and development was time-consuming. Introduction of FPGAs not only revolutionised the digital development of logic, computing etc., but also motivated a gradual change of business models of many big companies such as AMD. AMD until very recently had their own foundry. In recent years, the company began outsourcing their designs to dedicated semiconductor foundries, de facto closing their fabrication centres⁴ Alfke *et al.* [172] call XC2064 the first *fabless* chip.

Design *for* and *with* Reconfiguration

Referring to the earlier dichotomy: design for reconfiguration is achieved by placing programmable LUTs, that can perform any logic within the architectural limits, and designing an interconnect fabric which can change its routing when required. Reconfiguration is done from program's memory - early FPGAs had one reconfiguration memory which was accessible to the user. Nowadays, thanks to emergence of glitchless transitions, dynamic (in-operation) partial reconfiguration (DPR) is also possible, however it requires more complex memory architectures.

Design with reconfiguration deals with associating user's program to the available hardware through a so-called instruction set architecture (ISA); this is also called *embedding problem*. In the case of FPGA the hardware resource pool is the set of all individual elements - switches, settable parameters, intellectual property (IP) blocks and many others [168]. The *embedding problem* is often too difficult to tackle by hand (NP-type problems [173]), and specific tools are required to transform a design into a functional circuit. Similarly to computer language compilers, FPGA have their own high-level synthesis tools [174] for that purpose.

The above covers *how* to design with reconfigurability. However the reason why this domain attracts such a huge and uninterrupted interest lies in the answer to the following: *what* can one design with reconfigurability? Static architectures tend to compromise performance for

⁴AMD laid the foundations for GlobalFoundries, which effectively is the spin-off company of AMD and their owners.

generality. As Lyke [168] discusses, any problem to be power- and performance-optimal requires its own dedicated architecture. However, even a platform whose fabric can be altered prior to computation is sub-optimal when deployed to solve dynamic problems. Dynamic problems are characterised by time-varying parameters. In order to be solved optimally, they require a dynamically changing platform. Lyke argues, that in an ideal world, every computer should be sculpted one transistor at a time. This is in fact, as we know, impractical due to simply immense work required to do so.

Though it may sound abstract and impossible, this idea gives rise to reconfigurable computing - a platform whose very hardware architecture can change and adapt to the given task. Moreover, FPGAs further leverage other concepts, that allow them to stand out: in-memory computing is more easily achieved as data does not have to be regularly stored and fetched from dedicated memory units. Owing to those capabilities Xilinx, the leader in FPGA technology, had showed already in 1991 that FPGAs can outperform supercomputers (what was then considered a supercomputer - Cray 2) [175]. DNA sequencing problem was used to demonstrate that highly-capable FPGA platforms were a factor of 325 faster than a standard fixed-architecture supercomputer. This is just a single example where digital reconfigurability finds its application. Other fields include - software-defined networks, software-defined radios or cloud computing.

Challenges

The performance metrics and application space described above have indeed fueled the research in that direction. According to Elsevier's database (Engineering Village) in 1991 there were nearly 80 publications with term *FPGA* in the title or abstract, while in 2019 that number has gone up to nearly 9,500. Overall, one may find a modest collection of 150,000 FPGA-related records. It should be remembered that FPGAs while they are the dominant subset of all PLDs, belong to a much wider family of digital reconfigurable systems. There are a few reasons, why platforms such as FPGA are still being heavily researched - some obstacles are yet to be cleared.

The challenges in promoting the digital reconfigurability can be narrowed down to three main aspects. Firstly, as this is inherently a transistor-based platform, its performance scaling is heavily linked to the infamous Moore's Law [45]. That is, achieving rapid performance scaling is becoming more difficult, as the technology node of the classic integrated circuit process has nearly reached its limit. One discussed solution to delay the inevitable end to Moore's Law is to take advantage of the third dimension and pack more transistors, more computational power vertically. This has already been demonstrated and analysed by some groups [176].

The second challenge facing reconfigurable systems is the architectural overhead. Compared to custom ASIC, FPGAs are based on resource redundancy - the oversupply of building blocks is often not fully utilised. Additionally, reconfigurable platforms require hardware to perform re-

configuration - in the case of floating gate MOSFET this is a high voltage tolerant programming network, characterised by large dimensions. It is estimated that single purpose platform with the function of one FPGA configuration can be as much as 35 times smaller, 4 times faster and consume a tenth of the power [177]. Hauck calls this *The Law of FPGAs vs ASICs* : "For any FPGA-based application, there is an ASIC implementation of the system that is AT LEAST as fast, dense, power-efficient, and cheap in (very) high volumes as the FPGA based solution" [178]. The statement is an important one, however not at all surprising, as custom solution is sought usually for those reasons.

Finally, possibly the biggest challenge facing reconfigurable systems is reconfiguration itself: how to optimally synthesise a given problem with available hardware? This is called *expressive power* of a platform [168]. In general, circuit design is an NP-complete problem - it would take a non-deterministic Turing machine a polynomial time to solve the problem. Reconfiguration can be thought of as a circuit design problem with certain restrictions, such as number of available components or final bandwidth. Moreover, often multiple hardware realisations of the problem exist. It is likely impossible to carry out an exhaustive search for the optimal solution, and sometimes the search can return a null solution as well. It may be the result of either low-performing synthesis tool or truly lack of a feasible solution in the space available.

2.7.2 Analogue Platforms

The Case for Analogues

Given the qualities of digital platforms it may seem at first that analogue platforms will have a difficult time making an impact in the presence of FPGAs. After all, FPGAs manipulate very robust, discrete signals, with high immunity to external noise, while analogue signals often demand high fidelity of circuit blocks and high bandwidth of the system, making it therefore difficult and complex to realise. Moreover a stream of digital bits is much easier to manipulate, store and reproduce, whereas analogue signals very often cannot be stored without some information loss. It may seem surprising then, that there is in fact a strong case for reintroduction of certain analogue platforms. In fact, Hasler writes: *the hope for programmable and configurable analog and mixed-mode devices has been at least as strong if not stronger than the original drive for digital reconfigurability* [169].

The first analogue reconfigurable platform can be traced back to as early as 1870's. Lord Kelvin designed and built a tide-predicting machine, that was able to repeatedly evaluate the otherwise laborious sum of trigonometric functions. This invention was later generalized by Claude Shannon in his seminal paper, where he discussed the mathematics of a hypothetical machine able to solve differential equations in the continuum - the analog domain [179]. Shannon has proven in 1931 that a theoretical reconfigurable machine able to solve any differential equation

problem - a General Purpose Analog Computer (GPAC) - would require banks of just 5 different components: adders, multipliers, integrators, constant units and amplifiers. Some mechanical analogue computers existed beforehand, but lacked the computational power or were simply too cumbersome to use.

Rather unfortunately from the perspective of analogue computing, introduction of vacuum tubes and later MOSFETs and the invention of the integrated circuit process coincided with the mathematical formulation of general purpose computers and subsequently led to analogue solutions being set aside. The non-idealities of the analogue building blocks - offsets, noise, drift, non-linearity to name a few, are responsible for the dominance of digital versus analogue circuits. Digital systems from the early days tackled all of those: as technology progressed, IC processes became more precise, repeatable and their characterisation became more accurate. This enabled the analogue platforms to resurface in the research domain in the early 1990s [180].

Prior to the publication by Lee and Gulak [180], there existed a notion of fixed architecture with settable coefficients, such as single chip analog neural network [181]. However as mentioned earlier, Hasler clearly explains the nomenclature - these were programmable not reconfigurable platforms. For a long time this was the closest attempt at realising FPGA's analogue equivalence - the field programmable analogue array. Lee and Gulak took this concept and discussed using subthreshold technique - simulated bipolar behaviour with FETs in weak-inversion mode.

Architectural Classification

There are two major classes of FPAA's in literature: current-controlled and FGFET-based. The class distinction is made based on the method of reconfiguration, as the rest of the architecture is dependent on it. There is a third class - bank of elements, but in reality it is an incredibly simplistic and limited approach, used in early solutions as a proof-of-concept.

Bank of Elements: The platform developed by Lee and Gulak belongs to the third class. Developed in $1.2\mu\text{m}$ CMOS process it featured relatively few op-amps with a bank of capacitors and resistors which could be connected to the appropriate terminals through configuration bits stored in registers. At the time transistor switches were not regarded as a feasible solution to fabric interconnecting. Instead the authors opted to introduce a 12T, highly linear transconductor elements. Due to this approach the complexity of the fundamental architecture of the FPAA simply exploded, as every switch grew over 12 times in size. Using the scale of digital systems discussed earlier, the bank of elements approach can be compared to SPLDs. Small, individual subsystems, such as filters could be tested, however practical applications were not possible.

Current Controlled: Pankiewicz *et al.* [182] present a current controlled method of realising FPAA's reconfigurable fabric. A tuneable operational transconductance amplifier (OTA) is the

constituent element in their design. The OTA features a programmable current mirror - a binary ladder of 31 mirrors. The entire design is differential, and thus features higher immunity to external noise. The interconnecting fabric is realised with simple MOS switches. The full circuit diagram of just a single programmable OTA is a result very complex, and must be designed with utmost care.

Functional synthesis is achieved with classic $g_m C$ techniques. To achieve full control of integrators, Pankiewicz proposes to use a binary ladder of 31 capacitors, giving a total of 5 bits of capacitance tunability (with LSB of 0.438pF). This combined with 5 bits of transconductance control gives 1024 (not necessarily distinct, group claims the max/min ratio of 700) reconfiguration states. A complete array of 40 OTA-C elements, rather surprisingly is reported to exhibit a 20MHz bandwidth.

FGFET: Floating gate FET based FPAA arrays as of writing of this thesis are solely researched by a single group led by Hasler. Nonetheless, the proposed approach can be regarded as the most complete and promising to date. The large scale FPAA platform is as opposed to previously discussed methods the closest analogue relative of the powerful FPGA.

The FPAA platform, called RASP [183] or reconfigurable analog signal processor utilises FGFETs embedded in the switch fabric as well as programming networks to perform reconfiguration. They act both as switches and as analogue memory cells (discussed in section 2.3.3): they direct signals and scale the circuit parameters.

RASP is a standalone fully functional analogue platform, featuring an open-source microcontroller and SRAM while the bulk of the chip is taken up by the FPAA fabric itself. The fabric is composed of an array of digital and analogue blocks (computational logic blocks - CLB, and computational analogue blocks - CAB). The mixed-mode design is one of the milestones that made FPAA more popular in recent years. While analogue solution have the potential to outperform digital engines in many areas, e.g. calculus, the future by many is considered to be a hybrid combination of the two worlds [168], [169], [178], [183], [184]. An overview of RASP capabilities is briefly discussed in subsection 2.7.2 *Reconfigurable Analog Signal Processor*.

Behavioural Classification

Malcher and Pankiewicz [185] propose a higher abstraction in classifying analog reconfigurable platforms: (1) static non-linear, (2) dynamic linear discrete time, (3) dynamic linear continuous time, and (4) other.

This approach determines system's true 'analogueness'. For example devices from category (1) can be just simple mathematical operators: multipliers, divider, log-based functions and so on. They are linked by the lack of time dependence in their functioning - they are analogue in a single dimension and that is the signal amplitude.

Class (2) circuits add to class (1) in that they allow for some time variation. Circuits in this class are best described by Z-transforms and are often realised with switched capacitor techniques. Signal amplitude is analogue, while its time dependence is discrete.

Systems in class (3) are 'the most' analogue - two-dimensional continuity is possible in both signal value and time. Systems of this kind are best described by Laplace Transforms and include circuits whose behaviour is expressed as a linear differential equation, e.g. classical filters and other linear, time-invariant systems.

However, in light of hybrid solutions described by Hasler this classification does not reflect the progress made in the field of FPAA's. Those advances ought to be either placed in class (4) or into a new class (5): dynamic linear hybrid circuits. Class (5) platforms unify the worlds of analogue and digital systems. Though, one can argue that original classification refers to only true analogue systems and as such hybrid platforms should not be accounted for. As a counter argument, one might say that there is no, and never was, a clear distinction between the two worlds - are switched capacitor systems truly analogue? Therefore drawing a line is arbitrary.

The point above raises an interesting question - what makes a memristors analogue in its nature? Is it the fact that it can be programmed to many different resistive states? If so, how many to be deemed analogue? Binary devices are undoubtedly digital, but a device with a 1000 tightly packed states? Or maybe it is actually the range coverage and the tightness of state packing within that range? If a memristor with programming range from 1 to 2 Ω is characterised by 10 non-volatile, non-overlapping states, it sure does seem "more analogue" than another memristors with 10 states distributed over a much larger range. Perhaps the answer to "what makes memristor analogue" lies not in what it does, but how it does it? Unlike logic gates, memristors continuously respond to incoming signals. Even if a device is in so-called sub-threshold operation, its state will still fluctuate. As opposed to logic gates, where slight perturbation of the input does not result in any perturbation at the output, memristors are very sensitive. So perhaps it is the physics-driven state change that allows many to subconsciously view memristors, or floating gate FETs as analogue components.

This debate can continue, as every engineer will have a slightly different opinion. The bottom line is that classification is used to categorise items based on the features of interest. Based on that, existence of the fifth class is justified.

Reconfigurable Analog Signal Processor

The RASP 3.0 presented in 2016 [183] is, to the best of the author's knowledge, the first system-on-chip (SoC) standalone realisation of the FPAA. Its architecture is shown in Figure 2.19. The key elements are: microcontroller, SRAM memory, registers, I/O communication ports, bank of digital to analogue converters (DAC) and the fabric itself.

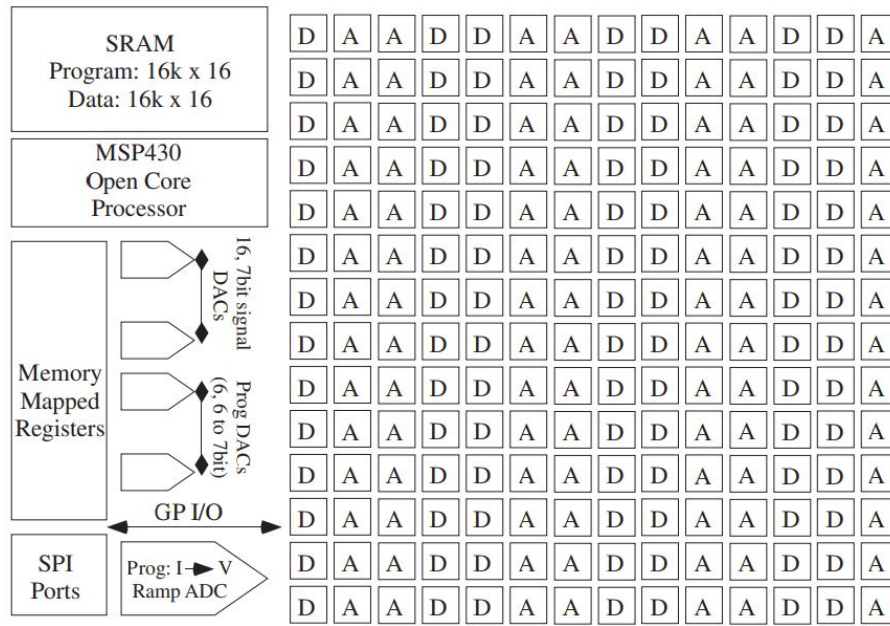


Figure 2.19: High level design of the RASP FPAA. Figure reprinted from [183]. *Copyright 2016 IEEE*

The fabric can be further decomposed into CLBs, CABs, connection blocks (C blocks) and switch blocks (S blocks). Each CLB consists of a four input lookup table (LUT), while CABs have OTAs, individual transistors, capacitors and other primitives. Architecturally CABs are a lot more complex, however also a lot more powerful than a single LUT. Overall, the fabric features 98 CABs and 98 CLBs.

Using RASP Hasler's group has shown experimentally that the large-scale FPAA in fact surpasses purely digital architectures in vector matrix multiplication. They have demonstrated an improvement of over 1000 in the metric of number of multiply-accumulate (MAC) operations per second per unit of power [186]. To put this into perspective the first digital signal processor performed at the level of 10MMAC/s/W, that is 10 million MAC operations per second per Watt of power. Current digital techniques operate at the level of 10MMAC/s/mW - a thousand times energy efficiency improvement. An analogue VMM on RASP shown by Hasler performed at the level of 10MMAC/s/ μ W - a further 1000 fold improvement. An ASIC designed classifier is capable of working at roughly 10MMAC/s/nW. It is estimated that biological efficiency reaches the level of around 1MMAC/s/pW. That is, there is a room to improve by a factor of 100 than the best integrated circuit available to date. These results are not surprising. Already in 1990s Mead made the prediction that analogue computation could be as much as 1000 times more efficient than digital [187].

The group has shown a number of applications of the RASP. On the circuit synthesis side, they have built and tested ladder filters and envelope detectors showing identical performance to real circuits [188]. On the neuromorphic side, the group has demonstrated the use of FPAA for implementing Winner-Takes-All classifier [189]. They have used an example of XOR classifi-

cation - a non-linear problem, usually requiring more than one layer when implemented on an artificial neural network. Finally, the group has also shown a rudimentary speech recognition classifier, able to detect the word 'dark' using the WTA classifier. The audio was decomposed into a number of subbands through a reconfigurable bandpass filter. Each band passed through an envelope detector followed by a low pass filter, before being input into the WTA classifier [183].

Memristor-Filled FPAA

Quite relevantly and possibly interestingly Poikonen discussed the use of memristors on an FPAA platform [190]. For that reason they developed an integrated circuit and post-processed arrays of memristors on top. The group used a MIM-type device, with palladium and tungsten electrodes, and tungsten oxide as the active layer. The switching behaviour is attributed to the migration of oxygen vacancies, i.e. it is a valence change mechanism depicted in Figure 2.8. However, the presented concept didn't succeed as one might have hoped, because the memristors used exhibited strong relaxation properties. This meant they were volatile, though the group argued some application where this is useful may exist.

On top the memristors, FGFETs are also employed to control currents and to act as switches. Another downside of the proposed implementation is the high ON resistance of the FGFET switches. The group reports resistances in the range of $10\text{k}\Omega$. However, Hasler defends this [169], treating the switch fabric as a resistive design element. This vastly complicates the designs, as precise modeling of losses on routing is required and lossless connections are nearly impossible.

Other Academic Platforms

Here a short list of other academic projects is presented (Table 2.3). The list is by no means exhaustive. The entries are not discussed in detail, as they either belong to one of the classes described earlier, or they did not provide any new significant changes to the current *status quo*.

Commercialisation

While a VLSI technology is still researched, smaller platforms are already available in production. Because the technology is in its infancy there is little demand for the currently existing platforms, and some have even been discontinued since. Table 2.4 gives an overview of what is and was available to customers. It is worth noting that the term 'field programmable analogue array' has not solidified both in research and in industry. As such other variations exists such as:

Project / Research Team	Year	Reconfiguration Method	Systematic Complexity	Design Elements	Demonstrated Deployment	Bandwidth
RASP 3.0 [188]	2016	FGFET	98 CABs 98 CLBs	OTA, Transistor, FGFET, Multiplier, LUT	Analogue Signal Conditioning Neuromorphic	55MHz (350nm) 45GHz (45nm)* 90GHz (10nm)*
Pankiewicz [182]	2002	Binary Current Mirror Ladder	40 CABs	OTA, Current Mirror, Capacitor	Analogue	20MHz
Henrici [191]	2009	FGFET	55 CABs	OTA, Capacitor	Analogue Signal Conditioning	186MHz
Fernandez [192]	2011	MOS Switches	25 CABs	Translinear BJT-like Elements	Analogue Non-Linear Operations	20MHz
Soliman [193]	2012	Digital Control	7 Macrocells	CCII	Analogue	100-200MHz
Gaudet [194]	1997	Transmission Gates	4 CABs	CC, Transconductor, Capacitor, Buffer	Analogue Non-Linear Operations	11-13MHz
Loobi & Lyden [195]	2000	MOS Switches	1 CAB	Op-Amps, Adder, Subtractor, (Resistor Ladder)	Power Signal Generation	1MHz
Chang [196]	1997	Switched Current, Digital Word Control	N/A	Current Copier, Phase Current Comparator, Output Switch, Current Reference	Signal Generation Analogue	N/A

Table 2.3: Comparison of academic efforts in the field of FPAA. *The bandwidth is estimated, as the chip was not realised.

- Field-Programmable Mixed-Analog-Digital Array (FPMA)
- Electrically Programmable Analog Circuit (EPAC)
- Totally Reconfigurable Analog Circuit (TRAC)
- Field Programmable Analog Device (FPAD)
- Reseau analogique programmable (RAP)
- Field Programmable System-On-a-Chip (FIPSOC)
- Reconfigurable Analog Signal Processor (RASP)
- In-System Programmable Analog Circuit (ispPAC)
- Dynamically Reconfigurable (Programmable) Analog Signal Processor (dpASP)
- Programmable System on Chip (PSoC)

As indicated in Table 2.4, only two companies are currently producing FPAA or FPAA-like integrated circuits - Anadigm and Cypress. The presently sold platforms benefit from full ecosystem built around them - graphical user interface, automated hardware mapping and monitoring. Other endeavours were either too primitive, lacked minimal functional complexity, were too slow or simply impractical. While in the past other companies such as Motorola were involved in manufacture of FPAA chips, the projects have closed, as the state-of-the-art digital chips were better suited for deployment.

Company	Family	Control	Systematic Complexity	Design Elements	In Production	Bandwidth
Anadigm [197]	Vortex dpASP	MOS Switches, Switched Capacitor	4 CABs 4 CABs	OpAmp, Filter, LUT, SC, VGA	End-of-Life Yes	2MHz 2MHz
Cypress [198]	PSoC	Switched Capacitor MOS Switches	1-12 UAB	SAR, ADC, OpAmp, Comparator, Sigma-Delta, Filter, Capacitive Sensor, AMUX	Yes	<10MHz
Lattice Semiconductor [199], [200]	ispPAC20	SRAM	1-8	Filter, Amplifier, Integrator,	X	1-1.57MHz
	ispPAC30	E2CMOS	PACells	Analog ALU	X	
	ispPAC80	MOS Switches			X	
Motorola [201]	MPAA020	Switched Capacitor MOS Switches	20 CABs	OpAmp, SC	X	0.2MHz
Zetex [202]	TRAC020	MOS Switches	20 Cells	Add, Negate, Log, Antilog, Differentiate, Integrate	X	3-7MHz
IMP, Inc. [203], [204]	EPAC	MOS Switches Switched Capacitor	N/A (Expert Cells)	DAC, Amplifier, Comparator,	X	N/A (<1MHz)
SIDSA [205]	FIPSOC	MOS Switches	N/A	Amplifier, Filter, Comparator, ADC, FPGA	X	N/A

Table 2.4: Comparison of commercially available and discontinued FPAA-like products. UAB stands for Universal Analogue Block, SC - switched capacitor, VGA - variable gain amplifier, SAR - successive approximation register (ADC), AMUX - analogue MUX.

Application Horizon

Technology is nothing without applications. There is a number of strong motivations behind continued growth of the analogue reconfigurable domain. While FPGAs continue to take over most DSP tasks - classical computing and now also neuromorphic computing, here we look at the application space of FPAA platforms. The following areas are listed in an order from *low-hanging fruits* to perhaps surprising and non-intuitive ones.

The foremost application is to use the analogue platforms for educational purposes, as easy-to-use breadboards with embedded components. Hasler [206] came up with an FPAA centred VLSI course that aims to teach neuro-inspired circuit design using the analogue reconfigurable platform. Their ecosystem benefits from a software interpretation tool, that allows the students to design the circuit on a PC and is automatically translated into a hardware design.

Next obvious application may be rapid analogue IC-level prototyping [207]. Without the need to go through long cycles of design-layout-fabrication, FPAAs allow for quick, yet rough, idea testing and circuit development. Of course, complexity of the prototype is determined by the underlying architecture. For example, the SoC platform developed by Hasler would not allow for low-power prototyping due to the use of FGFETs. However behavioural synthesis is naturally made possible.

The first practical, yet obvious, application is to employ FPAA platforms in remote or harsh environments, where human access is minimal. A demonstration of remote capabilities, as an Internet-of-Things (IoT) device, is conducted in [208]. While scientifically interesting applications have not been pursued just yet, it is not difficult to imagine self-calibrating and self-adjusting space exploration equipment, e.g. antennas, impedance matching networks, or even computational units. Those software defined solutions already exist on FPGA [209], however analogues may prove more efficient.

Remote adjustments, by definition require 'the reconfigurator' - a system responsible for mapping instructions to hardware [185]. By removing the human interaction from the process and allowing for automated self adjustments, based on some cost function, applications such as evolvable hardware become possible. A great, albeit dated, review of the progress and the future of evolvable hardware is presented in [210]. Evolvable hardware brings the concepts of genetic algorithms to hardware, allowing for potentially new, more efficient and undiscovered circuit typologies to be developed. This concept fits well the FPAA, because some platforms already enable dynamic reconfiguration, that is the hardware is able to change during operation. An example of dynamic abilities of an FPAA platform is automatic gain control [211], an application often used to demonstrate capabilities of an analogue system.

The realisation of automated 'reconfigurator' necessitates the use of a computational unit. As mentioned earlier, an analogue computer is shown to be better suited for certain signal processing tasks. Analogue reconfigurable hardware such as FPAA have been shown to excel at neuromorphic computation such as classification [189]. Some groups even propose FPAA architectures targeting the bio-inspired field of computation by mimicking synaptic connections on hardware [212].

2.8 Summary

This chapter is, to the best of the author's knowledge, the most complete and thorough discussion of reconfigurable components and systems. Modern day approaches building on historically important developments are presented. The resistive switching phenomenon is singled out, because the remainder of the thesis builds around the memristive components. The RS importance is stressed through thorough discussion of underlying physics, behavioural description and phenomenological modelling. Other intuitive elements such as memcapacitors are presented as they form an extension to the mem-concept.

The discussion then takes a step back and looks at what is required before whole systems can be realised. Of particular interest are the FPGA and analogue FPAA platforms, as they are regarded to have unprecedented impact on the future of circuit design. Focusing on FPAA platforms, works by Hasler are discussed in more detail. The SoC realisation is contrasted against other academic efforts, showing a huge performance margins over other platforms. Finally, some commercial realisations are presented. However, as shown they greatly trail behind the academic works and are very limited in their deployment area.

This discussion is by no means exhaustive. It would be a Sisyphean work to attempt covering all aspects, as the domain of reconfiguration is currently experiencing fast growth in interest. This discussion barely scratches the surface. Most interesting and relevant points were extracted and presented, such that the context of the following work is well embedded in reader's mind.

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Chapter 3

Memristor Enabled Reconfigurable Analogue Blocks

This chapter begins with a theoretical overview of gyrators. Their usefulness in the context of creating variable components is explained. Using bi-layer memristors and a PCB test platform measurements of a tunable gyrator, inductor and capacitor are presented and discussed. Furthermore, the chapter sheds some light on complex gyrator structures: a formally defined upper bound of the gyrator's performance in circuits is presented. Following from the gyrator's non-idealities, frequency dependent negative resistors are shown to be realisable. The original contributions of this chapter are: universal impedance scaling circuit; memristive current control; memristor tuned inductor, capacitor and gyrator; theoretical derivation of performance limitations stemming from CMOS processes.

3.1 Realising Gyrators

3.1.1 Background

Tellegen postulated the existence of a fifth passive linear element: a gyrator [1]. Controversially, the addition of this fifth element, reduces the gamut of fundamental components to just three - resistor, capacitor and gyrator. That is because both the linear transformer and the inductor can be realised with a combination of the main three components as it will be shown later. Nonetheless, gyrators are not widely used primarily due to the lack of a true passive realisation.

Active broadband realisations of gyrators alongside gyrator-like structures have been used in communication, mainly telephony or in graphic and audio equalisers. Their niche is where electrically large, good quality factor, physically small inductors are required. Technologically,

physical capacitors are closer to ideal than physical inductors are. On the other hand, inductors realised by combining broadband gyrators with high-quality capacitors have much better inductive behaviour, albeit at the cost of increases power dissipation and noise.

3.1.2 Theory

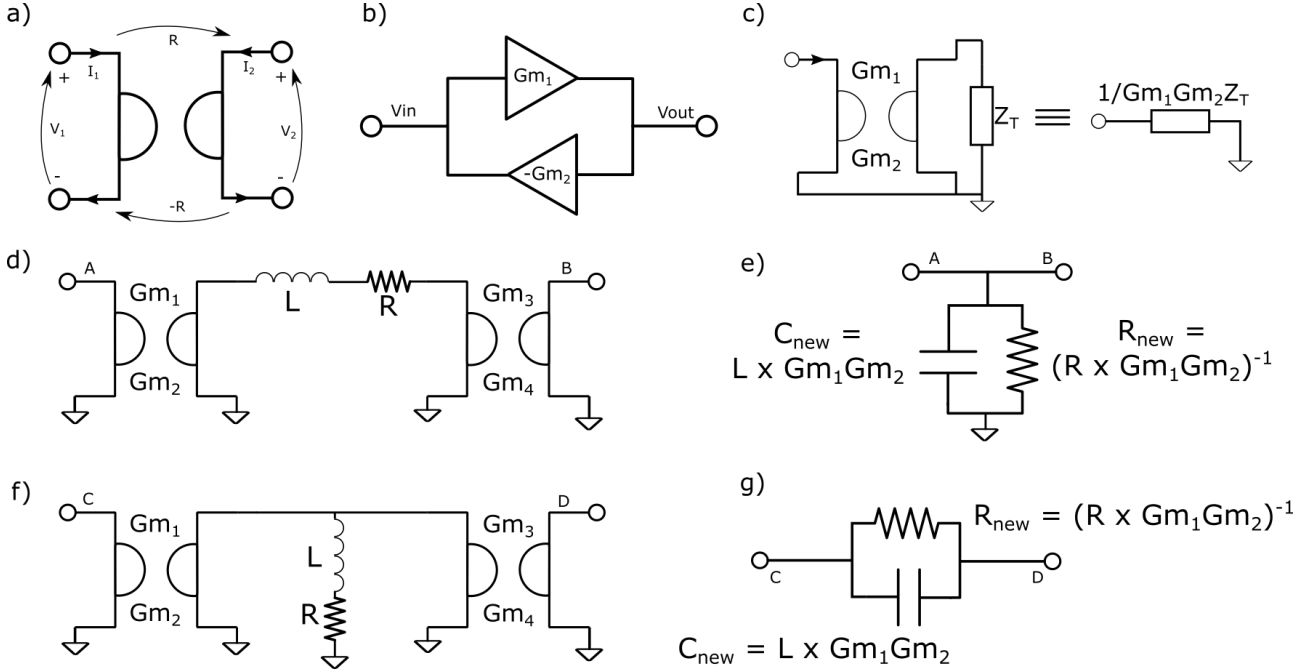


Figure 3.1: Fundamental characteristics of the gyrator. **a)** Gyrator symbol, representing the device as a two-port, 4 terminal network. Arrows denoting potential point towards higher voltage. **b)** Active realisation of a gyrator. **c)** Impedance inversion property. **d)** and **e)** Floating component topology, showing conversion of floating series into grounded parallel combination. Nodes A and B show the same terminals in both circuit diagrams. There are in fact the same node. **f)** and **g)** Floating topology, showing conversion of grounded series into floating parallel combination. Nodes C and D show the equivalent nodes between both diagrams.

A schematic symbol of the gyrator, as proposed by Tellegen, is shown in Figure 3.1a. The device is a two-port with 4 terminals. The voltages and currents on the two ports are related to one another through the following set of equations:

$$v_2 = Ri_1 \quad (3.1)$$

$$v_1 = -Ri_2 \quad (3.2)$$

While there is no real resistance, the units are Ohms. Therefore the output current is linearly dependent on the input voltage, and the input current is linearly dependent on the output

voltage. In fact, a theoretical passive gyrator is a lossless device, where instantaneous power consumption is zero:

$$P_1 = i_1 v_1 = -R i_1 i_2 \quad (3.3)$$

$$P_2 = i_2 v_2 = R i_1 i_2 \quad (3.4)$$

$$P_T = P_1 + P_2 = -R i_1 i_2 + R i_1 i_2 = 0 \quad (3.5)$$

The scaling constant is referred to as gyration conductance or gyration factor - K :

$$K = R^{-1} = G_m \quad (3.6)$$

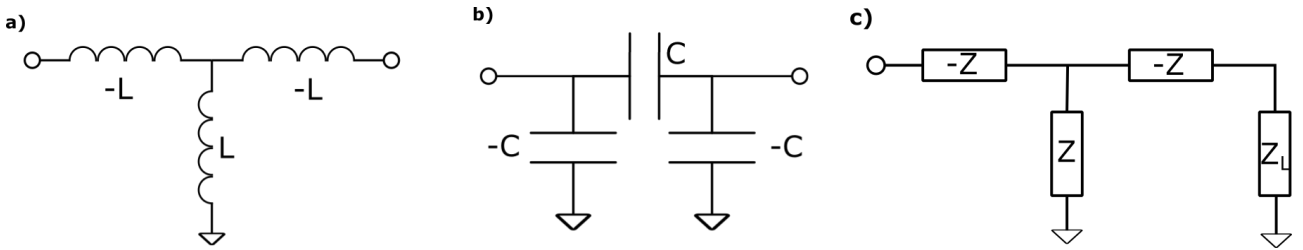


Figure 3.2: J- and K- Inverter Topologies. **a)** Three T-connected inductors, two with $-L$ values and one with L form a K-inverter. **b)** Three pi-connected capacitors (2 negative-valued and one positive) form a J-inverter. In reality negative-valued components are not readily available; designs often absorb those values into nearby components. **c)** Circuit used for analysis of the impedance inversion property.

In theory both the forward and backward gyration factors are equal in magnitude. This is necessary to ensure lossless operation. True standalone passive realisations of the gyrator are not possible, as they require negative-valued capacitors or inductors (e.g. narrow-band gyrators such as J-, K-inverters - Figure 3.2). The general behaviour of J-,K-inverters is derived below. Taking a T-structure as an example, let's assume there is a load Z_L connected at the output. The analysis assumes that the K-inverter is made of two negatively valued $-Z$ impedances and one positively valued Z impedance, e.g. in Figure 3.2)c $Z = j\omega L$ deems is equivalent to the circuit is subplot a. Then we have:

$$Z_{in} = ((Z_L + (-Z))^{-1} + Z^{-1})^{-1} + (-Z) \quad (3.7)$$

$$Z_{in} = \left(\frac{(Z_L - Z)Z}{Z_L - Z + Z} + (-Z) \right) \quad (3.8)$$

$$Z_{in} = \frac{Z_L Z - Z^2}{Z_L} - Z \quad (3.9)$$

$$Z_{in} = \frac{Z^2}{Z_L} \quad (3.10)$$

Therefore by using inductive impedance to invert the load $Z = j\omega L$ and setting the desired frequency of inversion to $\omega = \omega_g$:

$$Z_{in} = -\frac{(\omega_g L)^2}{Z_L} \quad (3.11)$$

Hence at a specific frequency impedance connected at the output of the K-inverter appears to be *inverted* or gyrated from the perspective of the input port.

In practice negative components are absorbed into nearby elements; as a standalone piece of circuitry, gyrators are presently not realisable. To mitigate that, active versions have been pursued, e.g. second generation current conveyor (CCII) based topology as proposed by Sedra [2]. In fact the current-mode method is the most robust way of building gyrators. The CCII blocks are replaced with general purpose operational transconductance amplifiers (Figure 3.1b).

From Figure 3.1b the output current flowing out of the emulated gyrator is:

$$I_{out} = V_{in} Gm_1 \quad (3.12)$$

Similarly current into the input port is:

$$I_{in} = -V_{out} Gm_1 \quad (3.13)$$

which matches the theoretical gyrator behaviour.

In active gyrators, the forward and backward gyration constants do not have to be equal. In fact they can be chosen arbitrarily, however the gyrator loses some of its properties if it is not finely tuned. For generalisation, the two constants will be treated separately.

By inspection of equations 3.1 and 3.2, the phenomenological description of the gyrator can be deduced. Namely, the device reverses the roles of input voltage and current, such that a

positive input phase is mapped to a negative output phase and vice-versa, whilst scaling the magnitude of the connected load. This is called an impedance inversion property of gyrators and is depicted in Figure 3.1c. Through basic nodal analysis:

$$Z_{in} = \frac{V_{in}}{I_{in}} \quad (3.14)$$

$$I_{in} = V_{out}G_{m2} \quad (3.15)$$

$$V_{out} = I_{out}Z_t \quad (3.16)$$

$$I_{out} = V_{in}G_{m1} \quad (3.17)$$

it can be shown that a grounded impedance Z_T connected to the output port of the gyrator is *seen* from the input port as:

$$Z_{in} = \frac{1}{G_{m1}G_{m2}Z_T} \quad (3.18)$$

That is the impedance is inverted and scaled. While for real loads this is but a transformer, imaginary and complex loads undergo behavioural changes. Connecting a capacitor C to the output gives:

$$Z_T = \frac{1}{j\omega C} \quad (3.19)$$

$$Z_{in} = j\omega \frac{C}{G_{m1}G_{m2}} = j\omega L_g \quad (3.20)$$

$$L_g = \frac{C}{G_{m1}G_{m2}} \quad (3.21)$$

where j indicates the imaginary number and ω is the angular frequency in radians per second. By electrically inverting a capacitor, gyrators are able to actively synthesise an inductor L_g with value being the ratio of capacitance and the product of forward and reverse gyration factors. However, this method is still limited - using a single gyrator only allows access to a single port of the synthetic component, i.e. it allows to synthesise grounded impedance functions.

To open up the other port of the device a second gyrator is needed. Intuitively, after reversing the roles of voltage and current, their polarities are switched back. Care must be taken to ensure that the input and output gyrators are matched such that any further loads are not scaled. If they are not matched, then the unmatched gyrator cascade will scale the impedance of the rest of the circuit, which may, or may not, be desirable.

Gyrators, through the impedance inversion property, convert a series combination of components into the parallel combination of their inversions and vice-versa. Moreover, floating components (Figure 3.1d) are mapped into a grounded equivalents (Figure 3.1e) and contrariwise too (Figure 3.1f-g).

Active gyrators are not the only way to achieve impedance inversion. True passive impedance inverters which can achieve similar results exist, but tend to be severely limited in bandwidth. In microwave circuit, for example, one may use a quarter wave impedance transformer, where the characteristic impedance of the line plays the role of the gyration constant. However for broadband electronics from DC to several MHz, such an option is impractical.

In this work gyrators are constructed with two transconductors in feedback configuration (Figure 3.1b). If, somehow, the transconductance of both amplifiers can be controlled simultaneously, then this will result in a variable gyrator. Many off-the-shelf operational transconductance amplifiers provide the terminal to control the bias current of the device. Similarly to the long-tail-pair configuration, scaling the bias current results in directly proportional scaling of the gain of the element. By employing a variable current source e.g. a memristor controlled current mirror, control over gyration constant is achieved also.

3.2 The Memristor as a Component Value Tuner

3.2.1 Bilayer Memristors

The memristors used for this work were developed at the University of Southampton (UoS) by Dr Spyros Stathopoulos (SS) [3]. The devices are bilayers - titanium dioxide and aluminium oxide are stacked and sandwiched between platinum electrodes (Figure 3.3a-c).

Devices were made on 6" oxidised silicon wafers with 200 nm of thermal SiO₂. Bottom electrodes were defined by lift-off in N-Methyl-2-pyrrolidone (NMP) on electron beam evaporation of titanium (5nm; adhesion layer) and platinum (10 nm). This step is followed by negative photolithography and the deposition of 25 nm of TiO₂ using magnetron sputtering (Leybold Helios Pro XL) from a Titanium target precursor in O₂/Ar ambient (8 sccm/35 sccm) at 2 kW power with an additional 15 sccm O₂ flow at the additional plasma source. An additional 4 nm layer of Aluminium Oxide (Al_xO_y) is then deposited with the same tool without breaking the vacuum from an Al target precursor again in O₂/Ar ambient (8 sccm/35 sccm) at 100 W power. Fabrication of the active layer is finalised with lift-off to expose the bottom electrode access pads. The top electrode is fabricated again with electron evaporation of Pt and lift-off in NMP.

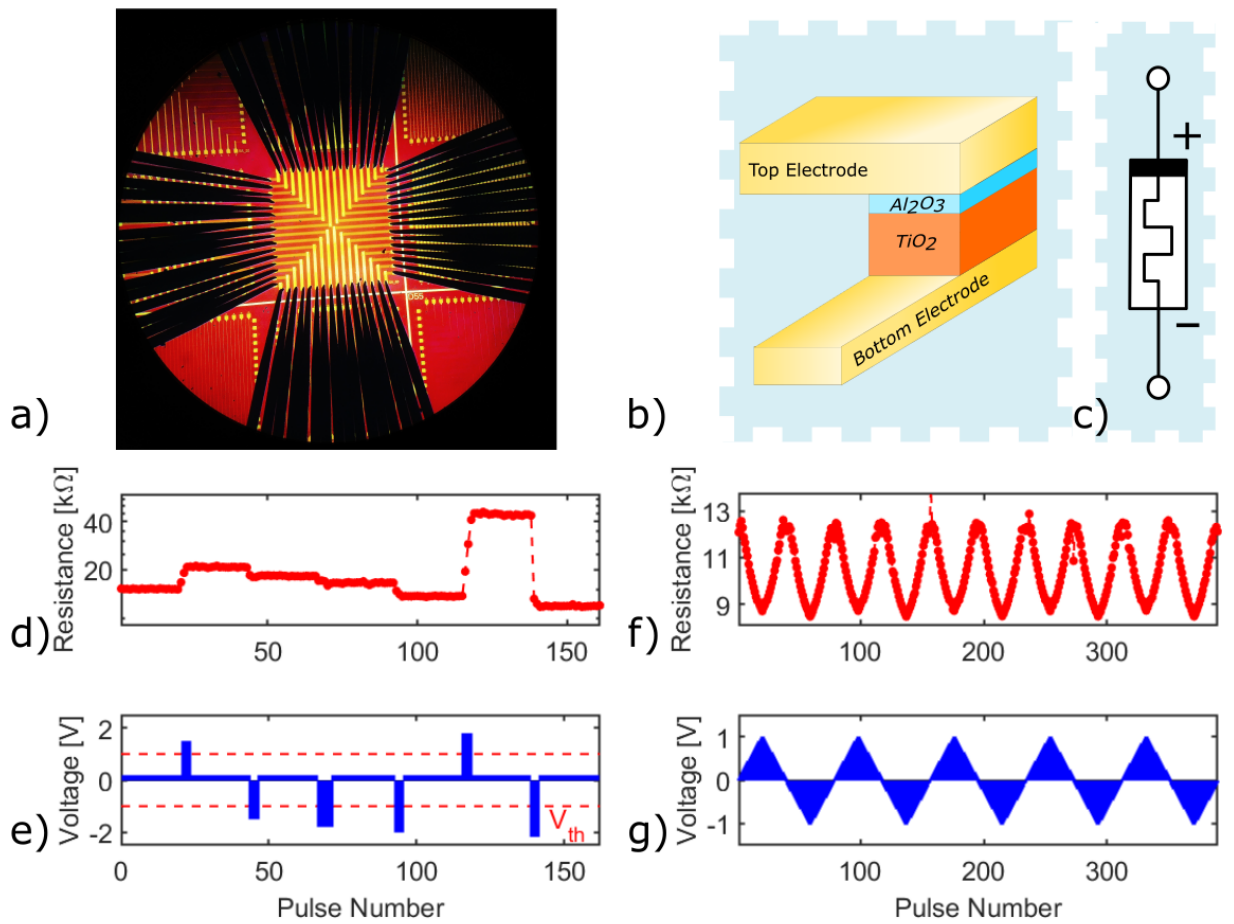


Figure 3.3: Bilayer TiO_2 and Al_2O_3 memristors: leveraging static and dynamic memristive behaviour. **a)** Microphotograph of a memristor discrete device array. Individual devices are accessed by probe needles, also visible in the image. **b)** Structure of a single standalone memristor. The active material (TiO_2/Al_2O_3 bilayer) is sandwiched between the top and bottom electrodes. **c)** Schematic symbol of a memristor. The asymmetric symbol indicates that a voltage applied as indicated acts to decrease the resistance. **d)** Measured resistive state change as response to the voltage stimulus shown in subplot e). **e)** Voltage stimuli above the threshold voltage result in resistive state change, showing the time-voltage dilemma [4]. **f)** Schottky-like behaviour of a memristor below the switching threshold of the device. y-axis is static resistance measured at the voltage indicated in g). **g)** Stimulus waveform for nondestructive sub-threshold current-voltage sweep test.

Non-ideal Behaviour

These devices are subject to several types of non-idealities: threshold behaviour and tunneling diode-like non-linearity. These phenomena are shown in Figure 3.3d-g.

Threshold behaviour: as discussed in Chapter 2, some memristive devices require high enough potentials to switch. This in fact is advantageous to non-volatile reconfigurable circuits, as it allows to simply and non-destructively read out the device. In this work, it was found experimentally that the bulk of the devices could be safely read out or interrogated with

potentials below 0.5V. Fabrication process variation resulted in a distribution of device properties: some memristors exhibited switching thresholds as high as 1.5V, whereas other would switch during read out.

Tunneling diode-like behaviour: The devices strongly resemble tunneling metal-insulator-metal (MIM) diodes. This is because memristors follow a similar structure, where the insulator allows for controlled tunneling current modulation. A standard MIM diode, if made of two identical electrodes with a uniform insulator, will be fully symmetrical. Bilayer memristors do exhibit a small degree of non-symmetry due to the nonuniform dielectric, however as a first order approximation it can be neglected at subthreshold operation.

Looking at the energy band diagrams of the simplified memristor at subthreshold operation, shown in Figure 3.4b-d, it is clear that the device should be polarity agnostic, due to inherent physical symmetry. Therefore the tunneling current, which is discussed in greater detail in Chapter 2, will be equal at both positive and negative polarities, and its dependence on the electric field will be nonlinear, as measured and shown in Figure 3.4a. For completeness, the results clearly indicate subthreshold operation, as the characteristic hysteresis is not present. Therefore the device has not undergone any resistive changes.

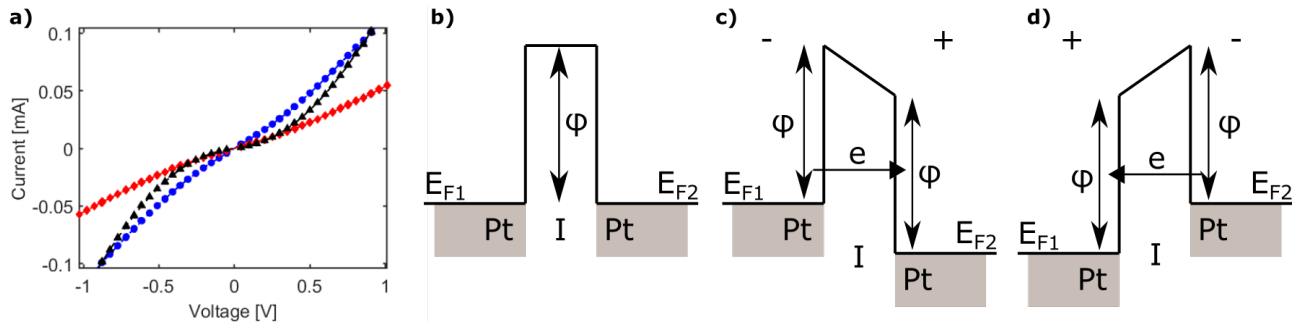


Figure 3.4: Resemblance of tunneling diode behaviour at subthreshold operation. **a)** Non-linear IV characteristic of the memristors tested. 3 supposedly identical devices from the same wafer were formed with the same forming procedure and an identical IV measurement was performed on each of them, showing symmetric, non-linear behaviour, strongly resembling that of a MIM tunneling diode. Nonetheless each device shows a different response which is the effect of the well-known device-to-device variability issue affecting memristive technologies. **b)** Energy band diagram of the simplified memristor at rest. The device is symmetric and the bilayer structure is omitted. $E_{F1,2}$ represent Fermi levels, while ϕ denotes the work function of the metal. **c)** Under positive bias, tunneling current is established. **d)** Due to assumed symmetry, under negative bias equal tunneling current should flow, whose magnitude is determined by the magnitude of the electric field.

3.2.2 PCB Test Platform

To test whether memristor can reliably control the gyration operation, memristor-controlled gyrated impedances were realised on a printed circuit board (PCB). Off-the-shelf transconductors were selected: to realise gyrators LM13700 OTA was used. The LM13700 benefits from a

equilibrium. The load line behaviour effectively made impossible to precisely select the static memristance. This was rectified in further CMOS simulations and realisations, by enforcing a constant voltage across the device.

The current mirror was designed in such a way that the maximum bias current (2mA as per LM13700 datasheet) was not exceeded at the minimum memristance of around $3k\Omega$. The minimum memristance of the devices was strongly dependent on the series resistance of the electrodes and chip traces. SS at UoS fabricated devices of varying geometries - from $1\mu m$ to $100\mu m$ electrode width. Through experimentation $40\mu m$ geometries resulted in minimum memristance of around $1k\Omega$. Below the minimum value, the device would irreversibly short, becoming a fixed resistor.

The final iteration of test PCBs is shown in Figure 3.6. The memristor was located on a wafer connected through a probe card and extension leads. Two of the extension leads corresponding to the memristor of choice where when directly connected to the PCB through the terminals located in the top left corner of each PCB depicted in the photograph. Between tests, the device would be manually disconnected from the PCB and plugged back into the programming platform.

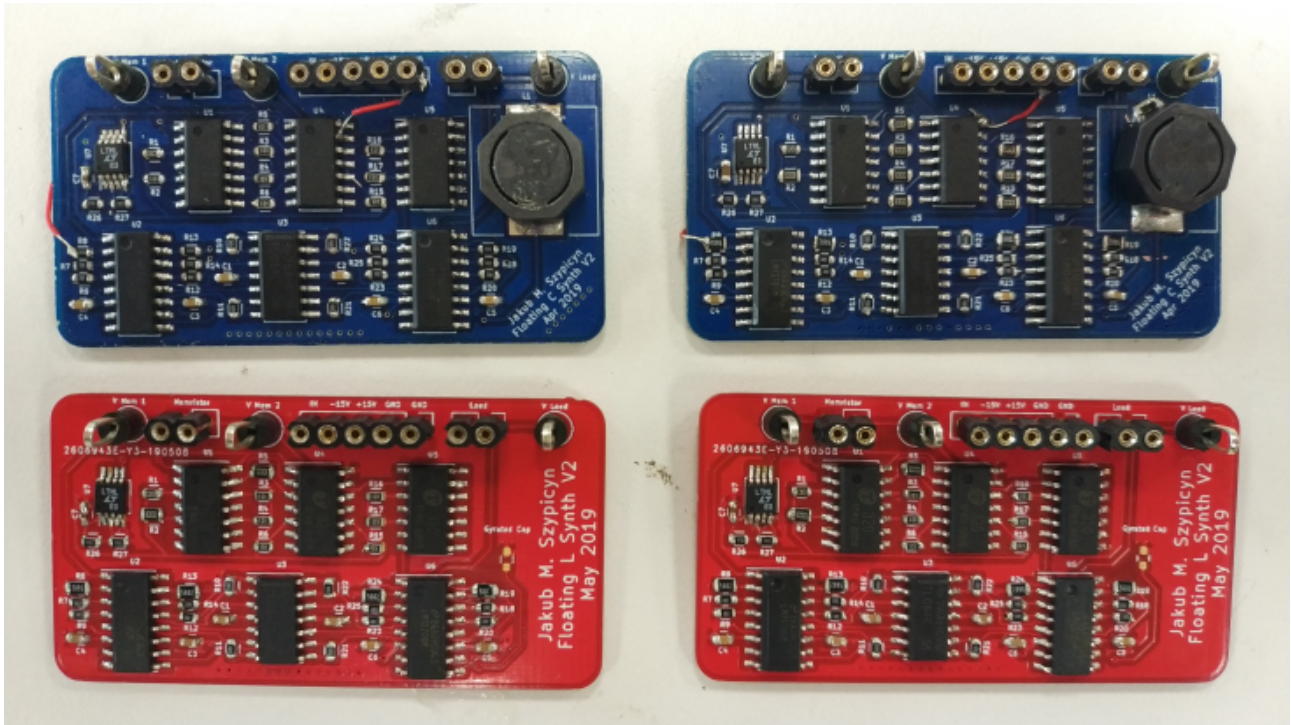


Figure 3.6: Assembled printed circuit boards used for testing of the impedance function scaling concept. This is the third iteration, following a breadboard design and first general PCB design, where the gyrated load could be freely connected. For the purposes of more precise testing, this generation of PCBs had a fixed gyrated load - blue PCBs inverted physical inductors, red PCBs inverted physical capacitors. 7 IC packages are present on each board: 2 dual LM13700 OTAs, 1 quad operational amplifier for buffering, 3 BJT arrays and 1 linear voltage regulator.

3.3 Memristor-Tuned Gyrator

3.3.1 Current Scaling

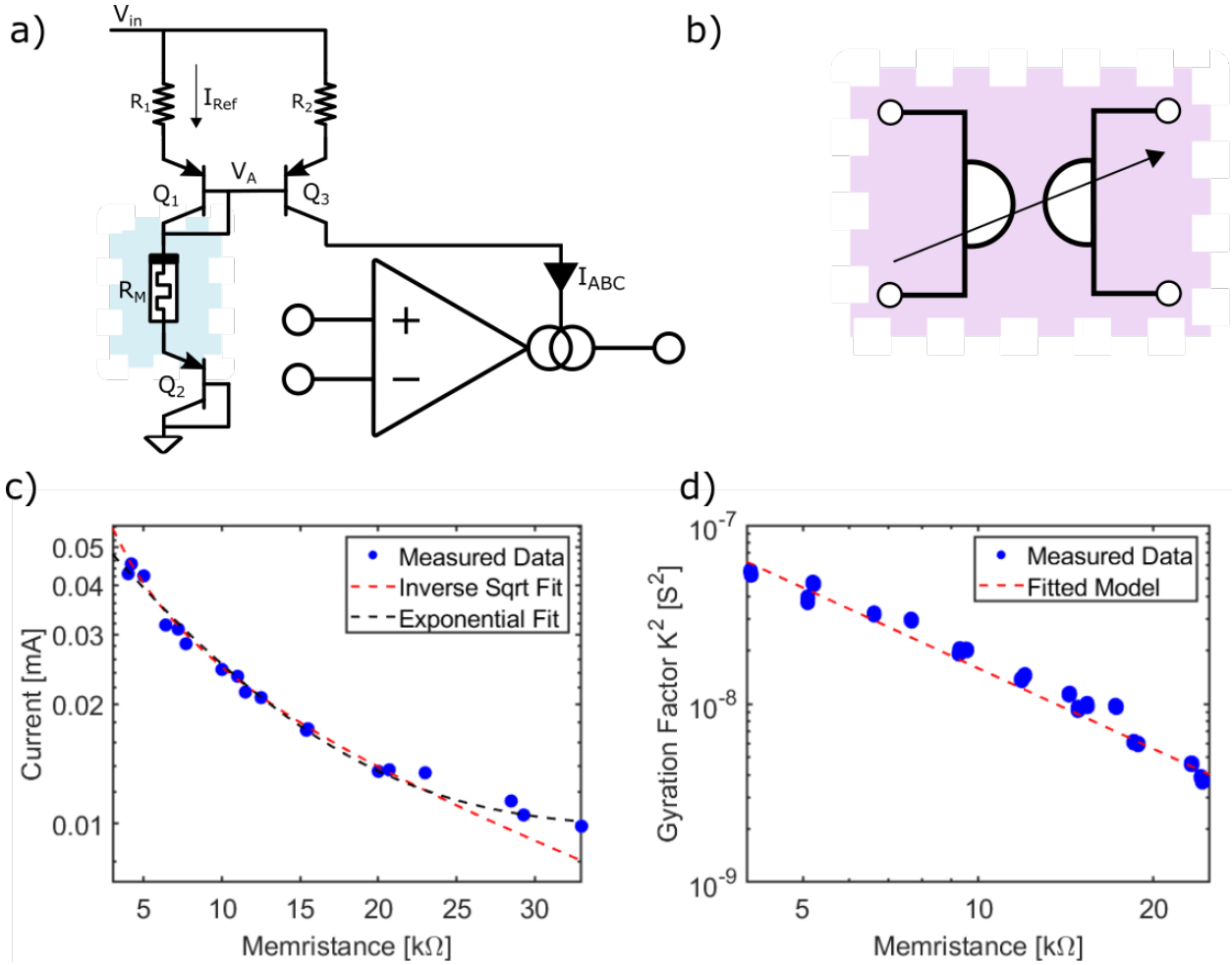


Figure 3.7: Memristor tuned gyrator. **a)** Variable transconductance amplifier - a building block of a variable gyrator. A memristive current mirror controls current bias (I_{ABC}) into the OTA, tuning its gain. **b)** Schematic symbol of tuneable gyrator; it is an impedance inverter, a 4 terminal device. (c.f. transformer). **c)** Measured reference current of the memristor controlled source alongside proposed exponential and inverse square fitted models. **d)** Modulating the resistive state of the single memristor in (a) tunes the gyration constant. A simple model is proposed for the limited range of memristances used.

The relationship between memristance and the bias current is not an obvious one. Using the component definitions shown in Figure 3.7a two expressions for the node voltage V_A can be derived (assuming base currents are negligible):

$$V_{BE2} = V_T \ln(I_{Ref}/I_S) \quad (3.22)$$

$$V_A = V_{BE2} + I_{Ref}R_M \quad (3.23)$$

$$V_{BE1} \simeq V_{BE2} \quad (3.24)$$

$$V_A = V_{in} - I_{Ref}R_1 - V_{BE1} \quad (3.25)$$

V_{BE} is the potential drop from base to the emitter of the BJT, I_S is the saturation current and V_T is the thermal voltage of the device. Continuing:

$$V_{in} - I_{Ref}R_1 - V_{BE1} = V_{BE2} + I_{Ref}R_M \quad (3.26)$$

$$I_{Ref} = \frac{V_{in} - 2V_T \ln(I_{Ref}/I_S)}{R_1 + R_M} \quad (3.27)$$

The closed form solution to this equation does not exist. It can however be written in terms of the Lambert $\mathcal{W}$ function:

$$I_{Ref} = \frac{2V_T \mathcal{W}\left(\frac{(R_M+R_1)e^{V_{in}/2V_T}}{2V_T/I_S}\right)}{R_M + R_1} \quad (3.28)$$

where Lambert $\mathcal{W}(z)$ defines a function for which any complex pair of numbers z and w satisfy:

$$we^w = z \quad (3.29)$$

note that z is the argument, while w is the value of the function. As a direct relationship between memristance and reference current cannot be found analytically, fitted models are proposed instead. For a narrow range of memristances, such as those used in this work - from $3k\Omega$ to $100k\Omega$ - the expression in equation 3.28 can be approximated to the form:

$$I_{Ref} = Ae^{BR_M} + Ce^{DR_M} \quad (3.30)$$

where A, B, C and D are the fitting constants. Through parameter fitting it was found that $A = 5.786 \times 10^{-5}$, $B = -1.2 \times 10^{-4}$, $C = 7.34 \times 10^{-6}$ and $D = 6.253 \times 10^{-6}$, best represent the

behaviour of the current mirror. However, for an even narrower range of memristances used (up to $33k\Omega$) a simpler approximation holds valid - an inverse square root law:

$$I_{Ref} = \frac{3.7 \times 10^{-3}}{\sqrt{R_M}} - 1.25 \times 10^{-5} \quad (3.31)$$

The measured results along the two fitted functions are shown in Figure 3.7c. LM13700 datasheet [5] asserts that the relationship between the bias current (I_{ABC}) and the transconductance is linear. Following from that, and taking equation 3.31 into consideration, the relationship between memristance and the gyration factor K^2 should be approximately:

$$K^2 \propto \frac{1}{R_M} \quad (3.32)$$

However, because of the additional $\frac{1}{\sqrt{R_M}}$ terms which were neglected, the inverse relationship quickly breaks down even in a limited range of memristances. Empirically it was found (Figure 3.7d) that the gyration factor depends on memristance as follows:

$$K^2 \propto \frac{1}{R_M^{1.5}} \quad (3.33)$$

3.3.2 Non-Ideal Behaviour

Self-Resonance

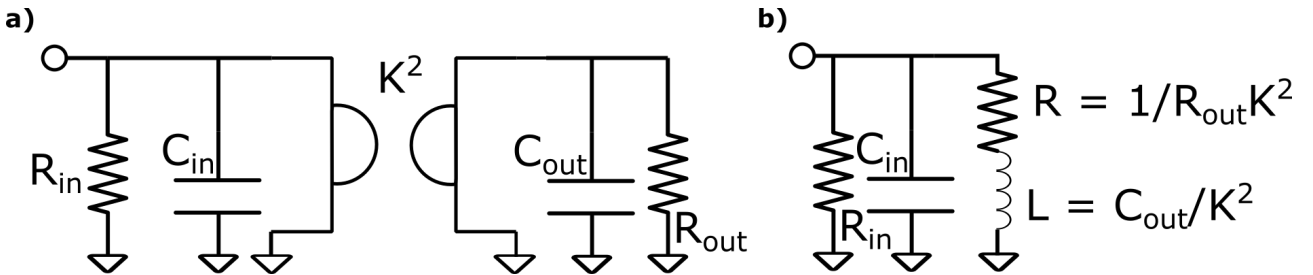


Figure 3.8: Origin of self resonance in gyrator structures. **a)** Simple model of a gyrator incorporating non-ideal input and output characteristics **b)** Equivalent circuit

While on paper the method seems like a *panacea* to all reconfiguration problems, the gyrator-based synthesis does come at a price. Similarly to other theoretical passive elements, a realisation of a gyrator finds its limitation due to physical structure. Comparing to self-resonance of

inductors, gyrators experience a similar phenomenon which is dictated by the input and output capacitances as well as the gyration constant. This means that the bandwidth of the circuit is determined by the delay between input and output of the gyrator, or how quickly it converts voltage to current and vice-versa.

The problem is depicted in Figure 3.8. The output capacitance of the gyrator is turned into an input inductance. Together, the two reactive effects realise an LC tank. The resonant frequency is:

$$L_{in} = \frac{C_{out}}{K^2} \quad (3.34)$$

$$\omega_{tank} = (LC)^{-1/2} \quad (3.35)$$

$$\omega_{tank} = \frac{K^2}{C_{in}C_{out}} \quad (3.36)$$

It is clear that in an ideal gyrator without any capacitive effects the resonant frequency is infinite. Naturally, as those effects are unavoidable, the self-resonance will modulate with memristance as per equation 3.33. What this implies is that as the gyration constant decreases, and the magnitude of the gyrated impedance increases, the useful bandwidth also decreases. This poses a basic limit on the feasible magnitude of the realisable synthetic impedance function. If left uncompensated, it will also lead to disastrous effects when loaded with a physical capacitor in the usual range of few tens of picofarads.

DC Input Resistance

The input and output impedance of the gyrator further limit the low frequency characteristics of the device. The equivalent Laplace domain impedance of the device is a second order function, which at DC becomes:

$$Z_{eq}(s) = \frac{R_{in}R + sR_{in}L}{s^2R_{in}LC_{in} + s(R_{in}RC_{in} + L) + R_{in} + R} \quad (3.37)$$

$$= \frac{R_{in}\frac{1}{R_{out}K^2} + sR_{in}\frac{C_{out}}{K^2}}{s^2R_{in}\frac{C_{out}}{K^2}C_{in} + s(R_{in}\frac{1}{R_{out}K^2}C_{in} + \frac{C_{out}}{K^2}) + R_{in} + \frac{1}{R_{out}K^2}} \quad (3.38)$$

$$\lim_{s \rightarrow 0} Z_{eq}(s) = \frac{R_{in}R}{R_{in} + R} \quad (3.39)$$

$$= \frac{\frac{R_{in}}{R_{out}K^2}}{R_{in} + \frac{1}{R_{out}K^2}} \quad (3.40)$$

Rather unsurprisingly, at DC the circuit reduces to a parallel combination of the input resistance and the gyrated output resistance. In a perfect gyrator both R_{in} and R_{out} would tend to infinity. However, as the values are in fact finite, the resulting input referred resistance is non-zero, resulting in a gyrator defined DC input resistance. Similarly to the resonant frequency, the precise value of the DC input resistance will be defined by the gyration factor of the device.

Quality Factor

The quality factor of the device is a measure of its energy storing capability compared to its energy losses. For capacitors that is the ratio of leakage resistance or equivalent parallel resistance to its true capacitive property. For an inductor quality factor is a ratio of the energy storage as a magnetic field to the heat dissipated through the equivalent series resistance.

The quality factors the input impedance and the input referred output impedance are equal, provided that $C_{in} = C_{out}$ and $R_{in} = R_{out}$. Capacitive quality factor is indeed that same as the referred inductive one.

$$Q_{C_{out}} = \frac{R_{out}}{X_{out}} = \omega C_{out} R_{out} \quad (3.41)$$

$$Q_{L_{ref}} = \frac{\omega L}{R} = \frac{\omega C_{out}}{K^2} / \frac{1}{R_{out} K^2} = \omega C_{out} R_{out} \quad (3.42)$$

$$Q_{L_{ref}} = Q_{C_{out}} \quad (3.43)$$

This however does not imply that the gyration does not affect the quality factor of the circuit. It most certainly does, if the gyrated circuit is treated independently of the output impedance.

Complex Gyration Constant

Due to layout, cross-coupling and unwanted (parasitic) behaviour of most known components, the transconductance of the OTA is in fact complex, not real. Inherent circuit delays, leading to perceived capacitive effects, transform the transconductance, and subsequently the gyration constant into:

$$K = G_m = \frac{1 + sRC_{delay}}{R} \quad (3.44)$$

In the limit, when there are no circuit delays, K clearly reduces to the form shown in equation 3.6. This however leads to frequency dependent gyration factor. Depending on the magnitude

of the capacitive delay, the frequency dependence becomes prominent at MHz or GHz level. For example, on the PCB platform, as it will be demonstrated in subsequent sections, bandwidth limitations stemming from complex gyration constant result in a narrow range of useful frequencies - sub 1MHz. Elementary RC time constant calculation allows to estimate the corner frequency of the gyrator, where $R = 1/\mathcal{R}[K]$ and $C = \mathcal{I}[K]/\omega$.

Stability

Gyrators are designed as negative feedback circuits. Using the model from Figure 3.8a, the poles and damping factor of the circuit are found. The input impedance of the circuit is:

$$Z_{eq} = \frac{R_{in} \frac{1}{R_{out} K^2} + s R_{in} \frac{C_{out}}{K^2}}{s^2 R_{in} \frac{C_{out}}{K^2} C_{in} + s \left(R_{in} \frac{1}{R_{out} K^2} C_{in} + \frac{C_{out}}{K^2} \right) + R_{in} + \frac{1}{R_{out} K^2}} \quad (3.45)$$

$$= \frac{R_{in} R_{out}^{-1} + s R_{in} C_{out}}{s^2 R_{in} C_{out} C_{in} + s (R_{in} R_{out}^{-1} C_{in} + C_{out}) + R_{in} K^2 + R_{out}^{-1}} \quad (3.46)$$

Assuming that input and output conductance are similar ($R_{in} \simeq R_{out}$), this can be simplified to:

$$Z_{eq} = \frac{1 + s R_{in} C_{out}}{s^2 R_{in} C_{out} C_{in} + s (C_{in} + C_{out}) + R_{in} K^2 + R_{out}^{-1}} \quad (3.47)$$

$$= \frac{R_{in}^{-1} + s C_{out}}{s^2 C_{out} C_{in} + s (C_{in} + C_{out}) R_{in}^{-1} + K^2 + R_{out}^{-1} R_{in}^{-1}} \quad (3.48)$$

Since $R_{out, in}$ are generally large ($> 1M\Omega$) and much larger than K^{-1} :

$$Z_{eq} = \frac{R_{in}^{-1} + s C_{out}}{s^2 C_{out} C_{in} + s (C_{in} + C_{out}) R_{in}^{-1} + K^2} \quad (3.49)$$

Hence the poles of the circuit are:

$$p_{1,2} = - \left(\frac{C_{in} + C_{out}}{2 R_{in} C_{in} C_{out}} \pm \frac{\sqrt{(C_{in} + C_{out})^2 - 4 K^2 C_{in} C_{out}}}{2 R_{in} C_{in} C_{out}} \right) \quad (3.50)$$

Therefore the poles of the circuit are located in the left side of the s-plane, meaning the design is stable, however improper damping can still render it unusable. The damping factor (ζ) as well as natural frequency (ω_0) can be deduced by comparing the denominator of the impedance expression to the standard second order circuit:

$$s^2 + 2\omega_0\zeta s + \omega_0^2 = 0 \quad (3.51)$$

Therefore:

$$\omega_0 = \sqrt{\frac{K^2}{C_{in}C_{out}}} \quad (3.52)$$

$$\zeta = \frac{C_{in} + C_{out}}{KR_{in}\sqrt{C_{in}C_{out}}} \quad (3.53)$$

Rather unsurprisingly following the stability analysis, the expression for the self resonant frequency has been derived once again. However, more interestingly the damping factor is a function of the capacitive loading as well as the gyration constant K . Hence, large transconductances can lead to degradation of damping and thus result in transient oscillations. At the same time as capacitive loading C_{out} increases the absolute value of ζ also increases, which seems intuitive as higher capacitor loading will *absorb* or filter any oscillations.

Resonance of Two Gyrator Circuit

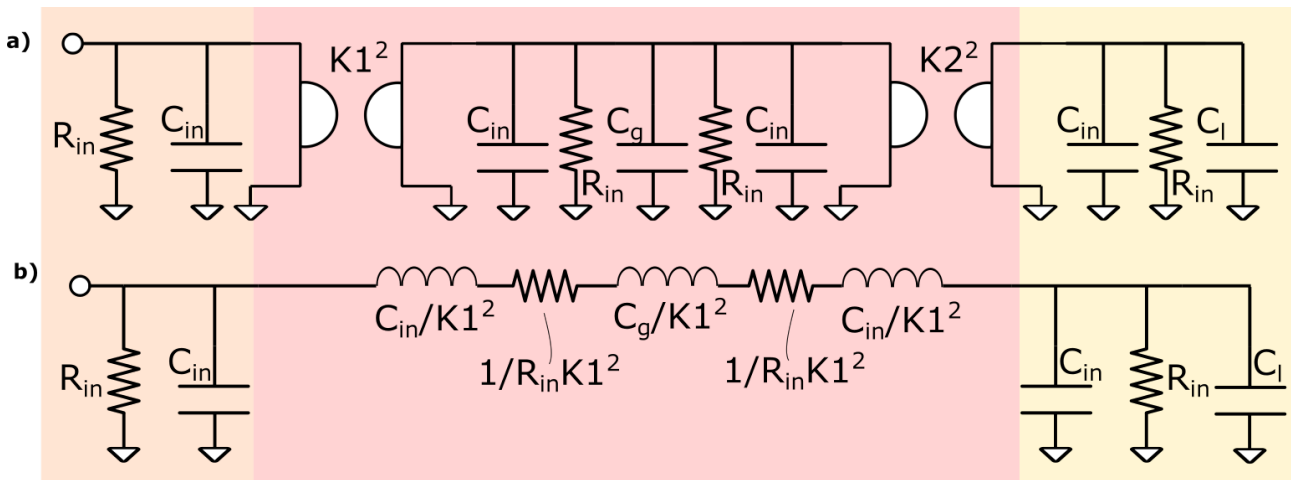


Figure 3.9: **a)** Typical two gyrator LC resonant circuit. **b)** Equivalent gyrator-free circuit assuming $K1 = K2$. The circuit can be further simplified by combining series inductances and resistances.

The above analysis can be applied to 2 gyrator connections. Using simplified notation where $X|Y$ implies that component X is parallel to component Y circuit in Figure 3.9 has an input impedance of:

$$Z_{in} = j\omega C_1 | (R_1 | (j\omega L_1 + R_2 + (j\omega C_2 | R_3))) \quad (3.54)$$

For full analysis of the above equation please refer to Appendix B. Here, just the results of the derivation are presented and discussed.

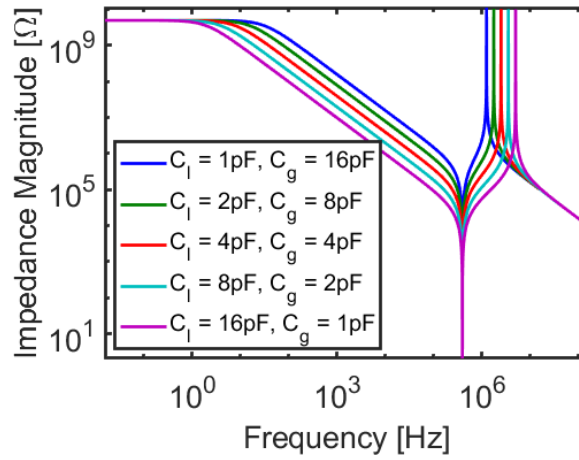


Figure 3.10: Resonance and quality factor of a capacitively loaded two gyrator circuit shown in Figure 3.9 and described by equation B.1. For analysis the following values were assumed: $R_n = 10G\Omega$, $K_1^2 = 100pS^2$, $C_{in} = 100pF$. The first resonant frequency, below 1MHz is attributed to the product of the gyrated capacitance and load capacitance. The second resonant peak is the result of energy exchange between the synthetic inductor and input capacitance. Tuning the parameters allows to tune both resonance's frequency and quality factor. Here however only the first peak is of interest.

In the following analysis the higher frequency resonance is omitted as it is the result of energy exchange between parasitic capacitances and the inductor. One observation is that gyrated and load capacitance come as a products in highest order terms in both numerator and denominator of the impedance function. Therefore the frequency behaviour such as resonant frequency depends on the product of these two capacitances. This enables independent control of the quality factor of the first (lower frequency) resonance as shown in Figure 3.10. The circuit behaves as described by the high level equation B.1. At low frequencies the resistive component dominates. As frequency increases the load capacitance begins to play a bigger role, dropping the measured input impedance, until resonance between C_l and synthetic inductance is reached. As frequency continues to rise the inductive behaviour briefly dominates the response until resonance between the inductor and input capacitance is observed. Following from that C_{in} wholly dominates the response. While the first resonant frequency is determined by the product

of C_l and C_g the quality factor is based on their ratio. It can be seen from the results plotted that even in a lossy gyrator the quality factory of the resonance is very high.

Bandwidth of N-Gyrator Circuit

The above discussion can be further generalised to an N-gyrator circuit. In an unloaded circuit self-resonance is a consequence of gyrated input capacitances. C_{in} at one port forms an LC resonant circuit with C_{in} at the other port. Three cases are considered:

1. Single gyrator circuit (Figure 3.11a)
2. Double gyrator circuit (Figure 3.11b)
3. Triple gyrator circuit (Figure 3.11c)

For simplicity it is assumed all gyrators have the same gyration constant K , and equal input capacitance C_{in} . Moreover, unloaded conditions are assumed, and all elements are referred to the input side (conventionally on the left hand side of the circuits).

Single gyrator circuit: The input capacitance on port 2, is seen as inductance of magnitude $L = K^{-2}C_{in}$, thus forming an LC resonant circuit, with resonant angular frequency:

$$\omega_1 = \frac{1}{\sqrt{CL}} = \frac{K}{C_{in}} \quad (3.55)$$

Double gyrator circuit: In this case the input capacitance of gyrator 1 port 2 adds to the input capacitance of gyrator 2 port 1. Solving the circuit backwards, output gyrator is first resolved resulting in a single gyrator circuit with a series LC load. Resolving this circuit yields a classic Pi-filter (C1-L-C2), with $C_1 = C_2 = C_{in}$ and $L = 2K^{-2}C_{in}$. The resonant angular frequency of the Pi-filter is:

$$\omega_2 = \frac{1}{\sqrt{L \frac{C_1 C_2}{C_1 + C_2}}} = \frac{\sqrt{K^2}}{\sqrt{2C_{in} \frac{C_{in}^2}{2C_{in}}}} = \frac{K}{C_{in}} = \omega_1 \quad (3.56)$$

Triple gyrator circuit: Following the same logic three input capacitances in the centre of the network are summed. The other two gyrators contribute two inductances parallel to the $3C_{in}$ capacitor, $L_1 = L_2 = K^{-2}C_{in}$, forming effectively an inductor $L_{1|2} = L_1 || L_2 = K^{-2}C_{in}/2$.

The LC network is then gyrated to the side of the gyrator 1 port 1 to form yet again a Pi-filter (C-L-C) with $C_1 = C_{in}$, $L = 3K^{-2}C_{in}$, $C_2 = C_{in}/2$. The resonant angular frequency of this Pi-filter becomes:

$$\omega_3 = \frac{1}{\sqrt{L \frac{C_1 C_2}{C_1 + C_2}}} = \frac{\sqrt{K^2}}{\sqrt{3C_{in} \frac{0.5C_{in}^2}{1.5C_{in}}}} = \frac{K}{C_{in}} = \omega_2 = \omega_1 \quad (3.57)$$

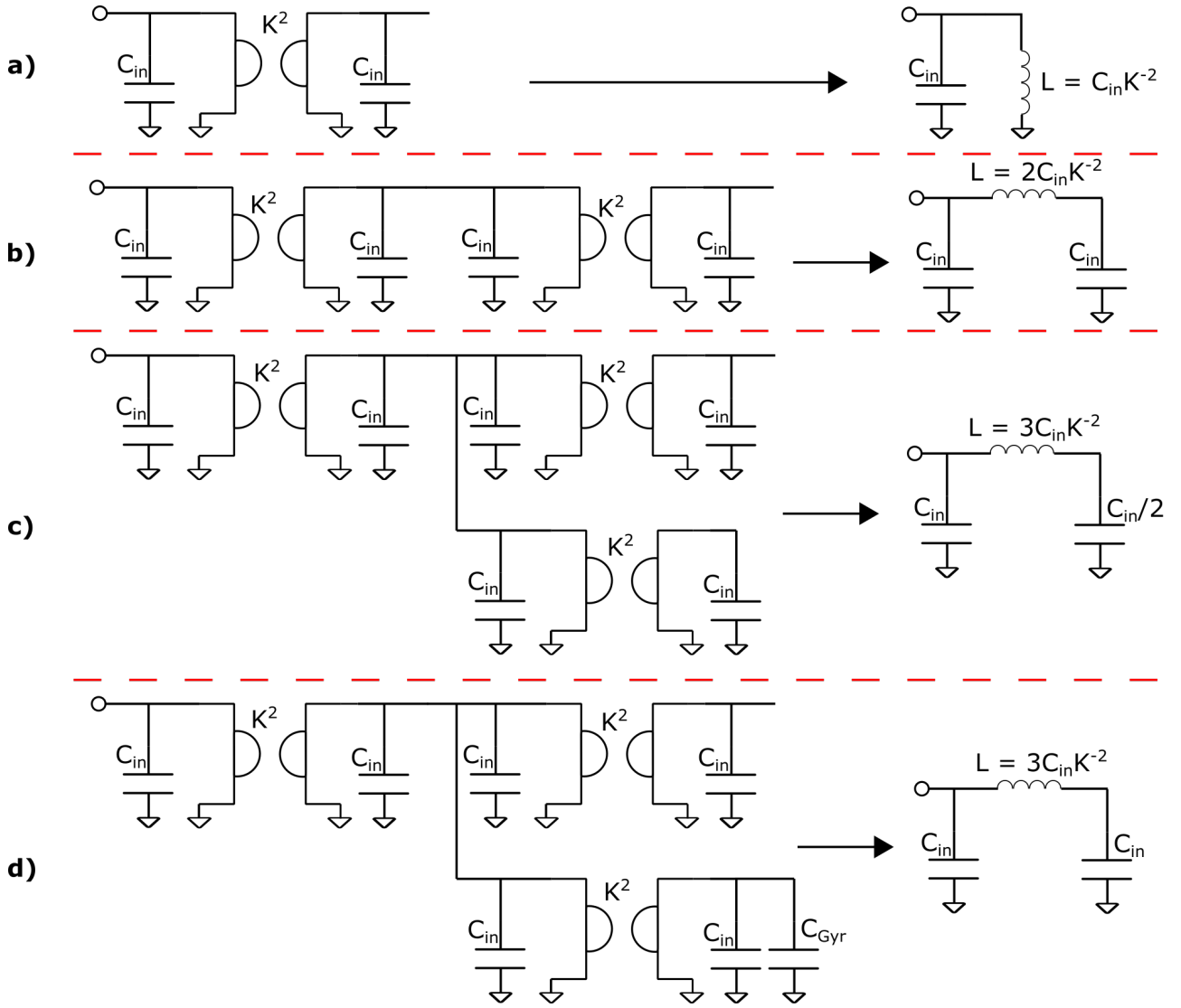


Figure 3.11: Self-Resonance of Gyrators - 4 cases which exemplify the problem of reduced bandwidth in gyrator-rich circuits. **a)** Single gyrator network and its LC equivalent. **b)** Double gyrator network and its CLC Pi filter equivalent. **c)** Triple star connected gyrator network and its CLC Pi filter equivalent. **d)** The same triple star connected gyrator network with capacitive load and its CLC Pi filter equivalent.

This can be further generalised to N -star connected and unloaded gyrators. Such configuration will always result in a Pi filter. The general values of the components become $C_1 = C_{in}$, $L = NK^{-2}C_{in}$, $C_2 = C_{in}/(N - 1)$. It can be seen that all Pi filters resulting from connecting N -gyrators in a star configuration yield a resonant frequency of $\frac{K}{C_{in}}$.

More interestingly though, taking the limit $N \rightarrow \infty$, the C-L-C Pi network reduces to just a single grounded capacitor C_{in} , effectively eliminating any resonance, since synthetic inductor becomes approximately an open circuit. Furthermore, increasing N increases the quality factor of the resonant network, in the limit yielding infinite quality factor. Thus it would seem that adding more gyrators in a star configuration should improve the bandwidth. This would be the case if it weren't for some parasitic series resistances and indeed capacitive loads.

However to understand where the reduction in bandwidth arises from, circuit loading needs to be considered, i.e. C_{Gyr} in Figure 3.11d, as well as internal delays of the gyrator. Assuming C_{Gyr} is much larger than C_{in} ¹, the bottom gyrator forms an inductor of magnitude $L_1 = K^{-2}C_{Gyr}$ in parallel with equivalent capacitance of $3C_{in}$ and another inductor $L_2 = K^{-2}C_{in}$. Since L_1 appears in parallel to L_2 and is much larger than L_2 , its effect is negligible, and thus the circuit simplifies to just $C = 3C_{in}$ in parallel with L_2 . This in turn when referred to the input of the first gyrator forms the standard Pi-filter with values of $C_1 = C_{in}$, $L = 3K^2C_{in}$ and $C_2 = C_{in}$. Note that the second capacitor is now twice as big as it was in plot c. This effectively scales the resonant frequency by a factor of $\sqrt{(2/3)}$, i.e. it reduces it.

The picture becomes complete when internal delays of the gyrator are accounted for, i.e. the gyration factor is assumed complex (equation 3.44). The gyration resistance decreases as a function of frequency therefore, conductance is expected to increase:

$$R_{Gyr}(j\omega) = |R| \frac{1}{1 + j\omega T} \quad (3.58)$$

$$K(j\omega) = |K|(1 + j\omega T) \quad (3.59)$$

where $-1/T$ is the pole of the OTA. Accounting for the OTA delay, and once again computing the behaviour of the single gyrator circuit an LC network is realised, where $C = C_{in}$ and $L = K(j\omega)^{-2}C_{in}$. Then resonance and hence the bandwidth are defined as:

$$\left| \frac{1}{j\omega C_{in}} \right| = |\omega K(j\omega)^{-2}C_{in}| \quad (3.60)$$

$$\frac{1}{\omega C_{in}} = \omega C_{in} |K|^{-2} \frac{1}{1 + (\omega T)^2} \quad (3.61)$$

$$1 + (\omega T)^2 = \omega^2 C_{in}^2 |K|^{-2} \quad (3.62)$$

$$\omega^2 (|K|^{-2} C_{in}^2 - T^2) = 1 \quad (3.63)$$

$$\omega = \frac{1}{\sqrt{|K|^{-2} C_{in}^2 - T^2}} \quad (3.64)$$

For an ideal OTA, without any delays the pole frequency is at infinity: $1/T \rightarrow \infty$, that is $T \rightarrow 0$. In this case the network simplifies to a standard LC resonant circuit. However, any delay of the OTA reduces the useful bandwidth of the circuit. In general the more transconductors there are in the network the larger the effect of the delay and hence we observe a decreased bandwidth of the circuit. This can be better seen by allowing:

¹It is the case for the PCB realisation. Input capacitance is quoted as 5pF while the gyrated capacitance is very large - 10nF.

$$\omega_{Res} = \frac{|K|}{C_{in}} \quad (3.65)$$

$$\omega_{Delay} = \frac{1}{T} \quad (3.66)$$

$$\text{therefore : } \omega = \frac{1}{\sqrt{\left| \frac{1}{\omega_{Res}^2} - \frac{1}{\omega_{Delay}^2} \right|}} \quad (3.67)$$

$$\omega = \frac{\omega_{Res}\omega_{Delay}}{\sqrt{|\omega_{Delay}^2 - \omega_{Res}^2|}} \quad (3.68)$$

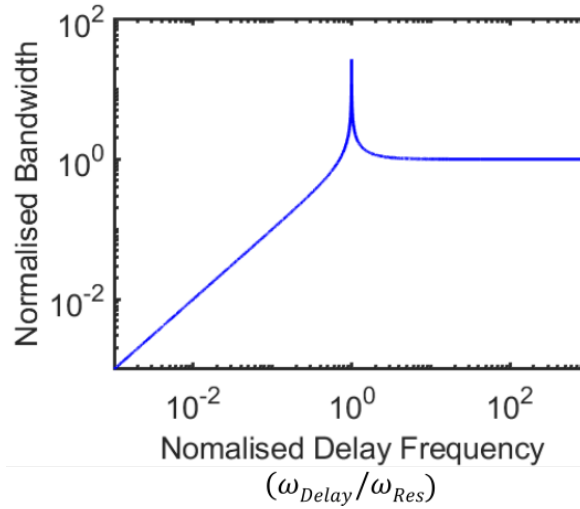


Figure 3.12: Effect of self-resonance and single pole delay onto gyrator bandwidth. Values are normalised with respect to the self-resonant frequency.

By normalising the function to the value of ω_{Res} the characteristic presented in Figure 3.12 is realised. Clearly when the single pole dominates the response, i.e. when the delay frequency is smaller than the theoretical self-resonant frequency, the bandwidth is limited by the pole, as expected. When the pole is located beyond the resonant frequency, it is the ω_{Res} that limits the performance. Interestingly, when the two frequencies are close to one another, it is theoretically possible to enhance the bandwidth beyond the two limiting values. In practice it is expected that the realised circuit will be highly unstable and furthermore will require immense power to support the bandwidth.

Process Dependence

More insight into the behaviour described above is gained by examining the simplest case: single transistor transconductor. An N-channel common source MOSFET acts as a transconductance amplifier. In saturation the output (drain) current and therefore the transconductance are:

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{Th})^2 (1 + \lambda V_{DS}) \quad (3.69)$$

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{2I_D}{V_{GS} - V_{Th}} \quad (3.70)$$

where W and L are the FET gate dimensions, and μ_n and C_{ox} are process dependent parameters representing electron mobility and oxide capacitance. V_{GS} represents the voltage applied to the gate of the FET, V_{Th} is the device threshold voltage, V_{DS} is the resulting voltage at the output of the transconductor, while λ models short channel imperfections.

The low pass behaviour of FET transistors is dominated by the pole frequency arising from gate capacitance and channel transconductance:

$$\omega_{FET} \simeq \frac{g_m}{C_g} \quad (3.71)$$

The commonly adopted approximation for gate capacitance in saturation region, particularly more accurate in older technologies is [6]:

$$C_g = \frac{2}{3} W L C_{ox} \quad (3.72)$$

This is approximately true around the point where output voltage equals the overdrive voltage of the transistor ($V_{GS} - V_{Th}$). As a consequence the pole frequency of the transistor becomes:

$$\omega_{FET} \simeq \frac{\frac{2I_D}{V_{GS}-V_{Th}}}{\frac{2}{3} W L C_{ox}} \quad (3.73)$$

$$= \frac{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{Th}) (1 + \lambda V_{DS})}{\frac{2}{3} W L C_{ox}} \quad (3.74)$$

$$= \frac{3}{2} \frac{\mu_n}{L^2} (V_{GS} - V_{Th}) (1 + \lambda V_{DS}) \quad (3.75)$$

Hence the pole of the simple OTA becomes:

$$T = \frac{1}{\omega_{FET}} \quad (3.76)$$

Gyrators cannot however be analysed solely based on the individual characteristics of the transconductors. The joint effects need to be quantified, such as effective transconductance due to additional network and input/output capacitance due to connected devices. Neglecting the joint effects calculations quickly prove that bandwidth of such a gyrator would be infinite, requiring infinite power:

$$\omega_{BW} = \frac{1}{\sqrt{|g_m^{-2}C_g^2 - \frac{1}{\omega_{FET}^2}|}} \quad (3.77)$$

$$= \frac{1}{\sqrt{|\left(\frac{2/3WLC_{ox}}{\mu_n C_{ox} \frac{W}{L}(V_{GS}-V_{Th})(1+\lambda V_{DS})}\right)^2 - \left(\frac{2L^2}{3\mu_n(V_{GS}-V_{Th})(1+\lambda V_{DS})}\right)^2|}} \quad (3.78)$$

$$= \frac{1}{0} \rightarrow \infty \quad (3.79)$$

Allowing the transconductance to remain unaffected, capacitive effects have to be accounted for. Input capacitance of the complete gyrator is *at least* the sum of gate capacitance of the forward transconductor and the drain capacitance of the feedback one. Hence [7]:

$$C_{in} = C_g + C_d \quad (3.80)$$

$$C_{in} = \frac{2}{3}WLC_{ox} + WL_{diff}C_j + (2L_{diff} + W)C_{jsw} \quad (3.81)$$

where L_{diff} defines the diffusion length of a MOSFET, C_j is the junction capacitance of the bottom (substrate) wall and C_{jsw} is the junction capacitance due to side walls. Overall, they act to increase the input capacitance of the gyrator structure:

$$\omega_{Res} \propto C_{in}^{-1} \quad (3.82)$$

Therefore as input capacitance increases, the resonant frequency decreases, meaning that the delay frequency of the MOSFET is larger than the self-resonant frequency. Depending on the ratio of the two this can in theory lead to slightly increased bandwidth as shown in Figure 3.12. The input capacitance in equation 3.81 is the smallest possible value, when just two FETs are used. In practice it is impossible to realise a gyrator with just two devices and hence the input capacitance is expected to be bigger, as the output node will be loaded with additional devices. In addition, as a recommendation for future work, it may be beneficial to extend the order of the model by incorporating delays in carrier transfer and well as delays due to channel filling of the individual FET transistors.

Memristor Fluctuation Sensitivity

In this work, the precise value of memristance dictated the magnitude of transconductance of the gyrators. For this reason sensitivity to memristive fluctuations must be as per equation 3.33:

$$K^2 = A \times R_M^{-1.5} + B \quad (3.83)$$

where A and B are constants dependent on the biasing of the OTAs. Hence sensitivity is:

$$S_{R_M}^{K^2} = \frac{R_M}{K^2} \frac{\partial K^2}{\partial R_M} \quad (3.84)$$

$$= -1.5A \frac{R_M}{K^2} R_M^{-2.5} \quad (3.85)$$

$$= -1.5A \frac{R_M^{-1.5}}{K^2} \quad (3.86)$$

Through least squares fit of the linear trend, the value of A is estimated to be around 3.04×10^{-12} S²/Ω:

$$S_{R_M}^{K^2} \simeq \frac{4.56 \times 10^{-12}}{R_M^{1.5} K^2}. \quad (3.87)$$

3.4 Memristor-Tuned Inductor

3.4.1 Measurement Setup and Procedure

Setup

Memristor-enabled inductor measurements were performed at UoS. The setup consisted of: standalone memristor array, probe station, Wentworth probe card, DC power supply unit (PSU), Arc One programmer, a PC running Arc One GUI, Keysight 200MHz oscilloscope, test PCB and temperature/humidity meters (Figure 3.13).

The wafer with memristor array was positioned on the probe station with a vacuum table. A custom probe card interfacing between the memristor array and outside electronics was then

aligned with the wafer. The exact positioning and quality of contact with the electrodes was examined through a digital microscope embedded into the probe station. Wires connected to the probe card were then connected either to the PCB under test or ArC One. The PCB was powered externally through a $\pm 15V$ DC supply. Data from the PCB was acquired through an oscilloscope connected to the test points mounted on the board. Data from ArC One was gathered through the GUI installed on a PC. Finally, additional temperature and humidity data was acquired through a handheld digital meter.

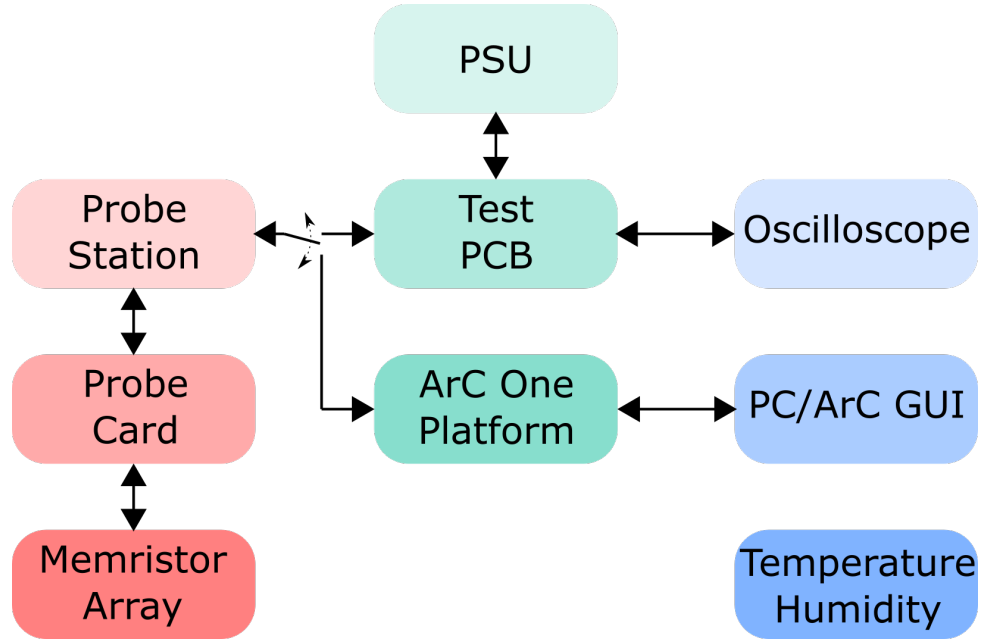


Figure 3.13: Measurement setup used for both inductive and capacitive tests. Chart shows interconnect between individual blocks. Arc One and PCB were interchangeably connected depending on the type of measurement undertaken.

ArC One

ArC One is platform based on the research of Berdan [8], [9]. The platform allows to easily interface up to 1024 individual memristors, perform whole characterisation of the device (IV measurement, polarity, sensitivity, retention) and it allows to form and program the devices into desired level. The platform can measure memristances from tens of Ohms up to few $M\Omega$. All of the memristor handling outside of the PCB environment was performed through ArC One.

When using a full crossbar array of memristors ArC One implements sneak path mitigation techniques, to ensure minimal distortion to other elements. In the following tests a standalone array was used, i.e. each device was independent (32 individual devices on a 32 by 32 array). Therefore sneak paths were not of a concern to the performance of the devices.

Acquired Data

To measure inductance (Figure 3.15a) an RL circuit was constructed, with grounded resistor, as to make full use of both terminals for the synthetic inductor. The transfer function across the inductor was measured using the built-in frequency response analysis (FRA) function on the oscilloscope. This later allowed to fit a model and extract the synthesised inductance. 0.5V was selected as an input amplitude, as higher values led to gyrator saturation and therefore data invalidation.

On the memristor side, a characteristic subthreshold current-voltage relationship was measured. By supplying a predefined train of pulses (varying in amplitude from -0.5V to 0.5V in 0.05V steps, repeated three times over), ArC One measured current through the device. Additionally, retention tests were performed to assess temporal stability of the device under test, by reading out the value of the memristance at regular intervals (every second), with a fixed amplitude subthreshold pulse (0.2V) for a predefined duration (2 or 5 minutes). Finally, programming data (over-threshold pulses and resulting memristance) was extracted to assess the exact state of the device. ArC One has a built-in programming option, whereby target resistance is provided and limiting parameters for the programming pulses are input. For most tests voltage pulses ranging from 4 to 10V and their width ranged from 100ns to 100 μ s. Each combination of pulse width and amplitude was used 10 times. The automatic programmer stopped when the measured memristance was within 10% of the target value.

Ambient data (temperature and humidity) was also recorded to ensure that all measurements are taken in similar conditions, as they play pivotal role in device behaviour [10].

Procedure

The following general decision tree was implemented for the tests (Figure 3.14). Due to the sometimes unpredictable and highly experimental nature of the devices tests often had to be interrupted or restarted. The main reasons were: subthreshold drift, relaxation of the device, damage due to mechanically induced charge (triboelectric effect), electrostatic 'zapping' (ESD) of the devices, or simply random behaviour. When the device characteristics varied between or during the test, the device was cycled - its memristance was increased over tenfold and decreased, as to promote a new CF growth inside the device. If multiple cycling operations proved unsuccessful, a new device was selected.

A single test, therefore, consisted of a single measurement of temperature and humidity, 3 sets of IV measurements, 2 sets of retention data, 4 memristor voltage values and two sets of FRA data.

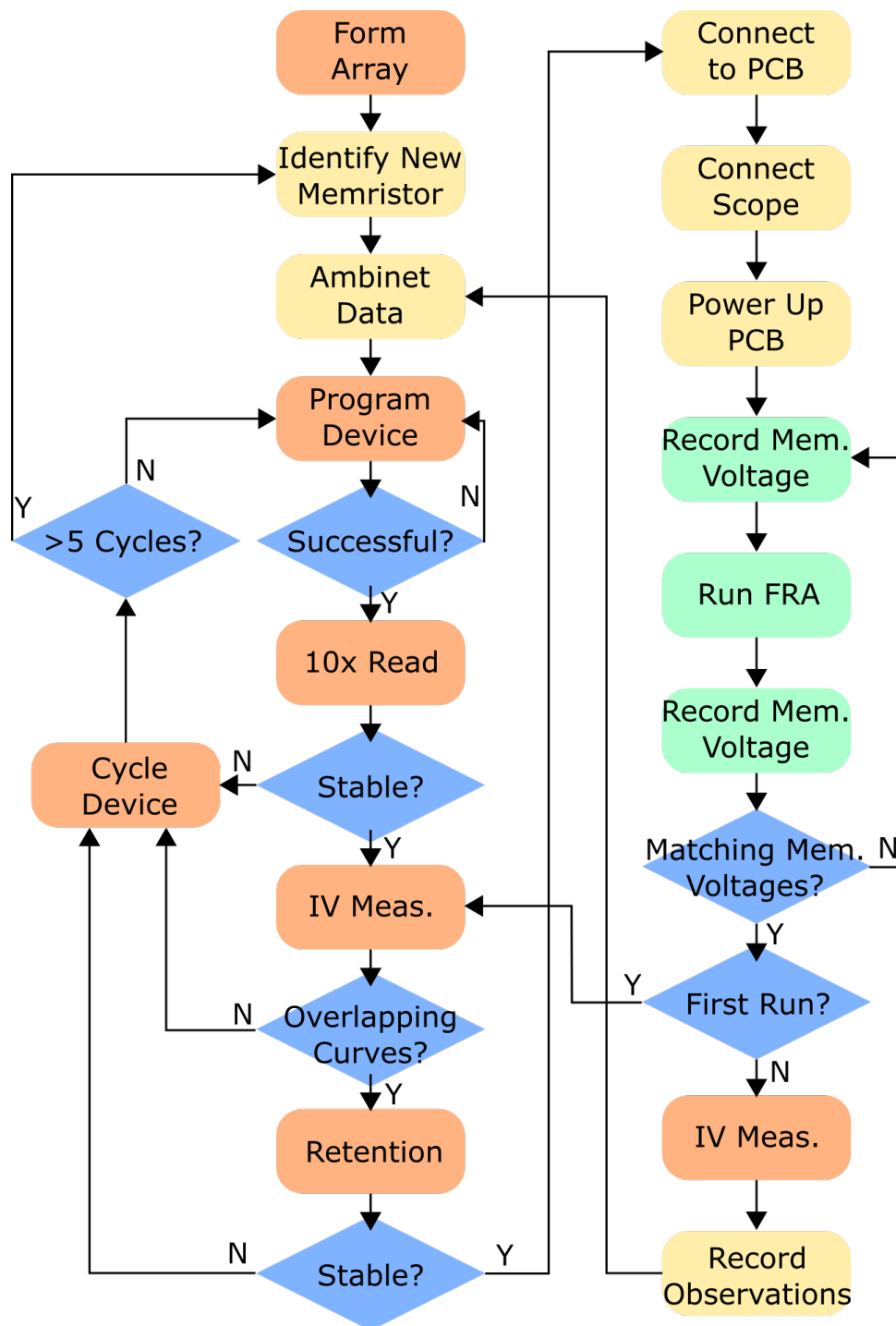


Figure 3.14: Procedural decision tree for building blocks tests. Orange blocks refer to ArC One related activities, blue are decision blocks, green relate to oscilloscope and yellow are miscellaneous.

3.4.2 Model Fitting

The FRA results were used to estimate 5 unknown parameters in the RL circuit: inductance, ESR, load resistance and both gyration factors. The parameter fit was represented as a minimisation problem taking difference between measured values and the model as the objective function. A heuristic search approach, using Nelder-Mead simplex algorithm (see Appendix A) was used to find the local minimum of the objective function - J :

$$J(R_{ESR}, L, R_L) = |V_{in} \frac{R_L}{R_L + R_{ESR} + sL} - V_{Meas}| \quad (3.88)$$

Despite knowing the true load resistance used, its value was also estimated using the simplex algorithm. This in turn allowed to estimate the gyration constants and increased the confidence in the minimisation results (if resulting load resistance in fact matched true value used). The initial starting point for the algorithm was provided using previously estimated values, when tested with resistors instead of memristors.

The model represents an ideal scenario and doesn't account for higher order modes and distortions (e.g. complex gyration constant), as true inductive properties are being examined. Therefore as results will show, the model breaks down at high frequencies.

3.4.3 Results

The following results were gathered using $1nF$ gyrated capacitor and a load resistor of $10k\Omega \pm 1\%$. A memristor with cross-sectional area of $40\mu m \times 40\mu m$ was tuned into the following (approximate) resistive levels: $4.1k\Omega$, $6.6k\Omega$, $9.5k\Omega$, $11.8k\Omega$, $14.8k\Omega$ and $23.2k\Omega$.

Frequency Response Data

FRA data - Bode Plot - is shown in Figure 3.16a-b. The data was filtered once to remove high frequency artifacts and to extract global trends. In plot **a** an arrow was drawn to indicate progression of curves as memristance was tuned. Since the circuit was setup as a low pass filter, increasing the memristance, reduces the gyration factor (equation 3.6), which in turn increases the synthetic inductance (equation 3.21). As the inductance of the RL circuit increases, the corner frequency decreases: $\omega_c = R/L$. And as is the case in first order low pass filters, the phase ought to decrease from 0 to $-\pi/2$ radians.

First indications that the circuit behaviour deviates from the expected results can be seen in the FRA data. Near 1 MHz the gain of the circuit levels off and in some cases begins to rise.

Simultaneously, the phase response keeps decreasing beyond the expected value, indicating that the circuit is more complex than the model presented. In fact if the synthetic inductor is modelled as depicted in Figure 3.15b, the data matches theory. Comparably large input and output capacitance (few pF according to datasheets) bring the phase to $-\pi$ radians, while the coupling RC network shorts the inductor at higher frequencies resulting in the rise in both gain and phase. On the PCB the wide tracks often running parallel to one another resulted in significant cross-coupling - estimated in the excess of $100fF$.

These artifacts can be significantly reduced with custom application specific integrated circuit (ASIC) design, using the appropriate technology, such as TSMC 180nm (see Appendix C). Input capacitances as small as few femto-farads are possible, while careful layout may reduce the coupling capacitance and increase the coupling resistance.

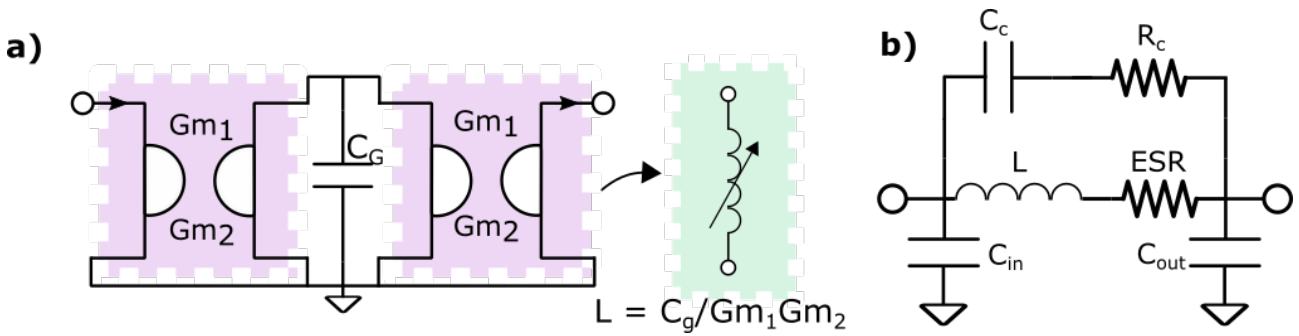


Figure 3.15: Circuit and model of the synthetic inductor. **a)** Physical circuit, showing two variable gyrators and a fixed grounded capacitor. **b)** Higher order model of the synthetic inductance. It is inclusive of input and output capacitances as well as coupling capacitor and resistor.

Using the simplex algorithm and the first order model of the circuit inductance, ESR and load resistance were extracted from the data (Figure 3.16d-f). Mean inductance at low frequencies was then plotted against setting memristance (plot c). Control data was acquired with resistors to ensure correct memristive readout through ArC One. The data estimated through NM algorithm shows close matching between load resistance and its approximated value. Moreover, contrary to both inductance and ESR, load resistance remains constant at all memristive settings, which gives further confidence in the optimal parameter fit of the simplex algorithm. Allowance was made for 1% tolerance on the used load resistor, that is to say a $10k\Omega$ resistor may in fact be $10.1k\Omega$. Then the estimated value of $10.25k\Omega$ deviates from the nominal load by 150Ω . This can be attributed to two factors: simplex local minimum has not been reached or there was a slight mismatch between the input and output gyration constants (plot h). While it is not possible to determine the contribution of each, it is assumed that gyration mismatch is the primary reason for the increase in measured load resistance.

Looking at the inductance curves in plot d, it is noticeable that at lower synthetic values and at lower frequencies the inductance appears to be rising with frequency. This is an artifact of the measurement, as at low frequencies and inductances, FRA is dominated by real values.

Precision of the measurement limits the accuracy of the data estimation. Clearly, as inductance rises or as frequency rises, the magnitude of the imaginary part increases allowing more accurate estimation.

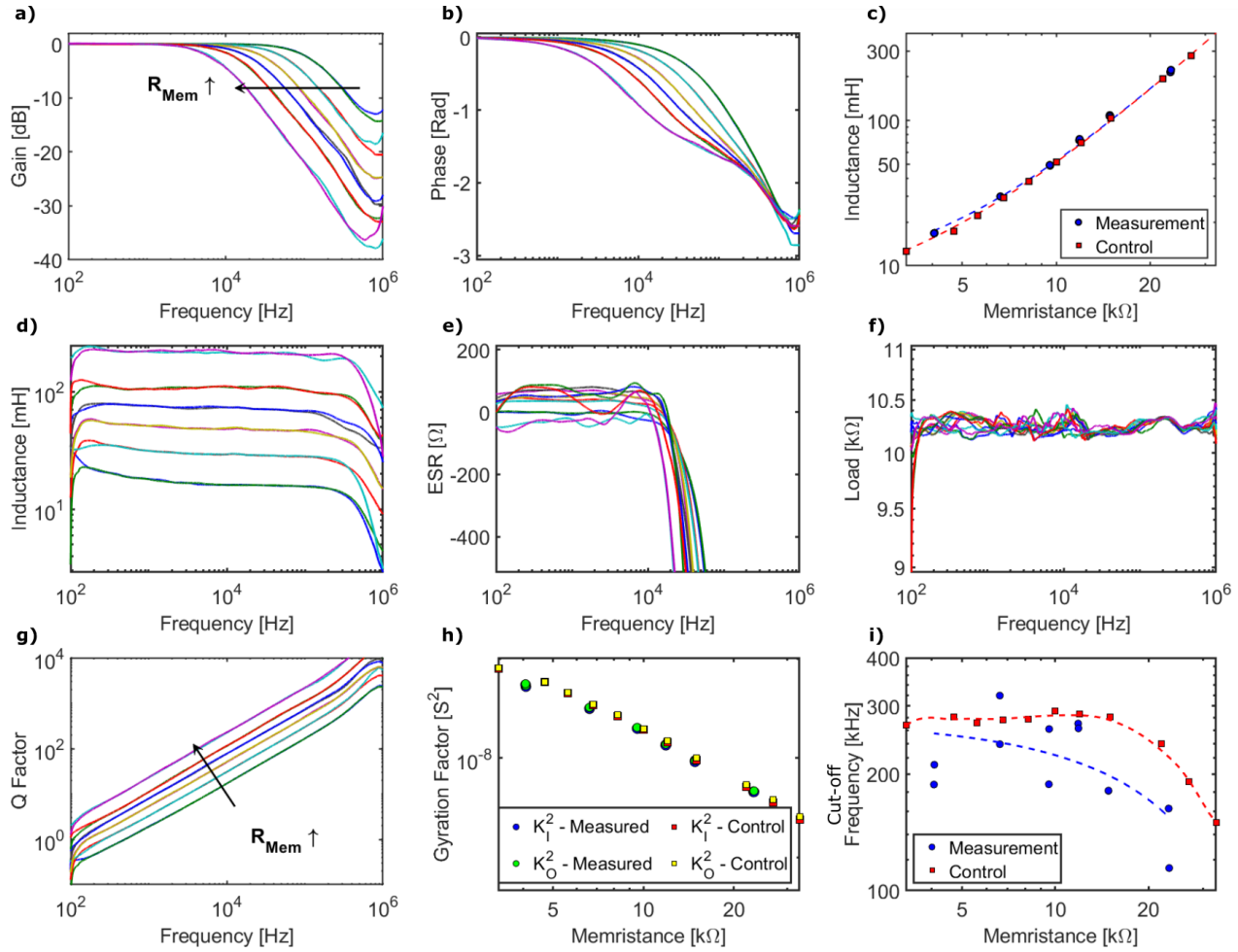


Figure 3.16: Memristor reconfigured synthetic inductor. **a)** Filtered magnitude response of the FRA for all 12 tests. **b)** Filtered phase response of the FRA for all 12 tests. **c)** Memristor controlled synthetic inductance. Blue points represent results acquired with memristors. For confirmation, a second set of results was gathered using similarly valued resistors, shown as red data points. **d)** Inductance as function of frequency - data extracted using simplex minimisation algorithm. **e)** Extracted ESR of the inductor, showing that the simple model of series inductor and resistor breaks down beyond 10kHz , resulting in negative resistance. This could be improved with the use of more complex model shown in Figure 3.15b **f)** Extracted load resistance of the RL circuit, showing close matching with nominal value of $10\text{k}\Omega$. **g)** Extrapolating low frequency ESR of the inductor, its quality factor is shown as function of frequency. **h)** Dependence of the input and output gyration factors - K_I^2 and K_O^2 - on the memristive setting. Plot shows data acquired with memristors and resistors for comparison. **i)** Estimated bandwidth of the synthetic inductor. Measurements with memristors suffered a much lower signal to noise ratio, as the connection to memristors required nearly 1m long leads.

Results of the ESR, however, further confirm that the simple model doesn't hold at higher frequencies. Due to LC mixing and the s^2 term, the data analysis resolved the resulting negative component as equivalent series resistance. However, by extrapolating the low frequency data,

it can be assumed that the ESR remains constant at higher frequencies.

The above poses an interesting question: whether it is reasonable to assume that ESR remains fixed (choose the more complex model), or to effectively allow negative resistance and treat it as an ideal inductor (simple model). On one hand, by choosing the complex model, deeper appreciation of the parasitic behaviour is gained allowing to mitigate it in future realisations. On the other hand, the purpose of this block is to simulate inductance. The circuit should therefore be assessed based on its ability to do so, by fitting its parameters into the ideal inductor model.

The two models therefore play different roles: the ideal model is a practical approach, allowing to assess circuits suitability for a given application; the complex model is a simulation-centric approach allowing to improve the behaviour of the ideal model.

Performance Metrics

As expected, and given the dependence of the gyration constant on memristance 3.6, inductance varies approximately proportionally to $R_M^{1.5}$ (Figure 3.16c). Data acquired with resistors in place of memristors confirmed, that the memristive setting was correctly recorded through ArC One platform. In order to eliminate any suspicion of drift, each measurement was repeated twice. Close overlap between each set of points was observed, showing minimal drift of the memristor in-between and during tests. Care was taken to correctly protect the PCBs from ESD and triboelectric effects, by star grounding everything on the mains safety ground.

An average ESR was calculated by extrapolation, since some values were negative (assumed due to simplicity of the model used, rather than due to resonance or amplification). Overall the low frequency distribution of estimated series resistance spanned the range from -30Ω to 80Ω , with an average of 60Ω . The average ESR value was then used to estimate the quality factor of the device (Figure 3.16g). The values match and exceed those of standard ferrite leaded inductors. A typical off-the-shelf $100mH$ inductor will have around 420Ω of ESR and its quality factor (Q) will peak at 15 (at 10kHz). Using capacitors with inherently higher quality factors and gyrating them yields Q from 16.8 (17.5mH at 10kHz) to 230 (240mH at 10kHz).

Large wire-wound inductors outperform even larger PCB-based ($5.5cm \times 2.5cm$) synthetic inductor realised here. However the concept presented, easily scales down to CMOS ASIC levels, where a similar function can be performed using a fraction of the area. It is estimated that inductors 6 times larger than similarly sized CMOS coils can be realised in silicon.

The slight mismatch between nominal and measured load resistance has been attributed to the mismatch in gyration constants (Figure 3.16h). However the extra 150Ω represents only a 1.5% change. The calculated gyration factors therefore overlap one another quite closely.

Finally, a circuit's bandwidth was acquired by estimating the frequency at which the inductance begins to drop, i.e. point when the second derivative with respect to the frequency is minimised. This point is associated with the drop in phase the device introduces from $-\pi/2$ to $-\pi/4$. The results are presented in Figure 3.16i. The control measurements, acquired with resistors show a clear trend. This however wasn't reproduced with memristors due to an increase in noise of the bias network. Memristors were interfaced through two nearly 1m long connections - from probe card, through to external connectors. Wires were twisted, where it was possible, however measurement quality still appeared to suffer as a consequence. A best fit quadratic function was estimated, showing similar trend to that of the control values. As memristance increased, the synthetic inductance also increased, reducing the useful bandwidth from 300kHz (at $5k\Omega$) to 180kHz (at $30k\Omega$).

Reduction in bandwidth is a consequence of the gyrator's complex model parasitics. As inductance increases, capacitive effects become more prominent at lower and lower frequencies, either routing the input signal to ground or coupling it straight to the output. Furthermore, a hard limit imposed by the self-resonance effect, is reduced as memristance increases, which further imposes restrictions on the bandwidth of the input signal.

Memristor Data

A single memristor was used for this test - it was neither damaged during operation nor during characterisation. For each setting, three IV measurements were performed. They allowed to calculate the resistance-voltage relationship (Figure 3.17a). For each test the three curves are plotted - a good indication that the memristor remains unchanged is a perfect overlap of all three curves, as demonstrated here. Furthermore, for each test the voltage across the memristor was measured to pinpoint the exact value of the memristance used in the test. These points are plotted on top of the curves. The problem discussed earlier, resulting in a complex Lambert function behaviour (equation 3.28), is illustrated here. As memristor is programmed into higher resistive level, the voltage across it increases, increasing the read out voltage, thus reducing the static memristance (with respect to its 0V value).

Automatic programming through ArC One is also demonstrated illustrating technological difficulties with memristors. In some cases the automatic programming was smooth resulting in fast convergence to the desired value (plots d&e). Sometimes the device was resilient to state changes, confusing ArC One with regards to the switching polarity of the device. That is the threshold of the device appeared to increase from one resistive level to another. In other cases, e.g. that shown in plot f, the device could not be programmed with standard programming protocol. A single pulse of reverse polarity was used to cycle the device, allowing the device to be successfully programmed.

The memristance retention data acquired was converted into inductance using the measured

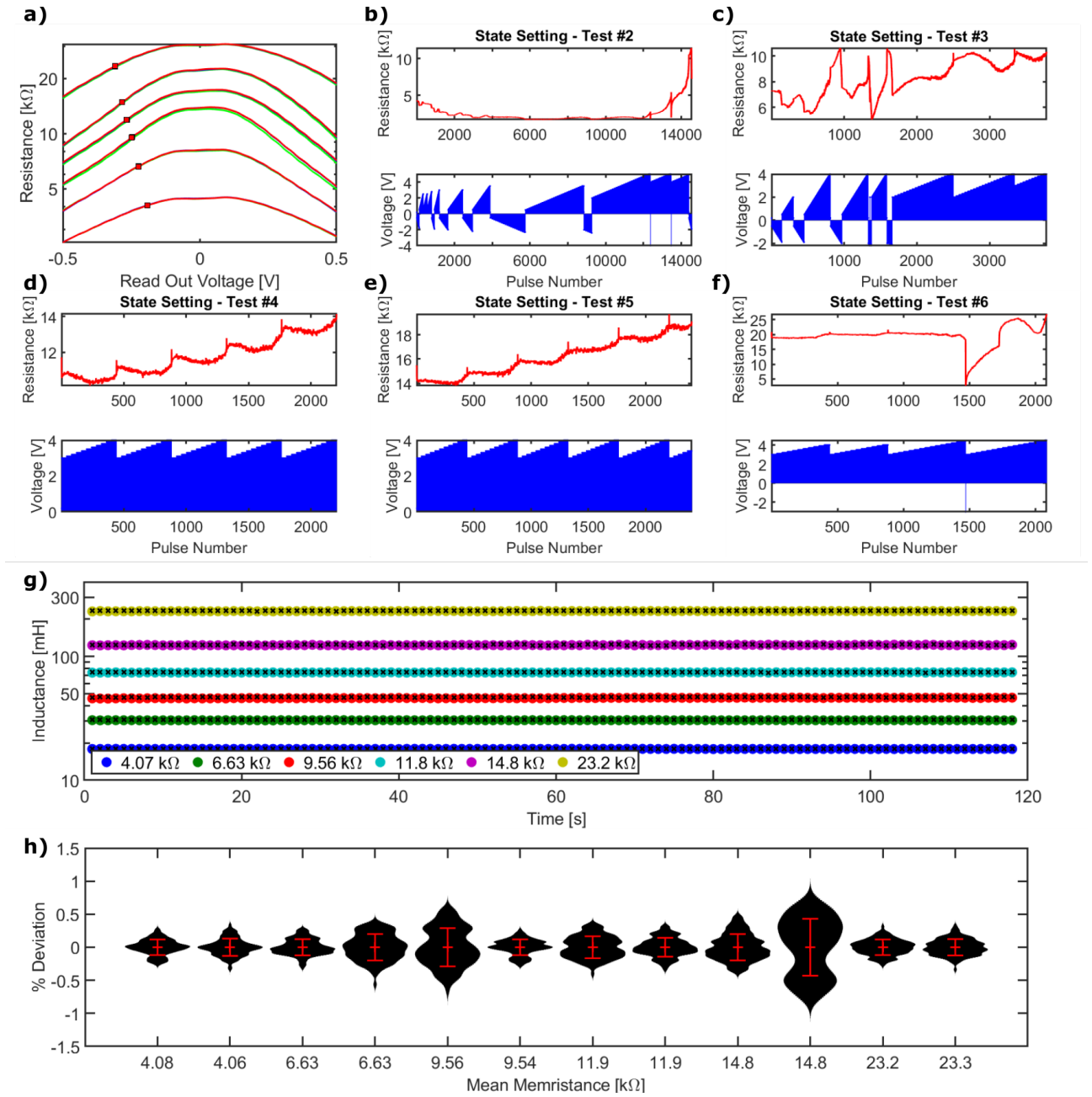


Figure 3.17: Memristor performance during inductive synthesis. **a)** Resistance-voltage curves resulting from the IV measurements. For each group of three measurements, the loading point is indicated. Loading point represent the voltage at which the given memristor was operated, yielding its static resistance during that test. **b) - f)** Results of the automatic memristor programming. In some cases automatic programming was smooth (e.g. d or e). In other, ArC One struggled to identify switching polarity, which resulted in messy-looking graphs. For each test, red trace shows the progression of the resistance, while blue trace shows the applied programming pulses. **g)** Inductive retention over 2 minutes. **h)** Distribution of memristance for each retention test. Red lines for each measurement represent mean and standard deviation. Black body represents the histogram (data distribution) of each test. For visual effect each histogram is symmetric along the vertical axis.

data. The device was interrogated every second for 2 minutes at every state twice. The plotted data (plot g) shows stability over the test period. The data also shows that each set of retention

data perfectly overlaps each other, showing that the device retained its state during continuous DC biasing when connected to the PCB. Each FRA test lasted between 3 and 4 minutes. To further highlight, that stability and endurance were not of a concern, distribution of the acquired memristance data is presented in a 'violin' plot (Figure 3.17h). For each memristive setting, percentage deviation from the mean is shown, along the standard deviation lines. Overall, the devices remained within $\pm 1\%$ of their mean value. Some settings resulted in higher spread, however this seems to be independent of the value of the memristance. Furthermore, many of the distributions closely follow a Gaussian shape. This is important as it means that the process is wide sense stationary, with time-independent mean. Therefore the distribution can be mainly attributed to the measurement noise, rather than device drift.

3.5 Memristor-Tuned Capacitor

3.5.1 CMOS Scalable Approach

There are two methods of synthesising capacitance - with and without inductors. Of course the very reason why many synthesise inductors in the first place is the poor quality, large tolerance and large area they consume. Therefore an inductor-less solution is preferred when realising synthetic capacitors.

The approach shown in Figure 3.18a-c benefits from just a single variable gyrator. That means the input and output gyrators need to be matched just once, and any variation stemming from the memristor tuned bias circuitry is omitted. However the drawback is the increased number of gyrators need to synthesise the impedance function. This results in increased power consumption as well as diminished bandwidth of the circuit.

The alternate approach (Figure 3.18d) benefits from lower complexity, and lower power dissipation. However, poor quality of CMOS inductors together with relatively low self-resonant frequencies are likely to require additional compensation techniques, to stabilise the device. In PCB realisation, the concept with fixed inductor holds, since large ESR sufficiently dampens the response.

3.5.2 Results

Procedure

A procedure similar to that of the synthetic inductor was followed. Tests were performed using both architectures - with and without physical inductor. In both cases the FRA data was fitted to the capacitor model. In the inductor-less case, the circuit was found to be unstable and it

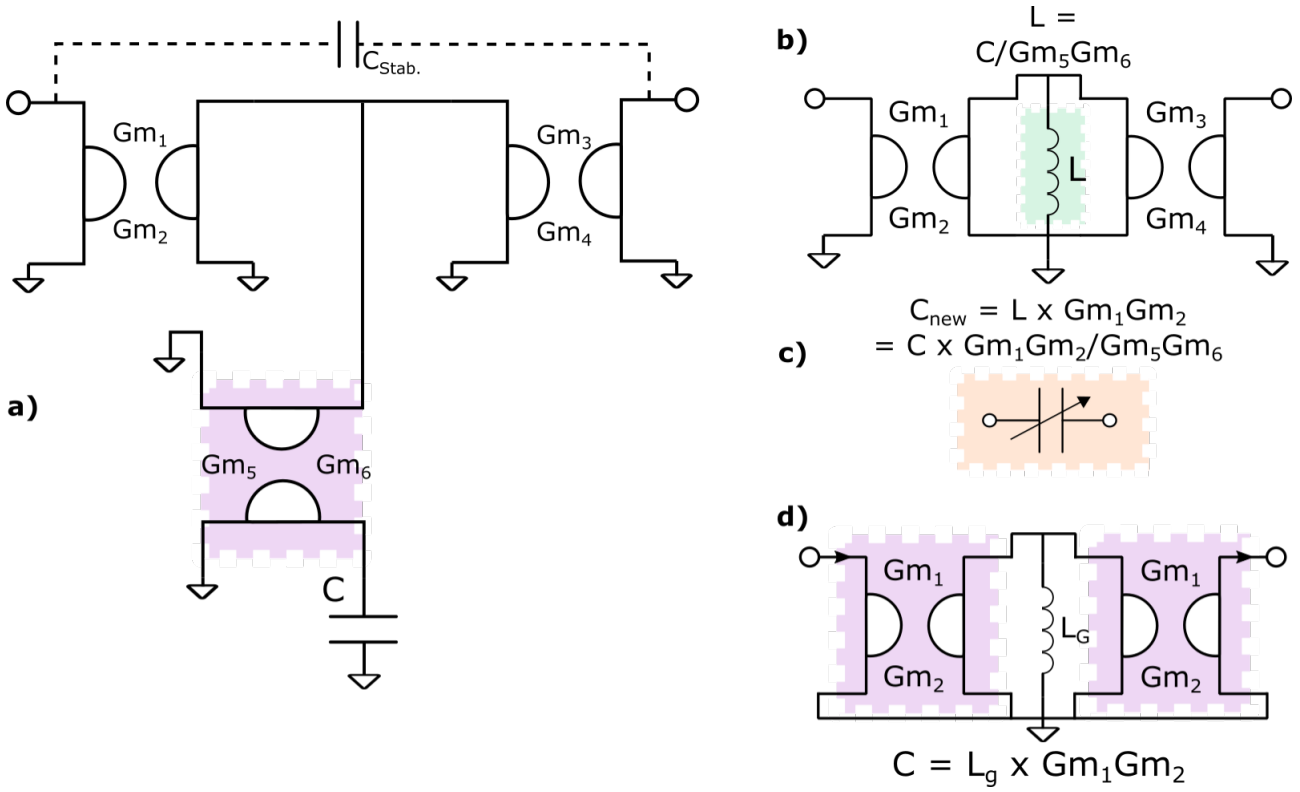


Figure 3.18: Two methods of realising synthetic variable capacitors. **a)** CMOS scalable method based on triple gyrator. By gyrating a capacitor, a tuneable inductor is formed. Optional stabilising capacitor was used as shown by the dotted connection. **b)** Tuneable inductor is then gyrated once again to form the variable capacitor. **c)** Magnitude of the variable capacitor is determined now by the ratio of two gyrators. **d)** Alternative method requires a physical inductor.

was compensated with a capacitor parallel to the input gyrator. This had a stabilising effect, however it also introduced effective series inductance into the synthetic circuit.

Capacitor Stabilised 3-Gyrator Architecture

A ceramic 10nF capacitor was gyrated. Due to the addition of the stabilising capacitor across the input gyrator, the circuit was modelled as a series inductor and capacitor. The test setup followed that of the synthetic inductor. For FRA analysis, an a high pass RC network was constructed using 2.2k Ω load resistor. 7 resistive states of the memristor were used: 4.3 k Ω , 5.3 k Ω , 6.8 k Ω , 10.5 k Ω , 13.7 k Ω , 20.2 k Ω and 24.7 k Ω . More importantly, as it will become evident in the IV traces for each set of results, 3 different memristors were used, as they became defective during testing. This produced distinctly varying memristive properties.

Figure 3.19a-b shows the FRA data of the synthetic RC high pass filter. Quite distinctly deviations from the ideal behaviour can be observed at lower frequencies in the phase response. Furthermore the addition of the bypass capacitor manifests itself as clear resonant peak in the gain response, and as phase drop below 0 radians. Nonetheless the extracted data (through NM

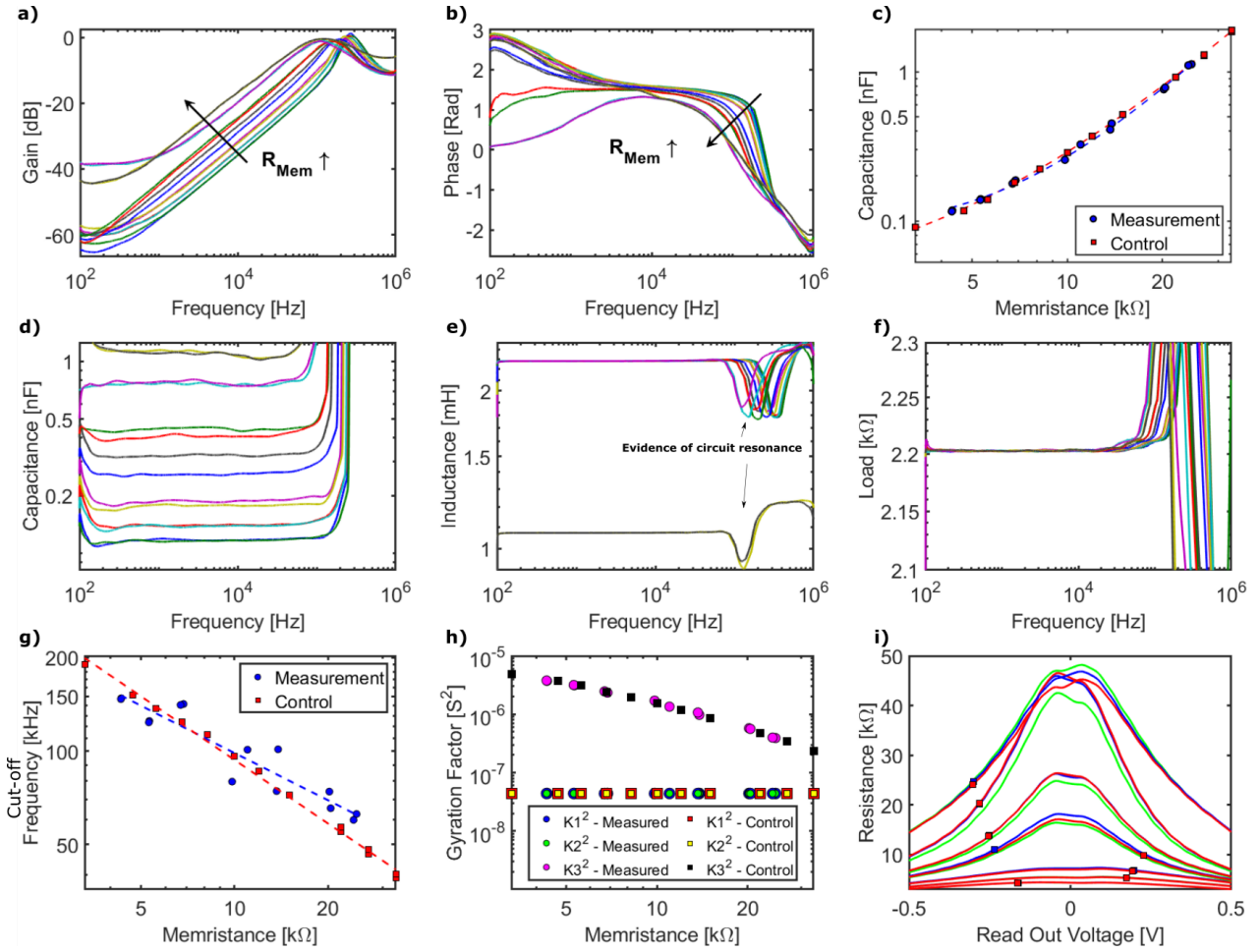


Figure 3.19: Performance of inductor-less synthetic capacitor. Results gathered were gathered with PCB test platform and circuit was stabilised with a bypass capacitor. **a)** Gain responses of the FRA data. **b)** Phase responses of the FRA data. **c)** Extracted memristor tuned capacitance. **d)** Frequency dependence of the memristor tuned capacitance. **e)** Synthetic series inductance, realised as a result of using a bypass capacitor. Two value of stabilising capacitor were used, resulting in two groups of data. **f)** Extracted load resistance used for the test, showing close matching with real resistor used within bandwidth of operation. **g)** Measured bandwidth of the synthetic capacitor. Measurements were repeated with real resistors for control. **h)** Estimated gyration constants of the fixed gyrators (K1 and K2) as well as variable gyrator (K3). Data was compared to control values gathered with real resistors. **i)** Resistance-voltage curves resulting from IV measurements during each test. Operating points for each setting are highlighted as points.

simplex algorithm fitting data into series RLC network) shows clear tunability of the synthetic capacitor. At $4.3k\Omega$ a capacitance of $118pF$ was measured, while at $24.7k\Omega$ the value rose to $1.11nF$. The relationship between capacitance and memristance follows that of inductor, i.e. $C \propto R_M^{1.5}$. This is due to the fact that the input and output gyrators remain fixed, while the value of the embedded synthetic inductor is controlled - leading to a directly proportional behaviour (as shown in Figure 3.18c).

Through model fitting using the NM simplex algorithm, frequency dependence of the capaci-

tance, inductance and load resistance was resolved (Figure 3.19d-f). It can be seen that there are two groups of inductive measurements one positioned around 2.2mH mark and one around 1.1mH mark. That is a result of stabilising capacitor change for the last measurement.

Looking at the resolved values of the load resistance, it can be seen that the value of $2.2k\Omega$ is indeed correctly estimated up to a point where the simple RLC model breaks down. Similar patterns are observed in all three parameter graphs, thus reinforcing the view that a more complex model would be more suited for higher frequencies.

However, the design is again evaluated based on its ability to synthesise capacitance. Its bandwidth is inversely proportional to the memristance as shown in plot g. The noisy memristive data shows comparable trend to the data acquired with resistors and higher signal-to-noise ratio (SNR). Effectively at $20k\Omega$ the useful bandwidth of the device is just around 60 to 70 kHz (using PCB test platform). These numbers are expected to increase by 2 orders of magnitude when realised on CMOS.

The data allowed to estimate the gyration constants of all three gyrators - input (K_1), output (K_2) and tuned one (K_3) (plot h). Data shows that the both input and output are perfectly matched and align with the control data. Simultaneously, tuned gyrator shows inverse relationship with memristance as expected.

Finally, Figure 3.19i shows the static resistance-voltage characteristic of each device. The shape overlap and inconsistency arises from using three different memristors, which further exemplifies the difficulty in utilising the devices. The three devices were on the same wafer and the same array. Naturally, due to varying electrode lengths they each had different effective series resistance, however the shapes are indicative of substantially different nanoelectronic behaviour.

Fixed Physical Inductor Architecture

The procedure for the test with physical inductor was simplified, having demonstrated the stability and repeatability of the measurements. A single read out was performed at each memristive level. A physical $10\mu H \pm 30\%$ inductor with minimal ESR of $18.5m\Omega$ was used.

The resulting synthetic capacitor was therefore expected to produce comparably low equivalent parallel resistance (EPR). Its presence is already seen in the FRA gain data (Figure 3.20a). At low frequencies, EPR dominates the response, thus bringing the phase to 0 radians. As frequency increases capacitive behaviour becomes more prominent, until corner frequency of the test RC circuit is reached. For the tests a $33k\Omega$ resistor was used. As standard phase roll-off is observed (plot b), however as in previous cases it overshoots and continues below the theoretical value.

As opposed to the 3 gyrator configuration, here an inverse dependence on the memristance is observed. This is due to the fact that capacitance in this setup scales as:

$$C_{synth} = K^2 L \quad (3.89)$$

Hence, as memristance increases, bias current decreases, reducing the transconductance of the OTA. Overall the gyration factor reduces as a result, bringing the synthetic capacitance down. In addition, due to the use of a $10\mu H$ inductor, the realised capacitance is comparably low, especially on PCB, ranging from 800fF (at $33k\Omega$) to 10.2pF (at $3.3k\Omega$).

What valued inductor What ESR - it shows in low freq response of gain Simplified procedure Results comparing to inductorless approach

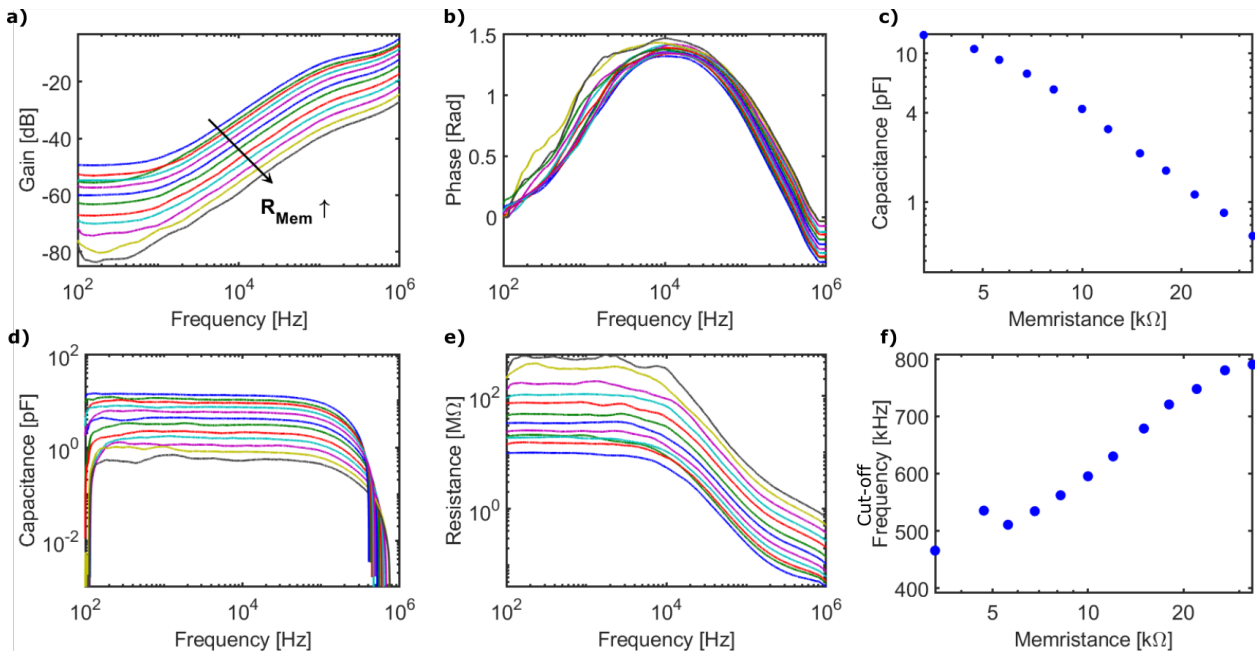


Figure 3.20: Performance of synthetic capacitor based on gyrated physical inductor. **a)** Gain response of the FRA measurement. **b)** Phase responses of the FRA analysis. **c)** Memristor tuning results in inverse relationship between memristance and capacitance. **d)** Capacitance spectrum, showing larger bandwidth than triple gyrator structure. **e)** Extracted equivalent parallel resistance of the synthetic capacitor. **f)** Estimated bandwidth of operation, showing nearly ten fold improvement over inductor-less approach.

The simple leaky capacitor model used in the NM extraction algorithm proves accurate for frequencies up to 10kHz. Beyond that, the EPR begins to drop. However, the value of the parallel resistance starts at around 10 to $200M\Omega$, and as it drops it remains in the $M\Omega$ region. Capacitance on the other hand, remains fixed until frequency limitations of the discrete components begin to dominate. This results in much higher bandwidth than all of the previous methods presented - from 500 to 800 kHz.

3.6 Discussion

3.6.1 Limitations and Mitigation

In this chapter four reconfigurable elements were demonstrated: memristor-enabled gyrator, inductor and two capacitors. Their behaviour is summarised in Table 3.6.1. The memristors used as tuning elements in this realisation make continuous, precise, and non volatile control of the synthesised behaviour possible. However, like any practical circuit, the memristive blocks are subject to imperfection factors.

First, the greatest limitation of broadband, high dynamic range impedance synthesis is power dissipation: large internal node voltage swings require a significant power supply overhead. In the presented PCB-based demonstrator the measured power dissipation for the synthetic inductor as a function of memristance was ≈ 700 mW at 3.3 k Ω (Figure 3.21). As the memristance increases to 82 k Ω , the power drops to around 250 mW. Most of the power losses stem from the OTA's bias network and are simple to eliminate through further design optimisation. Moreover, there is a limit to the maximum feasible memristance setting (around 100 k Ω with the presented technology), which determines the smallest gyration constant obtainable. Transitioning the design on chip would mean a power rail reduction from ± 15 V to 3.3 V and thus decrease the power consumption by two orders of magnitude, to single-digit mW at the cost of a reduced dynamic range. Further gains are possible using more resistive memristors that become progressively available as the technology matures. As a result a whole palette of low-power CMOS synthetic tuneable components is in sight not only at low, but eventually at radio frequencies.

Synthetic Component	Range	Bandwidth	Drawback	Comment
Gyrator	$4 \times 10^{-8} \text{ S}^2 - 5 \times 10^{-9} \text{ S}^2$	Up to 800kHz	Requires buffering Limited current range	None
Inductor	17.5mH - 240mH	Up to 300kHz	Inherently resonant	Larger inductors were also realised. This method has theoretically no upper bound. Inductors as large as 50H were synthesised. Main consequence is reduction in bandwidth.
Capacitor (Inductorless)	118pF - 1.11nF	Up to 200kHz	Limited stability Decreased bandwidth	PCB layout was sub-optimal. Stability was affected by presence of objects near the board.
Capacitor (With Inductor)	800fF - 1.05pF	Up to 800kHz	Requires physical inductor Leaky synthetic capacitor	Low capacitance realised due to low value of physical inductor. Potentially higher value is possible with bigger area consumption.

Table 3.1: Summary of all memristor controlled building blocks. Table shows what is demonstrated in this chapter - value range and bandwidth. In further applications of those components, other bias settings were also used allowing to synthesise various other component values.

Second, the memristor is a non-linear device, whose resistance depends on the voltage applied across its terminals. The circuits presented in this chapter do not hold the memristors in an effectively constant voltage bias under normal operation. this leads to slight variations in the current mirror behaviour, resulting in the complex Lambert function behaviour. However, as

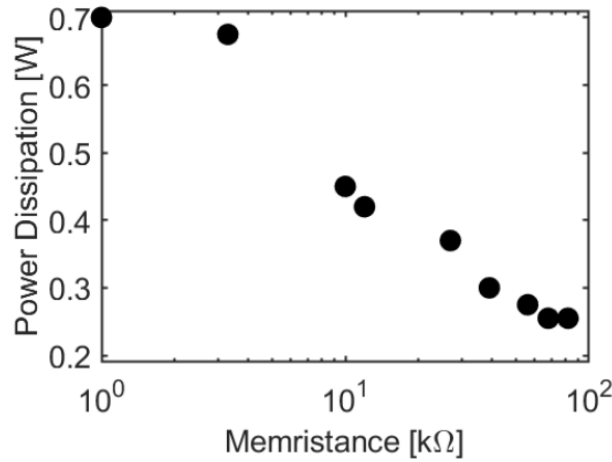


Figure 3.21: Power dissipation of PCB based synthetic components. Power dissipation is agnostic of synthesised nature of the reactance.

memristor is part of the bias network, the signals incident on the gyrator do not reflect on the device, hence it is signal-independent despite non-linearities in its IV characteristic.

Next, all synthetic components' behaviour depends on the frequency response of the transconductors used: the measured bandwidth for the analog blocks shown, is limited by the gyrator self-resonance to 100kHz-800kHz, depending on the gyration factor realised. This is the result of the large input capacitances of the discrete OTAs used for the demonstration. In a PCB-based implementation the useful bandwidth is further reduced by the trace capacitances. However, within their ultimate environment - on an integrated circuit - bandwidths in excess of several MHz are possible, thus extending the utility of the presented method to higher frequency applications such as fast analogue computational platforms or RF circuits. Appendix C shows simulations with 0.18 μm CMOS, currently under development by Shen [11]. Further performance gains are achievable at more advanced technology nodes.

3.6.2 Active Synthesis in Literature

Gyrators and their use in realising active inductors and capacitors have been known for some decades now. Nonetheless the above presented methods do show improvements in some performance metrics over the currently used solutions. Active inductors can be split into two subgroups: narrow-band and wide-band synthesis. Narrow-band devices tend to operate at a predetermined frequency or range of frequencies. They are often a lot smaller and less power-hungry. At the same time offer little to no tunability range and have to be designed for specific applications, i.e. they are not general purpose building blocks. Wide-band devices are quite the opposite: often based on gyrator (Gm-C) structure, they often very broadband behaviour, however they come at a price of large power consumption and big area occupancy. Some of the methods are discussed in the following paragraphs, highlighting their differences to the

memristor-tuned solution discussed in this chapter.

Narrow Band Synthesis

Wu Current-Reuse Active Inductor [12]: Wu proposed a simplified version of a gyrator where the roles of the positive and negative transconductors are realised through common-gate and common-source FETs, respectively. The realised input-referred RLC tank takes the following values:

$$C = C_{gs1} \quad (3.90)$$

$$R = \frac{1}{g_m} \quad (3.91)$$

$$L = \frac{C_{gs2}}{g_{m1}g_{m2}} \quad (3.92)$$

$$ESR = \frac{g_{o1} + g_{o2}}{g_{m1}g_{m2}} \quad (3.93)$$

While current source I_1 remains fixed, additional source I_2 is used to modulate the transconductance g_{m2} . The circuit is designed to *reuse* the current of the preceding stage as the source I_2 . The limitations of the above lie in the inductors dependence on the remainder of the circuit design, and dependence of the inductance value on the gate source capacitance (equation 3.72). The precise value of C_{gs} is modulated due to input signals distorting the DC bias of the FET. As such inductance will vary based on the previous stage, technology used, signal magnitude and frequency. Finally, the grounded inductor realisation proposed by Wu consumed nearly 38mW (14mA at 2.7V), whilst realising a very limited range of inductances, albeit at RF frequencies (bandwidth from 400MHz to 1.1GHz)

Lin-Payne Active Inductor [13]: The bandwidth of the proposed solution ranges from 1.1 to 2.1GHz. Its advantage undoubtedly very low voltage operation as the circuit requires a rail of just $V_T + V_{Sat}$ to operate - the authors discuss sub-1V power rail to operate the circuit. Of course, this leads to a trade-off in dynamic range of the input signals. Circuit analysis leads to similar expression of equivalent RLC values as those of Wu Current-Reuse method. Additionally, in theory the inductance can be also tuned through the bias currents, however Lin-Payne presented no such results. The drawback are yet again: narrow bandwidth, low headroom and lack of demonstrated tunability.

Ngow-Thanachayanont Active Inductor [14]: Bandwidth of the reported circuit once again is relatively narrow - 10MHz to 1GHz. In that range the inductive behaviour is clear, however the ESR begins to increase rapidly at 200-300MHz, effectively realising a very low quality inductor above those frequencies. Circuit analysis yields component values dependent

on transconductance of individual FETs as well as their nodal capacitances, hence producing such a limited range of useful frequencies. As with other transistor level approaches, the realised inductances are fairly small - bigger than similarly sized spiral inductors, however smaller than values achievable with wide-band tuning techniques. The group reports nominal value between 31 and 40nH. Large transistor dimensions, required to realise practical values of inductors, have an adverse effect on the ESR (at DC). The group reports as much as 23Ω of resistance for a 31nH inductor at DC. When measured at 1GHz, the quality factor was found to be around 1.6.

Other Active Inductors: The list of similar CMOS, narrow-band approaches is indeed quite large. Among other methods there is Hara Inductor [15], [16] or Wu Folded Inductor [17]. Hara's approach was to bias a FET device in its triode region and thus realise a resistor. The voltage-controlled resistor (VCR) is then used to change the bias of further MOSFETs, which realise the active inductor. However, the value of the inductance is not straightforward and frequency dependent:

$$L = \frac{C_{gs}(g_m R - 1)}{g_m^2 + \omega^2 C_{gs}^2} \quad (3.94)$$

The headroom limitations of Hara's inductor are addressed by Wu Folder inductor realisation. The input impedance of the circuit in this case becomes:

$$Z_{in} = \frac{sRC_{gs} + 1}{sC_{gs} + g_m} \quad (3.95)$$

The inductor implicitly has a fixed bandwidth of operation, which for practical reasons cannot be widely adjusted to lower frequencies. An advantage of the folded inductor is its lower power consumption of around 4.2mW.

MOS Capacitance: Capacitance is that much easier to realise, in that it is inherently present in MOS devices. By controlling the properties of the MOS stack it is possible to realise CMOS compatible capacitors. The gate capacitance depends on both voltage applied and the frequency of the input signal. When the device is in the inversion, capacitance is at its lowest (at high frequencies). As the device enters depletion mode, the MOS capacitance begins to rise and finally settles at its maximum value once the device reaches accumulation mode. At high frequencies the story is a little different: MOS stack exhibits high capacitance in both inversion and accumulation mode, but drops in the depletion region. The difference in capacitive properties in the inversion mode for low and high frequency signals stem from interfacial polarisation [18]:

$$\text{Accumulation : } C_{HF} = C_{LF} = C_{ox} \quad (3.96)$$

$$\text{Depletion : } C_{HF} = C_{LF} = \left(\frac{1}{C_{ox}} + \frac{\chi_d}{\epsilon_s} \right)^{-1} \quad (3.97)$$

$$\text{Inversion : } C_{LF} = C_{ox} \quad C_{HF} = \left(\frac{1}{C_{ox}} + \frac{\chi_{d,max}}{\epsilon_s} \right)^{-1} \quad (3.98)$$

, where χ_d represents variable depletion width of the device. This results in practical limitations: MOS devices cannot be used for high frequency, bipolar signals as the effective capacitance will be a function of time, applied signal frequency and amplitude.

Wide Band Synthesis

Inductors: Wide band synthesis is often performed with OTAs and derivatives of second generation current conveyors. A study by Al-Absi [19] followed similar approach and utilised an LM13700 OTA to build active inductors. While the simulations are idealised, practical results yielded a bandwidth 3.5 times smaller than the presented method (80kHz vs 300kHz) and a similar range of component values. The study however lacks a viable method of control and simply simulates an ideal current source. Since the study also used discrete components, the group used 10nF capacitor: a value 10 times larger than the capacitor used in this chapter. Furthermore, by not isolating the input of the LM13700 with a MOSFET based buffer, the group failed to realise ESR as low as the memristor-enabled method (100-150Ω).

Other methods are often very similar [20]–[23]. However, in principle the results are often incomplete: they lack a method of reconfiguration, they realise a grounded active inductance, are solely based on idealised simulations or form a part of bigger circuit and therefore cannot be considered as direct drop-in replacement for physical inductors. Yucel and Yuce [24] provides an excellent summary of tunable all-pass filters developed to date.

Capacitors: Wide-band tunable capacitors are usually realised with MEMS devices, as they offer wide range of component value and extremely high Q factors. CMOS compatible approaches are however rare. They either rely on current multipliers [19], complex DC/AC converters loaded with physical inductors [25] or simply a bank of binary switched capacitors [26]. Among the listed methods current multipliers show the biggest potential as reported results (though often simulated) claim direct drop-in replacement and high range of values [27].

3.6.3 Final Remarks

The methods presented in this chapter should be viewed as proof of concept: the PCB versions are extremely limited and underperforming compared to what is achievable on CMOS. Conveniently, however, the presented circuits find their equivalents in transistor-level architectures, rendering this approach viable. While active inductors do indeed perform better than other discrete devices in literature (bandwidth, range of values, stability), the tunable capacitor proves more difficult to defend, due to its instability. As such to make use of the memristor tuned capacitors very careful design and layout are required so as to ensure stability. However, even then, the blocks may struggle to act as direct drop-in replacements, as reactive loading may destabilise the circuit. It is therefore believed that other methods, which do not require 3 gyrators, such as current scaling briefly mentioned in the previous paragraph, may prove more useful for the purposes of synthesising variable capacitance. In the following chapter, both memristor enabled inductors and capacitors are tested in standard applications, to further assess their performance.

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Chapter 4

Applications of Memristor Enabled Building Blocks

The following Chapter is a practical one. Its aim is to demonstrate versatility of the building blocks demonstrated in the previous Chapter. Their use as direct drop-in replacement for standard passive elements is shown through low-level applications such as: filters, resonators, oscillators and compensators. The measurements presented in those areas show exciting opportunities for reconfigurable systems. The discussion then continues with simulated memristor amplifiers and an investigation of the consequences of recently reported memcapacitive switching on memristive devices. The contributions of this work are continuous time and value reconfigurable passive circuits. The discussed circuits steer away from designs based on redundancy or data converters and instead employ memristors and memimpedances to perform parametric and functional tuning.

4.1 Introduction

The applicability of the memristive building blocks - the reconfigurable inductor, capacitor and resistor (memristor) - in realising basic analogue functions is studied to further assess the performance of these units. These functions include: phase compensators, filters, pulse width modulators, resonators and amplifiers. These subsystems are often found in complex electronic devices, but they are usually limited in their performance to either fixed behaviour or discrete reconfiguration steps. As such it is envisioned that through testing of application, it will be possible to answer three questions:

1. Is the memristor suitably isolated from spurious, input-induced signals?

2. What system complexity is possible with gyrator based blocks?
3. Is there anything to be gained by introducing analogue reconfigurability to classic circuit topologies?

4.2 Filters

All electronic circuits can be regarded as filters. The purpose of the filter is to modify the spectrum of the signal to fit the particular application - most commonly filters are thought to include classic low or high pass filters. Circuits such as operational amplifier, which are internally compensated, are low pass filters, albeit with often high pass-band gain. Another non-intuitive example of a filter is a standard current mirror, which purpose is to filter no frequencies, thus acting as an allpass filter. Of course due to transistor technology limitations, gate capacitance will lead to low-pass behaviour. As filters are therefore the constituent elements of electronics, their implementation with gyrator-based building blocks is evaluated. Four circuit topologies are presented which can be viewed as standard realisations.

4.2.1 Single Active Element: Lead-Lag Compensator

Theory

The analysis begins with a circuit utilising just a single building block so as to better understand the limitations of each cell. An adjustable lead-lag compensator is a simple, but extremely versatile filter frequently used to compensate analogue feedback circuits. In the literature it is also referred to as the bilinear filter. A lead-lag filter is a combination of a low-pass (integration) and a high-pass (differentiation) filter resulting in a Laplace domain transfer function:

$$H(s) = G \frac{\omega_1 + s}{\omega_2 + s} \quad (4.1)$$

where G is the gain. The phase lead component (high-pass) allows to control the speed of the transient response of the system, while the phase lag (low-pass) component provides control of the steady-state performance. The relative positioning of the low-pass and high-pass corner frequencies ($\tau_{1,2} = \omega_{1,2}^{-1}$) determines the nature of the compensation. Multiple lead-lag compensators can also be used to synthesise more complex filter functions. For example, three adjustable lead-lag compensators can approximate a universal proportional-integral-derivative (PID) controller.

Lead-lag filters shown in Figures 4.1a and 4.2a have been assembled using the synthetic blocks. Two memristors control the values of $\tau_{1,2}$, allowing to tune the integral and derivative behaviour.

Inductor-controlled lead-lag

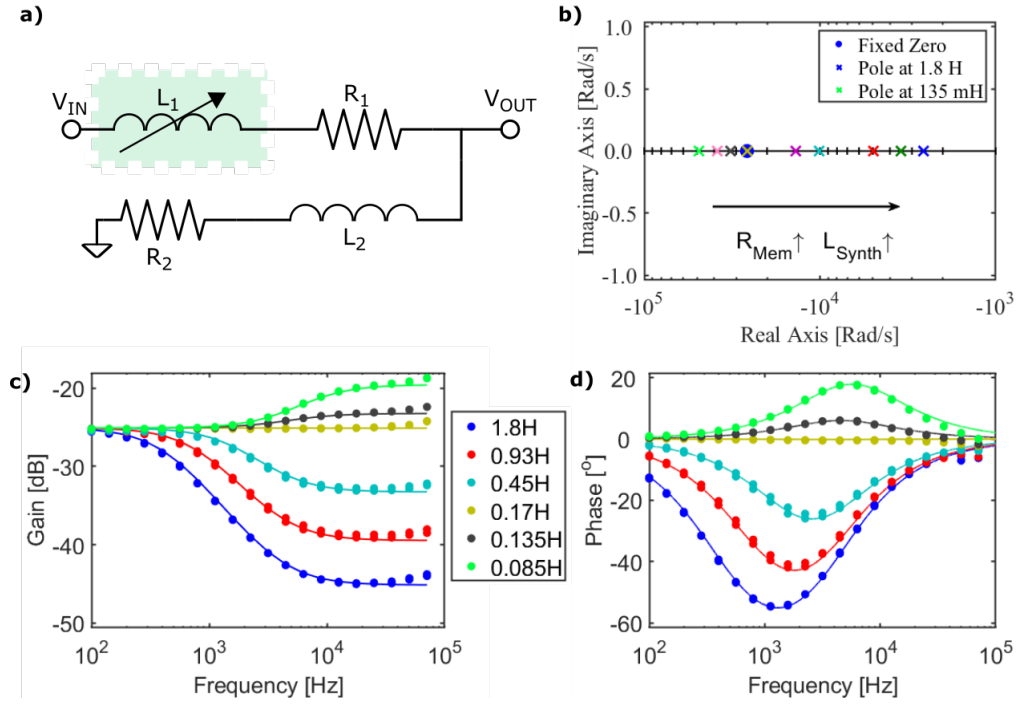


Figure 4.1: Passive inductive reconfigurable lead-lag compensator. **a)** Passive inductor controlled lead-lag circuit. Inductor L_1 is variable; L_2 , R_1 and R_2 are fixed. **b)** Pole-zero representation of the lead-lag tuning. Zero frequency remains constant, while pole location can be freely controlled. **c)** FRA gain results of the inductive lead-lag at various memristive settings. **d)** Complimentary FRA phase results clearly demonstrating lead, lag and no compensation.

This compensator was designed with a fixed zero (at $1/\tau_1 = 26 \text{ rad/s}$, $R_2 = 220 \Omega$, $ESR_{L_2} = 40 \Omega$ and $L_2 = 10 \text{ mH}$) and variable pole (at $\omega_2 = 1/\tau_2$) frequencies (Figure 4.1b). The synthetic inductance increases with memristance causing the pole frequency to decrease:

$$G = \frac{L_2}{L_1 + L_2} \quad (4.2)$$

$$\tau_1 = \frac{L_2}{R_2} \quad (4.3)$$

$$\tau_2 = \frac{L_1 + L_2}{R_1 + R_2} \quad (4.4)$$

$$\text{therefore : } f_2 = \frac{1}{2\pi} \frac{R_1 + R_2}{L_1 + L_2} \quad (4.5)$$

The resistance was chosen to be $R_1 = 4.4 \text{ k}\Omega$, a value selected to be much larger than the

inductor series resistance. The tuneable inductor, with value in the 85mH up to 1.8H range, was realised by gyrating a 100nF capacitor. Gain and phase delay plots of the filter are shown in Figure 4.1c-d.

Capacitor-controlled lead-lag

Both the pole and the zero frequency of the compensator (Figure 4.2b) are set by the variable capacitance C_1 . The pole location can be made largely independent of the value of C_1 if C_2 is much bigger than C_1 :

$$G = \frac{C_1}{C_1 + C_2} \quad (4.6)$$

$$\tau_1 = \frac{1}{R_1 C_1} \quad (4.7)$$

$$\tau_2 = \frac{1}{C_1 + C_2} \left(\frac{1}{R_1} + \frac{1}{R_2} \right) \quad (4.8)$$

Ensuring that:

$$\frac{C_2}{C_1 + C_2} \simeq 1 \quad (4.9)$$

allows to simplify:

$$\tau_2 \simeq \frac{1}{C_2} \left(\frac{1}{R_1} + \frac{1}{R_2} \right) \quad (4.10)$$

$$\text{therefore : } f_2 = \frac{C_2}{2\pi} \frac{R_1 R_2}{R_1 + R_2} \quad (4.11)$$

The location of the transfer function zero frequency is controlled with the synthetic capacitor C_1 . C_2 was set to 470 pF, while the biggest value of the synthesised C_1 is 13 pF, ensuring the condition in equation 4.9 is met. C_2 could alternatively be realised with the synthetic capacitor. Resistor values used are $R_1 = 1M\Omega$, $R_2 = 10k\Omega$.

Measured results for the capacitor-controlled lead-lag compensator, shown in Figure 4.2c-d, are in close agreement with theory. The discrepancies observed at low frequencies in the capacitive realisation are due to the finite variable equivalent parallel resistance (EPR) of the synthetic capacitor. Depending on the value of the gyration constant EPR can vary from as low as few $M\Omega$ up to 100 $M\Omega$. Further analysis of pole-zero location is shown in Figure 4.2b. It shows that zero location has indeed remained constant despite tuning of the lead-lag. In summary, the

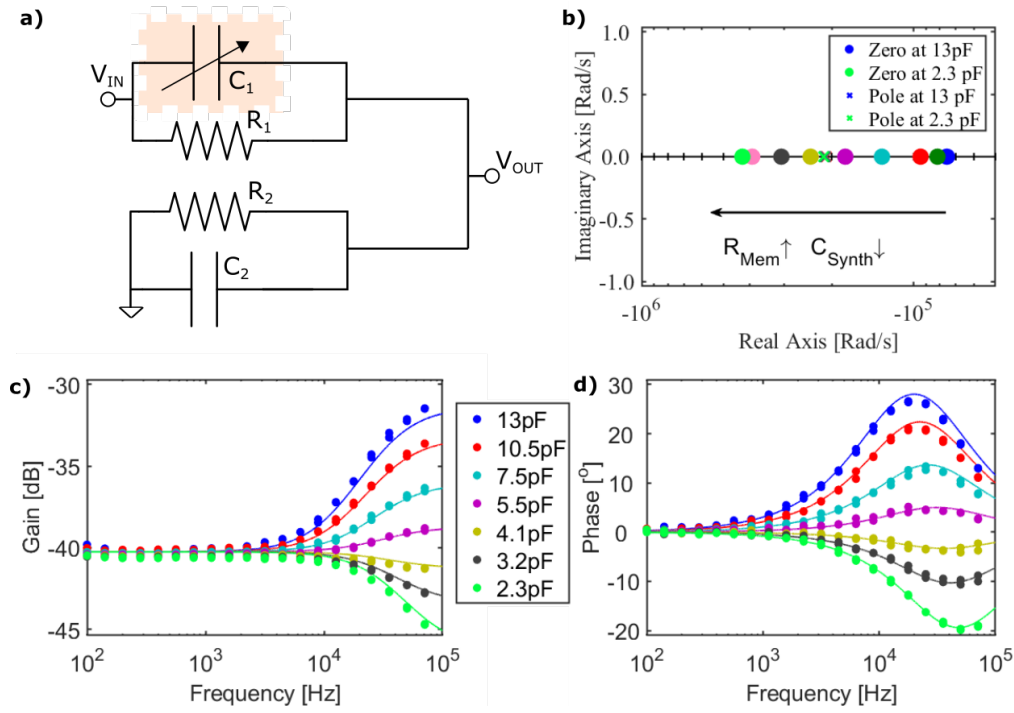


Figure 4.2: Passive capacitive reconfigurable lead-lag compensator. **a)** Passive capacitor controlled lead-lag circuit. Capacitor C_1 is tuned; C_2 , R_1 and R_2 are fixed value physical components. **b)** Pole-zero representation of the lead-lag tuning. Pole frequency is remains largely constant, while zero location can be freely controlled. **c)** FRA gain results of the capacitive lead-lag at various memristive settings. **d)** Complimentary FRA phase results clearly demonstrating lead, lag and no compensation.

measurements presented here demonstrate a novel method of synthesizing adaptable control units. The ubiquity of a single lead-lag compensator and its low complexity can be leveraged in the design of adaptive control systems, such as PID controllers.

Implications

The above allows to make three conclusions regarding the usefulness of the building blocks. Firstly, the gyrator-based synthetic components clearly allow for an easy and predictable re-configuration of the basic functionality. Together with ArC One platform, the tests could be repeated with $\pm 5\%$ accuracy. As the technology matures, and underlying physics is better understood the repeatability margins will shrink.

Secondly, as expected from results in the previous chapter the blocks in the discrete form have fairly low bandwidth. This manifests itself as deviation from the theoretical gain and phase responses. In the case of variable inductor, the gain always drifts up around the edge of the bandwidth. It would have been expected to observe the same for capacitor-based lead lag, however the accuracy of the capacitance estimation is limited since the values are oft the order of parasitics.

Thirdly, what was not mentioned in the results above is the limited input range. Since gyrators reverse the roles of voltage and current, low impedance synthesis, will lead to high input currents, which will transform into high nodal voltages within the gyrator structure. Therefore the input voltage must be controlled to prevent nodes hitting the rail voltage.

4.2.2 Two Active Elements: RLC Resonator

Theory

Understating the limitations of a single building block circuit, allows to use two synthetic components and asses their performance further. Here an RLC topology is used to demonstrate independent control of both the centre frequency and the quality factor. Two memristors are used to achieve this. This is to say that by varying the values of both L and C it is possible to retain the same centre frequency while changing the quality factor, and vice-versa. This however requires control of both devices simultaneously as demonstrated by the equations below. The RLC filter is yet another embodiment of a second order filter - in particular it forms a bandpass filter, where corner frequencies can be very closely spaced, i.e. feature very high quality factor, depending on the choice of component values. It perhaps makes more sense to look at RLC circuit as a resonator rather than filter even though the two are definitions are very closely linked. The reason behind this is that RLC circuit is defined by a centre (or resonant) frequency ω_c and its quality factor Q of that resonance rather than two corner frequencies as shown in by its Laplace domain transfer function:

$$H_{RLC}(s) = G \frac{\frac{\omega_c}{Q} s}{s^2 + \frac{\omega_c}{Q} s + \omega_c^2} \quad (4.12)$$

$$\omega_c = \frac{1}{2\pi\sqrt{LC}} \quad (4.13)$$

$$Q = \frac{1}{R} \sqrt{\frac{L}{C}} \quad (4.14)$$

High quality resonant circuits are often used as clock generators in digital processors. The clock frequency is then halved multiple times to produce the required speed of the processor. This approach requires a simple fixed resistor-capacitor (RC) relaxation oscillator, with multiple divide-by-2 blocks. As a result the frequencies are distributed logarithmically and the circuit is designed with inherent resource redundancy. A higher precision tunable clock allows to run at frequencies closer to the maximum processing capability. To realise that, a resonant circuit based on a resistor, synthetic capacitor and a synthetic inductor was built: a series RLC resonator (Figure 4.3a). Both the centre frequency and the quality factor of this resonator can be adjusted by the resistance of two memristors, as shown earlier. Signal voltages were

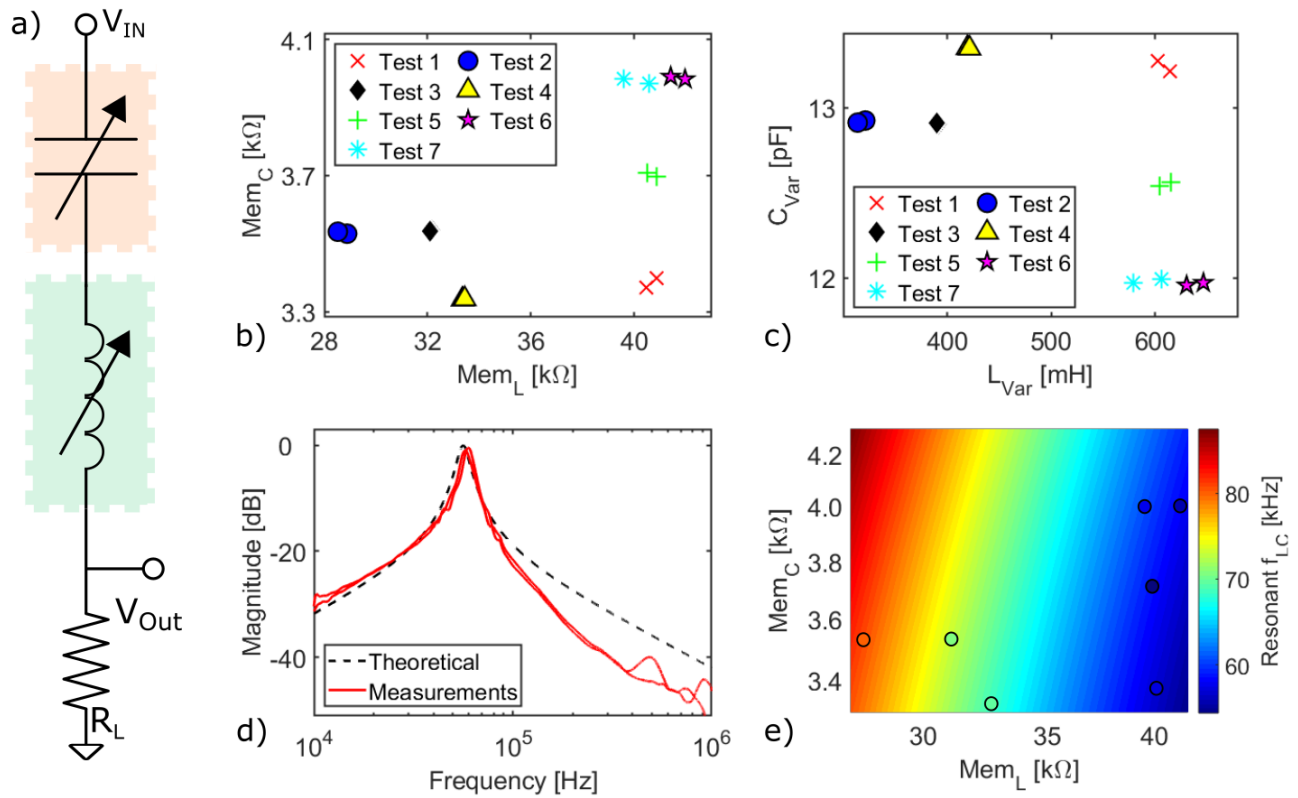


Figure 4.3: RLC tuned frequency and quality factor resonator. **a)** RLC resonant circuit. The load was 33 k Ω . **b)** A total of seven tests were run. These are the memristances used for each test and for each synthetic component. Frequency response measurements were repeated twice; the variation between two runs for one test are attributed mainly to the charge injection during reconfiguration switching. Tests 3 and 4 are examples of when the stray charge did not affect the memristors. **c)** The operating points for each test in terms of synthesised inductance and capacitance. **d)** Results of test 7. The magnitude of the resulting transfer function from both measurements is drawn along the theoretical expected curve. The measured behaviour closely follows the theoretical curve up until 100 kHz. The combined poles introduced by a total of 4 gyrators produce a faster roll-off. **e)** Expected theoretical resonance frequency, within the specified range of memristances. The measurements are within $\pm 5\%$ of theoretical values. Coloured points show the extracted resonant frequencies of each second measurement.

limited to ± 0.5 V in order to avoid saturation in internal circuit nodes. Two memristors were used to program the variables of this circuit, seven tests were performed, each with different memristor settings. The test summary is presented in Figure 4.3b-c. Plots show the state of both memristors and corresponding synthetic values for each test. Each test was carried out twice. In most tests there is some drift in the memristance controlling the inductor, except in tests 3 and 4. As the higher resistive states are more volatile, reproducibility is weaker at the larger memristance values.

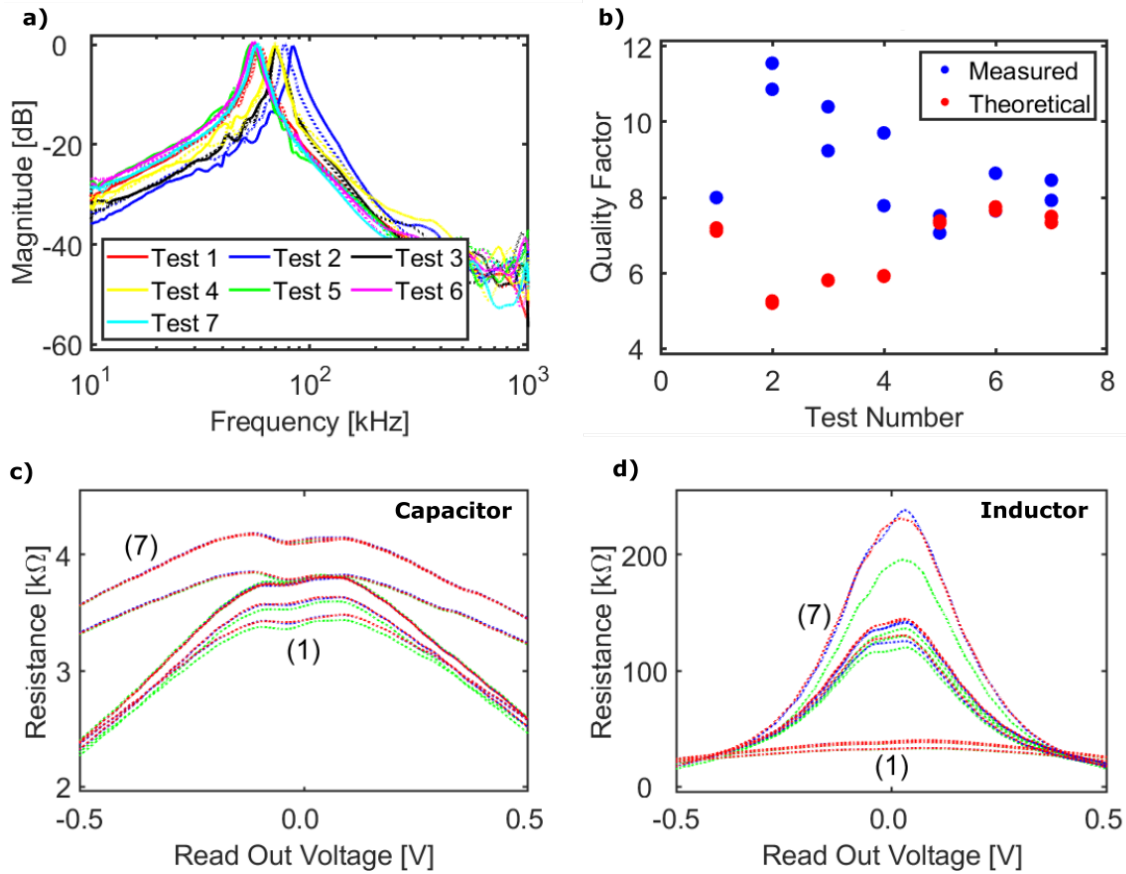


Figure 4.4: Further analysis of RLC data. **a)** All Bode Plots of the gain of the RLC resonator. **b)** Measured and theoretical quality factors for each test. Discrepancy in results for tests 2,3 and 4 is caused by the faster roll off of the frequency response near the edge of the operational bandwidth of the devices. **c)** Voltage-resistance curves for memristor (used in C_{Var}) readout for all 7 tests. **d)** Voltage-resistance curves for memristor (used in L_{Var}) readout for all 7 tests.

Test Results

Figure 4.3d shows the magnitude of two transfer functions measured in test 7 alongside an ideal curve. The response of the synthetic resonator closely matches that of an ideal RLC resonator up to frequencies of 100 kHz, where the transconductor frequency response introduces a divergence of experimental from theoretical behaviour. Measured resonant frequencies are within $\pm 5\%$ of the expected values (Figure 4.3e). Centre frequency estimation is accurate to about 3 kHz by direct observation, limited by the sampling rate of the FRA tool. Centre frequency estimation can be improved to 1 kHz by cubic interpolation (Figure 4.4a). Quality factors, estimated from the ratio of resonant frequency to 3 dB bandwidth ($Q = f_c / \Delta f_{3dB}$), are in close agreement to expected values (Figure 4.4b). The values are of the correct order of magnitude, however their precise values seem inflated in some instances. This is largely due to faster than 20dB/decade roll-off. The gain response is affected due to encroaching bandwidth of the PCBs. Results confirm this, as the biggest error in Q-measurement is seen in tests with highest resonance frequencies (Tests 2, 3 and 4), while tests with relatively low resonant frequency (Test 1, 5, 6 and 7) match the theory perfectly. In principle the quality factor and the resonant frequency

of an RLC setup can be both tuned independently, e.g. if both inductance and capacitance halve, the quality factor will remain unchanged, while resonant frequency will double:

$$Q = \frac{1}{R} \sqrt{\frac{L}{C}} \quad (4.15)$$

$$\omega_{Res} = \frac{1}{\sqrt{LC}} \quad (4.16)$$

It was found that memristance drift is largely attributable to charge injection: connecting and disconnecting the gyrator circuit to the probe-card which accesses the memristors induces a triboelectric charge. This is enough to offset the memristance by about 2% of its nominal value (Figure 4.4c-d). Retention tests with the memristors continuously connected to the impedance emulators show minimal drift when connected. The impedance emulation circuit is not, therefore, causing memristance drift. An electronic low charge injection switch will eliminate triboelectric charge injection.

Implications

The above allows to draw four conclusions. Firstly, as one might have expected adding more blocks in a straightforward configuration ultimately leads to further bandwidth decrease. Since the building blocks are essentially filters themselves, two such blocks double the roll off, hence shifting the corner frequency to a lower value.

Secondly, addition of multiple blocks leads to an interesting problem. Assuming the error in programming can be modelled as a Gaussian process, the more components there are in a circuit, the lower the absolute error, as ideally the individual contributions cancel out. This assumption neglects the fact that each component plays a different role in the circuit and thus the total error is not simply a function of quantity and distribution. If such approximation can hold as a first order simplification, then indeed the mean error decreases, however the full statistical spread increases from $\pm 5\%$ to $\pm 10\%$.

Thirdly, in a single active component the input voltage was already limited. As discussed in the results of RLC, the voltage for the circuit had to be limited to $\pm 0.5V$. The more components there are, in particular the more active blocks that are connected together, the more complicated is the definition of the input range. If identical blocks are connected together, then the input voltage range remains unchanged, as these are passive component simulators, so the voltage in most cases will drop across the component¹ The formal limit on input voltage is a function of the input current, as its the current that is gyrated into voltage. Subsequently the input

¹In resonance it is possible to exceed the input voltage. Charge pumps, though not purely passive, are often used to boost the voltage locally. However, here discussion revolves about majority of circuits.

current is limited by the load of the circuit. Therefore it is theoretically possible to connect many blocks in series, provided the load limits the current. Conversely a single active block may be saturated if the load connected to it is very small.

Finally, finishing on a positive note, the blocks demonstrate that their quality factor remains unaffected during operation. the closely match the desired theoretical values, and do not limit the performance of the RLC circuit. Clearly, what the above study is missing is the assessment of the maximum quality factor of a functional circuit. Results in chapter 2 give a good indication of what may be expected.

4.2.3 Two Active Elements: EEG Band Select

Theory and Benchmarks

Having shown that under certain conditions two elements do in fact work well together, the performance of the building blocks may be judged on a specific application, namely bio-signal filtering.

The techniques of the previous Chapter were used to synthesise large reactive impedances in order to implement an electronically adjustable electroencephalography (EEG) band select filter. EEG is the measurement of the electrical activity of the brain. Electrodes, placed on the scalp, record μV -level signals. These are conventionally classified by their frequency in the delta (sub 4Hz), theta (4-7Hz), alpha (8-12Hz), beta (12-30Hz) and gamma (30-100Hz) bands [2]. There is an increasing interest in developing non-clinical, wearable, EEG devices for the early detection of epilepsy, and also for monitoring of dementia and other cognitive degenerative diseases.

Current state-of-art [3] equipment has limited operational autonomy of typically 9 hours as a result of high power costs. The power limitations of wearable EEG hardware are the subject of intense research activity [4]–[6]. Analogue circuit level techniques, though, rarely cover the entire range EEG of frequencies, especially the lower frequencies. Sub-threshold MOS filters which have been used [4] for the lower frequency bands are limited both in dynamic range and reconfigurability to between 20 and 40Hz. Other reported results are frequently limited to simulations [7]. The filter reported here offers a significant improvement in performance metrics, such as power, area and reconfigurability over other implementations (Table 4.1).

Test Results

In Figure 4.5b the measured transfer function of the proposed band-pass filter at 4 different center frequency settings is shown. Figure 4.5c shows how the resistive states of the memristors

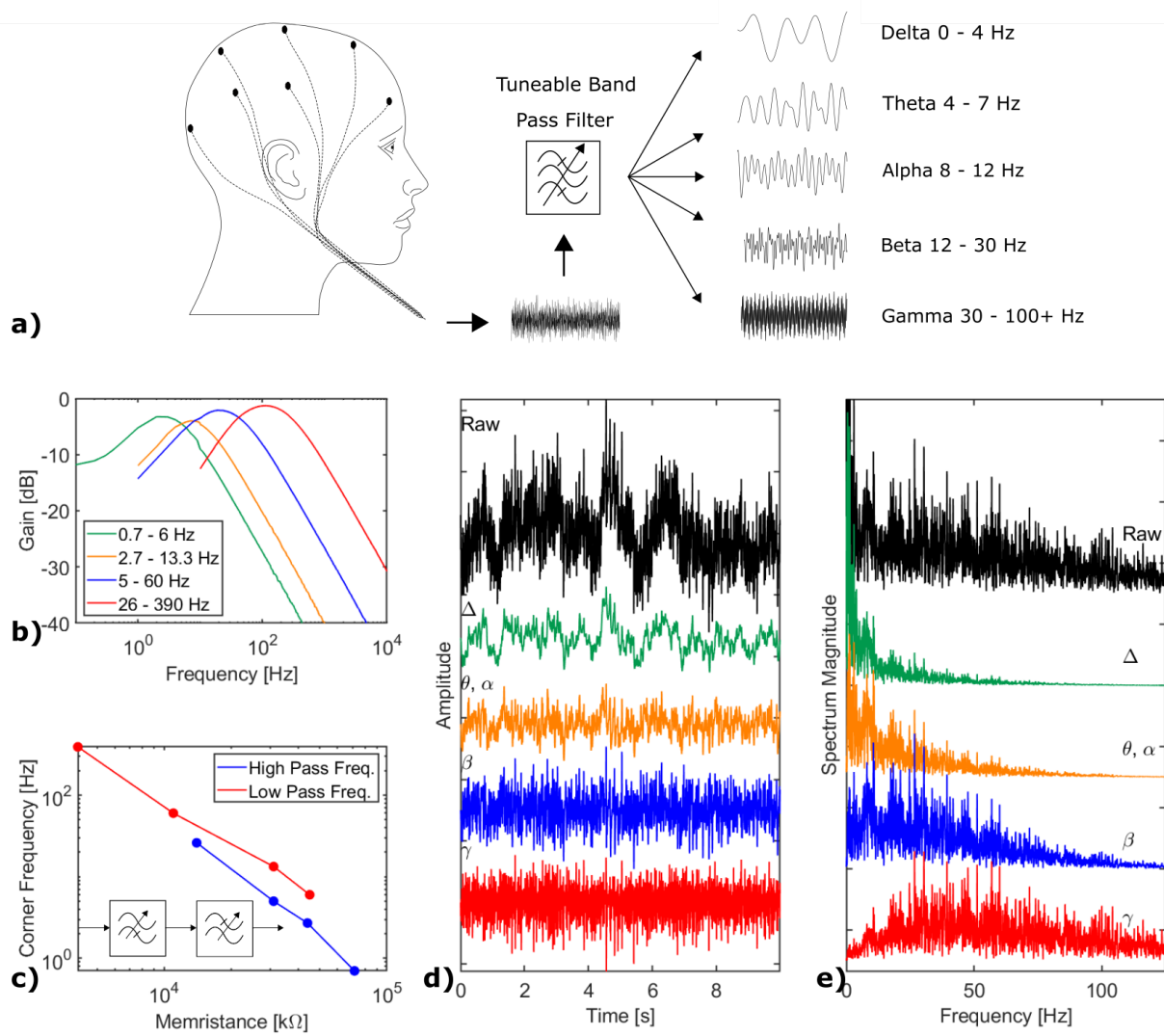


Figure 4.5: Using reconfigurable memristor-based filters for processing EEG signals: first order reconfigurable EEG band select front end filter. **a)** EEG signal band selection is a key data processing task of electroencephalography. **b)** Measured band-pass filter transfer characteristics at four different frequency settings: Cut-off frequencies can be adjusted from less than 1 Hz to nearly 400 Hz. **c)** Band-pass filter tuning details: The band-pass filter was realised using two, cascaded high and low pass filters (see inset) where the memristors were independently tuned in each block in order to set the high and low corner frequencies. **d)** Real EEG signal [1] (black trace) and outputs after processing through the band-pass filter, set with each of the four settings in panel (b). Trace colours correspond to different target frequency bands and correspond to those in panel (b). **e)** Frequency spectrum of the raw and filtered signals from panel (d), showing different EEG bands.

were used to independently control the high and low corner frequencies of the filter. These are first order low pass filters with the usual 20 dB per decade of roll-off. The high pass filter was realised using an RL network, where the resistor was shunt. Conversely, the low pass filter was realised with an RL network, where the inductor was shunt. The large ESR of the synthetic inductors causes the high pass filter behaviour to flatten out near DC. High pass filters could be tuned between 0.7 Hz and 26 Hz. Tuning the filters to higher frequencies is possible if lower

	Low Pass	High Pass	Gain	Power	Comment
Psychlab, EEG8	4 settings: from 40Hz to 10kHz	9 settings: from 0.01 to 30Hz	9 settings: from 46 to 106dB	Connected to mains power	Filters feature Bessel response
Frequency Devices, Model 950	6 settings: from 10Hz to 50kHz	6 settings: from 10Hz to 50kHz	3 settings: 0, 10, 20dB	Connected to mains power	Filters selection of Bessel or Butterworth
Lim et al.	Tuneable: from 20 to 40Hz	Fixed	5 settings: from 54 to 83.5dB	476 μ W at 2.65V supply	gm-based modulation using sub-threshold MOS
Saurabh et al.	N/A	As low as 10 mHz	N/A	4.48mW at 1.8V supply	Switched capacitor technique for realising large time constants
Lie et al.	3 settings: DC, 5.2 and 11Hz	Tuneable: 38 to 200 Hz	Dependent on filter choice: 20 to 92dB	4.74 μ W at 2V supply	Designed for ECG. Filters based on banks of capacitors; Gains affixed to filter selection
Synthetic Blocks	96 setting: from 6 to over 390Hz	96 setting: from 0.7 to over 26Hz	Not Implemented	PCB: up to 700mW at ± 15 V IC: μ W up to 2mW at 3.3V	Gain stage with 96 settings could be implemented with two gyrators in series

Table 4.1: Comparison table of configurable commercial EEG filters (in red) and researched techniques (blue), with the proposed memristor-based technique (green).

memristance values are used or the control current is scaled. Low pass corner frequencies were adjustable from 6 Hz to 390 Hz. Finally, measured data was used to construct computational filter models which were applied to an EEG signal data-set [1]. The raw EEG signal was successfully separated into 4 frequency bands as shown in Figure 4.5d-e. Faster roll-offs of the stop band can be achieved with higher order filters.

Such low cut off frequencies of the filters used were made possible through changing of the gyrator bias and synthesising 50H inductors. The gyration constant K is inversely proportional to the diode bias current (I_D) of the operational transconductance amplifier used to construct the gyrators [8]. It's origin is purely ascribed to the architecture of the OTA used. Please see the referenced datasheet for more clarification. Increase of I_D results in smaller value of K (defined as the ratio of the output current of the OTA I_{Out} to the input voltage). Subsequently the diode current was increased 10 times:

$$I_{Out} = I_S \frac{2I_{ABC}}{I_D}, \quad \text{for } |I_S| < \frac{I_D}{2} \quad (4.17)$$

This however had an adverse affect on the bandwidth of the system as leakage currents were now proportional to bias currents at much lower frequencies. However, since the filter was used to extract low frequencies, the bandwidth limitation did not affect its performance. Moreover, with decreased diode bias current and with increased gyration constant the circuit resulted *for free* in a much reduced power consumption.

For the purposes of power performance assessment it should be noted that the PCB-based circuits presented here have a significantly higher power dissipation compared to what would be achievable on-chip. For that reason, integrated circuit versions of these filters were simulated in a commercially available 180nm CMOS process. This yielded a peak power dissipation of 2mW (Appendix C), demonstrating that they are suitable for battery operation. Current state-of-art analogue low frequency filters can in fact operate at nW [9] level. These systems, however, lack

reconfigurability and have a further reduced voltage overhead. Furthermore, the memristors used as tuning elements in this realisation make continuous, precise, and non volatile control of the cut-off frequency possible. Additionally, at the system level the need for high data-rate data converters operating with high temporal resolution (i.e. high sampling rate) is eliminated, resulting in lower circuit complexity and further efficiencies.

Implications

It may seem that delicate applications can be handled with gyrator-based building blocks. However, to fully demonstrate the utility of the synthetic blocks a higher order, faster roll-off filter would have to be built. There are however limitations to the performance that can be achieved.

Firstly, as demonstrated and explained relatively large ESR of the synthetic inductor greatly limits the low frequency response. This allows to change the earlier behaviour definition of the building blocks: these are in fact bandpass filters rather than low pass. the ESR demonstrates itself twofold in the results - with gain flattening towards the DC level and through sub-0dB bandpass gain.

Secondly, adding more blocks will inevitably lead to instability of the circuit. Already with two components it was relatively easy to set the filter into oscillation, by bringing an ungrounded hand close to the circuit. Therefore higher order filter would have to be designed not as standalone blocks but together, thus removing the idea that they can be used as *Lego*-like building blocks or as drop-in circuit element replacements.

On a positive note, the tests have shown that it is simple to change the component value range, by simply tuning the bias conditions. In principle this could be implemented with memristors as well, giving truly large range from as little as 1mH to 50H (value ratio of 5000).

4.2.4 Parametric Tuning: Variable Gain Amplifier

One of key universal and ubiquitous elements in system design are variable gain amplifiers (VGA). As mentioned earlier, an amplifier is simply a low pass filter with high passband gain. They are used to adjust dynamic range of long chains of systems by tuning the signal amplitude. VGAs are commonly used in communication systems, where the signal amplitude varies between base stations and hence must be adjusted to optimise the signal strength at the point of interest. Another major application space for VGAs is the music industry - particularly on music consoles, allowing to controllably boost selected audio frequencies.

VGAs come in two flavours - digitally and continuously controlled. Digitally controlled VGAs realise discrete gain levels, e.g. through built-in selectable pool of feedback resistors. So-called

analogue controlled VGAs provide the designer with a voltage control pin, where externally generated reference voltage level tunes the VGA biases, thus synthesising continued range of gain levels. the limitation arises in realising reference voltage levels, as data converters are inherently discrete, power-hungry and do not scale very well. Hence memristor based approaches can in theory lead to smaller footprints and increased efficiency.

Circuit Analysis

The circuit shown in Figure 4.6 realises a single ended input to differential output memristor controlled variable gain amplifier. The circuit can be decomposed into three constituent parts: memristor gain control, a Gilbert cell and a 3 stage transimpedance amplifier.

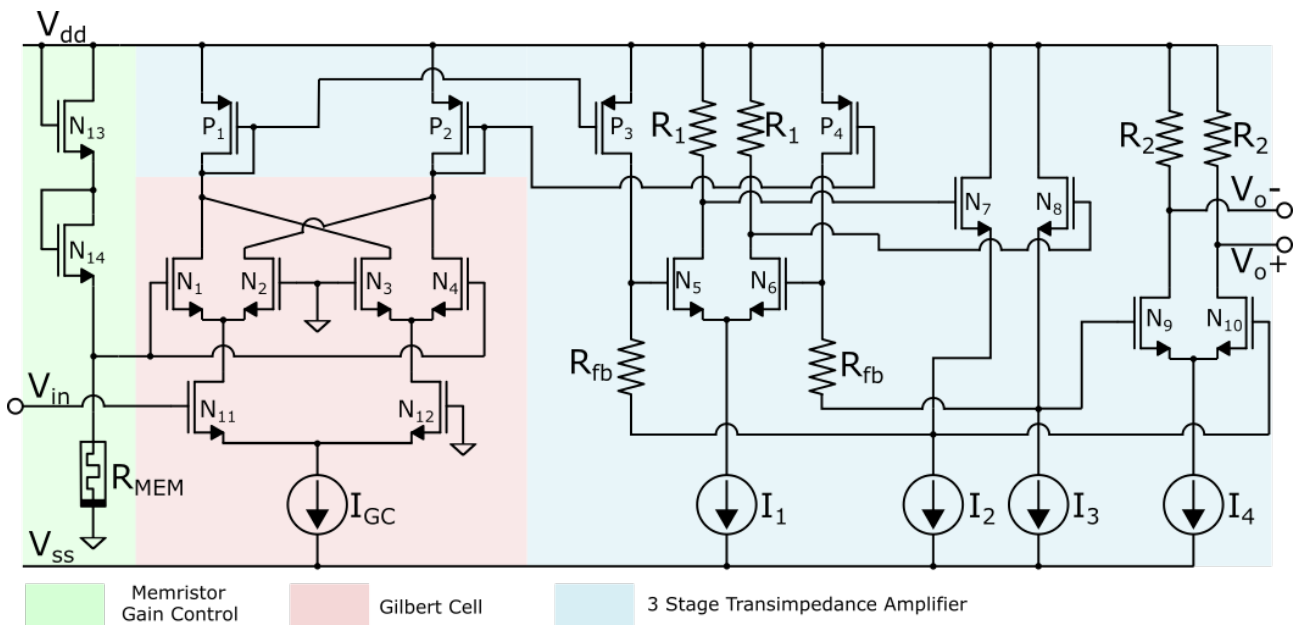


Figure 4.6: Circuit schematic of the 250MHz memristor-controlled variable gain amplifier.

Memristor Gain Control (MGC): Similarly to most commercial VGAs the gain control is effectively realised through control of the reference voltage. Instead of using an expensive data converter, an inexpensive memristor controlled current source is used. Two diode connected transistors are used as active load, to step down the rail voltage to subthreshold value as to prevent memristive switching. The precise value of the voltage is then adjusted through memristive programming. The circuit is designed such that practical values of the memristor can be used: $1\text{k}\Omega$ - $100\text{k}\Omega$.

Gilbert Cell: A classic four-quadrant multiplier [10] is used at the centre of the proposed VGA. A differential input to transistors N1-4 is affixed to the output of the memristor controlled voltage reference. High input impedance of the N1-4 network, renders the MGC with high and variable output impedance suitable for this purpose. The second differential input (N11-12), made into single-ended, is the entry port for signals. The cell is biased through current

sink I_{GC} . The Gilbert Cell produces differential output currents which are flowing through transistors P1-2.

Three Stage Transimpedance Amplifier (3S-TIA): The input into the three stage design [11] is provided through the current mirrors located at the outputs of the Gilbert Cell (transistors P1-4). The currents are fed into feedback resistors R_{fb} . The first stage is composed of transistors N5-6 and resistors R_1 . The voltage output of the first stage is then used to drive the second stage (transistors N7-8), which is effectively a buffer (voltage follower), isolating input stage from the output. The two stages are balanced through the bias currents I1-3, the output currents of the Gilbert Cell and the output currents of the second stage. The resulting voltage at the output of the second stage is used to drive the third and final stage - a common source amplifier biased through I4, and loaded with resistors R_2 .

Parameter	Value	Parameter	Value	Parameter	Value
N1-6/9-12 Length	$0.6\mu\text{m}$	N11-12 Width	$0.5\mu\text{m}$	R_2	$500\text{k}\Omega$
N7-8 Length	$2\mu\text{m}$	N13/14 Width	$0.2\mu\text{m}$	R_{fb}	$1\text{M}\Omega$
N13/14 Length	$2.5\mu\text{m}$	P1-4 Length	$0.6\mu\text{m}$	I_{GC}	$5\mu\text{A}$
N1-4 Width	$0.22\mu\text{m}$	P1-4 Width	$0.3\mu\text{m}$	I_1	$1\mu\text{A}$
N5-8 Width	$0.3\mu\text{m}$	R_{Mem}	$1\text{k}-100\text{k}\Omega$	I_{2-3}	$20\mu\text{A}$
N9-10 Width	$1\mu\text{m}$	R_1	$630\text{k}\Omega$	I_4	$7.95\mu\text{A}$

Table 4.2: Design parameters of the memristor controlled 250MHz VGA.

Results

Table 4.2 shows the component parameters used to simulate the circuit. The component value selection was done through iterative optimisation using SPICE software. The circuit was simulated using TSMC180nm technology and using standard 5V tolerant CMOS devices available. The circuit was powered through $\pm 5\text{V}$ rails. The summary of the results is presented in Figure 4.7.

The VGA exhibits nearly 50dB of signal amplification at the highest memristive setting. As memristance decreases, the reference voltage reduces and subsequently the transconductance of the Gilbert Cells falls. As a result a drop in gain is observed. A relatively linear relationship is observed between memristance and absolute gain (measured in V/V), which translates into an exponential dependence when measured in decibels, as seen in plot c. At around $40\text{k}\Omega$ the

gain sensitivity begins to drop, resulting in eventually in a plateau which describes the absolute limit on the gain of the VGA.

Interestingly, the VGA's bandwidth is gain-agnostic as opposed to standard amplifiers, which usually are subject to a form of gain-bandwidth product constraint. This realisation benefits from constant DC to 250MHz operational frequency range (plot a). This comes as a result of slight inductive peaking, introduced at the output of the Gilbert Cell. Sometimes, physical inductors of very small values are introduced in series with transistors P1 and P2 to achieve marginal Q-enhancement around the corner frequency. Alternative methods include active simulation of inductive loads around the frequency of interest usually with 2 transistors and a resistor. Here a current mirror together with the first TIA stage result in a slightly inductive input impedance, which overall enhance the Q at around 200-250MHz mark.

The enhancement can be clearly seen in the phase response. Phase drops more quickly than in the usual single pole amplifier, demonstrating higher order transfer function around the cut-off point. This is confirmed by the gain roll-off which was measured to be around 80dB per decade, suggesting the system behaves like a fourth order filter.

Despite the higher order inductive-capacitive behaviour and the Q enhancement the amplifier is stable, as seen in Figure 4.7d. Applying a 5ps rise time 1mV step function to the input of the VGA results in stable response. Some overshoot is seen, however there is just a single cycle of oscillation. The frequency of the oscillation is found to be approximately 300MHz, which approximately matches the frequency at which the Q-enhancement is located. The measurement is limited by the time scale resolution. The overshoot based on simulations is estimated to be 20% at all settings, while the settling time is 2ns throughout.

From the perspective of memristance usage, the voltage across the memristor throughout remains below switching threshold: 9.2mV at 1k Ω , and 651mV at 100k Ω . Consequently the current through the memristor ranges from 6.51 μ A to 9.2 μ A. Furthermore, the mem-device is fully isolated from the signal path, resulting in constant DC bias across the device.

Finally the proposed memristor controlled 3S-TIA dissipates between 572 μ W to 586 μ W depending on the memristance. While this technique trails behind state-of-the-art VGA in areas such as power consumption or bandwidth, this method offers full continuity in time and tuning range. Furthermore, replicating the circuit with a smaller technology node, can in theory lead to increased bandwidth as well as reduced power, since bias currents involved will scale down.

Implications

First of all, to address the obvious - these are idealised simulations based on a perfectly non-volatile memristor. Nonetheless, building upon results from previous experiments, the operational conditions for the memristor, namely its position in the circuit as well as potentials

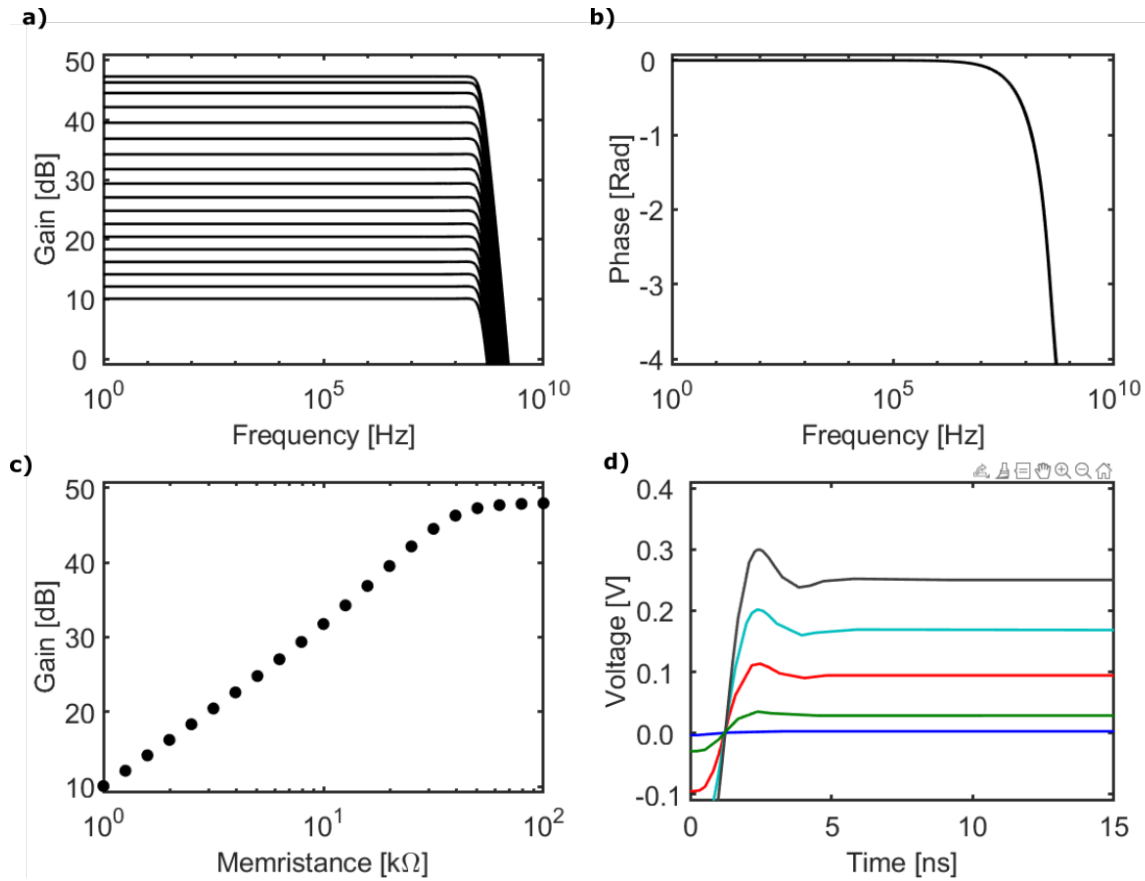


Figure 4.7: SPICE simulation results of the memristor controlled VGA using TSMC180nm technology. **a)** Gain of the VGA spanning memristances from $1\text{k}\Omega$ to $100\text{k}\Omega$. **b)** Complimentary phase response. The phase remains identical at all gain settings. **c)** Mean low frequency gain versus memristive setting. Towards $100\text{k}\Omega$ settings, gain begins to plateau. **d)** Step response of the VGA at various gain levels demonstrating stability of the system. Input step with amplitude of 1mV was applied.

across it, and the desired memristance values are in accordance with previous observations of what is achievable.

This method, while it does not utilise a synthetic block, effectively presents identical control mechanism. Single memristor performs the tuning of the systems functionality. In that aspect it removes the redundancy of synthesising an intermediate function (reactance for example), which is then used to generate the response of choice (e.g. low pass filter). It is therefore expected, as confirmed by the simulations, the an IC realisation of such an amplifier will be superior to a counterpart driven by variable reactance blocks.

Having said that, this is not a generic approach. The benefit of the building block approach is that the constituent components can be easily re-purposed for other applications. Using the direct approach, mean committing to the architecture. removing that layer of functional reconfiguration, leaving simply parametric tuning.

4.2.5 Functional Tuning: Biquadratic Filter

Theory

The lack of functional reconfiguration of the above approach can be rectified by implementing more complex architectures such as those of biquadratic filters. The topology quite easily allows to implement functional changes to the response by tailoring the respective filter coefficients. Analogue biquadratic filter is a circuit level implementation of the classic digital infinite impulse response filter, or IIR, with two feedforward and two feedback coefficients. Often the biquadratic filter is further simplified into a commonly used topology, e.g. Tow-Thomas or Kerwin–Huelsman–Newcomb filters.

Practically what the filter allows to achieve is functional reconfiguration of the frequency response - the filter can be designed as either low pass, high pass, band pass, band stop or all pass filter. Moreover it carries the parametric tuning capability with is as well, as it allows to tailor the corner frequencies for any of the above functional realisations.

The filter realisation is presented in Figure 4.8. Individual transconductor (Gm-cell) is a simple long tail pair based amplifier, where the current difference between the two legs forms the output current. The magnitude of transconductance is controlled through a control voltage applied to transistor N7. Eight such Gm-cells allows to build an analogue version of the classical digital IIR filter. 5 Gm-cells realise coefficients a_{0-2} and b_{0-1} , 2 realise integrators (with capacitor at the output), and an input Gm-cells (optional) simply converts the input voltage into input current. Output current is then converted into output voltage through a load resistor. The magnitude of the coefficients can be easily controlled with memristor tuned voltage reference as it was done in Figure 4.6.

The above circuit is characterised by the following transfer function:

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = G \frac{a_2 s^2 + a_1 s + a_0}{s^2 + b_1 s + b_0} \quad (4.18)$$

- where G is a circuit and bias dependent gain. The transconductor parameters as well as biquadratic filter component values are presented in Table 4.3.

Results

The idea, albeit not novel, rarely is seen in analogue electronics literature. More often the simplified versions of the biquad are used (mentioned earlier). The digital equivalent is ubiquitous.

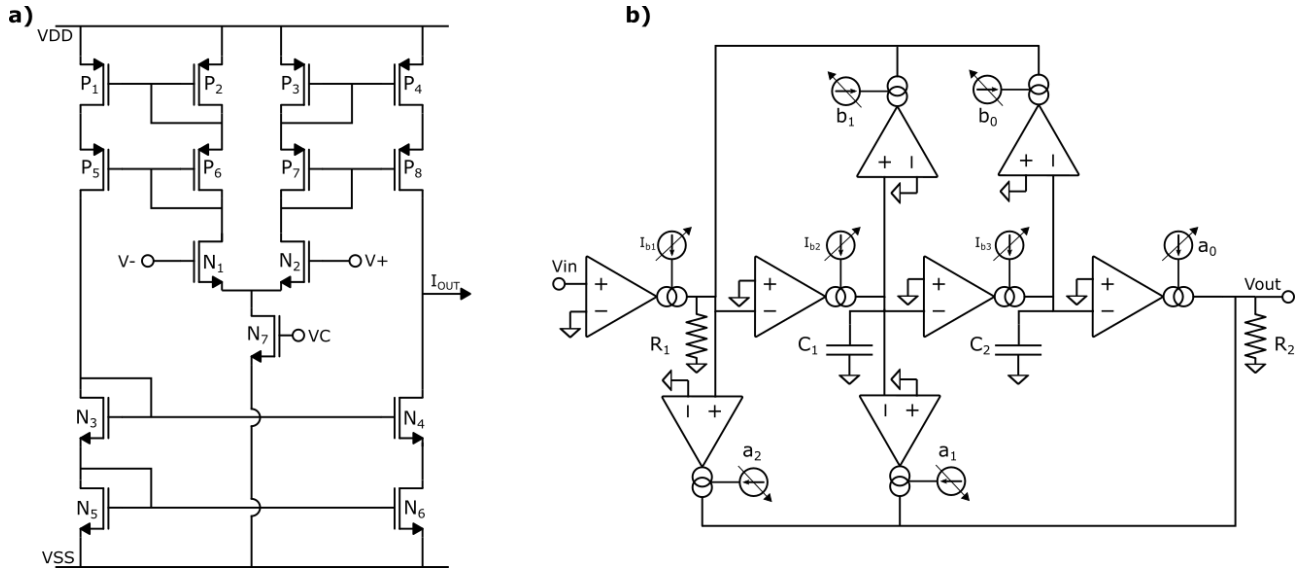


Figure 4.8: Analogue biquadratic filter design using TSMC180 technology. **a)** Transistor level transconductor design. The magnitude of transconductance is controlled through control voltage Vc. **b)** High level biquadratic filter design, using the transconductor as building block. Individual coefficients a_{0-2} and b_{0-1} are controlled through voltage controlled current sources.

This can be primarily attributed to large analogue complexity, which is evident from the design above - it requires at least 7 and in some cases 8 transconductor elements.

Nonetheless, it forms a great platform to demonstrate the usefulness of memristor tuning in fundamental functional reconfiguration, without needing to synthesise intermediate functions such as reactance. From theory it is known that controlling the coefficient values can allow to generate virtually any second order filter response. Here four responses are presented - low pass, bandpass, notch and bandwidth limited all pass filters.

Results in Figure 4.9 show that simply through reference voltage tuning, it is possible to carry out functional tuning of the biquad filter. For example to realise a low pass filter (subplot a):

$$H_{LPF}(s) = G \frac{a_0}{s^2 + b_1 s + b_0} \quad (4.19)$$

, both a_2 and a_1 must be *switched off*. This is realised with simply supplying maximum negative bias to the VCCS emulating the respective coefficient. Other coefficients can be freely tuned to set the desired quality factor and cut off frequency.

The same process may be followed for other topologies. Importantly, the control voltages can be easily supplied through memristor controlled current sources. This ensures that the memristor is not reprogrammed during operation and eliminates the need for eight independent data converters, which would otherwise be needed to parametrically and functionally tune the circuit.

Parameter	Value	Parameter	Value	Parameter	Value
N1-6 Length	$0.6\mu\text{m}$	P1-8 Length	$0.6\mu\text{m}$	V(Ib1)	-3.5V
N7 Length	$5\mu\text{m}$	P1-8 Width	$0.75\mu\text{m}$	V(Ib2)	-3V
N1-2 Width	$1.2\mu\text{m}$	R1	100k Ω	V(Ib3)	-3V
N3-6 Width	$0.75\mu\text{m}$	R2	10k Ω	Vdd	5V
N7 Width	$10\mu\text{m}$	C1	100pF	Vss	-5V
N9-10 Width	$1\mu\text{m}$	C2	100pF		

Table 4.3: List of design parameters for the analogue biquadratic filter.

The circuit was designed with TSMC 180nm exhibits 250MHz of bandwidth. The power consumption varies depending on the function realised. The larger the value of specific coefficient, the larger the current draw of that particular Gm-cell. The power is bounded by two limiting cases: when all coefficients are off (i.e. set to 0 through -5V control biases) and when all coefficients are maximally on (here saturation is assumed to be around -2.5V). The bounding power draws are then $510\mu\text{W}$ (with turned down integrator Gm-Cells) and 41.6mW (with maximum integrator gain). This is the price to be paid for functional reconfiguration (not mentioning the energy required to reconfigure the memristor themselves).

Implications

The implication of the above is quite substantial. To achieve functional reconfiguration, it is not required to rearrange, reconnect and generally change the circuit layout. This can be achieved already on the circuit level, with memristor controlled switches. While conceptually the feedback and feedforward Gm-cell realise coefficients, functionally they are simply glorified analogue switches. Hence by introducing a redundancy in the design and providing the means to switch individual blocks in and out in an analogue fashion, it is possible to synthesise different circuit topologies, while not changing the circuit itself.

4.2.6 Comments

To tie all of the above together, five different filter topologies were presented. Three of them were implemented with reconfigurable blocks. The three experiments revealed that a discrete form maximum of two concurrent blocks may be used at once. Adding more blocks, will lead to instability. The experiments with two blocks were difficult to carry out - upon powering up the boards, the circuits could naturally enter oscillatory mode. Sometimes, multiple attempts

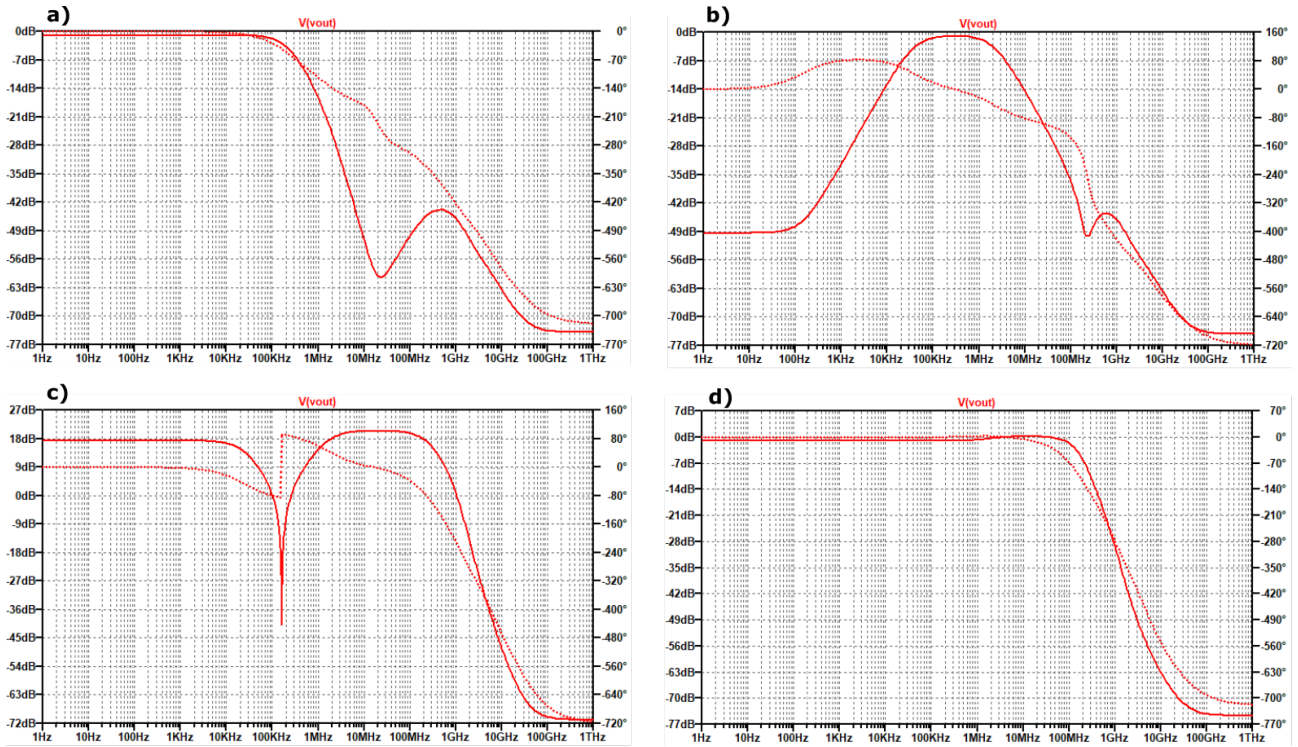


Figure 4.9: Biquadratic filter topologies realised through memristor controlled voltage tuning.

a) Low pass filter. $V(a_0) = -3.5\text{V}$, $V(a_1) = -5\text{V}$, $V(a_2) = -5\text{V}$, $V(b_0) = -3.5\text{V}$, $V(b_1) = -3.5\text{V}$. **b)** Band pass filter. $V(a_0) = -5\text{V}$, $V(a_1) = -3\text{V}$, $V(a_2) = -5\text{V}$, $V(b_0) = -4\text{V}$, $V(b_1) = -3\text{V}$. **c)** Notch filter. $V(a_0) = -3.5\text{V}$, $V(a_1) = -5\text{V}$, $V(a_2) = -3\text{V}$, $V(b_0) = -4.1\text{V}$, $V(b_1) = -3.5\text{V}$. **d)** All pass filter. $V(a_0) = -3.5\text{V}$, $V(a_1) = -3\text{V}$, $V(a_2) = -4.1\text{V}$, $V(b_0) = -3.5\text{V}$, $V(b_1) = -3\text{V}$.

at powering up the boards had to be made in order to avoid instability. Looking back, adding a large capacitor between each rail and ground would allow to achieve the same, as the power up would be less abrupt, decreasing the instantaneous high frequency signal passing through the circuit.

As a side effect of multiple power up/power down procedure, there was a slight drift of memristance. This could have been due to larger charge injection upon power up, than the device experiences at constant DC supply. Hence some of the error in the measurements could have been avoided with a more careful power supply decoupling.

The two additional experiments - the VGA and the biquadratic filter - were purely theoretical, using widely available models of memristors, together with a TSMC Spice library. The approaches presented show alternative methods of achieving the same goal, i.e. realising filters, at a fraction of the cost and with immensely greater circuit properties, such as power consumption, bandwidth to name a few. Memristors were used in exactly the same fashion as in the building blocks, they merely control the current bias, however the avoidance of large gain elements and multiple feedback topologies greatly increases the stability margins and simplifies the implementation in system design.

The immediate drawback is that the circuit loses its modularity - the blocks are designed for one purpose only: to filter the signals. Building blocks from Chapter 3 give the advantage of synthesising virtually anything, with the help of an appropriate platform such as Field Programmable Analogue Array (see Chapter 5 for the discussion).

4.3 Waveform Generators

Moving forward, other applications, particularly those resulting in high bandwidth signals, are of interest. Design of a relatively high frequency systems with the building blocks allows to appreciate the system stability as the input and output are driven. One example of this is presented here and contrasted against an alternative approach based on memcapacitors.

4.3.1 Two Buffered Active Elements: Ring Oscillator

Theory

Ring oscillators (ROs) are used to build voltage controlled oscillators (VCO). Because of their high jitter, they are also used to generate random numbers (TRNG). Fixed frequency ring oscillators are often used as process control monitor (PCM) devices in order to determine and quantify silicon process variations and tolerances. It is therefore used as a diagnostic tool, with output frequency distribution informing of temperature variations and fabrication imperfections. Analogue tunable ring oscillators have not been pursued extensively in literature and as such there is a lack of demonstrated application space. This is due to large complexity required in tuning ROs and comparably simpler reconfiguration techniques when using VCOs.

A classical ring oscillator is a network of odd number of inverters that loop back onto themselves. Conventionally, these oscillators are used as static waveform generators. Recently, some work on FPGAs was performed showing how to dynamically tune the oscillator by clocking the inverters and dynamically changing their number to synthesise higher and lower frequencies [12].

In principle, inverters alone suffice to realise an oscillator. However tunability then can only be realised by changing the geometry of the inverters used, e.g. through a bank of varying NOT gates. Each geometry results in slightly different propagation delay, thus modulating the output frequency. Conventionally, tunability of the ring oscillators is achieved through embedded low pass filters between the inverting stages. These hardware filters are however either fixed or tuned through a bank of replacement components, allowing to adjust the frequency into discrete predetermined values. This method however consumes space and introduces redundancy - most

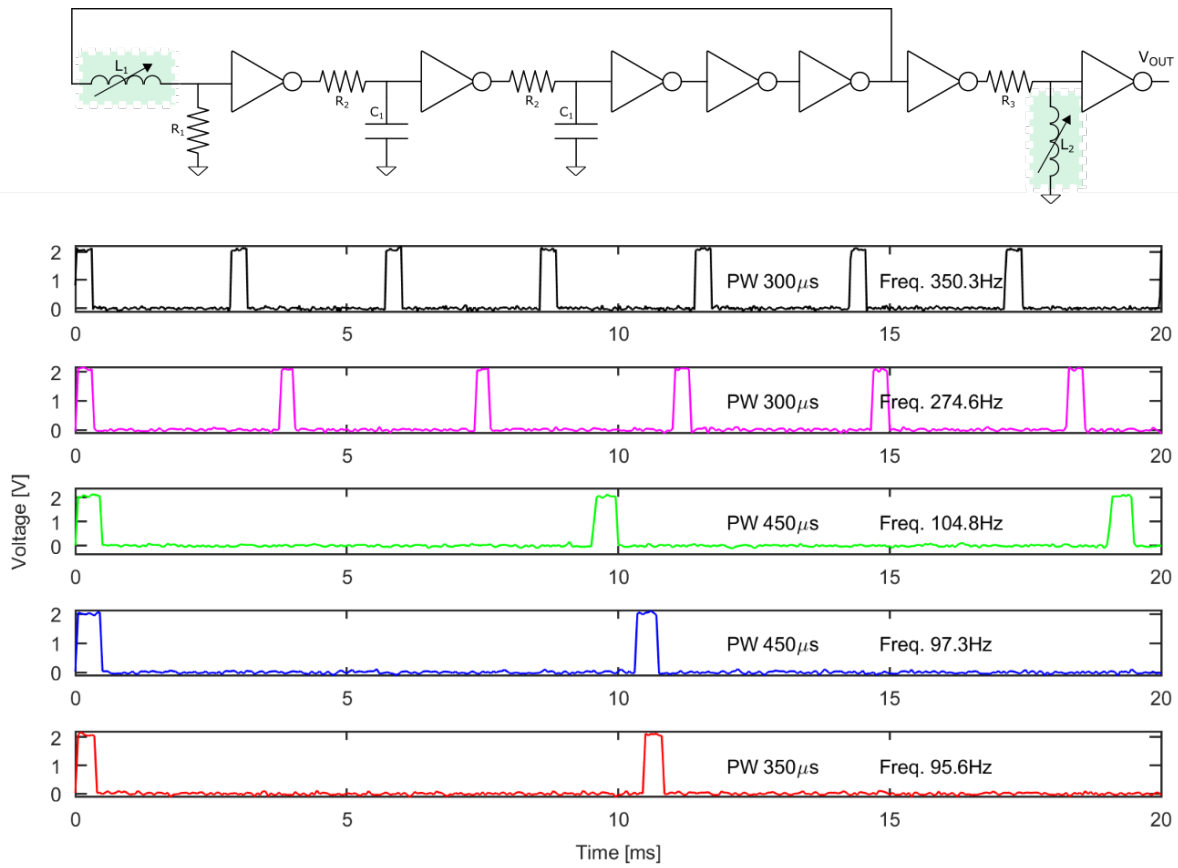


Figure 4.10: Low frequency controlled duty cycle and period ring oscillator. Top figure shows the reconfigurable ring oscillator, whose frequency and duty cycle are tuned through inductors L_1 and L_2 . Bottom plot shows the output of the ring oscillator at various memristance settings. A frequency range of 95 to 350Hz is demonstrated. However the true range can in fact be larger by exploiting more extreme memristive states. Pulse widths realised span the range from 300 to 450 μ s.

of the elements in the banks are unused during operation. This is addressed with continuously tuned building blocks presented in the previous Chapter.

VCO design can be greatly simplified by tuning the frequency at source, while the circuit complexity of the RO remains effectively the same, when employing tunable inductors. The large vast range of time constants allows to synthesise frequencies in the range from sub-hertz all the way to MHz region with the integrated circuit realisation. Therefore tuning can be then carried out through memristance programming rather than through data converters, which restrict the implementations to discrete values and do not scale well for large systems.

Use Case for EMS

Tunable oscillators lend themselves as control units in medical care such as in electrical muscle stimulation (EMS) protocols. It has been found [13] that sedated or intubated patients who stay long periods in the intensive care unit lose muscle strength and muscle mass as a result.

The group has shown that in the first two weeks of immobilisation, patients lose on average 10% of the muscle circumference in their legs. The group has subsequently shown that an EMS protocol which applies electrical pulses at varying frequencies and duty cycles can actually stop and reverse muscle atrophy. The pilot study revealed that on average the patients recorded an increase in their muscle circumference of 8-9% in the first two weeks.

The drawback is that the bedside apparatus required is usually corded and powered through mains. In principle the system can be designed as a wearable, allowing those who don't require constant hospital attention to continue the recovery at home. As such a tunable ring oscillator, which allows to control both the frequency and the pulse width is presented in Figure 4.10. The frequency control is achieved through control of the inductive low pass filter realised with L_1 . The pulse width is controlled through a differentiator seen at the output of the ring oscillator L_2 .

The frequency range can in principle be adjusted through the fixed RC low pass filters seen in the network, e.g. the range can be pushed to 1-100 Hz by increasing their time constants. Similarly, the range of pulse widths can be shifted by changing the value of the resistor. However, due to ever present ESR there is always a limit on the realisable pulse width for a given series resistor. It can consequently lead to change in behaviour, if the selected series resistor is of the same order of magnitude as the ESR, the differentiator will additionally attenuate the signal, causing the circuit to output constant value.

In this realisation the following dependencies are present: as memristance increases, synthetic inductance increases, reducing the corner frequency, increasing the resulting pulse width. Therefore narrow pulses require small memristances. There is however a limit to memristance scaling, as its ESR will dominate. This problem however can be tuned into the limit on the maximum realisable pulse width, by introducing one more inverter at the output, consequently changing the dependency that as memristance increases, it reduces the pulse width.

Implications

The two elements in the above setup were kept separate and properly isolated. This as expected resulted in a very stable setup. The blocks were resilient to ambient noise, and did not enter oscillatory behaviour as it was the case with joint building blocks. Furthermore, even though the signals generated had relatively fast edges, compared to the capabilities of the building blocks, the use of fast inverter at the output removes the effect of limited bandwidth of the blocks. All in all, the key takeaway of the ring oscillator demonstration is that multiple blocks can be safely used so long they are mutually isolated.

4.3.2 Alternative Approach: Linear-Logarithmic Monostable Nanosecond Multivibrator

Theory

Monostable multivibrators are used as timing circuits, clock frequency multipliers, they are also often found in repeaters restoring distorted pulses in signal paths. However, the lack of electronic control mechanism makes this an unattractive method for complex signal processing circuitry or precise instrumentation. By enabling the tunability of the multivibrator's response, it is possible to pave the road for many fascinating application, such as computational blocks, logarithmic amplifiers, spiking neurons or memcapacitance readout systems. Early interest into tuned monostable multivibrators came in the late 1960's and early 1970's with various degrees of success [14], [15]. Due to the emerging CMOS technology and ubiquitous application specific integrated circuits (ASIC), large multi-amplifier solution became impractical in today's technology. More recent efforts involve electronic current-mode control methods [16]–[18], however the results published allow for relatively slow pulse generation.

Many low-complexity monostable multivibrator designs are based on an RC discharge [19]. This approach doesn't translate well to practical tunable systems, as electronically variable capacitors and resistors are cumbersome to realise, integrate and tune accurately: frequent solutions include PN junction devices, micro-electro-mechanical-systems (MEMS) or impedance synthesis. This has recently changed with the reintroduction of memristive devices and an observation of simultaneous memcapacitive effects [20].

The memristor-centred research has enabled the development of neuromorphic architectures through the advancement of reconfigurable systems, which allow for bio-inspired synthesis of circuits and signals. Realisation of reconfigurable pulse generator enables time domain in-memory computation, simple PWM generation or analog encoding.

Coupled Memristive and Memcapacitive Behaviour

The coupled memristive and memcapacitive effect has been observed in metal-insulator-metal (MIM) structures [21] by Qingjiang et al. While its origin is not thoroughly understood, a phenomenological model was derived. Since then other groups have produced similar results in various materials, e.g. organic stacks or perovskites, showing that memcapacitance is inherently tangled with memristance (see Chapter 2 for more information).

Qingjiang et al. provide the empirical models of both the resistive and capacitive switching on a single device. However, the consequences of the phenomenon are not further explored. The resistive switching model is based on the classic Strukov function with a single state variable

x , whose behaviour is described by equations E.1-E.2. Prodromakis window function - $f(x)$ - was shown to represent switching most accurately.

$$\frac{dx}{dt} = ki(t)f(x) \quad (4.20)$$

$$k = \frac{\mu_v R_{On}}{T^2} \quad (4.21)$$

R_{Off} and R_{On} represent resistive switching limits of the device. The instantaneous value of the resistance is dictated by the state variable x , which takes any value between 0 and 1. It is defined by equation 1, where $i(t)$ is the input current over time. The proportionality constant k , defined by ion mobility μ_v , R_{On} and the insulator thickness T , represents devices responsiveness to applied stimuli.

Similarly for memcapacitors, the C_{On} capacitance is defined as minimum, while C_{Off} as maximum possible value the device can take. The definition of x remains unchanged. The value of k was estimated numerically. The same window function is used as before.

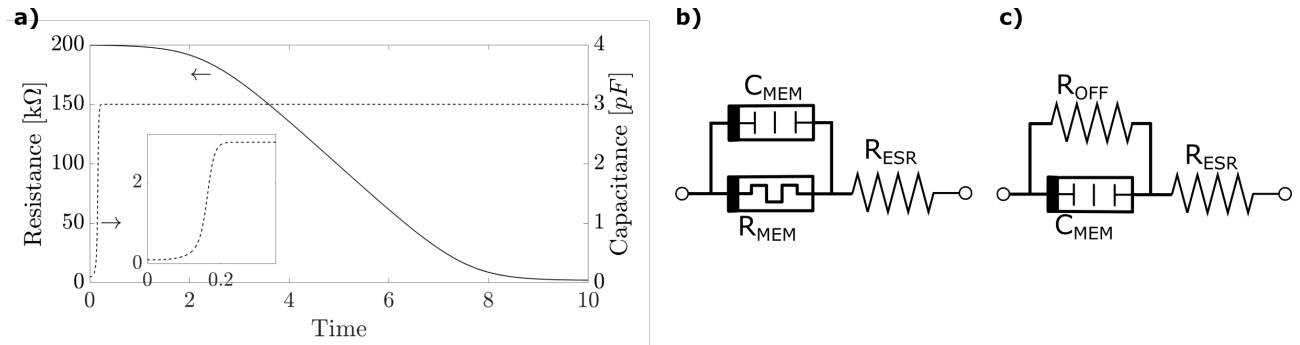


Figure 4.11: Reported memcapacitive switching in MIM devices. **a)** Coupled resistive (solid line) and capacitive (dotted line) switching on a single device. The time axis is arbitrary and depends on the magnitude of the applied stimulus. This representation of the model was simulated by applying a constant DC current. **b)** Memristor equivalent circuit: full behavioural model described by Qingjiang et al. **c)** Extracted model in the variable capacitance region.

The reported resistive model parameters are: $R_{On} = 2k\Omega$, $R_{Off} = 200k\Omega$, $T = 10nm$ and $\mu_v = 10^{-14}m^2V^{-1}s^{-1}$. The value of k was calculated to be $2 \times 10^5 A^{-1}s^{-1}$. In case of the memcapacitor the parameters assume the following values: $C_{Off} = 3 \times 10^{-12}$, $C_{On} = 10^{-13}$ and $k = 10^7$.

The precise values of the 'on' and 'off' resistances and capacitances are in fact of little significance. What is more important is how quickly the device can span its entire range of values. For each switching phenomenon this is dictated by its respective k constant, as both the window function and input current in equation 1 are equal. The model suggests that capacitive switching is about 50 times more responsive.

Practical implications of dissimilar switching rates on a single device are significant. They imply that the device can undergo full capacitive switching while retaining its high resistive state (Figure 4.11a). The device changes its operation from a lossy memcapacitor to a low speed memristor and vice-versa. The precision component analyser results confirmed that the device can be modelled as a lossy capacitor with some equivalent series resistance (ESR) (Figure 4.11b). When the device is operated in its capacitive switching region, the parallel resistance is assumed constant (Figure 4.11c). Classic impedance scaling techniques can be used to multiply the capacitance if needed, such as gyrator-based amplification or more direct techniques such as those presented in [22], [23]. Switching the device within its variable capacitance region, enables the synthesis of memcapacitive behaviour.

Implementation and Design Considerations

The circuit is designed as a monostable multivibrator, with the ability to trigger at both falling or rising edge. The architecture is complete with just two blocks - a delay unit and a XOR gate. The input signal is split; its original and delayed copies are compared, and a pulse equal to the delay is generated. The design is feasible with small technology node integrated circuit processes - memcapacitive effect must dominate the parasitic gate capacitance. Lack of amplifiers in the design and subsequently lack of Miller capacitance enables the full use of memcapacitor's range. High level block design is shown in Figure 4.12a.

XOR delays are diminished with a 3T architecture [24]. Although, this XOR configuration benefits from just a single transistor delay, the design suffers from glitches, which can be partially addressed by careful tailoring of W/L ratios [25]. However, a much safer approach is to use a standard 8T architecture [26].

The main delay unit is shown in Figure 4.12b. The variable capacitance model presented in Figure 4.11c is used to control the RC time constant of low pass filter. The second memristor is used to set the threshold voltage on the comparator to restore the pulse shape.

The grounded memcapacitor is used directly in the signal path. If the logic level is unrestricted this will cause the device to drift and quite likely exit the variable capacitance region and enter variable resistance mode. Care must therefore be taken to ensure that sub-threshold potential is applied across the device.

The design could be realised with fixed capacitor and a series memristor, however it adds extra complexity to the design. To program the device, mem-element needs to connect to a programming circuit. A grounded memcapacitor requires a single connection, while floating memristor requires both terminals to switch. Furthermore a grounded memcapacitor is less likely to be reprogrammed by parasitic inductive spiking or ESD, than a floating memristor, as only one terminal is susceptible to noise.

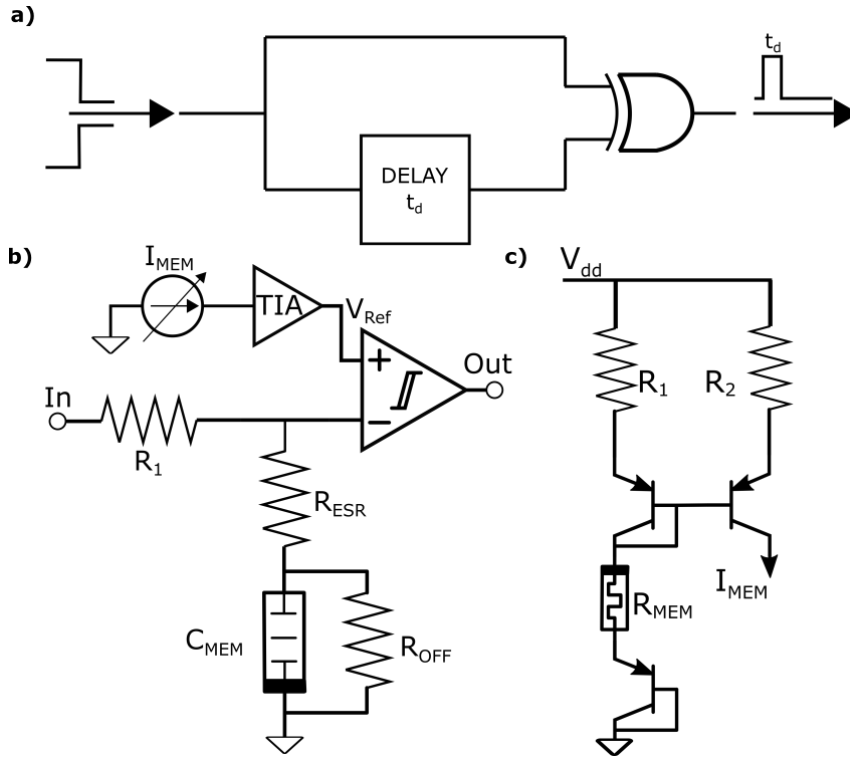


Figure 4.12: High-level description of the nanosecond pulse generator. **a)** High level view of the monostable multivibrator. The XOR gate at the output allows the multivibrator to output a pulse at both falling and rising edges of the input signal. **b)** Schematic representation of the proposed delay unit. Positive terminal: Memristor tuned current source sets the threshold voltage through a transimpedance amplifier (TIA). Negative terminal: an RC network delays the edge of the input signal. **c)** Memristor controlled current source.

A memristor tuned current source feeds into a transimpedance amplifier (TIA), which sets the reference voltage on the comparator. The TIA is realised with a grounded resistor, minimising power and areal consumption. A current mirror with memristive degeneration has been shown in Chapter 2 to fulfill the role of tuneable current source (Figure 4.12c). Additionally, resistor ratio (R_1/R_2) allows for further current scaling. A single programming circuit can be used to adjust both of mem-devices.

Circuit Analysis

When capacitance fully switches, the model estimates a negligible resistance drop of 0.15% - around 300Ω. Appropriate choice of the resistor forming the RC network allows to fully neglect the impact of R_{Off} . ESR, resulting from long and thin interconnects to the memristor, can be controlled during manufacture. Its effect can therefore also be neglected.

Assuming perfect comparator properties the voltage across the capacitor on the rising edge of the input pulse is:

$$V_c = V_p(1 - e^{-t/RC}) \quad (4.22)$$

where V_p denotes the logic level (peak input value). The comparator ideally toggles when $V_c = V_{Ref}$, where V_{Ref} is externally provided threshold voltage:

$$V_{Ref} = V_p(1 - e^{-t_r/RC}) \quad (4.23)$$

Where t_r is time required for the filtered signal to reach the threshold voltage. This is rearranged as:

$$t_r = -RC \ln(1 - V_{Ref}/V_p) \quad (4.24)$$

Similarly the delay of the falling edge can be expressed as:

$$t_f = -RC \ln(V_{Ref}/V_p) \quad (4.25)$$

The output pulse has the same width for both rising and falling edge triggers if:

$$2V_{Ref} = V_p \quad (4.26)$$

Equations 4.24 and 4.25 suggest that there are two means of controlling the delay of the signal - linear and logarithmic. To linearly vary the delay, the value of RC constant has to be adjusted. By programming the memristor the ratio of $R_{off}C_{off}$ (that is RC_{Max}) to $R_{on}C_{on}$ (or RC_{Min}) of 30 (Figure 4.11a) is achieved. Logarithmic control is achieved by keeping the RC time constant fixed and varying the threshold voltage V_{Ref} .

At high frequency of input triggers, the response of the multivibrator changes. Assuming input square wave with half-period of $T_o = 1/2f_c$, such that $T_o < 5RC$ the above equations will not hold as capacitor will not reach steady-state voltage. The voltage across the capacitor will be bounded between:

$$V_{Lower} = V_p \left(1 - \frac{e^{-T_o/2RC} - 1}{e^{-T_o/RC} - 1} \right) \quad (4.27)$$

$$V_{Upper} = V_p \frac{e^{-T_o/2RC} - 1}{e^{-T_o/RC} - 1} \quad (4.28)$$

so that $0 < V_{Lower} < V_{Upper} < V_p$ holds.

The main consequence of using high frequency trigger signals is the compression of the range of voltage thresholds that can be used. Consequently as frequency increases, the logarithmic behaviour is reduced to a linear one. This follows from the Taylor expansion of equation 4.25:

$$T_p \simeq -RC \frac{V_{Ref}}{V_p} + \text{constant} \quad (4.29)$$

The sensitivity of the output pulse width to threshold voltage change for isolated trigger signals

is:

$$\frac{\partial T_p}{\partial V_{Ref}} = -\frac{RC}{V_{Ref}} \quad (4.30)$$

and for high frequency driving signals:

$$\frac{\partial T_p}{\partial V_{Ref}} = -\frac{RC}{V_p} \quad (4.31)$$

A number of limitations stemming from the design can be noted. Firstly, this circuit is not envisaged to work with discrete elements, due to small memcapacitances realised. Discrete impedance scaling techniques will suffer the same consequences. A small technology node integrated circuit process is adequate for this design.

Secondly, due to finite switching speeds of transistors dictated by their gate capacitance and transconductance, all elements add to the delay. As a result the pulse width tunability will be limited by the non-zero delay of the comparator. The maximum length of the output pulse is limited by the magnitude of the RC time delay. Due to small capacitances, large resistors are required, which will significantly degrade the input SNR and distort the linear/logarithmic nature.

Finally, the continuity of the range will be directly determined by the number of reliably accessible states of the mem-devices. It has been shown that a single device can be reliably programmed into at least 92 distinct, non-overlapping resistive states [27]. Simultaneously, state-of-the-art memcapacitors are reported to store maximum 2 bits of information. It is estimated that memcapacitive technology trails the memristive development by around 6 years.

Simulation Results

Figure 4.13 shows the full circuit design using TSMC 180nm technology. All dimensions are uniform with $W = 0.22\mu\text{m}$ and $L = 0.6\mu\text{m}$. the design features a potential divider to ensure the voltage level at the memcapacitor is below its switching threshold. Figures 4.14a-c show the simulation results.

These results were obtained for a falling edge trigger (Figure 4.14a) described by equation 4.25. Figure 4.14c shows that modulation of the RC time constant, through reconfiguration of the memcapacitance, yields a linear behaviour which closely matches the theoretical prediction. All three lines have similar gradient of $\ln(V_{Ref}/V_p)$. Some deviation from the ideal behaviours is observed, however as the reference voltage decreases and relative pulse widths increase the percentage error decreases.

Similarly, results in Fig. 4.14b show logarithmic behaviour (the x axis is log scaled). The gradient of the resulting straight lines when plotted against $\ln(V_{Ref}/V_p)$ closely matches $-RC$

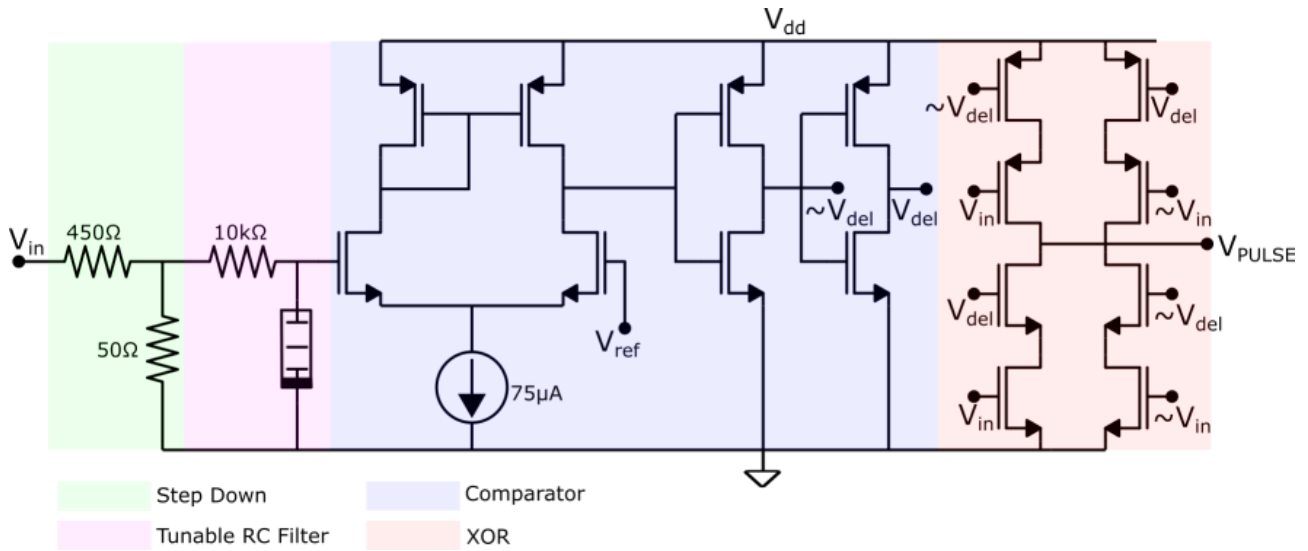


Figure 4.13: Transistor level pulse generator. The circuit was simulated using TSMC 180nm technology. To realise the inverted input signal, a 2 transistor inverter was used.

value of the setup used.

The design was found to allow pulses as narrow as 2ns, yielding a bandwidth of around 250MHz. In fact, by translating the circuit into smaller technology node, even faster pulses are expected, which closer matching to theory.

The main limitation observed during simulation is the switching point of the two inverters at the output of the differential pair. When the input signal crosses over with the threshold voltage, the first inverter does not switch as a binary element, rather it exhibits a sigmoid function. The following inverter and then the XOR gate are consequently affected producing pulse widths which deviate from the expected value. This can be addressed with faster transistors, i.e. smaller gate capacitance or higher transconduction. In fact by increasing the tuning current it is always possible to match theoretical and measured results for a narrow set of threshold voltages and RC time constants.

Using 5V supply and $75\mu A$ current bias, the simulated power consumption settles at $375\mu W$ in the idle state (both high and low) and briefly peaks at around $650\mu W \pm 100\mu W$ (depending on the pulse width) during the pulse transition. The increased power during transition is attributed to high frequency switching losses due to technology-dependent transistor capacitances. In addition, the pulse width determines the exact peak power dissipation, as longer pulses are the result of less abrupt signal crossover in the comparator. Comparator, thus switches more slowly, producing the sigmoid behaviour discussed earlier, leading to power waste. Notwithstanding, huge power savings can be realised with a more modern CMOS technology, e.g. 10nm, as the bias currents scale down. Simultaneously, lower rail voltage can be used, e.g. 1.8V. Combined the two improvements could yield over a ten-fold power reduction.

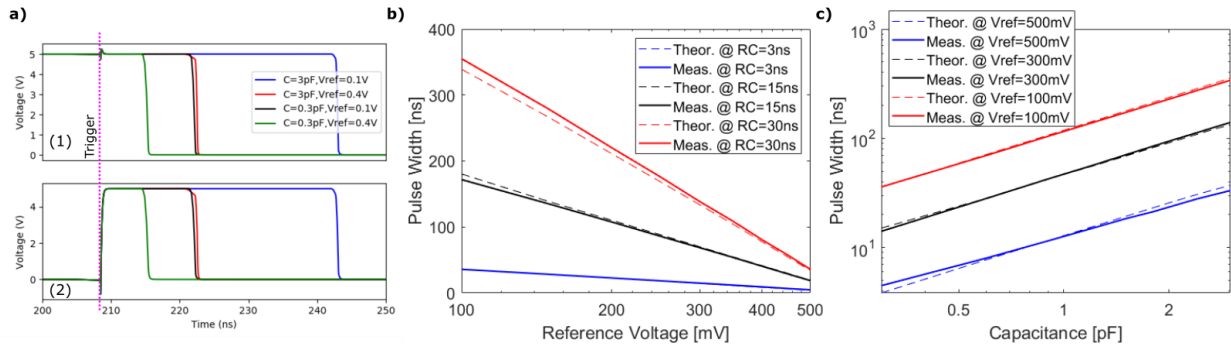


Figure 4.14: Simulation results of the nanosecond pulse generator using TSMC180nm technology. **a)** Output pulse shape at various settings. Subplot (1) shows the delayed copy of the trigger, while subplot (2) shows the output of the XOR gate. **b)** Logarithmic control of the pulse width. Reference voltage of the comparator is swept from 100 to 500mV. Resulting pulse widths realised with RC of 30, 150 and 300ns are plotted alongside theoretical values. The x-axis is scaled logarithmically, thus producing the distinct straight curves. **c)** Linear control of the pulse width. Discharge time constant is varied from 3 to 30ns (capacitance setting from 0.3 to 3pF). Pulse width obtained at threshold voltages of 100, 300 and 500mV are plotted alongside theoretical values. Strong linear behaviour is observed as predicted.

Memcapacitance Read Out

The proposed circuit is an ideal candidate to sense and measure capacitance and memcapacitance in devices. By enabling the circuit to work in the log-mode, i.e. through the control of the reference voltage, RC time constant can be extracted quite simply, by triggering the multivibrator and reading out the pulse widths. Similarly, to confirm the existence of memcapacitance, the reconfigured device could be read out in both linear and logarithmic modes. This is a small and cheap alternative to precision instrumentation and also very suitable as on-board instrumentation. The device can be also used to measure variations in resistance using the same concept of RC tuning - by overwhelming the parallel memcapacitance with large fixed capacitor, pulse width can be modulated with memristance alone.

Care must be taken as not to switch the device with the trigger pulse. For that reason a potential divider was introduced (Figure 4.13). Alternatively, control signal could be supplied already at the correct level.

The realisation benefits from a low-interrogation requirement. To prevent keeping the potential difference across the device for long, the rising edge followed by falling edge triggers can be applied one after the other. The smaller the RC constant, e.g. by reducing the value of resistance, the shorter the break between input edges is required.

Finally, the benefit of using smaller technology node is higher bandwidth. This enables sub-nanosecond output pulses, allowing to interrogate the mem-device with incredibly fine signals, virtually removing any effect they may have on the device state.

Implications

This is an altogether different approach. It uses the variable component directly in the signal path of the system, something which was avoided in all the previous experiments. Therefore rather than parametrically tuning a gain element in the circuit, through memristive current control, the memcapacitor acts directly on the input signal. Provided that the assumptions and the model hold valid, this method answers the current problem of synthetic capacitors. Namely, if tunable memcapacitors of the form discussed above do exist, there is virtually no reason to gyrate physical or synthetic inductors. Even with a limited tuning range of a memcapacitor, by using an impedance multiplier the value of the capacitor can be inflated at will.

However, the reality may be as underwhelming as it is with memristors, in that they do not behave very well when interrogated with circuit signals. Moreover, since the geometries involved are indeed small, the bandwidth of the memcapacitor is expected to be small, as it is the case with memristors.

4.3.3 Comments

Two waveform generators were presented in this section, which as it was the case with filters, highlight the key differences in functional synthesis between the building blocks and more dedicated, almost application specific, approaches. The ring oscillator has shown that using multiple building blocks in a single circuit is possible with proper isolation. However, the power consumption quickly becomes too large to render the system wearable or even battery operated. Therefore a modular approach is to be taken, a compromise must be made - power consumption or functionality. The more building blocks there are, the more degrees of freedom in reconfiguration there are available to the user/controller. At the same time since one discrete block can consume as much as 750mW (up to 2mW on IC) the system quickly demands more current with each additional block. Nonetheless this can still be implemented on a benchtop mains-powered platform such as FPAA (see Chapter 5).

In contrast to the discrete building blocks, a memcapacitor approach is presented. Conceptually, this is an altogether different approach - as discussed earlier, it uses an active device directly in the signal path. However based on the models presented in literature, such deployment is justified. The approach yet again demonstrates superior performance over building blocks, however once again, rendering the design static - i.e. with a single functionality.

4.4 Discussion

4.4.1 Static and Dynamic Deployment

Referring to the research questions introduced at the beginning of this Chapter, the circuits and experimental results give overall a degree of confidence that some gyrator based solutions may in fact prove useful on larger scale. Their characteristics however ought to be scrutinised such that practical limitations on systematic level are clear. Low-pass and high-pass filter presented in Chapter 3, and used as part of the characterisation routine, have already highlighted that a simple two-element circuit can be easily reconfigured to desired cut-off frequencies. This was achieved without dedicated data converters and resulted in analogue continuity in time and value.

It may therefore seem that memristor tuned blocks are the answer to the pressing issue of continued miniaturisation of circuits and systems. Using the methodology presented in this work, whereby memristor is used in a bias circuitry and its value is held static, this illusion is in fact not accurate. Reconfiguration does require another system, sometimes called *the reconfigurator* [28]. As opposed to dynamically reconfigured memristors, where their value continuously changes as a response to applied input stimuli, static memristors are positioned in very delicate architectures such that they remain static at all times. The devices are only allowed to change their value when the decision to do so is made - be it through a user input or through algorithmic adjustment.

This choice between using memristors in static (DC) and dynamic (AC) modes of operation is purely dictated by the maturity of the fabrication technology implemented. On a single wafer the yield of functional devices still remains comparably low, much lower than what is achieved with CMOS techniques nowadays. The fundamental properties of the devices are statistical - using them in deterministic dynamic systems still proves challenging. The opposite is true for the static use of memristors: a basic reconfigurator able to program the device to the desired resistive level, assess IV properties and determine threshold voltage of the device is enough to allow the devices to be used in low power and low voltage DC systems.

This is further highlighted by the recently measured frequency response of those devices [29]. Memristors exhibit relatively small resistance-bandwidth product as parallel (mem)capacitors dominate at high frequencies. The study observed that memristors show similar characteristics to operational amplifiers: they can be described as a single pole system. It appears that memristor could be used as a direct drop-in replacement for resistors in AC application, as long as the device exhibits approximately linear (Ohmic) IV response and the device is interrogated voltage levels below the switching threshold. However the technology limitations currently enable the memristive effects to be only measured at nano-scale, where stray capacitances play significant role and cannot be easily eliminated [29].

This however does not imply that dynamic use of memristors is impractical. On the contrary, device statistics make it an interesting tool for communication or high-density information storage by effectively treating the device as Shannon's channel. This is however beyond the fundamental scope of this Chapter. To summarise, memristive devices fabricated with modern technologies are well-suited for DC operation, where they form a part of bias circuit or for fairly low frequency subthreshold operation. This is only made possible with an addition of extra hardware - the reconfigurator - which enables on-chip programming and characterisation of the inherently statistical properties of the devices.

4.4.2 Building Blocks for Standard Circuits

Following from the stability analysis presented in Chapter 3, the circuit design should be carefully tailored to fit the systematic requirements. It was shown that loading the circuit with reactive components can in fact relocate the poles of the gyrator-based building blocks and thus affect the resonant frequency, damping factors and what follows the stability margins. The low-complexity systems presented in this Chapter were free from unwanted behaviour usually associated with large, complex circuits - high noise, distributed capacitance or large gains to name a few.

On the small scale presented here, gyrator based building blocks have been effectively used as direct drop-in replacements of physical inductors and capacitors. The tests were carried out with both physical fixed value components and tuned memristor enabled synthetics, resulting in virtually no perceivable changes other than what was already known - limited bandwidth and input signal range. Most of the realised systems did not introduce significant additional capacitive loading to the blocks, with perhaps capacitive lead-lag as the one exception, where a physical 470pF capacitor was used. It is expected though, as derived in the stability analysis, that significant capacitive loading would have detrimental effect on the performance of the building blocks. There are two approaches one could take to address this: careful design and characterisation, involving additional elements used for compensation or incorporation of the building blocks into larger ready-made reconfigurable systems.

Both approaches have their practical advantages as well as disadvantages. By employing the route of meticulous and precise design, the functionality of the blocks as direct drop-in replacements is preserved. This is beneficial from the perspective of general purpose, high-level design and fast prototyping, allowing the designer to focus on the functional behaviour, rather than follow the rabbit-hole of performance optimisation. Standalone building blocks give a new lease of life to the old and classic techniques that have since been replaced with digitally reconfigurable solutions, such as those presented in this Chapter - signal conditioning, processing and generation. However, this comes at a price: the gyrator-based blocks will always be outperformed by ASIC design. The general purpose blocks will compromise many features such as

controlled value range, power consumption or physical size. The IC design itself will require high skill. After all, every time the block is reconfigured its self-resonant frequency and damping factor change. To accommodate for large variations in stability margins, it is imperative that the design must feature additional compensatory sub-circuits.

An alternative approach to realising functional and parametric tuning involves custom design of tunable systems from ground up: rather than implementing designs based on variable equivalents of classic components, it appears more optimal to design entire blocks and architectures whose behaviour can be reconfigured. This is in part demonstrated through the variable gain amplifier and monostable multivibrator presented in this Chapter. They represent a change in mindset required to advance the analogue reconfiguration - EEG band select or pulse width modulation simply builds upon the concept of a filter. While parametric reconfiguration is a more intuitive approach, there are huge performance margins to be gained by going into ASIC and enabling functional synthesis, as clearly demonstrated. Though the design process is indeed longer, the circuits do not feature the usual inductors or capacitors. Instead the reconfiguration is embedded into the very fabric of the system. This concept can be further expanded with appropriate platforms (discussed in Chapter 5), enabling both functional reconfiguration as well as parametric tuning.

Therefore both solutions offer desirable characteristics; on one hand ease of use of gyrator based blocks makes them suitable for high-level synthesis, fast prototyping and allows to quickly recycle classic circuit techniques, on the other reconfigurable ASIC offers a whole palette of high-performance reconfigurable systems. The blocks presented in this thesis do lend themselves as parametric valves: from controllers to signal generators. Furthermore, use of multiple such blocks in a single circuit has been demonstrated. A formal limit on the maximum number of synthetic inductors and capacitors is not given, as every topology will vary. In principle if the circuit of choice has suitably isolated consecutive functional blocks, the limit is in fact arbitrary. The pulse width modulator is a great example, where one block was embedded into the ring oscillator, while the other played a role of differentiator in a subsequent stage. The two were isolated through a series of inverters, allowing them to operate as expected.

4.4.3 The Capacitor Problem

Triple gyrator variable capacitors have proven cumbersome and difficult in utilising. This is primarily the reason for the dominance of variable inductive elements in this Chapter. While the resonant frequency remains unchanged, an star connected gyrators effectively form a reasonably high Q resonator. That is the more gyrators there are, the higher the order of the circuit, resulting in faster gain roll-off, leading to narrower and more prominent *peaking* in the frequency response. The synthetic in the current form have little to offer to the designer. The circuit is redundant and unstable. The aspect of redundancy arises from the fact that a physical capacitor

is first gyrated into ground synthetic inductor before its function is yet again reversed. Other techniques such as those mentioned in Chapter 2 currently prove more feasible.

This isn't to say that capacitive tuning is impossible. On the contrary; as more publications claiming quaternary memcapacitors emerge, it may prove altogether impractical to synthesise reconfigurable capacitors. It is the inductors that still seem to elude researchers. Results in this Chapter have indeed considered such a possibility. While the technology appears to be trailing memristive developments by around 7 to 8 years in terms of memory capacity, the idea of fully tunable resistors and capacitors is lingering on the horizon.

Since the fabrication process of mem-devices is CMOS compatible allowing post-fabrication of devices on the top metallisation layer, entire mem-powered chips are possible. This therefore leaves one incompatible element - inductor. To the best of author's knowledge there is no study showing that meminductive behaviour observed in a package that competes with memristors and memcapacitors is possible. There are isolated studies claiming some degree of inductive tuning, however the results often show compound behaviour or simply arise from misinterpretation of data. Hence, there will be memristor enabled synthetic inductors can feasibly fill that gap on chip and allow further designs.

4.4.4 Summary

The *verbatim* questions stated at the beginning of the Chapter can be answered to summarise the findings of this part of the thesis.

Is the memristor suitably isolated from spurious, input-induced signals? The memristors remain agnostic to the function the blocks play in a wider system. As it was the case in Chapter 3, there are only two reasons for measured inconsistencies in memristive levels: 1) the mechanically induced charge as well as some electrostatic discharge during handling led to device reprogramming, and 2) as memristors wear out over time, their threshold voltage appears to drop significantly, leading to volatile behaviour and device relaxation. The voltage across the simulated device, as part of the variable gain amplifiers, remained constant. Some variation, of the order of 20-30 μ V was recorded when input signal far beyond the dynamic range of the system leading to output saturation were provided. This shows that with sufficient impedance between input and the memristor, the device will behave as required.

What systematic complexity is possible with gyrator based blocks? The PCB based realisations of the building blocks only lend themselves to a very limited range of applications, usually those requiring one or two such components at most. Even then, the devices should ideally be isolated. It is still possible to stack them in various configurations - one such example of RLC filter was presented in this Chapter. However, the blocks should be viewed as proof of concept; that is the simulated behaviour on CMOS will allow huge performance boosts to

be realised. However even CMOS design will not change the fundamental problem of gyrators and that is their self-resonance. Hence for a given architecture there exists a critical number of synthetic blocks which can be connected together before the system becomes unstable - this number is application dependent.

Is there anything to be gained by introducing analogue reconfigurability to classic circuit topologies? Plenty. Classic techniques that have since been replaced by digital solutions may once again be revisited challenging the status quo. It is generally accepted, as discussed in Chapter 2, that many of the digital functions can be more efficiently replaced by an analogue ASIC design. This was the motivation behind realising the EEG band select filters presented in this Chapter. By enabling parametric reconfigurability, circuits are cleared from resource redundancy and a continuous range of parameter values is established at fraction of the power and area. Taking this idea one step further and designing systems with tuned fabric, functional synthesis is achievable.

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Chapter 5

Towards Integrated Analogue Computation

Chapter 5 conducts a theoretical feasibility study of using reconfigurable blocks on large arrays such as field programmable analogue arrays. An architecture is first proposed which would be able to host such large numbers of analogue components. Following that, noise analysis of a CMOS gyrator candidate is presented showing the true nature of these analogue blocks. Assuming that in fact it is possible to realise a platform like that, the chapter discusses in detail one particular application, namely differential equation solving, a ubiquitous problem in computational methods. Finally, the chapter is concluded with an overview of potential applications of such FPAA and ones that are already being pursued.

5.1 Introduction

The previous two chapters give insight into one possible method of realising analogue reconfiguration with memristors. Chapter 3 presented a general methodology, while Chapter 4 focused on identifying the limitations of the gyrator-based approach. The conclusion of the discussion thus far can be interpreted two-fold: on one hand the memristor tuned devices do indeed provide improved performance characteristics over other analogue methods. The blocks are smaller, offer continuity in control which is only limited by the memristor technology and quite importantly are non-volatile. On the other hand, whilst the individual blocks may save space on silicon, the need for a reconfigurator greatly narrows down the application space, and stability of some systems limits the synthesisable complexity.

Taking the above into account, the transconductor-rich blocks lend themselves perfectly well to realise very large reconfigurable analogue arrays, as demonstrated by Hasler [1]. This gives

good starting ground for a discussion on performing computation with the presented blocks. The following chapter will revolve around Field Programmable Analogue Arrays, or FPAAs for short - modern day analogue computers (see Chapter 2).

5.2 Large Reconfigurable Platforms

Memristor arrays offer higher density of digital and analogue memory, as well as allow tighter packing of individual subsystems, since they are deposited on top of the silicon. Direct integration of CMOS and memristors in a single process is still impossible or impractical, however post-processing enables effectively stacking the devices and exploiting the third dimension on the wafer (Figure 5.1a). Presently this appears to be the preferred method. The downside to 3D stacking is the need to provide extra metallisation and silicon area to connect the layers. This may indeed require 4 transistors in a fully reconfigurable system per memristive device as connections to the circuit and to the reconfigurator must be facilitated (Figure 5.1b). The number of transistors can be reduced to just two, if circuits are designed such that memristor remains grounded both in-circuit and during reconfiguration. However a two transistor approach inherently requires dual-supply power rail architecture, since both positive and negative voltage programming pulses would be required. A 4 transistor architecture simply takes advantage of an H-bridge connection in a single-supply system.

Therefore the area limitations of CMOS with post-processed memristor arrays are two-fold: large reconfigurator and large transistor switch array. The transistors used to switch the memristors in and out of the circuit have to be large enough to tolerate high voltages and currents required to form and program the devices. For example, the bilayer devices used throughout this work, require voltages up to 12V to be formed and programmed. This determines minimum feature size of the switches, as to prevent dielectric breakdown of the devices. At the same time, there is a further need to make the transistor wide: narrow devices will tend to limit the programming current through the memristor, effectively limiting the compliance current. Narrow transistors, with large channel resistance may in fact prevent the memristor from being programmed (when interfaced by the reconfigurator) or add unwanted series resistance (when interfaced by the circuit).

This leads to a rather counter-intuitive observation: despite the immense downsizing of the analogue tunable components, the additional circuitry required to enable the technology to become useful, effectively increases the area per component. That is the case at least for small systems, which would more likely benefit from classic digital reconfiguration techniques e.g. through FLASH memory or CMOS compatible FGFETs.

The picture changes once the size of the platform increases, featuring thousands or millions of such memristive devices. The size of the reconfigurator becomes negligible compared to the

rest of the entire system. While the increased platform size doesn't affect the switch count per device, beyond certain critical size the chip benefits from economies of scale. It is then, and only then, that the full potential of the memristor arrays can be exploited. The effective memory density of such a platform is becoming comparable to state of the art FLASH technologies. In 2016 Micron revealed that their 3D technology had reached the density of 2.7Tb per inch squared. That roughly translates to 6 bits of information occupying on average $1.3 \times 10^{-15} \text{m}^2$. Currently the best results show that memristive technology is capable of storing the same 6 bits on area of $49 \times 10^{-15} \text{m}^2$ (220x220 nm)[2]. As memristor technology matures, the feature size decreases. This can eventually lead to ultra-dense arrays able to store the same 6 bits on an area of just $0.6 \times 10^{-15} \text{m}^2$ - half that of 3D CMOS [3]. By taking advantage of the 3D stacking and applying it to memristor crossbars can in theory results in drastically enhanced memory densities. At the same time, since memristors have ultra-low power read and write operations, the density scaling is not met by proportional heat increase, which is one of the strong benefits of memristive technology.

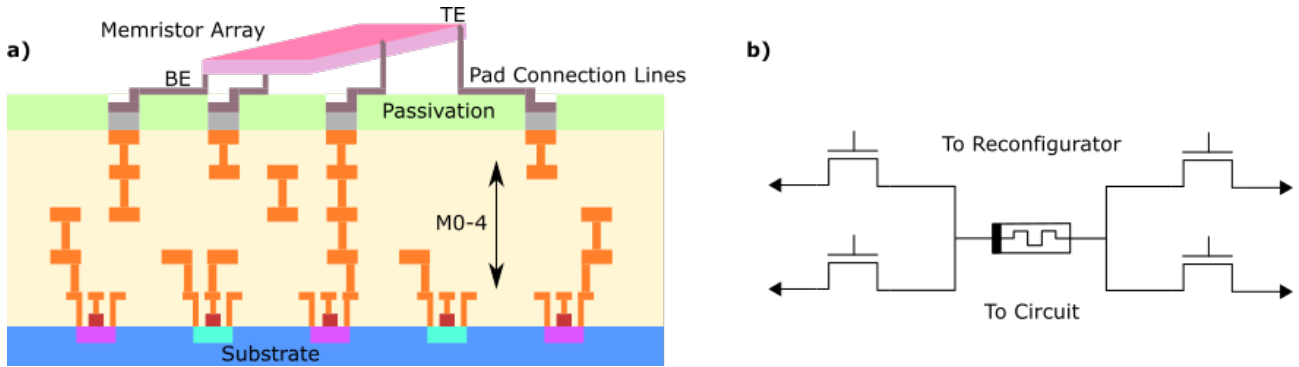


Figure 5.1: Integration of CMOS process with memristor array. **a)** Typical cross sectional view through a CMOS wafer with a post-processed memristor array on top. Passivation layer on top is etched to make way for connections to both top and bottom electrodes (TE and BE). **b)** 4 transistor connection required to swap the memristor between reconfigurator and circuit.

5.2.1 FPAA Architecture

Field programmable analogue arrays are very well suited to host banks of memristors. In fact, such an approach was demonstrated, albeit unsuccessfully due to poor memristor behaviour [4]. However, the group has already answered the key question: it is possible to realise a sufficiently large analogue platform with post-processed memristors on the top layer. This allows to shift focus from *how* to *what*.

FPAA are versatile and powerful tools used for arithmetic computation, circuit synthesis and calculus. They leverage the physical behaviour of devices, as postulated by Mead [5], to enhance the computational efficiency. Most FPAAs however, only achieve continuity in time and input/output signal but not in parametric or functional tuning. Full analogue prowess can be achieved with standard FPAA architectures combined with memristive tuning mechanisms.

Architecturally, the platform ought to be based on the results presented by Hasler [6], due to its demonstrated superior performance over other topologies.

In classical current controlled or FGFET realisations of the FPAA there are 4 main components: computational analogue blocks, switch and connection fabric, centralised processor and its memory, and some I/O drivers. A memristor filled architecture requires an addition of a fifth and sixth block - a precision programmer and a memristor crossbar array.

Computational Analogue Block

Computational analogue blocks or CABs are the workhorses of the FPAA, similarly to the configurable logic blocks (CLB) of the FPGA. They enclose reconfigurable devices used to synthesise an input computational problem. While in FPGAs the structure of CLBs is homogeneous, FPAA designers tend to introduce multiple versions of CABs to reflect the need for certain components. As a result there can be multiple designs on a single chip (Figure 5.2).

Fine Blocks: Fine blocks contain the most often used elements - individual transistors, direct access ports to memristors, variable capacitors and inductors, flip-flops and look-up tables (LUT). These are ubiquitous, low complexity and smallest elements, appearing in most computational problems.

Medium Blocks: Medium blocks present the compiler with a set of predefined higher level units, to optimise the synthesis. These blocks may include impedance inverters (gyrators), variable gain amplifiers, tunable transconductance amplifiers, standard op-amps, current mirrors and full adders.

Coarse Blocks: Coarse blocks incorporate reconfigurable subsystems that may often be used. For example, band pass or notch filters are present in almost all sensing applications. These blocks should provide easy accessibility to some predefined reconfigurable filters, e.g. full biquads, PID controllers and multipliers. Due to their high silicon requirement, coarse blocks trail medium and fine blocks in terms of the total count on an FPAA fabric.

Switch Blocks and Interconnecting Fabric

The interconnect fabric plays a pivotal role in FPAA design, it can epitomise fundamental problems of analogue design. Unlike in FPGA, FPAA needs to deliver fine signals between blocks. The interconnect fabric will often limit the useful bandwidth of the FPAA, and can lead to signal degradation. One way of looking at this problem is to take a full advantage of it [1], and introduce in-fabric signal processing, effectively treating the losses as design elements, e.g. resistors. This is indeed a complex solution as it requires highly precise modelling of the

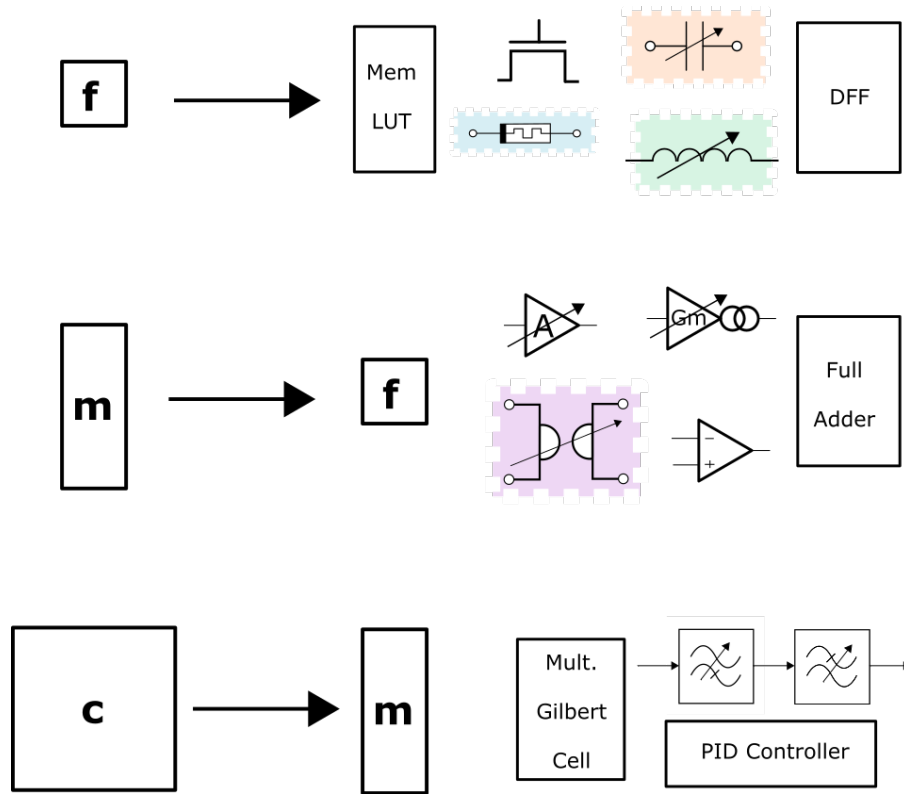


Figure 5.2: Composition of computational analogue blocks, discriminating between fine, medium and coarse elements. Fine elements contain most commonly used elements such as memristors or transistors. Medium elements contain all of the fine elements plus some ready-made higher level blocks such as op-amps or variable amplifiers. Finally, coarse elements contain all of the medium elements and commonly used subsystems, e.g. variable front-end filters or PID controllers. It is important to recognise that an ideal FPAA should allow for digital functionality offered by FPGAs as well as analogue processing.

fabric. It further introduces a certain dilemma, e.g. signal quality or redundancy and higher complexity.

CPU and Memory

A centralised unit is required to run the program, along with a quite vast memory. This is mandatory since the processing is inherently analogue, and the data is presented to the user in digital format. Fundamentally, digital microprocessors are likely to retain their superiority over analogue counterparts in certain disciplines - logic and task scheduling.

Interface and I/O

The I/O block is a standard set of hardware protocols for communication. Interface units may include a whole array of analogue to digital converters, which take the analogue solution and pass it onto the I/O block and/or memory.

Memristor Programmer

A standalone FPAA design that is envisaged, requires a block to program the individual tuning elements - memristors. Currently reconfiguration in subsystem testing is achieved with a standalone platform - ArC One™[7]. The embedded reconfigurator could therefore be an IC version of the presently used discrete programmer. Since the devices are incredibly delicate and sensitive, the platform has to be highly specialised operating at pico-ampere level.

Memristor Crossbar Array

This is the heart of reconfigurability. Memristors, with the recently reported 6.5bit [2] equivalent memory capacity are ideal for system-wide tuning. They have a number of advantages - low area consumption, low power, high-level of tuning, non-volatility and ease of interfacing. Current fabrication methods allow to pack thousands of the devices onto a wafer.

In addition, the memristors are post-processed on top of the silicon wafer, meaning the area consumption is actually determined by the underlying integrated circuit, high integrated memristor count is an added benefit of this emerging nanotechnology.

5.2.2 Layout

Figure 5.3 shows the proposed layout structure of the memristor-filled FPAA. The first block in top left corner shows a structure of a functional block. Each functional block has the capacity to synthesise low complexity circuit on its own. While the precise layout and count of the fine, medium and coarse elements is arbitrary, it shows clearly one possible issue with using multiple blocks. Namely the connection and switch fabric are highly non-uniform, leading to two issues. Firstly from the design perspective it is more challenging to architect the fabric. However for a single design this would have to be done just once, as each functional block is effectively identical. Secondly, non-uniform switch fabric adds extra complexity to the compiler. Since FPAAs will need to handle very low level signals, and hardware synthesis is known to be an NP problem, an anisotropic fabric could make optimal synthesis infeasible.

This approach is the only one that guarantees efficient layout and area consumption; designing a uniform fabric would lead to either bigger individual blocks or large unused chunks of die area. This poses an interesting question: what is the optimal fabric configuration for small FPAA, yet one big enough to justify the use of memristors? It is indeed possible that already at this scale an anisotropic fabric could degrade the performance to a point, where using analogue over digital computation offers no advantage. To conclude the discussion, it is believed that very large arrays would have to be designed with a uniform switch fabric.

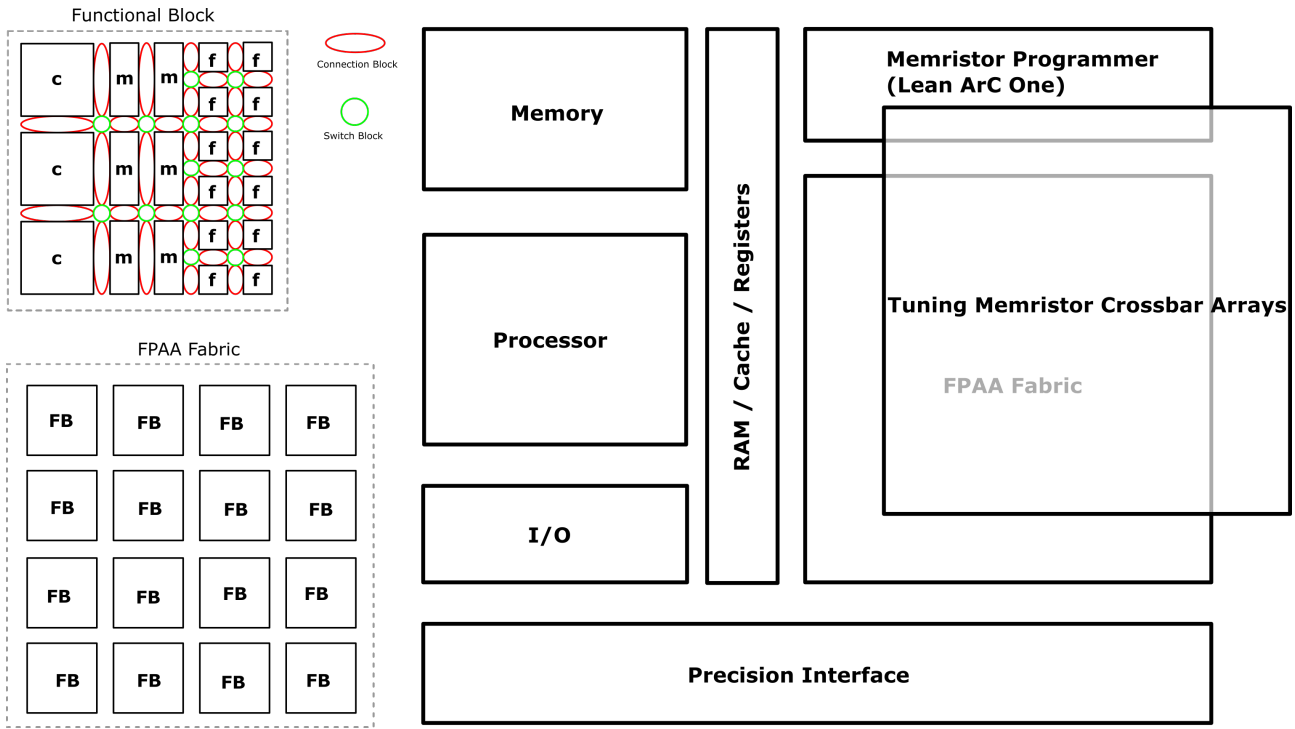


Figure 5.3: Proposed architecture of a memristor filled field programmable analogue array. Top left shows individual structure of a functional block containing the fine, medium and coarse computational analogue units. Bottom left shows arrangement of the functional blocks forming the heart of the FPAA - its computational fabric. Block diagram on the right shows the high-level architecture of the FPAA platform incorporating memristor arrays. The physical layout, orientation, count and size are arbitrary.

The above question could be rephrased: how many connections does each block need to have? Can more than one block be lumped together in such a way as to equalise the number of connections? Seeing that the design proposed in Figure 5.2, recycles smaller blocks and incorporates them into bigger ones, it is certain that the number of connections for an individual block grows with block size. This can therefore be addressed with fine-tuning of the count of fine elements in each of the blocks as to provide the same number of connections to each block. Once all blocks have the same I/O count the fabric design can be simplified, as the number of word-lines and bit-lines in a standard Manhattan architecture would remain constant.

Arranging functional blocks in an $N \times N$ configuration, yields the FPAA fabric itself. Since the functional blocks are all the same, the connections are all identical to those of an FPGA simplifying the design. The FPAA fabric is then embedded on a silicon die alongside other elements discussed earlier to form the standalone FPAA platform. Memristor elements are post-processed on top of the FPAA fabric for ease of connectivity.

5.3 Noise of Gytrators

5.3.1 Ugur and Tarim Gyrator

A large array, filled with gyrators could prove unfeasible for a different reason. Noise generated by gyrators is not very well understood, and theoretical estimations are not accessible in literature. If in fact, noise produced by the arrays of gyrators significantly degrades the signal to noise ratio of the system, then the whole computational platform will be invalidated. This is one of the primary problems of analogue computation, and the reason for such a rapid success of digital counterparts, which are characterised by superior immunity to noise. It is therefore imperative to address the issue of theoretical noise performance of a single gyrator structure.

For this purpose a broadband CMOS gyrator is selected from literature, which offers the characteristics described in Chapter 3. The schematic digram is presented in Figure 5.4a. Transistor M1 acts as a negative transconductor ($-g_{m1}$). The output of the transconductor located at the drain of M1 is connected to the gyrated capacitance. The voltage across the capacitor is then fed into the feedback gyrator (M2), which is also characterised by a negative value of the transconductance ($-g_{m2}$). To reverse the sign, the output current is mirrored, through transistors M3 and M4 and its direction, hence polarity at the input of the gyrator is reversed. The gyration factor is controlled by bias current supplied through a current mirror M5/M6.

The transistor level schamatic can be represented in terms of its functional amplifiers. There are three individual amplifiers in the circuit - 2 transconductors and one current mirror. The high level representation of Ugur and Tarim gyrator is presented in Figure 5.4b.

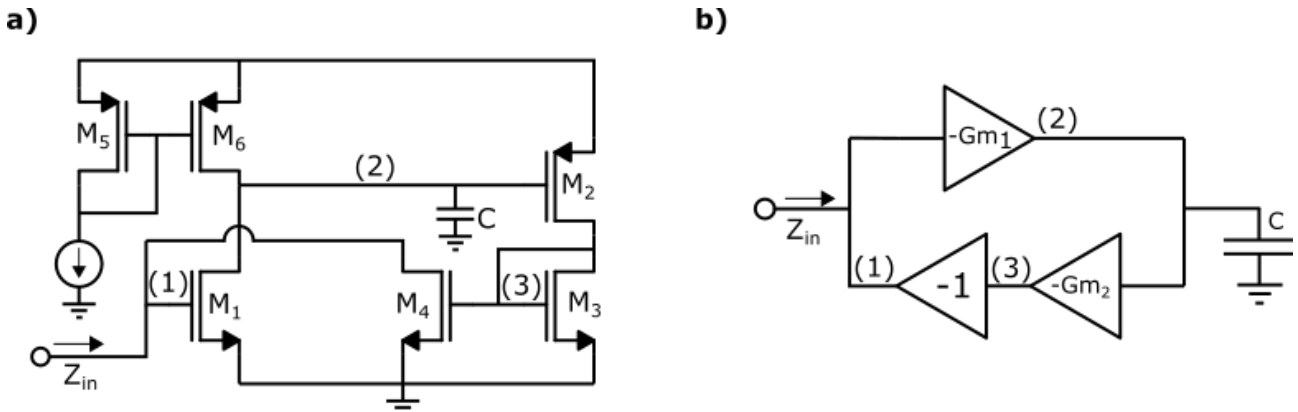


Figure 5.4: Simple broadband CMOS gyrator by Ugur and Tarim [8]. **a)** Transistor level schematic diagram of the broadband gyrator. **b)** Higher abstraction level identifying three key components in the broadband gyrator.

5.3.2 Noise Model

Amplifier Noise Model

To analyse the noise of a gyrator a standard amplifier noise model can be adopted (Figure 5.5), since gyrator is simply a combination of three such amplifiers. The model consists of ideal amplifier with input referred voltage and current noise sources. Furthermore the source driving the amplifier is also assumed non-ideal. However, as discussed in [9], even the basic amplifier model is often further simplified by either assuming lack of correlation of V_n and I_n or by completely removing I_n from calculations. In large signal applications, these crude simplifications can be justified, however the assumptions do not hold valid anymore when signals are near the order of magnitude of noise.

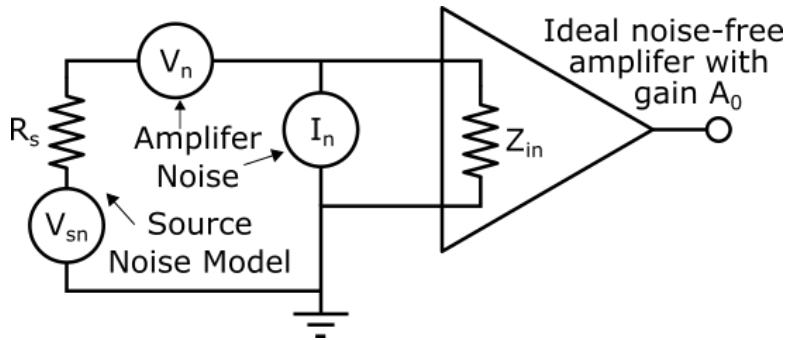


Figure 5.5: Classical amplifier noise model.

There will inherently exist some correlation between V_n and I_n . By assuming an independent Johnson source the equivalent input noise of the amplifier (V_{ni}) is expressed as:

$$V_{ni}^2 = V_{sn}^2 + V_n^2 + V_n^2 R_s^2 + 2C V_n I_n R_s \quad (5.1)$$

C in the equation represents the normalised correlation coefficient, whose absolute value is not bigger than one. C can in fact be a complex number and as it will be shown, for a case of a single MOSFET it is dominated by its imaginary part.

$$C = \frac{\mathbb{E}[V_n I_n]}{\sqrt{\mathbb{E}[V_n^2] \mathbb{E}[I_n^2]}} \quad (5.2)$$

$\mathbb{E}[*]$ indicates an expected value of the process variable. This model is useful as it allows to analyse each of the functional blocks from Figure 5.4b. The steps are to identify all noise sources and refer them to the input to fit the above model parameters. Note that equation 5.1 is independent of the input impedance of the amplifier.

Gyrator Noise Model

Following from the amplifier noise model, a gyrator equivalent can be derived. Each sub-block of the functional schematic presented in Figure 5.4b can be in fact modelled as an amplifier with its own noise contributions. This is presented in Figure 5.6. Since, each of the amplifiers also acts as a source to the following stage, their respective output impedances must be accounted for.

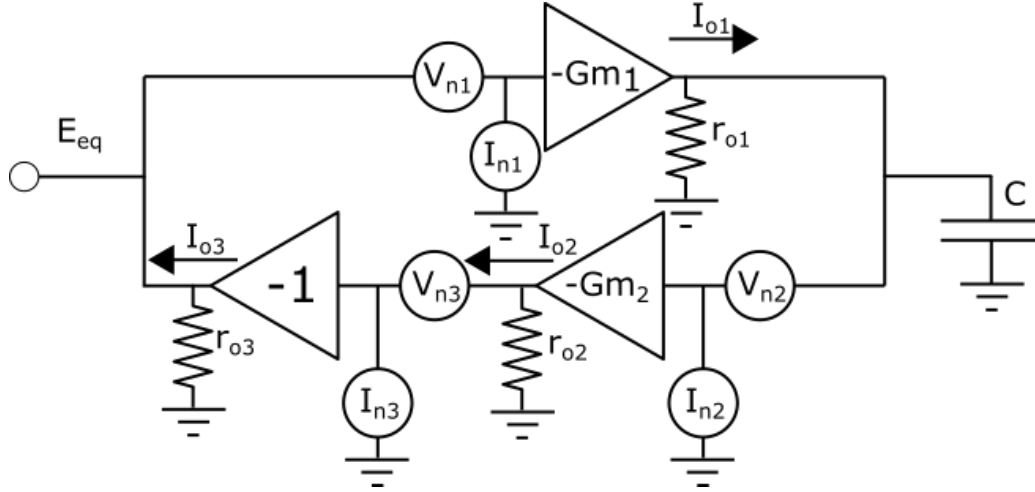


Figure 5.6: Gyrator noise model, based on amplifier model. Model is presented as a functional diagram of the Ugur and Tarim gyrator with individual noise sources. Each amplifier is characterised by its gain, output impedance, two correlated noise sources and and output noise current.

This circuit can then be analysed similarly to the general amplifier model, where the previous stage plays the role of a noisy source. For simplicity no input is present, so that intrinsic noise E_{eq} of the gyrator can be estimated.

$$E_{eq}^2 = V_{n1}^2 + I_{n1}^2 r_{o3}^2 + I_{o3}^2 r_{o3}^2 + 2C_1 I_{n1} I_{o3} r_{o3}^2 + 2C_2 I_{n1} V_{n1} r_{o3} + 2C_3 I_{o3} V_{n1} r_{o3} \quad (5.3)$$

Notice that due to feedback the output noise current of the current mirror (i.e. the inverting stage) will be weakly correlated to the sources V_{n1} and I_{n1} . In fact all the output noise currents will be partly correlated to **all** of the standalone noise sources. We can thus continue the derivation as follows:

$$I_{o3}^2 = I_{n3}^2 + \frac{V_{n3}^2}{(r_{o2}^2)} + I_{o2}^2 + f_1(I_{n3}, V_{n3}, I_{o2}) \quad (5.4)$$

where function $f_1()$ represents all the correlation terms.

$$I_{o2}^2 = Gm_2^2 \left[I_{n2}^2 (r_{o1} \| Z_C)^2 + V_{n2}^2 + I_{o1}^2 (r_{o1} \| Z_C)^2 + f_2(I_{n2}, V_{n2}, I_{o1}) \right] \quad (5.5)$$

where Z_C - the capacitor impedance, appears in parallel with the source, or output, impedance of the first transconductance stage. Finally:

$$I_{o1}^2 = Gm_1^2 E_{eq}^2 \quad (5.6)$$

The set of equations 5.3-5.6 when solved for E_{eq} will produce the input referred equivalent noise source. It is impractical to derive it here, as it will be an immensely complex function. Some simplifications can be made, if correlations between sources are known or can be eliminated. For completeness:

$$f_1(I_{n3}, V_{n3}, I_{o2}) = 2C_4 \frac{I_{n3}V_{n3}}{r_{o2}} + 2C_5 I_{n3}I_{o2} + 2C_6 \frac{I_{o2}V_{n3}}{r_{o2}} \quad (5.7)$$

$$f_2(I_{n2}, V_{n2}, I_{o1}) = 2C_7 I_{n2}V_{n2}(r_{o1} \parallel Z_C) + 2C_8 I_{n2}I_{o1}(r_{o1} \parallel Z_C)^2 + 2C_9 I_{o1}V_{n2}(r_{o1} \parallel Z_C) \quad (5.8)$$

The result in equation 5.8 represents the general case with *some* noise sources $V_{n1,n2,n3}$ and $I_{n1,n2,n3}$. To understand the behaviour further, each stage ought to be analysed independently to identify the input refereed noise sources.

5.3.3 Common Source Transconductor

Both M1 and M2 play the role of a negative transconductor based on common source topology of a MOSFET. A single MOSFET can have as many as 7 distinct noise sources:

1. Thermal drain noise - arises from thermal excitation of carriers in the channel of the MOSFET. It is generally most prominent in resistive structures as the thermal current gives rise to thermally generated potential across the resistive structure.
2. Shot noise - consequence of discrete nature of charges. This is particularly a nuisance at extremely low current application, producing random spikes which can be modelled by Poisson distribution.
3. Flicker noise - the dominant noise source at very low frequencies since it follows 1/f relationship. Its origin remains poorly understood.
4. Generation/Recombination noise - also called g-r noise. Arises due to statistical mean time of recombination of holes and electrons in semiconductor devices, particularly in photon detectors.

5. Random telegraph noise (RTN) - sometimes also called burst or popcorn noise. It is most prominent in semiconductor devices and ultra-thin gate oxide films. While scientific community still struggles to explain all occurrences of popcorn noise, it is often theorised that it may stem from random trapping and detrapping of carriers.
6. Gate induced noise - it is technically not a noise source *per se*. It is the result of thermal noise current generated in the channel of a MOSFET, which in turn induces voltage at the gate of the device.
7. Various thermal noises due to intrinsic resistances - due to imperfections of the CMOS process, stray resistances will be present at each of the terminals of the FET device, giving rise to more thermally generated noise.

For low frequency applications, models tend to include flicker and thermal noise sources. For higher frequencies, e.g. RF, flicker noise is omitted and instead gate induced noise is considered. Since the gyrator is designed to operate from near DC to RF we need to account for all three major sources. It is assumed that the role of shot, G/R and telegraph noise sources are negligible compared to the rest.

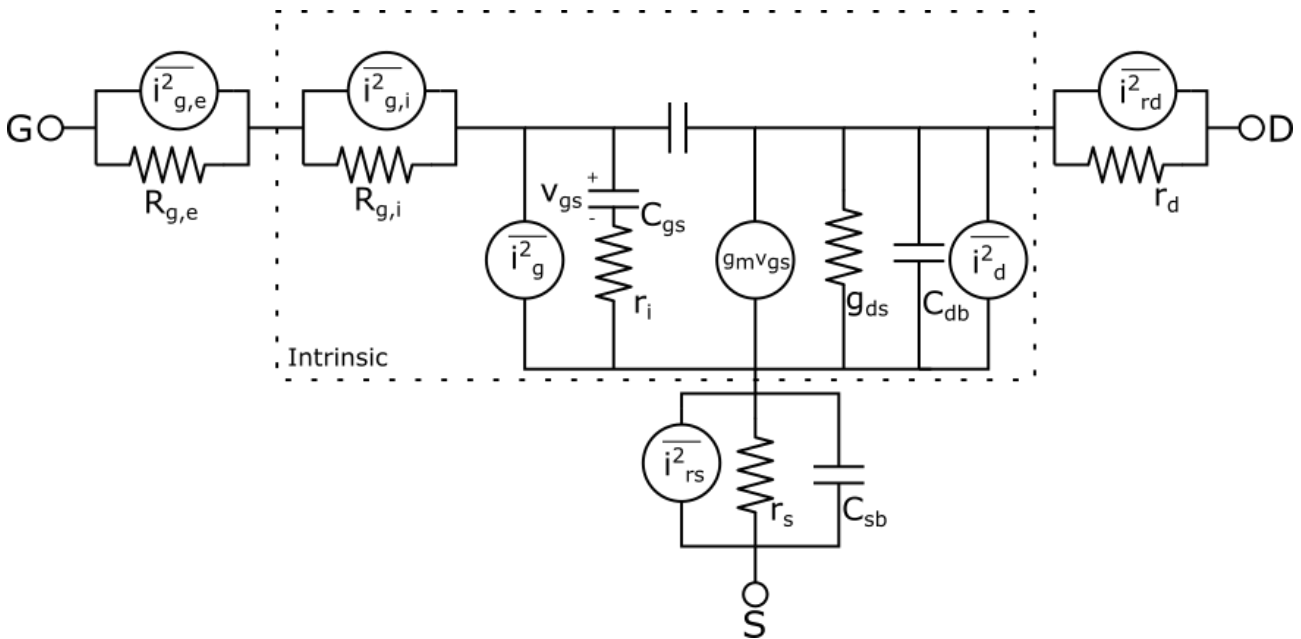


Figure 5.7: High frequency noise model of a MOSFET showing both the intrinsic and extrinsic contributions to the overall noise behaviour.

Figure 5.7 shows a standard high frequency noise model of a MOSFET. The individual parameters are described below:

- $R_{g,i/e}$ - intrinsic and extrinsic gate resistance - arising from metallisation layers of a CMOS stack and bond wires.

- r_d - drain resistance - arising from finite conductivity of a FET drain.
- r_s - source resistance - arising from finite conductivity of a FET source.
- C_{xy} - capacitance between gate, body, drain and source terminals - result of various conductor - insulator - conductor structures distributed across the device.
- r_i - charging resistance (proportional to $(kg_m)^{-1}$) - result of non-zero charging time of the gate capacitance, whcih is dictated by channel transconductance.
- g_{ds} - channel (drain to source) conductance
- $i_{g,i/e}^2$ - Johnson current noise of the intrinsic and extrinsic gate resistance
- $i_{rs/d}^2$ - Johnson current noise of extrinsic terminal resistance
- i_d^2 - Johnson current noise of the channel
- i_g^2 - induced gate noise
- $g_m v_{gs}$ - voltage controlled current source

To account for low frequency effects, e.g. Flicker noise, it is simply required to add a Norton or Thevenin equivalent between gate and source of the device.

All the resistance related sources have a Johnson-Nyquist spectral density:

$$i_{rs/d}^2 = \frac{4kT\Delta f}{R_{s/d}} \quad (5.9)$$

$$v_{g,i}^2 = 4kT R_{g,i} \Delta f \quad (5.10)$$

where $R_{g,i}$ is the value of the gate resistance (dependent on manufacturing and layout). Similarly the thermal channel noise is described as:

$$i_d^2 = 4kT\gamma g_{d0}\Delta f \quad (5.11)$$

where γ is a bias dependent variable. Usually a value of 2/3 is assumed for simple calculation with long-channel devices. For short-channel FETs this value can increase significantly, as it is an increasing function of V_{DS} . No closed form solution exists in literature, to the est of author's knowledge, and numerical methods are often adopted. The key takeaway is that low noise operation requires small drain-source potential.

In the equations above g_{d0} is the transconductance evaluated in the absence of small-signal v_{ds} . Usually a constant value of g_m is assumed for simplicity.

At high frequencies FET deices may be analysed as a distributed RC network. Geurst[10] and van der Ziel [11] show that the first order approximation of the gate conductance is

$$g_g = \frac{1}{5} \frac{\omega^2 C_g^2}{g_{d0}} \quad (5.12)$$

Since it is a conductance term, it has an associated Johnson-Nyquist source:

$$i_g^2 = \beta 4kT g_g \Delta f \quad (5.13)$$

where β is approximated as 4/3 for old technology node MOSFETs. Unfortunately to the best of author's knowledge a more recent approximation of the coefficient does not exist in literature.

More importantly the thermal channel noise and the gate induced noise sources are correlated. It can be intuitively explained: taking a small section of a channel, the thermal current noise generated in that section will give rise to a fluctuating voltage across the small resistive section. Due to capacitive coupling the gate will observe fluctuation in voltage which in turn will induce a fluctuating current at its terminal. Van der Ziel shows that the normalised correlation of the thermal channel and gate induced current noise sources is approximately:

$$C = \frac{\mathbb{E}[i_g i_d^*]}{\sqrt{\mathbb{E}[i_g i_g^*] \mathbb{E}[i_d i_d^*]}} \approx -0.395j \quad (5.14)$$

The resulting correlation value is nearly purely imaginary - which intuitively makes sense - the capacitively coupled signals (voltage across the channel and current out through the gate resistance) will be nearly orthogonal. Absolute value of the coefficient signifies the direction and strength of the correlation, whereas the phase carries further information allowing to estimate one signal from another. In addition, the purely imaginary term signifies no power dissipation and minimal noise of the device.

Finally, to account for low-frequency additions flicker noise must be considered. While there is no consensus on the physical origin of the '1/f' noise, multiple models are presented in literature - The McWorther Model based on number fluctuations and The Hooge Model based on mobility fluctuations. Newer models tend to combine the two propositions into a unified model. For SPICE simulations and hand-calculation a behavioural model is used, though it is considered

a big oversimplification:

$$v_f^2 = \frac{K_f}{C_{ox}^2 WL} \frac{1}{f} \quad (5.15)$$

, where K_f is a device constant, though in reality the exact value is dependent on the operating point of the FET.

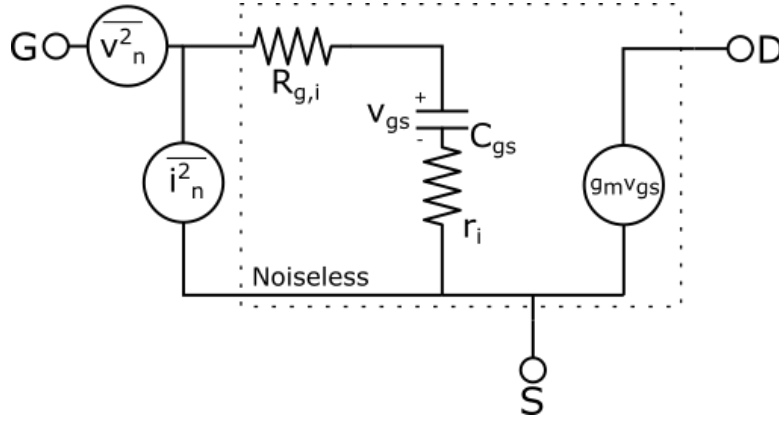


Figure 5.8: High frequency noise model of a MOSFET showing both the intrinsic and extrinsic contributions to the overall noise behaviour.

Taking all of the above into account, the complex FET model can be represented with a simplified version shown in Figure 5.8. The input referred parameters are given by Golio [12]:

$$v_n = v_{g,i} - \frac{i_d}{g_m} + (R_{g,i} + r_i)i_g - j\frac{f}{f_t}(R_{g,i} + r_i)i_d \quad (5.16)$$

Equation 5.16 presented by Golio, appears to neglect flicker noise, as it treats the device as an RF medium. In that scenario, the approximation is indeed valid, since thermal noise density will begin to dominate already in the ultra low frequency region. However, for completeness in simulations presented at a later stage in this chapter, the broadband gyrator model, and in particular the transconductor model, shall be complimented by an independent flicker noise source (equation 5.17).

$$v_n = v_f + v_{g,i} - \frac{i_d}{g_m} + (R_{g,i} + r_i)i_g - j\frac{f}{f_t}(R_{g,i} + r_i)i_d \quad (5.17)$$

$$i_n = i_g - j\frac{f}{f_t}i_d \quad (5.18)$$

where f_t is the intrinsic cut-off frequency due to channel transconductance:

$$f_t = \frac{g_m}{2\pi\sqrt{C_g^2 - (g_m R_{g,i} C_{gs} - C_{gs})^2}} \approx \frac{g_m}{2\pi C_g} \quad (5.19)$$

$$C_g = C_{gs} + C_{gd} \quad (5.20)$$

In summary both M1 and M2 in Fig. 5.4a can be represented as noiseless sources with input noise sources described by equations 5.16-5.18.

5.3.4 Current Mirror

To complete the analysis, the noise contribution of the current mirror needs to be quantified. In this case it is a simple two transistor amplifier as shown in Figure 5.9a.

Half of the current mirror is simply just another common transconductor (M2). This simplifies the analysis as just the noise sources of the diode connected M1 need to be derived. Figure 5.9b shows small-signal model of a current mirror, with respective noise sources. This is a simplified version of the models shown in Figure 5.7.

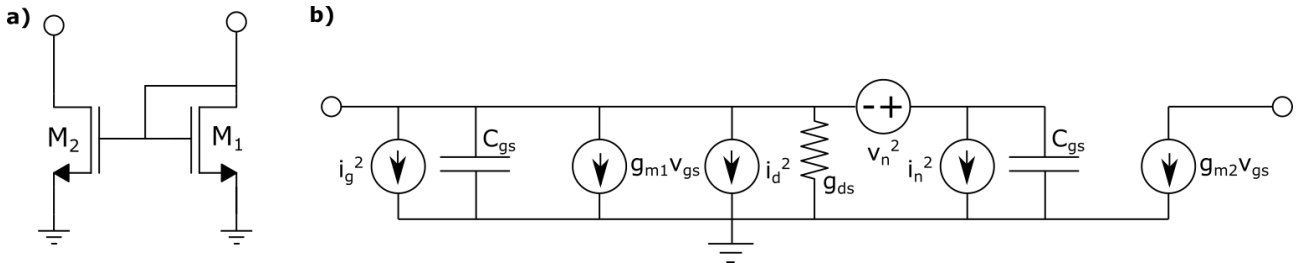


Figure 5.9: Noise model of a simple current mirror adapted from the Ugur and Tarim gyrator. **a)** Transistor level representation of the current mirror. **b)** Small signal model of the simple current mirror. The output FET is represented as a noiseless device with input noise sources defined by equations 5.16-5.18

In theory both M1 and M2 should not be treated independently as their respective noise sources will be at least weakly correlated: thermal channel noise in one device will induce a voltage gate noise in the other device. However to enable first order approximation and allow hand calculations, M1 and M2 are assumed independent.

In diode connected FET i_g^2 term, proportional to the square of the gate capacitance, is largely eliminated due to direct connection of gate to the drain. The main noise source is the Johnson-Nyquist of the channel i_d^2 . Therefore, due to independence of the remaining sources the input referred current noise of the current mirror can be estimated as:

$$i_{nCM}^2 = i_n^2 + i_d^2 \quad (5.21)$$

$$v_{nCM}^2 = v_n^2 + v_f^2 \quad (5.22)$$

where v_f^2 is the flicker noise contribution of the input transistor.

5.3.5 Model Validation

The set of equations 5.3-5.7 defined by physical properties of the Ugur and Tarim gyrator shown in equations 5.16, 5.18, 5.21 and 5.22 were solved numerically for a realistic set of design parameters. These results were then contrasted with TSMC 180nm simulations of the same gyrator. Apart from design parameters, there are 9 key unknowns - the correlation coefficients of the noise sources. Fast numerical approaches allow to quickly simulate various cases. In the following results 6 different cases were adopted: partly correlated sources ($C_{1-9} = \pm 0.5$), fully correlated sources ($C_{1-9} = \pm 1$), one set of random correlation coefficients drawn from a uniform distribution ($C_{1-9} \sim \mathcal{U}(-1, 1)$) and one case with fully uncorrelated sources ($C_{1-9} = 0$).

In the simulations temperature was assumed to be 300K. Subsequently the transconductance of the two single MOSFET OTAs was swept and noise power was estimated. Figure 5.10 summarises the results of the gyrator noise performance as a function of correlation coefficients, transconductance and frequency.

At low frequencies and sufficiently low transconductances (under 10^{-5}S) the flicker noise dominates the response. A clear $1/f$ dependence can be observed in most cases up to around 1000Hz. At those transconductance levels the noise then begins to rise once again at high frequencies, resulting in some operational point defined by frequency and transconductance, where the noise power is at its minimum. The high frequency noise power pick up, can be largely attributed to gate induced noise. As frequency increases the magnitude of the gate voltage noise of a FET increases proportionally. The point at which the high-frequency noise begins to dominate the response is dictated by the transconductance and the gate capacitance. It can be seen in all cases that as transconductance rises, the corner frequency (g_m/C_g) also increases.

Interestingly, at the transconductance of $10\mu\text{S}$ the flicker noise is more prominent. This feature appears in feedback loops such as a gyrator presented here. A clearer trend is observed through the graph, which then becomes proportional to the frequency. Its exact origin is not yet understood, as it is the result of complex numerical approximation.

Above $10\mu\text{S}$ transconductance, the flicker noise is attenuated, and the gyrator operates in extremely low noise mode, dominated by thermal sources only. It must be emphasised that

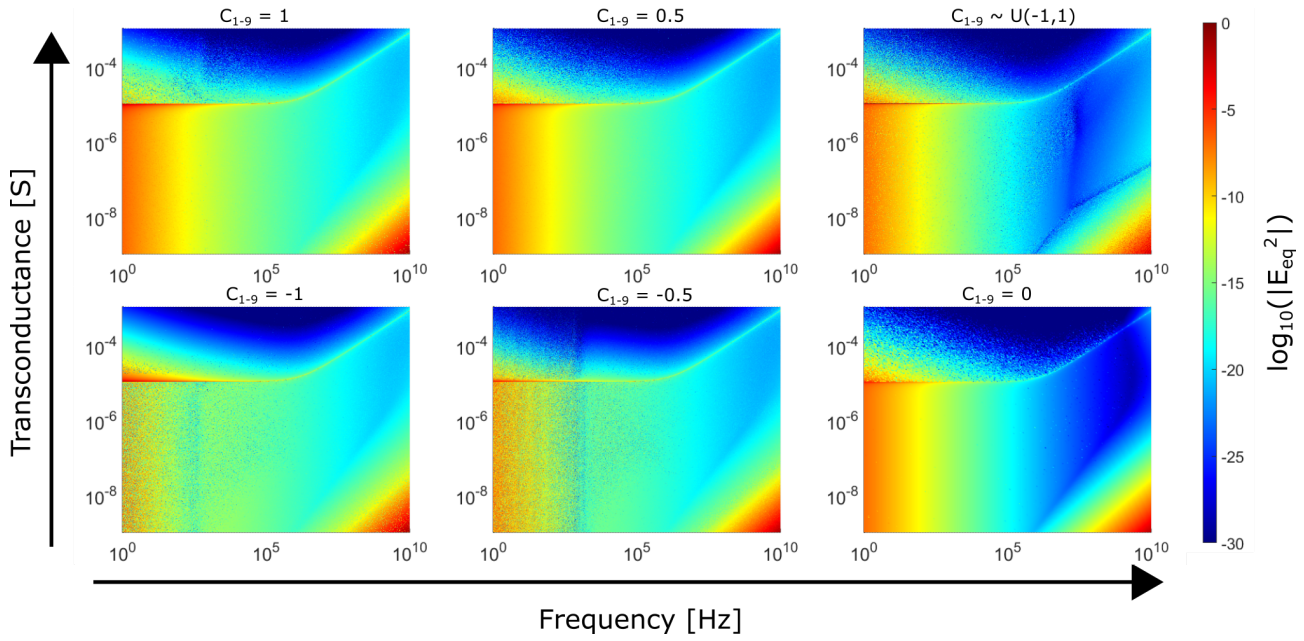


Figure 5.10: MATLAB simulation results of the intrinsic gyrator noise as a function of variable correlation coefficients, transconductance and frequency. The data shows the log of the input referred noise density. Data granularity is set at 1000x1000 sample points. Due to the use of minimisation algorithms, salt and pepper noise is present in the results, stemming from divergence of the approximation.

the noise model is agnostic of the functionality of the gyrators. Therefore the low noise of the transconductor might attributed to the device not functioning as intended.

The noise shape remains largely unaffected by the choice of correlation coefficients. This is a great advantage for numerical approximations, as it exponentially decreases the time to estimate performance of a single gyrator. Having said that, some dependence can be observed: where the C coefficients are either random or all 0, the noise power in the MHz region is substantially smaller, indicated by the deeper blue colour. Rather surprisingly, when negative correlation is present the noise power is as high as with all positive correlation coefficients.

Further evidence that the noise model correctly predicts the behaviour of the gyrator can be seen in Figure 5.11. The derived model (with all zero correlation coefficients) is contrasted at a single instance of transconductance against a simulated SPICE realisation. The shape of the noise closely matches that of physics based TSMC FET models, however the precise values of the noise power can be as much as 10 times off. This can be largely attributed to the mismatch in derived model parameters, which are proprietary belonging of TSMC. As a first order approximation, the above model however correctly predicts the behaviour and therefore allows to deliberate about the applicability of noisy gyrators in large reconfigurable networks.

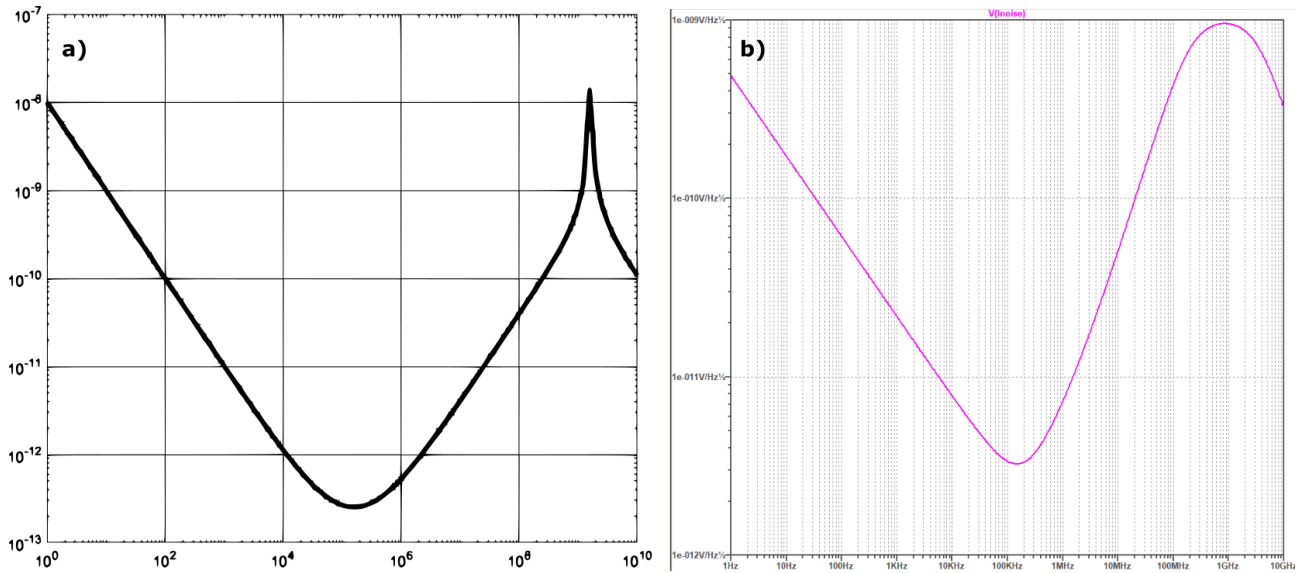


Figure 5.11: Direct validation of the gyrator noise model, through SPICE simulation using TSMC180 FET models. In the SPICE simulation the BSIM4 physics based flicker noise model was used as opposed to simple flicker model used in the derived model ($FNOIMOD = 1$ for SPICE). Horizontal axis represent frequency in Hertz, while vertical axis represent noise magnitude in $V/\sqrt{Hz}$. **a)** One instance of the general noise shape presented in Figure 5.10. Clearly the transconductance is above $10\mu S$ which manifests itself with the 'dip, peak and dip' as frequency increases. **b)** Ugur and Tarim gyrator input referred noise. The gyrator was biased as to be functional.

5.3.6 Noise in Reconfigurable Platforms

It is not uncommon to design a mixed-signal ASIC chip only to find out that it is completely dysfunctional due to large noise factors. In particular low level analogue systems suffer greatly in the presence of high frequency switching on digital side of the chip. Mixed-mode design in itself is an art and requires both electronics expertise as well as common sense and intuition when laying out the design. High frequency clocking signals, like switch mode power supplies, induce extremely high amplitude stray artifacts into nearby signal paths. Since the waveforms are frequently broadband, e.g. square waves, the induced signals are harmonics of the centre frequency.

In general noise can be divided into two sub-classes: inherent noise and interference noise. The interference noise, of which one example is the cross coupling between digital and analogue parts of a systems, can be addressed with informed layout techniques, proper grounding, good power supply noise rejection and any techniques aimed at reducing externally generated interference.

The second sub-class is the inherent noise: noise stemming from device physics and behaviour. On a fundamental level, those are the basic noise mechanisms - flicker, Johnson-Nyquist and others. On a systematic level, the inherent noise of the combined effect of all those sources working in unison, such as an example of the Ugur Tarim gyrator.

Unfortunately, the noise shaping - technique used to boost signal-to-noise ratio, involves frequency translation and is only available in digital systems and data converters. Similarly dithering, which allows to diffuse the error due to high noise in digital systems, has no equivalent in the analogue domain. Therefore two approaches can be adopted when managing inherent noise on analogue platforms such as FPAA: model-driven design and dual data conversion.

These are of course well-known techniques particularly useful in audio signal processing [13]. Other classical approaches include physical filtering, use of chopper amplifiers to address flicker noise or cooling to reduce thermally generated noise. The model-driven approach makes use of the state-of-the art component models. As the understanding of certain phenomena increases over time, the models themselves become more realistic allowing to minimise the noise effect already at the design stage. For instance use of feedback in high gain loops can have detrimental effect on the overall noise figure of a system, as it is demonstrated with the gyrator case. Dual data conversion is not that common in the era of digital storage of information. It involves sampling of the analogue input, digital removal of noise, and final transformation of the signal back into its original domain. Most often, as it is the case with audio signal processing, input signal is sampled, digitally processed and stored in that format, e.g on CDs or flash memory. However an analogue platform such as FPAA, would require the signal to be converted back into the analogue domain.

It is therefore clear that platforms such as FPAA, which are predominately analogue, but pack digital functionality also, will greatly suffer from both sub-classes of noise. However no study so far has concentrated on evaluating the performance of FPAA in the presence of high noise floor. One can hypothesise what the possible findings could be. At this point it is obvious that Ugur Tarim gyrator is far too noisy to be designed in bulk on an FPAA platform. Low frequency contribution of the order of $\text{mV}/\text{Hz}^{1/2}$, suggests that flicker noise will significantly reduce the signal to noise ratio, since gyrators handle an extremely wide range of signals. If the noise shape can be generalised to any gyrator topology, then the use of gyrators on an FPAA fabric must also be questioned, since they only offer reasonable noise levels at a narrow range of frequencies. This may be the price worth paying to achieve analogue reconfiguration.

5.4 Computational Methods

While the presence of many gyrators can lead to disastrous behaviour of the large reconfigurable platform, the development of gyrator-free structures such as memcapacitors and potentially meminductors still hold the question valid: can analogue computation be performed more easily? The fundamental question that needs to be answered is: what are the memristor-filled analogue platforms useful for?

5.4.1 SISO: Single Input Single Output

SISO systems are ever-present: they form a large proportion of all modern day computational units, e.g. digital filters, which take input sample and based on finite or infinite impulse response calculate the next filtered value. The usual way to analyse SISO systems is through the classic Bode plot, root-locus or Nyquist stability criterion tools.

The term SISO is most commonly associated with digital systems, because the input signal is discretised and subjected individually or in limited scope in conjunction with other sequential inputs to various processing techniques, before a single element or value is output. Usually the time step between consequent samples can dictate how well a given SISO system behaves: too large of a time-step and the system is unstable, divergent. Too low of a time-step and the system is computationally too expensive to offer real time performance. Naturally, a compromise must always be struck, leading the design to sacrifice both stability margins as well as computational performance.

Analogue blocks, as envisaged by Mead over 2 decades ago, remove that ambiguity of ideal time-step while improving the real-time performance, which is effectively limited by the speed of the data receivers, be it a data converter or a human eye.

A classic example of a SISO system is an ordinary differential equation (ODE) solver. Employing digital integrators and/or simply numerical methods, a solution can be found. Both of those approaches suffer from rapid accuracy degradation as time-step is increased, or the length of the solution is too large. In this example, notion of symbolical solution, in terms of variables is omitted and the discussion purely focuses on specific solutions to a single differential equation.

Example: Non-Homogeneous Second Order Linear Differential Equation Solver

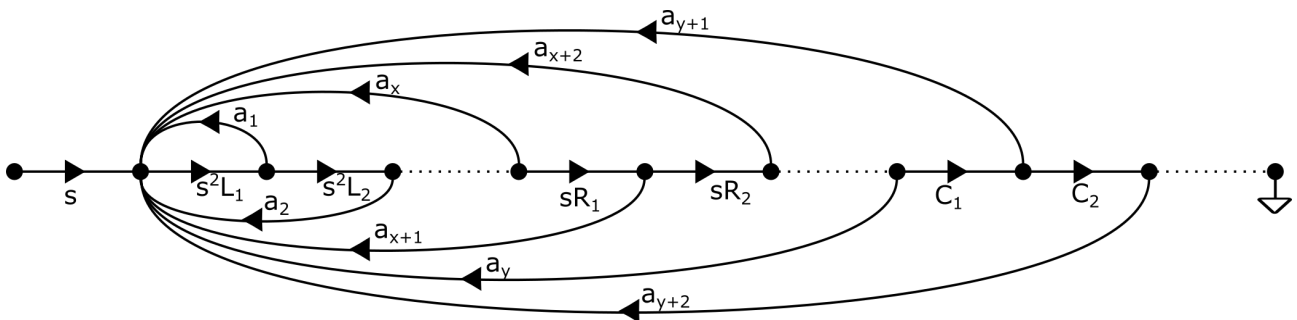


Figure 5.12: Signal flow chart of the second order linear differential equation synthesis and solving circuit, based on fully tunable blocks. The chain series components begins with x inductors, followed by y resistors and concludes with z capacitors. Synthesised equation is provided in Equation 5.28.

The analogue counterpart to fully tunable differential equation synthesis is presented in Figure 5.12. The system is simple a series connection of inductors, resistors and capacitors. Voltage

from each node is then scaled fed back to the input and summed with the input signal. For simplicity of the analysis and discussion the individual similar components are grouped together - that is the chain has first x inductors, followed by y resistors and ends with z capacitors, such that $x + y + z = L$. The input to the differential equation is always voltage, while the current assumes the role of the output. The input signal may first be integrated to give the following form of synthesised equation:

$$v(t) = B_2 i''(t) + B_1 i'(t) + B_0 i(t) \quad (5.23)$$

Without integration of the input the synthesised equation becomes:

$$v'(t) = B_2 i''(t) + B_1 i'(t) + B_0 i(t) \quad (5.24)$$

In the notation above $f'(t)$ signifies the first derivative of function $f()$ with respect to variable t . Coefficients B_{0-2} are realised with variable components. To find the coefficients the following generalisations are adopted. The i^{th} components takes the value of K_i :

$$\text{Capacitor : } K_i = C_i^{-1} \quad (5.25)$$

$$\text{Inductor : } K_i = L_i \quad (5.26)$$

$$\text{Resistor : } K_i = R_i \quad (5.27)$$

Therefore the equation 5.24 can be rewritten in terms of the respective current derivatives, component values and feedback coefficients a_i :

$$\frac{dV}{dt} = \sum_{i=0}^{L-1} \left(K_i \frac{d^{n_i+1}}{dt^{n_i+1}} i(t) \times \left(1 - \sum_{j=0}^i a_j \right) \right) \quad (5.28)$$

where n_i signifies the derivative order of the i^{th} components:

$$\text{Capacitor : } n_i = -1, \quad \frac{d^{-1+1}f(t)}{dt^{-1+1}} = f(t) \quad (5.29)$$

$$\text{Inductor : } n_i = 1, \quad \frac{d^{1+1}f(t)}{dt^{1+1}} = f''(t) \quad (5.30)$$

$$\text{Resistor : } n_i = 0, \quad \frac{d^{0+1}f(t)}{dt^{0+1}} = f'(t) \quad (5.31)$$

Taking into account the assumption that the components are ordered the general equation 5.28 can be rewritten as:

$$\begin{aligned} \frac{dV}{dt} = & i''(t) \times \sum_{i=0}^{x-1} \left(L_i \times \left(1 - \sum_{j=0}^i a_j \right) \right) + \\ & i'(t) \times \sum_{i=x}^{x+y-1} \left(R_i \times \left(1 - \sum_{j=0}^i a_j \right) \right) + \\ & i(t) \times \sum_{i=x+y}^{L-1} \left(C_i^{-1} \times \left(1 - \sum_{j=0}^i a_j \right) \right) \quad (5.32) \end{aligned}$$

By comparing the equations 5.32 and 5.24, coefficients B_{0-2} can be deduced. What is interesting to notice is that each coefficient is composed of one group of component values, e.g. B_0 is independent of resistors and inductors. However, it should be noted that the equation does not immediately provide independence of each coefficient, due to the recurring $\left(1 - \sum_{j=0}^i a_j \right)$ term, which reappears as a consequence of feedback paths. This means that a feedback path associated with the inductor-part of the chain also affects the coefficient realised with resistors and vice-versa. In other words Mason's Gain Formula applies to the system.

The above method in its form allows for infinitely many realisations of a single equation, since there are in total $(3+2(x+y+z))$ parameters to adjust: count of inductors, resistors, capacitors, their respective values and each of the feedback multipliers.

Synthesis by feedback control: By further restricting some parameters the above equation can be greatly simplified allowing to more easily compile the solution. For example by enforcing the following:

$$R_i = R \quad (5.33)$$

$$L_i = L \quad (5.34)$$

$$C_i = C \quad (5.35)$$

$$\sum_{i=0}^{x-1} a_j = 0 \quad (5.36)$$

$$\sum_{i=x}^{x+y-1} a_j = 0 \quad (5.37)$$

that is, by ensuring that all like components are equally valued and that the sum of feedback coefficients for the inductive and resistive parts is zero, the coefficients can be written as:

$$B_2 = L \left(x - \sum_{i=0}^{x-1} (x-i-1)a_i \right) \quad (5.38)$$

$$B_1 = R \left(y - \sum_{i=0}^{y-1} (y-i-1)a_{x+i} \right) \quad (5.39)$$

$$B_0 = C^{-1} \left(z - \sum_{i=0}^{z-1} (z-i)a_{x+y+i} \right) \quad (5.40)$$

The conditions in 5.33-5.37 provide two benefits. Firstly they further restrict the family of synthesis solutions. However the total pool of all possible realisation of a single differential equation still remain infinite. Secondly, the conditions allow the coefficients to be fully independent of one another. That is, changing feedback and/or component values in one group of components does not affect the coefficient associated with other passives.

Theoretically this method requires just 5 components to realise any second order differential equation of the given form. This can be easily seen, by examining the cases where $x = y = z = 1$, that is there are only three elements. Due to the conditions in 5.36 and 5.37:

$$a_0 = a_1 = 0 \quad (5.41)$$

Therefore the coefficients become:

$$B_2 = L(1 - 0) = L \quad (5.42)$$

$$B_1 = R(1 - 0) = R \quad (5.43)$$

$$B_0 = C^{-1}(1 - a_2) \quad (5.44)$$

Clearly, with just three elements both B_2 and B_1 are forced to be positive and equal to the value of component used. By allowing $x = y = 2$ and $z = 1$ the following is realised:

$$a_0 = -a_1 \quad (5.45)$$

$$a_2 = -a_3 \quad (5.46)$$

$$B_2 = L(2 - a_0) \quad (5.47)$$

$$B_1 = R(2 - a_2) \quad (5.48)$$

$$B_0 = C^{-1}(1 - a_4) \quad (5.49)$$

By choosing appropriate values of $a_{0,2,4}$ any ODE of the second order form discussed here can be realised with just 5 components (2 inductors, 2 resistors and 1 capacitor, along with five feedback amplifiers and a single summer). This unfortunately only holds in theory. In practice, the presented method requires ultra-fine setting of feedback coefficients due to practical limitations in realising component values. For example, to realise $B_0 = 1$ with a 1pF capacitor one would have to be able to set $a_4 = 1 - 10^{-12}$, which is impossible.

This problem is independent of the component count. Even with long chain of capacitors a relatively minuscule gain would have to be realised precisely. This alone renders this synthesis method impractical.

Synthesis by Component Value Control: This method puts a restriction on the feedback components. By assuming that elements a_i can be described by a geometric progression:

$$a_0 = \frac{3}{2} \quad (5.50)$$

$$a_i = -\frac{1}{2}a_{i-1}, \quad i \in [1, x-1] \quad (5.51)$$

$$a_x = \frac{3(1-\gamma)}{2} \quad (5.52)$$

$$a_j = -\frac{1}{2}a_{j-1}, \quad j \in [x+1, x+y-1] \quad (5.53)$$

$$\gamma = \sum_{k=0}^{x-1} a_k \quad (5.54)$$

$$\mu = \sum_{k=x}^{x+y-1} a_k \quad (5.55)$$

the coefficients can then be described by the following equations:

$$B_2 = \sum_{i=0}^{x-1} L_i \left(-\frac{1}{2}\right)^{i+1} \quad (5.56)$$

$$B_1 = \sum_{i=0}^{y-1} R_{x+i} (1-\gamma) \left(-\frac{1}{2}\right)^{i+1} \quad (5.57)$$

$$B_0 = \sum_{i=0}^{z-1} C_{x+y+i}^{-1} (1-\gamma-\mu) \left(-\frac{1}{2}\right)^{i+1} \quad (5.58)$$

$$(5.59)$$

Clearly there is a strong interdependence between all terms, due to reappearing feedback coefficients γ and μ . That is a feedback components appearing in the B_0 coefficient does also reappear in the definition of B_1 . However the advantage is that geometric feedback progression with values whose absolute value is below 1 can be easily realised with a passive binary ladder. In particular, in this case where the values are scaled by a factor of $-1/2$, simple R-2R ladder would prove most useful. Of course there is still need to use inverters in every other feedback, but the count of active elements is essentially halved.

While there is an interdependence in the B_{0-2} terms, due to geometric progression, that value is bounded. For example the term γ which appears in both B_1 and B_0 , and is the sum of feedback coefficients in the inductive portion of the chain, in the limit converges to a value of 1, but never reaches it, thus allowing to control the value of B_1 . If in fact an infinite number of inductors was used, in theory B_1 would be forced to 0, but for entirely different physical reasons.

The key problem with the following approach is the limitation on the range of synthesised coefficient values. The values of B_{2-0} are forced to be of the same order of magnitude as the value of components used. For example trying to synthesize $B_2 = 20 \times 10^{-9}$ having tunable inductors with the range of 1 to 10nH is in fact impossible. Firstly by ensuring that all the negative terms are minimised, i.e. by setting $L_i = 1nH$ for $i \in [0, 2, 4...]$ and by maximising the other terms: $L_i = 10nH$ for $i \in [1, 3, 5...]$:

$$\begin{aligned}
 B_2 &= \sum_{i=0}^{x-1} L_i \left(-\frac{1}{2}\right)^{i+1} = \\
 &= \left(-\frac{1}{2}\right) \times 1n + \left(\frac{1}{4}\right) \times 10n + \left(-\frac{1}{8}\right) \times 1n + \left(\frac{1}{16}\right) \times 10n + \dots = \\
 &= -\frac{2}{3} \times 1n + \frac{1}{3} \times 10n = 2.67n \quad (5.60)
 \end{aligned}$$

Clearly the maximum value of B_2 is the weighed average of the minimum and maximum component value. The same argument can be repeated to obtain a lower bound and also for other coefficients. However this is not necessary as the above example sufficiently illustrates the problem of using this method.

Reasons to pursue other synthesis methods: The two methods presented are by no means exhaustive. They are merely two possible ways of realising the differential equations. There are in fact countless other methods that could prove a lot more useful. If one such method is found, which feasibly allows to set any values to B_{0-2} then this analogue method may indeed be practical. In particular, in the advent of emerging technologies such as memcapacitors and even potentially meminductors, this could be an advantageous method for fast, accurate and efficient synthesis.

Needless to say, both methods presented do not hold valid even with gyrator-based structures. One would be strongly advised against using the building blocks to realise such long chains, as too many gyrators will almost certainly lead to oscillatory behaviour. Furthermore, gyrator based approach for long chains would dominate the power budget of the system.

Nonetheless, with the possibility of using truly passive mem-devices, the chain approach to solving differential equations may prove very useful.

5.4.2 MISO & MIMO: Multiple Input Single/Multiple Output

Multiple input systems, both MISO and MIMO, are significantly harder to analyse because of the larger number of parameters. Stability in one dimension, that is for one input, does not at all guarantee stability in another dimension. For extremely large input space it can

prove computationally impossible to exhaustively characterise the system. It may be possible to simplify the problem with the use of multivariate extensions of the single-variate stability theorems.

MISO Example: Complementary Filtering

However, arguably, multiple input systems are that much more fascinating. For example, in robotics it is often desired to accurately determine the physical position in three dimensional space, utilising all 6 degrees of freedom (DoF): three for translation in x, y and z direction as well as three for rotational orientation: pitch, yaw and roll of the system. To achieve that often an inertial measurement unit would be used, an IMU for short. Typical of the shelf IMUs incorporate both accelerometer and a gyroscope. Some even add magnetometer, giving a total of 9 degrees of freedom.

A common use of an IMU is to determine an inclination on which the system is based (Figure 5.13a). This is more complicated when the system itself is constantly changing speed and/or direction. In a stationary or non-accelerating system, accelerometer suffices to achieve the task. Since accelerometers measure proper acceleration¹, input from gravity is accounted for. Knowing IMUs original frame of reference figuring out the inclination simply requires the system to calculate an appropriate Euler angle - pitch, roll or yaw.

The same could be achieved with a gyroscope, which measures the rotational velocity represented in radians per second. Simply integrating the output of the gyroscope results in rotational displacement. The problem with MEMS based IMUs is firstly that they are prone to short-term drift. Since the mass embedded inside the measurement unit has inertia, the mass-based measurement will always lag behind the true movement of the system. Secondly, as any mechanical system, relaxation of the MEMS springs when the object is stationary can lead to creep in data. Furthermore, digital integration often leads to ever-increasing error due to finite resolution of data and inaccuracy of the gyroscope. In the presence of noisy output of the IMU, integration leads to a growing error described by a random walk process.

It appears that accelerometers are the go-to tools for measuring inclines. However the problem arises in accelerating systems, since the MEMS mass is now subjected to both gravitational acceleration and systematic acceleration. In that scenario it is simply impossible to accurately determine the angle. At the same time, relying on just the gyroscope can only be temporary. For that reason complimentary filters are used. A simple first order complimentary filter for an IMU, which measures inclination in the XY plane can be algorithmically described as:

¹In relativity theory, proper acceleration is measured relative to a free-fall.

$$\theta_{acc} = \tan^{-1}\left(\frac{y}{x}\right) \quad (5.61)$$

$$\theta_{gyr} = \theta_{filtered_{i-1}} + \omega_z \times dT \quad (5.62)$$

$$\theta_{filtered_i} = A \times \theta_{gyr} + (1 - A) \times \theta_{acc} \quad (5.63)$$

where θ_{acc} is the angle estimation from accelerometer, ω_z is the angular speed in the z-axis from gyroscope and A is some filtering parameter whose value lies between 0 and 1. This first order filter, greatly reduces the drift of gyroscope-only data, and reduces the error caused by system acceleration.

The same system could be employed on an FPAA platform, where the two data streams would be filtered, integrated and their weighted summation would be performed in fraction of the time required to do so on a digital platform. The idea of complimentary filtering can be expanded to larger multi-input systems. This can be thought of as a simplified Kalman filtering, based on measurement and observation vector (Figure 5.13b). In the industry this is called sensor fusion and extended Kalman filtering is the preferred method of choice.

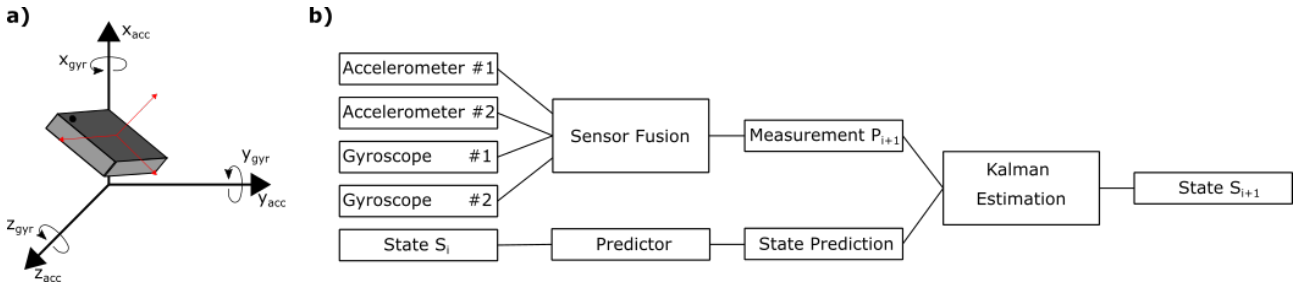


Figure 5.13: Sensor fusion as an example of multiple input single output system. **a)** IMU is rotated with six degrees of freedom with respect to some original frame of reference, here shown as the black coordinate system. The challenge is then to find the three angles through which the IMU has been rotated. **b)** An example of a simple pipeline showing how Kalman filtering is accomplished using sensor fusion. The blocks show arbitrary functions such as state prediction and state estimation.

MIMO Example: Image Processing

MIMO systems are envisaged to show the true colours of the multimodal, high density, very large scale arrays. Due to architectural parallelism and physics-based computation the execution time for a single and thousand multiply-accumulate (MAC) operations is simply determined by signal propagation time, assuming there is enough hardware to accommodate all MAC operations at once.

This is very advantageous when processing large matrices, such as images: FPAAs similarly to graphical processing units are extremely well-suited to solve matrix-based problems. Memristor

crossbar arrays have already been demonstrated to perform edge detection very well, with large number of publication available on that subject (e.g. [14]). Converting RGB pixels into grey-scale and then further converting the shade of the pixel into potential allows to quickly find edges in an image. An edge will correspond to pixels having extreme shade values, thus forcing larger current through a memristor, causing its resistive level to shift on average more than non-edge memristors.

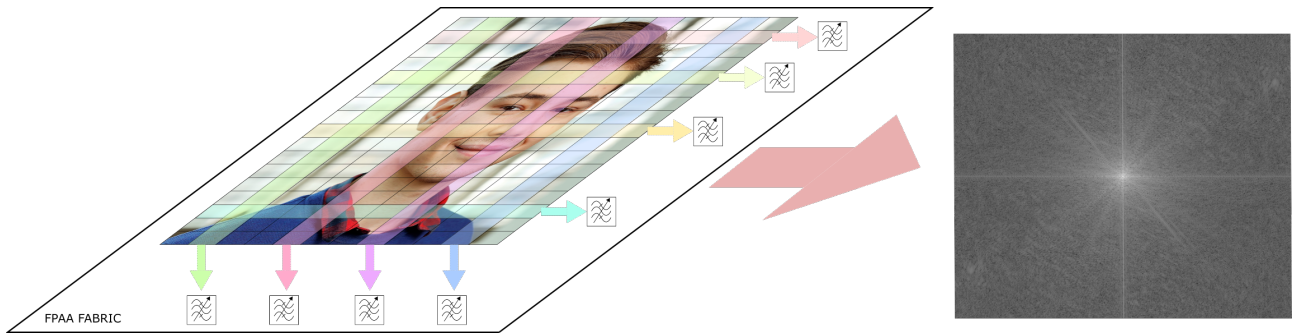


Figure 5.14: Fast image processing application. Accurate Fourier decomposition of the image may be performed in real-time with banks of reconfigurable filters. The Fourier signature could then be compared against stored values to identify the contents of the image. More complex techniques can be further adapted to allow for a more robust recognition performance.

Similarly the concept can be extended to pattern detection in images with arrays of reconfigurable filters (Figure 5.14). By encoding a specific pattern of image frequencies which correspond to certain objects, for example a face, an image with certain characteristics can be taken and passed through the array of filters. Simplest way to view this is as Fourier decomposition. Similarly to 2D waveforms, such as square waves, 3D shapes - 2D faces with colour - have certain unique Fourier signature. Of course Fourier decomposition on its own, will significantly underperform compared to state-of-the-art digital methods. However, the advantage of FPAA platforms is that they enable "hardware-isation" of most software algorithms, such as feature detection, tracking and many more.

The clear obstacle is that images are inherently digital, and therefore image scaling, could potential limit the performance of such a system. However the same problem is present in digital computation, and hence the solution can be translated into analogue world quite easily.

5.5 Applications

This chapter has so far illustrated what still needs to be done to enable powerful analogue computation. There are clear limitation - high noise factor or gyrator-rich structures, feasible computational methods and a cutting-edge architecture which would host the entire platform. Once those issues have been addressed many applications would be just within reach. These are illustrated in Figure 5.15 and discussed individually below.

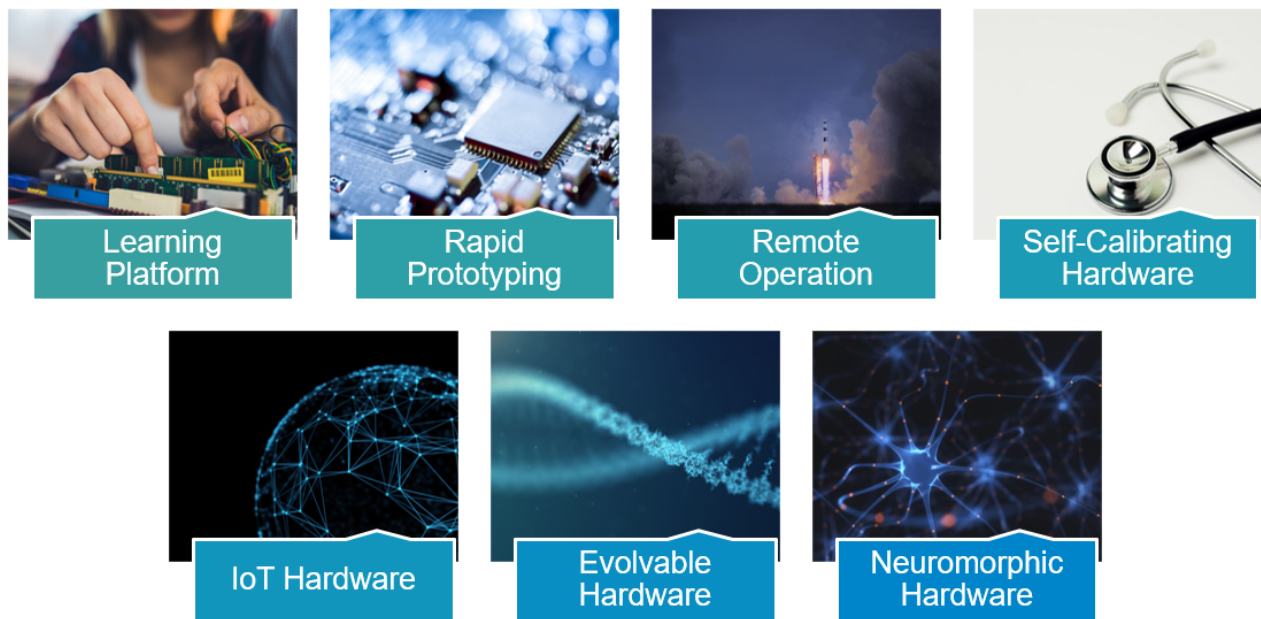


Figure 5.15: Taxonomy of applications of analogue reconfigurable platforms.

A transistor switch produces heat every time it switches. Modern digital platforms pack billions of transistors switching at gigahertz levels. Heat dissipation is becoming increasingly problematic as chips scale. A given computational problem is usually performed until certain precision is reached to save time and energy. Therefore from the start, digital computers present the user with a choice - precision or time and power efficiency. This problem, while still pertinent on analogue platforms, is less critical. Switching losses are minimised and precision is limited by the choice of data converters and available signal-to-noise ratios. With added techniques of noise shaping or sample averaging the precision can be made arbitrary.

The extra performance margins enable a whole spectrum of applications. Beyond the discussed differential equation solvers, and signal conditioners, an analogue platform can act as rapid prototyping machine for analogue IC design, similarly to FPGA. FPAA are thought to open up new educational paths as they allow virtually any circuit synthesis.

The FPAA can act as instrumentation, and with system-on-chip realisations already present, integration into wearable electronics is just an engineering problem. EEG wearable headset are often limited by the battery lifetime. FPAA offer theoretically improved power management for the same processing capability.

Finally, analogue reconfigurability is attracting attention for applications in harsh and inaccessible environments, e.g. space exploration. Performing low power system-wide reconfiguration or tuning to mitigate the effects of offsets, noise or drift could be made simpler with an analogue platform such as this one. Importantly, initial research suggests that some memristors are radiation hard, enabling the space application.

Learning Platform

Possibly the lowest hanging fruit is to use analogue reconfigurability as a learning tool. Current alternatives include either direct SPICE simulation or breadboard prototyping. FPAA based learning platforms offers to combine best of two worlds - one one hand it allows for interactive operation, similarly to SPICE, enabling changing of component values "on the fly". On the other hand, the synthesised circuit is real, just like one on a breadboard, thus allowing to appreciate the physical and practical limits of standard building blocks such as inductors or operational amplifiers.

Since the board is packed with many practical ready-made blocks, as single platform could suffice to characterise FET transistors, memristor or learn about filter topologies - all in one environment. The precursor of FPAA technology, Hasler, has taught a course based on the group SoC FPAA architecture [15].

Rapid Prototyping

The use of the FPAA as a learning platform can be extended to research and industry. It enables quick idea development and can be used for feasibility studies. The platform by no means, is designed to produce optimal results. Similarly to FPGA, there would always exists an ASIC realisation that will be at least as good in the metric of choice as the synthesised solution.

The common pitfalls of integrated circuit development involve poor technology modelling and lack of simulated external parameters such as EM radiation and other noise sources. Additionally typical IC development can take months and even a year. FPAA, while it doesn't substitute the process at all, it supports it. An FPAA designed in the technology of choice, could in fact enable clearer understanding of device performance and limitations. At the same quick prototyping could save months which would otherwise be spent designing and laying out flawed and/or dysfunctional systems.

Remote Operation

Remote operation requires a system to adjust itself without human intervention. Imagining the FPAA capabilities can be expanded into radio frequencies, there is a number of interesting applications, including adaptive impedance matching and beam steering. It is easy to envisage this kind of platform used in space exploration, where hardware intervention is not straightforward. The Jet Propulsion Lab of NASA has conducted a study of FPAA usage in space environment in 2007 [16], which has not been followed up.

Self Calibrating Hardware

Associated with the remote operation, is self-calibrating hardware. A classic problem of design for long lasting analogue systems is the inherent drift and creep. Similarly designing analogue systems whose performance will remain unchanged over wide temperature ranges, is difficult and costly, supported mostly by military-grade electronics. Even with temperature compensated architectures, there are inherent discrepancies, whose effect remains uncalibrated. In all those scenarios, provided the space allows for it, an FPAA platform could be implemented to provide dynamic system calibration.

IoT Hardware

Following from remotely operated hardware, it is just a stone's throw towards Internet of Things applicability. A remote system like that has been demonstrated with FPAA platforms [17]. While the connectivity itself is not a feature of the FPAA, rather an extra protocol both in hardware and software is necessary, the combination of the two opens up new possibilities.

First of all, the platform could play the role of a virtual environment. A centralised hardware bank, similar to servers, allowing for easy access could be used to synthesise large and complex systems, utilising many platforms, without the need to relocate the platform from user to user.

Secondly, with the added connectivity, the devices can be used for sensing and actuating applications without the need for human intervention. More over the sensed data can be pre-processed in analogue domain on the platform before being streamed to the user, thus saving bandwidth and power simultaneously.

Evolvable Hardware

Possibly most exciting application of the FPAA is the idea of evolvable hardware. While not new, this idea has so far failed to engage the community due to lack of feasible approach. Evolvable hardware brings the genetic algorithms to physical structures potentially allowing to realise far more efficient, non-intuitive solutions to common problems, further progressing the state-of-the-art.

Genetic algorithms, based on nature, allow for a supervised expansion of capabilities, particularly those skills which closely match the desired behaviour. Starting with a random population of systems, their desired characteristic is measured - be it the transfer function or the bandwidth. The systems whose behaviour most closely matches the set out fitness function are somehow modified and a new population of test systems is produced. This process continues until performance gains between each population reach the threshold level.

This approach has a number of benefits - first of all, it requires minimal input from the user. Once programmed, the system converges towards a solution. Secondly, it is not uncommon for the algorithm to produce a number of successful genetic mutations, which all evolve until the last population, thus giving a choice to the user, based on additional metric.

The disadvantages are obvious to realise: genetic algorithm is a numbers game. Both time and large populations are required to increase confidence that a solution will be generated, and that the solution will be optimal. Therefore evolvable hardware can be extremely slow and power consuming, but it can also be rewarding in terms of designed system performance.

Neuromorphic Hardware

A generalisation of the above concept can be made. Neuromorphic hardware spans a broad area of research. Synaptic behaviour is often reproduced with memristors, which in similar fashion perform multiply-accumulate function extremely well. It is there not surprising that a lot of effort goes into realising hardware versions of common neural network algorithms. FPAA filled with memristors could be easily converted into extremely vast and equally fast neural network. As opposed to software methods, which are often limited by code parallelism and number of truly parallel threads, and number of available cores, analogue artificial neural networks are simply limited by hardware propagation time. While this idea has already been introduced in FPGA, in-memory computation enabled with memristive devices has a theoretical advantage over digital methods.

There are recent attempts to exploit the analogue dynamics of memristive devices to design novel high-performance circuits and systems for unconventional computing. These include the systematic methodology proposed in [18] to design memristor memcomputing cellular nonlinear networks, as well as the exploitation of the local-activity of certain volatile memristor physical realisations [19] to develop oscillatory networks for problem solving [20] applications or biological system modelling [21].

5.6 Conclusion

This chapter discussed some of the strengths and weaknesses of memristor tuned hardware, when used as building blocks for field programmable analogue array platform. On one hand there is the appeal to use the memristive devices for all kinds of tuning purposes, on the other hand comparing to digital methods, analogues still need refinement. There are some early forays into FPAA architectures, and this Chapter has discussed how the current architectures would need to be modified to accommodate the memristive blocks. As complexity of the platform scales up, routing is expected to be the dominant source of inaccuracy and performance

limitations. Therefore it is suggested that the interconnect fabric is equally important as, if not more than, the analogue computational blocks themselves. This is because without a well-designed fabric the performance of the CABs will suffer.

Having solved the architecture problem, the next challenge is using the analogue blocks to do something useful. Forgetting about the ever-present issues of analogue components, such as SNR, drift, tolerances and so on, the Chapter has shown that using device physics as postulated by Mead 30 years ago [5], is not that straightforward; the devices come with their own limitations. As an example, it was discussed that one potential method of second order differential equation synthesis would require the capacitive tuning down to 12 decimal places, which is simply impossible. Therefore abandoning classic digital arbitrary precision architectures has to be accomplished cleverly.

At the moment, there exists no non-volatile analogue memory which can store a byte of information on an effective area comparable to flash memory for instance. Invention of such a memory cell will open up more engineering challenges. How does one perform precise computation? What architecture is required to store other types of variables such as *double* or *long* onto the analogue unit? What would that same architecture need to have in order to enable in-memory computing on a distributed set of information, i.e. information that is stored on multiple analogue cells? How to efficiently store that information, so that routing for in-memory computation is optimised? At which point should the transition between analogue and digital computation occur? These are just some of the open questions to which there is yet no answer.

Coming back to the main point, synthesis comes at a cost - large noise and power consumption. While operation using device physics is definitely more efficient than current digital methods, analogue reconfiguration introduces large overheads: biases. In order to achieve ubiquitous, general purpose behaviour the systems must be designed to accommodate all flavours of signal and must allow to use memristors in their natural regions of operation - presently in the few to few hundred kilo Ohms region. All those restrictions render the circuits extremely inefficient, for what they offer to the designer. Perhaps it is the case that general purpose analogue reconfiguration should be application targeted, thus allowing to optimise the performance for the specific application. Or perhaps a different method of achieving what was described in this chapter, which does not require the use of the FPAA platform, will be invented.

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Chapter 6

Conclusion

This thesis has attempted to answer a fundamental question: is memristive technology mature enough to enable some interesting applications such as functional reconfiguration of analogue circuits. As with any research question, the answer is non-binary, it cannot be simply categorised into 'yes' or 'no' regime.

The work demonstrated in this thesis has shown that for limited time, well-defined memristors are excellent parameter and functionality tuners. The technology is still unreliable; it is impossible to manufacture two perfectly identical memristors which will respond in the exact same way to a given set of stimuli. Poor bandwidth further limits the use of memristors in high frequency systems, where the signals directly interact with the devices. At the time of writing this thesis, memristor can be used only as part of the bias network, where both voltage and signal frequencies are tightly bounded and controlled.

Still, there is a great promise in utilising memristors as functionality switches on platforms such as field programmable analogue arrays. As demonstrated in this thesis and numerous other authors, analogue computation is superior to digital in terms the speed/power trade-off.

Experiments carried out in this work used active impedance synthesis as a platform for discussion. The approach was selected as currently it is difficult or impractical to realise high bandwidth, large range and low power tunable inductors and capacitors. This lack of effective value control of analogue elements is one of the primary reasons why analogue computers heavily lack in performance compared to their digital counterparts. Efficient and effective analogue computers present designers with the added challenge of performing computation in the physics realm, rather than logic space. This is an added to challenge to already present drift, thermal variations and precision linked to fabrication tolerances.

As demonstrated, the first step towards analogue computation is realising fundamental instrumentation. Basic filters and signal generators were presented, where memristors played the role of system tuners, e.g. controlling quality factors, cut off or centre frequencies, controlling

pulse widths and even completely changing the topology of the filter from low pass to notch and more.

Detailed summary of the main thesis achievements follows below.

6.1 Summary of Thesis Achievements

Chapter 2

The background chapter to the best of author's knowledge is first of a kind and most detailed treatment of the topic of reconfiguration. The discussion traces the history of analogue memory and system reconfigurability, from early forays such as mechanical potentiometers as neural weights storage devices. The literature review then covers some of the currently used methods which allow to store continuous or analogue data, such as popular floating gate FET devices. Following that the discussion focuses on resistive switching phenomena and builds the overview from ground up. Starting from history, through atomic description to phenomenological modelling, the review is completed with a summary of currently research memory elements - memtransistors, memcapacitors and theoretical higher order elements. The component level reconfiguration is then followed by systematic reconfiguration, through the introduction of platforms such as FPGA and FPAA. The long dominance of digital reconfigurability is explained and the platform is contrasted against the analogue ones. The narrative then continues with resurrection of analogue methods - their history and future impact are presented.

Chapter 3

This chapter introduces the building blocks, which are effectively memristor controlled variable inductor and capacitor. The chapter begins with theoretical description of the gyrator based blocks and lists the limitations of the approach. For the first time, a memristor-controlled gyrator is shown, and memristor tuning is demonstrated. A theoretical discussion of the N-gyrator system follows showing that many star connected gyrators can in fact produce a high quality resonator.

The gyrator-based building blocks are designed on PCB giving a good testing platform for the subsequent experiments. Properties of tunable capacitors and inductors are examined showing that inductances as high 50H can be feasibly realised on a PCB (while IC demonstration has shown 10mH, 6 orders of magnitude higher than similarly sized spiral inductors). The results of capacitor tests have shown that gyrator-based tunable capacitors are extremely delicate and require special stabilisation in order to operate as intended.

Chapter 4

Chapter 4 delves into parametric and functional analogue circuit tuning. Each circuit application highlights what the potential problems and advantages are. Beginning with just one active element a lead-lag filter is realised. By simply tuning the value of the memristor the behaviour of the filter changes from lead to lag and vice-versa. Using two active elements, this work demonstrated that high Q RLC filters are attainable, where both the Q factor and resonant frequency can be independently controlled. Moving onto more practical circuits, two active elements were used to pre-process a real EEG signal and decompose it into its constituent bands. The section on filters is concluded with two SPICE simulations using TSMC180 technology, showing other more direct methods of parametric and functional tuning, without the need to synthesise intermediate properties, such as reactance.

The chapter then presents two tunable waveform generators. Notably one of the methods is based around recently modelled memcapacitive behaviour, which is tightly linked to memristive switching. The discussion on memcapacitance completes the original publication, as the authors neglected to further understand the consequences of the behaviour they described.

The chapter finishes with closing remarks on the suitability of memristors in modern day applications, showing effectively that the basic functionality is there. Nonetheless, as already mentioned a few times, the technology needs to mature before real commercial applications can be generated.

Chapter 5

Chapter 5 tackles the subject of physical computation. It begins with introduction of the possible platform capable of hosting large quantities of analogue components, which could individually be tuned by memristive devices. Owing to work of other research groups, the concept of memristor post-fabrication on top of CMOS is exploited. Possible issues stemming from a gyrator-rich architecture are then discussed, showing that gyrator noise can in fact greatly limit the performance of the FPAA by significantly lowering the SNR and hence reducing the resolution of the underlying computation. The discussion then continues with the assumption that the problems and imperfections can in fact be resolved. Various analogue computational methods are proposed which would benefit from reconfigurable analogue blocks. Finally, the chapter concludes with an overview of possible applications of a functioning platform, if ever one will exist.

6.2 Future Work

6.2.1 CMOS Testing

All of the work presented in this thesis is either based around discrete components on a PCB or is a result of theoretical simulation. To further the knowledge of those blocks it is advised that integrated circuit realisation of the most promising topologies are designed, fabricated and tested. This is in part already taking shape, with work of Jiawei Shen (see Appendix C). However further effort is required to bring to life gyrator-less topologies presented in Chapter 4 - biquadratic filter or linear-logarithmic multivibrator. This is possibly the lowest hanging fruit which is the result of this work.

6.2.2 Memcapacitance

In preparation for the next stage, it was envisaged that this work would address the ambiguity of memcapacitive switching on memristive devices. A lot of publications mention that memcapacitance is sometimes observed as a by-product of resistive switching. However, to the best of author's knowledge, there is no conclusive study whose objective is purely this phenomenon. There are a few hypotheses as to why this behaviour is observed - some attribute it to the modulation of the effective dielectric constant, others claim that is the result of filament formation which reduces the plate separation of the capacitor.

In preparation for this work, an automated read out instrumentation was developed based on precision component analyser Wayne Kerr 6440A. The software written for the automated memcapacitance read out can be obtained from the author. Due to the pandemic this work was interrupted.

Moreover, three terminal memcapacitor topologies form an interesting testing platform, where the standard metal-insulator-metal stack is replaced with metal-insulator-metal-insulator-metal, thus potentially allowing to realise low-quality highly tunable, CMOS compatible memcapacitors.

6.2.3 FPAA Computation

While the concept of FPAA may seem an attractive, it requires further development and understanding of the basic computational methods. Many propose fairly simple multiply-accumulate based algorithms, such as vector multiplication. It is clear that analogue components are capable of so much more, as already demonstrated in Chapter 5. Rather than simply exploiting

memristive history, and basic current addition, physical phenomena linked for example to integration and differentiation of capacitor and inductor ought to be intelligently exploited. One such attempt was made with a ODE solver proposed in Chapter 5, however the methodology lacked realistic and feasible synthesis method, as it was limited by the accuracy with which certain physical parameters can be realised. It is therefore encouraged to research more scalable approaches to analogue computation which will leverage the concept postulated by Mead 30 years ago.

6.2.4 Theory of Evolvable Hardware

While there was some interest into systematic circuit design, otherwise known as evolvable hardware, the results did not make an impact onto the scientific community. However, until recently this concept was solely built around standard and well known components and methods. The tuning elements were switches and transistor controlled current sources. With the introduction of memristive tuning and IC integratable impedance synthesis, the idea of supervised circuit evolution could once again be re-investigated. The implications of a successful methodology, as discussed in Chapter 5, could be truly immense, changing the way circuits are designed these days. It is possibly the most exciting, at the same time, the most challenging proposal for future work, based around the building blocks described in this thesis.

Appendix A

Nealder Mead Simplex Implementation

A.1 Introduction

Nealder Mead Simplex (NMS) algorithm [1] is a heuristic approach that is commonly used to optimise (to find a global minimum of) a non-differentiable objective function. As most other similar algorithms, NMS can also be easily applied to multi-variable differentiable functions in order to save time by manually computing all the partial derivatives of the function.

A.2 Use of NMS in Parameter Extraction

As seen in Chapter 3 an example of the objective function is the case of tunable inductance is:

$$J(R_{ESR}, L, R_L) = |V_{in} \frac{R_L}{R_L + R_{ESR} + sL} - V_{Meas}| \quad (\text{A.1})$$

The difficulty in computing the partial derivatives by hand is the undescribed nature of V_{Meas} as it comes directly from the measurement. This isn't to say it is impossible to calculate the partial derivatives and find their minima. However it proves easier to find them through the method of optimisation. The only downside to using NMS is that global minimum is not a guaranteed output of the function. It is in fact possible for NMS to be stuck in a local minimum. To avoid that the algorithm may initially be run multiple times with randomly distributed starting points (around the reasonably expected solution) to maximise the chance of locating the global solution. Once the solution has been found for one frequency, the next solution is of course expected to be near the previous one, hence the previous solution acts as a starting point for the next.

Simplex is a general term describing a particular shape depending on the dimensionality of the problem. For a 1D problem simplex is simply a straight line with 2 vertices; a 2D problem uses a triangle (3 vertices); 3D problem uses a tetrahedron (4 vertices) and so on. Equation A.1 is clearly a three dimensional function, hence simplex takes the form of a tetrahedron.

There are three main steps of the NMS algorithm:

1. **Vertex Scoring:** Each vertex of the simplex is evaluated. Based on the resulting values of the function, the vertices are then ordered from smallest to biggest. It seems intuitive that the solution should lie in the general direction of the smallest vertices, hence the vertex with the biggest value is disregarded.
2. **Centroid Estimation:** The coordinates of all the vertices (apart from the disregarded point) and averaged. This forms the centroid point.
3. **Simplex Transformation:** There are four main ways of transforming the original simplex. These are:
 - **Reflection:** The worst scored vertex (v_w) is reflected through the centroid. That is the new vertex (v_{ref}) is co-linear with the worst scored vertex and centroid and lies equidistant from centroid as the worst vertex. The idea is simple: move the simplex away from the location of the worst vertex. Following this transformation the value of vertex is evaluated. If the new vertex is scored such that it is not the worst and it is also not the best, the loop terminates here and new centroid is found.
 - **Expansion:** If the new vertex happens to be the best scored vertex of the simplex, the newly found vertex is shifted along the same line as before but further away from the centroid (sometimes referred to as greedy optimisation) forming a new point (v_{exp}). The better of the two points - v_{ref} , v_{exp} - becomes the new vertex.
 - **Contraction:** If point v_{ref} happens to be even worse than v_w , then the evaluation point (v_{con}) lies halfway between the centroid and v_w . That is the space beyond the centroid is not further explored on this iteration, and the new point lies inside the simplex shape. If v_{con} is better scored than v_w the loop terminates here and new centroid is estimated. If however this is not the case the last transformation is performed.
 - **Shrink Contraction:** In the case when none of the transformations resulted in a new better scored vertex, the whole simplex is contracted. All point apart from the best scored one are shifted. Usually, all points are moved closer along the original edge of the simplex in the direction of the best vertex such that their distance is halved. No evaluation is performed here and the loop terminates leading to new centroid estimation.

The whole process terminates when either the simplex reaches a predefined minimum volume - that is all the vertices are sufficiently close together, or maximum number of iterations has been

performed. The final set of vertices is averaged to give the optimal solution to the objective function.

From the process above it is clear that the algorithm can easily get stuck in a local minimum, as the simplex won't ever expand in a non-decreasing direction. Simultaneously, apart from brute force and exhaustive search algorithms it is impossible to always guarantee global solution, particularly if the argument space of the objective function is not bounded.

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Appendix B

Supplementary Theory Derivation

B.1 Resonance of Two Gyrator Circuit

The analysis used to present the results in Chapter 3 section 3.3.2 is shown here. Using simplified notation where $X|Y$ implies that component X is parallel to component Y and $X - Y$ implies series connection, circuit in Figure 3.9 has an input impedance of:

$$Z_{in} = C_1|(R_1|(L_1 - R_2 - (C_2|R_3))) \quad (B.1)$$

$$C_1 = C_{in}, \quad R_1 = R_{in}, \quad L_1 = \frac{C_g + 2C_{in}}{K_1^2}, \quad R_2 = \frac{2}{R_{in}K_1^2}, \quad C_2 = (C_l + C_{in})\frac{K_1^2}{K_2^2}, \quad R_3 = R_{in}\frac{K_2^2}{K_1^2}$$

This results in:

$$Z_{in}(s) = \frac{s^2 R_1 R_3 C_2 L_1 + s(R_1 L_1 + R_1 R_2 R_3 C_2) + R_1(R_2 + R_3)}{s^3 R_1 R_3 C_1 C_2 L_1 + s^2(R_1 C_1 L_1 + R_1 R_2 R_3 C_1 C_2 + R_3 C_2 L_1) + s(R_1(R_2 + R_3)C_1 + L_1 + R_2 R_3 C_2 + R_1 R_3 C_2) + R_1 + R_2 + R_3} \quad (B.2)$$

Which assuming that $C_g, C_l \gg C_{in}$, $K_1 = K_2$ and $R_{1,3} \gg R_2$:

$$Z_{in}(s) = \frac{s^2 R_{in} C_g C_l + s(C_g + 2C_l) + R_{in} K_1^2}{s^3 R_{in} C_{in} C_l C_g + s^2 C_g C_l + s(\frac{C_g + 2C_l}{R_{in}} + R_{in} K_1^2 C_l) + 2K_1^2} \quad (B.3)$$

Furthermore, in practical MOSFET based gyrators since $R_{in} \gg K_1^{-1}$ the following is true:

$$\frac{C_g + 2C_l}{R_{in}} \ll R_{in} K_1^2 C_l \quad (\text{B.4})$$

$$Z_{in}(s) = \frac{s^2 R_{in} C_g C_l + s(C_g + 2C_l) + R_{in} K_1^2}{s^3 R_{in} C_{in} C_l C_g + s^2 C_g C_l + s R_{in} K_1^2 C_l + 2K_1^2} \quad (\text{B.5})$$

Appendix C

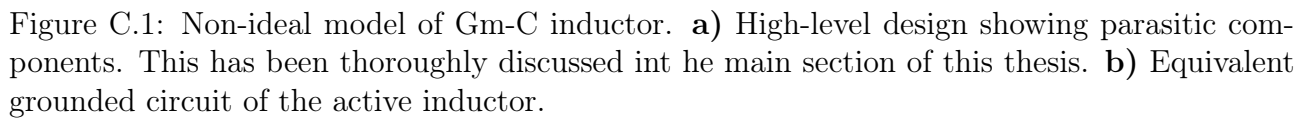
CMOS Synthetic Inductor

C.1 Introduction

the following work has been carried out by Jiawei Shen. The methodology and the results of this thesis were used to further the development of the integrated circuit realisation of active inductors. The topology presented in Chapter 3 was used by Jiawei to simulate the performance using TSMC180BCD technology and was subsequently used to layout the design in silicon. The work shown in this appendix has been presented at MEMRISYS 2019 [1] as well as at ISCAS 2020 [2].

C.2 Integrated Circuit Realisation

Reader is invited to read Jiawei Shen's original conference paper to understand the design more thoroughly. Here selected figures from his publication are shown to highlight the key design choices which lead to the performance described in the next section.



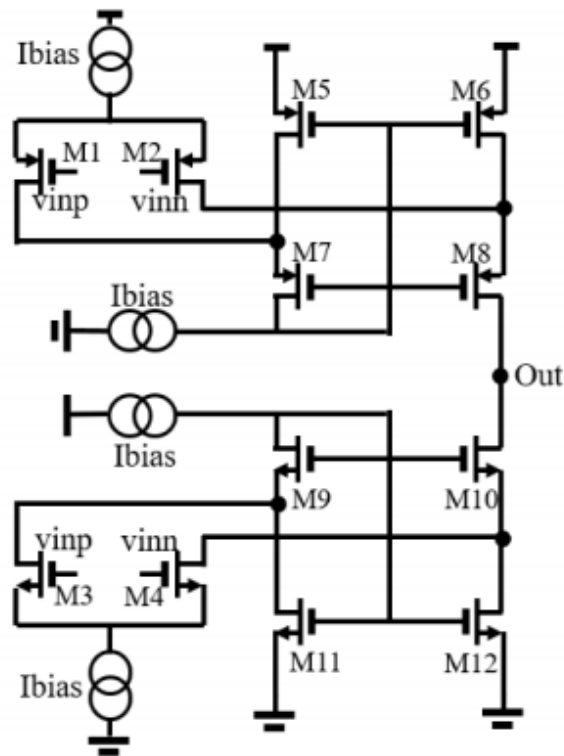


Figure C.3: Shen's proposed realisation of the operational transconductance amplifier. It features a rail-to-rail folded cascode transconductor design.

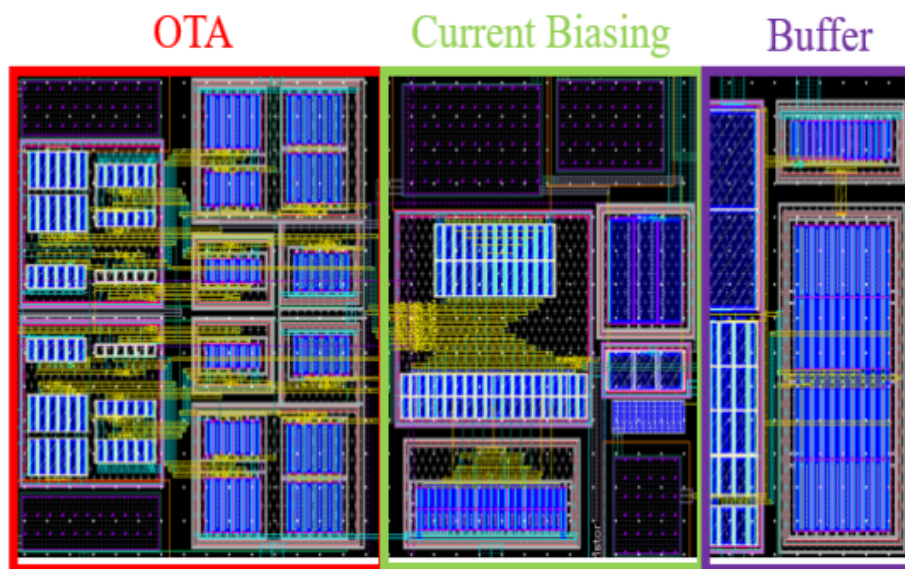


Figure C.4: Layout of the reconfigurable inductor in 0.18um TSMC CMOS. The total area used is 0.013mm².

C.3 Performance Metrics

The results are summarised in the subsequent Figure. When managed to simulate inductances as high as 10mH on an area of just 0.013mm², which is about 6 order of magnitude over what is feasibly achievable with typical spiral inductor of similar size. More importantly power consumption of an IC inductor has dropped 3 order of magnitude over the PCB realisation presented in this thesis, proving the concept is in fact feasible and can be used (in limited scope) in battery operated applications.

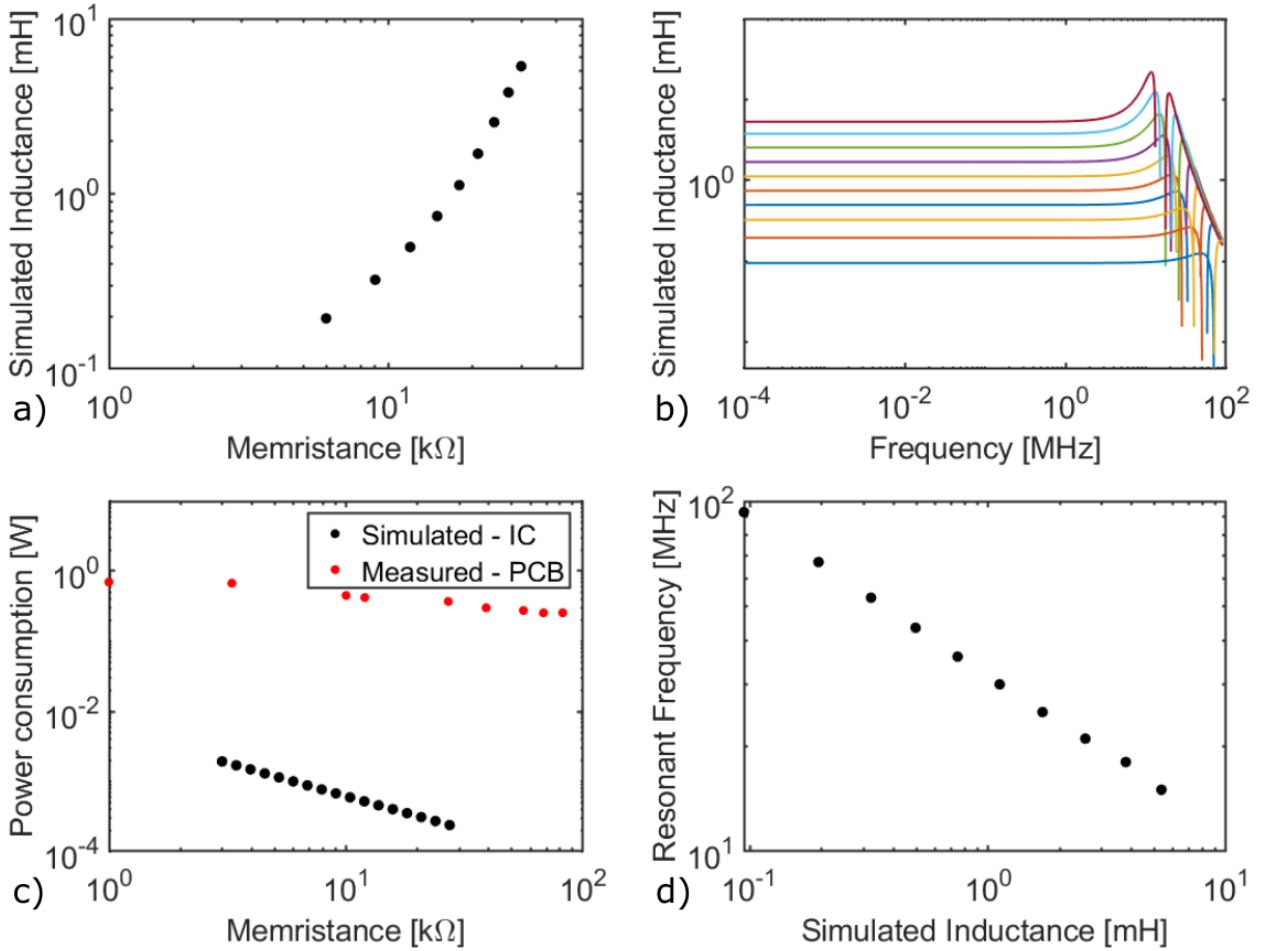


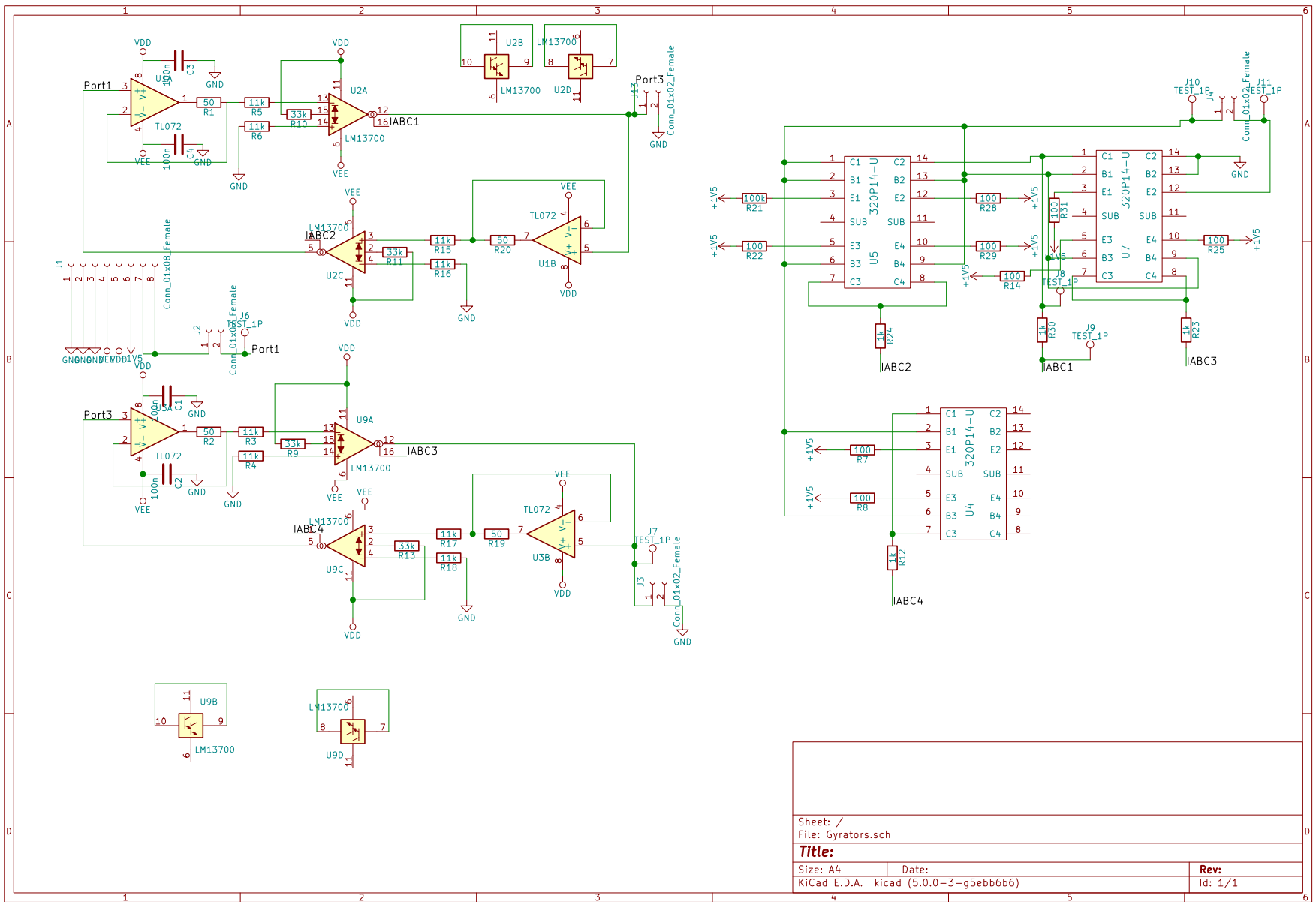
Figure C.5: Performance results of the IC inductor. **a)** Inductance as a function of memristance setting showing similar behaviour to that described in Chapter 3. **b)** Frequency response of the inductor, showing some clearly defined bandwidth limits. **c)** Power consumption of the IC version versus the PCB version. **d)** Self-resonant frequency as seen in subplot b as function of memristance setting.

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Appendix D

Schematic of General Purpose Floating Impedance Scaler



Appendix E

Model of the Memcapacitor used for Simulations

The models used for simulations of the memcapacitor behaviour were sourced from the supplementary material of [1]. The resistive switching model is based on the classic Strukov function [2] with a single state variable x , whose behaviour is described by equations E.1-E.2. Prodromakis window function [3] - $f(x)$ - is shown to represent switching most accurately.

$$\frac{dx}{dt} = ki(t)f(x) \quad (\text{E.1})$$

$$k = \frac{\mu_v R_{On}}{T^2} \quad (\text{E.2})$$

R_{Off} and R_{On} represent resistive switching limits of the device. The instantaneous value of the resistance is dictated by the state variable x , which takes any value between 0 and 1. It is defined by equation 1, where $i(t)$ is the input current over time. The proportionality constant k , defined by ion mobility μ_v , R_{On} and the insulator thickness T , represents devices responsiveness to applied stimuli.

Similarly for memcapacitors, the C_{On} capacitance is defined as minimum, while C_{Off} as maximum possible value the device can take. The definition of x remains unchanged. The value of k was estimated numerically. The same window function is used as before.

The reported resistive model parameters are: $R_{On} = 2k\Omega$, $R_{Off} = 200k\Omega$, $T = 10nm$ and $\mu_v = 10^{-14}m^2V^{-1}s^{-1}$. The value of k was calculated to be $2 \times 10^5 A^{-1}s^{-1}$. In case of the memcapacitor the parameters assume the following values: $C_{Off} = 3 \times 10^{-12}$, $C_{On} = 10^{-13}$ and $k = 10^7$.

Data shown below is directly sourced from the supplementary material of [1].

For each memory device in the equivalent circuit model in Fig. 4g, detailed state equations are given as follows:

Memristor:

$$R_{MEM} = R_{OFF} - (R_{OFF} - R_{ON})x \quad (1)$$

$$dx/dt = ki(t)f(x), k = (\mu_v R_{ON}) / D^2 \quad (2)$$

$$f(x) = \{1 - ((0.5 - x)^2 + 0.75)^{10}\} \quad (3)$$

Memcapacitor:

$$D_{MEM} = D_{ON} + (D_{OFF} - D_{ON})x, D_{MEM} = 1 / C_{MEM} \quad (4)$$

$$\frac{dx}{dt} = ki(t)f(x) \quad (5)$$

$$f(x) = \{1 - ((0.5 - x)^2 + 0.75)^{10}\} \quad (6)$$

Table S1 | Simulation Parameters utilized in equivalent circuit model

Stimulus	Magnitude: 6V, Frequency: [1,10MHz]			
	Switching range	Initial state	Ion mobility	Window Function
Memristor	$R_{OFF}=200K\Omega$ $R_{ON}=2 K\Omega$	$R_{INI}=200K\Omega$ $D=10nm$	$\mu_v=1e-14$	$f(x)=\{1-((0.5-x)^2+0.75)^{10}\}$
Memcapacitor	$C_{OFF}=3pF$ $C_{ON}=0.1pF$	$C_{INI}=3pF$	$k=1e7$	$f(x)=\{1-((0.5-x)^2+0.75)^{10}\}$
Meminductor	$L_{OFF}=7 \mu H$ $L_{ON}=0.35 \mu H$	$L_{INI}=0.35\mu H$	$k=10$	$f(x)=10*\{1-((0.5-x)^2+0.75)^{10}\}$
Nanobattery	$V_{emf}=0.04V$			

For simulations of the proposed equivalent circuit model, parameters settings are demonstrated in Table S1. Considering the pulse-induced programming resistive switching could be incomplete, parameters selected for the memcapacitor are a little larger than the measured results in Fig. 2c (0.1pF-0.3pF). However, it should be noted that in repeated simulation cycles, the initial states for three memory elements are not fixed, which is different from Biolek's models. Specifically, when biased with saturation stimulus, the internal variable cannot return exactly the same value with pristine initial state in an individual simulation cycle. Therefore, in this work, simulation will make use of the final state of internal variable in each individual cycle as the updated Initial state of next simulation cycle. By this way, the accuracy of simulation results could be improved.

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Appendix F

Publications Stemming from this Work

Szypicyn, Jakub, *et al.* "**Memristor-Based Reconfigurable Analogue Building Blocks**". In-preparation

Szypicyn, Jakub, *et al.* "**Linear-Logarithmic Nanosecond Monostable Multivibrator**". Microelectronics Journal, Under Review

Szypicyn, Jakub, *et al.* "**Towards Integrated Circuit Analogue Computing**". In IEEE International Conference on Electronics, Information and Communication 2021 (Invited Paper)

Szypicyn, Jakub, *et al.* "**Memristor-enabled reconfigurable integrated circuits**". In IEEE International Conference on Electronics, Information and Communication 2020 (Invited Paper)

Szypicyn, Jakub, *et al.* "**Variable Passives Synthesis**". Proceedings of International Conference on Memristive Materials, Devices & Systems (MEMRISYS) 2019

Szypicyn, Jakub, *et al.* "**Memristive Hybrid Linear/Logarithmic Nanosecond Pulse Generator**". Proceedings of International Conference on Memristive Materials, Devices & Systems (MEMRISYS) 2019