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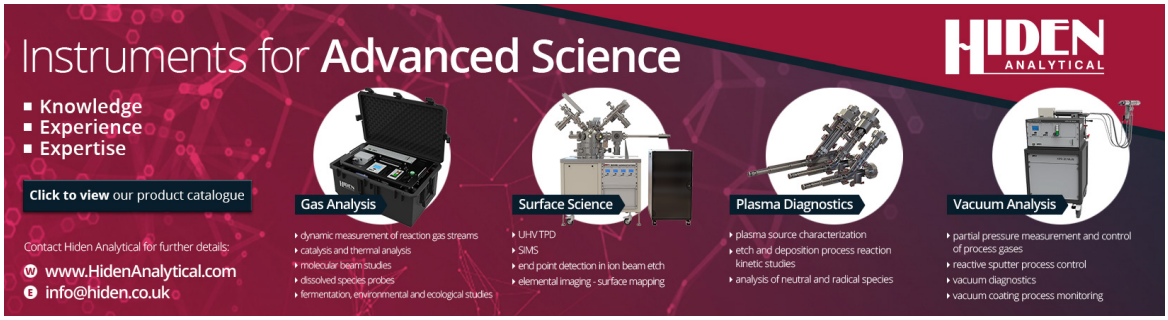
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ABSTRACT

A hybrid silicon single-electron transistor (SET)–field-effect transistor (FET), tunable by gate voltages between single-electron and classical FET operation, at room temperature (RT) is demonstrated. The device uses a side-gated, ∼6 nm wide, heavily doped n^+ silicon fin. A gate-controlled transition occurs from a depletion mode FET, including characteristic output saturation, to a quantum dot SET with "Coulomb diamond" characteristics above and near the threshold voltage, respectively. Below the threshold voltage, *p*-FET behavior implies ambipolar operation. Statistics for 180 research devices show a high yield of ∼37% for RT SET–FET operation and mean single-electron addition energy ∼0.3 eV. This yield also demonstrates the probability of single-electron effects in highly scaled doped nanoFETs and the possibility of electrically tunable, RT quantum and classical mode, nanoelectronic circuits.

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Single-electron and quantum dot (QD) devices in silicon, with precise charge control, obtained using Coulomb blockade, quantum confinement, and resonant tunneling effects provide a means to control statistical charge fluctuations in ultra-low power few-nanometer scale semiconductor devices.[1–5] Room temperature (RT) nanoelectronic operation requires QD single-electron addition energy, E_a (i.e., the amount of energy required to add/remove an electron from a QD[5]) to be greater than 0.1 eV, and much larger than the thermal energy $k_BT = 26$ meV at RT.[6–11] This typically needs the QDs to be scaled in all three dimensions, to sub-10 nm sizes.[1–3,5] In contrast, highly scaled "classical" silicon field effect transistors (FETs), such as FinFETs or gate all around (GAA) planar and nanowire channel FETs, have at least some device dimensions well above 10 nm, e.g., the channel length and height in FinFETs.[12,13] While quantum effects such as electron confinement may occur in highly scaled classical FETs, increasing the threshold gate voltage, quantum effects are not exploited explicitly to enable single-electron control and switching. Single-electron/QD devices operating at cryogenic temperatures are also of interest in Si qubit definition and sensing via spin-charge conversion.[14,15] These devices may, therefore, be regarded as bridging the gap between highly scaled Si "CMOS" and future quantum computation, logic, and memory circuits.[16] In addition, RT SETs have a significant potential in sensing applications as extremely precise charge sensors.[17]

Single-electron/QD transistors operating at RT may be defined using various QD geometries, including Si nanochannels,[18–21] nanocrystals,[22–24] and nanowires.[9,11] In contrast to a classical FET, where the influence of any quantum effects in the channel, e.g., increases in V_{th} due to quantized channel electron gas energy states, is small, electrical operation in QD SETs is controlled primarily by quantum effects. Examples include formation of "0-D" and quasi-molecular energy states, gate controlled resonant tunneling, and single-electron charging effects. Recently, we have shown RT single-electron operation in single QD and electrostatically coupled double QD transistors using QDs defined by P donor atoms in $Si/SiO_2/Si$ point contact channels, which lead to very large $E_a \sim 0.1$–0.3 eV.[6,7] Donor atom QDs have also been demonstrated in cryogenic CMOS nanoFETs,[25,26] although the shallow ∼10–50 meV depth QD potential well limits operation to these temperatures. Such devices and gate-induced QD CMOS

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FETs[16] have been used to demonstrate Si qubits, which are of great potential for scalable silicon quantum computation.[27]

In this Letter, we demonstrate a hybrid RT single-electron transistor (SET)–FET that is tunable from a classical nanoFET to a RT QD SET using the gate voltage V_{gs}. Unlike our previous work on RT QD transistors using dopant atom QDs embedded in fully oxidized Si-SiO_2-Si point-contacts,[6–8,10] a smaller than 10 nm scale silicon channel remains in the hybrid SET–FET devices. This allows gate tunable hybrid SET-FET behavior to be observed, including classical FET output characteristics with drain current (I_{ds}) saturation, which is not possible in our previous devices due to the fully oxidized point-contact. The SET–FET uses a ∼6 nm wide n^+ channel Si fin and dual side gates. QDs form within the fin, which are associated with isolated dopant atoms and Si nanocrystals. Operation as a classical FET includes previously unreported output characteristic saturation at $V_{gs} > V_{th}$; however, ambipolar p-channel FET operation behavior is seen for $V_{gs} < V_{th}$. When $V_{gs} \sim V_{th}$, this device transitions to having SET Coulomb diamond characteristics associated with the QDs. Statistics for 180 test devices show SET–FET operation with a high yield of ∼37% and a mean single-electron addition energy of ∼0.5 eV. These devices demonstrate the high likelihood of QD effects in doped nanoFETs and provide a means to define tunable hybrid SETs–ambipolar FETs for integrated classical and quantum nanoelectronic circuit application.

QD SET/FETs (Fig. 1) were fabricated in silicon-on-insulator (SOI) wafers with a heavily n-doped (P dopant, $\sim 10^{20}$ cm^{-3}) 50 nm thick top Si layer. Electron-beam lithography (EBL) in bi-layer PMMA was used to define an Al hard mask for pattern transfer into the top Si, via reactive ion etching (SF_6:O_2, 80 nm etch depth).[10] A scanning electron micrograph of the fabricated device is shown in Fig. 1(a). The device structure, before oxidation, consists of a Si point-contact channel (∼20 nm width × 20 nm length × 50 nm height) with triangular source and drain Fermi sea regions on either side. Heavy doping allows for the tips of the source, drain, and gate regions to remain highly conductive, even after oxidation. Dual, in-plane gates ∼200 nm from the channel are defined on either side. After oxidation, the Si core of the device is reduced to a fin ∼6 × 20 × 36 nm^3. Variation in channel dimensions, due to non-uniformity of oxidation, and in the associated potential barrier formed by quantum confinement across the fin can pinch off the Si channel, leading to the formation of few-nanometer scale Si nanocrystal QDs.[9,11,22] Furthermore, P dopant atoms, embedded in depleted Si regions or in the grown SiO_2 shell near the SiO_2/Si channel interface may tunnel-couple to the channel, creating dopant atom QDs.[7] Schematic diagrams of the fin-FET channel and QD array are shown in Fig. 1(b) (control gates are not shown for clarity). While a uniform dopant distribution in the device is shown for simplicity, in reality, this will be random. The device dopant density corresponds to ∼2000 dopant atoms lying within the entire point contact and ∼400 atoms in the un-oxidized Si core.

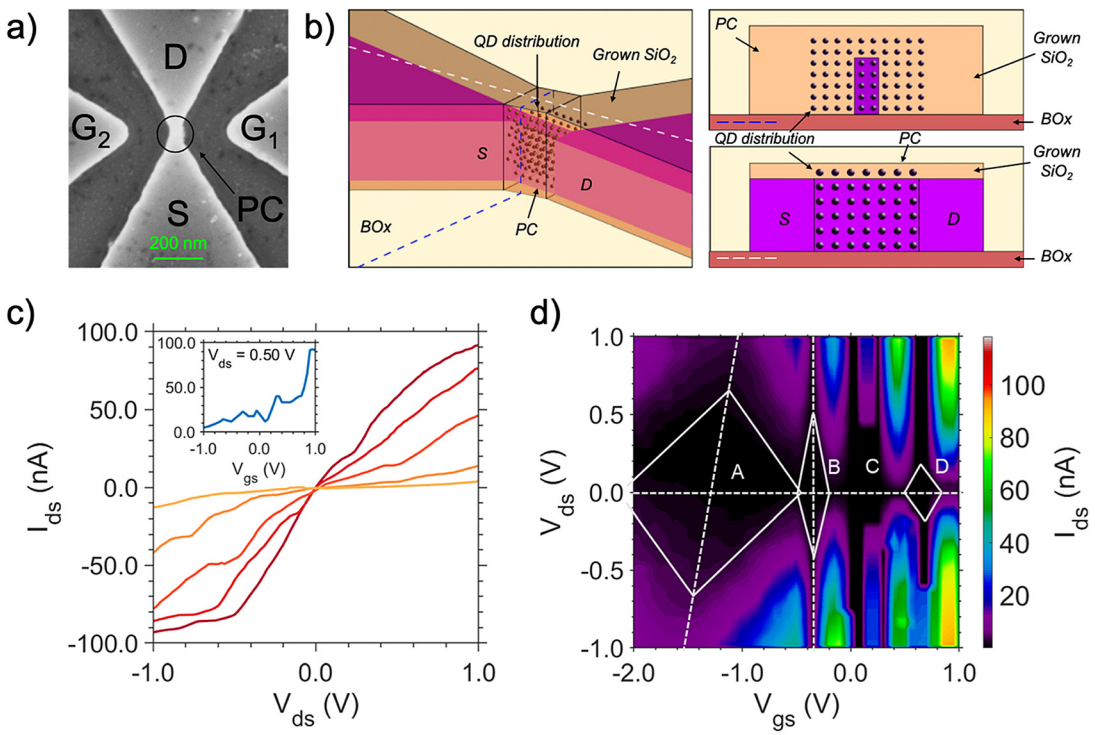


FIG. 1. (a) Scanning-electron micrograph (SEM) of a SET–FET: source (S), drain (D), point-contact (PC), and gates (G_1, G_2), labeled. (b) Schematics of the PC region. Left: Si fin channel geometry and QD array. Upper right: cross section along blue dashed line in left image. Lower right: cross section along white dashed line in left image. (c) I_{ds} vs V_{ds} FET characteristics for different V_{gs} values, 1.00 (dark red), 0.45 (dark orange), –0.10 (orange), –0.65 (light orange), and –1.20 V (yellow). Inset in (c) I_{ds} vs V_{gs} for $V_{ds} = 0.50$ V. (d) Absolute current in I_{ds} vs V_{gs} and V_{ds} of a SET–FET device.

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The source–drain current I_{ds} vs source–drain voltage V_{ds} output characteristics of a SET–FET (device 1) for V_{gs} values 1 to −1.2 V are shown in Fig. 1(c), where n-type "depletion mode" or "normally on" transistor characteristics are observed. As the device is normally on, threshold gate voltage $V_{th} < 0$ V to turn I_{ds} "off." Current saturation is clearer for larger values of V_{gs}, well above the $V_{th} \sim 0$ V. The inset to (c) shows the I_{ds} vs V_{gs} transfer characteristic, for $V_{ds} = 0.5$ V. Near V_{th}, current peaks are observed in I_{ds} vs V_{gs}, implying the presence of discrete energy states in the channel. These may be investigated in detail using QD charge stability plots.

The absolute current ($|I_{ds}|$) vs V_{gs}, V_{ds} charge stability plot for device 1 is shown in Fig. 1(d). Coulomb diamond regions A, B, and D, marked by white lines, are observed around V_{th}, indicating the presence of single-electron charging. Area C indicates another Coulomb diamond; however, current switching has obscured the diamond shape. This explains the origin of the current peaks in Fig. 1(c) inset. Device behavior at RT is qualitatively similar to donor atom QD CMOS FETs at cryogenic temperature.[21,26,28,29] Each diamond region corresponds to constant electron number on the underlying QDs. The diamond size is determined by $E_a = E_c$ (single-electron charging energy) + ΔE_k (quantum confinement energy difference). $E_c = e^2/C$, where C is the QD effective capacitance. ΔE_k is determined by both the effective size and shape of the localized potential, and the quantum energy level numbers. For an effective gate capacitance C_g, the diamond width $\Delta V_{gs} = e/C_g$. Larger diamonds possibly then correspond to smaller values of C and C_g. Diamond sizes change from A to D, indicating either multiple underlying QDs with different values of C and C_g, or a single dominant QD where C and C_g change with V_{gs}.[7]

The electrical characteristics of a second SET–FET, device 2, is shown in Fig. 2. While these characteristics are qualitatively similar to device 1, i.e., a mix of classical FET behavior and single-electron charging (Coulomb diamonds), there are changes in detail. Three Coulomb diamonds, A, B, and C, are observed in Fig. 2(a). Although these diamonds are less prominent than in device 1, this indicates either larger QDs or a hybrid behavior when SET features are observed in the FET current characteristics; hence, resulting in a smaller diamond size at larger V_{ds}. The device turns off below $V_{th} \sim 0$ V, and the diamonds are observed only above V_{th}. The diamonds are observed for $|V_{ds}| < 0.4$ V, although their effect on the channel conductance leads to current valley line features (marked by dashed vertical lines) even at higher values of V_{ds}. Furthermore, the diamonds reduce monotonically in size with V_{gs} from A to C. This possibly suggests that they are caused by a single dominant QD with increasing C and C_g values due to an increase in QD size.[6,7] Effective QD size may increase either due to widening of the corresponding potential well with increasing V_{gs}, similar to gate-induced QDs,[6] or due to the existence of an anharmonic potential well, with width increasing as electrons are added to the well.[7] Nearby QDs may also contribute to the electrical characteristics, leading to fine features [shown by white arrows in Fig. 2(a)]; however, their influence is very weak.

Figures 2(b) and 2(c) show FET output and transfer characteristics for device 2. FET behavior in device 2 is more pronounced than in device 1, with stronger current saturation in the positive V_{ds} output characteristics (b). The transfer characteristics in (c) also show ambipolar gating for larger values of V_{ds} ($V_{ds} = 2$ V), with p-FET-like characteristics for $V_{gs} < 0$ V, suggesting the presence of additional energy bandgap "tail" states or nanocrystal/grain boundary states in the ∼6 nm wide Si-fin. The transfer characteristic average current also saturates at $V_{gs} > 3$ V. Current oscillations are, however, observed in the saturated gate region, corresponding to "line" features extending from diamond regions in Fig. 2(a) (along the dashed vertical lines).

In order to determine the prevalence of hybrid SET–FET characteristics in heavily doped Si fin channels, 180 individual devices, on a 3×3 cm^2 SOI sample, were fabricated and characterized. Figure 3 shows device statistics, using a color coded sample map, and empirical cumulative distribution and histograms of V_{th} for operational devices. A hybrid SET–FET, or mainly FET with very weak SET signatures only, behavior is observed in ∼37% (67/180) of the devices [Fig. 3(a), dark blue: hybrid SET–FETs, "x" marks FET only]. Of these, 48% (32/67) are strong hybrid SET–FETs. Various shades of orange indicate faulty devices (dark: diode/fully off, medium: fabrication failure, and light: no gate effect or unstable). Device failure is attributed to effects such as non-uniform oxidation of the few nanometer scale fin width, failed hard mask liftoff, etc. A significant reason for device variability is the stochastic variations in the position, number, and size of the dopant atom or nanocrystal QDs. Further variability results from fabrication problems in fin geometry due to uncertainties in lithographic pattern transfer and oxidation in our laboratory

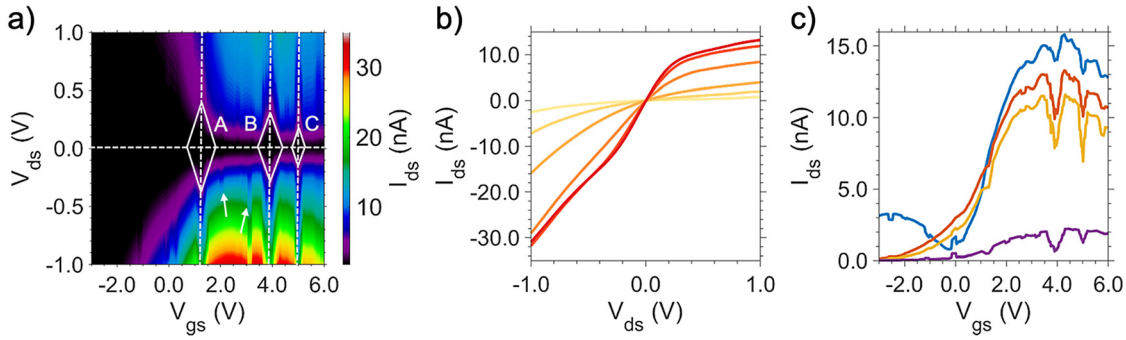


FIG. 2. (a) I_{ds} vs V_{gs}, V_{ds} for a second device with Coulomb diamonds marked by white lines and labels A, B, and C with $V_{ds} = 0$ along the dashed horizontal line. Dashed vertical lines indicate the diamond axes. (b) I_{ds} vs V_{ds} characteristics of the device in (a) at various V_{gs} values: 3.65 (red), 2.60 (dark orange), 1.55 (orange), 1.50 (light orange), –0.55 (dark yellow), and –1.60 V (yellow). (c) I_{ds} vs V_{gs} characteristics of the device in (a) at various V_{ds} values: 0.02 (purple), 0.65 (yellow), 1.00 (orange), and 2.05 V (blue). The increase at negative V_{gs} for $V_{ds} = 2.05$ V (blue curve) indicates p-FET-like ambipolar behaviors.

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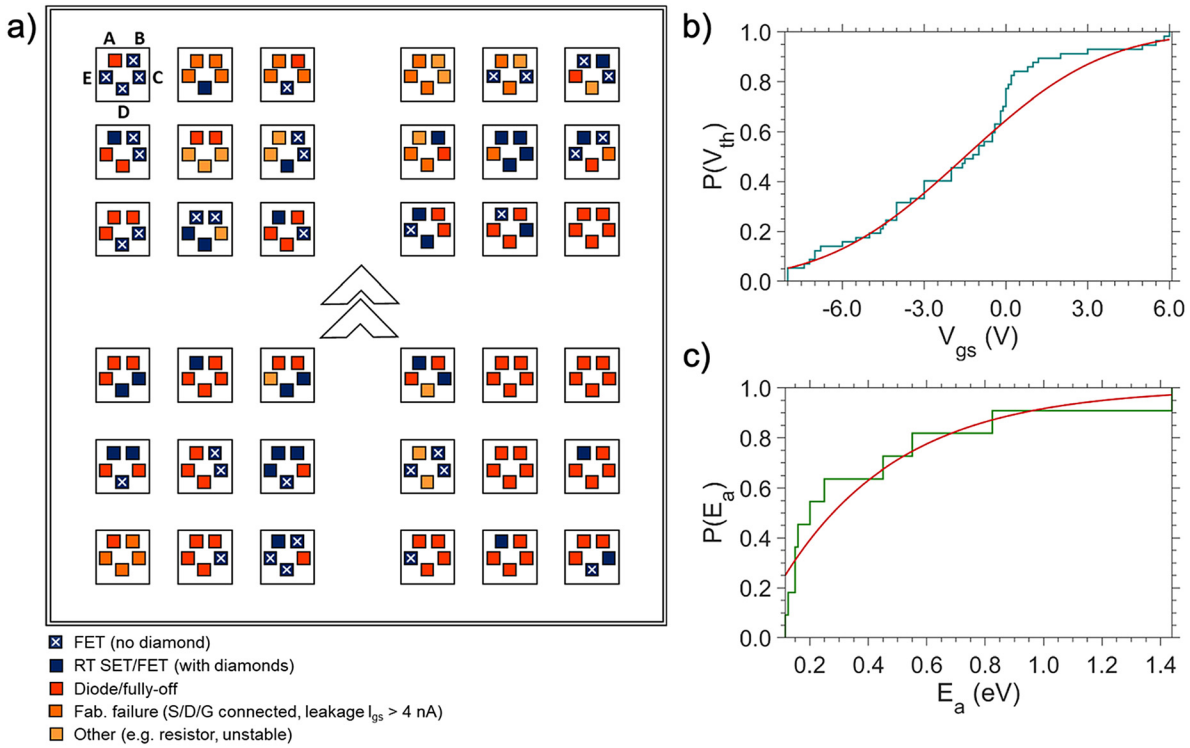


FIG. 3. (a) Color coded map of the 3 × 3 cm^2 SOI chip (180 devices). (b) Cumulative distribution of V_{th} for working SET–FET devices, mean $V_{th} \sim -1.5$ V with a normal distribution fit (red line). (c) Cumulative distribution of E_a for working SET–FET devices, mean $E_a \sim 0.28$ eV with an exponential distribution fit (red line).

environment. These problems can be mitigated in an industrial "fab" environment, where dimensional control at the ∼1 nm level is possible.[30,31]

Our device structure uses a Si fin, following high-scaled, ∼10 nm fin width classical CMOS FinFET geometry. However, unlike in classical Fin-FETs, SET–FET fin source–drain separation and height are also scaled, to ∼10–40 nm. While dual side gates are used for ease of fabrication in the laboratory, surround gate geometries as in CMOS FinFETs remain possible. Furthermore, the point-contact channel is heavily doped to enable QD formation, unlike the channel in normally off, lightly doped CMOS FinFETs. Reducing device variability would require some degree of control over QD size and position. Potential methods to achieve this include thermal annealing, controlled oxidation, and single ion implantation, e.g., Ref. 32. This may enable well controlled RT SET–FETs, switchable between classical many-electron FET ($I_{ds} \sim 100$ nA) and ultra-low power single-electron QD transistor (∼1 nA or less) modes. Furthermore, we note that our devices are fabricated in the laboratory and not in a commercial semiconductor fab. However, the 37% operational device yield is higher than previously reported.[8] For the hybrid SET–FETs, V_{th} values are presented as a cumulative distribution plot [Fig. 3(b)], where the probability that V_{th} of the measured devices $P(V_{th})$ is less than or equal to a particular value of V_{gs}. The cumulative distribution may be fitted by a normal distribution with mean $V_{th} = -1.5$ V. However, the standard deviation is rather large, ∼4 V, a consequence of nanofabrication variability in a laboratory environment. Furthermore, a strong rise in the distribution occurs at 0 V, where 80% of the n-type depletion mode FET devices has a threshold voltage ≤0 V. Threshold values >0 V are associated with the standard n-type enhancement mode FET behavior.

As Coulomb diamonds of various sizes are observed, the diamond widths (ΔV_{gs}) and heights (ΔV_{ds}) may be used to estimate the average values of the QD E_a and radii (r). The addition energy is given by $E_a = \Delta E_k + E_c$. Between the ground and first excited state, $\Delta E_k = \pi^2\hbar^2/2mr^2$ by assuming an infinite square potential, and $E_c = e^2/C = e^2/(4\pi\varepsilon\varepsilon_0 r)$, where C for an assumed spherical QD is given by $4\pi\varepsilon\varepsilon_0 r$. E_a is often calculated from ΔV_{ds} using $\Delta V_{ds} = 2e/C = 2E_a/e$, with equal voltage drops across similar capacitive source/drain tunnel barriers, C_b. However, in our devices, a significant percentage of V_{ds} can drop external to the QD, e.g., in the tips of the triangular source/drain regions, leading to $\Delta V_{ds} > \Delta V_{gs}$. Hence, it is not possible to extract E_a directly from ΔV_{ds}. Instead, by using the diamond width, $\Delta V_{gs} = [(2C_b + C_g)/C_g]\ (2E_a/e)$, it is possible to extract E_a.[7,8] Weak tunnel coupling of the QDs, where $2\,C_b < C_g$ implies that $\Delta V_{gs} \sim 2E_a/e$; hence, an estimate of E_a may be extracted. The cumulative distribution for the extracted E_a values, where the probability that E_a of the measured devices $P(E_a)$ is less than or equal to a particular value of E_a, is shown in Fig. 3(c). Most (∼80%) devices have $E_a \sim 0.1$–0.6 eV, with an average value $E_a \sim 0.28$ eV for all devices, much larger than the RT thermal energy $k_BT = 0.026$ eV. An average QD radius may be extracted by solving for r in the equation $E_a = \Delta E_k + E_c = \pi^2\hbar^2/2mr^2 + e^2/(4\pi\varepsilon\varepsilon_0 r)$ for $E_a = 0.28$ eV. It is found that the average QD radius is ∼2.05 nm. This size lies within a range that is

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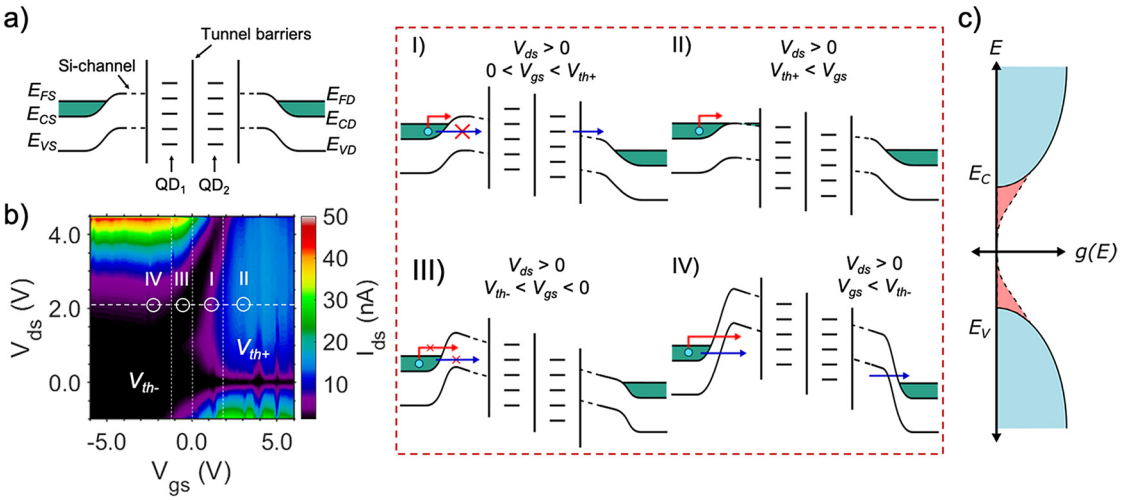


FIG. 4. Energy band diagram for SET–FET devices. (a) Band diagrams for SET–FET without any bias. $E_{FS(D)}$, $E_{CS(D)}$, and $E_{VS(D)}$ are fermi (F), conduction (C), and valence (V) energy levels for source (S) and drain (D), respectively. Filled states are shown in teal. Non-uniformity or disorder along the Si channel leads to tunnel barriers (vertical solid lines) confining QDs. Multiple QDs (energy states indicated) can exist along the channel (two QDs are shown, for simplicity). (I–IV) SET–FET band diagrams with (I) $0 < V_{gs} < V_{th+}$, (II) $V_{th+} < V_{gs}$, (III) $V_{th-} < V_{gs} < 0$, and (IV) $V_{gs} < V_{th-}$ with $V_{ds} > 0$ in all cases. Red arrows are thermally activated tunnel currents, and blue arrows are bias-induced tunnel currents. (b) Experimental charge stability diagram from Fig. 2(a) over a larger voltage range with all four cases marked. Vth+ and Vth– are the threshold voltages for *n*- and *p*-type behaviors. (c) Density of states for SET–FETs where tailed states, belonging to QDs, sit in between E_C and E_V in the energy gap (red).

similar to dopant atom QDs ($r \sim 2$ nm) and Si nanocrystals ($r \sim 3$–9 nm). Higher values of E_a may result from multiple, series QDs along the current path.[4,6] These may be formed by defect (band tail) or dopant states, gate-induced QDs, or non-uniformity in the Si fin.[33]

The band diagram for SET–FET devices is proposed in Fig. 4. The equilibrium condition is shown in Fig. 4(a), and four further cases are presented: (I) $0 < V_{gs} < V_{th+}$, (II) $V_{th+} < V_{gs}$, (III) $V_{th-} < V_{gs} < 0$, and (IV) $V_{gs} < V_{th}$, with $V_{ds} > 0$ in all cases. The locations of these cases, with respect to the charge stability diagram of device 2 (measured over a wider voltage range), is shown in Fig. 4(b). Greater electron depletion is shown in the narrow Si fin compared to the wider source/drain regions. Both Si channel and potential barrier/QD regions (vertical solid lines with intermediate, confined energy states) are possible along the fin and are shown schematically in (a). Arrows indicate tunnel (blue) or thermally activated (red) current. The potential barrier height must be much larger than $k_BT = 26$ meV at RT to allow RT single-electron charging to occur. Multiple QDs can exist in the channel [two QDs are shown for simplicity in (a)]. In the case of a dopant atom origin for the QDs, as many dopants exist in the channel and well-defined Coulomb diamonds are observed, single or a few dominant QDs are addressed near V_{th+}, where an FET channel is only weakly formed. For $V_{gs} \gg V_{th+}$ or for large V_{ds}, tunnel barriers are overcome by the bias and mainly classical FET operation occurs. At moderate V_{ds} and small $V_{gs} < V_{th+}$, only thermally activated current can flow (I). Larger gate bias ($V_{gs} > V_{th+}$) will pull the channel and QD states down, increasing current (II). Negative gate bias usually turns current off due to a higher fin potential barrier (III). However, at large V_{ds} [>2 V in Fig. 4(b)] and $V_{gs} < V_{th}$, band–band tunnel current may flow (IV), leading to ambipolar FET behavior. Finally, a generalized band density-of-states is shown schematically in Fig. 4(c). This includes conduction and valence bands (blue), and bandgap tail states as amorphous or nanocrystalline regions, or deep-level traps, may exist in the fin (red). Given sparsely distributed tail states, these can also form QD-like sites for single-electron charging.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Faris Yasser Abualnaja: Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Writing – original draft (equal); Writing – review & editing (equal). **Wenkun He:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Writing – original draft (equal); Writing – review & editing (equal). **Kai-Lin Chu:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Supervision (equal); Writing – original draft (equal); Writing – review & editing (equal). **Aleksey Andreev:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Writing – original draft (equal); Writing – review & editing (equal). **Mervyn Jones:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Supervision (equal); Writing – original draft (equal); Writing – review & editing (equal). **Zahid A. K. Durrani:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Funding acquisition (equal); Investigation (equal); Methodology (equal); Supervision (equal); Writing – original draft (equal); Writing – review & editing (equal).

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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