

Imperial College London
Department of Electrical and Electronic Engineering

Electrode Impedance Characterisation for Implantable Neural Interfaces

Vichaya Manatchinapisit

A Thesis submitted in fulfilment of requirements for the degree of Doctor of Philosophy
(PhD) and the Diploma of Imperial College London (DIC)

October 2025

Declaration of Originality

I hereby declare that this thesis is my own original work. Any material that is not my own has been properly cited and acknowledged. Any contribution made to the research by others, including colleagues within my research group and department, has been explicitly acknowledged in the thesis.

Vichaya Manatchinapisit

Copyright

The copyright of this thesis rests with the author. Unless otherwise indicated, its contents are licensed under a Creative Commons Attribution-NonCommercial 4.0 International Licence (CC BY-NC).

Under this licence, you may copy and redistribute the material in any medium or format. You may also create and distribute modified versions of the work. This is on the condition that: you credit the author and do not use it, or any derivative works, for a commercial purpose.

When reusing or sharing this work, ensure you make the licence terms clear to others by naming the licence and linking to the licence text. Where a work has been adapted, you should indicate that the work has been changed and describe those changes.

Please seek permission from the copyright holder for uses of this work that are not included in this licence or permitted under UK Copyright Law.

Vichaya Manatchinapisit

Abstract

Neurological disorders such as Parkinson’s disease and epilepsy affect millions in the UK. In drug-resistant cases, deep brain stimulation (DBS) is often required; however, traditional DBS delivers continuous stimulation, which may lead to adverse effects. Closed-loop DBS, which adapts stimulation based on real-time biosignals, improves efficacy and reduces side effects. Maintaining long-term effectiveness requires stable implanted electrodes, which can degrade over time due to tissue encapsulation, inflammation, and stimulation-induced changes. Monitoring electrode impedance is therefore essential for assessing performance, ensuring device reliability, and maintaining patient safety.

This thesis presents a system for characterising electrode impedance in implantable neural interfaces. The project was conducted in three phases: (1) establishing an accelerated degradation testing protocol; (2) developing a benchtop impedance measurement platform; and (3) designing an integrated circuit (IC)-based impedance measurement system. The accelerated testing protocol, incorporating continuous impedance monitoring, was validated using electrochemical impedance spectroscopy (EIS) under simulated degradation induced by thermal and electrical stimulation. A custom PCB platform was designed to perform EIS from 48 Hz to 100 kHz, demonstrating impedance measurements of DBS electrodes in phosphate-buffered saline (PBS) and tungsten wire under accelerated degradation.

Furthermore, a NeuroZ chip, fabricated in 180 nm CMOS technology, enabled EIS from 1 Hz to 100 kHz and resistance values between $100\ \Omega$ and $1\ \text{M}\Omega$. The chip was validated with DBS, stereoelectroencephalography (SEEG), electrocorticography (ECoG), and cuff electrodes. A multi-sine impedance measurement approach was also explored to reduce measurement time and minimise interference with neuromodulation treatments.

Overall, this work presents the development of an integrated circuit capable of performing impedance characterisation. Accelerated testing, benchtop validation, and IC-based measurements were conducted, providing a systematic framework to evaluate electrode performance. The outcomes of this research support the future design of more reliable and efficient neural interface technologies.

Acknowledgements

First and foremost, I would like to express my heartfelt gratitude to my family for their unwavering support, encouragement, and belief in me throughout this journey. Their love and support have been the foundation of my strength.

I extend my deepest thanks to my supervisor, Professor Timothy Constandinou, for his invaluable guidance, support, and mentorship throughout my research. His insights and encouragement have been instrumental in shaping this work and bringing it to completion.

I am especially grateful to Dr. Adrien Rapeaux and Dr. Ian Williams for their valuable suggestions and constructive feedback on experimental and circuit design. Their input significantly enhanced the quality and precision of my work. My sincere appreciation also goes to Dr. Feng Peilong and Mr. Andrea Mifsud for their expert guidance, advice on integrated circuit (IC) design, and support with design tools and resources. Additionally, I would like to thank Mr. Steven Wong for his insightful feedback and suggestions regarding PCB design, which played a critical role in the development of my research prototypes.

Finally, I am deeply appreciative of all the members of the NGNI Lab for their collaboration, support, and encouragement. The collegial atmosphere and shared knowledge within the lab have been a constant source of inspiration and have greatly contributed to the success of this project.

Contents

Abstract	ii
Acknowledgements	ii
1 Introduction	1
1.1 Motivation	1
1.2 Research Objectives	3
2 Background and State-of-the-Art	6
2.1 Bidirectional Neural Interfaces and Close-Loop Neuromodulators	6
2.1.1 Available commercial closed-loop neural interface/ research platform . . .	6
2.1.2 Academic Research on Neuromodulation ASICs	8
2.2 Neural interface electrodes	10
2.2.1 Electrochemical mechanism in the electrode-electrolyte interface	13
2.2.2 Recording electrodes	14
2.2.3 Stimulation Electrodes	15
2.3 Electrochemical measurements	16

2.4	Electrochemical Impedance measurement technique	19
2.5	Electrode Impedance Measurement on IC Chips	21
2.6	Accelerated lifetime testing for neural interface electrode	26
3	Design of Accelerated lifetime testing validation	27
3.1	Design of Accelerated electrode degradation system	27
3.1.1	Methodology	27
3.1.2	Results	32
3.1.3	Electrochemical Impedance Spectroscopy	35
3.1.4	Discussion	35
3.2	Automated platform for bench-top and developmental impedance measurements	39
3.2.1	Overall system diagram	39
3.2.2	Results	41
3.3	Conclusion	41
4	Custom bench-top platform for electrode impedance characterisation	44
4.1	The PCB design for the custom bench-top platform	45
4.1.1	Microcontroller (MCU)	46
4.1.2	Signal generation or DAC	47
4.1.3	Voltage-Controlled Current Source	49
4.1.4	Instrumentation Amplifier and Programmable Gain Stage	52
4.1.5	ADC	53

4.1.6	Power Supply	53
4.1.7	Software	54
4.2	Validation with implantable neural electrodes	56
4.3	Validation with Automated System for Operating the Bench-top	60
4.4	Conclusion	62
5	An integrated circuit-based EIS Platform	64
5.1	Design and Implementation	64
5.2	Top-Level Circuits	65
5.2.1	Operational Amplifier	67
5.2.2	Bias-Level Considerations	68
5.2.3	Digital-to-Analogue Converter (DAC)	69
5.2.4	Voltage-Controlled Current Source (VCCS)	69
5.2.5	H-Bridge	71
5.2.6	Differential Amplifiers	72
5.2.7	Serial to Parallel for programmable gain control	72
5.2.8	Analogue-to-Digital Converter (ADC)	74
5.3	Operation and Functional Overview of the NeuroZ Chip	76
5.3.1	Analogue and Digital Input/Output Management	76
5.3.2	Initialisation and Configuration	79
5.4	Data Flow and Signal Control	80
5.5	Layout	82

5.6	Power Measurement	82
5.7	Simulation	83
5.7.1	Current injection and measured voltage responses	84
5.7.2	Simulation EIS results	85
5.8	Measurement and Testing system	85
5.8.1	Testing board	85
5.8.2	Experimental and Impedance Measurement Validation	87
5.8.3	Single-Sine Impedance Measurement Results	91
5.9	Multi-Sine Impedance Measurement	103
5.9.1	Waveform Design and Selection	104
5.9.2	RC Component Testing	105
5.9.3	Experimental Setup	106
5.9.4	Multi-Sine Impedance Measurement Results	106
5.9.5	Expanded Multi-Sine Frequency Waveform Design	108
5.9.6	Two-Decade Multi-Sine Impedance Measurement results	118
5.10	Discussion	120
5.11	Conclusion	122
6	Conclusion	123
6.1	Future Works	125
6.2	Lessons Learned from This Research	126

A Appendix **128**

A.1 List of publications 128

A.2 EIS Results for Single-sine Waveform 129

A.3 EIS Results of Multi-Sine waveform 135

A.4 EIS Results of Two-Decade Multi-Sine Waveform 141

References **142**

List of Tables

2.1	Comparison ASIC for EIS measurement for implantable neural interface	22
2.1	(continued) Comparison ASIC for EIS measurement for implantable neural interface	23
4.1	Design requirements and specifications of the custom bench-top impedance measurement platform.	45
4.2	The component values for the impedance measurement board.	47
4.3	Candidate operational amplifiers evaluated for the ± 5 V VCCS implementation.	51
5.1	Impedance measurement IC expected specification	65
5.2	Rail-to-rail operational amplifier specification	68
5.3	Gain Configuration Table for Impedance Measurement System. The table shows all 16 possible configurations for the 8-bit binary input ('0bxxxxyyyy'), with corresponding gain values for the differential amplifier across the device under test ($Gain_{electrode}$) and the reference resistor ($Gain_R$).	74
5.4	Analogue input pin	76
5.5	Digital pin	77
5.6	Power pin	77

5.7	Neural electrode used in the experimental measurement and geometric surface area (GSA)	91
5.8	Summary of the results for the DBS-RC electrode across single frequency, multifrequency, and expanded multifrequency methods. Errors and RMS values are shown for different frequency ranges, compared with EIS measured by CHI760E in potentiostatic mode.	119
5.9	Summary of the results for the DBS-RC electrode across single frequency, multifrequency, and expanded multifrequency methods. Errors and RMS values are shown for different frequency ranges, compared with EIS measured by CHI760E in galvanostatic mode.	119
5.10	Summarised errors of NeuroZ impedance measurement across DBS, SEEG, ECoG, and cuff electrodes using single-sine, multi-sine, and two-decade multi-sine methods. The table highlights the averaged per cent errors and RMS values for low, middle, and high-frequency ranges	120

List of Abbreviations

AC Alternating Current

ACS American Chemical Society

ADC Analog-to-Digital Converter

ADs Antiepileptic Drugs

ASA Acrylonitrile Styrene Acrylate

ASAR Adaptive Stimulation Artifact Rejection

ASIC Application-Specific Integrated Circuit

BCI Brain-Computer Interface

BMI Brain-Machine Interface

CHI760E Electrochemical Workstation Model

CIC Charge Injection Capacity

CNS Central Nervous System

CV Cyclic Voltammetry

DAC Digital-to-Analog Converter

DBS Deep Brain Stimulation

DC Direct Current

DMA Direct Memory Access

DUT Device Under Test

ECoG Electrocorticography

EEG Electroencephalography

EIS Electrochemical Impedance Spectroscopy

FDA Food and Drug Administration

FFT Fast Fourier Transform

GPIB General Purpose Interface Bus

GSA Geometric Surface Area

HB H-Bridge

IC Integrated Circuit

INA Instrumentation Amplifier

LCR LCR Meter (Inductance, Capacitance, Resistance Meter)

LDO Low-Dropout Regulator

LFP Local Field Potential

LPF Low-Pass Filter

LUT Look-Up Table

MCU Microcontroller Unit

MEMS Micro-Electro-Mechanical Systems

MCO Microcontroller Clock Output

NXP Semiconductor Manufacturer

OCD Obsessive-Compulsive Disorder

OCP Open Circuit Potential

PBS Phosphate Buffered Saline

PCB Printed Circuit Board

PGA Programmable Gain Amplifier

PLL Phase-Locked Loop

RMS Root Mean Square

RNS Responsive Neurostimulation System

ROS Reactive Oxygen Species

SD Standard Deviation

SEEG Stereoelectroencephalography

SHE Standard Hydrogen Electrode

SMU Source Meter Unit

SNR Signal-to-Noise Ratio

UART Universal Asynchronous Receiver-Transmitter

VCCS Voltage-Controlled Current Source

VT Voltage Transient

List of Figures

1.1	Picostim by Amber Therapeutics[21]	2
1.2	Block diagram of DBS system	4
2.1	RNS (Responsive cortical Neurostimulation System) by Neuropace[25]	7
2.2	Percept PC Neurostimulator by Medtronic[32][34]	8
2.3	Brain Interchange System by CorTec [35]	9
2.4	Equivalent circuit of electrode/electrolyte interface	14
2.5	The measured voltage waveform between two electrodes during the stimulation pulse. The diagram is adapted from [88]	21
3.1	Overall experiment system including EIS measurement, current pulse simulation, and 3-electrode electrochemical cell from [101]	28
3.2	Electrochemical workstation and 3-electrode configuration electrochemical cell. .	29
3.3	Pourbaix or potential- pH equilibrium diagram of tungsten in PBS after 15 days. The demonstrates three regions, including corrosion (WO_4^{2-}), immunity(W), and passivation (WO_3). The diagram is adapted from [98]	30
3.4	The electrode potential across the tungsten wire and Ag/AgCl reference electrode during electrical pulse stimulation, measured by an oscilloscope.	32

3.5	Microphotograph of a new tungsten wire electrode showing its morphology before immersion into PBS solution. The diameter of the tungsten wire is 50 μm	34
3.6	Microphotograph of the tungsten wire after six hours of electrical stimulation. The wire fractured near the middle section, where the diameter was reduced to around 8.78 μm	34
3.7	Microscopic image of the tungsten wire surface after stimulation showing flaking and delamination along the wire axis. The surface morphology indicates mechanical degradation consistent with hydrogen-induced embrittlement. . . .	34
3.8	The averaged EIS across trials of the tungsten wire.	36
3.9	The normalised impedance as a function of stimulation time of three trials plotted with standard deviations	37
3.10	Block diagram of the automated platform integrating the electrochemical workstation with the developmental impedance measurement device.	39
3.11	Experimental setup of the automated platform combining the electrochemical workstation and impedance measurement device.	40
3.12	EIS data of electrode in the automatic platform over time	41
3.13	Microphotograph of electrode breakdown with the automatic platform. The electrode diameter close to the cutting point is around 13.82 μm	42
3.14	Flowchart for the operation of the automated platform.	43
4.1	The PCB-based Impedance measurement board consists of a high-pass filter, Voltage-controlled current source (VCCS), Instrumentation amplifiers (IA), low-pass filter(LPF), programmable gain amplifiers(PGA), and voltage buffer. The values of each component are shown in Table 4.2	47
4.2	System diagram of the custom impedance measurement platform integrating the microcontroller, signal-conditioning circuits, and electrode–electrolyte interface. .	48

4.3	Assembled PCB inside the 3D-printed case	48
4.4	Flowchart for the operation of custom PCB impedance measurement.	55
4.5	DBS electrode and Pt sheet in PBS solution connected to electrochemical workstation	56
4.6	Comparison graph between EIS measuring by CHI760E and Impedance measurement PCB	57
4.7	Percentage error of custom PCB impedance measurement board	58
4.8	Comparison graph between EIS measuring by CHI760E and Impedance measurement PCB	60
4.9	Average magnitude and phase errors between the PCB-based impedance measurement system and the bench-top electrochemical workstation during the accelerated degradation test	61
5.1	Top-level block diagram	66
5.2	Voltage controlled current source	70
5.3	H-Bridge control time diagram	71
5.4	H-Bridge stage	71
5.5	Example gain control serial input and latch time diagram	73
5.6	serial to parallel circuit including D flip-flop and active low latch	73

5.7	The testing board integrates the packaged NeuroZ chip and MCU via board-to-board pin connectors for impedance measurement. The MCU generates logic controls and receives the waveform output from the on-chip ADC. The received waveform data is then packaged and sent to a computer for impedance analysis. A level shifter converts 3.3 V to 5 V and vice versa for data transmission. A 5 V power supply, regulated by an LDO, provides 3.3 V for the level shifter and an external DAC, which supplies voltage references to the chip, as well as 1.8 V and 5 V to power the NeuroZ chip. The current bias (50 μ A and 1.6 mA) is sourced from the SMU. The system operates with digital control, signal processing, and power regulation for impedance characterisation.	75
5.8	NeuroZ chip in cadence	81
5.9	NeuroZ chip under microscope	82
5.10	Electrode-electrolyte interface equivalent circuit model (C_{dl} =double-layer capacitance, R_{ct} =charge transfer resistance, R_s =Electrolyte or solution resistance). . .	83
5.11	Simulated voltage and current waveforms across the DBS electrode model obtained in Cadence	84
5.12	EIS result for equivalent circuit model of DBS electrode	85
5.13	PCB testing board for impedance measurement, featuring an STM32 Nucleo H723ZG microcontroller (left), level shifters, and a socket for the packaged NeuroZ chip (centre). The board also includes LDOs, DACs for voltage references, and additional external components that will be able to replace the internal blocks of the NeuroZ chip, if needed.	86
5.14	Example time-domain responses obtained from the RC-equivalent circuit model of the DBS electrode across frequencies between 1 Hz and 100 kHz. The left column shows the measured voltage waveforms, and the right column shows the corresponding current responses recorded by the impedance measurement circuit.	90

5.15	Electrode Impedance Spectroscopy (EIS) comparison and interpolation results for DBS equivalent circuit model. Subfigures illustrate the original measured data and interpolated data for consistent frequency spacing.	93
5.16	Error analysis of measured EIS data for DBS equivalent circuit model. Subfigures show the error in absolute ohms and the percentage error between NeuroZ and CHI760E measurements.	94
5.17	Electrode Impedance Spectroscopy (EIS) comparison and interpolation results for 100 Ω . Subfigures illustrate the original measured data and interpolated data for consistent frequency spacing.	95
5.18	Error analysis of measured EIS data for 100 Ω resistor. Subfigures show the error in absolute ohms and the percentage error between NeuroZ and LCR meter measurements.	96
5.19	Electrode Impedance Spectroscopy (EIS) comparison and interpolation results for 10k Ω . Subfigures illustrate the original measured data and interpolated data for consistent frequency spacing.	97
5.20	Error analysis of measured EIS data for 10k Ω resistor. Subfigures show the error in absolute ohms and the percentage error between NeuroZ and LCR meter measurements.	98
5.21	Standard deviation (SD) of impedance measurements across the frequency spectrum (1 Hz to 100 kHz) obtained using the CHI760E system. (a) Potentiostatic mode: The SD is higher at low frequencies (1–10 Hz) for all electrode types, reflecting increased variability in this range. (b) Galvanostatic mode: Similar trends are observed, with the cuff electrode exhibiting the highest SD across the frequency spectrum in both modes.	100
5.22	Electrode Impedance Spectroscopy (EIS) comparison and interpolation results for DBS electrodes. Subfigures illustrate the original measured data and interpolated data for consistent frequency spacing.	101

5.23	Error analysis of measured EIS data for DBS electrodes. Subfigures show the error in absolute ohms and the percentage error between NeuroZ and CHI760E measurements.	102
5.24	Example integrated multi-sine excitation waveform showing the combined signal, its absolute amplitude, and the frequency spectrum (FFT) used for impedance characterisation.	104
5.25	Example time-domain responses obtained from the RC-equivalent circuit model of the DBS electrode using a multi-sine excitation waveform. The left column shows the measured voltage signals, and the right column shows the corresponding current responses sensed by the internal reference resistor	105
5.26	Electrode Impedance Spectroscopy (EIS) comparison and interpolation results for DBS equivalent circuit model. Subfigures illustrate the original measured data and interpolated data for consistent frequency spacing.	109
5.27	Error analysis of measured EIS data for DBS equivalent circuit model. Subfigures show the error in absolute ohms and the percentage error between NeuroZ with multi-sine waveform and CHI760E measurements.	110
5.28	Electrode Impedance Spectroscopy (EIS) comparison and interpolation results for DBS electrodes. Subfigures illustrate the original measured data and interpolated data for consistent frequency spacing.	111
5.29	Error analysis of measured EIS data for DBS electrodes. Subfigures show the error in absolute ohms and the percentage error between NeuroZ with multi-sine waveform and CHI760E measurements.	112
5.30	Two-decade multi-sine excitation waveform showing the combined signal, its absolute amplitude, and the frequency spectrum (FFT) used for impedance characterisation.	113

5.31	Example time-domain responses obtained from the RC-equivalent circuit model of DBS electrode using two-decade multi-sine excitation waveform. The left column shows the measured voltage signals, and the right column shows the corresponding current responses recorded by the impedance measurement circuit	113
5.32	Electrode Impedance Spectroscopy (EIS) comparison and interpolation results for DBS equivalent circuit model. Subfigures illustrate the original measured data and interpolated data for consistent frequency spacing.	114
5.33	Error analysis of measured EIS data for DBS equivalent circuit model. Subfigures show the error in absolute ohms and the percentage error between NeuroZ with multi-sine waveform and CHI760E measurements.	115
5.34	Electrode Impedance Spectroscopy (EIS) comparison and interpolation results for DBS electrodes. Subfigures illustrate the original measured data and interpolated data for consistent frequency spacing.	116
5.35	Error analysis of measured EIS data for DBS electrodes. Subfigures show the error in absolute ohms and the percentage error between NeuroZ with multi-sine waveform and CHI760E measurements.	117
A.1	Electrode Impedance Spectroscopy (EIS) comparison and interpolation results for SEEG electrodes. Subfigures illustrate the original measured data and interpolated data for consistent frequency spacing.	129
A.2	Error analysis of measured EIS data for SEEG electrodes. Subfigures show the error in absolute ohms and the percentage error between NeuroZ and CHI760E measurements.	130
A.3	Electrode Impedance Spectroscopy (EIS) comparison and interpolation results for ECoG electrodes. Subfigures illustrate the original measured data and interpolated data for consistent frequency spacing.	131

A.4	Error analysis of measured EIS data for ECoG electrodes. Subfigures show the error in absolute ohms and the percentage error between NeuroZ and CHI760E measurements.	132
A.5	Electrode Impedance Spectroscopy (EIS) comparison and interpolation results for Cuff electrodes. Subfigures illustrate the original measured data and interpolated data for consistent frequency spacing.	133
A.6	Error analysis of measured EIS data for cuff electrodes. Subfigures show the error in absolute ohms and the percentage error between NeuroZ and CHI760E measurements.	134
A.7	Electrode Impedance Spectroscopy (EIS) comparison and interpolation results for SEEG electrodes. Subfigures illustrate the original measured data and interpolated data for consistent frequency spacing.	135
A.8	Error analysis of measured EIS data for SEEG electrodes. Subfigures show the error in absolute ohms and the percentage error between NeuroZ with multi-sine waveform and CHI760E measurements.	136
A.9	Electrode Impedance Spectroscopy (EIS) comparison and interpolation results for ECoG electrodes. Subfigures illustrate the original measured data and interpolated data for consistent frequency spacing.	137
A.10	Error analysis of measured EIS data for ECoG electrodes. Subfigures show the error in absolute ohms and the percentage error between NeuroZ with multi-sine waveform and CHI760E measurements.	138
A.11	Electrode Impedance Spectroscopy (EIS) comparison and interpolation results for Cuff electrodes. Subfigures illustrate the original measured data and interpolated data for consistent frequency spacing.	139

A.12 Error analysis of measured EIS data for cuff electrodes. Subfigures show the error in absolute ohms and the percentage error between NeuroZ with multi-sine waveform and CHI760E measurements.	140
A.13 Electrode Impedance Spectroscopy (EIS) comparison and interpolation results for SEEG electrodes. Subfigures illustrate the original measured data and interpolated data for consistent frequency spacing.	141
A.14 Error analysis of measured EIS data for SEEG electrodes. Subfigures show the error in absolute ohms and the percentage error between NeuroZ with multi-sine waveform and CHI760E measurements.	142
A.15 Electrode Impedance Spectroscopy (EIS) comparison and interpolation results for ECoG electrodes. Subfigures illustrate the original measured data and interpolated data for consistent frequency spacing.	143
A.16 Error analysis of measured EIS data for ECoG electrodes. Subfigures show the error in absolute ohms and the percentage error between NeuroZ with multi-sine waveform and CHI760E measurements.	144
A.17 Electrode Impedance Spectroscopy (EIS) comparison and interpolation results for Cuff electrodes. Subfigures illustrate the original measured data and interpolated data for consistent frequency spacing.	145
A.18 Error analysis of measured EIS data for cuff electrodes. Subfigures show the error in absolute ohms and the percentage error between NeuroZ with multi-sine waveform and CHI760E measurements.	146

Chapter 1

Introduction

1.1 Motivation

Neurological conditions represent a significant public health challenge in the UK, with an estimated 16.5 million cases[1]—meaning that at least one in every six individuals suffers from one or more such conditions. Moreover, around 2,500 people are newly diagnosed each year with disorders such as Parkinson’s disease, epilepsy, multiple sclerosis, or motor neurone disease. Among these, Parkinson’s disease (PD) is a progressive neurological disorder characterised by the degeneration of neurons, leading to severe motor symptoms. This age-related condition affects approximately 145,000 individuals in the United Kingdom. Similarly, over 60,000 people in the UK are affected by epilepsy, a chronic neurological disorder caused by abnormal neuronal activity in the brain. Pharmacological treatments, such as dopamine-based drugs for PD and antiepileptic drugs (AEDs) for epilepsy, are typically the first-line therapy for managing these conditions. However, over 30 per cent of epilepsy patients experience drug-resistant seizures that cannot be effectively managed with AEDs alone[2]. For such drug-resistant cases, brain surgery and alternative treatments, such as deep brain stimulation (DBS), have become vital options[3]. Recent advancements in neuromodulation technology have prioritised safety and efficiency, making DBS more widely available and increasingly considered an earlier-stage treatment for these neurological disorders[4], [5], [6].

Deep brain stimulation, or DBS, is a surgical intervention for treating neurological conditions in patients who cannot control their symptoms with drug medication. This alternative DBS treatment has been approved by the CE mark since 1993 and by the FDA in the US since 1997[7], [8], and DBS has been developed for many decades to increase its efficacy in treating various neurological and psychological disorders, such as drug addiction[9], Obsessive-Compulsive Disorder (OCD)[10], depression[11], and eating disorders[12]. In addition, DBS can also suppress tremor symptoms in patients by stimulation in the thalamus area[13]. DBS considerably improves symptoms and reduces the required drug dose in Parkinson's patients [14]. Also, DBS can improve the quality of life of patients with epilepsy by decreasing the frequency of their seizure occurrences[15].

The majority of existing therapies by DBS are mostly based on planned or continuous electrical stimulation, which requires a clinician to set the stimulation level and pattern manually. In these cases, patients may experience neurological deficiencies, including speech abnormalities and mobility problems, due to too high or low levels of stimulation. To solve these side effect problems, several studies have shown that closed-loop or responsive stimulator possibly increases the efficacy of the neurostimulation treatment [16]. For example, closed-loop DBS significantly increased the motor score in Parkinson's patients rather than continuous DBS in [17][18]; similarly, responsive DBS based on seizure onset detection can effectively reduce the frequency of seizures occurring in patients with epilepsy [19][20].

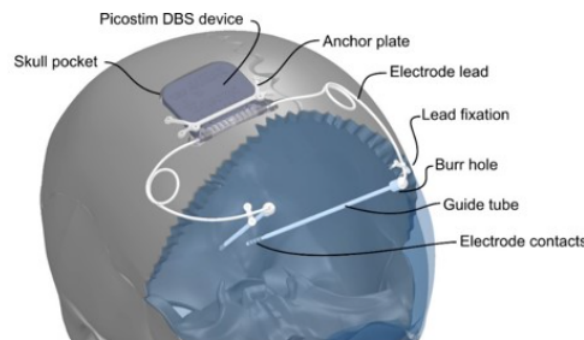


Figure 1.1: Picostim by Amber Therapeutics[21]

In addition, closed-loop neurostimulation can optimize the stimulation pattern for each patient and enhance performance by activating only when needed, thereby minimizing off-target effects

and prolonging battery life through reduced stimulation time[16]. In a closed-loop algorithm, the biosignals commonly used as biomarkers in the system are electrocorticography (ECoG), intracranial electroencephalography, local field potentials (LFP), and body movement.

A DBS device consists of multiple components, including the housing that encloses the battery and electronics, the lead, and the implanted electrodes. The electrodes are essential for stimulating neural tissue and recording signals, acting as the main interface between neuroprosthetics and the nervous system. However, these electrodes inevitably degrade over time, causing the electrode-tissue interface to exhibit distinct properties depending on implantation duration and specific conditions [22]. Additionally, the surrounding tissue continuously adapts to the implant, with foreign body responses potentially leading to tissue fibrosis and scarring. Moreover, neural stimulation at intensities sufficient to induce noticeable behavioural responses may alter nearby tissue characteristics, ultimately affecting electrode efficiency [23], [24].

Therefore, a monitoring system should be implemented to assess electrode status for both safety and performance efficiency. For safety purposes, all stimulators should be capable of monitoring electrode health, typically achieved through a basic I-V measurement, such as tracking electrode voltage during stimulation. However, as neurostimulation systems continue to advance, incorporating smaller and more numerous electrodes, the need for more rigorous characterisation has grown to ensure optimal functionality and long-term reliability. Additionally, electrode impedance is one of the electrochemical properties that reflects electrode behaviour and performance. Thus, this research aims to develop an electrode impedance measurement system and validation platform to enable long-term assessment of implantable neural interfaces.

1.2 Research Objectives

The fundamental aim of this research is to design, implement, and validate electrode impedance measurement for an implantable bidirectional neural interface. The specific research objectives are:

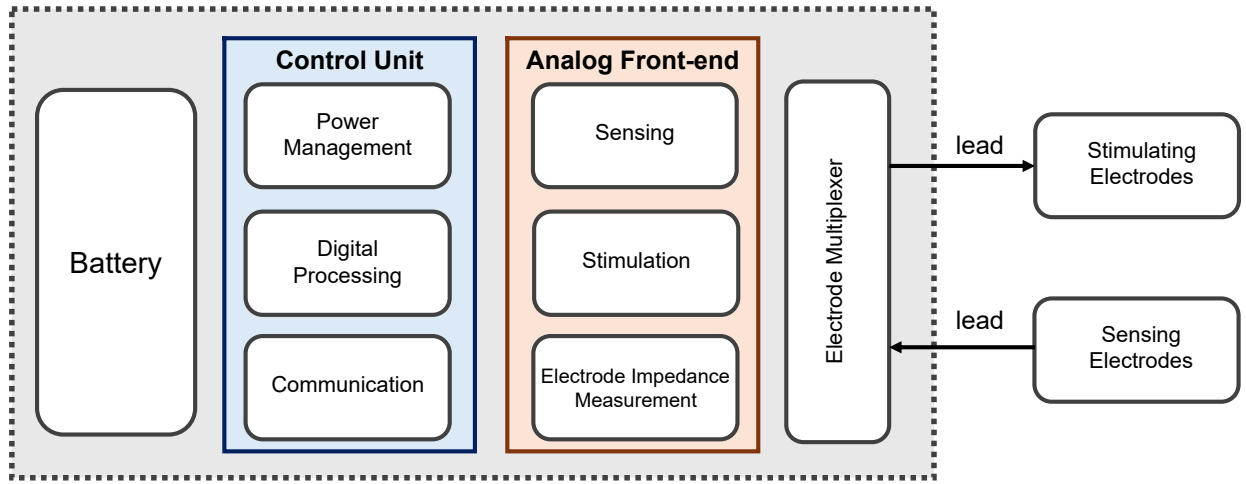


Figure 1.2: Block diagram of DBS system

- To investigate and compare suitable methods for impedance characterisation for long-term electrode monitoring.
- To design an impedance measurement capability for long-term electrode monitoring and integrate it within a bidirectional neural interface.
- To experimentally validate electrode characterisation system through *in vitro* accelerated lifetime electrode testing.

Each of the objectives stated above is addressed in a corresponding technical chapter, as outlined below:

Chapter 2: Background and State-of-the-Art

This chapter describes the fundamental theories and available technologies related to bidirectional neural interfaces and methods for measuring the impedance of implantable electrodes.

Chapter 3: Design of Accelerated Lifetime Testing Validation

This chapter explains the design of an experimental protocol for accelerating electrode degradation in phosphate-buffered saline (PBS). The automated platform enables the experiment

to alternate between stimulation and measurement periods every hour. Additionally, it supports impedance measurement using both bench-top electrochemical workstations and custom-developed devices, enhancing experimental efficiency and repeatability.

Chapter 4: Custom Bench-Top Platform for Electrode Impedance Characterisation

This chapter introduces a custom impedance measurement device designed on a PCB base. It outlines the initial hardware and software designs created for measuring and visualizing impedance, as well as validation with neural electrodes and the automated platform for accelerated lifetime testing validation.

Chapter 5: An Integrated Circuit-based EIS Platform for the Characterisation of Implantable Electrodes

This chapter presents the implementation of an electrical impedance spectroscopy (EIS) measurement circuit at the integrated circuit (IC) design level, validated using neural electrodes. Additionally, the IC chip's capability for combined multi-frequency measurements is tested and discussed.

Chapter 6: Conclusion

The final chapter provides a summary of the work presented, highlights contributions to the field, and offers suggestions for future research.

Chapter 2

Background and State-of-the-Art

2.1 Bidirectional Neural Interfaces and Close-Loop Neuromodulators

2.1.1 Available commercial closed-loop neural interface/ research platform

Several studies demonstrate that closed-loop neurostimulation is more effective than static stimulation. Nevertheless, few commercial medical devices capable of both sensing and stimulation have been approved by the FDA or received the CE mark; for example, NeuroPace's RNS system and Medtronic's Activa PC+S and Percept PC [25].

Neuropace has developed RNS (Responsive cortical Neurostimulation System) in the USA. This device is a responsive stimulation that generates an electrical stimulus in the brain at seizure foci during a seizure onset. In the RNS system, seizures are detected by recording the electrocorticographic (ECoG) signal and analysing this signal by three techniques: band-pass, line-length, and area feature analysis[16] [26]. The RNS system continually monitors ECoG activity from four sensing channels. When a seizure is observed, the data is saved with a timestamp so that a physician can monitor the brain activity throughout a long period of

therapy [27][28].

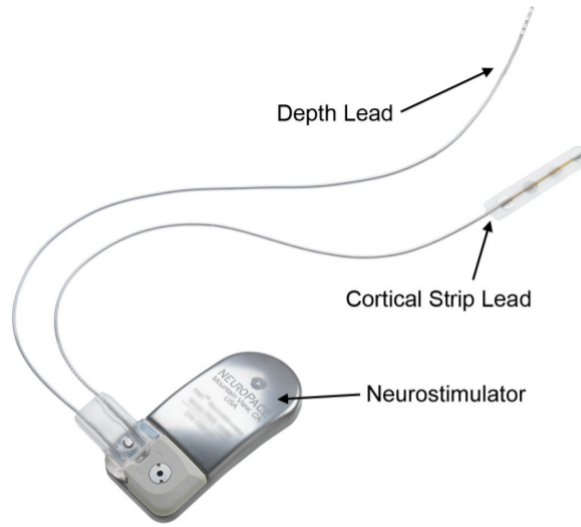


Figure 2.1: RNS (Responsive cortical Neurostimulation System) by Neuropace[25]

Another clinically-used commercial DBS device is Medtronic's Activa PC+S neurostimulator. This DBS is generally used to treat the motor symptoms caused by Parkinson's disease or essential tremor in case the medicine cannot effectively control symptoms. The neurostimulation system consists of sensing and stimulating functions that can operate concurrently. To remove stimulation artefacts from the LFP signal, common-mode rejection, a low-pass filter (less than 100 Hz), and spectral power processing are utilised in the system[29]. Besides, classification techniques such as support vector machines (SVM) are used to distinguish the desired signals(evoked action potentials and LFP) from electrical stimulation artefacts[16][30].

Activa PC+S was developed to become a new version of the DBS system called RC+S, which enhances sense-stimulation performance. Compared to the PC+S system, the Summit RC+S system has a MIC-band radio that increases the transmission distance of recorded data. In addition, custom FFT hardware has been integrated into the ASIC to minimise artefacts, DC offset, and harmonic noise. Moreover, the rechargeable system was added to improve sensing performance and extend battery life[30]. Currently, the most advanced system developed by Medtronic is Percept PC. This newest DBS device has a sensing technology called BrainSense Technology that continuously monitors and records brain signals(LFPs) from the implanted DBS lead electrodes. Thus, a clinician is able to monitor a patient's brain state and adjust

stimulation treatment following the patient's specific needs based on recorded brain activities[31][32]. However, the device is implanted in the chest while the electrodes are in the brain, signal recording relies on long leads. This setup makes the system highly susceptible to ECG artefacts, requiring an exceptionally high common-mode rejection ratio (CMRR) to recover the differential neural signals effectively[33].



Figure 2.2: Percept PC Neurostimulator by Medtronic[32][34]

The Brain Interchange System by CorTec is another simultaneous stimulation and sensing brain interface. This system is compatible with DBS lead brain stimulation, spinal cord stimulation, and other BCI applications. This implantable technology platform is fully wireless for both power delivery and data transmission. Therefore, it can be customised and flexible for any neuroscience research application. Also, this system can do both open and close-loop stimulation with a high number of channels, up to 32 channels in total, and concurrent stimulation at four channels[35]. However, a limitation of this system is the absence of an implantable battery, making it entirely reliant on a continuous wireless power link. This dependency may restrict its usability in daily life, such as in life-critical applications like deep brain stimulation (DBS) for Parkinson's disease, where consistent and uninterrupted therapy is crucial for symptom management.

2.1.2 Academic Research on Neuromodulation ASICs

Closed-loop controlled stimulation can improve stimulation therapy by minimising overstimulation and optimising the individualised stimulation setting for each patient. Although some

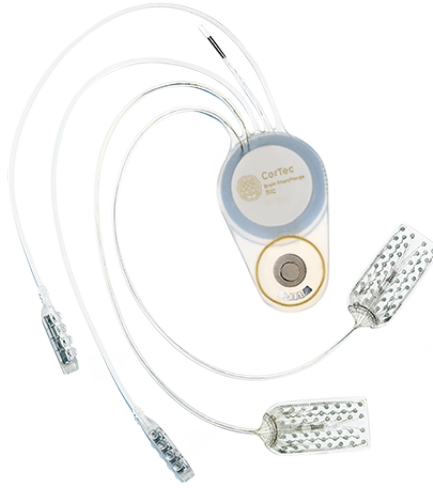


Figure 2.3: Brain Interchange System by CorTec [35]

commercial DBS devices have a closed-loop system with a bidirectional neural interface, as mentioned in the previous section, they are inflexible for some research studies due to their restricted number of sensing channels and capabilities such as concurrent sensing and stimulation. Therefore, several research groups are still developing sense-stim or bidirectional neural interface ASICs. For instance, a spectral analysis integrated circuit (IC) for chronic bidirectional BMI comprises four sensing channels, and each channel consumes 5 mW [36]. In [37], an ASIC for 32-stimulation channels and 8 low-power sensing channels with on-chip digital FFT was developed. In addition, a 0.338 cm^3 ASIC with 64 channels for simultaneous stimulation and sensing was developed and tested in [38] to collect data without stimulation artefacts. A high dynamic range sensing unit is coupled with a non-linearity correction unit in the sensing IC design, which improves the performance of recording small amplitude signals in the presence of significant stimulation artefacts. After that, the adaptive stimulation artefact rejection or ASAR unit analyses the recorded data in order to suppress stimulation artefacts and restore neural signals. In [39], Zhou created the Neuromodulation Integrated Chip (NMIC), which contains 64 recording channels and 4 stimulation channels. Two NMIC on-board are able to operate concurrently, increasing the number of recording channels to 128 for bi-directional BMI. In this system, electrical energy consumption was around $8 \mu\text{W}$ per channel.

Meanwhile, some researchers are developing ASICs for closed-loop stimulation by integrating

a sensing interface into the system. This allows real-time recording of brain activity as a biomarker, enabling feedback-driven regulation of stimulation. However, recording neural signals such as local field potentials (LFPs) during stimulation remains challenging due to the large amplitude difference—the stimulation voltage is approximately five to six times higher than the neural signals (on the millivolt scale). This disparity can cause amplifier saturation, making it impossible to extract the neuronal signal free from stimulation artefacts.

Several noise reduction techniques have been proposed to address this issue. For instance, chopper amplifiers and AC-coupled amplifiers help minimize DC offset and 1/f noise [40][41][42]. Common-mode rejection techniques have also been employed to eliminate stimulation artefacts [30]. Additionally, filters such as low-pass and high-pass filters can reduce electrode polarization and harmonic noise [28].

2.2 Neural interface electrodes

Implantable neural electrodes are designed to establish a connection between biological tissue and recording or stimulation devices. These electrodes come in various shapes and sizes, depending on their intended application. Some electrodes are placed on the surface of the skin or tissue, while others are inserted into the body to interact more directly with neural signals. The design and material composition of these electrodes are carefully selected to ensure compatibility with biological systems, optimize signal quality, and support long-term functionality in medical and research applications.

Peripheral Nerve Electrodes

Peripheral nerve electrodes are categorized into extraneural electrodes (cuff electrodes) and intraneural electrodes; for example, Longitudinal IntraFascicular Electrode (LIFE)[43], Transverse IntraFascicular Multichannel Electrode (TIME)[44], and Utah Slanted Electrode Array (USEA)[45] interfaces. The cuff electrode, wrapped around the nerve, has several variants, including the split ring, self-sizing, and flat interface nerve electrode (FINE), which improves

spatial resolution by flattening the nerve. In contrast, LIFE is a flexible wire inserted along a fascicle, TIME is a polyimide strip with platinum sites threaded transversely through the nerve, and USEA features an electrode array with varying heights to interface with multiple fascicles. The cuff electrode stands out as the most promising for neuroprosthetic applications due to its superior longevity, good spatial resolution, and successful human trials. While USEA offers high spatial resolution, its longevity is inadequate for clinical use, and the long-term stability of LIFE and TIME electrodes remains uncertain[46].

Designed for stimulating and recording compound action potentials from peripheral nerves, the cuff electrode is wrapped around the nerve and typically has a tripolar configuration with surface contacts. These contacts, made of platinum, generally range from 1 to 3 mm in length. Each contact of a cuff electrode typically exhibits a low and consistent impedance, with a 1 mm contact measuring approximately 6 k Ω and a 3 mm contact about 1 k Ω at 1 kHz [47].

DBS Lead electrodes

DBS electrode is the electrode typically used in the clinical cases for treating movement disorders such as Parkinson’s disease[48], epilepsy[49], and essential tremor[50]. These electrodes, commonly made of platinum-iridium alloy or platinum, are designed to deliver precise electrical stimulation to targeted brain regions, including the Thalamus (responsible for sensory and motor signal processing), the Subthalamic nucleus (involved in movement planning), and the Globus pallidus (which modulates motor activity).

As an example of standard clinical designs, commercial DBS leads such as the Medtronic 3387/3389 models are insulated with polyurethane (PU) for durability and biocompatibility. Each electrode contact is approximately 1–1.5 mm long, with impedance values typically ranging from 1 k Ω to 10 k Ω at 1 kHz [51], [52].

Stereoelectroencephalography (SEEG) electrode

SEEG electrode is an invasive depth electrode used primarily for mapping and diagnosing epilepsy, particularly in patients with refractory focal epilepsy. These electrodes are surgically implanted into specific brain regions, allowing for direct intracranial monitoring of electrical activity from both cortical and subcortical brain tissue. SEEG electrodes are crucial for accurately localising epileptogenic zones, which are the regions where seizures originate. SEEG became a standard method for pre-surgical epilepsy localisation, especially for deep brain structures that are difficult to access using ECoG[53]. Additionally, SEEG recordings are valuable in brain-machine interface studies and other neuroscientific research, as they offer precise data from deep brain regions without the need for extensive craniotomy[54].

ECoG electrode

ECoG electrodes are flat arrays of millimetre-scale metal contacts fabricated on a flexible substrate. They are typically placed on the cortical surface to record local field potentials (LFPs) from the brain. Because they do not penetrate the brain tissue, ECoG electrodes are considered less invasive than depth or penetrating electrodes. Each contact is typically 1–2.3 mm in diameter, and the impedance ranges from approximately 1.5 k Ω to 5 k Ω measured at 1 kHz[55] [56].

Microelectrode Array (MEA)

Microelectrode arrays (MEAs) are designed for extracellular neural recordings, with different types offering varied structures and electrical properties. Michigan-type arrays consist of a single silicon shank with recording sites distributed along its length, typically measuring 50 μm $\times$ 100 μm and 8 mm long. These probes facilitate depth-resolved recordings but have limited lateral coverage[57]. Utah arrays, on the other hand, are three-dimensional, bed-of-needles structures composed of a grid of penetrating silicon microelectrodes, each with a recording site at the tip. Their vertical arrangement allows for dense intracortical recordings, making them

good for brain-computer interface applications[58].

Tetrodes are constructed from four closely bundled microwires, enabling better spike sorting by capturing action potentials from multiple orientations. Their small size enhances single-unit discrimination, although they provide lower spatial coverage compared to array-based systems[58]. CMOS-based MEAs integrate high-density electrodes with on-chip amplification, reducing signal noise and allowing simultaneous recordings across many channels. The Neuropixels probe, for instance, features 960 recording sites, each measuring $12\mu\text{m} \times 12\mu\text{m}$ and spaced $25\mu\text{m}$ apart, fabricated using $130\mu\text{m}$ CMOS technology[57].

The impedance of these MEAs varies significantly depending on their material and size. Larger electrodes (e.g., Utah arrays) generally have lower impedance, which reduces thermal noise and enhances the signal-to-noise ratio (SNR). In contrast, smaller electrodes (e.g., CMOS arrays) require surface modifications, such as PEDOT coatings or platinum black deposition, to decrease impedance while maintaining recording fidelity[59]. Advances in flexible materials, such as polyimide-based arrays, help reduce mechanical mismatch with neural tissue, improving long-term biocompatibility and minimizing inflammatory responses[59].

2.2.1 Electrochemical mechanism in the electrode-electrolyte interface

When a metal electrode is immersed in an ionic solution like extracellular fluid, an electrode-electrolyte interface is formed between the metal and solution phases. At the interface, two electrochemical processes are taking place during the stimulation: the Faradaic reaction and the non-faradiac (or capacitive) reaction. In terms of electronic RC, this non-faradiac reaction may be represented as a double-layer capacitor (C_{dl}), with the resistance (R_e) representing the faradiac process of oxidation and reduction at the interface. As a result, the electrode-electrolyte interface between an implanted electrode and tissue has non-linear properties, which can be represented as in the Randle model[60].

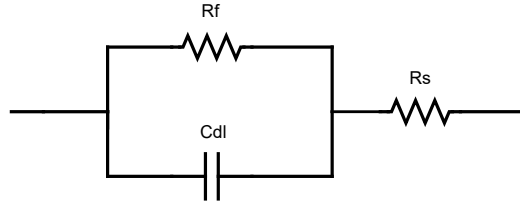


Figure 2.4: Equivalent circuit of electrode/electrolyte interface

The impedance of this electrode-electrolyte can be calculated across different frequencies as

$$Z_e(\omega) = R_s + \frac{R_f}{1 + (\omega C_{dl} R_f)^2} - \frac{j\omega C_{dl} R_f^2}{1 + (\omega C_{dl} R_f)^2} \quad (2.1)$$

$$R_f(\omega) = \frac{(Z'')^2 + (Z' - R_s)^2}{(Z' - R_s)} \quad (2.2)$$

$$C_{dl}(\omega) = -\frac{Z''}{\omega[(Z'')^2 + (Z' - R_s)^2]} \quad (2.3)$$

Where Z_e is the electrode-electrolyte impedance, R_s is electrolyte or solution resistance, C_{dl} is the double layer capacitance, R_f is faradiac reaction resistance, and ω is an angular frequency.

2.2.2 Recording electrodes

The key requirement for recording electrodes is low impedance relative to the amplifier's input impedance, whereas stimulation electrodes must ensure a safe and reversible electrochemical reaction at the electrode-electrolyte interface during charge injection. For recording applications, electrode impedance strongly influences both sensitivity and spatial selectivity. A lower-impedance electrode reduces thermal noise and improves the detectability of neural activity from neurons located at greater distances from the electrode surface [61], [62]. According to the quasi-static model of extracellular potentials [63], the voltage generated by a neuronal current source decreases approximately as the inverse of distance, expressed as

$$V(r) = \frac{I}{4\pi\sigma r},$$

where $V(r)$ is the extracellular potential at distance r , I is the transmembrane current, and σ is the tissue conductivity. Consequently, the signal amplitude attenuates with increasing distance, and low-impedance electrodes are advantageous for recording neurons farther away by maintaining a higher signal-to-noise ratio [64].

Two key factors influencing the charge-transfer mechanism at the electrode–electrolyte interface are the electrode area and the electrode material. When both the working and counter electrodes are made of the same material, the interface impedance can be reduced by increasing the effective surface area of the electrode. Conversely, if the geometric area is fixed, impedance can be further decreased by modifying or coating the surface with a material of higher microscopic roughness or porosity. Such coatings, including platinum black, iridium oxide, or poly(3,4-ethylenedioxythiophene):polystyrene sulfonate (PEDOT:PSS), increase the electrochemically active surface area, thereby enhancing double-layer capacitance and lowering interface impedance [65], [66], [67]. A larger effective surface area also reduces thermal noise, improving electrode sensitivity and signal-to-noise ratio (SNR), which leads to higher-quality neural recordings [61], [62].

Impedance is often measured at 1 kHz in many studies, as this frequency corresponds to the dominant spectral content of action potentials and facilitates comparison between electrode designs [65], [66], [67], [68], [69]. However, neural recordings cover a wide frequency range that includes both action potentials and low-frequency local field potentials (LFPs). Because electrode impedance varies with frequency, a single 1 kHz measurement does not fully represent electrode behaviour across all signal bands, particularly for low-frequency LFPs, making it an incomplete indicator of overall performance [68], [69].

2.2.3 Stimulation Electrodes

For the stimulation electrode, there are two phases of pulse stimulation, which are the cathodal and anodal phases. A cathodal phase is a phase in the direction of electrons flowing from the electrode surface to the tissue; on the other hand, an anodal phase is when electrons flow from

the tissue to the electrode. The charge delivered during each phase can be calculated by the time integral of the stimulation current[65].

Charge balancing in the cathodal and anodal phases of electrical stimulation pulses is an important key in avoiding damage to surrounding tissue and electrode degradation. The main purpose of this balancing is to maintain the electrode potential in the range that does not induce irreversible reactions, including reduction and oxidation, at the surface of the electrode. However, there are some cases in which a charge-balanced waveform cannot prevent electrode degradation, so current and charge densities need to be limited to keep only reversible processes occurring at the electrode-electrolyte interface.[65], [70], [71], [72]

Electrode voltage or potential, which charges and discharges during the current injection, can be observed by the shape of the voltage drop across two electrodes[70]. In addition, Electrode voltage needs to be only within the water window range to prevent the irreversible reaction of water, which can cause bubbles (H_2 and O_2) and tissue damage in the brain, as in the equation below[68] .

Reduction of water



Oxidation of water



2.3 Electrochemical measurements

To develop an effective electrode characterisation system for implantable neural interfaces, it is crucial to understand the electrochemical processes and performance parameters of the electrode-electrolyte interface in implantable electrodes used in clinical studies. Electrochemical measurement techniques such as cyclic voltammetry, voltage transients, and impedance spectroscopy offer valuable insights into the characteristics of the neural electrode-electrolyte interface.

Cyclic voltammetry

Cyclic voltammetry (CV) is a widely used electrochemical technique for characterising electrodes by sweeping the potential cyclically and measuring the resulting current. CV provides information on the electrochemical behaviour of electrode materials, including charge storage capacity (CSC), electrode potential limits, and reaction reversibility. For neural electrodes, CV is particularly useful for assessing performance in both *in vitro* and *in vivo*. While the CV profiles of materials like platinum and titanium nitride are well-established *in vitro*—for instance, ranging from -0.6 V to 0.8 V versus Ag/AgCl for Pt and PtIr alloy [65] and -0.9 V to 0.9 V versus SCE for titanium nitride [73]—*in vivo* measurements often vary due to interactions with the biological environment, such as tissue encapsulation and electrode surface degradation. However, reaching the "water window," where water electrolysis occurs, can be unsafe in clinical settings, limiting the use of CV in certain chronic clinical applications.

Voltage Transients

The voltage transient (VT) is a crucial electrochemical measurement for estimating the maximum amount of charge that can be injected during a current-controlled stimulation pulse. Typically, VT is conducted using a three-electrode setup consisting of a working, counter, and reference electrode. It measures the maximum polarization across the electrode-electrolyte interface by recording the most negative and most positive potential values during current injection. The current is then adjusted until the voltage reaches the water window potential, allowing for the determination of the maximum charge injection capacity (CIC)[65]. This capacity is considered a safety limit to avoid electrode or tissue damage and also as the maximum stimulation performance of electrodes.

Electrochemical impedance spectroscopy

The impedance at 1 kHz is a commonly used metric for characterising implantable neural electrodes due to its ease of measurement and comparability across systems. However, this value

primarily reflects the resistive components of the electrode system, providing limited insight into the capacitive behaviours critical for understanding the electrode's performance across a broader frequency range. For example, in large electrodes like those used in spinal cord stimulation (SCS), 1 kHz impedance is dominated by resistive elements, which may not fully capture the electrode-electrolyte interface properties or the interactions with biological tissue[74].

While convenient, 1 kHz impedance alone is insufficient for comprehensive electrode characterisation, Electrochemical Impedance Spectroscopy (EIS) offers a more detailed approach by measuring impedance across a wide frequency range, enabling a deeper understanding of the electrochemical processes at the electrode-electrolyte interface [75]. EIS can monitor changes in ion transport and electrochemical behaviour over time as a non-destructive measurement technique, making it particularly useful for evaluating implanted electrodes. It provides insight into neural electrode performance at relevant frequencies, such as 10–300 Hz for local field potentials (LFPs) and 700–15,000 Hz for single-unit recordings [76]. Additionally, EIS data can be modelled as equivalent circuits to reveal factors such as charge transfer dynamics and the effects of tissue encapsulation [77], providing a more comprehensive understanding of electrode performance.

Electrode-electrolyte interface model

The electrode-electrolyte interface is a critical region where charge transfer occurs between the metal electrode, which conducts charge via electrons, and the electrolyte, which conducts charge via ions in the solution. This interface connects the implantable research platform device to neural tissue. Two main types of charge transfer mechanisms are observed at this interface, including Non-Faradiac (Capacitive) Charge Transfer and Faradiac Charge Transfer. In the Non-Faradiac mechanism, no actual electron transfer occurs across the interface. Instead, it involves a redistribution of ions at the boundary, forming a capacitive double layer. The electrode stores charge like a capacitor at the interface, creating an electric field. The system can be modelled electrically by a double-layer capacitor (C_{dl}).

The Faradaic mechanism involves actual electron transfer between the electrode and electrolyte, resulting in chemical reactions such as reduction or oxidation. Faradaic reactions can be reversible or irreversible, depending on whether the reaction products remain near the electrode or diffuse away. This is represented by Faradaic impedance ($Z_{faradiac}$), accounting for both resistance and capacitance due to chemical reactions at the interface. In addition to these components used to model the electrode-electrolyte interface, another important element is solution resistance (R_s), which is the resistance of the electrolyte solution between the electrodes.

2.4 Electrochemical Impedance measurement technique

Electrochemical Impedance Spectroscopy (EIS) is a measurement that represents the electrochemical mechanisms of the electrode-electrolyte interface. Typically, the EIS is measured by applying a small electrical voltage or current to the electrodes and then measuring the current or voltage response to calculate the phase shift and amplitude of impedance over the frequency range. [78] [79]

$$|Ze| = \sqrt{Re(Ze)^2 + Im(Ze)^2} \quad (2.6)$$

and

$$\phi = \arctan\left(\frac{Im(Ze)}{Re(Ze)}\right) \quad (2.7)$$

Where Z_e is the impedance of the electrode, and ϕ is the phase shift.

Two primary techniques used for electrochemical impedance analysis are the single-sine and FFT-based measurement methods. In the single-sine technique, a low-amplitude sinusoidal voltage or current is applied to the electrode under test, and the corresponding response is measured to determine the impedance at that specific frequency. The process is then repeated while sweeping the excitation across the frequency range of interest. Although this method pro-

vides high accuracy and effectively rejects noise and harmonic interference, it is time-consuming and unsuitable for time-varying systems, where the electrode properties may change during the lengthy frequency sweep [80], [81], [82].

The FFT-based or multisine technique enables faster impedance measurements by applying a composite waveform that contains multiple sine components at different frequencies. The resulting current and voltage responses are recorded, and the impedance spectrum is calculated using the Fourier transformation[80], [81]. However, when multiple frequency components are summed, the instantaneous amplitude of the waveform can become large, potentially driving the electrode–electrolyte interface into a nonlinear regime and introducing harmonic distortion[83], [84]. To mitigate this, the phases of the sine components are often adjusted—using random or optimised phase arrangements—to minimise peak amplitude and produce a smoother excitation signal[81], [84]. Despite its speed advantage, the FFT-based approach can suffer from reduced signal-to-noise ratio (SNR) and is more sensitive to nonlinear or time-dependent changes in the system [85].

In both single sine and FFT techniques, if the amplitude of stimulus is high, this can cause non-linearity between current and voltage, which decreases the measurement accuracy. In FFT-based measurements, approximately 10–15 frequency components are typically distributed per decade across the frequency spectrum. The selected frequency range should avoid excessively high or low frequencies that could introduce noise or instability in the excitation signal. Also, the sampling rate needs to be higher than two times the maximum frequency in the range to avoid the alias problem [82], [85].

Another approach, commonly adopted in some commercial neural stimulators, estimates electrode impedance by analysing the voltage response to constant biphasic current pulses[86], [87]. This method, often referred to as the voltage transient (VT) technique, records the electrode potential during current injection to estimate impedance and evaluate charge-injection safety limits **Cogan2008**, [52]. While VT provides valuable real-time information for electrode monitoring, it differs from EIS in both principle and outcome. Specifically, VT captures the electrode’s transient behaviour during stimulation, whereas EIS characterises its frequency-dependent elec-

trochemical properties. Consequently, VT generally yields less accurate impedance values than the single-sine and FFT-based EIS techniques but offers complementary information regarding electrode performance.

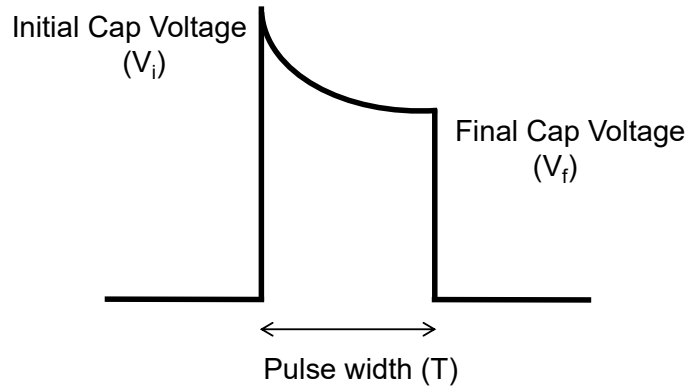


Figure 2.5: The measured voltage waveform between two electrodes during the stimulation pulse. The diagram is adapted from [88]

2.5 Electrode Impedance Measurement on IC Chips

Impedance measurement is fundamental to the development and optimization of implantable neural interfaces, particularly in neural recording and stimulation applications. It enables precise characterisation of the electrode-tissue interface, facilitates real-time monitoring of electrode health, and ensures safe and effective stimulation. Over the years, a variety of techniques, from academic prototypes to commercially available systems, have been developed to meet the unique demands of these applications.

Several academic studies have explored innovative techniques for impedance measurement. For instance, current-driven square-wave injections combined with advanced voltage measurement techniques are commonly used to estimate the electrode-tissue transfer function. In [89], a current square wave is injected, and the resulting voltage response is measured by a neural amplifier. By modelling the electrode-tissue interface as a simplified electrical circuit, the impulse response of the system is analysed to compute impedance. Similarly, [90] employs a frequency-shifting chopper circuit to minimise noise and drift, injecting square wave currents and analysing demodulated voltage responses to achieve impedance measurements across a

Table 2.1: Comparison ASIC for EIS measurement for implantable neural interface

Specification	Haas et al.	Ko et al.	Zamani et al.	Huang et al.
CMOS Technology Process	0.18 μm	0.13 μm	0.18 μm	0.18 μm
Power Supply	NA	1 V	1.8 V	1.8 V
Power Consumption	58 μW per channel	52 μW (entire IC)	1.55 μW (impedance measurement)	13.22 μW per channel (impedance measurement)
Number of Channels	1 channel (Simultaneous measurement of 1 electrode)	Single channel (no multiplexer)	Single channel (no multiplexer)	16 channels (multiplexer)
Electrode Configuration	2-electrode	4-electrode	4-electrode	2-electrode
Impedance Measurement Technique	Impulse Response Estimation	Frequency Shifting Chopper	Lock-in Amplifier with Semi-Square Current	Differential current switch with CMFB bias
Impedance Measurement Methodology	Low-gain neural amplifier mode measures electrode-tissue impedance by estimating the transfer function.	frequency-shifting chopper-based instrumentation amplifier for impedance measurements with high-frequency signal analysis.	injecting a semi-square current waveform into the tissue and using a lock-in amplifier to extract in-phase and quadrature components of impedance.	Current-steering architecture with common-mode feedback (CMFB) to inject precise currents and measure resulting voltages.
Modulation or Waveform	Square Waveform	Square waveform	Semi-ramp waveform	Step current
Frequency Range	15 mHz to 70 Hz	0.25 kHz - 1.24 MHz	2 kHz	15.625 Hz
Amplitude of Injected Current or Voltage	300 mV (Voltage Pulse)	Programmable 0-169 μA	1 μA	2 μA
Impedance Range (Minimum/Maximum)	0-30k Ω	0-800 Ω (programmable)	100 Ω - 3.3 k Ω	1 k Ω - 100 k Ω
Impedance Resolution	NA	NA	1.35 Ω_{rms}	17 Ω_{pp}
Impedance Measurement Error	15%	0.24% (from impedance measurement results)	3.12% (systematic and non-sinusoidal input errors)	3.4% (from impedance measurement results, fabrication mismatch considered)
Electrode Type	NA	NA	Cardiac tissue electrodes	Subdural grid electrodes
<i>In Vivo</i> Validation	No	Yes	No	No
Chip Area	0.204 mm ²	NA	0.055 mm ²	3.8 mm ²
Applications	Neural stimulation safety and monitoring (e.g., DBS, ECoG electrode-tissue impedance monitoring)	Bioimpedance measurement for body composition analysis	Bioimpedance measurement for cardiac pacemaker	Electrode-tissue impedance for neurostimulation
References	[89]	[90]	[91]	[92]

Table 2.1: (continued) Comparison ASIC for EIS measurement for implantable neural interface

Specification	CINESIC32	WIMAGINE	NeuroPace RNS System	RC+S	Automated Impedance Measurement System	Intan RHS2116
CMOS Technology	0.35 μm	0.18 μm	NA	NA	NA	NA
Power Supply	3.3 V	3.3V	3 V	NA	Battery-powered	3.3 V
Power Consumption	134 μW per channel (ECoG recording)	134 μW per channel (ECoG recording)	1.55 μW (entire system)	NA	NA	Low power (<1 mW, complete interface)
Number of Channels	32 channels (multiplexer)	64 channels (multiplexer)	2 channels (multiplexer)	1 channels	Multiple channels (configurable)	16 channels (multiplexer)
Electrode Configuration	2-electrode	4-electrode configuration	2-electrode	2-electrode	2-electrode	2-electrode
Impedance Measurement Technique	Injected current and measured electrode Voltage	NA	DC Impedance/ Ohm's law	DC Impedance/ Ohm's law	Automated Measurement via Stimulation Pulses	DAC and Capacitor for sine wave generation and impedance measurement
Impedance Measurement Methodology	Low-noise amplifier with differential output	Low-noise differential amplification	NA	NA	Voltage-based measurement with RC parameter calculation	8-bit DAC and 0.1,1,10 pF
Modulation or Waveform	Sinusoidal wave	NA	Charge balanced, biphasic square wave pulses	Square waveform	Stimulation pulse	Sinusoidal wave
Frequency Range	40 Hz	NA	10 - 1 kHz (recording cut-off frequency)	1-4kHz	NA	<10kHz
Amplitude of Injected Current or Voltage	20 nA	10-500 μA	3 mA (40 ms/phase)	0.4 mA (80 ms/pulse)	NA	38 nA (max)
Impedance Measurement Range (Minimum/Maximum)	1 k - 10 k Ω	100 - 10 k Ω	50 - 5 k Ω	NA	NA	50 - 1 M Ω
Impedance Resolution	1 Ω	1 Ω	0.5 Ω	NA	NA	NA
Impedance Measurement Error	NA	NA	5% (systematic impedance variability)	NA	NA	NA
Type of Electrode Tested	ECoG electrodes	ECoG electrodes	Depth and cortical electrodes	DBS Lead electrode	Leads with multiple electrode pairs	MEA electrodes
<i>In Vivo</i> Validation	No	No	Yes	No	No	-
Chip Area	86 mm ²	Ø50 mm (device)	NA	NA	NA	4.94 × 4.74 mm ²
Applications	Low-power ECoG recording for BCIs	Wireless, long-term ECoG recording	Responsive neurostimulation for epilepsy	Bioimpedance measurement for Neural interface	Automated impedance measurement for neurostimulators	Miniaturized neural recording and stimulation
References	[93]	[94]	[27], [95]	[86]	[87]	[96]

wide frequency range (0.25 kHz to 1.24 MHz). In [91], semi-square waveform currents are injected, and a lock-in amplifier extracts the in-phase and quadrature components to estimate impedance magnitude and phase. These approaches demonstrate the precision and adaptability of academic methodologies for diverse biomedical applications.

Additionally, [92] introduces a differential current switch architecture with common-mode feedback (CMFB) bias for impedance measurement. In this method, precise step currents are injected into the electrode-tissue interface, and the resulting voltage is measured at a frequency of 2 kHz. The CMFB ensures stability and minimizes fabrication mismatches, achieving an impedance resolution of $17\ \Omega$ with a measurement range of $1\ \text{k}\Omega$ to $100\ \text{k}\Omega$. This technique, validated using subdural grid electrodes in phosphate-buffered saline (PBS), demonstrates high accuracy for neural stimulation and monitoring applications.

There are many academic neural interface designs; however, few neural interface ASICs integrate impedance measurement functionality directly on-chip. The CINESIC32[93] and WIMAGINE[94] systems represent significant advancements in this area. The CINESIC32 circuit, designed for ECoG recording, includes an impedance measurement block that injects sine-wave currents at 20 nA and 40 Hz to characterise the electrode-tissue interface. However, the system does not extensively detail the methodology for the impedance circuit design or the calculation process. The WIMAGINE system, a wireless ECoG recording platform, employs two interconnected CINESIC32 chips to support 64 channels. Although the WIMAGINE paper includes *in vivo* experimental graphs showcasing impedance measurements in monkeys, it does not elaborate on the circuit implementation or methodologies used for impedance characterisation. These systems highlight the integration of neural recording and impedance measurement, albeit with a limited focus on impedance-specific methodologies.

The NeuroPace RNS[27], [95] and Medtronic RC+S [86] systems are commercial neurostimulators that utilize current pulse injection to measure impedance using *Ohm's Law*:

$$Z = \frac{V_{\text{measured}}}{I_{\text{pulse}}}.$$

This method ensures consistent monitoring of electrode-tissue status. For example, the NeuroPace manual specifies that if the impedance of a deep brain or cortical electrode exceeds $350\ \Omega$ or falls below $250\ \Omega$, the electrode must be replaced or removed.

Additionally, the impedance of implanted electrodes in medical devices can be calculated from the electrode potential measured during the current stimulation pulse [88], as in the equation below.

$$V_f = V_i \times e^{T/RC} \quad (2.8)$$

Thus,

$$R = T / (C \times \ln(V_i/V_f)) \quad (2.9)$$

Where R is the equivalent resistor, and C is the equivalent capacitor of the electrode model. T is the stimulation pulse width. V_i is the initial voltage, and V_f is the final voltage of the measured pulse, as shown in Fig. 2.5.

Another commercial bidirectional neural interface, the Intan RHS2116[96], incorporates advanced impedance measurement functionality. The device generates sine-wave currents using a digital-to-analogue converter (DAC) and capacitors. By injecting programmable sine currents and measuring the voltage response, the impedance is calculated with high precision. The Intan device integrates neural recording and impedance monitoring, offering versatility in electrophysiological and neuroprosthetic applications.

The impedance measurement which has been developed within this research group is only PCB-based. The PCB-based bioimpedance measuring equipment described in [97] is used to determine the impedance values in each tissue area. The stimulation components of this system employ a DAC to create a customised multi-tone sinusoidal waveform, which is subsequently transformed to current using a voltage-to-current converter. The current output is injected into one pair of electrodes, whereas the voltage is measured by the other pair of electrodes.

The recorded voltage is amplified by the instrument amplifier, and then it is pre-processed with FFT in the microcontroller before it is analysed on a computer to create the tissue impedance map in Matlab.

2.6 Accelerated lifetime testing for neural interface electrode

Several methods have been proposed in the literature to reduce the time required for validating the long-term integrity of implant electrodes. One such technique involves temperature elevation, accelerating the chemical reaction rate of electrodes immersed in an electrolyte. However, excessively high temperatures can induce reactions that do not typically occur at normal biological temperatures ($\sim 37^\circ\text{C}$).

Another accelerated aging method for testing electrode stability is the reactive oxygen species (ROS) technique. This approach involves adding hydrogen peroxide (H_2O_2) to the electrolyte, mimicking the immune response, such as inflammation, in the human body. The addition of H_2O_2 significantly increases the corrosion rate of tungsten immersed in phosphate-buffered saline (PBS), from 300-700 $\mu\text{m}/\text{year}$ to 10,000-20,000 $\mu\text{m}/\text{year}$, as reported in [98].

A combination of both temperature elevation and the addition of H_2O_2 (or ROS) is referred to as the reactive accelerated aging (RAA) protocol. Temperature elevation can alter the structure of the electrodes and the insulation layer coating their surface. Meanwhile, the addition of H_2O_2 or ROS accelerates the dissolution of metal materials. Consequently, the RAA protocol effectively simulates electrode degradation, as demonstrated in [99], [100]. However, the RAA method still requires seven days and a high temperature of 87°C to produce impedance changes equivalent to those observed after six months of *in vivo* testing [99].

Chapter 3

Design of Accelerated lifetime testing validation

3.1 Design of Accelerated electrode degradation system

To validate the impedance measurement system, a significant amount of time is required to create degradation on the electrode. Thus, it is necessary to design a method to accelerate the degradation reaction on the electrode in order to validate the impedance measurement device, which will be developed as part of the final objective of the thesis. Therefore, an electrode degradation-accelerating system was designed and published at the BioCAS 2022 conference[101]. The accelerated testing protocol and results will be explained in this chapter.

3.1.1 Methodology

The electrode degradation was accelerated by immersing a bare tungsten wire in PBS, with the temperature maintained at 67°C using a hot plate stirrer. Meanwhile, monophasic current pulses were applied between the tungsten wire and the Pt sheet until the bare tungsten wire

Portions of the research presented in this chapter have been published in V. Manatchinapisit, A. Rapeaux, I. Williams, and T. G. Constandinou, "Accelerated testing of electrode degradation for validation of new implantable neural interfaces," in *Proc. IEEE BioCAS*, Taipei, Taiwan, 2022, pp. 534-538 [101].

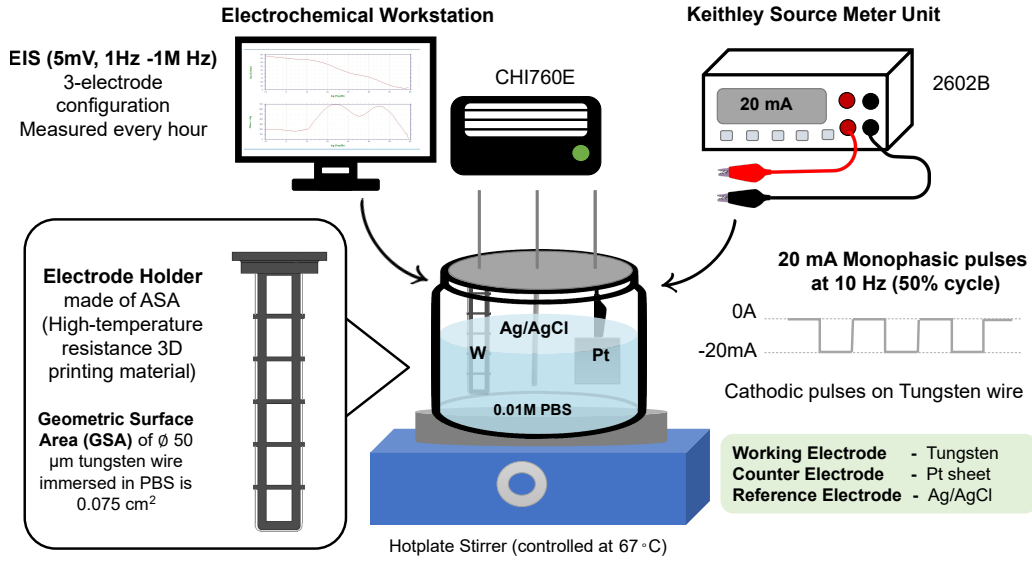


Figure 3.1: Overall experiment system including EIS measurement, current pulse simulation, and 3-electrode electrochemical cell from [101]

failed. Additionally, the Electrochemical Impedance Spectroscopy (EIS) was measured every hour during the experiment.

• Electrochemical Impedance Spectroscopy (EIS)

EIS is an electrochemical measurement technique [75] commonly used to characterise and predict the electrochemical properties of implantable electrodes. For instance, the electrode impedance at brain frequencies indicates the performance of the neural electrode. Furthermore, the impedance spectrum measured from the electrode can be fitted to electrode-electrolyte equivalent circuit models, which provide insights into charge transfer characteristics and the electrode surface integrity. From many studies, tissue encapsulation can also be included in the model to estimate the electrode's performance after implantation [102], [103]. Consequently, EIS should be measured to characterise and monitor the functionality of implanted electrodes.

In this experiment design, the EIS was measured in potentiostatic mode and recorded every hour to observe the progression of impedance related to electrode degradation using the Electrochemical workstation (CHI 760E). The voltage amplitude of the EIS measurement was 5 mV, and the frequency spectrum was swept from 1 Hz–1 MHz. Furthermore, the EIS measurements in this experiment were performed in an open-circuit state.

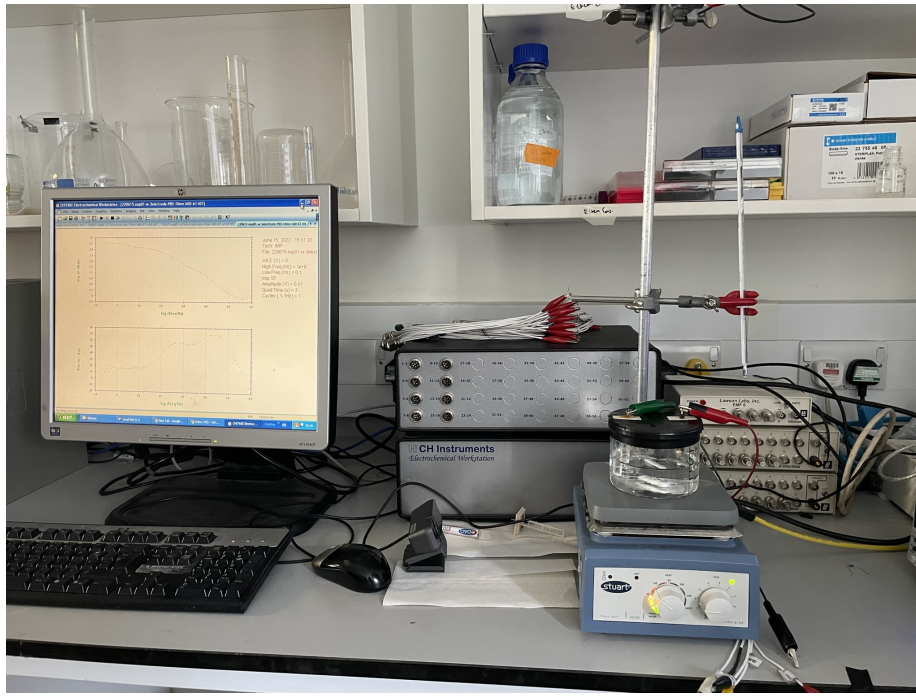


Figure 3.2: Electrochemical workstation and 3-electrode configuration electrochemical cell.

- **Tungsten wire electrode**

In the past, some neural recording electrodes were made of tungsten, which is a bio-compatible material. Tungsten also has the ability to create a protective oxide layer when immersed in an electrolyte with a pH below 4. However, the neutral pH of human physiological fluid is about 7.4, so the anodic electrochemical reaction at the electrode-electrolyte interface inside the body can still produce soluble tungsten ions (WO_4^{2-}), which leads to corrosion of the tungsten microelectrode implanted in vivo [104]. Moreover, when tungsten is used in electrical stimulation applications, an increase in potential can cause further corrosion. Thus, tungsten was chosen in this experiment to verify the overall protocol initially because it has the potential to degrade rapidly.

The impedance spectrum of the electrode wire was measured under the three-electrode configuration. The working electrode was a bare tungsten wire, which had a diameter of $50\text{ }\mu\text{m}$ and was fixed on an electrode holder made of Acrylonitrile Styrene Acrylate (ASA), which has high resistance to temperature. The total length of the wire immersed in the PBS solution was 5.014 cm , while the total geometric surface area was 0.075 cm^2 . The counter electrode was a $25 \times 25\text{ mm}$ Pt sheet, and the reference electrode was a

leakless miniature Ag/AgCl reference electrode by eDAQ. The electrolyte solution was 0.01 M Phosphate Buffered Saline (PBS), which mimics the ion concentrations of human biological fluid *in vitro*. This PBS solution acts as a buffer to maintain the pH of the electrolyte at around 7.4, which is the pH of human physiological fluid.

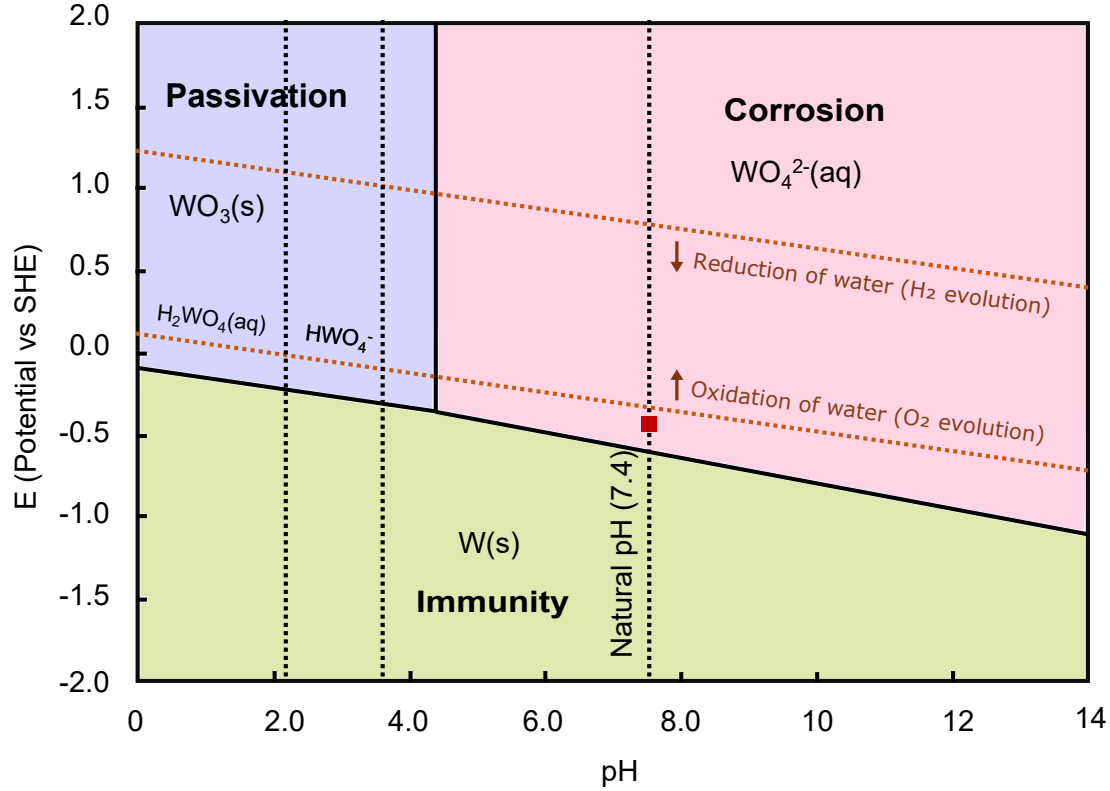


Figure 3.3: Pourbaix or potential- pH equilibrium diagram of tungsten in PBS after 15 days. The diagram demonstrates three regions, including corrosion (WO_4^{2-}), immunity (W), and passivation (WO_3). The diagram is adapted from [98]

• Electrical stimulation

In neural stimulation, waveform design strongly influences both electrode stability and tissue safety. Direct current (DC) stimulation can deliver the largest net charge transfer, but continuous charge flow drives irreversible electrochemical reactions—including water electrolysis, metal dissolution, and local pH changes—which lead to gas formation, tissue injury, and electrode corrosion [65], [105]. Monophasic pulses limit continuous current delivery and are therefore safer than DC; however, their lack of charge balancing still allows accumulation of reaction products and electrode degradation [65], [70]. In contrast, *charge-balanced biphasic waveforms* restore the electrode potential within the water window, preventing irreversible Faradaic reactions and reducing both electrode corrosion and

tissue necrosis [65], [70], [106].

In this study, monophasic cathodic current pulses were deliberately employed to accelerate electrode degradation. A Keithley 2602B Source Meter Unit delivered 20 mA pulses at 10 Hz (50 % duty cycle) between the tungsten and platinum electrodes until the tungsten wire fractured. The cathodic pulses caused the electrode potential to drop outside the water window, leading to hydrogen evolution and gas formation on the tungsten surface.

• Thermal aging system

The electrochemical reactions occurring on the electrode–electrolyte interface can be accelerated by elevating the temperature of the system. The temperature dependence of chemical reaction rates follows the Arrhenius law, where the rate constant increases exponentially with temperature according to $k = Ae^{-E_a/(RT)}$ [107], [108]. The thermal aging (acceleration) factor between an elevated temperature and a reference temperature can therefore be expressed as

$$\text{Aging factor} = \frac{k_{T_{\text{Accelerated}}}}{k_{T_{\text{Normal}}}} = \exp \left[\frac{E_a}{R} \left(\frac{1}{T_{\text{Normal}}} - \frac{1}{T_{\text{Accelerated}}} \right) \right] \quad (3.1)$$

where E_a is the activation energy (J mol^{-1}), R is the universal gas constant ($8.314 \text{ J mol}^{-1} \text{ K}^{-1}$), and $T_{\text{Accelerated}}$ and T_{Normal} are absolute temperatures (K) for accelerated and physiological conditions, respectively. While this model provides a physically grounded description of temperature-dependent degradation, the empirical Q_{10} rule is often used for biological and electrochemical systems as an approximation [109]. In this approach, a Q_{10} value of approximately 2 indicates that the rate of a chemical reaction doubles for every 10°C increase in temperature [109]. However, excessively high temperatures can trigger degradation mechanisms that do not occur under physiological conditions, which can reduce the reliability of accelerated aging results [109], [110].

Considering both acceleration and relevance, a temperature of 67°C was chosen in this study to achieve approximately an eightfold increase in the effective aging rate relative to physiological temperature (37°C).

The electrochemical cell, including the working, counter, and reference electrodes, was placed in a heat-resistant glass container on a hotplate stirrer. The PBS temperature was monitored using a thermometer, and the hotplate setting was adjusted to maintain 67°C. A magnetic stir bar was added to the container and operated during the stimulation period to prevent ion depletion near the electrode surface.

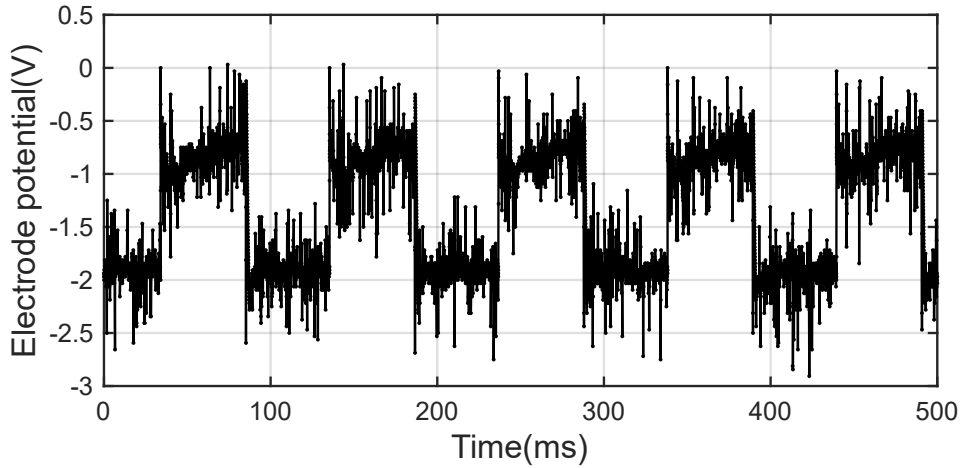
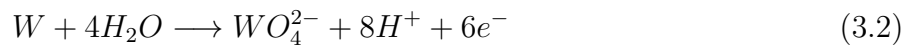


Figure 3.4: The electrode potential across the tungsten wire and Ag/AgCl reference electrode during electrical pulse stimulation, measured by an oscilloscope.

3.1.2 Results

Electrochemical reactions on tungsten (W) in PBS

The Pourbaix diagram (see Figure 3.3) from the study on tungsten corrosion in phosphate-buffered saline (PBS) [98] illustrates the potential at which faradaic reactions can occur on the tungsten surface as a function of electrolyte pH. According to the Pourbaix diagram, bare solid tungsten (W) immersed in phosphate-buffered saline (PBS, pH 7.4) can still undergo anodic dissolution depending on the applied potential, as the stability region of metallic tungsten does not fully encompass this physiological pH[98], [111]. Based on [98], [111], [112], the anodic electrochemical reaction producing soluble tungsten ions (WO_4^{2-}) is described as



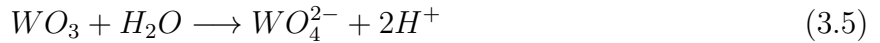
and



The main cathodic reaction is the reduction of water, which generates hydrogen gas at the electrode surface:



Tungsten can form a passive oxide layer, tungsten trioxide (WO_3), when the potential is near equilibrium (0.4 V vs. SHE or 0.195 V vs. Ag/AgCl) and the pH of the PBS is 7.4. However, this passive oxide can still dissolve following



In this study, monophasic cathodic current pulses were applied to the working electrode, causing the potential to drop below -2 V, as shown in Figure 3.4. At this potential, hydrogen evolution is expected to occur on the electrode surface, as described in Equation (3.4). The generated atomic hydrogen can also diffuse into the tungsten lattice, inducing internal stress and embrittlement of the metal structure. Such effects have been reported in tungsten exposed to hydrogen environments or under cathodic polarisation [111], [113], [114].

Visual inspection of tungsten degradation

After prolonged stimulation, the tungsten wires thinned and eventually fractured. An optical image of a new tungsten wire before immersion in PBS is shown in Figure 3.5, while Figure 3.6 presents the wire after six hours of electrical stimulation, showing erosion along the middle section that led to mechanical failure. The diameter of the wire near the fracture point decreased from $50\text{ }\mu\text{m}$ to approximately $8.78\text{ }\mu\text{m}$.

Further microscopic inspection of the tungsten surface (Figure 3.7) revealed localised flaking

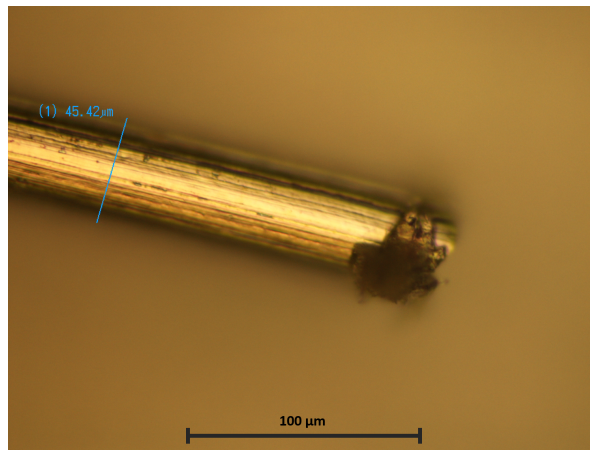


Figure 3.5: Microphotograph of a new tungsten wire electrode showing its morphology before immersion into PBS solution. The diameter of the tungsten wire is 50 μm .

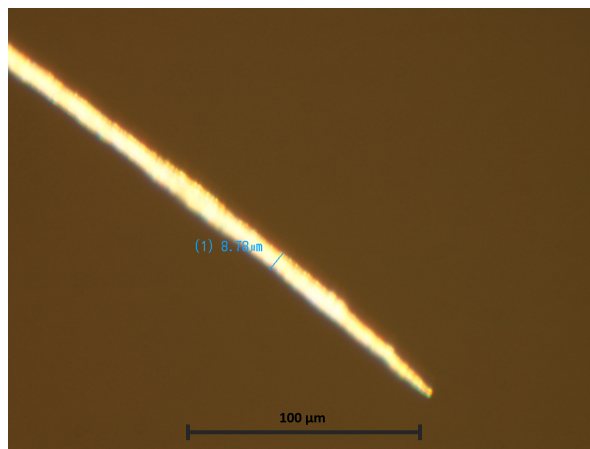


Figure 3.6: Microphotograph of the tungsten wire after six hours of electrical stimulation. The wire fractured near the middle section, where the diameter was reduced to around 8.78 μm .

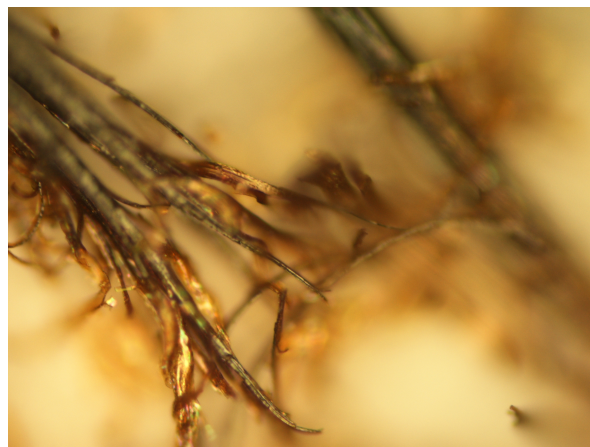


Figure 3.7: Microscopic image of the tungsten wire surface after stimulation showing flaking and delamination along the wire axis. The surface morphology indicates mechanical degradation consistent with hydrogen-induced embrittlement.

and delamination along the wire axis. This morphology suggests a mechanical mode of degradation rather than uniform electrochemical corrosion. Given the applied potential (below -2 V vs. Ag/AgCl) as shown in Figure 3.4, the formation of hydrogen bubbles and the diffusion of atomic hydrogen into the metal lattice are likely to occur. These processes can induce internal stress, promote crack propagation, and reduce ductility. Similar behaviour has been attributed to hydrogen embrittlement in tungsten and other refractory metals [111], [113], [114]. Consequently, the observed electrode failure is likely associated with hydrogen-induced mechanical degradation rather than oxidation-driven corrosion.

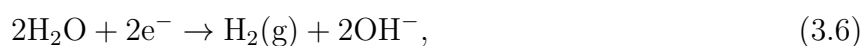
3.1.3 Electrochemical Impedance Spectroscopy

The electrode impedance spectroscopy was measured hourly, and the averaged impedance results from three trials are shown in Figure 3.8. When the PBS temperature elevated from 25°C (room temperature) to 67°C , the electrode impedance spectrum of all frequencies decreased.

In addition, from Figure 3.8, the normalised impedance results of impedance at each hour show that the impedance at a low frequency between 10 Hz-1 kHz have a slight increasing trend after the third hour of the stimulation. After the wires were broken down, the EIS results increased by approximately one magnitude across all frequency spectra.

3.1.4 Discussion

The tungsten electrode was subjected to continuous cathodic stimulation under accelerated conditions at 67°C . At the applied potential of approximately -2 V vs. Ag/AgCl, the electrode operates well within the hydrogen evolution region of the water stability window. Under these strongly reducing conditions, water is reduced to hydrogen gas according to



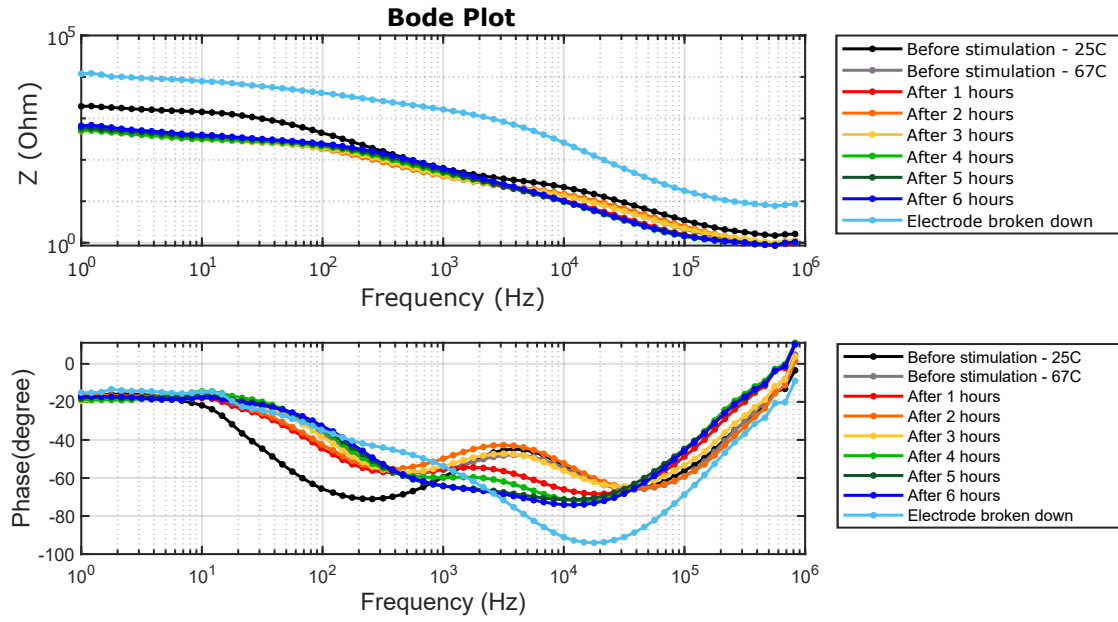


Figure 3.8: The averaged EIS across trials of the tungsten wire.

and atomic hydrogen generated at the electrode surface can adsorb and diffuse into the tungsten lattice. This process induces internal stress and mechanical weakening through hydrogen embrittlement, a mechanism well documented in tungsten and other refractory metals [111], [113], [114], [115]. The applied potential also promotes partial dissolution and redeposition of surface oxides, continuously altering the electrode–electrolyte interface.

Although these experimental conditions are more extreme than those found *in vivo*, they deliberately accelerate the electrochemical reactions responsible for surface modification, allowing degradation to be observed within hours. The hydrogen evolution and surface thinning occurring here are mechanistically similar to electrochemical etching processes used for tungsten-tip fabrication [116], where hydrogen bubble formation and localised dissolution at the meniscus cause necking and detachment of wire segments. In this study, a comparable morphology of surface flaking and delamination (Figure 3.7) confirms that the dominant degradation mechanism is hydrogen-induced rather than oxidation-driven corrosion.

The impedance spectra shown in Figures 3.8 and 3.9 reveal how these electrochemical and morphological changes manifest electrically. Each trial represents an independent tungsten wire sample tested under identical conditions, and consistent impedance trends were observed across

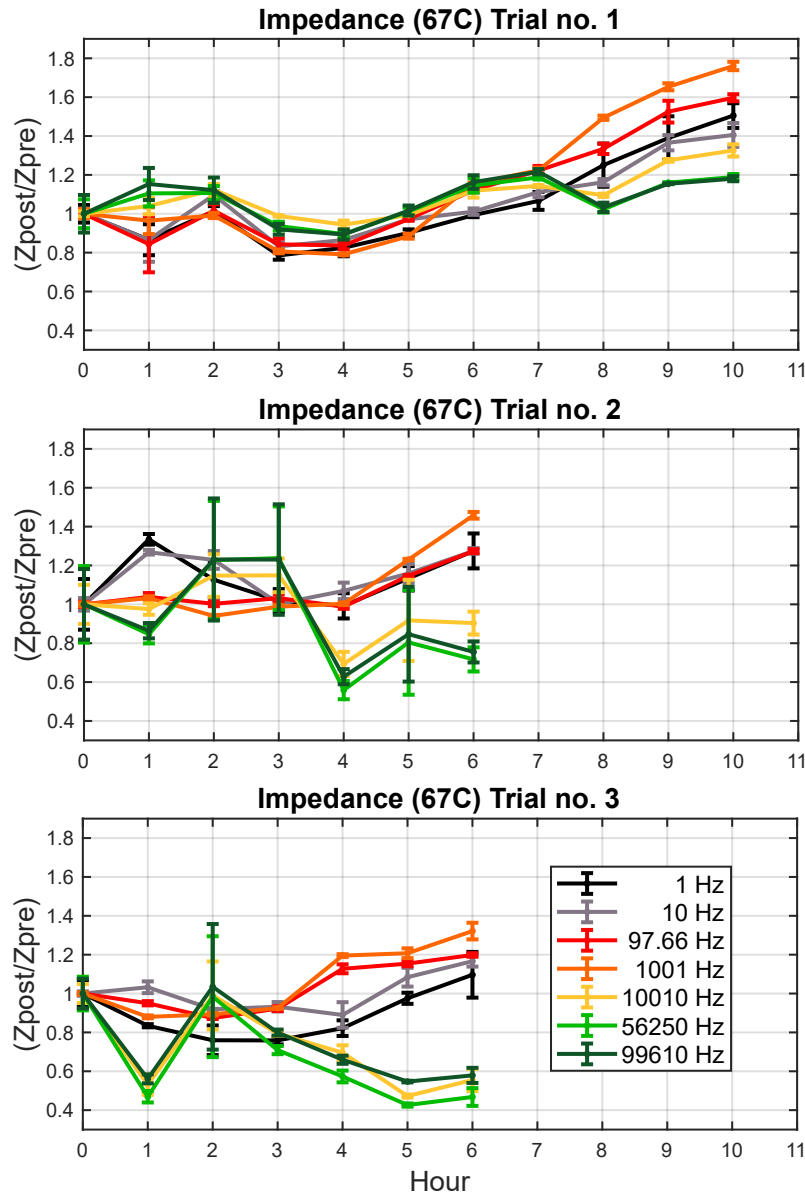


Figure 3.9: The normalised impedance as a function of stimulation time of three trials plotted with standard deviations

all three trials. During the initial stimulation period, the impedance magnitude decreased and the phase angle became more negative (approaching -70°), indicating an increase in interfacial capacitance (C_{dl}) due to surface activation and oxide reduction [65], [117]. As stimulation continued, the impedance at low frequencies (1–100 Hz) gradually increased and the phase shifted toward 0° , signifying a transition from capacitive to resistive behaviour. This trend corresponds to a decrease in C_{dl} and an increase in charge-transfer resistance (R_{ct}), caused by surface cracking, delamination, and partial isolation of the metal from the electrolyte [118], [119], [120]. The final spectrum obtained after electrode breakdown exhibited a steep impedance

rise across all frequencies, confirming loss of electrochemical contact.

The evolution of C_{dl} and R_{ct} explains the observed impedance trajectory: an early decrease followed by a progressive increase. Initially, oxide removal enlarges the active area, raising C_{dl} and lowering R_{ct} . Subsequent mechanical damage and hydrogen-induced delamination reduce the effective contact area and impede charge transfer, yielding higher overall impedance [121]. These results demonstrate that impedance spectroscopy can sensitively detect progressive surface deterioration of tungsten electrodes under accelerated conditions.

Although the observed mechanism (hydrogen-driven flaking) does not fully represent the complex, multi-factor degradation that occurs *in vivo*, the reproducible impedance variations provide a practical platform for validating impedance-measurement systems designed to monitor electrode health. Future improvements to the accelerated protocol could enhance physiological relevance: lowering the stimulation amplitude to clinically realistic levels, extending the test duration, and including oxidative agents such as hydrogen peroxide could promote slower, mixed corrosion–oxidation pathways more representative of chronic implantation. Such refinements would bridge the gap between high-stress accelerated tests and realistic *in vivo* conditions, while retaining the benefit of rapid, measurable impedance feedback for system validation.

3.2 Automated platform for bench-top and developmental impedance measurements

The accelerated testing was designed in the previous part; however, to repeat and perform several trials, an automatic platform must be used to operate the testing effectively. Also, the EIS must be measured every hour for both bench-top electrochemical workstations and developmental impedance measurement devices, which will be designed in the future. Therefore, the automatic platform for operating the standard bench-top electrochemical workstation concurrently with a developmental impedance measurement device was designed and implemented in this second part of the chapter.

3.2.1 Overall system diagram

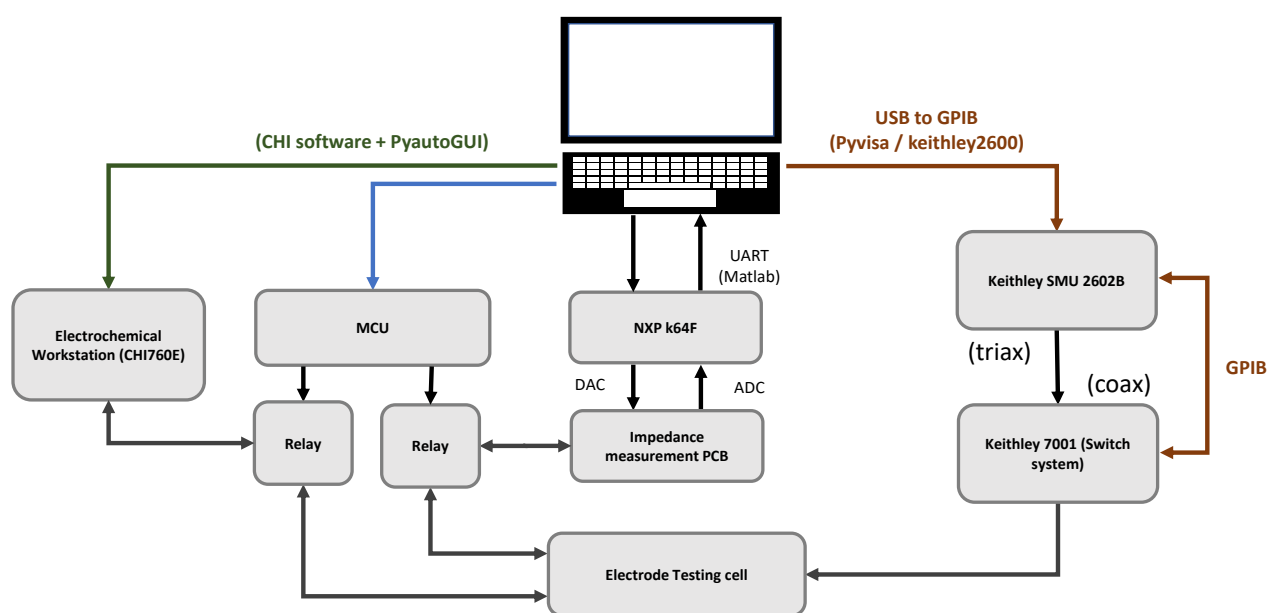


Figure 3.10: Block diagram of the automated platform integrating the electrochemical workstation with the developmental impedance measurement device.

The electrochemical workstation or CHI760E software was installed on the computer, and the

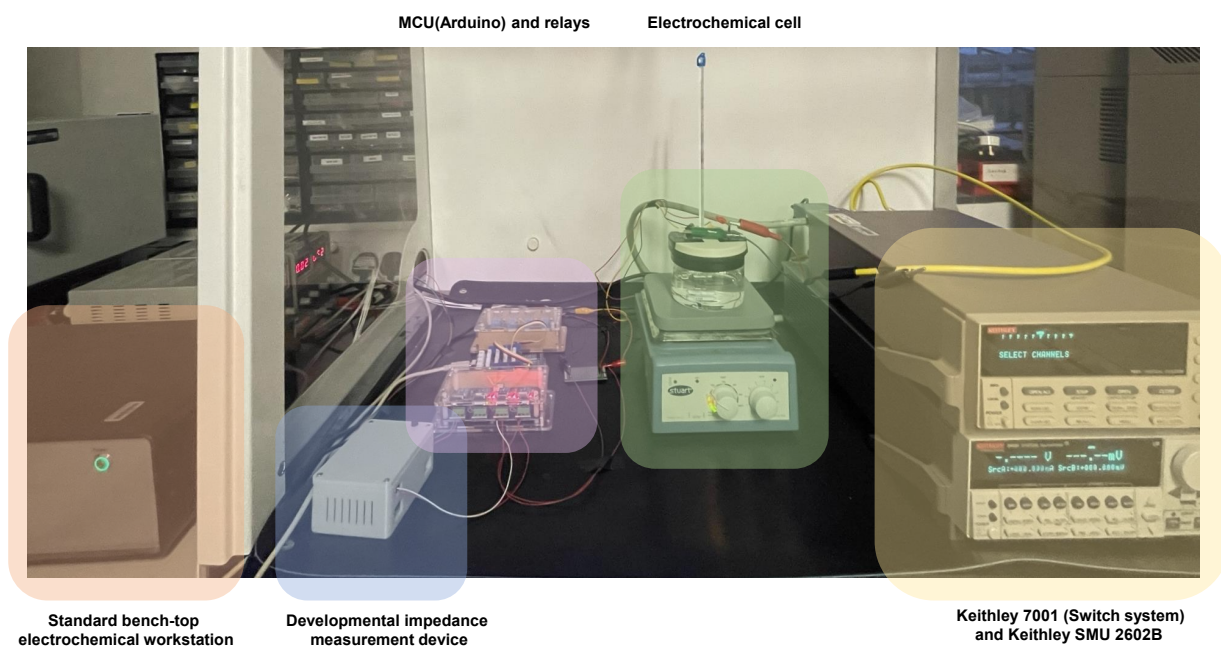


Figure 3.11: Experimental setup of the automated platform combining the electrochemical workstation and impedance measurement device.

GUI was controlled automatically with Python script using the PyautoGUI package. After every hour of stimulation, the Python script was run to switch off the relay to connect the electrochemical workstation to the electrochemical cell, preparing for the EIS measurement period. Afterwards, the CHI 760E software was run automatically to start the measurement three times, and all data was saved into the computer.

On the stimulation part, Keithley SMU 2602b was connected to Keithley 7001 (Switch system) with a GPIB port, and both were connected to the computer with a USB to GPIB cable. The Keithley was controlled through the computer using Pyvisa and keithley2600 packages. The switch in Keithley 7001 was closed to connect the stimulator to the electrochemical cell when the stimulation started and then opened to disconnect after every hour of current pulse stimulation.

3.2.2 Results

The electrode wire failed after approximately six hours of stimulation. The corresponding impedance spectra obtained from the automated impedance measurement system are presented in Figure 3.11, while a micrograph of the electrode near the fracture point is shown in Figure 3.13. Additionally, the EIS data acquired using the electrochemical workstation are illustrated in Figure 3.12.

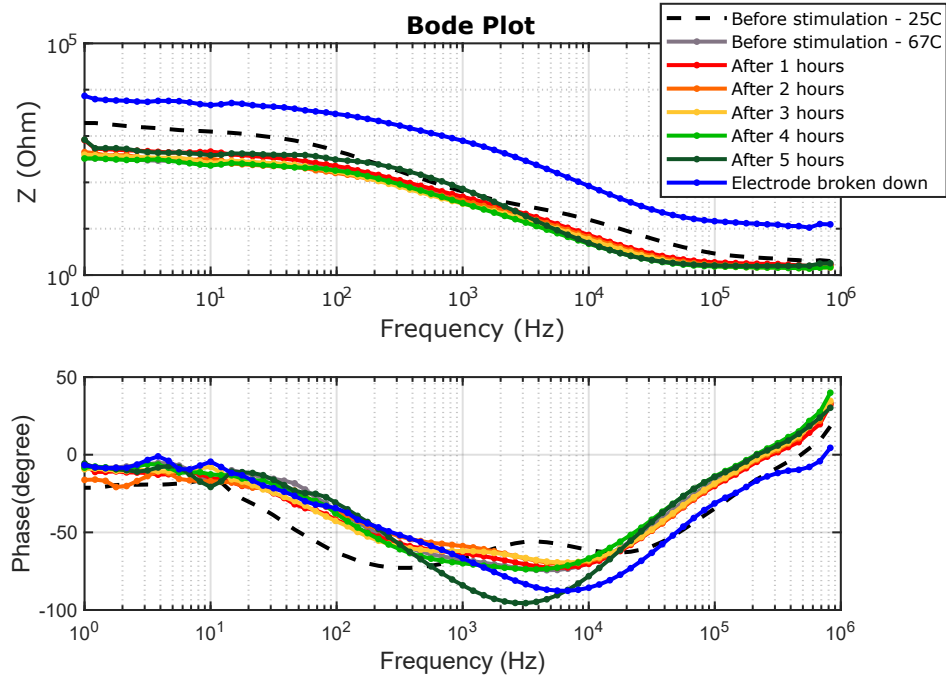


Figure 3.12: EIS data of electrode in the automatic platform over time

The platform can automatically accelerate electrode degradation. The microphotograph shows results that are similar to those of the manual setup in the first part of the chapter. Furthermore, the automatic platform can switch between bench-top measurement and another custom bench-top platform for electrode impedance characterisation.

3.3 Conclusion

This chapter focuses on demonstrating that electrical stimulation can accelerate electrode degradation, as characterised by electrochemical impedance spectroscopy (EIS) and microstructural

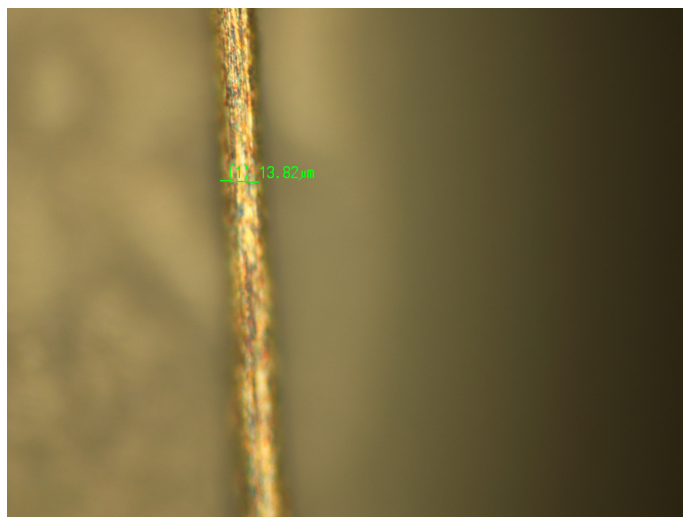


Figure 3.13: Microphotograph of electrode breakdown with the automatic platform. The electrode diameter close to the cutting point is around $13.82\text{ }\mu\text{m}$

changes observed under microscopy. In addition, temperature elevation is discussed based on theoretical considerations and supporting literature to explain its role in accelerating electrochemical reactions. In the following chapter, the impedance results obtained from the standard bench-top electrochemical workstation will be compared with those from the custom-built impedance measurement platform for electrode characterisation.

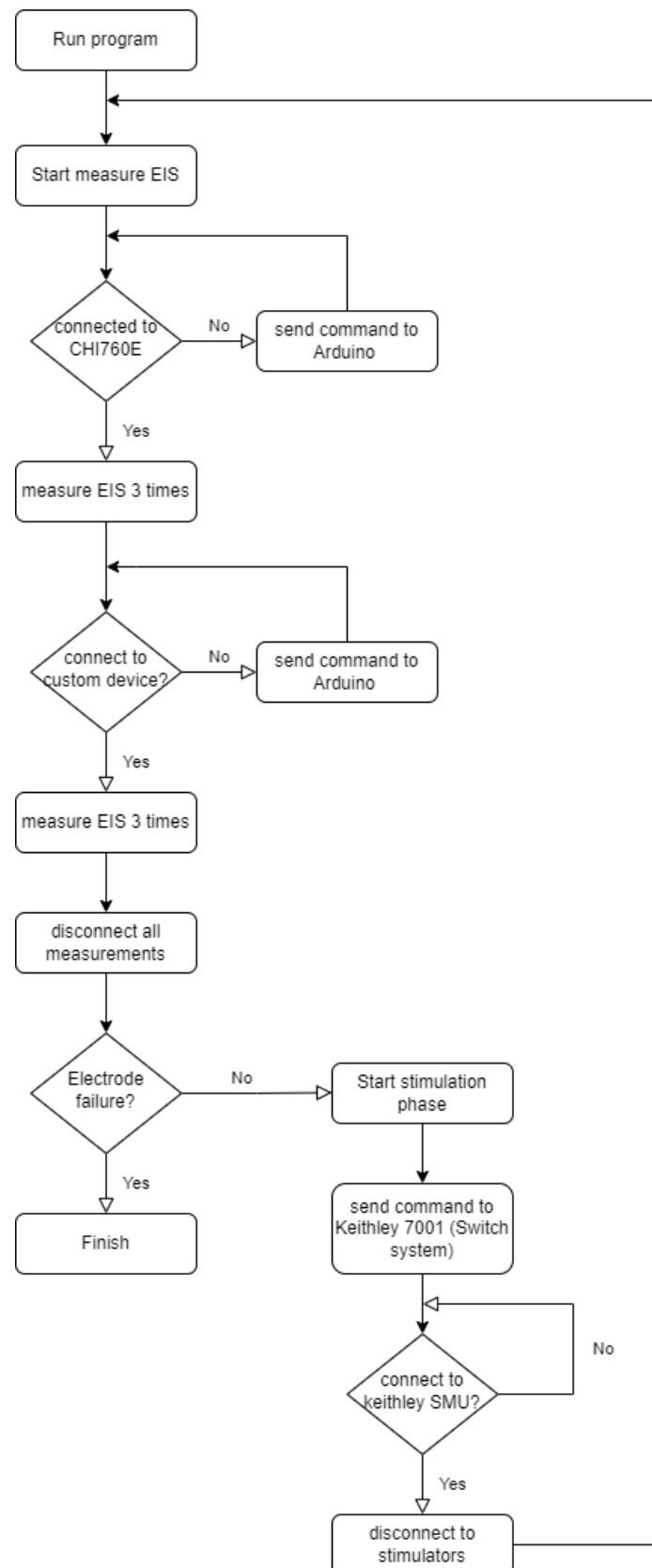


Figure 3.14: Flowchart for the operation of the automated platform.

Chapter 4

Custom bench-top platform for electrode impedance characterisation

Electrochemical impedance spectroscopy (EIS) is commonly performed using either potentiostatic or galvanostatic methods. Both approaches are theoretically equivalent and are chosen based on the specific application and impedance range [82]. While voltage-controlled waveforms are electronically simpler to generate, they may not always ensure safety. The delivered charge can vary due to the interaction between the electrode and the surrounding tissue [123], potentially leading to unpredictable results. In extreme cases, excessive charge delivery may cause tissue damage. As a result, voltage-controlled bio-interfacing is generally regarded as less safe since the current injection is not controlled when the load varies [124]. To address this issue, a galvanostatic mode has been implemented on the PCB. This mode measures the AC voltage response resulting from a constant AC current injection. For safety, the injected current is maintained at a constant amplitude of $10\ \mu\text{A}$ [125].

Portions of the research presented in this chapter have been published in V. Manatchinapisit and T. G. Constantinou, "A Portable and Low-cost Electrochemical Impedance Spectroscopy Platform for the Characterisation of Implantable Electrodes," in *Proc. IEEE EMBC*, Orlando, FL, USA, 2024, pp. 1-5 [122].

Table 4.1: Design requirements and specifications of the custom bench-top impedance measurement platform.

Specification	Value	Unit
Measurement Method	Galvanostatic (AC current injection)	–
Impedance Extraction Method	FFT-based analysis	–
Frequency Range	48 – 100 k	Hz
Amplitude of Injected Current	10	μA
Impedance Measurement Range	100 – 1M	Ω
Accuracy (compared with CHI760E)	≤ 5	%
Power Supply	± 5	V
Data Interface	USB / UART	–
PCB Dimensions	8.2×5.4	cm

4.1 The PCB design for the custom bench-top platform

A system block diagram, as shown in Figure 4.2, illustrates the design, which comprises three main components:

- **Front-End Instrumentation:** This includes a voltage-controlled current source to generate the stimulation signal and an instrumentation amplifier to measure the voltage across the electrodes.
- **Embedded Platform:** Built around a microcontroller (MCU), it controls the waveform generator or digital-to-analogue converter (DAC), the analogue-to-digital converter (ADC), and pre-processes the acquired data.
- **Computer Interface:** Used to calculate and display the electrochemical impedance spectrum.

The sinusoidal signal, generated by the waveform generator, is first converted into a current source. This sinusoidal current is injected into the working electrode and returned through the counter electrode. The voltage across the electrode pair is amplified by the instrumentation amplifier and converted into a digital signal. Simultaneously, the injected current is monitored by measuring the voltage across R_{Isense} , which is $1\text{k}\Omega$. The resulting waveform is processed using the Fast Fourier Transform (FFT) method to compute the impedance magnitude and phase shift at various frequencies of interest.

The PCB is engineered to include essential components such as a high-pass filter, a voltage-controlled current source (VCCS), instrumentation amplifiers, and programmable amplifiers. Control of the PCB is managed by a microcontroller unit (MCU), specifically the NXP FRDM-K64F. A digital-to-analogue converter (DAC) generates a sinusoidal waveform, which is then passed through a high-pass filter formed by R_1 and C_1 , with a cutoff frequency of 1.592 Hz, to remove the DC offset. Subsequently, the sinusoidal signal is converted from voltage to current using the VCCS, as illustrated in Figure 4.1.

High-speed operational amplifiers (ADA4807) by Analog Devices are employed in the VCCS, achieving a simulated current source bandwidth of approximately 1.6 MHz. A differential amplifier is incorporated in the feedback loop of the input amplifier to stabilise the voltage across resistor R_s , ensuring it corresponds to the input voltage [126]. Consequently, the system maintains a constant output current, determined solely by the input voltage and the value of $R_s = 100\text{ k}\Omega$. The injected current amplitude is fixed at $10\text{ }\mu\text{A}$.

The output current is directed into the electrode under evaluation, with the return current handled by a voltage buffer. This buffer uses a zero-drift operational amplifier (ADA4522) to provide a low-impedance current path and enable bias voltage adjustments. Concurrently, the voltage across the R_{Isense} ($1\text{ k}\Omega$) and the electrode-electrolyte interface is measured and amplified using instrumentation amplifiers. The resulting signal is then passed through an active low-pass filter with a cutoff frequency of 320 kHz, amplified by programmable inverting amplifiers, and digitised via the ADC on the MCU. The PCB design is shown in Figure 4.3, which demonstrates the board stacked onto the FRDM-K64F MCU. The board dimensions are $8.2 \times 5.4\text{ cm}$.

4.1.1 Microcontroller (MCU)

The FRDMK64F development board manufactured by NXP was selected to control the PCB board. The FRDM-K64F has a maximum operating frequency of 120 MHz, Direct Memory Access(DMA), 16-bit ADCs, and 12-bit DAC. DMA can transfer data from or to memory to

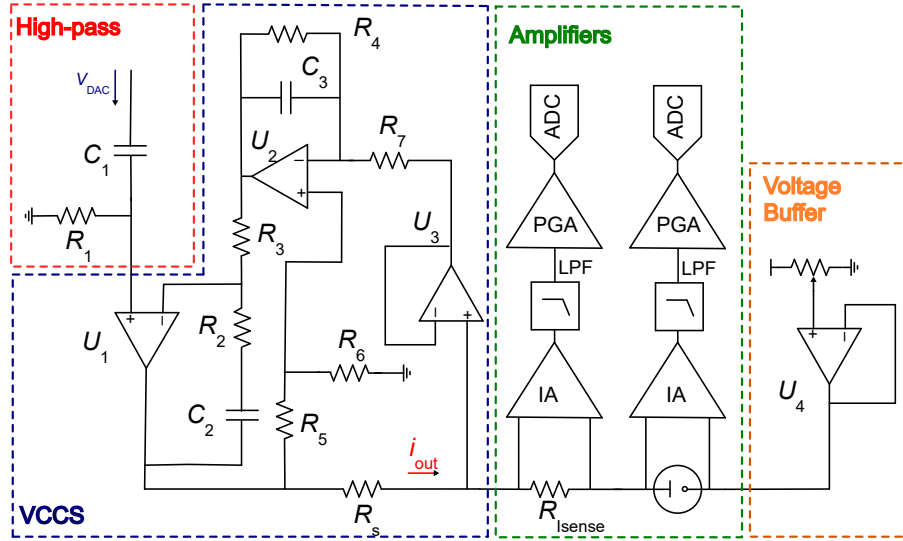


Figure 4.1: The PCB-based Impedance measurement board consists of a high-pass filter, Voltage-controlled current source (VCCS), Instrumentation amplifiers (IA), low-pass filter(LPF), programmable gain amplifiers(PGA), and voltage buffer. The values of each component are shown in Table 4.2

DAC for generating sinusoidal waveform at each frequency; also, DMA can transfer the data from ADC back to the buffer array waiting to send through a serial port to the computer.

4.1.2 Signal generation or DAC

A sinusoidal signal was generated using the integrated 12-bit DAC of the FRDM-K64F microcontroller. The DAC produced waveforms swept from 48 Hz to 100 kHz, with 16,384 samples per measurement cycle. Both the DAC and ADC operated at a sampling rate of 786,432 samples/s under Direct Memory Access (DMA) control. This sampling rate represents the maximum

Table 4.2: The component values for the impedance measurement board.

Component	Value	Component	Value
R1	10 k	C1	10 μ f
R2	100	C2	10 pf
R3	1 k	C3	5 pf
R4	1 k	U1, U2	ADA4807
R5	10 k	U3	ADA4522
R6	10 k	U4	ADA4522
R7	1 k	INA	AD8429
R _s	100 k	PGA	LTC6910
R _I sense	1 k	LPF	ADA4099

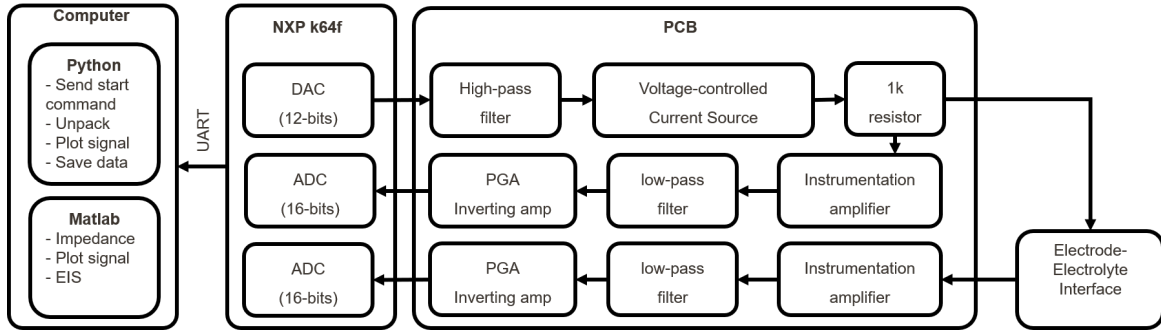


Figure 4.2: System diagram of the custom impedance measurement platform integrating the microcontroller, signal-conditioning circuits, and electrode–electrolyte interface.

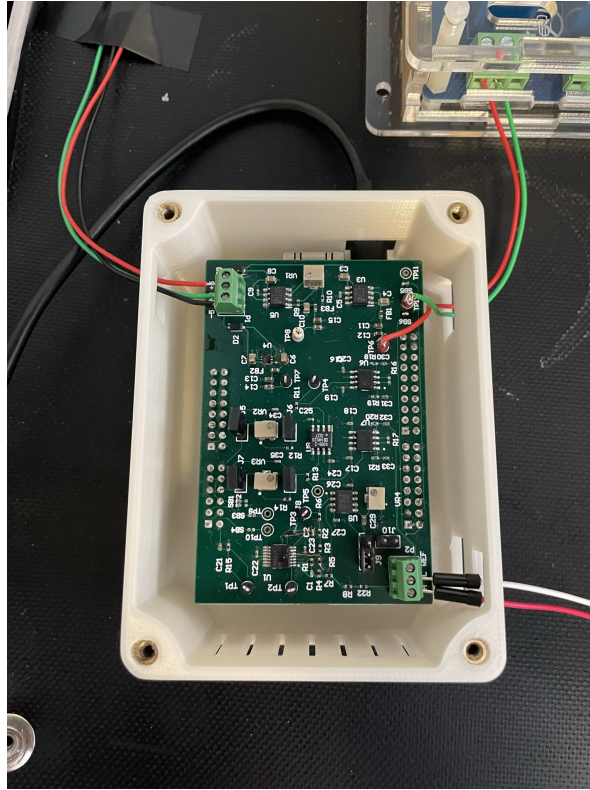


Figure 4.3: Assembled PCB inside the 3D-printed case

achievable value on the FRDM-K64F platform and, when divided by 16,384 samples, yields one full sinusoidal cycle at 48 Hz, which corresponds to the lowest frequency used in the measurement sweep.

Upon receiving a trigger, the Direct Memory Access (DMA) controller continuously streamed pre-computed waveform data to the DAC, ensuring uninterrupted signal generation with minimal processor overhead. The DAC output, with an amplitude of approximately 1 V, was subsequently passed through a high-pass filter composed of R_1 and C_1 to remove any DC offset

before being applied to the voltage-controlled current source (VCCS).

The choice of using the MCU's integrated DAC, rather than an external device, was motivated by several considerations. The 12-bit resolution was sufficient to produce low-distortion signals across the required frequency range, and the use of DMA enabled reliable streaming at the system reference clock, which also provided synchronisation with the ADC. This ensured that waveform generation and signal acquisition shared a common timing reference, improving measurement accuracy. Furthermore, integration of the DAC on the same device reduced component count, board area, and overall cost, while still allowing the flexibility to generate arbitrary or multi-sine waveforms when required.

The main trade-off of this approach was the limited output amplitude of around 1 V. However, this was acceptable because the VCCS converted the DAC voltage into a controlled current suitable for electrode excitation. Although external DACs could have provided a wider voltage range and potentially lower distortion, these benefits were outweighed by the additional cost and increased design complexity they would have introduced.

4.1.3 Voltage-Controlled Current Source

A voltage-controlled current source (VCCS) was implemented to generate precise microampere-level currents for electrode stimulation and impedance measurement. Several circuit topologies were considered. The buffered Improved Howland current pump (IHCP) preserves the low-component count of the classical Howland design while employing unity-gain buffers to isolate the resistor network from the load, thereby improving stability and output impedance. However, its transconductance accuracy and effective output resistance remain strongly dependent on resistor-ratio matching within the bridge; even small mismatches directly introduce current error and reduce output resistance [127], [128]. When applied to electrode-like loads (i.e. high-impedance with appreciable capacitance), the buffered IHCP typically requires resistor tolerances of $\leq 0.1\%$ (preferably 0.05–0.01%), careful printed circuit board layout, and in some cases additional output compensation to preserve phase margin [129], [130]. Voltage compliance

is further limited by the output swing of the op-amp and any headroom consumed by the buffer stages.

In comparison, a three-op-amp differential-sensing VCCS was selected for this design. In this configuration, the output current is defined directly through the sense resistor R_s , with the control loop driving the outputs such that the measured drop across R_s equals the input command voltage. The resulting load current is therefore determined by

$$I_{\text{out}} = \frac{V_{\text{dac}}}{R_s}.$$

This approach reduces sensitivity to resistor-ratio errors, improves tolerance to capacitive loading, and achieves high effective output impedance by actively driving both load terminals. Both IHCP and VCCS architectures support bidirectional operation under dual supplies, but the three-op-amp implementation shares compliance between two drivers, necessitating careful choice of rail-to-rail input/output (RRIO) amplifiers and appropriate headroom budgeting.

For the present design, the operational amplifiers were required to provide RRIO capability, wide input common-mode range, low offset and bias current for microampere-level accuracy, and sufficient bandwidth and noise performance to ensure stability with capacitive electrode loads. Several candidate devices from Analog Devices and Texas Instruments were evaluated, as summarised in Table 4.3. The ADA4807 was selected for the driver stages due to its high gain–bandwidth product (180 MHz), low input-referred noise density ($\sim 3 \text{ nV}/\sqrt{\text{Hz}}$), and fast slew rate ($225 \text{ V}/\mu\text{s}$), together with its ability to swing close to the supply rails at $\pm 5 \text{ V}$. For the precision sense/buffer stage, the ADA4522-2 was chosen, as its zero-drift architecture provides ultralow input offset ($< 5 \text{ }\mu\text{V}$) and minimal drift ($< 0.015 \text{ }\mu\text{V}/^\circ\text{C}$), thereby ensuring accurate regulation through the sense resistor. Other candidates (OPA2156, OPA1656, OPA1678, ADA4625-2, OPA2188) remain viable alternatives, each offering a different trade-off between bandwidth, precision, and availability.

Table 4.3: Candidate operational amplifiers evaluated for the ± 5 V VCCS implementation.

Parameter	ADA4807	ADA4522	OPA2156	OPA1656	OPA1678	ADA4625	OPA2188
Supply range (V)	± 5	± 2.25 – 27.5	± 2.25 – 18	± 2.25 – 18	± 2.25 – 18	± 2.25 – 18	± 2.25 – 18
V_{OS} (typ.)	0.4 mV	5 μ V	20 μ V	150 μ V	150 μ V	30 μ V	25 μ V
I_B (typ.)	100 nA	50 pA	20 pA	10 pA	2 pA	1 pA	45 pA
GBW (MHz)	180	3	45	56	36	19	2
Noise e_n (nV/ $\sqrt{\text{Hz}}$)	3.1	5.8	5.2	2.9	4.5	3.0	10
Slew rate (V/ μ s)	225	2.7	20	20	12	20	0.8

The final VCCS design, based on the topology in [122], [131], employs a fixed $R_s = 100 \text{ k}\Omega$ resistor for voltage-to-current conversion. The operational amplifier A_1 operates in a negative feedback configuration, with the differential amplifier A_2 in the feedback path, forming a closed-loop system. Negative feedback ensures that the voltage at A_1 's inverting input matches its non-inverting input due to the virtual ground properties of the op-amp. A_2 , configured as a buffered differential amplifier, stabilises the voltage across R_s , maintaining a constant output current proportional to the input voltage. The third amplifier, A_3 , acts as a buffer to provide high-impedance isolation, ensuring the circuit can drive the load effectively without disturbing loop stability.

For example, with $R_s = 100 \text{ k}\Omega$ and $V_{in} = 500 \text{ mV}$, the output current is

$$I_{out} = \frac{500 \text{ mV}}{100 \text{ k}\Omega} = 5 \mu\text{A}.$$

This configuration allows current modulation in the range of 0–10 μA using a sinusoidal input from the DAC as V_{in} . The output current is first delivered to a known resistor $R_{Isense} = 1 \text{ k}\Omega$ for calibration before being injected into the electrode. The return current is handled by the ADA4522 zero-drift amplifier, which provides a low-impedance return path and enables bias voltage adjustment, ultimately sinking the current back into the virtual ground and completing the circuit.

4.1.4 Instrumentation Amplifier and Programmable Gain Stage

The voltage across the electrode–electrolyte interface and the sensing resistor $R_{\text{Isense}} = 1 \text{ k}\Omega$ was measured using an instrumentation amplifier. This architecture was chosen because it provides high common-mode rejection and high input impedance, ensuring that small differential signals could be extracted reliably without loading the electrodes or being corrupted by environmental interference. Compared with discrete differential op-amp stages, an instrumentation amplifier also minimises mismatch errors and offers superior noise immunity, making it well suited for bioelectrical measurements.

In this design, the AD8429 was selected due to its ultra-low input-referred noise density of $1 \text{ nV}/\sqrt{\text{Hz}}$, high CMRR ($> 120 \text{ dB}$), and low input offset voltage ($50 \mu\text{V}$ max). These specifications enabled accurate and stable measurement across the 48 Hz – 100 kHz frequency range. The amplified signal was subsequently passed through an active low-pass filter with a cutoff frequency of 320 kHz to suppress high-frequency noise before digitisation. The op-amp employed in this filter stage (ADA4099) was chosen not only for its low-noise and precision characteristics but also for its proven stability. It is internally compensated and unity-gain stable, with reported phase margins of approximately 47° at 5 V and 57° at $\pm 15 \text{ V}$ supply. Step-response measurements demonstrate well-damped behaviour without excessive overshoot, and the device can reliably drive capacitive loads up to 100 pF . These properties ensured robust and distortion-free filter performance over the required operating bandwidth.

To accommodate electrodes with a wide range of impedances, the signal was then processed by a programmable inverting amplifier (LTC6910 PGA), offering selectable gains of $\times 1$, $\times 10$, $\times 20$, and $\times 50$. This flexible gain control allowed the measurement dynamic range to be adjusted without bulky mechanical switches or relays. Although limited to four discrete gain steps, this solution provided a practical balance between measurement flexibility, compactness, and ease of integration.

4.1.5 ADC

The NXP FRDM-K64F microcontroller was employed to coordinate the overall operation of the system, including waveform generation, amplifier control, and data acquisition. This device was selected as it integrates a 16-bit ADC alongside a 12-bit DAC and Direct Memory Access (DMA) controller, enabling both stimulus generation and response digitisation on a single platform. The on-chip ADC digitised the measured signals with sufficient resolution and sampling rate to capture the frequency response of the electrode impedance. Using the DMA to transfer waveform data to the DAC ensured deterministic and low-latency signal generation, while the ADC simultaneously acquired voltage responses without processor bottlenecks.

The digitised data were transmitted to a computer via UART, where Fast Fourier Transform (FFT) analysis was performed to compute impedance magnitude and phase across the 48 Hz–100 kHz frequency range. The use of the FRDM-K64F therefore provided a compact, cost-effective, and well-supported microcontroller solution that simplified hardware design, reduced external component count, and ensured tight synchronisation between stimulus delivery and signal acquisition.

4.1.6 Power Supply

Low-dropout (LDO) regulators were employed to generate the required ± 5 V supply rails for the PCB. These regulators were chosen over switching converters due to their superior noise performance and high power supply rejection ratio (PSRR), both of which are critical for preserving the integrity of sensitive analogue measurements. The ADP7142 and ADP7182 were selected to provide the positive and negative rails, respectively, offering low output noise, fast transient response, and excellent line/load regulation. In addition, 0.1 μ F ceramic capacitors were placed close to each IC for local decoupling, thereby suppressing high-frequency supply ripple and minimising coupling between analogue and digital domains.

The primary requirement of the supply stage was to ensure stable and low-noise analogue and digital rails across the system. Although LDOs are inherently less power-efficient than switch-

ing regulators, their superior PSRR and low-noise characteristics were prioritised to achieve accurate impedance measurements. This represented a deliberate trade-off, favouring reliable analogue performance and measurement fidelity over efficiency.

4.1.7 Software

The FRDM-K64F development board controls the PCB and facilitates the generation of sinusoidal waveforms by utilizing Direct Memory Access (DMA) to transfer data from a Lookup Table (LUT) to the onboard DAC. Simultaneously, the 16-bit ADCs digitize the voltage across the resistor and electrode. This hardware functionality underpins the software process, ensuring efficient data transfer and precise impedance measurement.

The software process begins with the device powering on, initializing the FRDM-K64F board and activating the DAC and ADC's PIT timer. Upon receiving a trigger, such as a button press or a high input pin, the microcontroller initiates the measurement protocol. The DMA transfers sinusoidal waveform data from the LUT to the DAC, dynamically adjusting as the frequency is swept. Simultaneously, ADC data is collected and transferred into buffer arrays (16,384 samples per frequency) via DMA. This data, along with a header, is packed and transmitted to the computer through UART communication. A white LED signals data transmission, turning off once the transfer is complete. The system then progresses to the next frequency within the range of 48 Hz to 100 kHz.

On the computer, MATLAB processes the transmitted data received via the UART interface. It unpacks the data, extracting details such as frequency, ADC values, and sample counts, and stores it for further processing. The impedance is calculated based on the received data and visualized as Electrochemical Impedance Spectroscopy (EIS) plots, covering the frequency range from 48 Hz to 100 kHz.

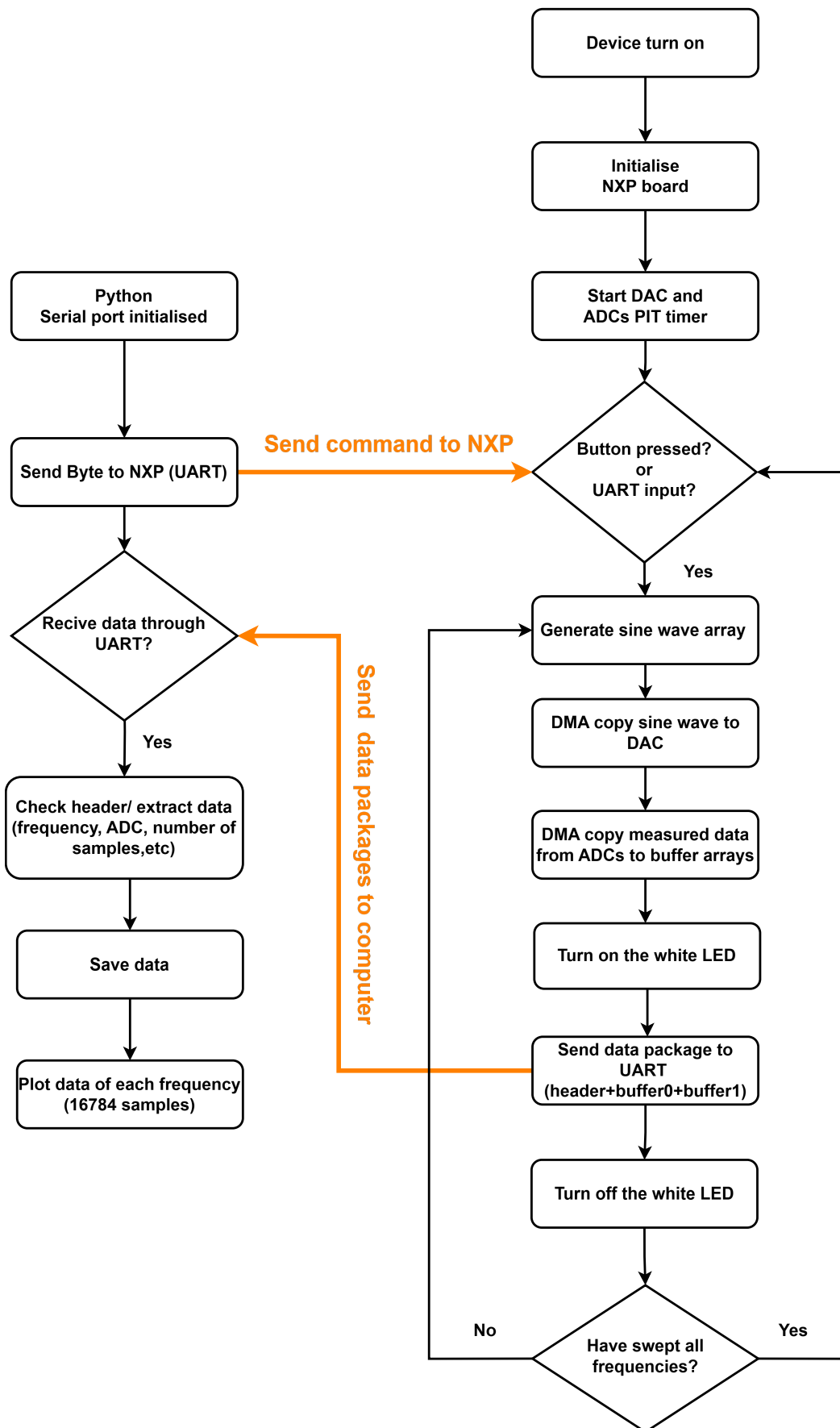


Figure 4.4: Flowchart for the operation of custom PCB impedance measurement.

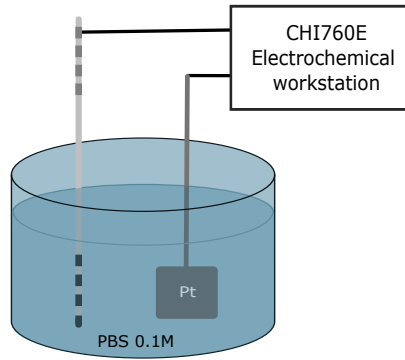


Figure 4.5: DBS electrode and Pt sheet in PBS solution connected to electrochemical workstation

4.2 Validation with implantable neural electrodes

Experiment Setup

The experimental validation was conducted using a Medtronic Model 3389 deep brain stimulation (DBS) electrode. This electrode features a polyurethane protective coating and four platinum-iridium contacts, each measuring 1.5 mm in length and 1.27 mm in diameter, with a 0.5 mm spacing between adjacent contacts. The electrode was immersed in a 0.01 M phosphate-buffered saline (PBS) solution at room temperature. The outermost contact served as the working electrode, while a platinum sheet (25 mm $\times$ 25 mm) acted as the counter electrode. The reference terminal of a CHI760E electrochemical workstation was connected to the counter electrode, forming a two-electrode configuration, as shown in Figure 4.5.

Electrochemical impedance spectroscopy (EIS) measurements were performed using the CHI760E instrument in galvanostatic and potentiostatic modes. For potentiostatic mode, the frequency range spanned 10 Hz to 1 MHz with a 10 mV voltage amplitude, while for galvanostatic mode, the frequency range was limited to 10 Hz to 10 kHz due to system constraints. Additionally, a custom PCB-based impedance measurement device was used to measure impedance across the frequency range of 48 Hz to 100 kHz.

To enable direct comparison between the impedance spectra acquired from the commercial potentiostat and the custom PCB-based measurement system, the data were resampled on a

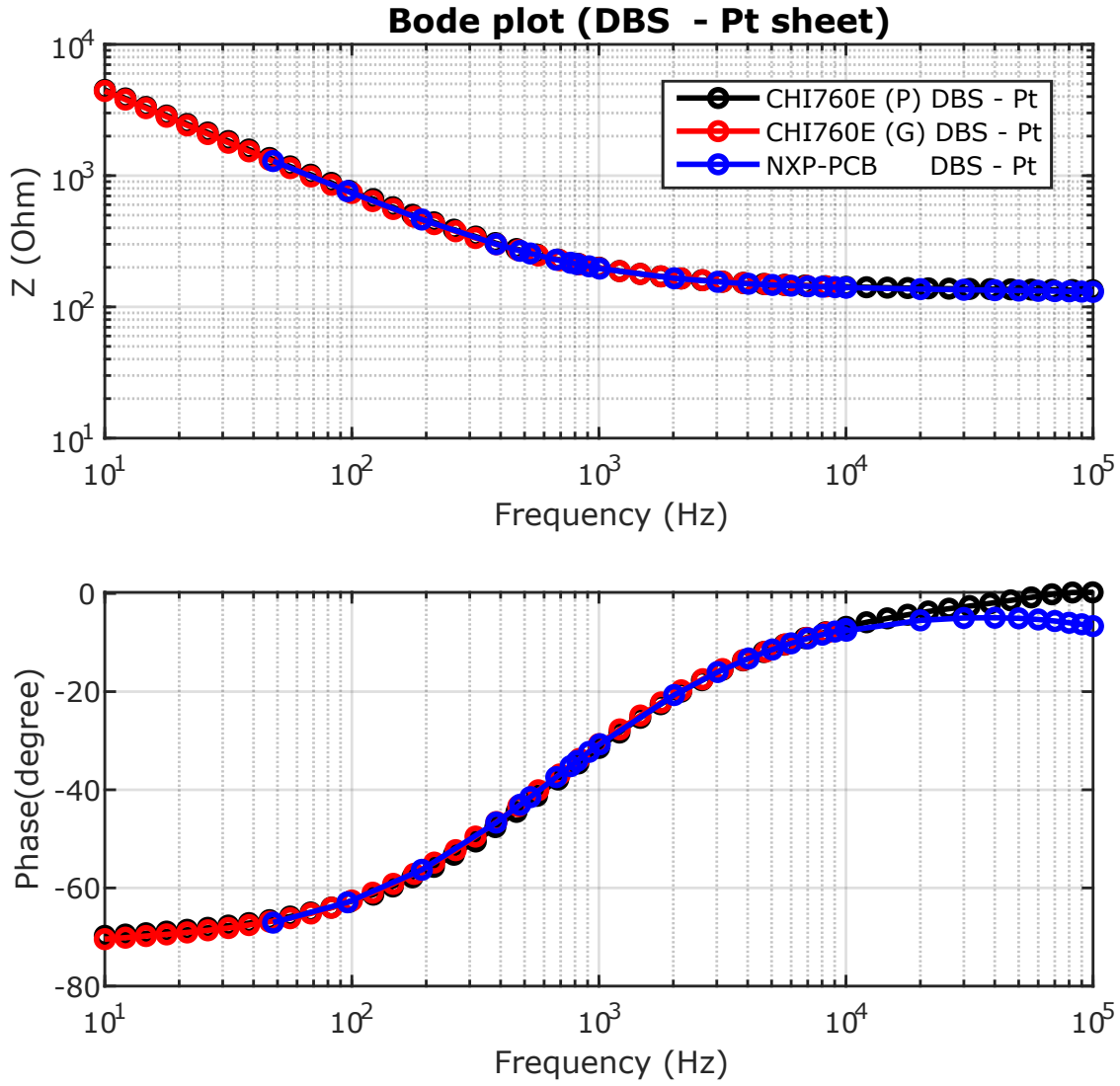


Figure 4.6: Comparison graph between EIS measuring by CHI760E and Impedance measurement PCB

common frequency grid. Since the two systems recorded at slightly different frequency points, the impedance magnitude and phase values were interpolated using linear interpolation over a logarithmically spaced frequency range from 48 Hz to 100 kHz. This procedure ensured that both datasets were aligned at identical frequencies, allowing point-wise calculation of absolute and percentage errors across the entire spectrum.

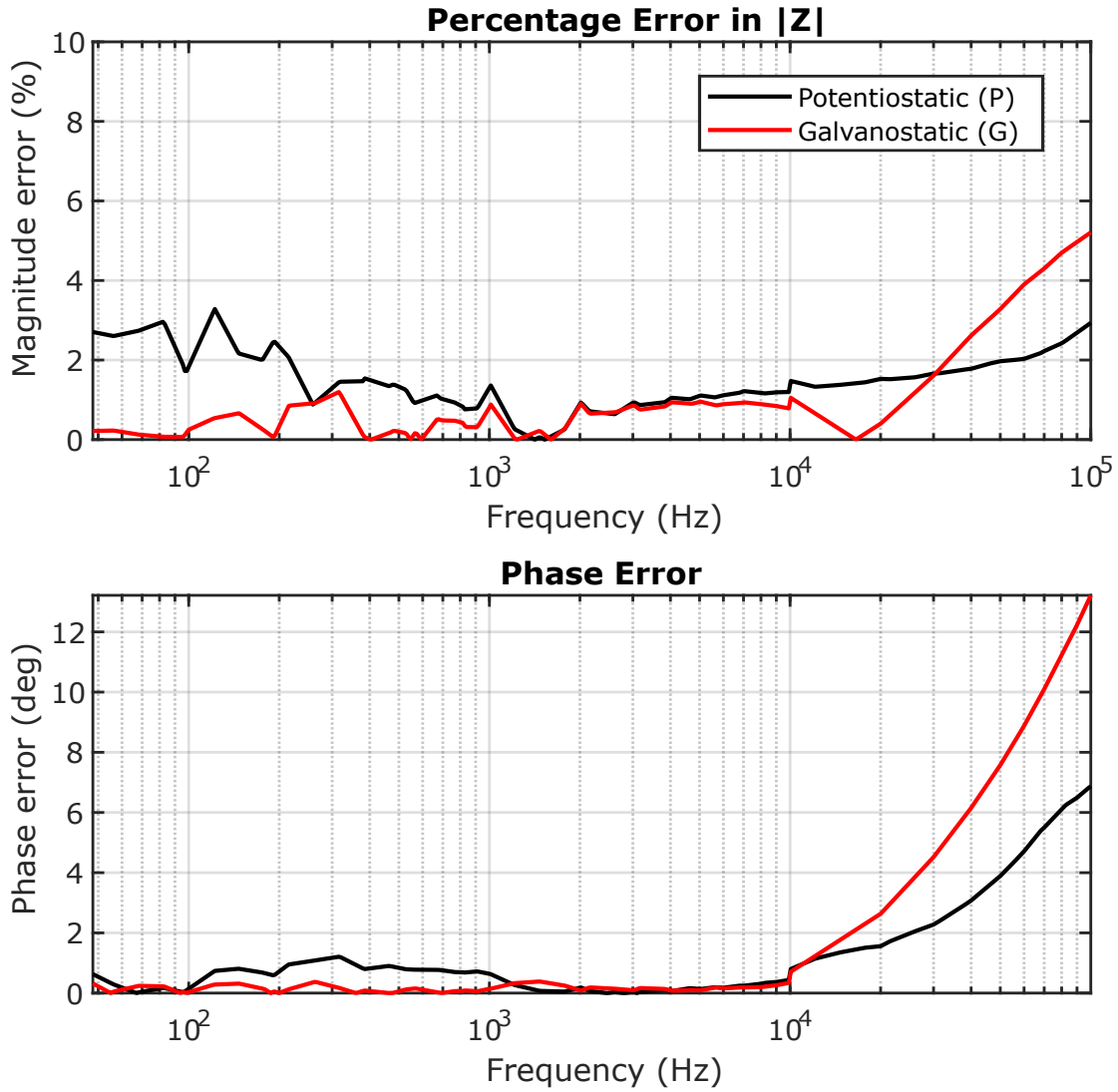


Figure 4.7: Percentage error of custom PCB impedance measurement board

Results

To compare the PCB-based device to the CHI760E system, linear interpolation was applied using MATLAB to resample the frequency points on the spectrum for comparing with the CHI760E. The analysis was then confined to the 48 Hz to 100 kHz range. The maximum magnitude errors between the systems were $54.4710\ \Omega$ for Potentiostatic Mode and $30.2578\ \Omega$ for Galvanostatic Mode.

The Bode plot (Figure 4.7) illustrates the impedance magnitude and phase across all measurement modes: galvanostatic EIS (red), potentiostatic EIS (black), and PCB-based EIS (blue).

The root mean square (RMS) errors for impedance magnitude were $\pm 3.65 \Omega$ (galvanostatic) and $\pm 4.79 \Omega$ (potentiostatic), while the corresponding phase RMS errors were $\pm 0.23^\circ$ and $\pm 5.33^\circ$, respectively.

At higher frequencies, larger phase errors were observed due to the ADC sampling rate of approximately 0.8 MHz in the custom device, which limited the number of samples per sine wave. Addressing this limitation would require either a higher sampling rate or the integration of external ADCs.

Discussion

The results demonstrate that the custom PCB-based impedance measurement system is capable of accurately determining the EIS of implantable electrodes, such as DBS electrodes, between 48 - 100 kHz frequency ranges with percentage error less than 5%. The two-electrode configuration introduces some limitations due to counter-electrode polarisation; however, it remains widely used in neural research experiments[92], [93]. For implantable applications, conductive materials such as platinum or stainless-steel screws can serve as counter-reference electrodes, providing a reliable alternative to Ag/AgCl, which is unsuitable for chronic use[132]. Future work could further improve measurement accuracy and enhance versatility as a research platform by adopting a three-electrode configuration with a dedicated reference electrode.

This system provides a foundation for electrochemical impedance spectroscopy (EIS) characterisation of implantable electrodes and demonstrates its potential for monitoring neural electrode impedance. To enable its use in implantable research platforms, the system will be scaled down and implemented in an integrated circuit (IC) design. The next chapter discusses the realisation of this EIS measurement architecture at the IC level, facilitating its application in compact, implantable neural interface devices.

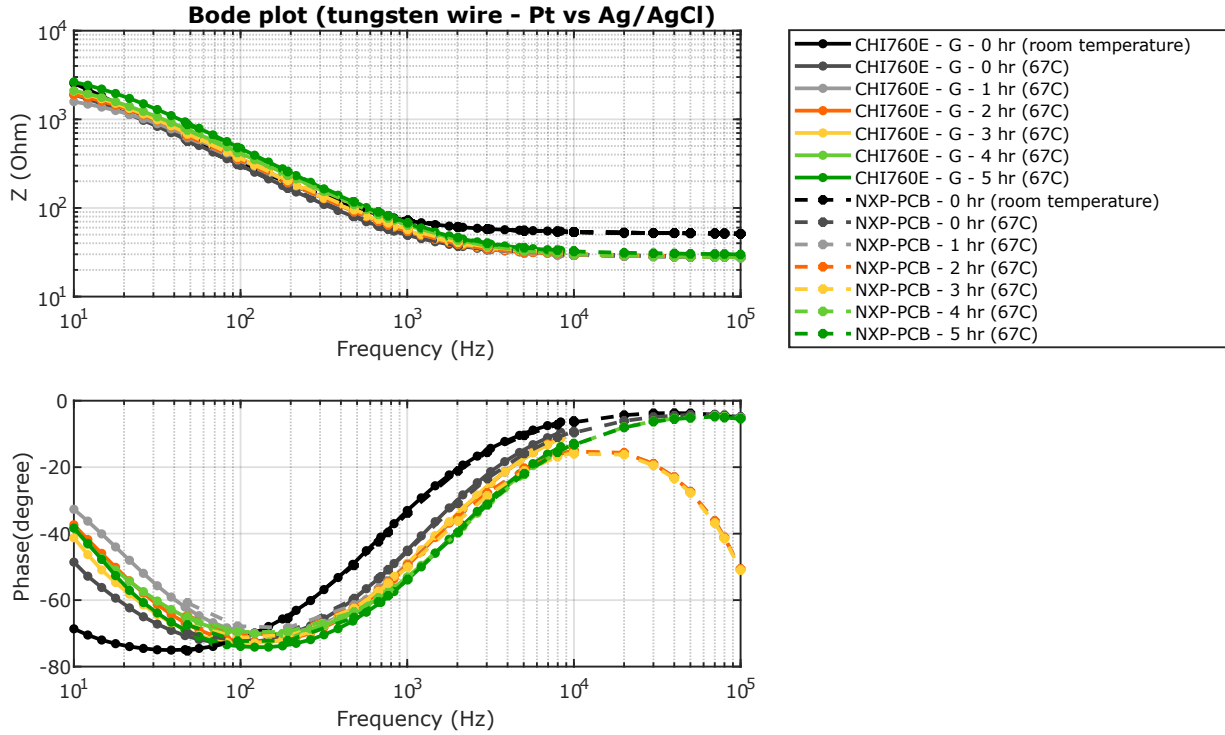


Figure 4.8: Comparison graph between EIS measuring by CHI760E and Impedance measurement PCB

4.3 Validation with Automated System for Operating the Bench-top

An automated platform was implemented to validate the PCB-based impedance measurement system alongside the CHI760E electrochemical workstation. The objective was to demonstrate that the custom system can reliably reproduce impedance measurements from a standard instrument and accurately track impedance variations associated with electrode degradation. Automated relay control and Python-based scheduling enabled synchronized stimulation and EIS measurement without manual intervention, improving repeatability and reducing experimental error.

The validation employed the accelerated aging protocol introduced in Chapter 3, using a tungsten electrode subjected to electrical and thermal stress. Impedance magnitude and phase data obtained from both systems were compared after resampling across 48 Hz–10 kHz using linear interpolation in MATLAB, with measurements performed in galvanostatic mode. As shown in

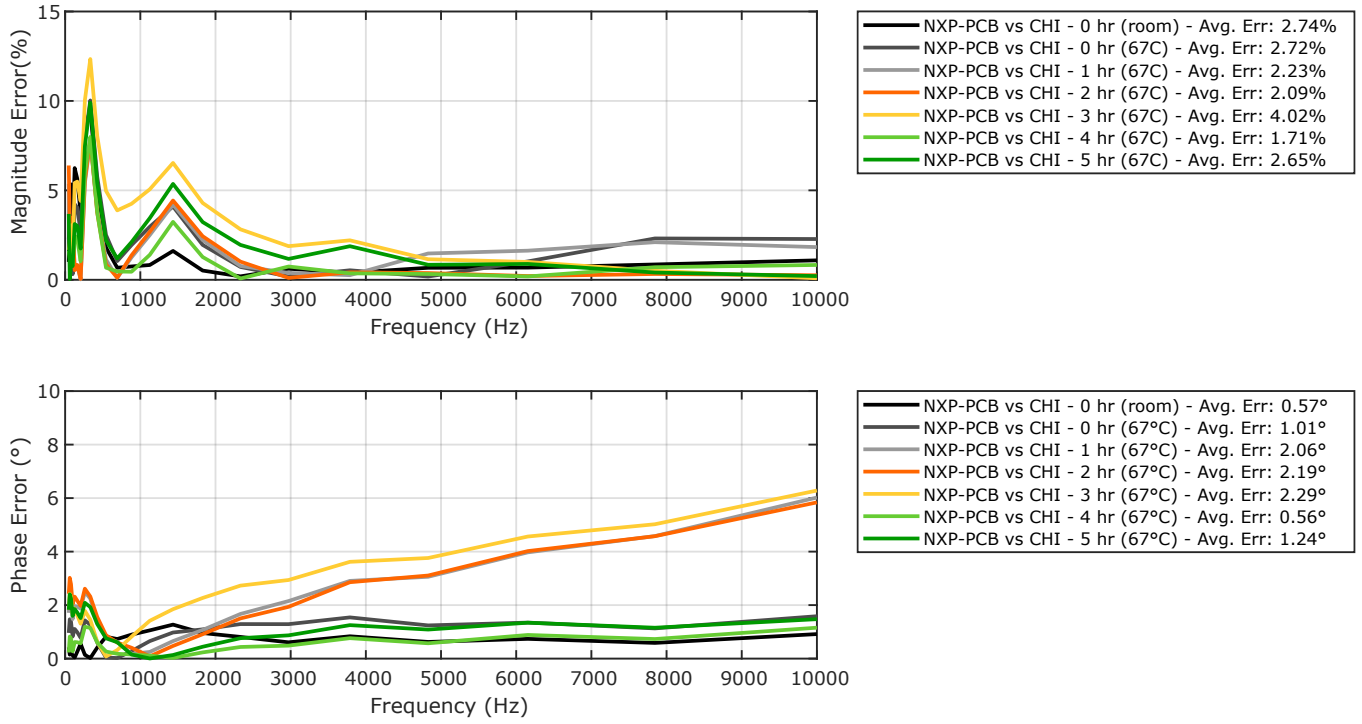


Figure 4.9: Average magnitude and phase errors between the PCB-based impedance measurement system and the bench-top electrochemical workstation during the accelerated degradation test

Figure 4.8, the PCB-based device achieved close agreement with the bench-top electrochemical workstation (CHI760E), with average magnitude errors ranging from 1.7% to 4.0% and phase errors between 0.6° and 2.3° over the five-hour degradation test. These results indicate that the system can reproduce impedance measurements comparable to those of the reference bench-top workstation and can capture changes associated with surface degradation under thermal and electrical stress. Although the experiment was conducted under accelerated *in-vitro* conditions and may not fully represent *in-vivo* behaviour, it demonstrates the system's capability to assess electrode impedance variations resulting from mechanical degradation processes.

Discussion

The PCB-based impedance measurement system produced results that closely matched those of the bench-top electrochemical workstation (CHI760E) throughout the accelerated degradation protocol. Over the six-hour experiment, the impedance of the tungsten electrode gradually

increased as degradation progressed under electrical stimulation and elevated temperature, consistent with the behaviour observed in Chapter 3. These impedance changes reflect the mechanical and electrochemical modifications occurring on the electrode surface during the aging process.

Impedance trends at representative frequencies exhibited a consistent increase over time in both measurement systems, indicating that the developed platform can reliably capture the evolution of electrode impedance during degradation. The agreement between the two systems demonstrates that the PCB-based platform is sufficiently accurate for *in-vitro* electrode characterisation (less than 4% error) and can be used to study surface degradation mechanisms under controlled conditions.

While the results confirm the device's performance for accelerated aging experiments, it is important to note that the observed impedance behaviour may not fully replicate *in-vivo* conditions, where biological factors such as tissue encapsulation and inflammation also influence electrode performance. Nonetheless, this validation provides a necessary step toward establishing the system's potential capability for long-term electrode characterisation. Building on these circuit design, the next chapter focuses on adapting the validated impedance measurement circuit for miniaturisation and integration at the IC level, enabling compact and scalable implementation within future bidirectional neural interface systems.

4.4 Conclusion

This chapter presented the development of a custom bench-top platform for electrode impedance characterisation. The system was designed to perform electrochemical impedance measurements for implantable neural electrodes and was evaluated using DBS lead electrodes and tungsten wire subjected to the accelerated degradation protocol described in Chapter 3. The developed platform was validated against a bench-top electrochemical workstation, showing close agreement across the tested frequency range.

The measurement system was designed to cover a frequency range from 1 Hz to 100 kHz. In

the current implementation, the lower frequency limit was constrained to 48 Hz due to the controller and hardware synchronisation between the DAC and ADC sampling processes. This limitation arose from the number of samples required per cycle and the available storage for waveform generation and acquisition. The measurable frequency range could be extended by reducing the sampling rate at lower frequencies, thereby decreasing memory and data transfer requirements.

Overall, the developed PCB-based platform provides a basis for impedance characterisation of implantable electrodes under controlled *in-vitro* conditions. The next chapter focuses on implementing this validated circuit at the integrated circuit (IC) level, which aims to improve measurement efficiency, extend the measurable frequency range, and enable compact integration within future neural interface systems.

Chapter 5

An integrated circuit-based EIS Platform for the Characterisation of Implantable Electrodes

5.1 Design and Implementation

This chapter builds upon the PCB platform introduced in the previous chapter, focusing on the implementation of an integrated circuit-based EIS platform for implantable electrode characterisation, specifically the Electrical Impedance Spectroscopy (EIS) measurement circuit designed for the NeuroZ chip. The NeuroZ chip, introduced and tested at the PCB level in the previous chapter, integrates essential components such as an 8-bit Digital-to-Analogue converter (DAC), a voltage-controlled current source (VCCS), an H-bridge, a buffered programmable differential amplifier, and a 12-bit Analogue-to-Digital converter (ADC). The design accommodates the constraints of implantable devices and the fabrication process using 180 nm CMOS technology, which supports only single-supply operation. To address these constraints, an H-bridge was introduced to enable polarity switching for the electrode under test, while a buffered differential

Portions of the research presented in this chapter have been published in V. Manatchinapisit, P. Feng, L. Xie, and T. G. Constandinou, "An Impedance Characterisation Circuit for Implantable Research Platforms," in *Proc. IEEE PRIME*, Larnaca, Cyprus, 2024, pp. 1-4 [133].

amplifier was employed for its simplicity and stability, ensuring compatibility with the project’s timeline and objectives.

Given the strict time constraints of the 2023 tape-out initial schedule—leaving only three months to complete the IC design—and my first time and my limited experience in designing a complete IC for fabrication, the decision was made to adapt and reuse existing circuit designs from prior lab projects, which will allow the system performance to be validated but be suboptimal in terms of complexity and power consumption. The 8-bit ADC and operational amplifier designs were sourced from [134], while the 12-bit ADC design was adapted from [134], [135], [136]. This approach allowed for feasibility within the restricted timeline while meeting the system requirements, as summarised in Table 5.1. The final design is tailored for experimental setups, enabling neural electrode impedance measurement with potential for future integration into implantable devices, such as deep brain stimulation (DBS) systems.

Specification	value	unit
CMOS Technology Process	180	nm
Power Supply		
Digital	1.8	V
Analog	5	V
Number of Channels	1	pair
Electrode Configuration	2	electrode
Frequency Range	1 - 100 k	Hz
Amplitude of Injected Current	5	μA
Impedance Measurement Range	100 - 1M	Ω
Impedance Resolution (ADC Resolution)	12	bits

Table 5.1: Impedance measurement IC expected specification

5.2 Top-Level Circuits

The EIS measurement circuit is designed as a compact and integrated system comprising several functional blocks, each fulfilling a specific role in the signal generation, delivery, and measurement workflow. The circuit’s architecture ensures high precision and stability while addressing the constraints of implantable device technology, such as single-supply operation and limited space.

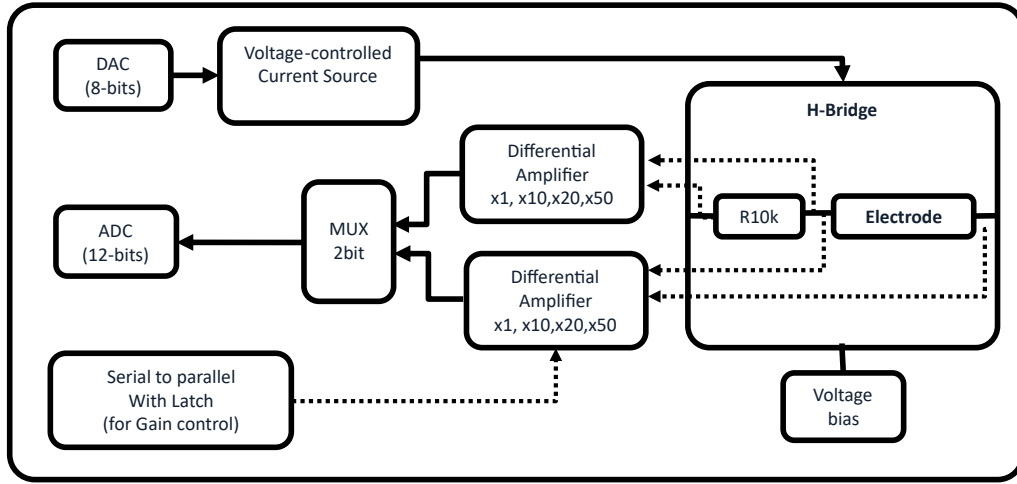


Figure 5.1: Top-level block diagram

At the highest level, the circuit consists of the following interconnected components:

1. Signal Generation:

An 8-bit Digital-to-Analogue Converter (DAC) generates a half-wave sinusoidal waveform with a 200 mV DC baseline. The DAC output serves as the input for the Voltage-Controlled Current Source (VCCS).

2. Current Conversion:

The VCCS converts the DAC's voltage output into a proportional current. This current is applied to the neural electrode through an H-bridge, which facilitates polarity switching for both cathodic and anodic phases.

3. Voltage Measurement:

Differential amplifiers capture voltage signals across the electrode and a reference resistor, amplifying the signals. A 12-bit analogue-to-digital converter (ADC) digitises these amplified signals for further analysis.

4. System Integration:

Rail-to-rail operational amplifiers maintain linear operation across the full voltage range. A 200 mV bias level aligns all signals with the system's operating point, ensuring compatibility with the electrode's open-circuit potential (OCP).

The system is designed to support impedance measurements across a frequency range of 1 Hz to 100 kHz. Each functional block has been carefully optimised to meet the performance, stability, and requirements, ensuring compatibility with implantable device constraints.

A block diagram of the top-level circuit is shown in Figure 5.13, illustrating the interconnections and signal flow between the key components.

5.2.1 Operational Amplifier

All circuit operations employ custom-designed rail-to-rail operational amplifiers to maintain consistent performance across the full voltage range. A 200 mV DC bias level was incorporated into the design to accommodate the non-ideal rail-to-rail behaviour of the operational amplifiers and to ensure that all signal levels remain within the specified input common-mode range (1.4–4.9 V).

Gain Bandwidth and Slew Rate Considerations

The performance of the operational amplifiers is critical to meeting the system design requirements, particularly in terms of gain bandwidth and slew rate. The amplifiers achieve a gain bandwidth of approximately 30 MHz when driving a 1 k Ω load and up to 40 MHz with a 5 M Ω load, which is sufficient to support impedance measurements up to 100 kHz.

Additionally, the slew rate of the operational amplifiers must be sufficient to accommodate the sinusoidal waveform generated by the DAC, which operates at a maximum frequency of 100 kHz with a peak amplitude of 0.5 V and the maximum supply is 5 V. The maximum rate of change of the sine wave occurs at its zero crossing and can be calculated as:

$$\text{Slew Rate} = 2\pi f_{\max} V_{\text{peak}}, \quad (5.1)$$

where $f_{\max} = 100$ kHz and $V_{\text{peak}} = 5$ V. Substituting these values:

$$\text{Slew Rate} = 2\pi(100 \times 10^3)(5) = 31400 \text{ V/ms} = 31.4 \text{ V}/\mu\text{s}. \quad (5.2)$$

Comparing this calculated value with the specification in Table 5.2, which lists a slew rate of $166.65 \text{ V}/\mu\text{s}$, confirms that the operational amplifiers meet the required performance. This ensures that the amplifiers can process high-frequency signals up to 100 kHz without waveform distortion.

The amplifiers' gain bandwidth and slew rate were selected to optimise performance while ensuring stability across the circuit's operational range. Stability is further reinforced by incorporating frequency compensation techniques to maintain a phase margin of at least 45° , as specified in Table 5.2.

Specification	value	unit
Technology	180	nm
Supply Voltage	5	V
Gain Bandwidth	30	MHz @ $1\text{k}\Omega$
	40	MHz @ $5\text{M}\Omega$
Input Common Mode Range	0.14-4.9	mV
Slew Rate	166.65	$\text{V}/\mu\text{s}$
Power Consumption	6.95	mW
Stability Margin	$\geq 45^\circ$	

Table 5.2: Rail-to-rail operational amplifier specification

5.2.2 Bias-Level Considerations

Open Circuit Potential (OCP) was measured six times for each electrode in a 37°C Phosphate Buffered Saline (PBS) solution using a CHI760E electrochemical workstation. The average open-circuit potential (OCP) values measured against the Ag/AgCl reference electrode were 406.50 mV for DBS, 17.00 mV for ECoG, 254.17 mV for SEEG, and 149.83 mV for CUFF electrodes. These values define the reference potentials for subsequent EIS measurements, with a bias voltage of approximately 200 mV applied to minimise perturbation while maintaining signal integrity. Conducting OCP measurements in physiological conditions helps evaluate the electrochemical stability and suitability of electrodes for EIS, ensuring the system is at equi-

librium prior to perturbation. The results provide essential baseline values for characterising electrode performance and ensuring reproducible outcomes in subsequent EIS experiments.

Additionally, the circuit operates around a 200 mV DC bias level to accommodate the non-ideal rail-to-rail behaviour of the operational amplifiers and to ensure all signals remain within the specified input common-mode range (1.4–4.9 V). This bias supports stable operation of the H-bridge, VCCS, and other connected subsystems while maintaining consistent alignment of voltage and current signals across the system. All circuit blocks, including the DAC, VCCS, differential amplifiers, and ADC, were designed or adjusted to operate with this bias level.

5.2.3 Digital-to-Analogue Converter (DAC)

The DAC utilises an R-2R ladder topology with a unit resistance $R_{\text{unit}} = 100 \text{ k}\Omega$. It is designed to generate a half-wave sinusoidal waveform ($0\text{--}180^\circ$) within a voltage range of $0\text{--}0.5 \text{ V}$. Due to the system's design constraints, the output waveform baseline is shifted to 200 mV, consistent with the system's DC bias level. The DAC output is buffered using a unity-gain rail-to-rail operational amplifier, which incorporates a constant g_m circuit [137] in the input stage and an indirect compensation technique [138] in the output stage. These enhancements enable the amplifier to handle a wide range of loads effectively. The buffered voltage output from the DAC is fed to the Voltage-Controlled Current Source (VCCS) for current conversion.

5.2.4 Voltage-Controlled Current Source (VCCS)

The VCCS circuit is identical to the design implemented on the PCB board described in the previous chapter. It is a high-speed, three-op-amp topology designed for voltage-to-current (V-to-I) conversion. The DAC output serves as the input (V_{in}) for the VCCS, which generates a half-wave sinusoidal output current proportional to the input voltage, using a fixed $R_s = 100 \text{ k}\Omega$. The current output is governed by:

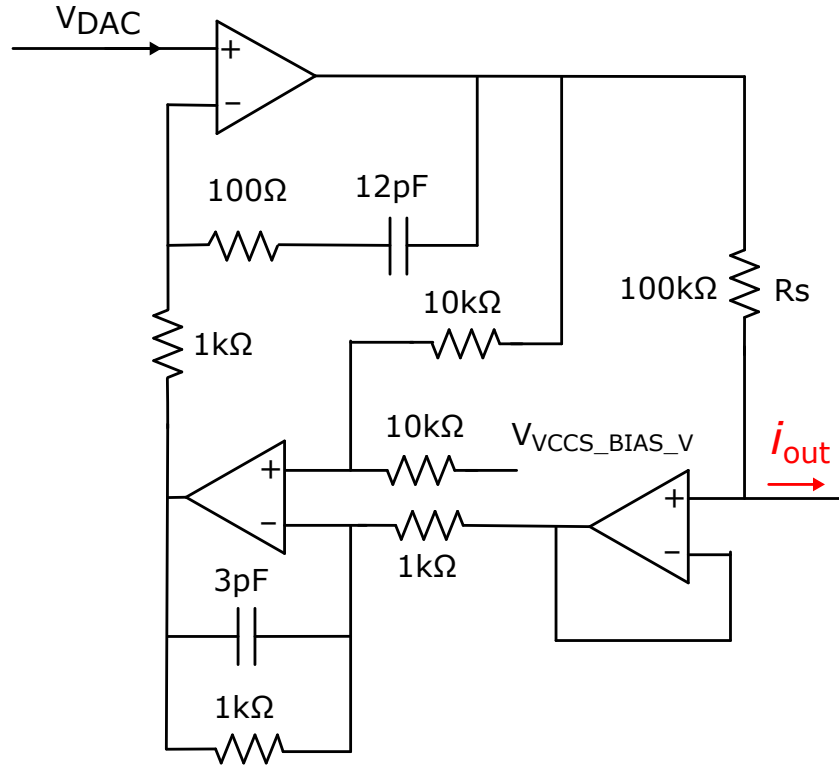


Figure 5.2: Voltage controlled current source

$$I_{\text{out}} = \frac{V_{\text{DAC}}}{R_s}$$

Negative feedback stabilises the voltage across R_s , enabling accurate and repeatable current generation by the VCCS. The nominal current amplitude, controlled by the output voltage of the DAC, is $5\text{ }\mu\text{A}$ ($10\text{ }\mu\text{A}$ peak-to-peak). To maintain consistency with the system's 200 mV DC bias, the ground reference of the VCCS is shifted accordingly, ensuring that the output current waveform remains centred around the same baseline.

The measurable impedance range is defined by the relationship between the DAC-controlled current amplitude and the voltage compliance of the circuit. With a nominal current of $5\text{ }\mu\text{A}$ and a compliance limit of approximately $\pm 0.5\text{ V}$, the system can accurately measure impedances up to $100\text{ k}\Omega$ without distortion. For higher-impedance conditions, particularly near $1\text{ M}\Omega$, the DAC output amplitude is reduced to generate a current of 500 nA ($1\text{ }\mu\text{A}$ peak-to-peak), ensuring the output voltage remains within the compliance limits. This configuration enables precise impedance characterisation across a range of $100\text{ }\Omega$ to $1\text{ M}\Omega$.

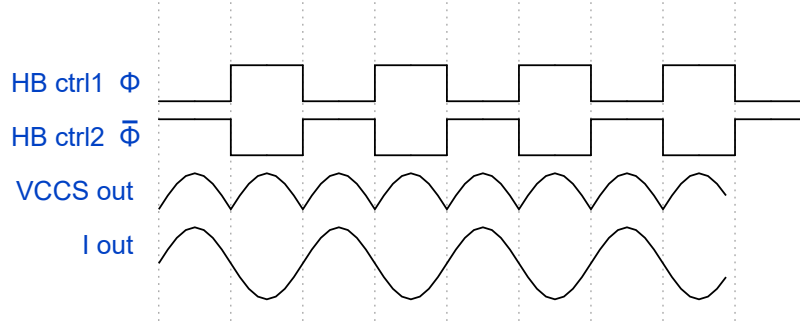


Figure 5.3: H-Bridge control time diagram

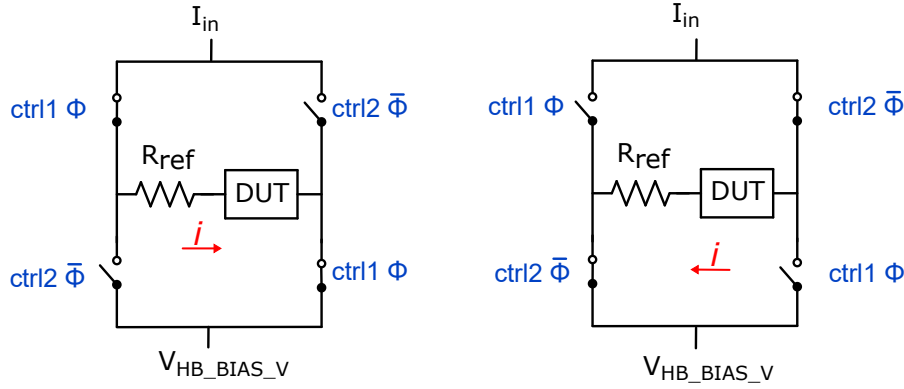


Figure 5.4: H-Bridge stage

5.2.5 H-Bridge

The H-bridge is responsible for controlling the polarity of the current applied to the working and counter electrodes, enabling the injection of both positive and negative currents. The total current delivered across the electrodes is maintained at $10\text{ }\mu\text{A}$ peak-to-peak. Voltage measurements are performed across the reference resistor ($10\text{ k}\Omega$) and the device under test (DUT) using two buffered differential amplifiers with high input impedance, ensuring precise signal acquisition without loading the measurement nodes.

Due to the non-ideal rail-to-rail performance of the operational amplifiers used in the circuit, the voltage at the return path of the H-bridge is DC-biased at 200 mV . Consequently, the baseline of the waveform generated is shifted to 200 mV . To maintain the output current waveform at this shifted baseline, the ground of the VCCS is also adjusted to 200 mV , ensuring proper alignment of the system's voltage and current signals.

5.2.6 Differential Amplifiers

The system incorporates two buffered differential amplifiers with programmable gain settings of 1, 10, 20, or 50. These amplifiers were selected for their simplicity and minimal component requirements, making them suitable for implementation given the project's time constraints. Additionally, reducing the number of resistors minimises the potential for resistor mismatch. The primary purpose of these amplifiers is to evaluate the performance of the electrical impedance spectroscopy (EIS) system.

To enhance measurement accuracy, buffers are integrated into both the positive and negative inputs of the amplifiers. This configuration increases input impedance, isolates the amplifiers from the signal source to prevent attenuation or distortion, and reduces noise and interference by providing a high-impedance interface. Since the system is designed to measure impedance over a wide frequency range (1 Hz to 100 kHz) with varying impedance magnitudes, the amplifiers are made programmable to accommodate different signal conditions. This programmability is achieved through the use of transmission gates, enabling the selection of appropriate gain settings for optimal performance across the measurement range.

Finally, to ensure compatibility with the subsequent analogue-to-digital converter (ADC) stage, the amplifier output is shifted to the mid-rail of the ADC's supply voltage (0.9 V, from a total supply of 1.8 V). This output shift prevents signal clipping and ensures accurate digitisation in the ADC.

5.2.7 Serial to Parallel for programmable gain control

The circuit consists of three primary components: an 8-bit shift register, a latch with an active-high enable signal, and a differential amplifier with digitally programmable gain control. The shift register, implemented with 8 D flip-flops connected in series, converts a serial input (D_{in}) into an 8-bit parallel output ($Q_1, Q_2, \dots, Q_8$) by sequentially shifting each bit on the rising edge of the clock (CLK). Initially, all flip-flops are reset to low (0), and with each clock pulse, the bits are shifted until the register holds the complete parallel data. The latch captures

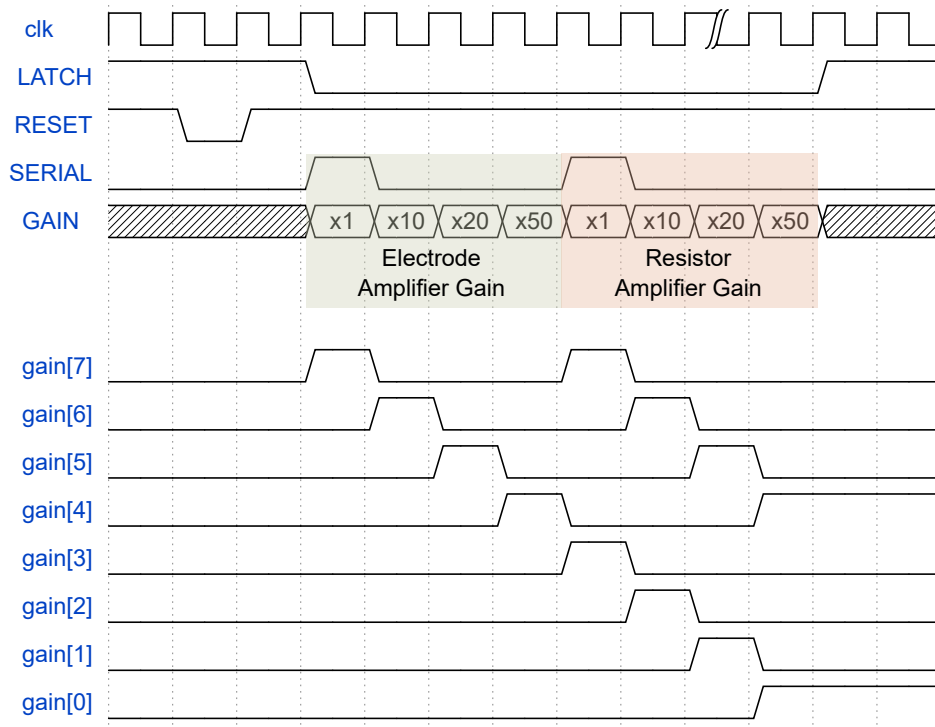


Figure 5.5: Example gain control serial input and latch time diagram

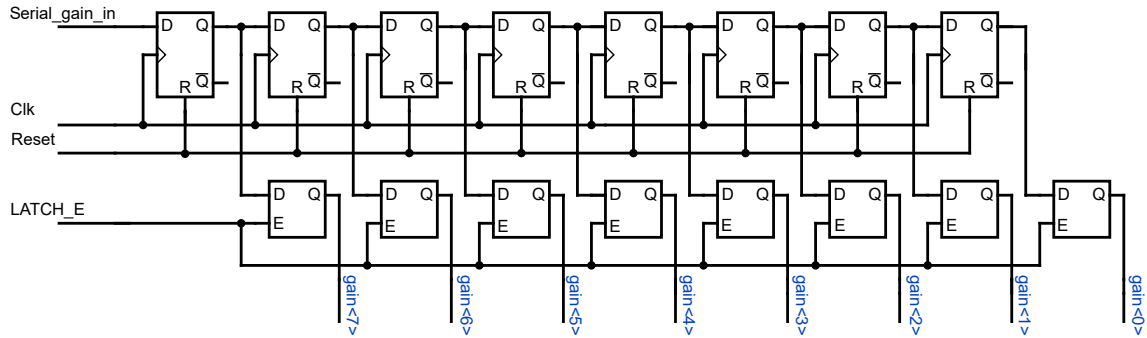


Figure 5.6: serial to parallel circuit including D flip-flop and active low latch

this parallel output when the enable signal (EN) is active high (1), retaining the data and decoupling the output from further changes in the shift register when the signal transitions to low (0). This stable parallel output is used to program the gain of a differential amplifier.

The 8-bit binary input (0bxxxxyyyy) provides flexibility, enabling a total of 16 unique gain configurations. The most significant 4 bits ($xxxx$) define $Gain_{\text{electrode}}$, applied to the device under test (DUT), while the least significant 4 bits ($yyyy$) determine $Gain_R$, applied to the reference resistor. This setup ensures precise and synchronised control of the amplifier's gain, with the latch governing the timing and stability of the output.

Input 1	$Gain_{electrode}$	$Gain_R$	Input 2	$Gain_{electrode}$	$Gain_R$
10001000	1	1	10001100	10	1
10001001	1	10	10001101	10	10
10001010	1	20	10001110	10	20
10001011	1	50	10001111	10	50
Input 3	$Gain_{electrode}$	$Gain_R$	Input 4	$Gain_{electrode}$	$Gain_R$
10010000	20	1	10010100	50	1
10010001	20	10	10010101	50	10
10010010	20	20	10010110	50	20
10010011	20	50	10010111	50	50

Table 5.3: Gain Configuration Table for Impedance Measurement System. The table shows all 16 possible configurations for the 8-bit binary input ('0bxxxxyyyy'), with corresponding gain values for the differential amplifier across the device under test ($Gain_{electrode}$) and the reference resistor ($Gain_R$).

By supporting independent gain configurations for both the DUT and the reference resistor, this design optimises the performance of the impedance measurement system. The programmable gain control facilitates accurate characterisation of the DUT across a wide frequency spectrum. Table 5.3 details the specific gain configurations available.

5.2.8 Analogue-to-Digital Converter (ADC)

The outputs of the two differential amplifiers are multiplexed into a 12-bit Analogue-to-Digital Converter (ADC), as illustrated in Figure 5.1. The ADC operates on a charge-redistribution successive approximation topology with a unit capacitance $C_{\text{unit}} = 33.4 \text{ fF}$. It features a sampling rate of 1 MHz and an input voltage range of 0.1 V to 1.7 V. The designs of the DAC and ADC are adapted from those described in [134], with modifications to meet the specific requirements of this application. The 200 mV baseline shift is accounted for in the ADC's signal processing to ensure accurate digitisation of the measurements.

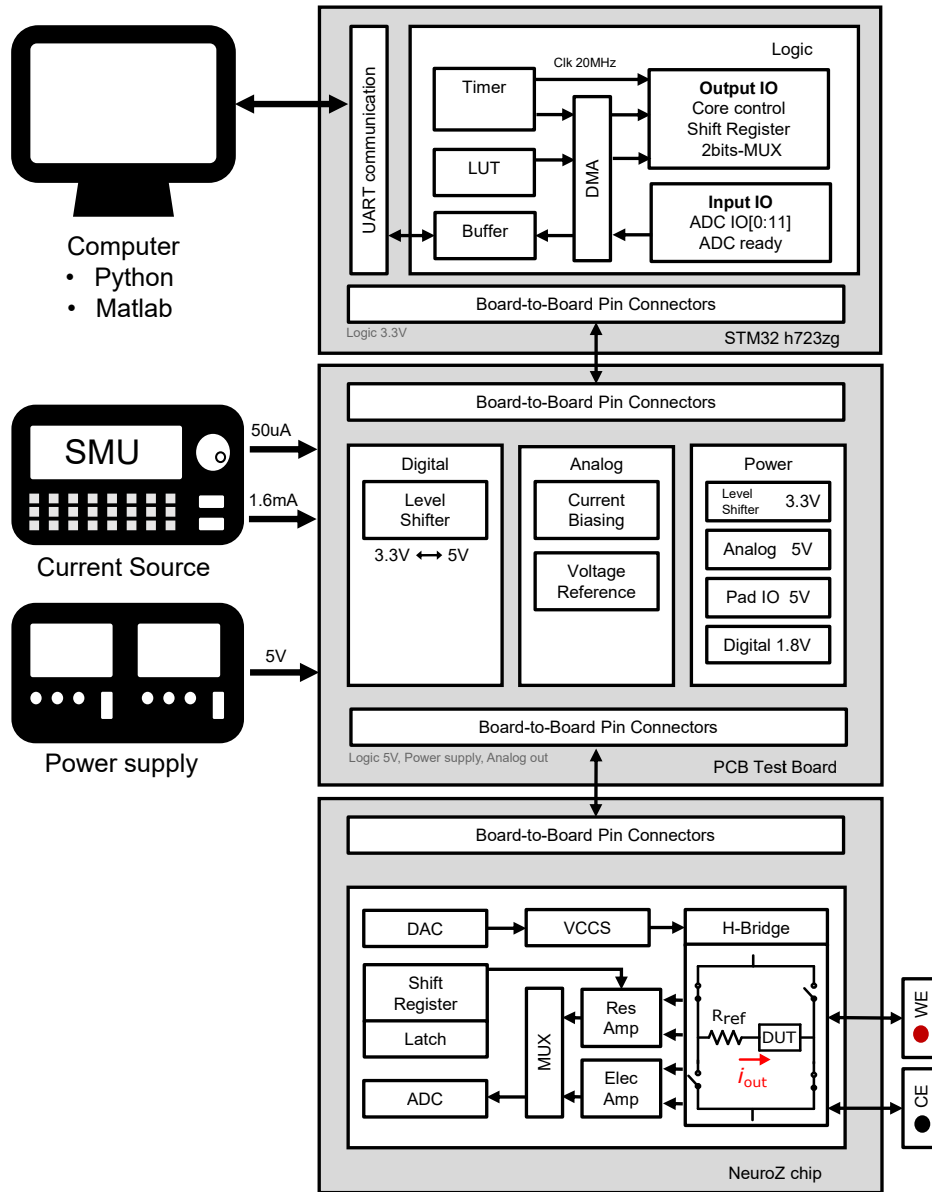


Figure 5.7: The testing board integrates the packaged NeuroZ chip and MCU via board-to-board pin connectors for impedance measurement. The MCU generates logic controls and receives the waveform output from the on-chip ADC. The received waveform data is then packaged and sent to a computer for impedance analysis. A level shifter converts 3.3 V to 5 V and vice versa for data transmission. A 5 V power supply, regulated by an LDO, provides 3.3 V for the level shifter and an external DAC, which supplies voltage references to the chip, as well as 1.8 V and 5 V to power the NeuroZ chip. The current bias (50 μ A and 1.6 mA) is sourced from the SMU. The system operates with digital control, signal processing, and power regulation for impedance characterisation.

5.3 Operation and Functional Overview of the NeuroZ Chip

The NeuroZ chip integrates a total of 74 interface pads, facilitating seamless communication between its analogue and digital subsystems. These connections include 23 analogue pads (11 inputs and 12 outputs), 19 digital pads (6 inputs and 13 outputs), and dedicated ground and power pads supporting 1.8 V and 5 V supplies. Designed for electrode-tissue interface characterisation, the NeuroZ chip enables control of signal generation and data acquisition. This system is tested using a custom PCB board and a microcontroller-based logic control setup. The following sections elaborate on its input/output management, initialisation processes, data flow, and post-processing for impedance analysis.

analogue pin	Input	Unit
ADC_REF_0V9	0.9	V
ADC_RANGE_1V6	1.6	V
DAC_VREF+	4.5	V
DAC_VREF-	0	V
IBIAS_P	50	uA
IBIAS_P50x	1.6	mA
VCCS_BIAS_V	200	mV
HB_BIAS_V	200	mV
DIFF_VREF_RS	0.9	V
DIFF_VREF_ELEC	0.9	V
ADC_VIN_MUX	0-1.8	V

Table 5.4: Analogue input pin

5.3.1 Analogue and Digital Input/Output Management

Analogue Inputs

The analogue subsystem accommodates inputs essential for biasing operational amplifiers, supplying voltage references, and ensuring signal conditioning. Biasing currents for the first and last branches of the operational amplifier are set to 50 μ A and 1.6 mA, respectively. Additional analogue inputs provide references for critical subsystems such as the Digital-to-Analogue con-

Digital pin	Input	Output	Frequency
CLK	5 V		20M
DAC8 <0:7>	5 V		8M
ADC			
ADC_START	5 V		5 k - 1 M
ADC_RESET	5 V		5 k - 1 M
HB MUX			
CTRL_01	5 V		$f_{sine}/2$
CTRL_02	5 V		$f_{sine}/2$
CTRL_dummy	5 V		
ADC MUX (2bits)			
CTRL_S01	5 V		
CTRL_S02	5 V		
Shift register (programmable gain)			
Serial_gain_in	5 V		
LATCH_EN	5 V		
RESET_SR	5 V		
12 bits ADC output			
ADC_ready		5 V	
ADC_DOUT_<0:11>		5 V	

Table 5.5: Digital pin

verter (DAC), a voltage-controlled current source (VCCS), an H-bridge circuit, differential amplifiers, and an Analogue-to-Digital converter (ADC).

Digital/Logic Control

The NeuroZ chip is mounted inside a CLCC84 ceramic package and plugged into a custom-designed testing PCB board for its operation. The PCB integrates multiple power management components, including low-dropout (LDO) regulators for 1.8 V, 3.3 V, and 5 V supplies. The

Power pin	Input	Unit
VDDPST	5	V
AVDDesd_5V	5	V
VDD_A5V0	5	V
VDD_A1V8	1.8	V
VDD_D5V0	5	V
VDD_D1V8	1.8	V
VSSPST	0	V
DGND	0	V
AGND	0	V

Table 5.6: Power pin

1.8 V and 5 V rails power the NeuroZ chip, while the 3.3 V rail supplies the external 12-bit DAC used to generate voltage references and supports a level shifter for translating signals between 3.3 V and 5 V logic levels.

Control of the NeuroZ chip is managed by the STM32 Nucleo-144 development board, which features the STM32H723ZG microcontroller. This microcontroller, based on an Arm Cortex-M7 processor operating at up to 550 MHz, provides extensive computational capabilities for embedded applications. The microcontroller generates critical digital input signals, including an 8-bit data stream for the integrated DAC, clock outputs for synchronisation, and serial control signals for configuring the gain of the differential amplifiers.

The STM32H723ZG leverages its MCO (Microcontroller Clock Output) pin to output a 120 MHz clock signal derived from its internal phase-locked loop (PLL). This signal serves as a clock input for the NeuroZ chip, ensuring precise operation and synchronisation. Additionally, its integrated peripherals, such as two 16-bit ADCs, two 12-bit DACs, and a 16-stream DMA controller, enable efficient data handling and real-time signal processing.

A level shifter on the PCB ensures compatibility between the 3.3 V operational voltage of the STM32H723ZG and the 5 V signals required by the NeuroZ chip. This bidirectional level shifter maintains signal integrity by converting 3.3 V outputs to 5 V and translating incoming 5 V signals to 3.3 V. Furthermore, the microcontroller transmits 8-bit serial data along with a latch signal to a shift register, which converts the serial data into parallel outputs. These outputs are used to configure the gain of the NeuroZ chip's differential amplifiers, optimising the system for impedance measurements.

Output Signals

The ADC outputs 12-bit parallel data to the microcontroller, which processes and packages it for transmission to an external computer. This facilitates real-time monitoring of electrode voltage and current signals for subsequent processing and analysis.

5.3.2 Initialisation and Configuration

Waveform Generation and Frequency Control

The generation of a half-sine waveform is the first step in the initialisation process. The waveform is stored as an 8-bit lookup table (LUT) in the microcontroller unit (MCU). The frequency of the sine wave is defined in this phase and adjusted dynamically by modifying the timer settings of the Direct Memory Access (DMA) module. A predefined frequency sweep ranging from 1 Hz to 100 kHz is employed, with specific points at 1, 10, 40, 100, 200, 500, 800, 1 k, 2 k, 5 k, 6 k, 8 k, 10 k, 20 k, 40 k, 50 k, 60 k, 80 k, and 100 kHz.

DMA and Timer Configuration

The DMA and timer are configured to transfer LUT values to the DAC, creating a continuous sine wave. For example, at a 1 kHz frequency, the DMA outputs a sample every 1 ms. Upon completing one half-sine waveform, an interrupt toggles the polarity of the H-bridge, enabling both current sinking and sourcing through the electrode-tissue interface.

ADC Sampling Setup

The ADC sampling rate is adjusted based on the injected sine wave frequency. For frequencies up to 800 Hz, the sampling rate is set to 5 kHz. For frequencies between 1 kHz and 10 kHz, a sampling rate of 100 kHz is used. For higher frequencies (10 kHz to 100 kHz), the rate increases to 500 kHz or 800 kHz. Due to an interrupt latency exceeding 155 ns, a 1 MHz sampling rate cannot be achieved with the 20 MHz system clock, where each clock cycle is 50 ns. Consequently, the maximum sampling rate is limited to 800 kHz.

Voltage Reference Configuration

Voltage references for the analogue subsystems are programmed via I2C commands to a 12-bit DAC on the test PCB board. This ensures stable operation of the VCCS, H-bridge, and other analogue components.

5.4 Data Flow and Signal Control

Half-Sine Waveform Transmission During operation, the DMA reads values from the LUT and transfers them to the DAC at intervals defined by the timer. This creates the sine wave signal that is applied across the electrode-tissue interface. Interrupts triggered upon completing the half-sine waveform toggle the H-bridge polarity, allowing the system to alternate between current sinking and sourcing.

ADC Sampling and Data Collection The ADC samples the voltage signals across the electrode and reference resistor, storing 20,000 samples in buffer arrays. These samples are transmitted as data packets via UART to a host computer for further processing. Metadata such as sine frequency, ADC sampling rate, and amplifier gain settings are included in the transmitted data.

Post-Processing and Analysis On the host computer, a Python script initiates the measurement sequence, receives the data transmitted from the device, and stores it for subsequent analysis. The recorded voltage and current signals are processed in MATLAB using the Fast Fourier Transform (FFT) to identify the dominant frequency component corresponding to the excitation signal. The amplitude and phase are extracted by locating the frequency bin with the maximum magnitude within a $\pm 10\%$ window around the target frequency. These values are then used to calculate the electrode impedance.

The amplitude of the current is derived as:

$$I_{\text{electrode}} = \frac{V_{\text{resistor}}}{R_{\text{ref}}}$$

where V_{resistor} is the voltage across the reference resistor, and R_{ref} is the resistor value. The impedance magnitude is calculated as:

$$Z_{\text{magnitude}} = \frac{V_{\text{electrode}}}{I_{\text{electrode}}}$$

The real and imaginary components of the impedance are computed using the phase angle

(ϕ) , which is obtained from the phase difference between the FFT-derived voltage and current signals. The impedance is then calculated as:

$$Z_{\text{real}} = |Z| \cos(\phi), \quad Z_{\text{imaginary}} = |Z| \sin(\phi)$$

The computed impedance values are used to construct Bode plots, which visualise the impedance magnitude and phase across the frequency range.

The NeuroZ chip integrates analogue and digital subsystems to perform electrode impedance characterisation over a wide frequency range. Dynamic frequency control, DMA-based data transfer, and ADC synchronisation facilitate consistent measurement timing and data acquisition. The collected data are processed using Python and MATLAB to extract impedance parameters for further analysis. Overall, the system provides a flexible platform suitable for

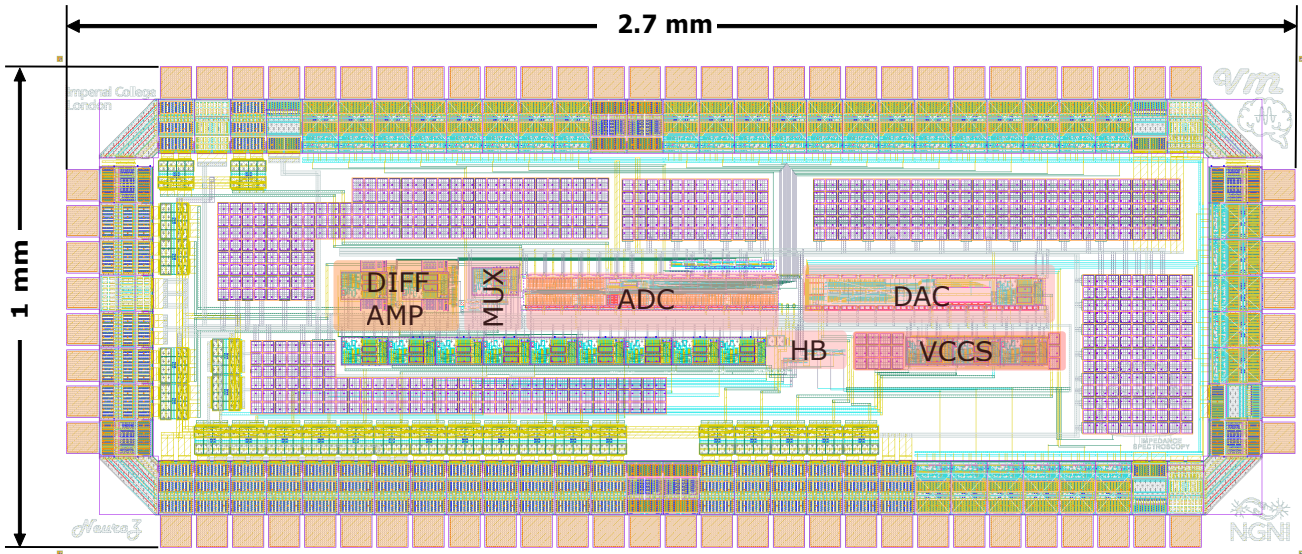


Figure 5.8: NeuroZ chip in cadence

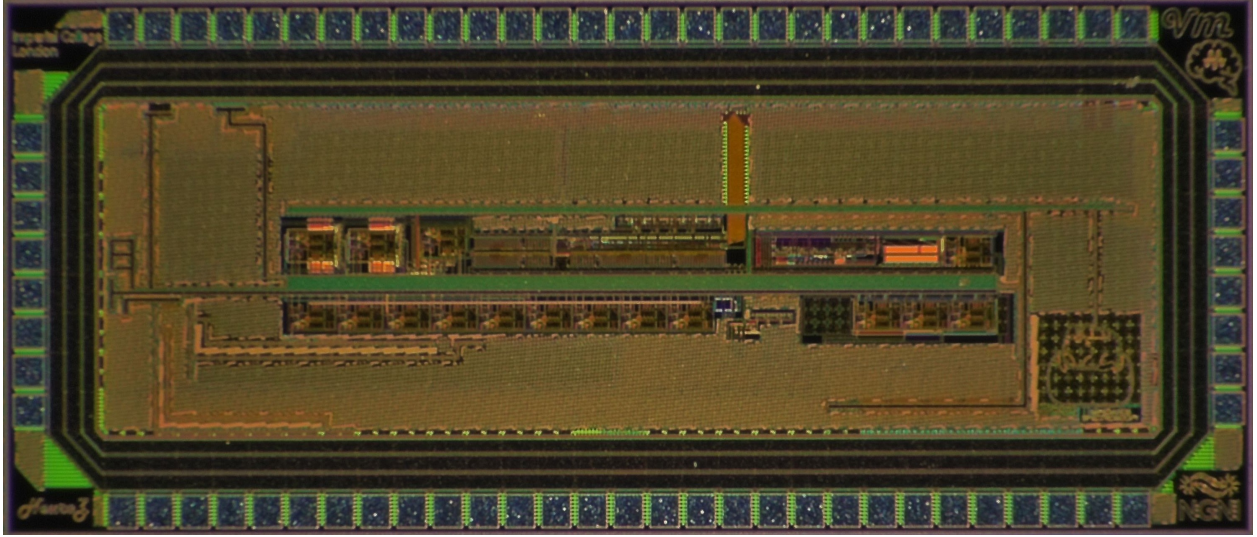


Figure 5.9: NeuroZ chip under microscope

5.5 Layout

The layout of the impedance measurement system is presented in Figure 5.9. This is a pad-limited design with a total area of $1 \times 2.7 \text{ mm}^2$, encompassing the core circuit, test buffers, and bond pads. The core circuit occupies an area of less than 0.5 mm^2 .

5.6 Power Measurement

The power consumption of the custom IC was measured using a regulated 5 V DC power supply to evaluate its energy efficiency during impedance characterisation. The current consumption was monitored directly from the power supply's built-in current display, ensuring a real-time measurement under operating conditions. During the impedance measurement process, the power supply indicated a current draw of 27 mA, leading to a total power consumption of:

$$P = V \times I = 5V \times 27mA = 135mW \quad (5.3)$$

In simulation, the test chip was estimated to operate with a power consumption of approxi-

mately 80 mW. However, the majority of this power is consumed by the rail-to-rail operational amplifiers used across the design. These amplifiers, which also function as test buffers to enable observation of internal node voltages, contribute significantly to the overall power budget. The discrepancy between simulated and measured power consumption is likely due to real-world factors such as parasitic losses, leakage currents, and power delivery inefficiencies that are not fully accounted for in simulation models. Furthermore, the impedance measurement function is designed to be used infrequently and will remain powered down for most of the time, minimising its overall impact on system energy consumption.

5.7 Simulation

The circuit was simulated in the Cadence Virtuoso analogue design environment using transistor models from the TSMC 180 nm CMOS process provided by the foundry. To incorporate realistic electrode impedance characteristics, Electrochemical Impedance Spectroscopy (EIS) measurements were conducted using an electrochemical workstation. A DBS lead (Medtronic 3389) was employed as the working electrode, with the outermost contact immersed in phosphate-buffered saline (PBS), while a platinum sheet (2.5 cm $\times$ 2.5 cm) served as the counter electrode and an Ag/AgCl electrode was used as the reference. The measured impedance data were fitted to a simplified Randles model, which represents the electrode–electrolyte interface, as illustrated in Figure 5.10. The fitting yielded $C_{dl} = 4.67 \mu\text{F}$, $R_{ct} = 147 \text{ k}\Omega$, and $R_s = 232 \Omega$. These extracted parameters were subsequently used in the circuit simulation to represent the electrode behaviour and to generate the corresponding impedance spectrum, as shown in Figure 5.12.

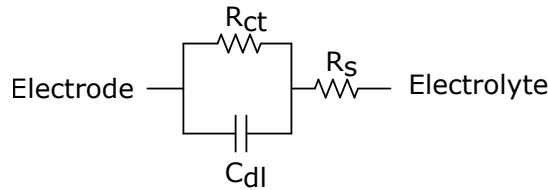


Figure 5.10: Electrode-electrolyte interface equivalent circuit model (C_{dl} =double-layer capacitance, R_{ct} =charge transfer resistance, R_s =Electrolyte or solution resistance).

5.7.1 Current injection and measured voltage responses

The simplified Randles model of the DBS electrode was incorporated as a reference component in the simulation to evaluate the performance of the complete system. Figure 5.11 illustrates the simulated voltage across the reference resistor and the DBS electrode model, together with the corresponding current and voltage waveforms within the EIS measurement path. At a representative frequency of 10 kHz, the half-cycle sinusoidal waveform generated by the DAC exhibits an amplitude of approximately 0.49 mV. The VCCS converts this input into a current output of 4.9 μ A, which is delivered simultaneously to R_{ref} and the DBS electrode–electrolyte model.

To extract the impedance characteristics, the simulated voltage signals were analysed using the Fourier Transform (FT), allowing the determination of both the magnitude and phase shift from the voltage responses measured across R_{ref} and the DBS electrode model.

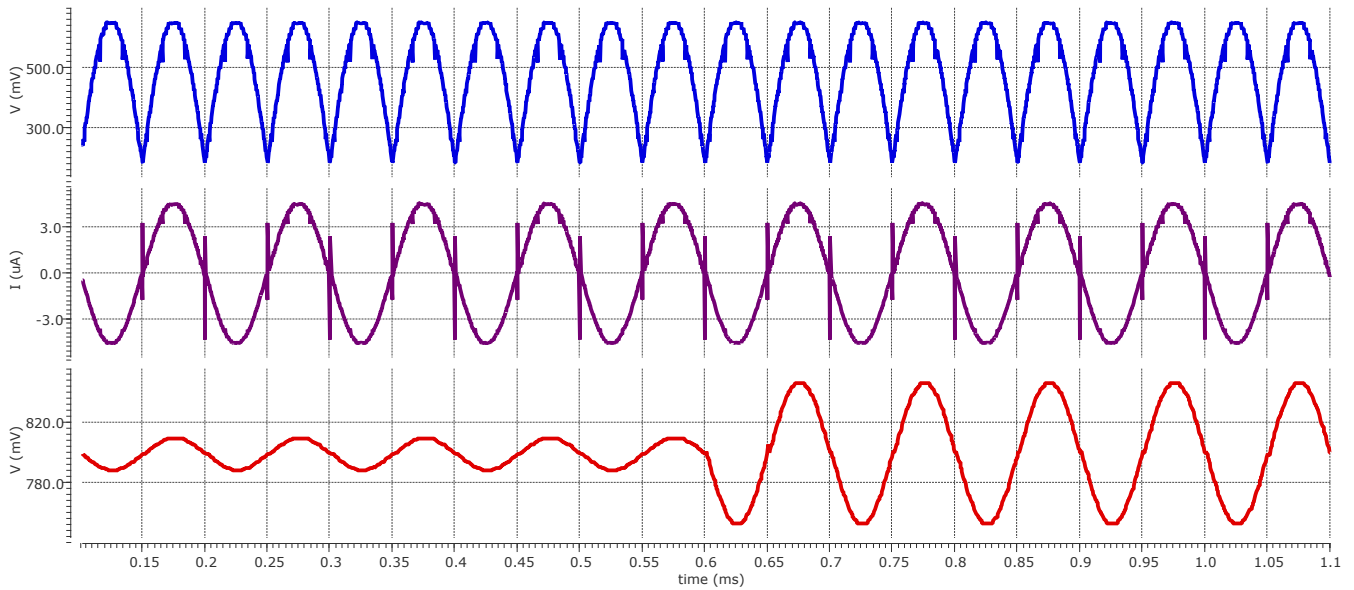


Figure 5.11: Simulated voltage and current waveforms across the DBS electrode model obtained in Cadence

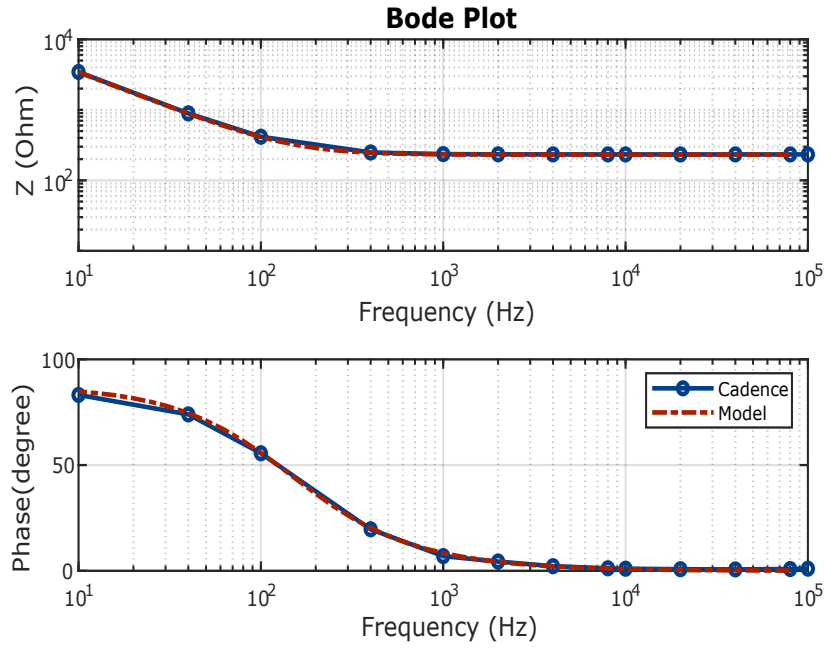


Figure 5.12: EIS result for equivalent circuit model of DBS electrode

5.7.2 Simulation EIS results

The sinusoidal waveform frequency was varied from 10 to 100 kHz in 13 incremental steps, as depicted in Figure 5.12. The Bode plot presents the impedance spectrum, contrasting the DBS electrode model (red) with the simulation results from Cadence (blue). The root mean square error for the magnitude was $\pm 54.43 \Omega$, while the phase shift error was approximately $\pm 0.5^\circ$ over the entire frequency range.

5.8 Measurement and Testing system

5.8.1 Testing board

The PCB testing board as in figure 5.13 was designed using Altium and features several key components to facilitate testing and debugging. The board includes a header pin for plugging in the STM32 Nucleo H723ZG microcontroller and another header for the packaged NeuroZ chip. It incorporates a level shifter to convert digital input and output signals between 3.3 V

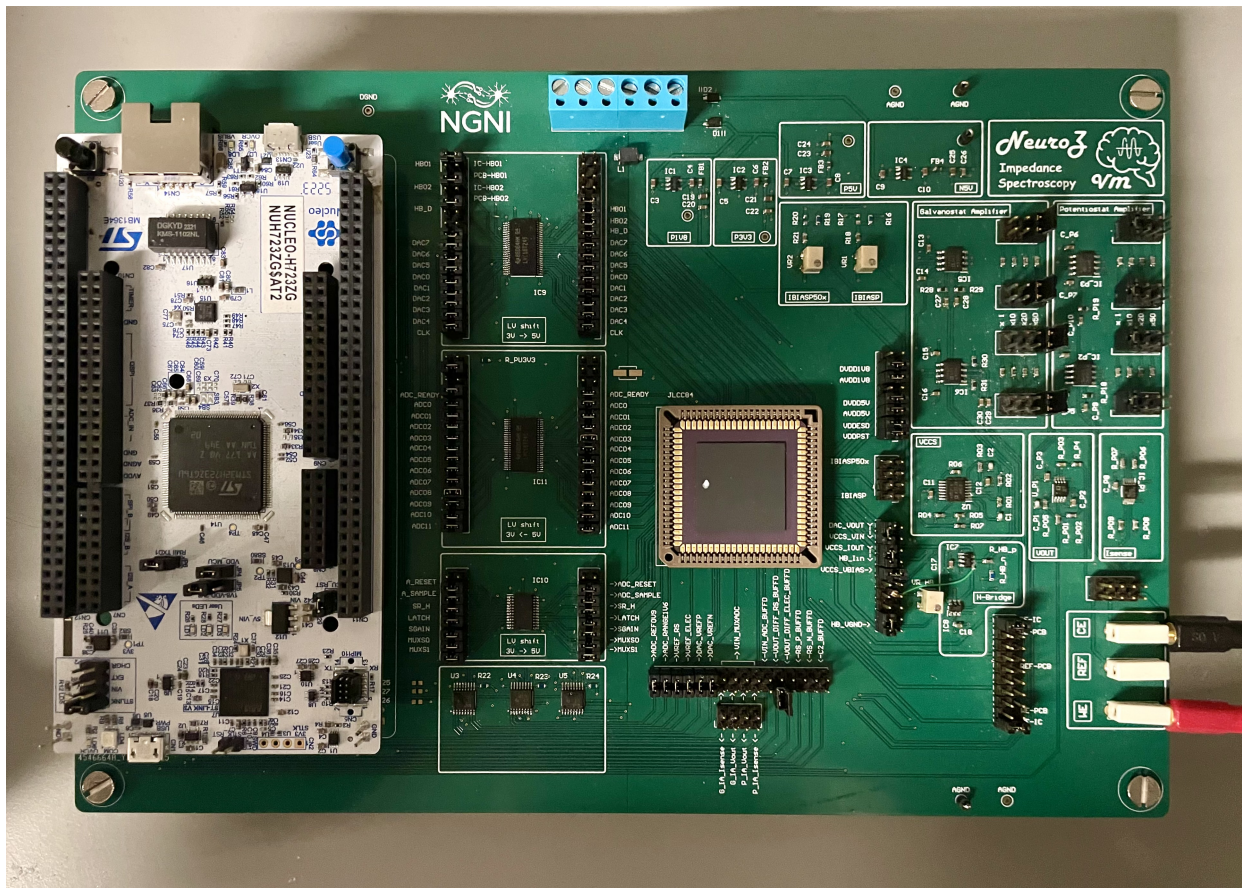


Figure 5.13: PCB testing board for impedance measurement, featuring an STM32 Nucleo H723ZG microcontroller (left), level shifters, and a socket for the packaged NeuroZ chip (centre). The board also includes LDOs, DACs for voltage references, and additional external components that will be able to replace the internal blocks of the NeuroZ chip, if needed.

and 5 V, ensuring compatibility with various devices. Low-dropout (LDO) regulators are used to generate 1.8 V for the IC digital supply, 5 V for the analogue supply, and additional supplies such as padding. Four 12-bit DACs are included to provide precise voltage references for the analogue pins, as detailed in the analogue pin table 5.4.

As the NeuroZ chip is a testing IC, it has numerous output pins dedicated to debugging. To accommodate potential issues, the board includes external components that can replace internal chip blocks, such as the VCCS, H-bridge, and programmable amplifier. Most of these external components are identical to those used in the PCB design discussed in the previous chapter. Fortunately, all chip components functioned correctly during testing, so no replacements were necessary. Consequently, the following measurement results are based entirely on the NeuroZ chip's performance.

5.8.2 Experimental and Impedance Measurement Validation

The experimental design utilised a DBS electrode model to simulate the electrode-tissue interface using RC components. The component values were consistent with those used in simulations performed on Cadence, ensuring alignment between simulated and experimental conditions. Measurements were conducted using three distinct systems: the CHI760E electrochemical workstation, the Agilent E4980A precision LCR meter, and the NeuroZ chip. These systems were employed to evaluate the impedance characteristics of the electrode model under controlled conditions.

Measurement Procedures

To enhance reliability and minimise variability, all measurements were repeated three times, and the results were averaged. Both the CHI760E and LCR meter were operated in potentiostatic mode, wherein voltage was applied, and current was measured, as well as in galvanostatic mode, wherein current was applied, and voltage was measured. A two-electrode configuration was employed for all measurements. For the CHI760E system, the reference and counter terminals were connected to form the second electrode.

The Agilent E4980A precision LCR meter recorded impedance spectra over a frequency range of 20 Hz to 100 kHz, with 20 Hz representing the lowest achievable frequency for this system. The CHI760E electrochemical workstation measured impedance in the frequency range of 1 Hz to 100 kHz in potentiostatic mode, using a 10 mV voltage excitation. In galvanostatic mode, the CHI760E measured within a frequency range of 1 Hz to 10 kHz, with the current automatically set by the system due to software limitations. Measurements using the NeuroZ chip followed comparable procedures, and the resulting data were compared to those obtained from the CHI760E and LCR meter to assess the consistency and accuracy of the NeuroZ chip.

Data Processing and Analysis

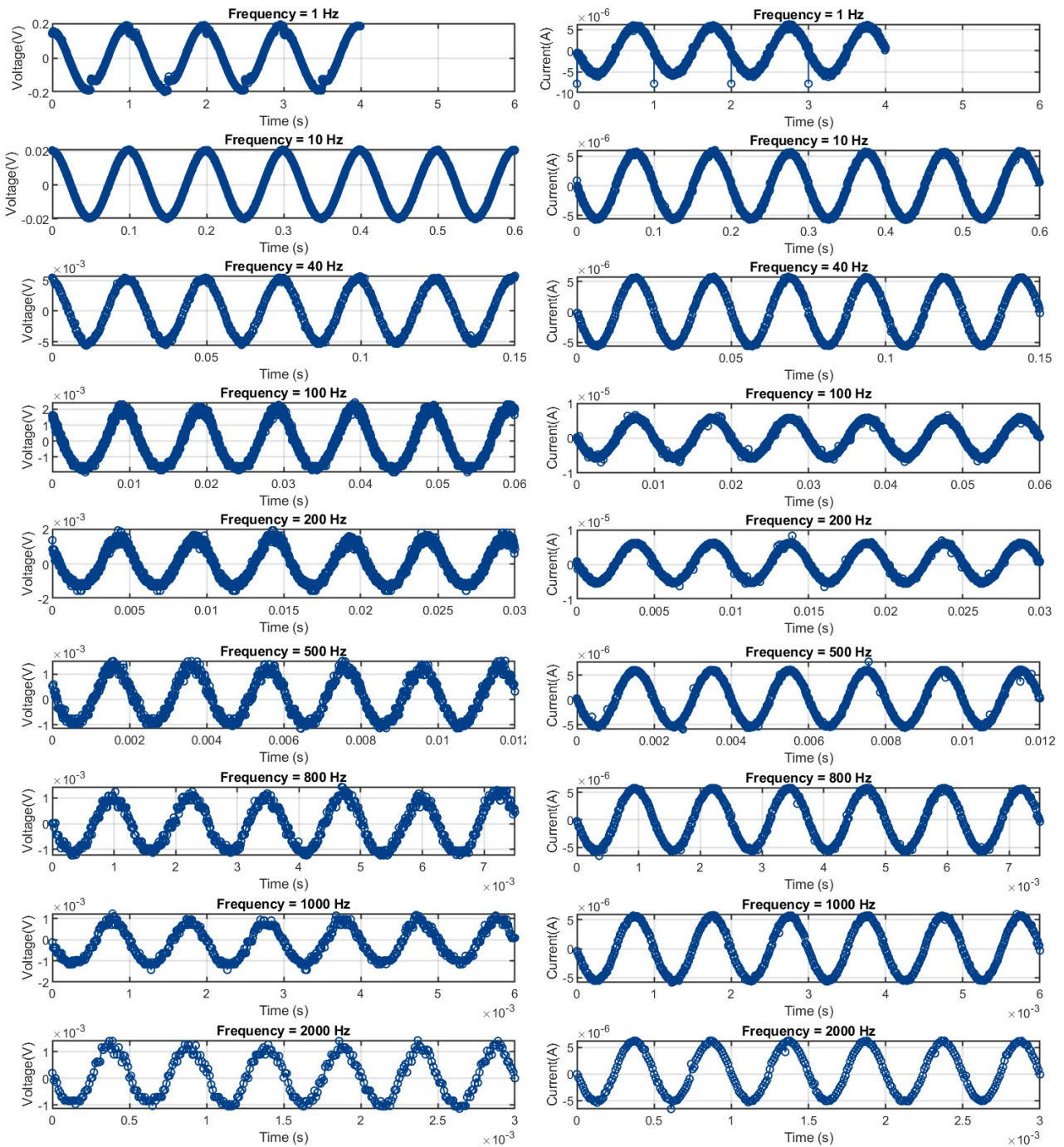
The recorded impedance magnitude data were processed using linear interpolation on a logarithmic scale to ensure uniformity in data representation. For each measurement, the data were interpolated to produce 10 evenly spaced data points per decade within the frequency range of 1 Hz to 100 kHz. These processed data points were used to plot electrochemical impedance spectroscopy (EIS) graphs, providing a clear visualisation of the impedance characteristics of the electrodes.

To evaluate measurement accuracy, the percentage error of the impedance magnitude across the entire frequency range was calculated. Additionally, the absolute error was computed and visualised through plots to offer a more granular assessment of measurement deviations. For each measurement set, the root-mean-square (RMS) error over the entire frequency range was calculated and displayed on the EIS graphs, providing a quantitative summary of the error magnitude for each system.

Neural Electrodes Validation

The same experimental setup and data analysis procedures were applied to real neural electrodes, including those used for deep brain stimulation (DBS), electrocorticography (ECoG), stereoelectroencephalography (SEEG), and cuff electrodes. All electrodes were immersed in phosphate-buffered saline (PBS) solution maintained at 37°C to replicate physiological conditions. For the real neural electrodes, only the CHI760E electrochemical workstation and NeuroZ chip were employed, as the LCR meter was excluded from this stage of the study.

The geometric surface area (GSA) and material properties of all electrodes, which are critical for interpreting impedance characteristics, are summarised in 5.7.



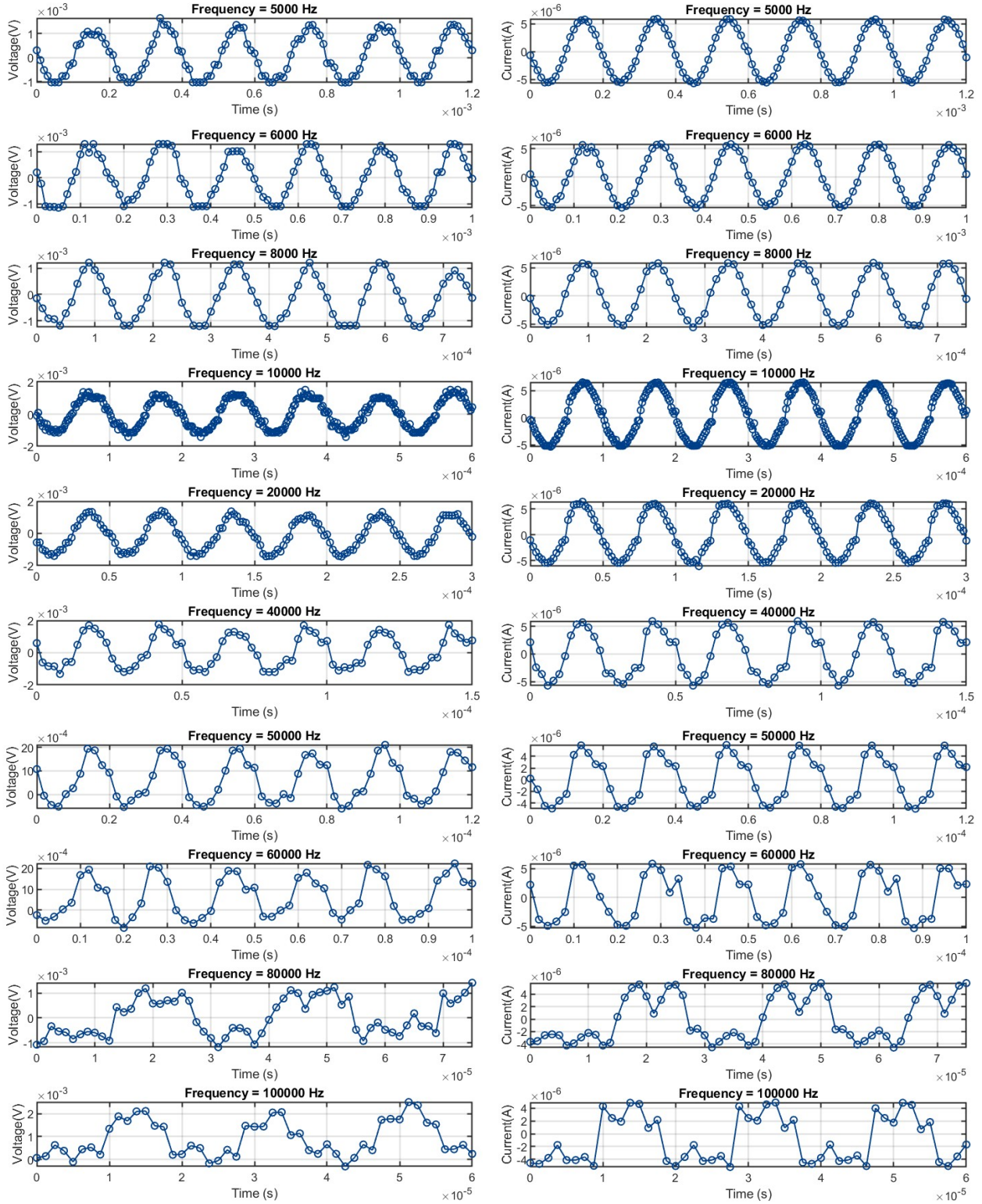


Figure 5.14: Example time-domain responses obtained from the RC-equivalent circuit model of the DBS electrode across frequencies between 1 Hz and 100 kHz. The left column shows the measured voltage waveforms, and the right column shows the corresponding current responses recorded by the impedance measurement circuit.

Electrode	Material	Tissue target	GSA (mm^2)
DBS	Pt/Ir	Brain /STN	5.98
ECoG	Pt	Brain Cortex	19.625
SEEG	Pt/Ir	Intracranial	5
Cuff	Pt/Ir	Nerve	0.675

Table 5.7: Neural electrode used in the experimental measurement and geometric surface area (GSA)

5.8.3 Single-Sine Impedance Measurement Results

RC-Equivalent Circuit Models

The NeuroZ chip was evaluated for impedance measurements using both resistive and RC-equivalent circuit models. For resistive validation, measurements were performed using resistors with nominal values of $100\ \Omega$ and $10\ \text{k}\Omega$. Their actual resistance values were first verified using an LCR meter to confirm the reference impedance. The corresponding root mean square (RMS) errors between the NeuroZ measurements and the reference values were $22.2\ \Omega$ and $431.6\ \Omega$, respectively, as shown in Figures 5.18 and 5.20.

For RC-equivalent circuit models, impedance spectra obtained from the NeuroZ chip were compared with those measured by the CHI760E and an LCR meter. Figures 5.15 present the impedance spectra and interpolated data (spanning 1 Hz to 100 kHz with 10 data points per decade), showing that the chip can capture the general frequency-dependent impedance response.

The DBS RC model tested under single-sine excitation showed that the NeuroZ chip produced percentage errors of 4.17% and 4.19% at low frequencies (1–10 Hz) when compared with the potentiostatic and galvanostatic modes of the CHI760E, respectively. In the mid-frequency range (10 Hz–10 kHz), the errors increased to 13.00% and 13.04%, while at high frequencies (10 kHz–100 kHz), the errors were 12.08% and 12.12%. The deviations observed at higher frequencies may be attributed to limitations in signal generation and acquisition. Although the ADC sampling rate of 1 MHz is theoretically sufficient for the measurement range, slight timing inconsistencies in the microcontroller’s switching control may have affected the H-bridge drive signals. These timing variations became more noticeable at excitation frequencies above

approximately 80 kHz, which may have led to waveform distortion and reduced measurement precision. The averaged RMS errors for the NeuroZ measurements were $148.80\ \Omega$ and $151.31\ \Omega$ relative to the CHI760E in potentiostatic and galvanostatic modes, respectively. The applied current waveform and the corresponding voltage measured across the DBS RC model are shown in Figure 5.14.

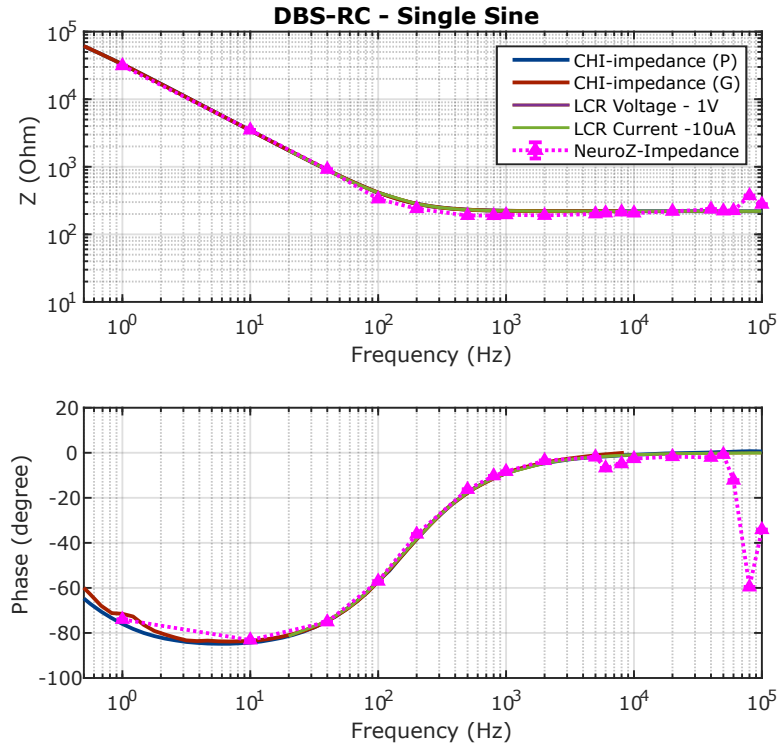
Overall, the NeuroZ chip maintained consistent impedance measurement performance between 1 Hz and 100 kHz for the DBS RC model, with percentage errors remaining below 13%. While some deviations were observed at higher frequencies, the results confirm that the system can perform impedance measurements of RC-equivalent circuit models under single-sine excitation within this error range.

Neural Electrode Measurements

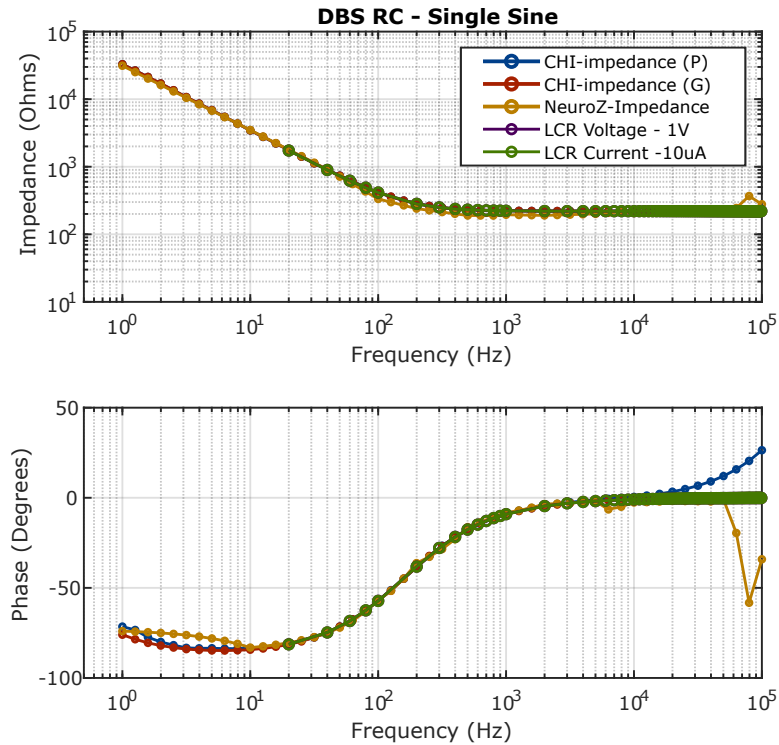
The NeuroZ chip was evaluated with various neural electrodes, including deep brain stimulation (DBS), electrocorticography (ECoG), stereoelectroencephalography (SEEG), and cuff electrodes, to assess its performance for neural interface applications. Across all electrode types, the impedance magnitude and phase spectra measured by the NeuroZ chip showed reasonable agreement with those obtained using the CHI760E system. While the CHI760E supports both potentiostatic and galvanostatic modes, the NeuroZ chip operates exclusively in a galvanostatic mode by applying a controlled current. For comparison, the results from the NeuroZ chip were evaluated against CHI760E measurements in both modes.

For DBS electrodes, the percentage errors measured by NeuroZ in the single-sine method were 19.59% at low frequencies (1–10 Hz), 6.50% in the mid-frequency range (10 Hz to 10 kHz), and 9.42% at high frequencies (10 kHz to 100 kHz) when compared to CHI760E in potentiostatic mode. Errors in comparison to the galvanostatic mode of the CHI760E were slightly higher, at 20.12%, 6.31%, and 8.29% for the same frequency ranges, respectively. The averaged RMS error was $448.65\ \Omega$ for potentiostatic mode and $493.06\ \Omega$ for galvanostatic mode.

SEEG electrodes, which have higher impedance due to their smaller surface areas, exhibited

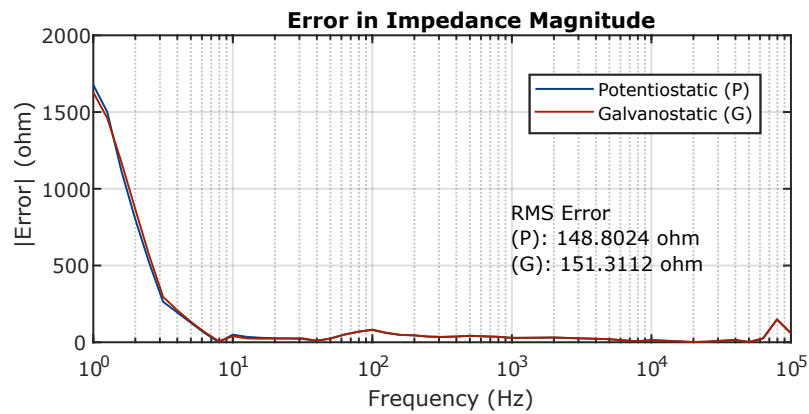


(a) EIS comparison between the measured impedance of DBS equivalent circuit model by NeuroZ, LCR meter and CHI760E. The blue curve represents CHI760E in potentiostatic mode, the red curve corresponds to CHI760E in galvanostatic mode, and the pink curve depicts data from NeuroZ. Additionally, The purple curve represents the LCR meter in potentiostatic mode, and the green curve corresponds to CHI760E in galvanostatic mode

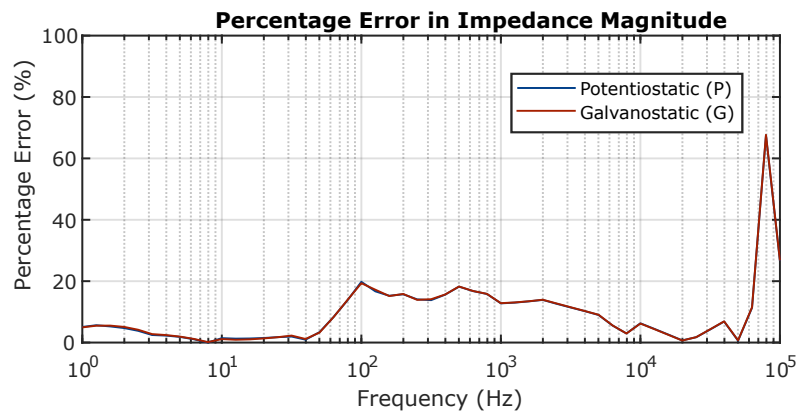


(b) EIS of the same data after interpolation from 1 Hz to 100 kHz, with 10 data points per decade.

Figure 5.15: Electrode Impedance Spectroscopy (EIS) comparison and interpolation results for DBS equivalent circuit model. Subfigures illustrate the original measured data and interpolated data for consistent frequency spacing.

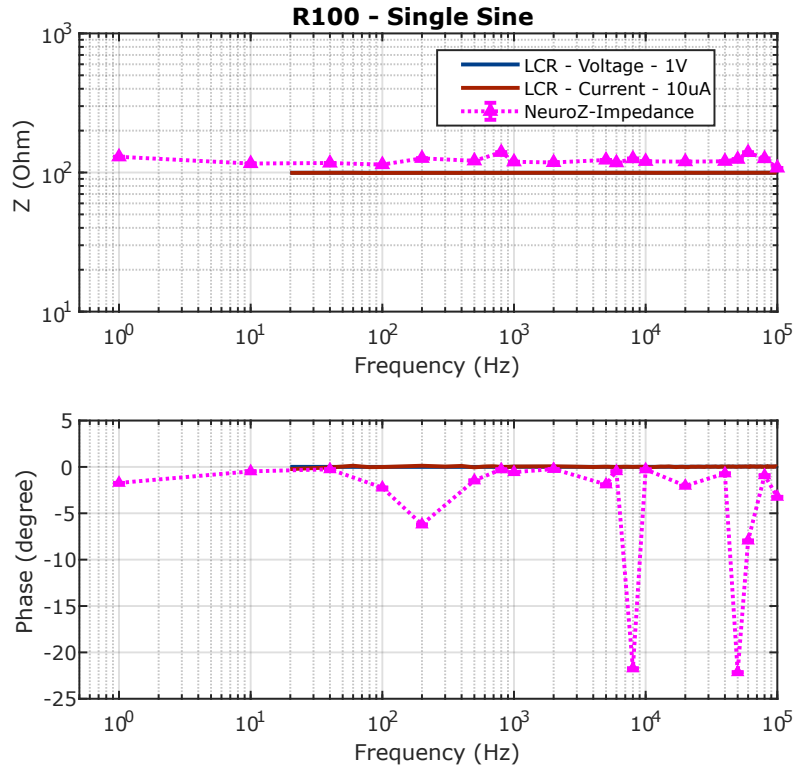


(a) Error in ohms. RMS error of the results is 148.8 Ω for the potentiostatic mode and 151.31 Ω for galvanostatic mode

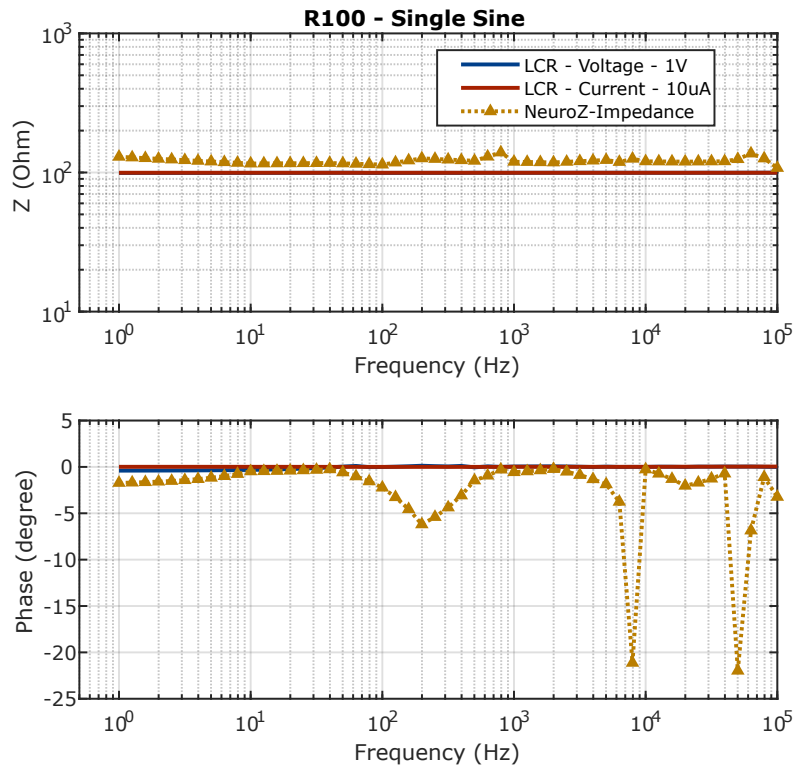


(b) Error in percentage.

Figure 5.16: Error analysis of measured EIS data for DBS equivalent circuit model. Subfigures show the error in absolute ohms and the percentage error between NeuroZ and CHI760E measurements.

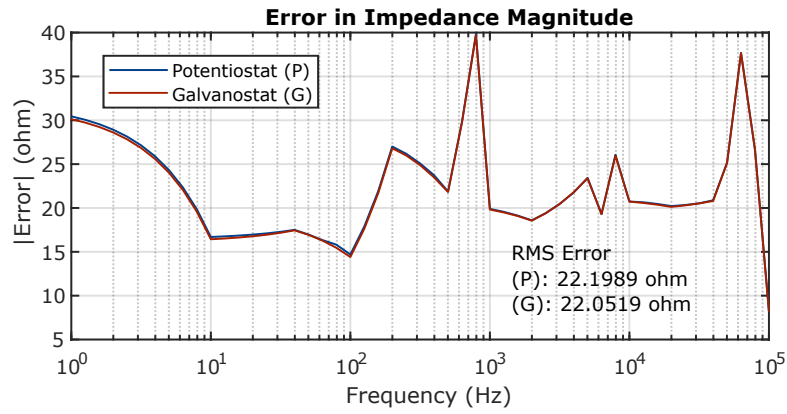


(a) EIS comparison between measured impedance of $100\ \Omega$ resistor by NeuroZ and CHI760E. The blue curve represents LCR meter in potentiostatic mode, the red curve corresponds to the LCR meter in galvanostatic mode, and the pink curve depicts data from NeuroZ.

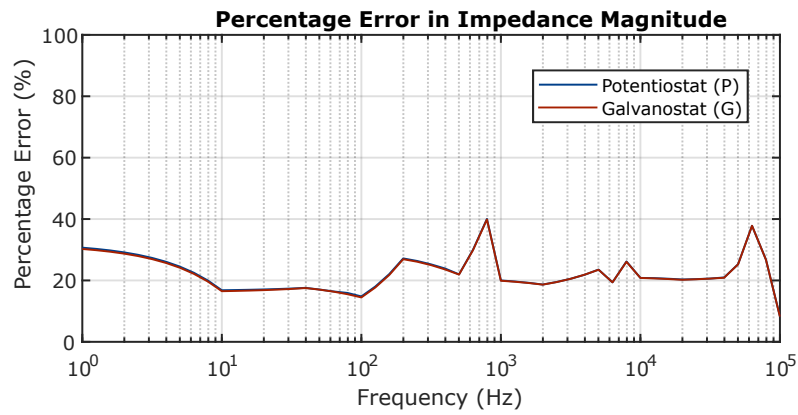


(b) EIS of the $100\ \Omega$ data after interpolation from 1 Hz to 100 kHz, with 10 data points per decade.

Figure 5.17: Electrode Impedance Spectroscopy (EIS) comparison and interpolation results for $100\ \Omega$. Subfigures illustrate the original measured data and interpolated data for consistent frequency spacing.

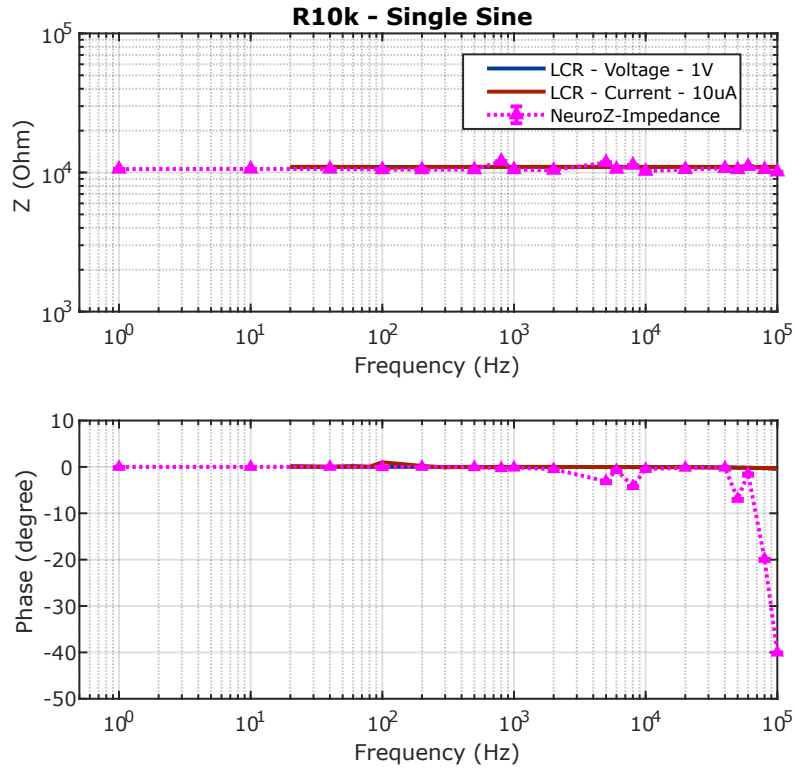


(a) Error in ohms. RMS error of the results is 22.2Ω for the potentiostatic mode and 22.05Ω for galvanostatic mode.

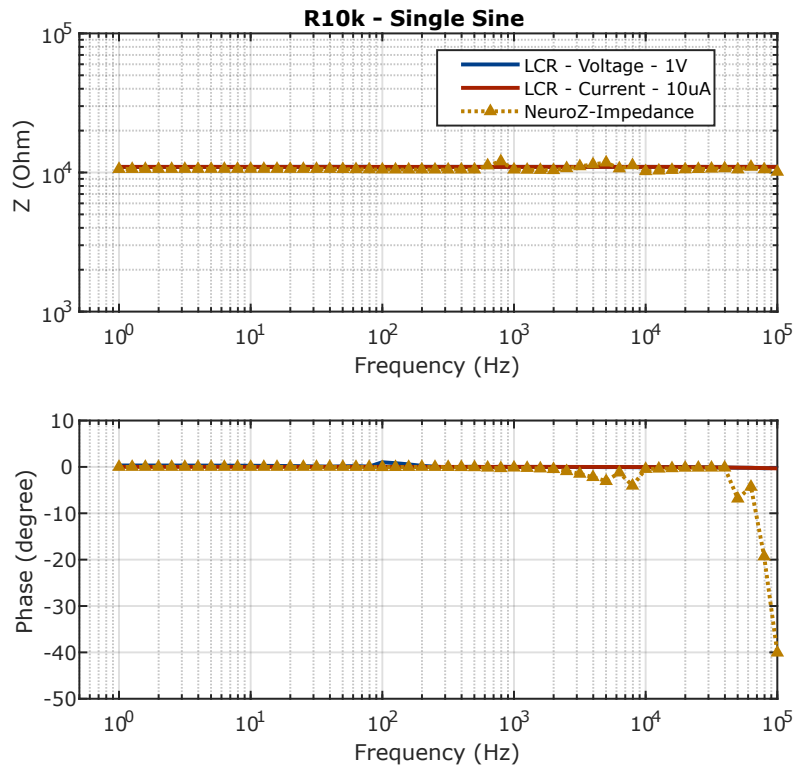


(b) Error in percentage.

Figure 5.18: Error analysis of measured EIS data for 100Ω resistor. Subfigures show the error in absolute ohms and the percentage error between NeuroZ and LCR meter measurements.

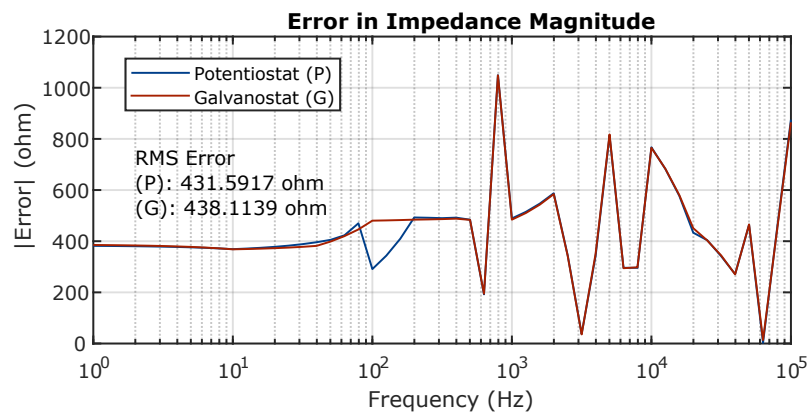


(a) EIS comparison between measured impedance of $10\text{ k}\Omega$ resistor by NeuroZ and CHI760E. The blue curve represents LCR meter in potentiostatic mode, the red curve corresponds to the LCR meter in galvanostatic mode, and the pink curve depicts data from NeuroZ.

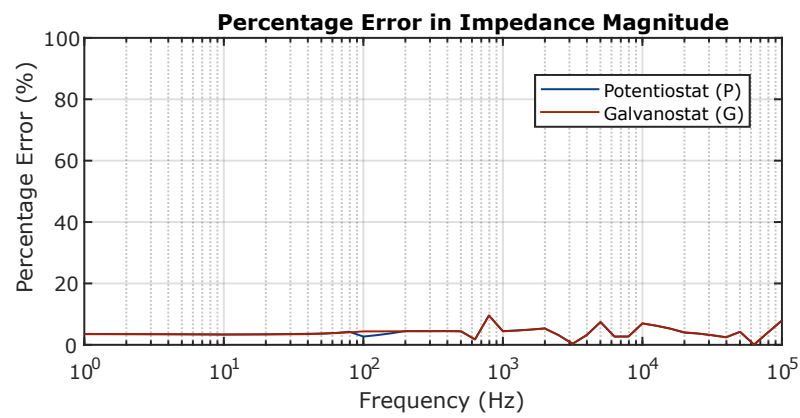


(b) EIS of the $10\text{ k}\Omega$ data after interpolation from 1 Hz to 100 kHz, with 10 data points per decade.

Figure 5.19: Electrode Impedance Spectroscopy (EIS) comparison and interpolation results for $10\text{ k}\Omega$. Subfigures illustrate the original measured data and interpolated data for consistent frequency spacing.



(a) Error in ohms. RMS error of the results is 431.59Ω for the potentiostatic mode and 438.11Ω for the galvanostatic mode.



(b) Error in percentage.

Figure 5.20: Error analysis of measured EIS data for $10k\Omega$ resistor. Subfigures show the error in absolute ohms and the percentage error between NeuroZ and LCR meter measurements.

larger percentage errors in the single-sine method. For the NeuroZ chip, the percentage errors in comparison to the CHI760E potentiostatic mode were 44.62%, 13.86%, and 64.53% in the low, mid, and high-frequency ranges, respectively. The galvanostatic comparison yielded errors of 47.82%, 14.12%, and 61.33% for the respective frequency ranges. The averaged RMS error for SEEG electrodes was $2086.37\ \Omega$ (potentiostatic) and $2436.37\ \Omega$ (galvanostatic), reflecting increased variability due to the high impedance of these electrodes.

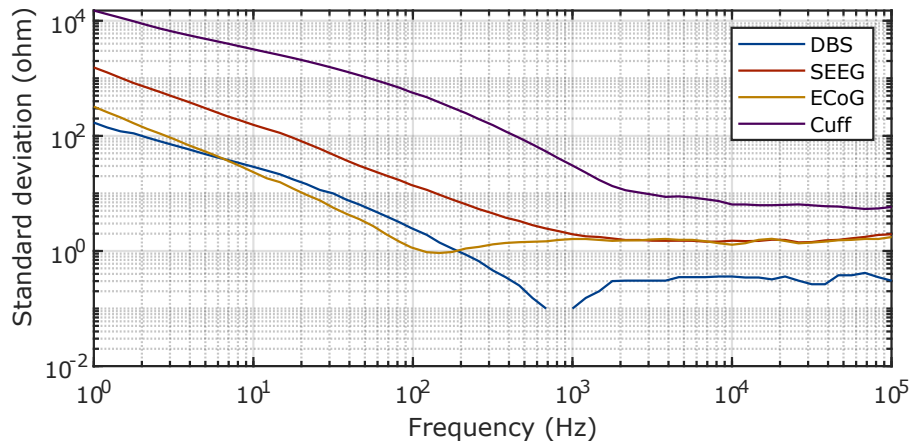
For ECoG electrodes, which are characterised by their larger surface areas and lower impedance, the NeuroZ chip demonstrated better accuracy. The percentage errors were 18.95%, 7.95%, and 103.32% in potentiostatic mode for low, mid, and high frequencies, respectively. Similarly, the errors in galvanostatic mode were 17.53%, 7.32%, and 98.35%. The averaged RMS errors were $599.23\ \Omega$ (potentiostatic) and $558.95\ \Omega$ (galvanostatic).

Cuff electrodes, which exhibited the highest impedance among the tested electrodes, showed larger errors in the single-sine method. The percentage errors were 21.09%, 14.30%, and 18.52% in potentiostatic mode for low, mid, and high frequencies, respectively. Errors in galvanostatic mode were higher at 67.56%, 20.11%, and 15.54% for the respective frequency ranges. The averaged RMS errors were $3161.77\ \Omega$ (potentiostatic) and $6960.22\ \Omega$ (galvanostatic), indicating greater variability in measurements for these high-impedance electrodes.

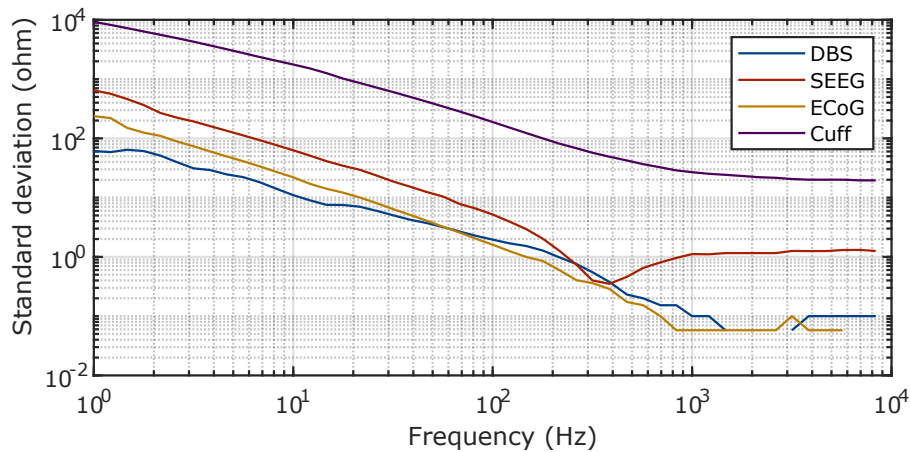
According to the standard deviation (SD) analysis of the CHI760E measurements shown in Figure 5.21, variability was highest at low frequencies (1–10 Hz) across all electrode types. Among the tested electrodes, cuff electrodes exhibited the greatest SD across the entire frequency range, followed by SEEG electrodes. This increased variability in cuff electrodes is likely attributable to their condition during testing. The cuff electrode had been previously used, and visual inspection suggested partial delamination between the silicone layer and the metal surface. Such delamination can modify the effective active area exposed to the electrolyte, resulting in variations in impedance. This effect is consistent with the higher standard deviation values observed in the measurements.

Overall, the NeuroZ chip was evaluated for neural electrode impedance measurements using the single-sine method. Errors were generally higher for SEEG and cuff electrodes due to their

high-impedance characteristics, whereas the results for DBS and ECoG electrodes remained within 20% across most frequency ranges. The mid-frequency band (10 Hz–10 kHz) consistently exhibited errors below 20% for all electrode types.

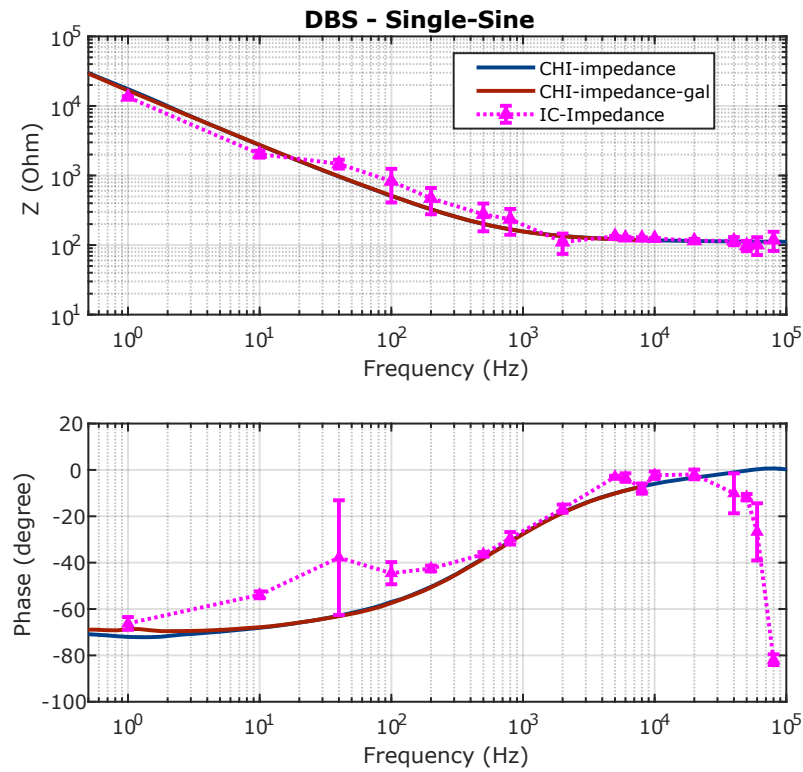


(a)

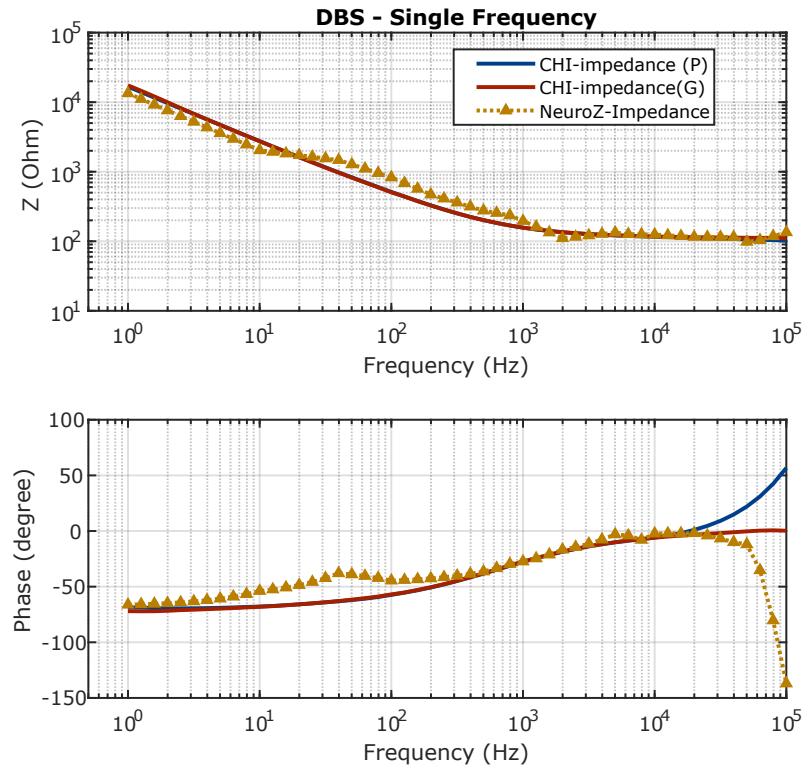


(b)

Figure 5.21: Standard deviation (SD) of impedance measurements across the frequency spectrum (1 Hz to 100 kHz) obtained using the CHI760E system. (a) Potentiostatic mode: The SD is higher at low frequencies (1–10 Hz) for all electrode types, reflecting increased variability in this range. (b) Galvanostatic mode: Similar trends are observed, with the cuff electrode exhibiting the highest SD across the frequency spectrum in both modes.

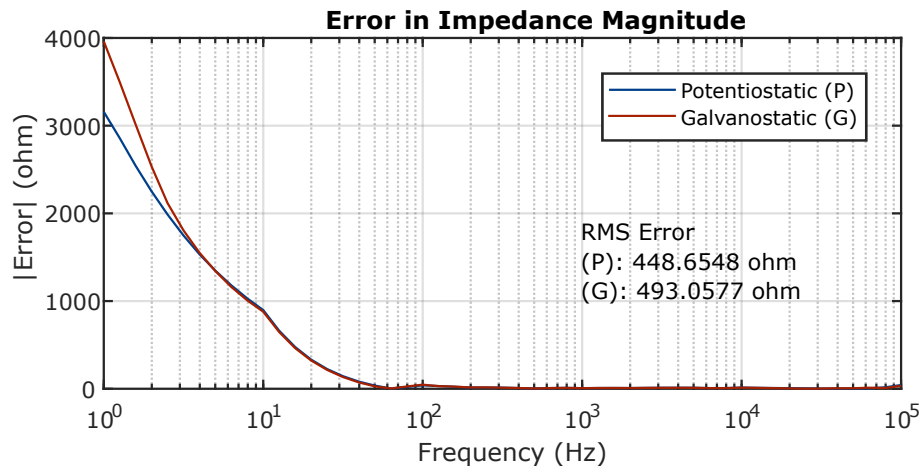


(a) EIS comparison between the measured impedance of DBS electrodes by NeuroZ and CHI760E. The blue curve represents CHI760E in potentiostatic mode, the red curve corresponds to CHI760E in galvanostatic mode, and the pink curve depicts data from NeuroZ.

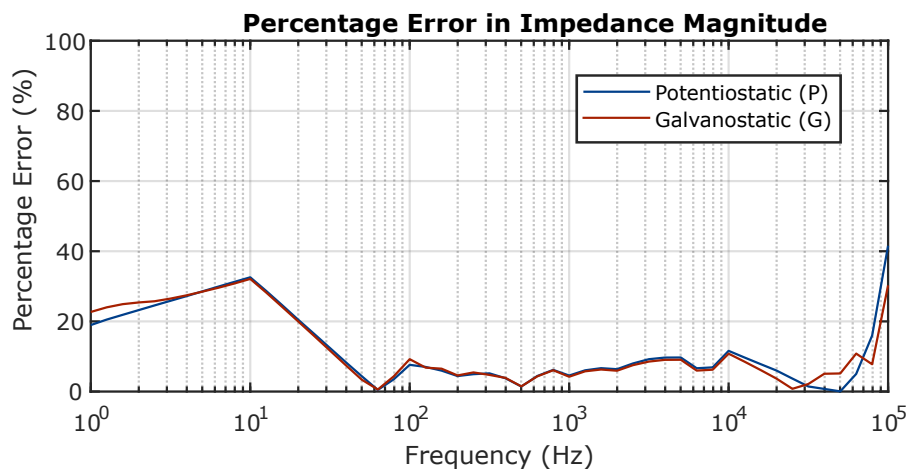


(b) EIS of the DBS data after interpolation from 1 Hz to 100 kHz, with 10 data points per decade.

Figure 5.22: Electrode Impedance Spectroscopy (EIS) comparison and interpolation results for DBS electrodes. Subfigures illustrate the original measured data and interpolated data for consistent frequency spacing.



(a) Error in ohms. RMS error of the results is 448.65 Ω for the potentiostatic mode and 493.06 Ω for NeuroZ.



(b) Error in percentage.

Figure 5.23: Error analysis of measured EIS data for DBS electrodes. Subfigures show the error in absolute ohms and the percentage error between NeuroZ and CHI760E measurements.

5.9 Multi-Sine Impedance Measurement

The integration of the multi-sine method into the impedance measurement waveform offers a method to enhance the efficiency of electrode-tissue characterisation in bidirectional neural interfaces. The primary objective is to reduce the time required for impedance measurement, thereby minimising disruptions to neuromodulation activity. To illustrate this advantage, the measurement duration of the multi-sine method was compared with that of the conventional single-sine sweep using the frequency and sampling configurations described in this work.

The single-sine method sequentially measured 19 frequency points from 1 Hz to 100 kHz, using sampling rates of 5 kHz (EIS frequencies less than 800 Hz), 100 kHz (EIS frequencies between 1–10 kHz), and 800 kHz (EIS frequencies between 10–100 kHz). Each frequency was measured for at least ten waveform cycles or until the 20000-sample buffer was filled, whichever was longer. Considering that a single ADC channel was time-multiplexed to acquire both the voltage across the DUT and the voltage across the 10 k Ω reference resistor, the total acquisition time for all frequencies was approximately 42 s.

In contrast, the multi-sine method employed four frequency patterns—{1, 3, 7 Hz}, {10, 30, 70 Hz}, {100, 300, 700 Hz}, and {10 k, 30 k, 70 k Hz}—each sampled at a rate determined by its highest tone. Each pattern was captured for at least ten cycles of its lowest frequency. The total acquisition time across all patterns was approximately 22 s, representing roughly a twofold reduction in measurement time compared to the single-sine sweep, while maintaining comparable impedance accuracy across the same frequency range. These times refer only to the waveform capture duration and do not include additional overheads such as configuration, settling, or data transfer.

This section presents the design, implementation, and testing of the proposed multi-sine waveforms for impedance characterisation.

5.9.1 Waveform Design and Selection

The frequency components integrated into the waveforms were strategically chosen to minimise harmonic interference while providing broad spectral coverage. Prior recommendations suggest limiting the number of combined frequencies to a maximum of ten[85]. For this study, a more conservative approach was adopted by combining only three frequencies per decade. Each frequency was selected as a prime number, further reducing harmonic overlap and enhancing measurement reliability.

The selected frequency sets included:

- **Pattern 1:** {1 Hz, 3 Hz, 7 Hz}
- **Pattern 2:** {10 Hz, 30 Hz, 70 Hz}
- **Pattern 3:** {100 Hz, 300 Hz, 700 Hz}
- **Pattern 4:** {10 kHz, 30 kHz, 70 kHz}

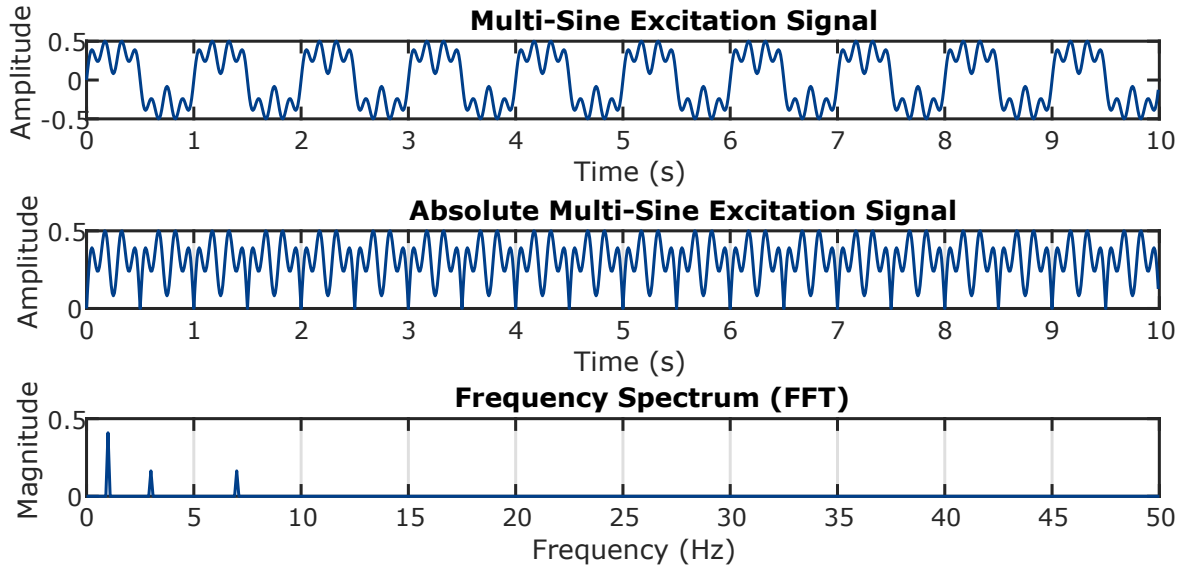


Figure 5.24: Example integrated multi-sine excitation waveform showing the combined signal, its absolute amplitude, and the frequency spectrum (FFT) used for impedance characterisation.

Due to the circuit design of the NeuroZ chip, which incorporates an H-bridge for switching the polarity of the injected current, the lowest frequency in each range was assigned the highest

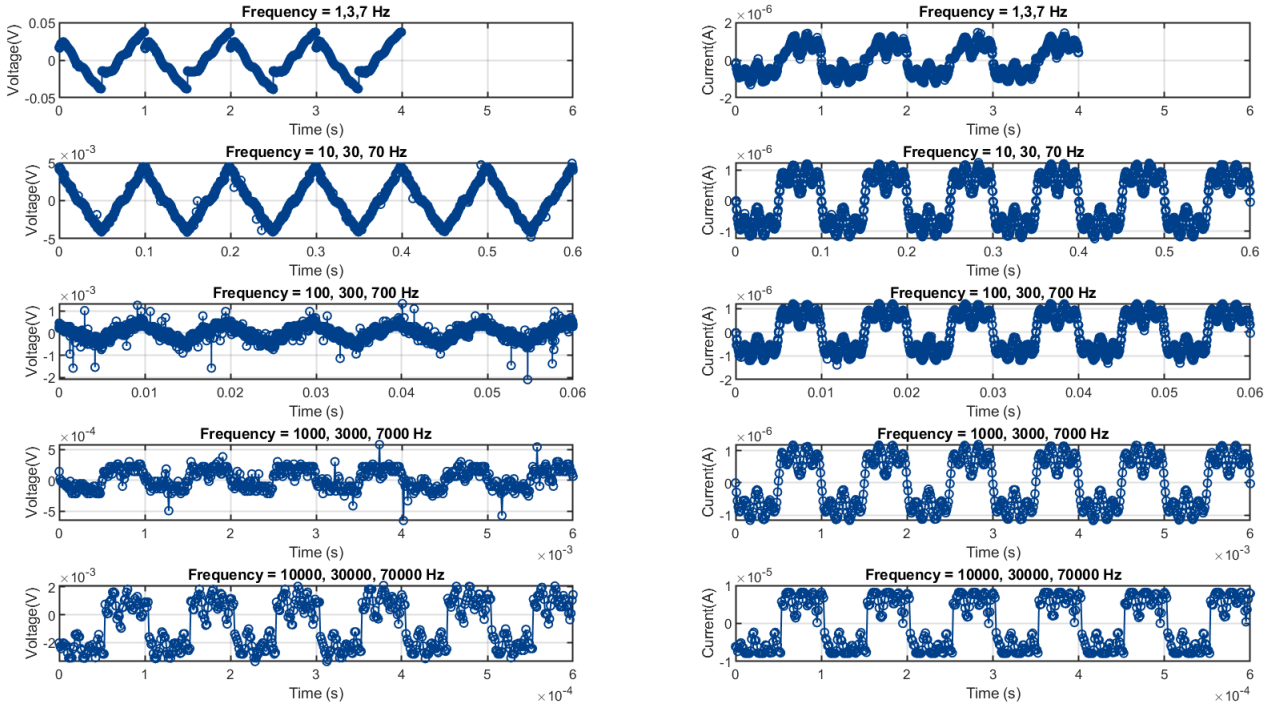


Figure 5.25: Example time-domain responses obtained from the RC-equivalent circuit model of the DBS electrode using a multi-sine excitation waveform. The left column shows the measured voltage signals, and the right column shows the corresponding current responses sensed by the internal reference resistor

amplitude. The amplitude ratios between frequencies were set at 5:2:2, and the combined waveform was normalised to an overall amplitude of $5\text{ }\mu\text{A}$. This normalisation ensures consistency across measurements and compatibility with the system's current injection capabilities.

5.9.2 RC Component Testing

To evaluate the performance of the designed multi-sine excitation patterns, tests were conducted on an RC-equivalent circuit representing the impedance characteristics of a deep brain stimulation (DBS) electrode model. The impedance spectra obtained using the multi-sine method were compared with those measured by the CHI760E electrochemical workstation. As shown in Figure 5.26, the results indicate that the proposed approach can reproduce impedance spectra comparable to those obtained from the reference system.

5.9.3 Experimental Setup

The experimental setup employed a DBS electrode model to simulate the electrode–tissue interface. For consistency, the same measurement configuration described in Section 5.8.3 was used, identical to that adopted for the single-sine experiments. Measurements were performed across multiple electrode types, including those used for deep brain stimulation (DBS) and electrocorticography (ECoG). The impedance characteristics were recorded for each frequency set using a multi-sine excitation waveform.

5.9.4 Multi-Sine Impedance Measurement Results

DBS equivalent circuit model

The NeuroZ chip was evaluated using the DBS-RC model under multi-sine testing conditions. The impedance measurements were compared to the CHI760E system, which served as the benchmark. Across all frequency ranges, the NeuroZ chip demonstrated consistent performance, though errors were influenced by frequency-dependent limitations. In the mid-frequency range (10 Hz to 10 kHz), the percentage errors were 9.89% and 9.97% compared to the CHI760E in potentiostatic and galvanostatic modes, respectively (Figure 5.26). At low frequencies (1–10 Hz), errors were higher at 9.59% and 9.61% for potentiostatic and galvanostatic modes, respectively, reflecting interpolation challenges inherent to the lower frequency range. At high frequencies (10 kHz to 100 kHz), the errors increased to 20.11% and 20.21% for potentiostatic and galvanostatic modes, respectively (Figure 5.27). The averaged RMS errors for the DBS-RC multi-sine tests were $487.41\ \Omega$ in potentiostatic mode and $489.42\ \Omega$ in galvanostatic mode. These results demonstrate that the NeuroZ chip performs reasonably well in multi-sine measurements, particularly in the mid-frequency range, where it achieves the best accuracy.

Neural Electrodes Multi-Sine Measurements

The performance of the NeuroZ chip was assessed using various neural electrodes, including DBS, ECoG, SEEG, and cuff electrodes, under multi-sine testing conditions. For DBS electrodes, percentage errors in the mid-frequency range (10 Hz to 10 kHz) were 33.00% and 32.76% for potentiostatic and galvanostatic modes, respectively, with averaged RMS errors of 535.22 Ω and 581.88 Ω (Figure 5.28, Figure 5.29). Low-frequency errors (1–10 Hz) were 16.97% (potentiostatic) and 17.96% (galvanostatic), while high-frequency errors (10 kHz to 100 kHz) were 22.95% and 18.09%.

SEEG electrodes exhibited higher variability, with mid-frequency errors of 16.18% and 15.56% for potentiostatic and galvanostatic modes, respectively. The averaged RMS errors were 2137.57 Ω (potentiostatic) and 2486.72 Ω (galvanostatic), reflecting the impact of high impedance on measurement consistency (Figure A.7, Figure A.8). Low-frequency errors were 43.83% (potentiostatic) and 47.02% (galvanostatic), while high-frequency errors were 11.24% and 9.93%.

ECoG electrodes, characterised by lower impedance, demonstrated improved accuracy in multi-sine testing. Mid-frequency errors were 11.83% and 11.16% for potentiostatic and galvanostatic modes, with RMS errors of 261.53 Ω and 230.56 Ω (Figure A.9, Figure A.10). Errors at low and high frequencies were 6.87% and 6.49%, and 8.75% and 10.70%, respectively.

Cuff electrodes, which exhibited the highest impedance among the tested electrodes, showed the largest errors. Mid-frequency errors were 59.81% and 74.51% for potentiostatic and galvanostatic modes, respectively, with RMS errors of 4483.62 Ω and 1801.91 Ω (Figure A.11, Figure A.12). Errors at low frequencies were 24.47% and 16.74%, and high-frequency errors were 56.01% and 50.90%.

The NeuroZ chip exhibited multi-sine measurement performance across all electrode types between 1 Hz and 100 kHz. Among the tested electrodes, ECoG electrodes exhibited the lowest percentage errors, while DBS electrodes showed moderate deviations compared with the reference systems. SEEG and cuff electrodes presented larger variations, which may be attributed to their higher impedance and sensitivity to parasitic effects. The mid-frequency

range (10 Hz–10 kHz) consistently resulted in lower errors across all electrodes. Although the multi-sine method produced slightly higher errors than the single-sine approach, it considerably reduced the overall measurement time. This trade-off between accuracy and speed suggests that the multi-sine excitation approach can be potentially applied in scenarios where rapid impedance characterisation is required, such as during neural interface calibration or real-time monitoring in neuromodulation experiments.

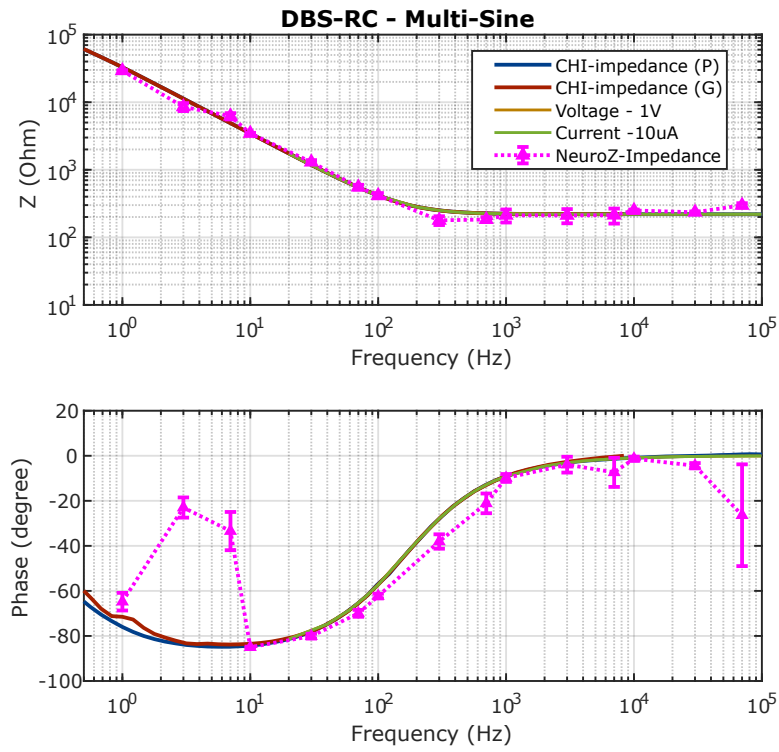
5.9.5 Expanded Multi-Sine Frequency Waveform Design

To further optimise the impedance measurement process, the two-decade frequency range of multi-sine excitation signals was tested. This approach combines multiple frequencies across two decades, allowing simultaneous characterisation over a broader spectrum. The frequency set was carefully chosen to include prime numbers, reducing harmonic interference in measurements.

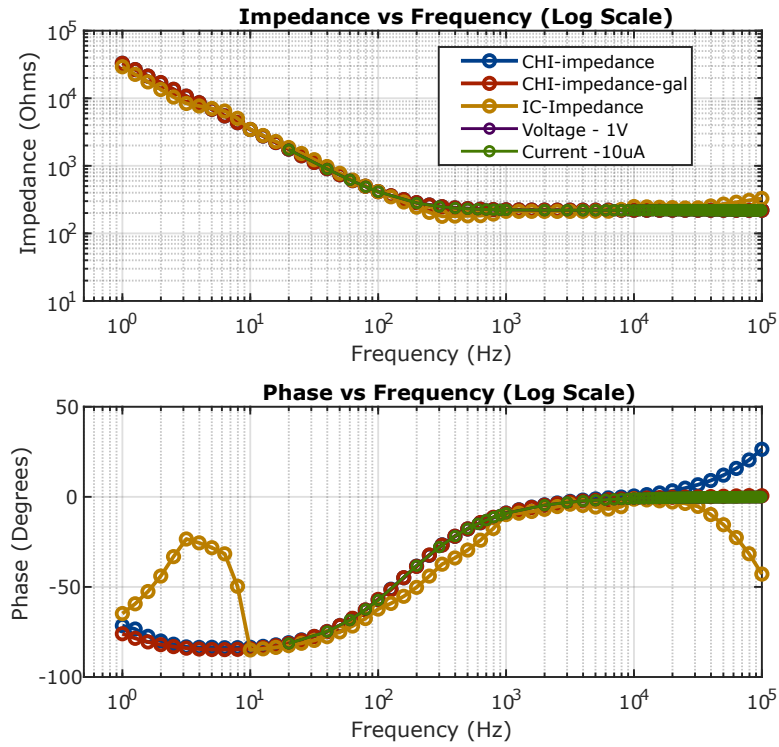
The selected frequency sets included:

- **Pattern 1:** {1 Hz, 3 Hz, 5 Hz, 7 Hz, 10 Hz, 37 Hz, 70 Hz}
- **Pattern 2:** {10 Hz, 30 Hz, 50 Hz, 70 Hz, 100 Hz, 370 Hz, 700 Hz}
- **Pattern 3:** {100 Hz, 300 Hz, 500 Hz, 700 Hz, 1 kHz, 370 kHz, 700 kHz}
- **Pattern 4:** {1 kHz, 3 kHz, 5 kHz, 7 kHz, 10 kHz, 37 kHz, 70 kHz}

In this configuration, the lowest frequency in the range was assigned the highest amplitude, with amplitude ratios set at 6:2:2:2:2:1:1. The waveform was normalised to maintain a peak amplitude of 5 μ A, ensuring compatibility with the NeuroZ system's current injection design. This configuration enables simultaneous measurement across a two-decade frequency range, reducing the total acquisition time by approximately 0.1 s compared with the single-decade multi-sine test. The expanded multi-sine frequency waveform was investigated to explore potential optimisation strategies for future implementations. In particular, combining wider frequency bands within a single acquisition may help minimise overall measurement overheads, such as configuration and data-transfer delays.

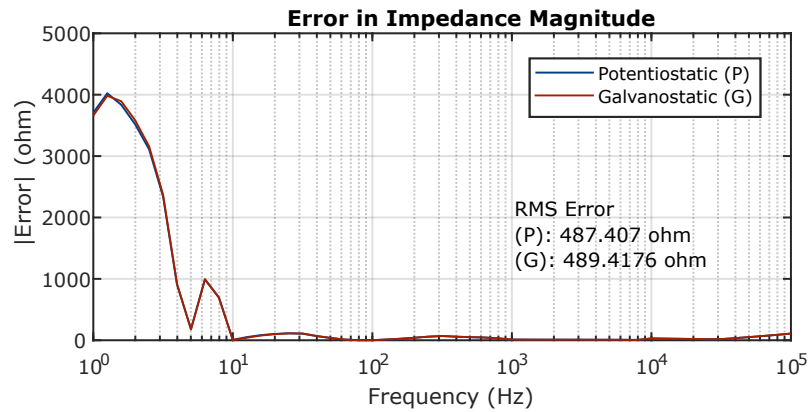


(a) EIS comparison between the measured impedance of DBS equivalent circuit model by NeuroZ, LCR meter and CHI760E. The blue curve represents CHI760E in potentiostatic mode, the red curve corresponds to CHI760E in galvanostatic mode, and the pink curve depicts data from NeuroZ with multi-sine waveform.

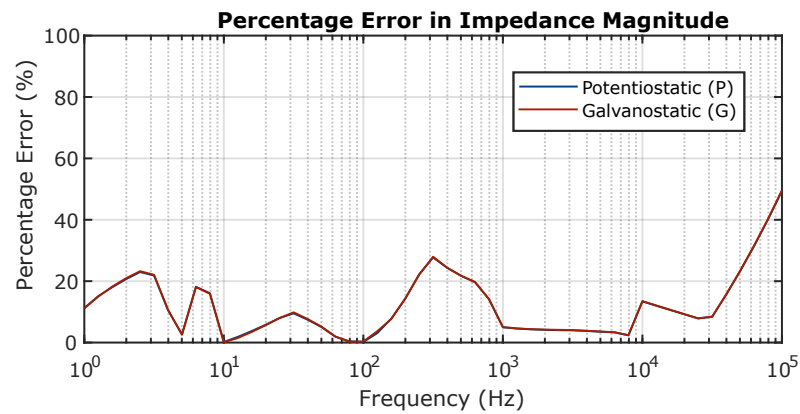


(b) EIS of the DBS circuit model data after interpolation from 1 Hz to 100 kHz, with 10 data points per decade.

Figure 5.26: Electrode Impedance Spectroscopy (EIS) comparison and interpolation results for DBS equivalent circuit model. Subfigures illustrate the original measured data and interpolated data for consistent frequency spacing.

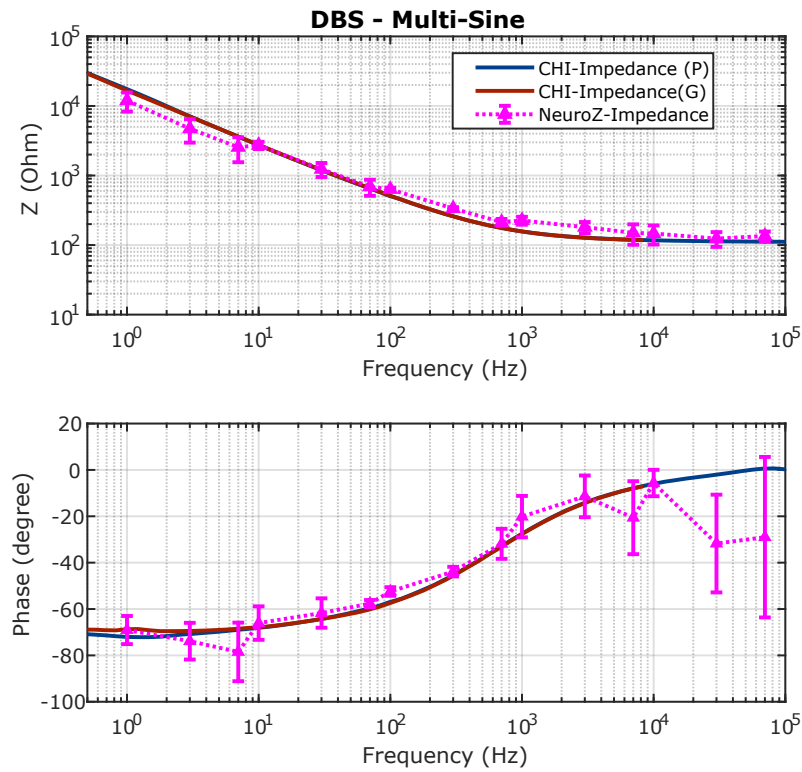


(a) Error in ohms. RMS error of the results is 487.4 Ω for the potentiostatic mode and 489.41 Ω for galvanostatic mode.

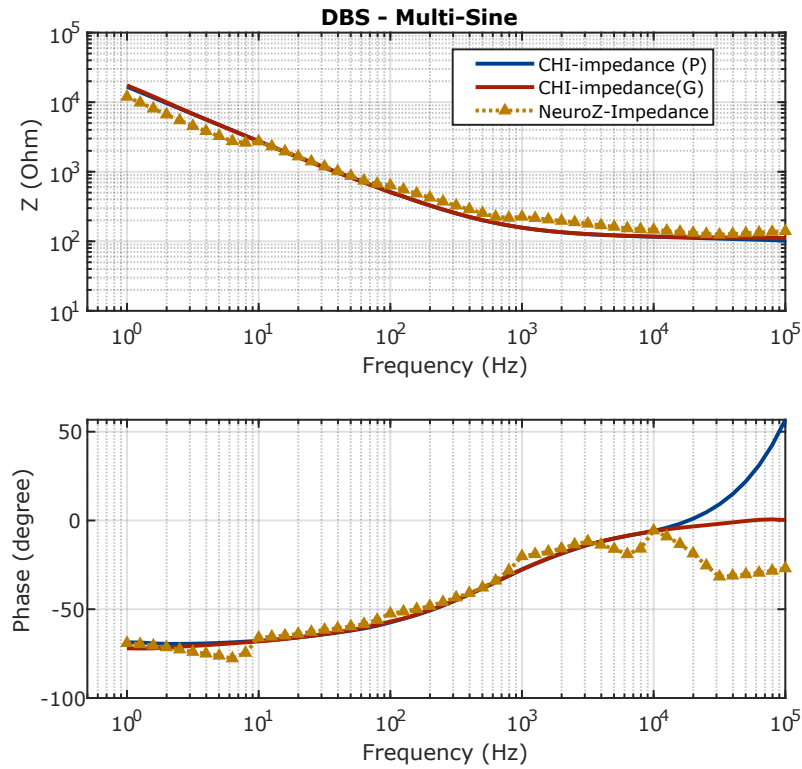


(b) Error in percentage.

Figure 5.27: Error analysis of measured EIS data for DBS equivalent circuit model. Subfigures show the error in absolute ohms and the percentage error between NeuroZ with multi-sine waveform and CHI760E measurements.

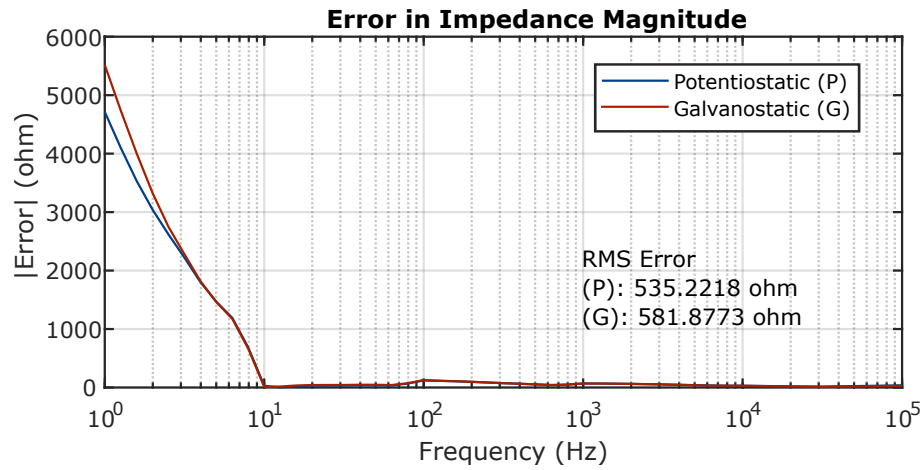


(a) EIS comparison between the measured impedance of DBS electrodes by NeuroZ with multi-sine waveform and CHI760E. The blue curve represents CHI760E in potentiostatic mode, the red curve corresponds to CHI760E in galvanostatic mode, and the pink curve depicts data from NeuroZ.

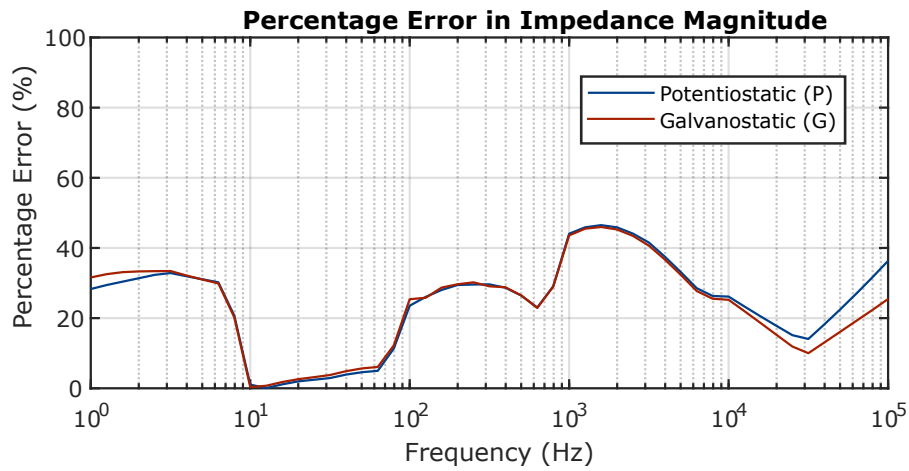


(b) EIS of the DBS data after interpolation from 1 Hz to 100 kHz, with 10 data points per decade.

Figure 5.28: Electrode Impedance Spectroscopy (EIS) comparison and interpolation results for DBS electrodes. Subfigures illustrate the original measured data and interpolated data for consistent frequency spacing.



(a) Error in ohms. RMS error of the results is 535.22Ω for the potentiostatic mode and 581.87Ω for galvanostatic mode.



(b) Error in percentage.

Figure 5.29: Error analysis of measured EIS data for DBS electrodes. Subfigures show the error in absolute ohms and the percentage error between NeuroZ with multi-sine waveform and CHI760E measurements.

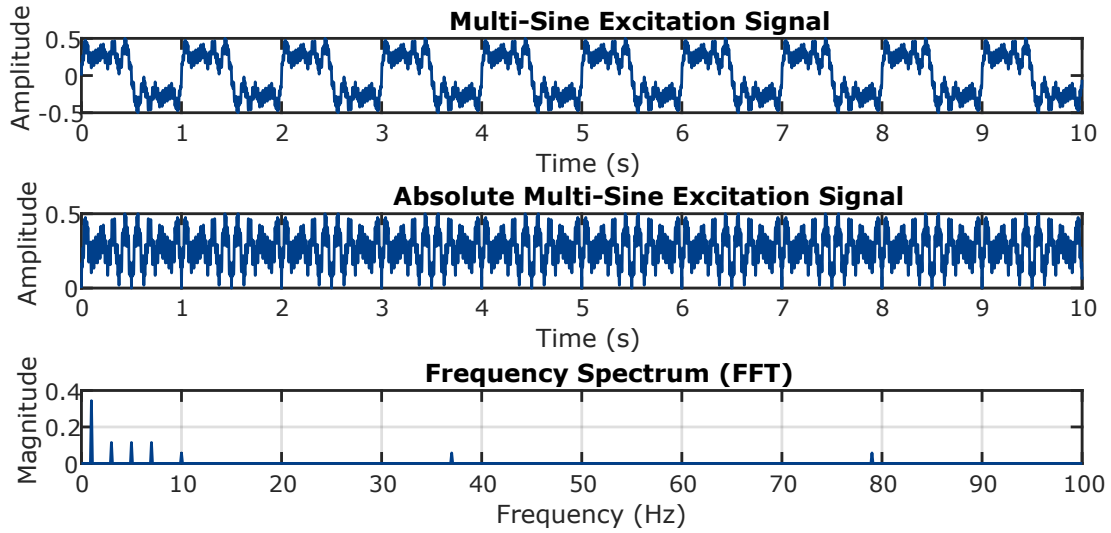


Figure 5.30: Two-decade multi-sine excitation waveform showing the combined signal, its absolute amplitude, and the frequency spectrum (FFT) used for impedance characterisation.

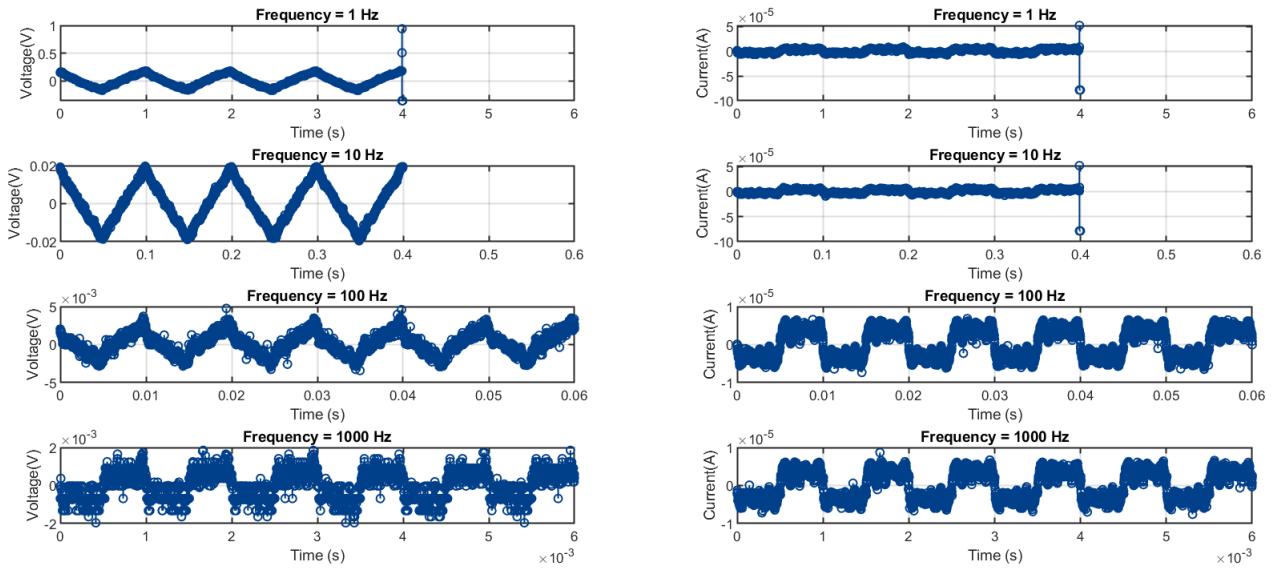
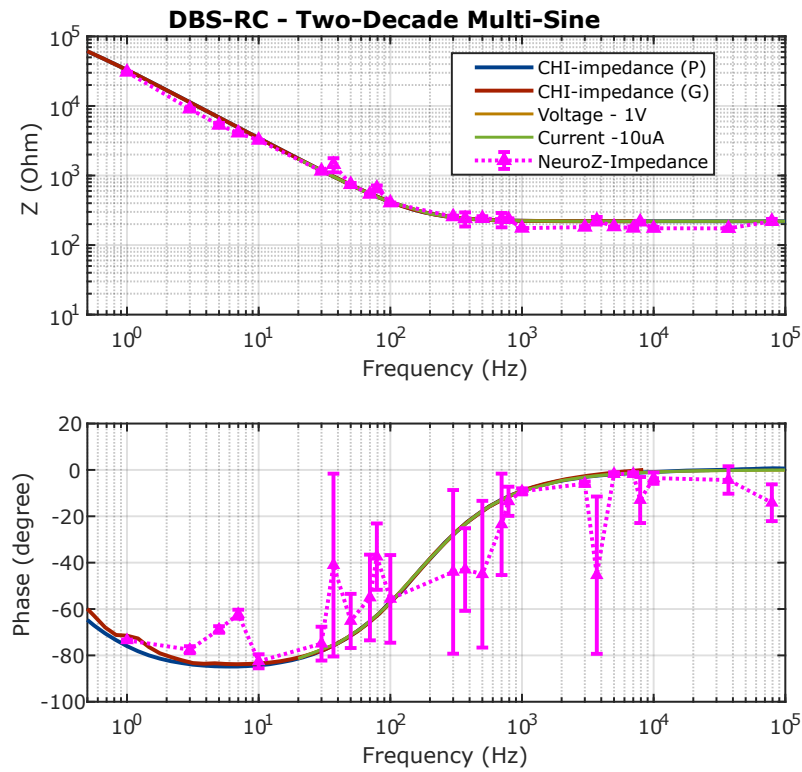
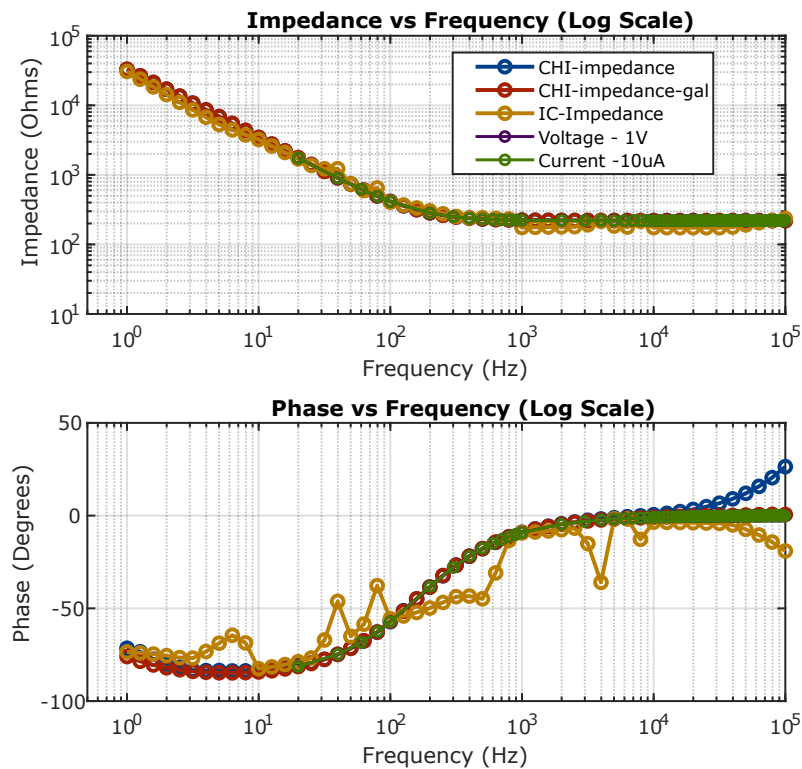


Figure 5.31: Example time-domain responses obtained from the RC-equivalent circuit model of DBS electrode using two-decade multi-sine excitation waveform. The left column shows the measured voltage signals, and the right column shows the corresponding current responses recorded by the impedance measurement circuit

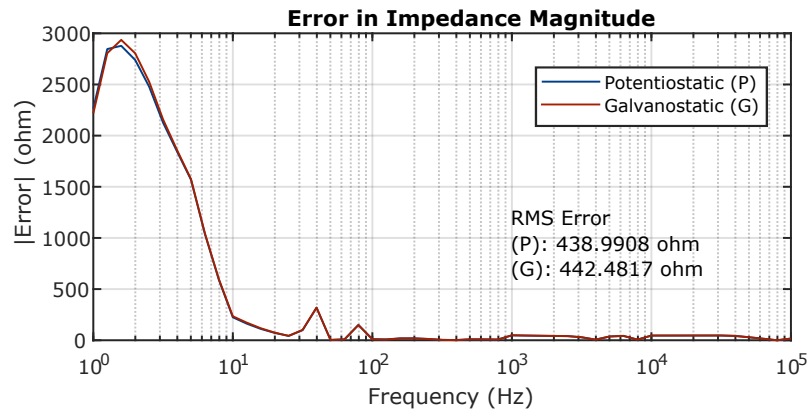


(a) EIS comparison between the measured impedance of DBS equivalent circuit model by NeuroZ and CHI760E. The blue curve represents CHI760E in potentiostatic mode, the red curve corresponds to CHI760E in galvanostatic mode, and the pink curve depicts data from NeuroZ with an two-decade multi-sine waveform.

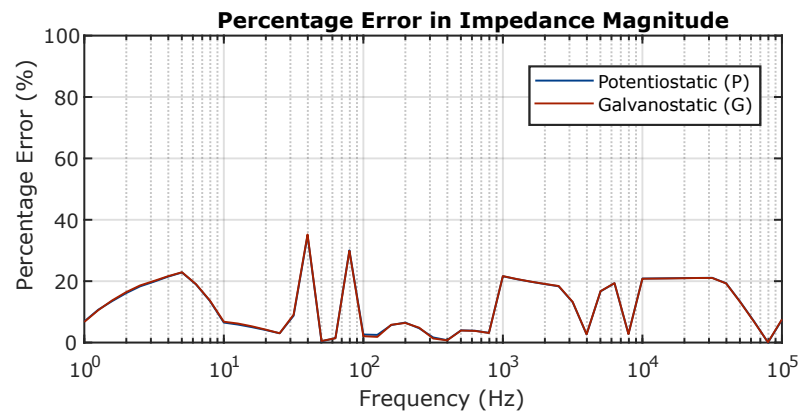


(b) EIS of the DBS circuit model data after interpolation from 1 Hz to 100 kHz, with 10 data points per decade.

Figure 5.32: Electrode Impedance Spectroscopy (EIS) comparison and interpolation results for DBS equivalent circuit model. Subfigures illustrate the original measured data and interpolated data for consistent frequency spacing.

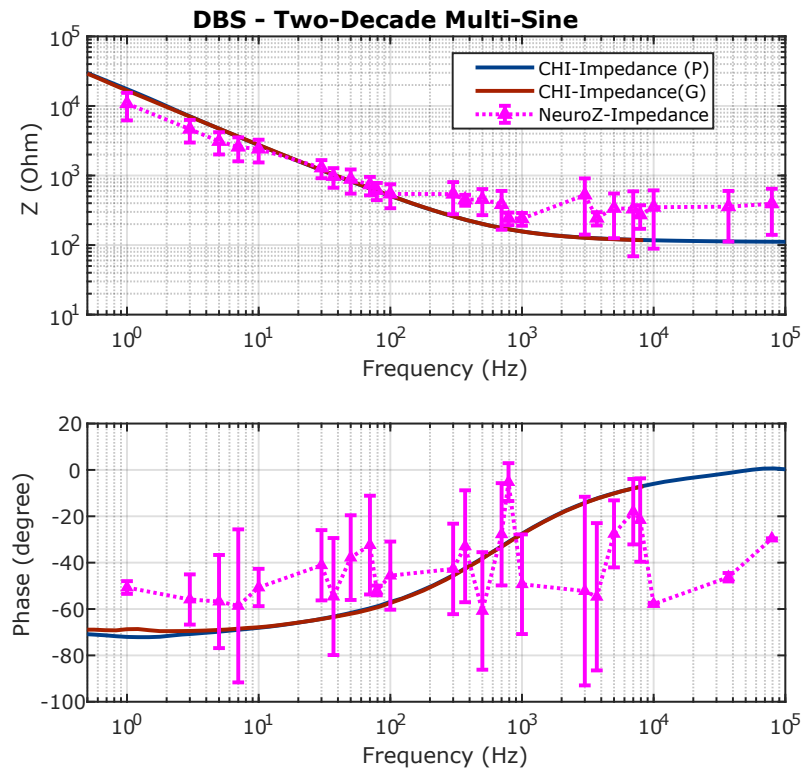


(a) Error in ohms. RMS error of the results is 438.99 Ω for the potentiostatic mode and 442.48 Ω for galvanostatic mode.

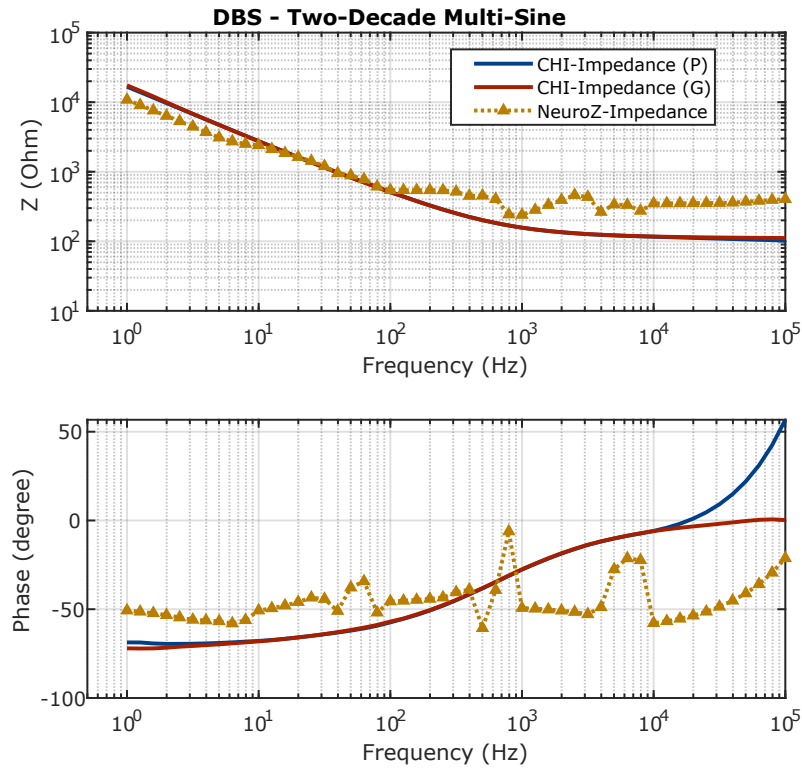


(b) Error in percentage.

Figure 5.33: Error analysis of measured EIS data for DBS equivalent circuit model. Subfigures show the error in absolute ohms and the percentage error between NeuroZ with multi-sine waveform and CHI760E measurements.

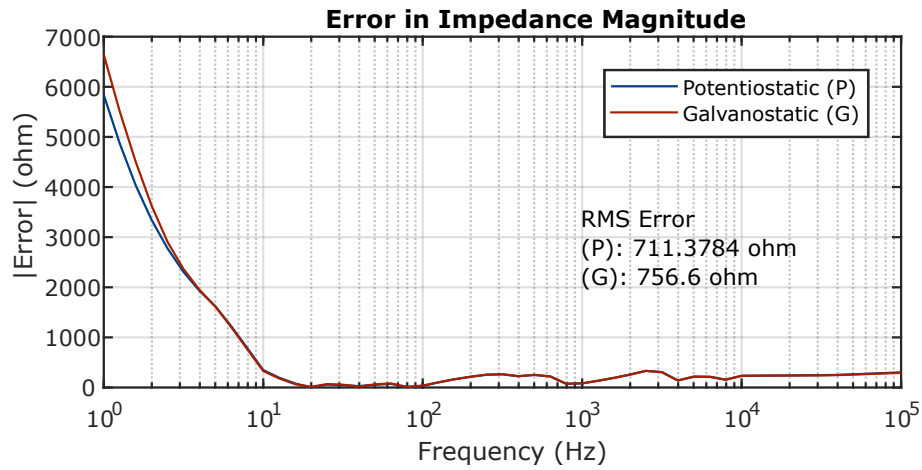


(a) EIS comparison between the measured impedance of DBS electrodes by NeuroZ with multi-sine waveform and CHI760E. The blue curve represents CHI760E in potentiostatic mode, the red curve corresponds to CHI760E in galvanostatic mode, and the pink curve depicts data from NeuroZ.

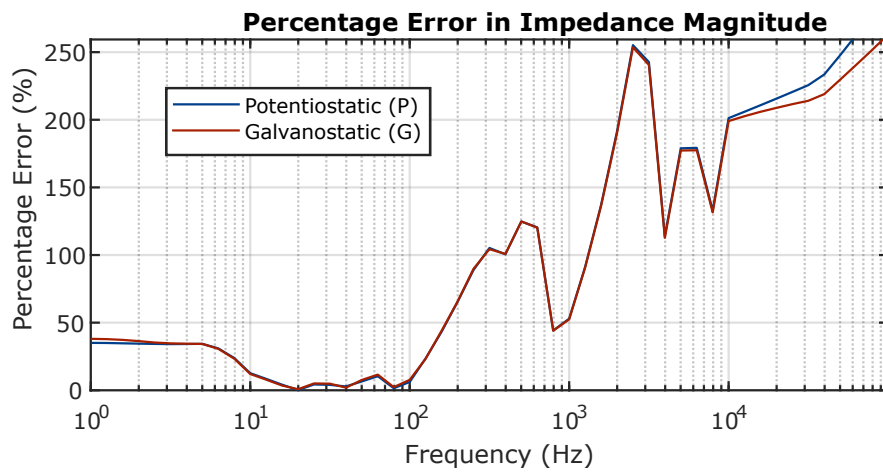


(b) EIS of the DBS data after interpolation from 1 Hz to 100 kHz, with 10 data points per decade.

Figure 5.34: Electrode Impedance Spectroscopy (EIS) comparison and interpolation results for DBS electrodes. Subfigures illustrate the original measured data and interpolated data for consistent frequency spacing.



(a) Error in ohms. RMS error of the results is 711.38 Ω for the potentiostatic mode and 756.6 Ω for NeuroZ.



(b) Error in percentage.

Figure 5.35: Error analysis of measured EIS data for DBS electrodes. Subfigures show the error in absolute ohms and the percentage error between NeuroZ with multi-sine waveform and CHI760E measurements.

5.9.6 Two-Decade Multi-Sine Impedance Measurement results

DBS-RC Two-Decade Multi-Sine Across Two Decades

The NeuroZ chip was evaluated using the DBS-RC model under two-decade multi-sine testing conditions, covering two decades of frequencies from 1 Hz to 100 kHz. This approach aimed to balance detailed characterisation with improved time efficiency. In the mid-frequency range (10 Hz to 10 kHz), the percentage errors were 10.02% and 9.96% for potentiostatic and galvanostatic modes, respectively, as compared to the CHI760E system (Figure 5.34). At low frequencies (1–10 Hz), errors increased to 12.61% and 12.72%, reflecting challenges in data interpolation in this range. High-frequency errors (10 kHz to 100 kHz) were 15.71% and 15.68% for potentiostatic and galvanostatic modes, respectively (Figure 5.35). The averaged RMS errors were $438.99\ \Omega$ in potentiostatic mode and $442.48\ \Omega$ in galvanostatic mode.

Neural Electrodes with Multi-Sine Impedance Measurement Across Two Frequency Decades

The NeuroZ chip was tested with various neural electrodes, including DBS, SEEG, ECoG, and cuff electrodes, using the two-decade multi-sine waveform covering two decades of frequencies. For DBS electrodes, the mid-frequency range (10 Hz to 10 kHz) showed errors of 119.00% and 118.39% for potentiostatic and galvanostatic modes, respectively, with RMS errors of $711.38\ \Omega$ and $756.60\ \Omega$ (Figure 5.34, Figure 5.35). Low-frequency errors (1–10 Hz) were 18.67% and 19.40%, while high-frequency errors (10 kHz to 100 kHz) were 236.07% and 222.37%.

SEEG electrodes exhibited significant variability, with mid-frequency errors of 18.92% and 19.01% for potentiostatic and galvanostatic modes, respectively. RMS errors were $1790.92\ \Omega$ and $2140.34\ \Omega$ (Figure A.13, Figure A.14). Low-frequency errors were 35.21% (potentiostatic) and 38.92% (galvanostatic), while high-frequency errors were 14.12% and 12.43%.

ECoG electrodes demonstrated better performance, with mid-frequency errors of 39.28% and 38.39% for potentiostatic and galvanostatic modes, respectively. RMS errors were $500.22\ \Omega$ and

468.96 Ω (Figure A.15, Figure A.16). Low-frequency errors were 27.24% and 27.49%, while high-frequency errors were 56.45% and 52.97%.

Cuff electrodes, characterised by the highest impedance, exhibited the largest errors among all electrode types. Mid-frequency errors were 105.58% and 121.57% for potentiostatic and galvanostatic modes, respectively, with RMS errors of 5866.97 Ω and 3776.22 Ω (Figure A.17, Figure A.18). Low-frequency errors were 22.22% and 28.85%, while high-frequency errors were 782.36% and 754.34%.

The results for RC passive components indicate that the multi-sine impedance measurement across two frequency decades provides accuracy less than around 16%. However, for neural electrodes, which typically introduce greater variation and noise, performance in the second decade was significantly less accurate compared to the single-decade method. This discrepancy is attributed to the reduced amplitude of the combined waveform in the second decade, which, even with the maximum gain (50x), resulted in higher errors.

Table 5.8: Summary of the results for the DBS-RC electrode across single frequency, multifrequency, and expanded multifrequency methods. Errors and RMS values are shown for different frequency ranges, compared with EIS measured by CHI760E in potentiostatic mode.

Electrode	1-10 Hz (%)	10-10k Hz (%)	10k-100k Hz (%)	Averaged RMS Error (Ω)
DBS RC - Single-Sine	4.17	13.00	12.08	148.80
DBS RC - Multi-Sine	9.59	9.89	20.11	487.41
DBS RC - Two-Decade Multi-Sine	12.61	10.02	15.71	438.99

Table 5.9: Summary of the results for the DBS-RC electrode across single frequency, multifrequency, and expanded multifrequency methods. Errors and RMS values are shown for different frequency ranges, compared with EIS measured by CHI760E in galvanostatic mode.

Electrode	1-10 Hz (%)	10-10k Hz (%)	10k-100k Hz (%)	Averaged RMS Error (Ω)
DBS RC - Single-Sine	4.19	13.04	12.12	151.31
DBS RC - Multi-Sine	9.61	9.97	20.21	489.42
DBS RC - Two-Decade Multi-Sine	12.72	9.96	15.68	442.48

Table 5.10: Summarised errors of NeuroZ impedance measurement across DBS, SEEG, ECoG, and cuff electrodes using single-sine, multi-sine, and two-decade multi-sine methods. The table highlights the averaged per cent errors and RMS values for low, middle, and high-frequency ranges

Electrode	1-10 Hz (%)		10-10k Hz (%)		10k-100k Hz (%)		Averaged RMS Error (Ω)	
	(P)	(G)	(P)	(G)	(P)	(G)	(P)	(G)
DBS - Single-Sine	19.59	20.12	6.50	6.31	9.42	8.29	448.65	493.06
DBS - Multi-Sine	16.97	17.96	33.00	32.76	22.95	18.09	535.22	581.88
DBS - Two-Decade Multi-Sine	18.67	19.40	119.00	118.39	236.07	222.37	711.38	756.6
SEEG - Single-Sine	44.62	47.82	13.86	14.12	64.53	61.33	2086.37	2436.37
SEEG - Multi-Sine	43.83	47.02	16.18	15.56	11.24	9.93	2137.57	2486.72
SEEG - Two-Decade Multi-Sine	35.21	38.92	18.92	19.01	14.12	12.43	1790.92	2140.34
ECoG - Single-Sine	18.95	17.53	7.95	7.32	103.32	98.35	599.23	558.95
ECoG - Multi-Sine	6.87	6.49	11.83	11.16	8.75	10.7	261.53	230.56
ECoG - Two-Decade Multi-Sine	27.24	27.49	39.28	38.39	56.45	52.97	500.22	468.96
Cuff - Single-Sine	21.09	67.56	14.30	20.11	18.52	15.54	3161.77	6960.22
Cuff - Multi-Sine	24.47	16.74	59.81	74.51	56.01	50.9	4483.62	1801.91
Cuff - Two-Decade Multi-Sine	22.22	28.85	105.58	121.57	782.36	754.34	5866.97	3716.81

5.10 Discussion

At high frequencies, particularly between 80 kHz and 100 kHz, the measured waveforms exhibited distortion caused by timing inconsistencies in the microcontroller controlling the NeuroZ chip. These irregularities introduced small phase and amplitude deviations between the generated and measured signals. Circuit simulations in Cadence, using the DBS electrode model under stimulation conditions, indicated that the on-chip circuitry was capable of performing impedance measurements up to 100 kHz. In practice, however, the precision of the external microcontroller imposed practical constraints, and consistent measurements were obtained only up to approximately 60 kHz, beyond which waveform quality degraded. This finding suggests that the limitation arises from the controller rather than the analogue front-end, and that extending the usable frequency range would require a higher-speed or more precisely synchronised control interface.

Within the mid-frequency range (10 Hz–10 kHz), the system demonstrated the most stable and accurate performance. This region corresponds to the frequencies most commonly used for

electrode impedance characterisation. Across all electrode types, the average percentage error ranged from approximately 6–16% for the single-sine method and 16–33% for the multi-sine method. These results were consistent across both potentiostatic and galvanostatic modes and showed comparable trends to those obtained using the reference electrochemical workstation system (CHI760E). The mid-frequency range therefore represents the optimal operating window in which both the measurement circuitry and the electrode–electrolyte interface exhibit stable behaviour.

At low frequencies (1–10 Hz), the measurement variability increased, particularly for the cuff and SEEG electrodes. Both electrodes also exhibited high standard deviations when tested using the reference electrochemical workstation system, suggesting that this variation partly reflects the intrinsic behaviour of these electrode types, which tend to show greater low-frequency fluctuation. In contrast, the DBS and ECoG electrodes maintained lower error levels in this range, with errors generally below 20%. These results indicate that low-frequency deviations are more likely related to electrode characteristics and polarisation effects rather than to the measurement circuitry itself.

Comparison of the different excitation methods illustrates the trade-off between measurement accuracy and acquisition time. The single-sine approach provided the highest accuracy but required sequential testing for each frequency, resulting in longer measurement durations. The multi-sine method, which combined several frequencies within one waveform, reduced the total measurement time from approximately 42 s to around 22 s—roughly half—while maintaining an acceptable accuracy level, with errors typically below 30%, particularly in the mid-frequency range. This balance makes the multi-sine configuration suitable for applications where measurement efficiency is important, such as time-constrained or real-time neural research experiments.

The two-decade multi-sine waveform extended the excitation range, allowing broad-spectrum impedance data to be acquired within a single cycle. However, the reduction in overall measurement time was limited, while the distributed spectral energy decreased the amplitude of each frequency component. Consequently, the signal-to-noise ratio was lower, particularly at higher frequencies within the combined one-cycle waveform, leading to increased measurement error

even at maximum amplifier gain. This approach could be refined through amplitude weighting or adaptive gain control to equalise the signal level across frequencies and improve accuracy in the higher frequency band.

The measured power consumption of the NeuroZ chip was approximately 135 mW, which is relatively high for continuous operation but acceptable when used intermittently. In practice, impedance measurements are expected to be performed periodically rather than continuously, which would considerably reduce the average power requirement. The bias level during measurement was set to approximately 200 mV, close to the open-circuit potential recorded for the working electrode. For long-term monitoring, measuring the electrode potential prior to each test and adjusting this bias dynamically could help minimise drift and improve measurement repeatability. Further reduction in power consumption could also be achieved by optimising biasing networks and digital clock control.

5.11 Conclusion

The NeuroZ chip demonstrated the capability to perform impedance measurements across a broad frequency range, with the most consistent performance observed between 10 Hz and 10 kHz. Measurement limitations were identified at the upper and lower extremes of the spectrum, primarily related to controller timing and electrode polarisation effects. Among the excitation methods evaluated, the single-sine approach provided the highest accuracy, the multi-sine method offered a practical balance between accuracy and acquisition time, and the two-decade multi-sine method extended frequency coverage but introduced higher measurement error.

This system has potential for further improvement through enhanced high-frequency synchronisation, adaptive gain design, and optimisation of power efficiency. In addition, incorporating bias-tracking to compensate for potential drift during long-term operation could improve the measurement stability over time. Addressing these aspects would enhance the overall precision and robustness of the measurement process. The final chapter summarises the overall findings of this study and considers possible directions for continued development.

Chapter 6

Conclusion

With the growing demand for advanced neural interface technologies, particularly deep brain stimulation (DBS) for treating drug-resistant patients, these devices have become increasingly preferred due to advancements in neurotechnology. One approach that researchers are actively exploring to enhance DBS performance is closed-loop neuromodulation. However, because closed-loop stimulation continuously adjusts the stimulation parameters in response to neural feedback, the dynamic changes in current delivery may alter the electrochemical environment at the electrode–tissue interface, potentially affecting electrode performance and long-term stability. Additionally, implanted electrodes—crucial for both neural stimulation and signal recording—gradually degrade over time due to exposure to harsh surrounding conditions, including temperature fluctuations, mechanical mismatch, and biological responses such as tissue encapsulation, inflammation, and stimulation-induced changes. Therefore, monitoring electrode impedance is essential for evaluating device performance, ensuring long-term stability, and maintaining patient safety.

To address these challenges, a comprehensive review of bidirectional neural interfaces and impedance monitoring techniques was conducted, establishing the role of impedance characterisation in implantable device stability. Based on this foundation, an accelerated testing protocol was developed to evaluate electrode degradation and was used to validate the designed custom PCB circuit system prior to its implementation in the integrated circuit (IC) design. A custom

benchtop platform was developed and tested with DBS electrodes, incorporating electrochemical impedance spectroscopy (EIS) across a range of frequencies.

Building on the benchtop circuit design, an integrated circuit-based impedance measurement system, the NeuroZ chip, was developed to enable impedance monitoring in a compact, implantable-compatible size. The system was tested in vitro with various neural electrodes, exploring both single-sine and multi-sine impedance measurement approaches. The introduction of a multi-sine measurement approach allowed impedance to be measured across multiple frequencies simultaneously, reducing acquisition time and improving efficiency. These developments enhance the capability for electrode monitoring and establish a research platform for implantable neural interface studies. The key contributions of this research are detailed in the following section.

The original contributions of this thesis are summarised as follows, with detailed discussions provided in the respective technical chapters. Relevant publications associated with each chapter are listed in the Appendix.

Accelerated Testing Protocol for Electrode Degradation An accelerated testing protocol was developed to evaluate electrode degradation by inducing controlled mechanical damage on the electrode surface (Chapter 3). The protocol combines elevated temperature and electrical stimulation to accelerate deterioration, while automated electrode switching and scheduled impedance measurements enable continuous long-term operation. This setup provides a repeatable and practical method for assessing impedance measurement systems under conditions representative of surface degradation and prolonged use.

NeuroZ Integrated Circuit for Flexible EIS Measurements A CMOS integrated circuit (“NeuroZ”) was designed in 180 nm technology to support electrochemical impedance spectroscopy across 1 Hz to 100 kHz, with resistance measurement capability between 100 Ω and 1 M Ω . The system was developed as a research tool, with an emphasis on flexibility and customisability for research studies. In addition to conventional single-sine excitation, the chip supports multi-sine operation, enabling faster impedance acquisition while reducing disruption during stimulation. Its functionality was validated using a range of clinically relevant neural electrodes, including DBS, SEEG, ECoG, and cuff electrodes, in PBS solution.

6.1 Future Works

Building upon the findings of this study, several promising avenues for future research can be identified. One potential research direction involves the application of machine learning algorithms to impedance data analysis. Predictive models could be employed to detect patterns in impedance variations, enabling early identification of electrode degradation or adverse tissue responses. By leveraging the predictive model, future studies could develop automated impedance monitoring systems that provide real-time feedback and adaptive stimulation adjustments based on electrode-tissue interactions.

Long-term in vivo validation remains a critical step in translating impedance monitoring techniques into practical applications. Future studies should focus on conducting extensive animal experiments and, ultimately, clinical trials to assess the robustness of impedance measurement methodologies in real-world conditions. These studies would provide essential insights into the impact of biological factors on impedance stability and facilitate the refinement of impedance-based monitoring systems for neural implants.

Additionally, the selection of appropriate measurement frequencies is crucial for optimising impedance characterisation in neural interface applications. Future research could investigate frequency selection strategies that best represent electrode performance under different physiological conditions, ensuring that impedance measurements capture meaningful variations related to electrode stability and function. Furthermore, integrating impedance monitoring with other sensing modalities—such as electrophysiological recordings, bioimpedance spectroscopy, or optical imaging—could provide a more comprehensive understanding of electrode behaviour and neural tissue responses. Such multimodal approaches could improve the accuracy of neural interface diagnostics and contribute to the development of more effective and adaptive neurotechnologies.

6.2 Lessons Learned from This Research

Frequency Dependence of Impedance in Neural Interfaces

Electrode impedance varies across frequency, and different ranges provide complementary information. Low frequencies are sensitive to insulation integrity and electrode coatings, while intermediate frequencies (hundreds of Hz to a few kHz) overlap with the bandwidth of neural signals and are relevant for assessing recording quality. Higher frequencies extend into the bioimpedance regime, where impedance can provide insights into tissue responses or encapsulation effects. This dependence highlights the importance of selecting appropriate frequency ranges depending on the application, whether for recording, stimulation, or long-term monitoring.

Development of an Adaptable Impedance Measurement System

This research led to the development of an impedance measurement system that captures the essential functions of a benchtop electrochemical workstation while being more compact and suited to implantable electrode studies. Although conventional workstations remain the reference standard for detailed electrochemical analysis, their bulk and complexity limit their direct applicability to in vivo experiments. The system developed here offers a practical and flexible platform for laboratory evaluation of implantable neural interfaces.

Optimisation of Frequency Selection for Implantable Devices

Rather than measuring the entire impedance spectrum, this study explored the use of strategically selected frequencies, including prime-numbered distributions across one to two decades. This approach reduces harmonic overlap, shortens measurement time, and still allows useful interpolation of the spectrum. While full-spectrum measurements remain valuable for comprehensive electrode characterisation, implantable devices may benefit from measuring only a

subset of frequencies. Careful selection of these frequencies can improve the efficiency of data acquisition while retaining the essential information needed for assessing device performance and safety.

Appendix A

A.1 List of publications

The conference publications related to this thesis are listed below according to the relevant technical chapter.

- **Chapter 3**

V. Manatchinapisit, A. Rapeaux, I. Williams and T. G. Constandinou, “Accelerated testing of electrode degradation for validation of new implantable neural interfaces, Characterisation of Implantable Electrodes,” *2022 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, Taipei, Taiwan, 2022, pp. 534-538, doi: 10.1109/BioCAS54905.2022.9948555.

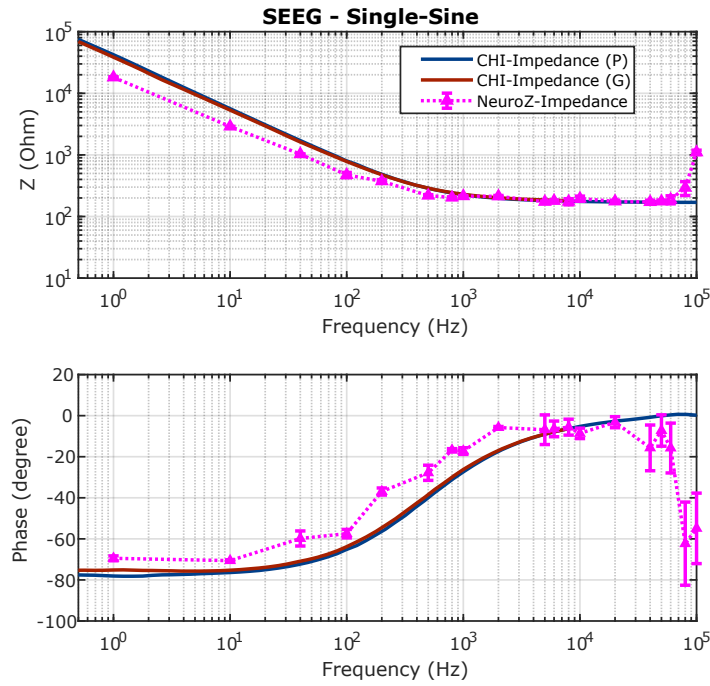
- **Chapter 4**

V. Manatchinapisit and T. G. Constandinou, “A Portable and Low-cost Electrochemical Impedance Spectroscopy Platform for the Characterisation of Implantable Electrodes,” *2024 46th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, Orlando, FL, USA, 2024, pp. 1-5, doi: 10.1109/EMBC53108.2024.10782309.

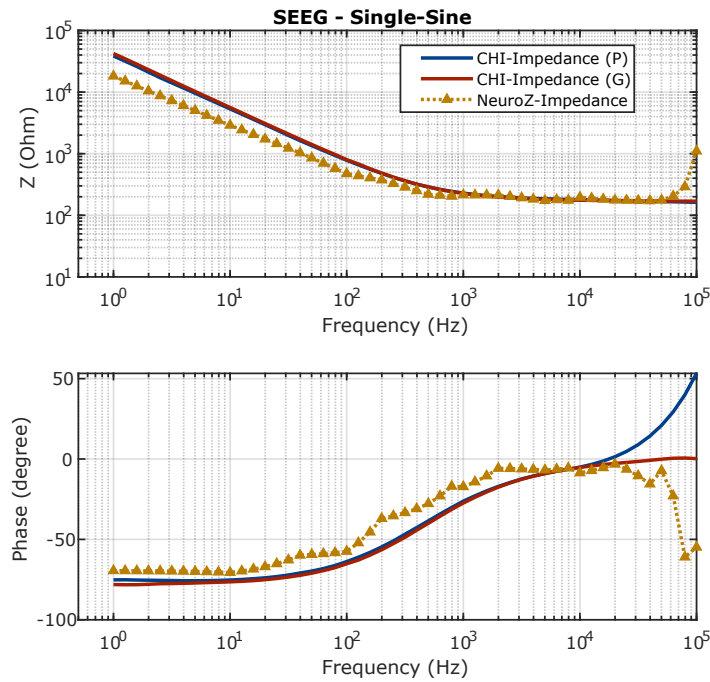
- **Chapter 5**

V. Manatchinapisit, P. Feng, L. Xie and T. G. Constandinou, “An Impedance Characterisation Circuit for Implantable Research Platforms,” *2024 19th Conference on Ph.D Research in Microelectronics and Electronics (PRIME)*, Larnaca, Cyprus, 2024, pp. 1-4, doi: 10.1109/PRIME61930.2024.10559709.

A.2 EIS Results for Single-sine Waveform

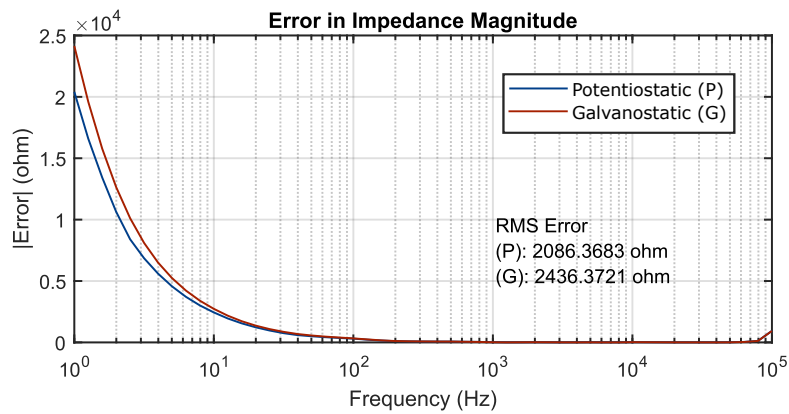


(a) EIS comparison between the measured impedance of SEEG electrodes by NeuroZ with multi-sine waveform (pink) and CHI760E in potentiostatic mode (blue) and in galvanostatic (red)

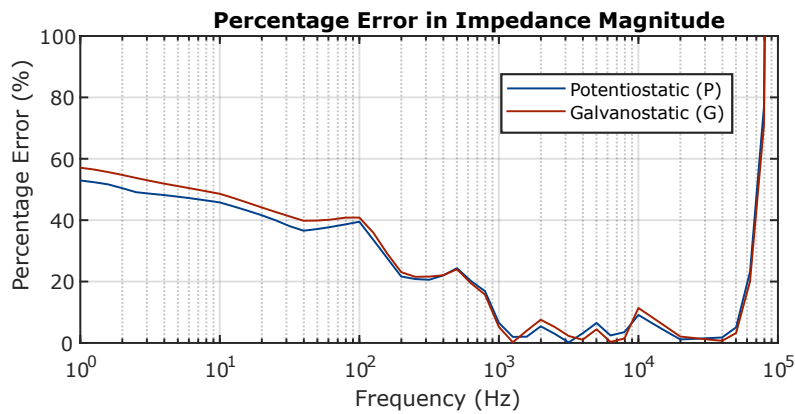


(b) EIS of the same data after interpolation from 1 Hz to 100 kHz, with 10 data points per decade.

Figure A.1: Electrode Impedance Spectroscopy (EIS) comparison and interpolation results for SEEG electrodes. Subfigures illustrate the original measured data and interpolated data for consistent frequency spacing.

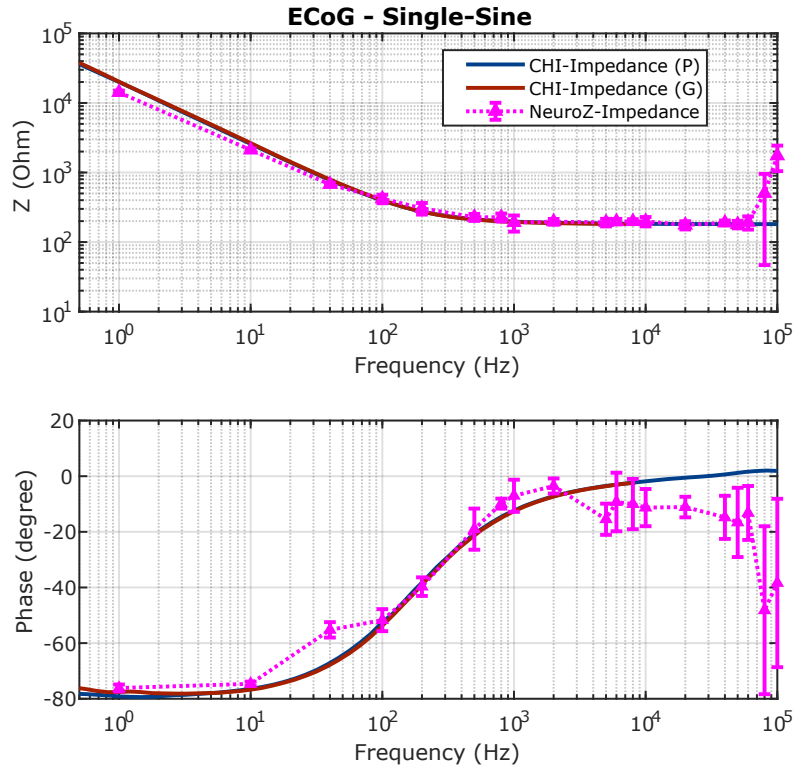


(a) Error in ohms. RMS error of the results is 2066.36 Ω for the potentiostatic mode and 2436.37 Ω for NeuroZ.

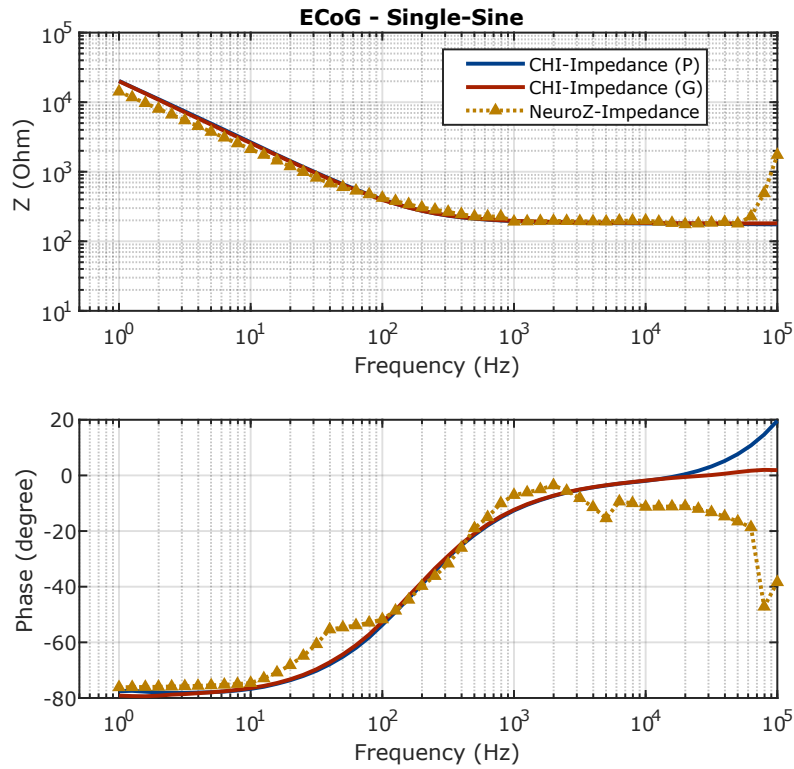


(b) Error in percentage.

Figure A.2: Error analysis of measured EIS data for SEEG electrodes. Subfigures show the error in absolute ohms and the percentage error between NeuroZ and CHI760E measurements.

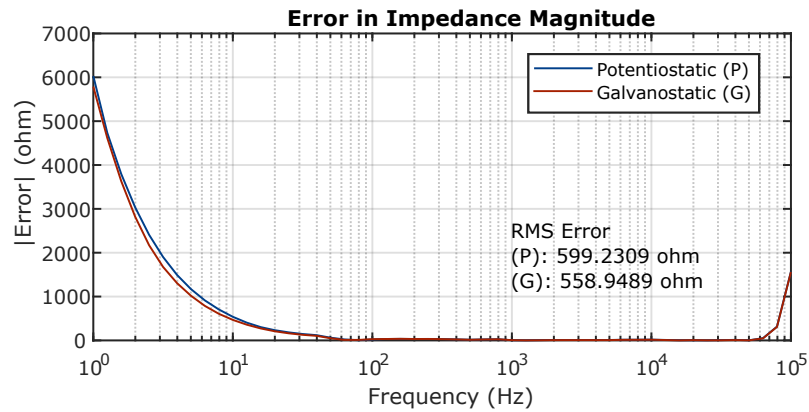


(a) EIS comparison between the measured impedance of ECoG electrodes by NeuroZ and CHI760E. The blue curve represents CHI760E in potentiostatic mode, the red curve corresponds to CHI760E in galvanostatic mode, and the pink curve depicts data from NeuroZ.

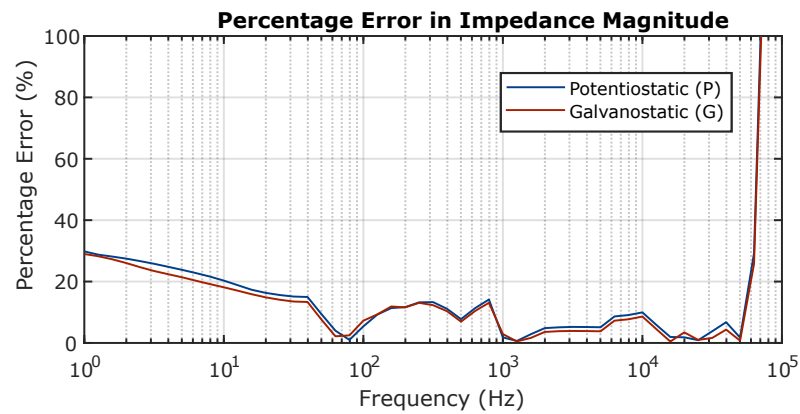


(b) EIS of the same data after interpolation from 1 Hz to 100 kHz, with 10 data points per decade.

Figure A.3: Electrode Impedance Spectroscopy (EIS) comparison and interpolation results for ECoG electrodes. Subfigures illustrate the original measured data and interpolated data for consistent frequency spacing.

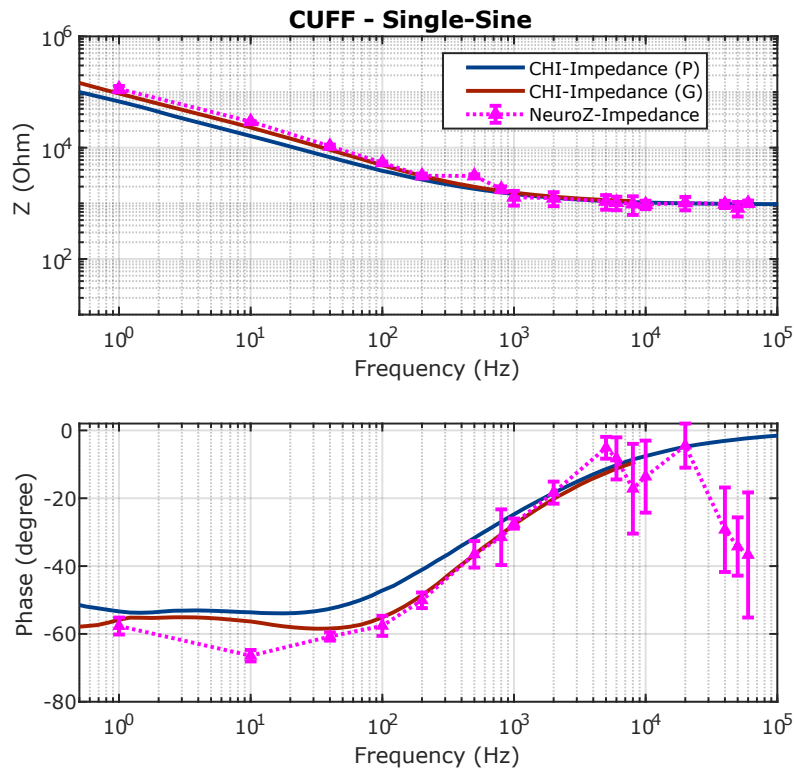


(a) Error in ohms. RMS error of the results is 599.23 Ω for the potentiostatic mode and 558.95 Ω for NeuroZ.

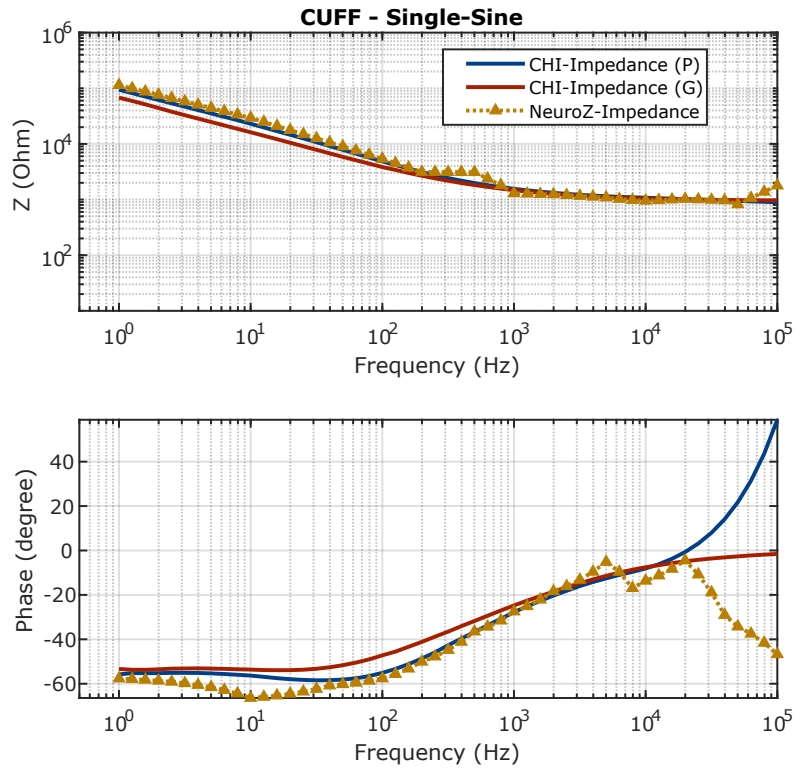


(b) Error in percentage.

Figure A.4: Error analysis of measured EIS data for ECoG electrodes. Subfigures show the error in absolute ohms and the percentage error between NeuroZ and CHI760E measurements.

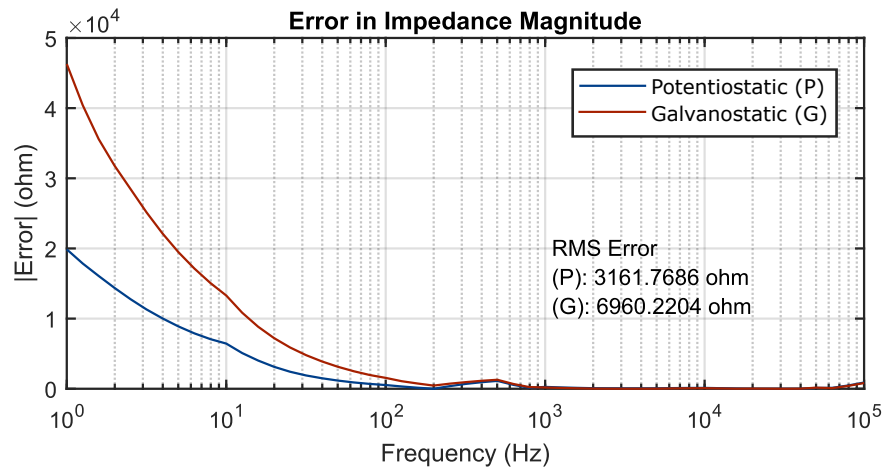


(a) EIS comparison between the measured impedance of Cuff electrodes by NeuroZ and CHI760E. The blue curve represents CHI760E in potentiostatic mode, the red curve corresponds to CHI760E in galvanostatic mode, and the pink curve depicts data from NeuroZ.

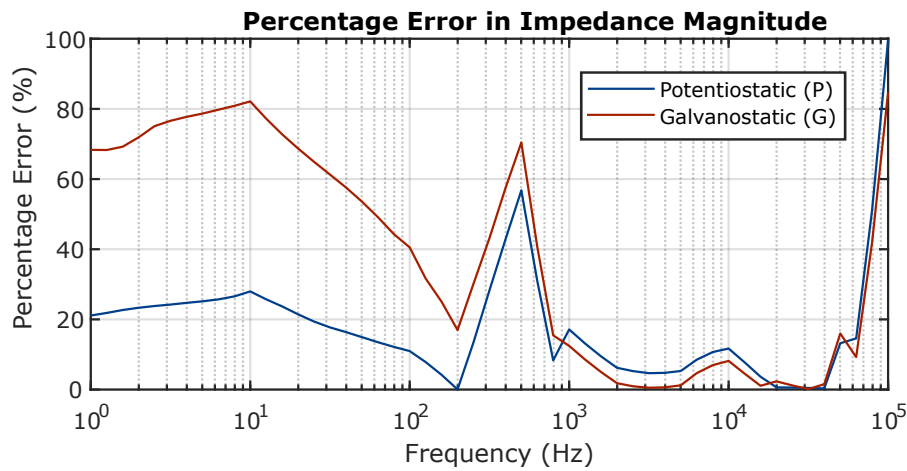


(b) EIS of the same data after interpolation from 1 Hz to 100 kHz, with 10 data points per decade.

Figure A.5: Electrode Impedance Spectroscopy (EIS) comparison and interpolation results for Cuff electrodes. Subfigures illustrate the original measured data and interpolated data for consistent frequency spacing.



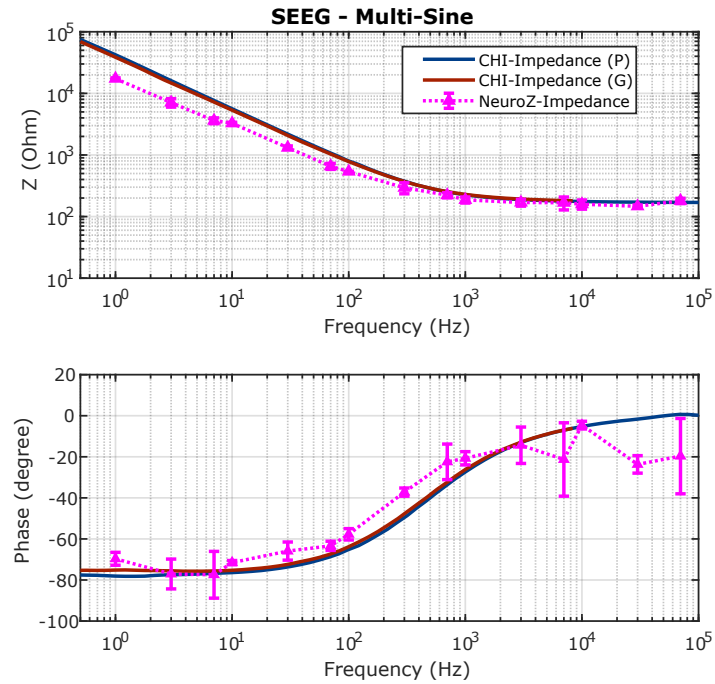
(a) Error in ohms. RMS error of the results is 3161.77 Ω for the potentiostatic mode and 6960.22 Ω for NeuroZ.



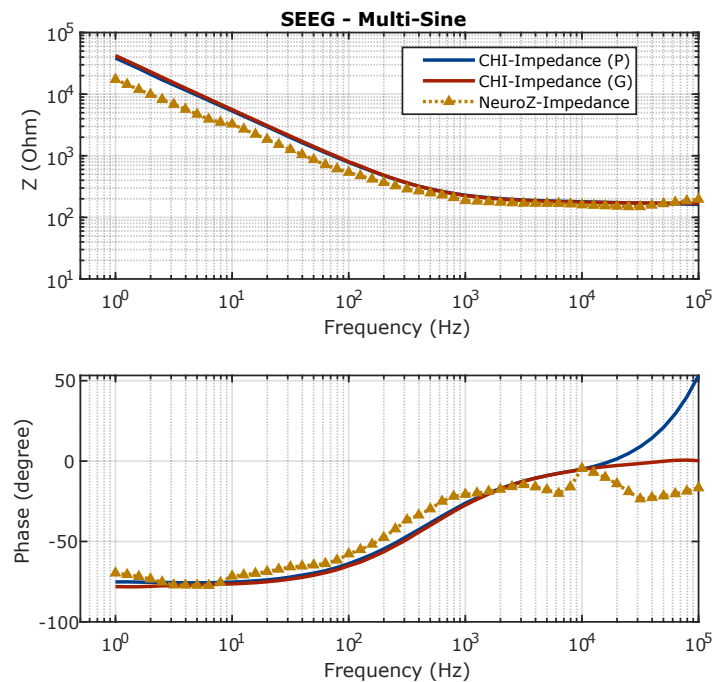
(b) Error in percentage.

Figure A.6: Error analysis of measured EIS data for cuff electrodes. Subfigures show the error in absolute ohms and the percentage error between NeuroZ and CHI760E measurements.

A.3 EIS Results of Multi-Sine waveform

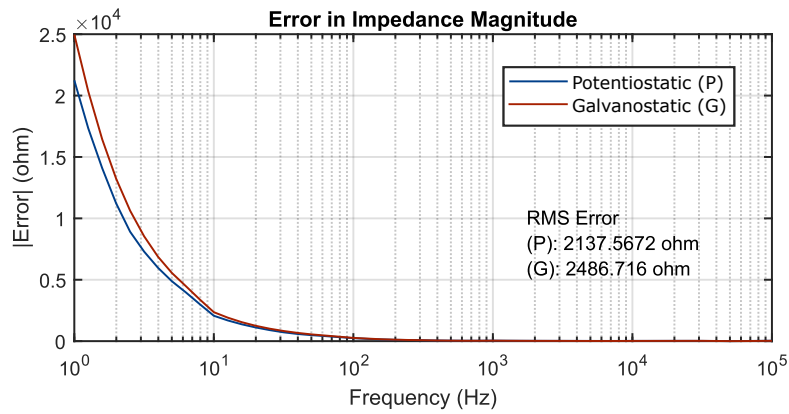


(a) EIS comparison between the measured impedance of SEEG electrodes by NeuroZ with multi-sine waveform (pink) and CHI760E in potentiostatic mode(blue) and in galvanostatic mode(red)

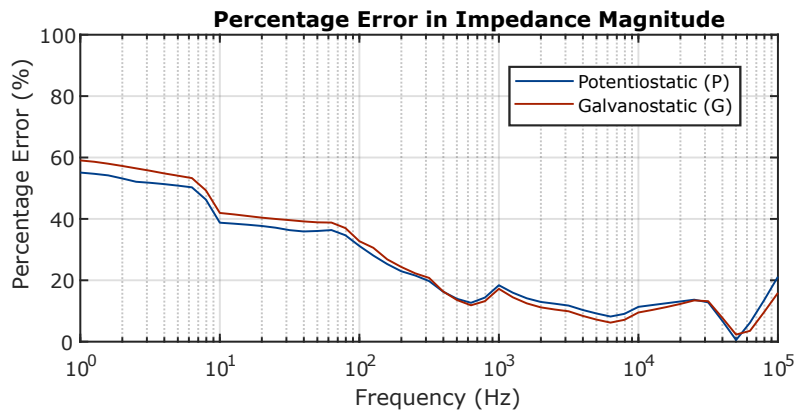


(b) EIS of the same data after interpolation from 1 Hz to 100 kHz, with 10 data points per decade.

Figure A.7: Electrode Impedance Spectroscopy (EIS) comparison and interpolation results for SEEG electrodes. Subfigures illustrate the original measured data and interpolated data for consistent frequency spacing.

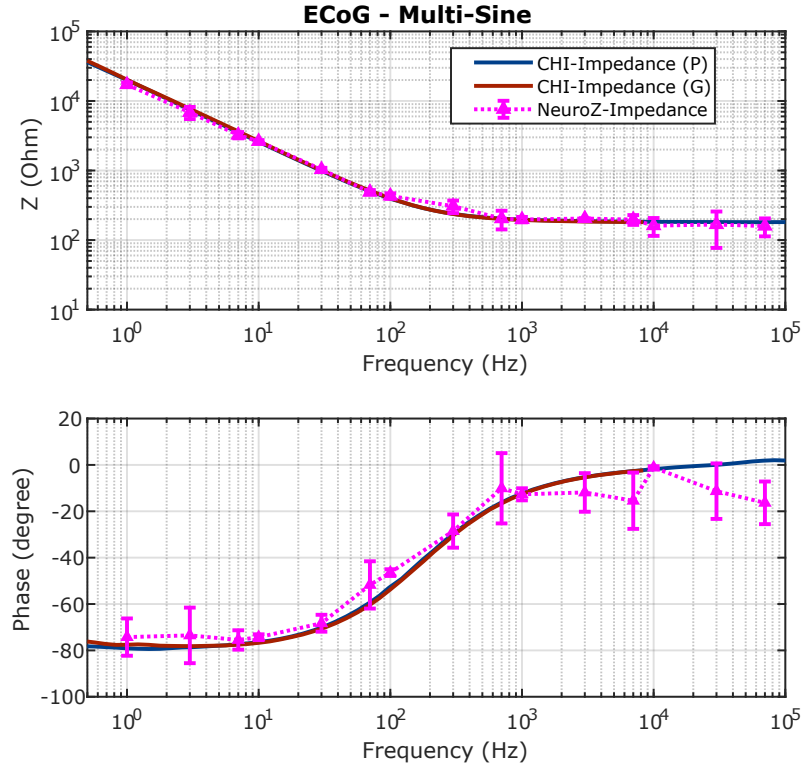


(a) Error in ohms. RMS error of the results is 2137.56 Ω for the potentiostatic mode and 2486.72 Ω for the galvanostatic mode.

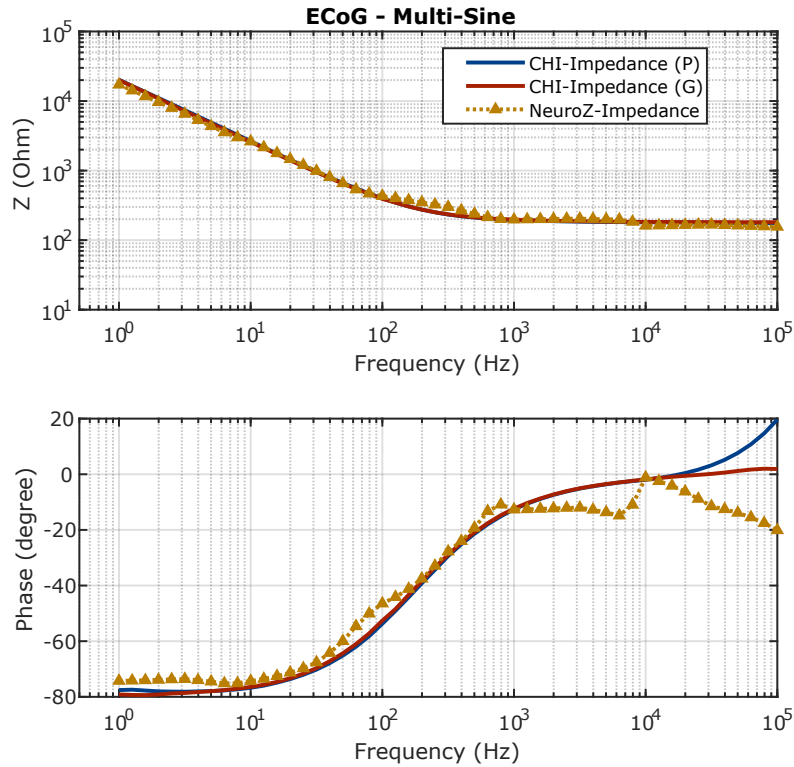


(b) Error in percentage.

Figure A.8: Error analysis of measured EIS data for SEEG electrodes. Subfigures show the error in absolute ohms and the percentage error between NeuroZ with multi-sine waveform and CHI760E measurements.

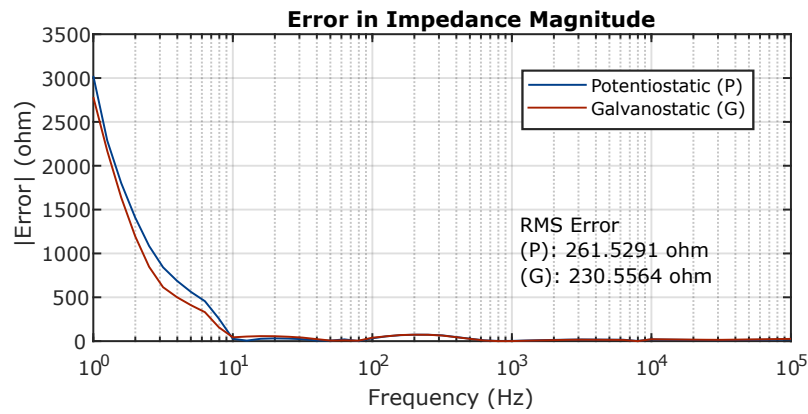


(a) EIS comparison between the measured impedance of ECoG electrodes by NeuroZ with multi-sine waveform (pink) and CHI760E in potentiostatic mode (blue) and in galvanostatic (red)

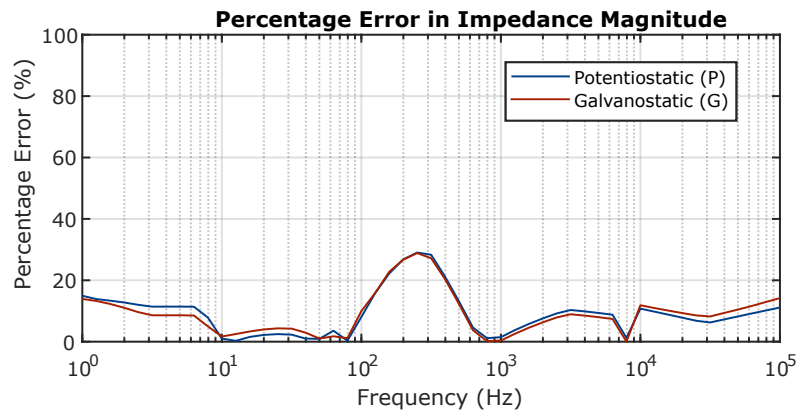


(b) EIS of the ECoG data after interpolation from 1 Hz to 100 kHz, with 10 data points per decade.

Figure A.9: Electrode Impedance Spectroscopy (EIS) comparison and interpolation results for ECoG electrodes. Subfigures illustrate the original measured data and interpolated data for consistent frequency spacing.

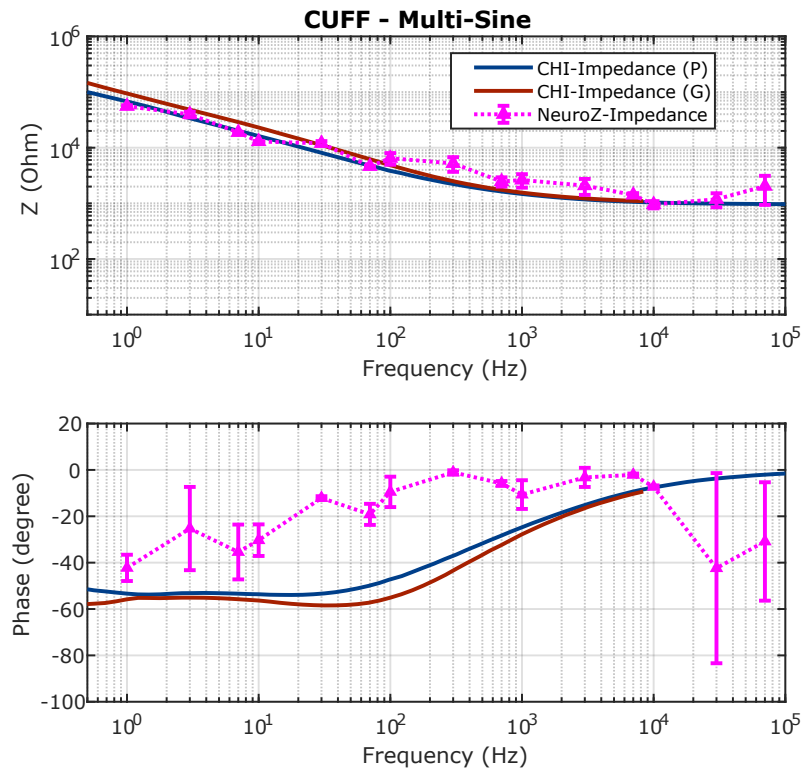


(a) Error in ohms. RMS error of the results is 261.53 Ω for the potentiostatic mode and 230.56 Ω for galvanostatic mode.

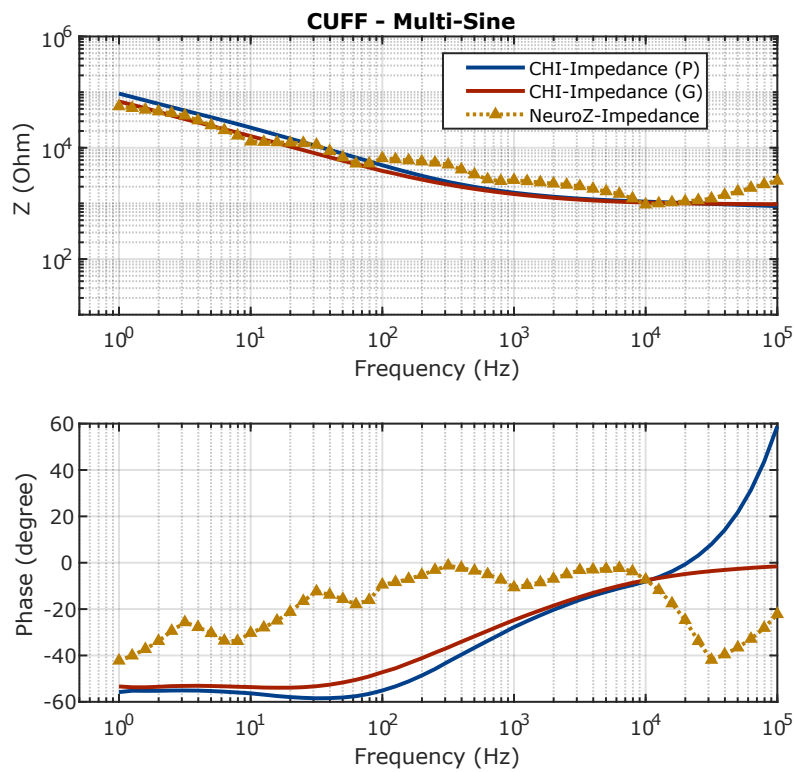


(b) Error in percentage.

Figure A.10: Error analysis of measured EIS data for ECoG electrodes. Subfigures show the error in absolute ohms and the percentage error between NeuroZ with multi-sine waveform and CHI760E measurements.

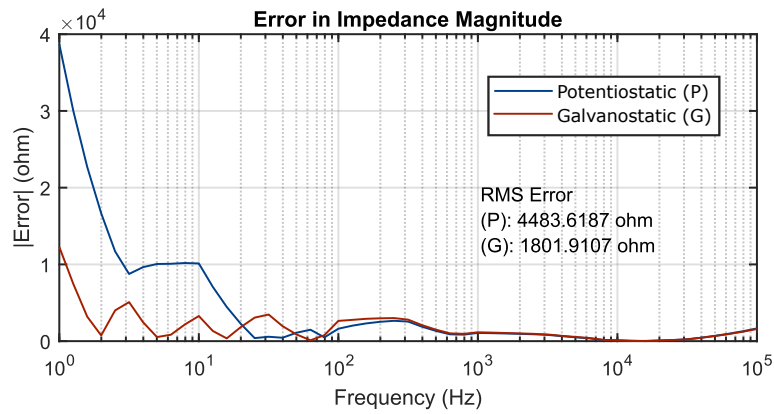


(a) EIS comparison between the measured impedance of cuff electrodes by NeuroZ with multi-sine waveform (pink) and CHI760E in potentiostatic mode (blue) and in galvanostatic (red)

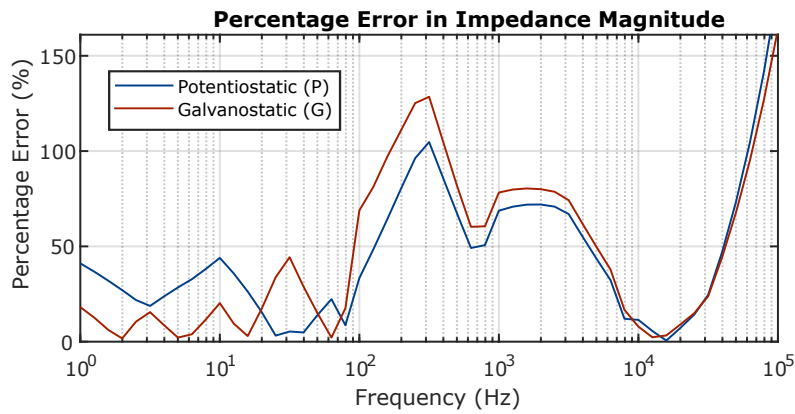


(b) EIS of the same data after interpolation from 1 Hz to 100 kHz, with 10 data points per decade.

Figure A.11: Electrode Impedance Spectroscopy (EIS) comparison and interpolation results for Cuff electrodes. Subfigures illustrate the original measured data and interpolated data for consistent frequency spacing.



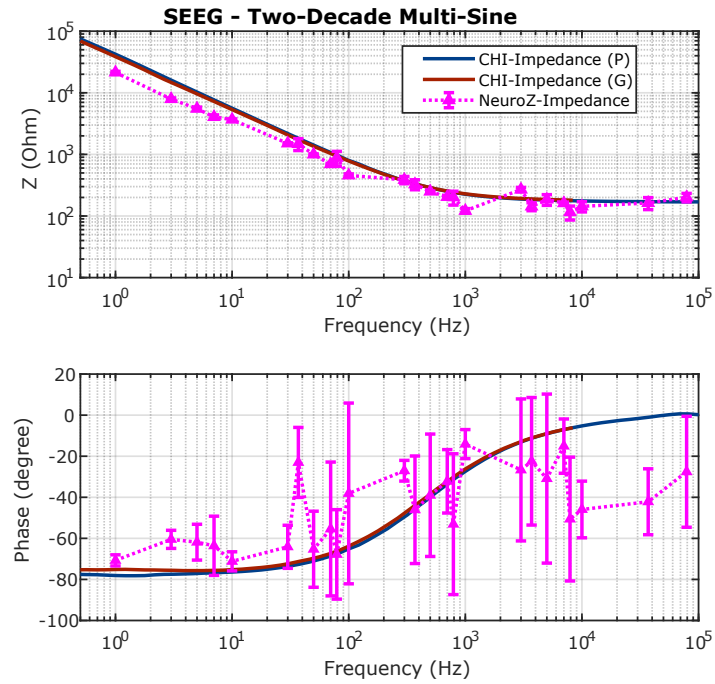
(a) Error in ohms. RMS error of the results is 4483.62 Ω for the potentiostatic mode and 1801.91 Ω for galvanostatic mode.



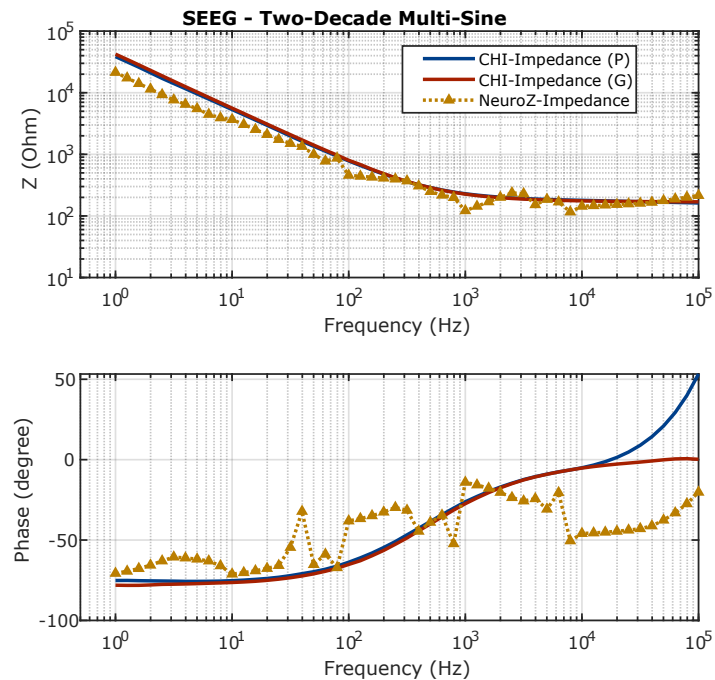
(b) Error in percentage.

Figure A.12: Error analysis of measured EIS data for cuff electrodes. Subfigures show the error in absolute ohms and the percentage error between NeuroZ with multi-sine waveform and CHI760E measurements.

A.4 EIS Results of Two-Decade Multi-Sine Waveform

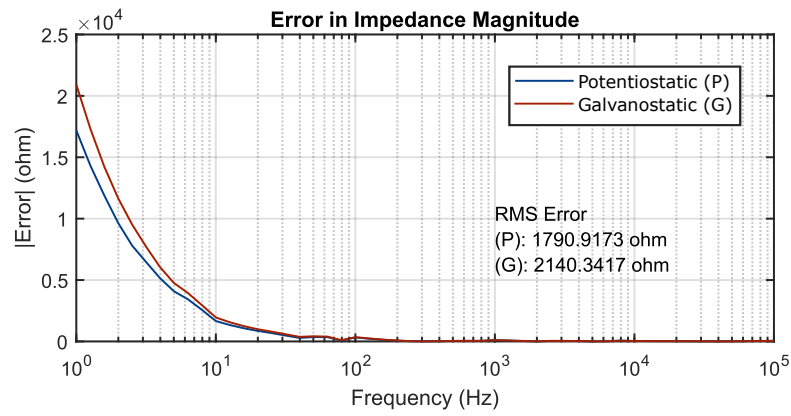


(a) EIS comparison between the measured impedance of SEEG electrodes by NeuroZ with two-decade multi-sine waveform (pink) and CHI760E in potentiostatic mode (blue) and in galvanostatic mode (red)

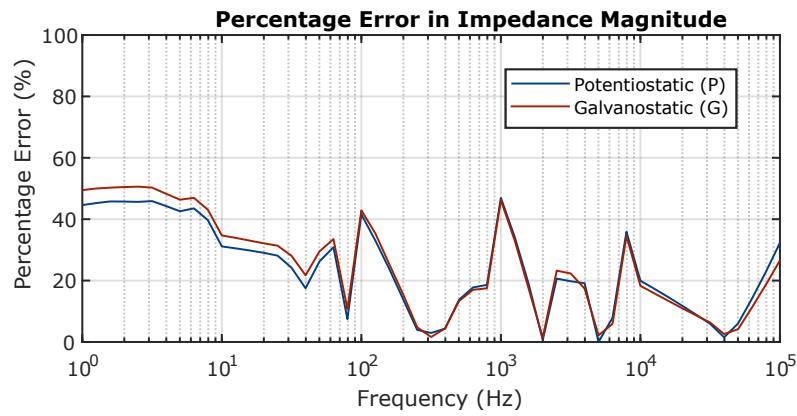


(b) EIS of the same data after interpolation from 1 Hz to 100 kHz, with 10 data points per decade.

Figure A.13: Electrode Impedance Spectroscopy (EIS) comparison and interpolation results for SEEG electrodes. Subfigures illustrate the original measured data and interpolated data for consistent frequency spacing.

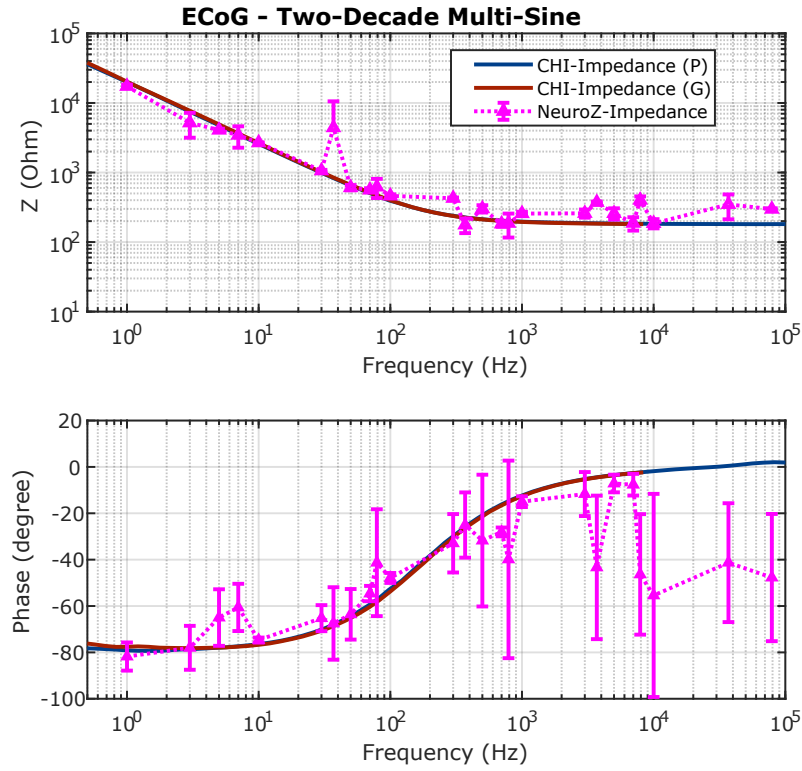


(a) Error in ohms. RMS error of the results is 1790.92 Ω for the potentiostatic mode and 2140.34 Ω for galvanostatic mode.

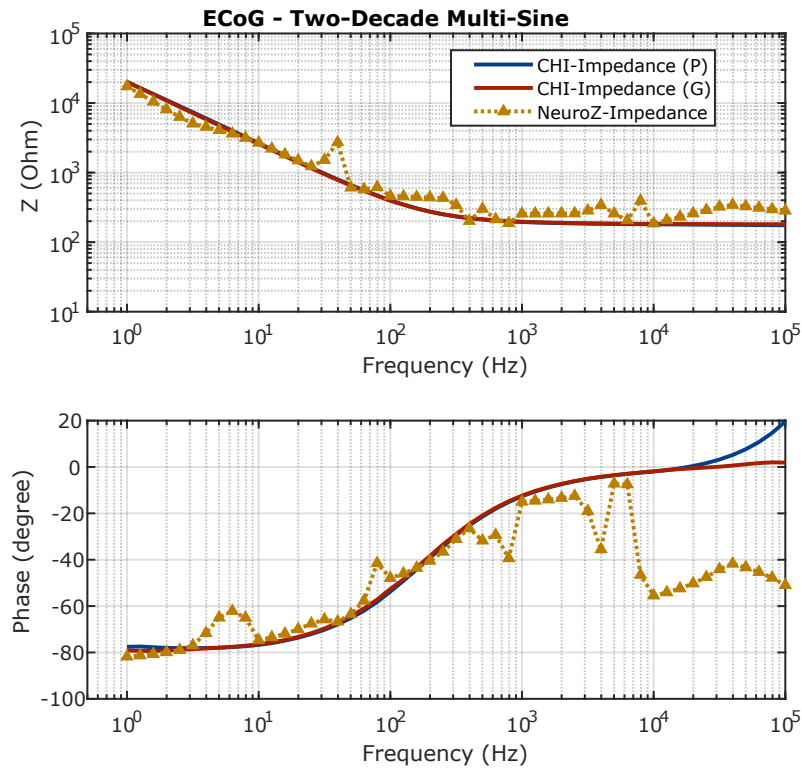


(b) Error in percentage.

Figure A.14: Error analysis of measured EIS data for SEEG electrodes. Subfigures show the error in absolute ohms and the percentage error between NeuroZ with multi-sine waveform and CHI760E measurements.

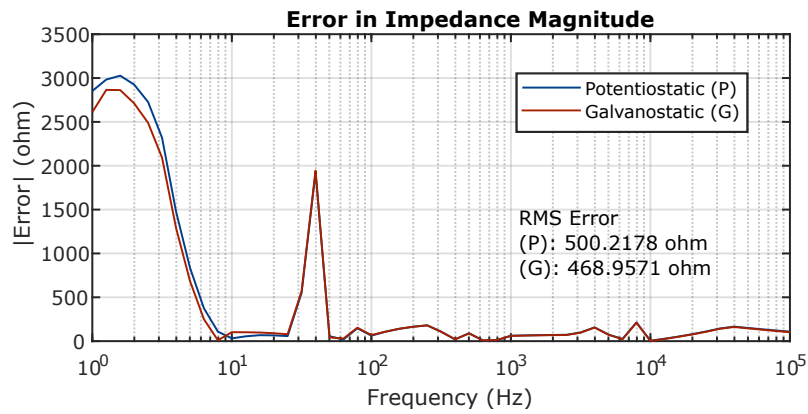


(a) EIS comparison between the measured impedance of ECoG electrodes by NeuroZ with two-decade multi-sine waveform (pink) and CHI760E in potentiostatic mode (blue) and in galvanostatic (red)

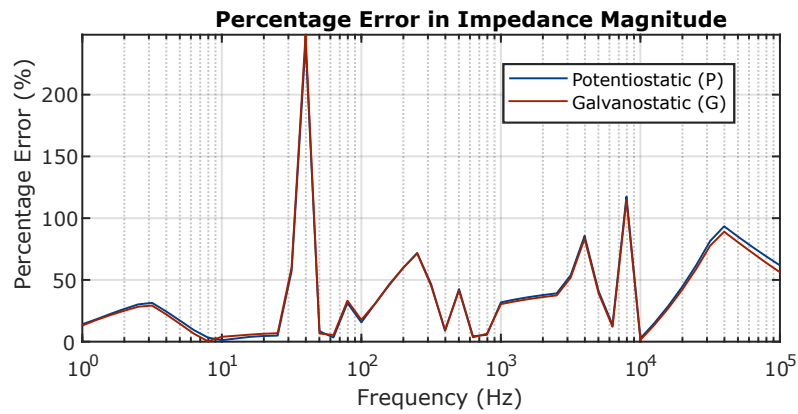


(b) EIS of the ECoG data after interpolation from 1 Hz to 100 kHz, with 10 data points per decade.

Figure A.15: Electrode Impedance Spectroscopy (EIS) comparison and interpolation results for ECoG electrodes. Subfigures illustrate the original measured data and interpolated data for consistent frequency spacing.

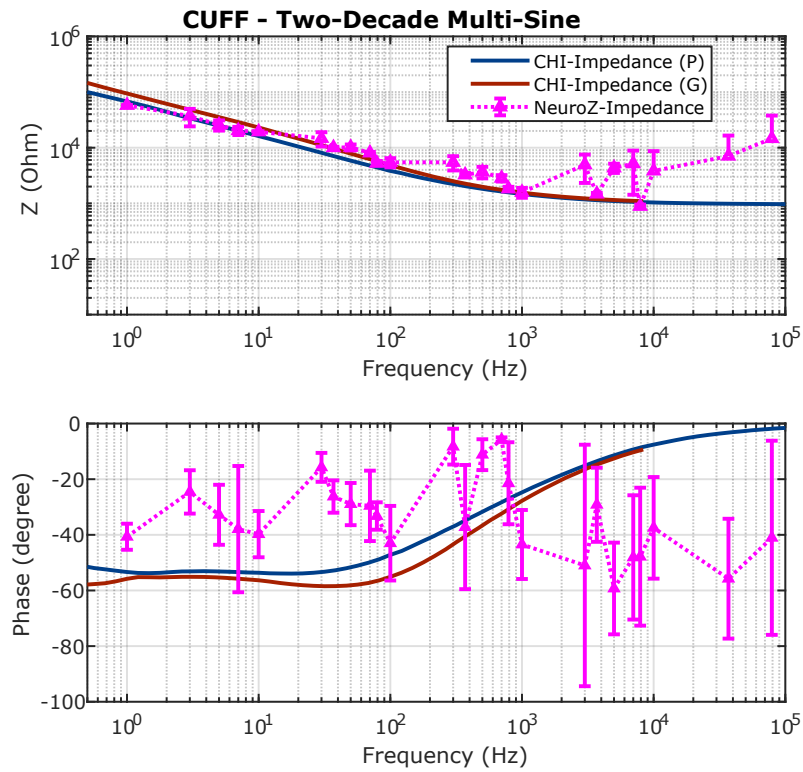


(a) Error in ohms. RMS error of the results is 500.22 Ω for the potentiostatic mode and 468.96 Ω for galvanostatic mode.

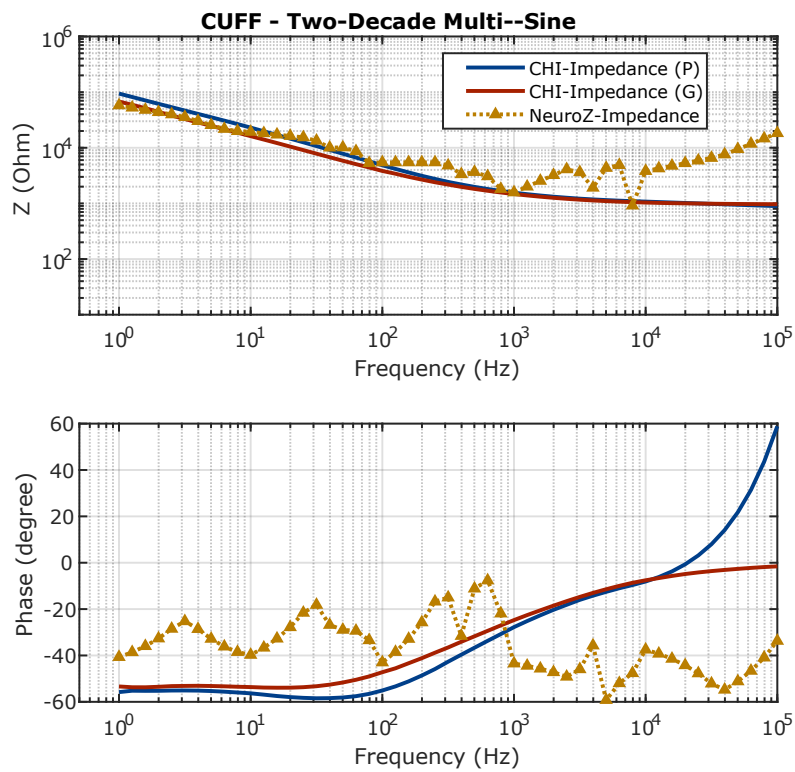


(b) Error in percentage.

Figure A.16: Error analysis of measured EIS data for ECoG electrodes. Subfigures show the error in absolute ohms and the percentage error between NeuroZ with multi-sine waveform and CHI760E measurements.

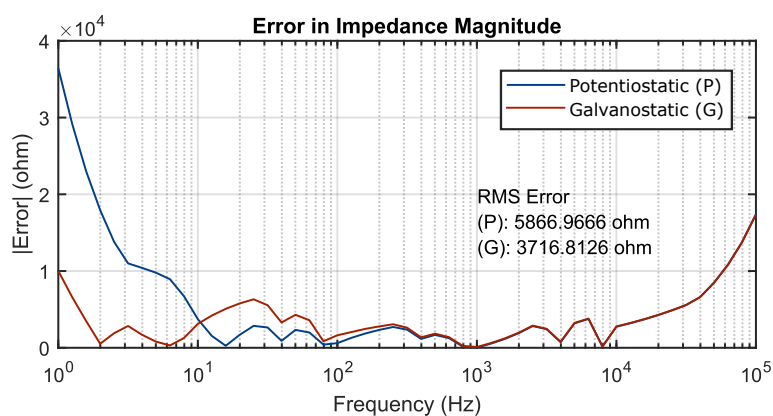


(a) EIS comparison between the measured impedance of cuff electrodes by NeuroZ with two-decade multi-sine waveform (pink) and CHI760E in potentiostatic mode (blue) and in galvanostatic (red)

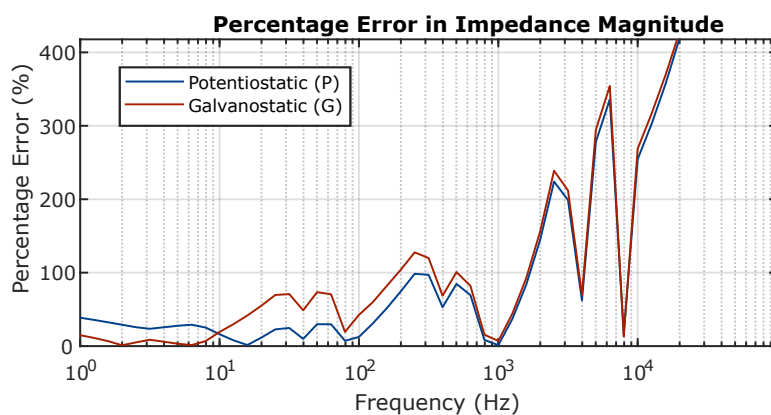


(b) EIS of the same data after interpolation from 1 Hz to 100 kHz, with 10 data points per decade.

Figure A.17: Electrode Impedance Spectroscopy (EIS) comparison and interpolation results for Cuff electrodes. Subfigures illustrate the original measured data and interpolated data for consistent frequency spacing.



(a) Error in ohms. RMS error of the results is 5700.53 Ω for the potentiostatic mode and 3776.22 Ω for NeuroZ.



(b) Error in percentage.

Figure A.18: Error analysis of measured EIS data for cuff electrodes. Subfigures show the error in absolute ohms and the percentage error between NeuroZ with multi-sine waveform and CHI760E measurements.

References

- [1] S. Betteridge, H. Caswell, J. Garlovsky, C. George, et al., *Guidelines for commissioning nhs neuropsychological services*, Nov. 2024. DOI: 10.53841/bpsrep.2024.rep183.a.
- [2] G. Assenza, L. L. Rocha, A. Fattorusso, E. Mencaroni, et al., “The pharmacoresistant epilepsy: An overview on existant and new emerging therapies,” *Frontiers in Neurology*, vol. 1, p. 674483, 2021. DOI: 10.3389/fneur.2021.674483.
- [3] N. Zangiabadi, L. D. Ladino, F. Sina, J. P. Orozco-Hernández, et al., “Deep brain stimulation and drug-resistant epilepsy: A review of the literature,” *Frontiers in Neurology*, vol. 10, p. 433066, JUN Jun. 2019, ISSN: 16642295. DOI: 10.3389/FNEUR.2019.00601/FULL.
- [4] T. Denison and M. J. Morrell, “Neuromodulation in 2035,” *Neurology*, vol. 98, pp. 65–72, 2 Jan. 2022, ISSN: 1526632X. DOI: 10.1212/WNL.0000000000013061.
- [5] S. S. Sandoval-Pistorius, M. L. Hacker, A. C. Waters, J. Wang, et al., “Advances in deep brain stimulation: From mechanisms to applications,” *Journal of Neuroscience*, vol. 43, pp. 7575–7586, 45 Nov. 2023, ISSN: 0270-6474. DOI: 10.1523/JNEUROSCI.1427-23.2023.
- [6] M. R. Burns, S. Y. Chiu, B. Patel, S. G. Mitropanopoulos, et al., “Advances and future directions of neuromodulation in neurologic disorders,” *Neurologic Clinics*, vol. 39, pp. 71–85, 1 Feb. 2021, ISSN: 0733-8619. DOI: 10.1016/J.NCL.2020.09.004.
- [7] J. Gardner, “A history of deep brain stimulation: Technological innovation and the role of clinical assessment tools,” *Social Studies of Science*, vol. 43, pp. 707–728, 5 Oct. 2013, ISSN: 03063127. DOI: 10.1177/0306312713483678.

- [8] A. Albanese, R. M. Fernandez, C. de Hemptinne, J. Frey, et al., “Past, present, and future of deep brain stimulation: Hardware, software, imaging, physiology and novel approaches,” *Frontiers in Neurology*, vol. 1, p. 825178, 2022. DOI: 10.3389/fneur.2022.825178.
- [9] T. R. Wang, S. Moosa, R. F. Dallapiazza, W. J. Elias, et al., “Deep brain stimulation for the treatment of drug addiction,” *Neurosurgical Focus*, vol. 45, E11, 2 Aug. 2018, ISSN: 1092-0684. DOI: 10.3171/2018.5.FOCUS18163.
- [10] L. Mar-Barrutia, E. Real, C. Segalás, S. Bertolín, et al., “Deep brain stimulation for obsessive-compulsive disorder: A systematic review of worldwide experience after 20 years,” *World Journal of Psychiatry*, vol. 11, p. 659, 9 Sep. 2021, ISSN: 2220-3206. DOI: 10.5498/WJP.V11.I9.659.
- [11] S. Delaloye and P. E. Holtzheimer, “Deep brain stimulation in the treatment of depression,” *Dialogues in Clinical Neuroscience*, vol. 16, p. 83, 1 2014, ISSN: 12948322. DOI: 10.31887/DCNS.2014.16.1/SDELALOYE.
- [12] D. Karaszewska, P. Cleintuar, M. Oudijn, A. Lok, et al., “Efficacy and safety of deep brain stimulation for treatment-refractory anorexia nervosa: A systematic review and meta-analysis,” *Translational Psychiatry 2022 12:1*, vol. 12, pp. 1–7, 1 Aug. 2022, ISSN: 2158-3188. DOI: 10.1038/s41398-022-02102-w.
- [13] P. R. Schuurman, D. A. Bosch, P. M. Bossuyt, G. J. Bonsel, et al., “A comparison of continuous thalamic stimulation and thalamotomy for suppression of severe tremor,” *New England Journal of Medicine*, vol. 342, no. 7, pp. 461–468, 2000.
- [14] L. Perestelo-Pérez, A. Rivero-Santana, J. Pérez-Ramos, P. Serrano-Pérez, et al., “Deep brain stimulation in parkinson’s disease: Meta-analysis of randomized controlled trials,” *Journal of Neurology*, vol. 261, no. 11, pp. 2051–2060, 2014, ISSN: 1432-1459. DOI: 10.1007/s00415-014-7254-6.
- [15] P. Kwan and M. J. Brodie, “Early Identification of Refractory Epilepsy,” *New England Journal of Medicine*, vol. 342, no. 5, pp. 314–319, 2000. DOI: 10.1056/NEJM200002033420503.

- [16] F. T. Sun and M. J. Morrell, “Closed-loop Neurostimulation: The Clinical Experience,” *Neurotherapeutics*, vol. 11, no. 3, pp. 553–563, 2014, ISSN: 18787479. DOI: 10.1007/s13311-014-0280-3.
- [17] S. Little, A. Pogosyan, S. Neal, B. Zavala, et al., “Adaptive Deep Brain Stimulation in Advanced Parkinson Disease,” pp. 449–457, 2013. DOI: 10.1002/ana.23951.
- [18] J. A. Herron, M. C. Thompson, T. Brown, H. J. Chizeck, et al., “Cortical Brain-Computer Interface for Closed-Loop Deep Brain Stimulation,” *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, vol. 25, no. 11, pp. 2180–2187, 2017, ISSN: 15344320. DOI: 10.1109/TNSRE.2017.2705661.
- [19] M. J. Morrell, “Responsive cortical stimulation for the treatment of medically intractable partial epilepsy,” *Neurology*, vol. 77, no. 13, pp. 1295–1304, 2011, ISSN: 1526632X. DOI: 10.1212/WNL.0b013e3182302056.
- [20] G. Nune, S. Arcot Desai, B. Razavi, M. A. Agostini, et al., “Treatment of drug-resistant epilepsy in patients with periventricular nodular heterotopia using RNS® System: Efficacy and description of chronic electrophysiological recordings,” *Clinical Neurophysiology*, vol. 130, no. 8, pp. 1196–1207, 2019, ISSN: 18728952. DOI: 10.1016/j.clinph.2019.04.706.
- [21] *Bioinduction: Our solution*, Accessed: Jan. 31, 2025. [Online]. Available: <https://bioinduction.com/the-solution/>.
- [22] K. Woeppel, Q. Yang, and X. T. Cui, “Recent advances in neural electrode–tissue interfaces,” *Current opinion in biomedical engineering*, vol. 4, pp. 21–31, 2017. DOI: 10.1016/j.cobme.2017.09.003.
- [23] J. Evers, K. Sridhar, J. Liegey, J. Brady, et al., “Stimulation-induced changes at the electrode–tissue interface and their influence on deep brain stimulation,” *Journal of Neural Engineering*, vol. 19, no. 4, p. 046004, 2022. DOI: 10.1088/1741-2552/ac7ad6.
- [24] J. Schulte, D. Ashouri, and T. Stieglitz, “The longevity of neural interfaces—mechanical oscillation of thin film metal-based neural electrodes determine stability during electrical stimulation,” *Advanced Functional Materials*, vol. 34, no. 11, p. 2310130, 2024.

- [25] *Neuropace: The rns system*, Accessed: Jan. 31, 2025. [Online]. Available: <https://www.neuropace.com/the-rns-system/>.
- [26] P. A. Starr, “Totally implantable bidirectional neural prostheses: A flexible platform for innovation in neuromodulation,” *Frontiers in Neuroscience*, vol. 12, no. SEP, pp. 1–5, 2018, ISSN: 1662453X. DOI: 10.3389/fnins.2018.00619.
- [27] NeuroPace, *Rns system patient manual for the rns neurostimulator model rns-300m and model rns-320*, Accessed: Jan. 31, 2025, Jun. 2020. [Online]. Available: https://www.neuropace.com/manuals/Patient_Manual.pdf.
- [28] R. Ranjandish and A. Schmid, “A review of microelectronic systems and circuit techniques for electrical neural recording aimed at closed-loop epilepsy control,” *Sensors (Switzerland)*, vol. 20, no. 19, pp. 1–36, 2020, ISSN: 14248220. DOI: 10.3390/s20195716.
- [29] S. Stanslaski, P. Afshar, P. Cong, J. Giftakis, et al., “Design and validation of a fully implantable, chronic, closed-loop neuromodulation device with concurrent sensing and stimulation,” *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, vol. 20, no. 4, pp. 410–421, 2012, ISSN: 15344320. DOI: 10.1109/TNSRE.2012.2183617.
- [30] S. Stanslaski, J. Herron, T. Chouinard, D. Bourget, et al., “A Chronically Implantable Neural Coprocessor for Investigating the Treatment of Neurological Disorders,” *IEEE Transactions on Biomedical Circuits and Systems*, vol. 12, no. 6, pp. 1230–1245, 2018, ISSN: 19324545. DOI: 10.1109/TBCAS.2018.2880148.
- [31] *Percept™ pc neurostimulator*, Accessed: Jan. 31, 2025. [Online]. Available: <https://www.medtronic.com/us-en/healthcare-professionals/products/neurological/deep-brain-stimulation-systems/percept-pc.html>.
- [32] M. Hoffman, *Percept pc deep brain stimulation system gets go-ahead*, Accessed: Jan. 31, 2025. [Online]. Available: <https://www.neurologylive.com/view/percept-pc-deep-brain-stimulation-system-gets-goahead>.
- [33] M. M. Sorkhabi, M. Benjaber, P. Brown, and T. Denison, “Physiological artifacts and the implications for brain-machine-interface design,” *Conference proceedings. IEEE In-*

- ternational Conference on Systems, Man, and Cybernetics*, vol. 2020, p. 1498, Oct. 2020, ISSN: 1062922X. DOI: 10.1109/SMC42975.2020.9283328.
- [34] D. Prutchi, *Medtronic receives approval for its perceptTM pc neurostimulator with brainsenseTM technology*, Accessed: Jan. 31, 2025. [Online]. Available: <http://www.implantable-device.com/2020/06/26/medtronic-receives-approval-for-its-percept-pc-neurostimulator-with-brainsense-technology/>.
- [35] *Brain interchange system*, Accessed: Jan. 31, 2025. [Online]. Available: <https://www.cortec-neuro.com/solutions/complete-system/>.
- [36] A. T. Avestruz, W. Santa, D. Carlson, R. Jensen, et al., “A 5 μW /channel spectral analysis IC for chronic bidirectional brainmachine interfaces,” *IEEE Journal of Solid-State Circuits*, vol. 43, no. 12, pp. 3006–3024, 2008, ISSN: 00189200. DOI: 10.1109/JSSC.2008.2006460.
- [37] P. Cong, P. Karande, J. Landes, R. Corey, et al., “A 32-channel modular bi-directional neural interface system with embedded DSP for closed-loop operation,” *European Solid-State Circuits Conference*, pp. 99–102, 2014, ISSN: 19308833. DOI: 10.1109/ESSCIRC.2014.6942031.
- [38] D. Rozgić, V. Hokinikyan, W. Jiang, I. Akita, et al., “A 0.338 cm³, artifact-free, 64-contact neuromodulation platform for simultaneous stimulation and sensing,” *IEEE Transactions on Biomedical Circuits and Systems*, vol. 13, no. 1, pp. 38–55, 2019. DOI: 10.1109/TBCAS.2018.2889040.
- [39] A. Zhou, S. R. Santacruz, B. C. Johnson, G. Alexandrov, et al., “A wireless and artefact-free 128-channel neuromodulation device for closed-loop stimulation and recording in non-human primates,” *Nature Biomedical Engineering*, vol. 3, no. 1, pp. 15–26, 2019, ISSN: 2157846X. DOI: 10.1038/s41551-018-0323-x.
- [40] F. H. Noshahr and M. Nabavi, “Multi-Channel Neural Recording Implants : A Review,” pp. 1–29, 2020. DOI: 10.3390/s20030904.

- [41] D. Luo, S. Member, M. Zhang, S. Member, et al., “A Low-Noise Chopper Amplifier Designed for Multi-Channel Neural Signal Acquisition,” *IEEE Journal of Solid-State Circuits*, vol. 54, no. 8, pp. 2255–2265, 2019. DOI: 10.1109/JSSC.2019.2913101.
- [42] Y. Liu, Z. Zhou, Y. Zhou, W. Li, et al., “electronics A Low-Noise Chopper Amplifier with Offset and,” pp. 1–12, 2020.
- [43] K. Yoshida and K. Horch, “Selective stimulation of peripheral nerve fibers using dual intrafascicular electrodes,” *IEEE Transactions on Biomedical Engineering*, vol. 46, no. 2, pp. 167–175, 1999. DOI: 10.1109/10.740875.
- [44] S. Raspopovic, M. Capogrosso, F. Petrini, and et al., “Restoring natural sensory feedback in real-time bidirectional hand prostheses,” *Science Translational Medicine*, vol. 6, no. 222, 222ra19, 2014. DOI: 10.1126/scitranslmed.3006820.
- [45] T. Davis, F. Wark, G. Hutchinson, and et al., “Restoration of sensation in upper-limb amputees via the utah slanted electrode array: Performance in chronic implants,” *Journal of Neural Engineering*, vol. 13, no. 5, p. 056002, 2016. DOI: 10.1088/1741-2560/13/5/056002.
- [46] E. H. Rijnbeek, N. Eleveld, and W. Olthuis, “Update on peripheral nerve electrodes for closed-loop neuroprosthetics,” *Frontiers in Neuroscience*, vol. 12, p. 314838, MAY May 2018, ISSN: 1662453X. DOI: 10.3389/FNINS.2018.00350/BIBTEX.
- [47] G. E. Loeb and R. A. Peck, “Cuff electrodes for chronic stimulation and recording of peripheral nerve activity,” eng, *Journal of neuroscience methods*, vol. 64, no. 1, pp. 95–103, Jan. 1996, ISSN: 0165-0270 (Print). DOI: 10.1016/0165-0270(95)00123-9.
- [48] A. Benabid, P. Pollak, C. Gross, D. Hoffmann, et al., “Acute and long-term effects of subthalamic nucleus stimulation in parkinson’s disease,” *Stereotactic and functional neurosurgery*, vol. 62, no. 1-4, pp. 76–84, 1994.
- [49] A. Schulze-Bonhage, “Deep brain stimulation: A new approach to the treatment of epilepsy,” *Deutsches Arzteblatt international*, vol. 106 24, pp. 407–12, 2009.

- [50] A. L. Benabid, P. Pollak, D. Gao, D. Hoffmann, et al., “Chronic electrical stimulation of the ventralis intermedius nucleus of the thalamus as a treatment of movement disorders,” *Journal of neurosurgery*, vol. 84, no. 2, pp. 203–214, 1996.
- [51] S. F. Lempka, S. Miocinovic, M. D. Johnson, J. L. Vitek, et al., “In vivo impedance spectroscopy of deep brain stimulation electrodes,” *Journal of Neural Engineering*, vol. 6, no. 4, 2009, ISSN: 17412560. DOI: 10.1088/1741-2560/6/4/046001.
- [52] X. F. Wei and W. M. Grill, “Impedance characteristics of deep brain stimulation electrodes in vitro and in vivo.,” eng, *Journal of neural engineering*, vol. 6, no. 4, p. 46 008, Aug. 2009, ISSN: 1741-2552 (Electronic). DOI: 10.1088/1741-2560/6/4/046008.
- [53] A. N. Almeida, V. Martinez, and W. Feindel, “The first case of invasive eeg monitoring for the surgical treatment of epilepsy: Historical significance and context,” *Epilepsia*, vol. 46, pp. 1082–1085, 7 Jul. 2005, ISSN: 1528-1167. DOI: 10.1111/J.1528-1167.2005.66404.X.
- [54] C. Herff, D. J. Krusienski, and P. Kubben, “The potential of stereotactic-eeg for brain-computer interfaces: Current progress and future directions,” *Frontiers in Neuroscience*, vol. 14, p. 123, Feb. 2020, ISSN: 1662453X. DOI: 10.3389/FNINS.2020.00123.
- [55] B. Rubehn, C. Bosman, R. Oostenveld, P. Fries, et al., “A mems-based flexible multi-channel ecog-electrode array,” *Journal of Neural Engineering*, vol. 6, no. 3, p. 36 003, May 2009. DOI: 10.1088/1741-2560/6/3/036003.
- [56] E. C. Leuthardt, G. Schalk, J. R. Wolpaw, J. G. Ojemann, et al., “A brain-computer interface using electrocorticographic signals in humans,” *Journal of Neural Engineering*, vol. 1, no. 2, pp. 63–71, Jun. 2004. DOI: 10.1088/1741-2560/1/2/001.
- [57] G. Hong and C. M. Lieber, “Novel electrode technologies for neural recordings,” *Nature Reviews Neuroscience*, vol. 20, pp. 330–345, 6 Jun. 2019, ISSN: 14710048. DOI: 10.1038/s41583-019-0140-6.
- [58] S. Liu, Y. Zhao, W. Hao, X. D. Zhang, et al., “Micro- and nanotechnology for neural electrode-tissue interfaces,” *Biosensors and Bioelectronics*, vol. 170, Dec. 2020, ISSN: 18734235. DOI: 10.1016/j.bios.2020.112645.

- [59] M. E. J. Obien, K. Deligkaris, T. Bullmann, D. J. Bakkum, et al., “Revealing neuronal function through microelectrode array recordings,” *Frontiers in Neuroscience*, vol. 9, p. 423, JAN 2015, ISSN: 1662453X. DOI: 10.3389/fnins.2014.00423.
- [60] J. E. B. Randles, “Kinetics of rapid electrode reactions,” *Discussions of the Faraday Society*, vol. 1, no. 0, pp. 11–19, 1947, ISSN: 0366-9033. DOI: 10.1039/DF9470100011.
- [61] R. R. Harrison, “The design of integrated circuits to observe brain activity,” *Proceedings of the IEEE*, vol. 96, no. 7, pp. 1203–1216, 2008. DOI: 10.1109/JPROC.2008.922562.
- [62] M. J. Nelson and P. Pouget, “Do electrode properties and impedance affect neural recordings?” *Journal of Neuroscience Methods*, vol. 188, no. 1, pp. 53–59, 2010. DOI: 10.1016/j.jneumeth.2010.01.033.
- [63] G. Buzsáki, C. A. Anastassiou, and C. Koch, “The origin of extracellular fields and currents—eeg, ecog, lfp and spikes,” *Nature Reviews Neuroscience*, vol. 13, no. 6, pp. 407–420, 2012. DOI: 10.1038/nrn3241.
- [64] D. A. Henze, Z. Borhegyi, J. Csicsvari, A. Mamiya, et al., “Intracellular features predicted by extracellular recordings in the hippocampus in vivo,” *Journal of Neurophysiology*, vol. 84, no. 1, pp. 390–400, 2000. DOI: 10.1152/jn.2000.84.1.390.
- [65] S. F. Cogan, “Neural stimulation and recording electrodes,” *Annual Review of Biomedical Engineering*, vol. 10, no. 1, pp. 275–309, 2008. DOI: 10.1146/annurev.bioeng.10.061807.160518.
- [66] R. A. Green, N. H. Lovell, G. G. Wallace, and L. A. Poole-Warren, “Conducting polymers for neural interfaces: Challenges in developing an effective long-term implant,” *Biomaterials*, vol. 29, no. 24-25, pp. 3393–3399, 2008. DOI: 10.1016/j.biomaterials.2008.04.047.
- [67] C. Boehler, C. Kleber, N. Martini, Y. Xie, et al., “Actively controlled release of dexamethasone from neural microelectrodes in a chronic in vivo study,” *Biomaterials*, vol. 237, p. 119782, 2020. DOI: 10.1016/j.biomaterials.2020.119782.

- [68] C. Boehler, S. Carli, L. Fadiga, T. Stieglitz, et al., “Tutorial: guidelines for standardized performance tests for electrodes intended for neural interfaces and bioelectronics,” *Nature Protocols*, vol. 15, no. 11, pp. 3557–3578, 2020, ISSN: 17502799. DOI: 10.1038/s41596-020-0389-2.
- [69] D. A. Robinson, “The electrical properties of metal microelectrodes,” *Proceedings of the IEEE*, vol. 56, no. 6, pp. 1065–1071, 1968. DOI: 10.1109/PROC.1968.6458.
- [70] D. R. Merrill, M. Bikson, and J. G. Jefferys, “Electrical stimulation of excitable tissue: Design of efficacious and safe protocols,” *Journal of Neuroscience Methods*, vol. 141, no. 2, pp. 171–198, 2005, ISSN: 01650270. DOI: 10.1016/j.jneumeth.2004.10.020.
- [71] L. S. Robblee and T. L. Rose, “Electrode materials and processes for biomedical applications,” *Proceedings of the IEEE*, vol. 68, no. 3, pp. 301–308, 1980. DOI: 10.1109/PROC.1980.11692.
- [72] D. B. McCreery, W. F. Agnew, T. G. H. Yuen, and L. A. Bullara, “Charge density and charge per phase as cofactors in neural injury induced by electrical stimulation,” *IEEE Transactions on Biomedical Engineering*, vol. 37, no. 10, pp. 996–1001, 1990. DOI: 10.1109/10.58588.
- [73] J. D. Weiland, D. J. Anderson, and M. S. Humayun, “In vitro electrical properties for iridium oxide versus titanium nitride stimulating electrodes,” *IEEE Transactions on Biomedical Engineering*, vol. 49, pp. 1574–1579, 12 I Dec. 2002, ISSN: 00189294. DOI: 10.1109/TBME.2002.805487.
- [74] G. Schiavone, X. Kang, F. Fallegger, J. Gandar, et al., “Guidelines to study and develop soft electrode systems for neural stimulation,” *Neuron*, vol. 108, no. 2, pp. 238–258, 2020, ISSN: 0896-6273. DOI: 10.1016/j.neuron.2020.10.010.
- [75] B.-Y. Chang and S.-M. Park, “Electrochemical impedance spectroscopy,” *Annual Review of Analytical Chemistry*, vol. 3, no. 1, p. 207, 2010.
- [76] A. Sridharan and J. Muthuswamy, “Quantitative assessment of the mechanical properties of the neural interface,” in *Handbook of Neuroengineering*, N. V. Thakor, Ed.

- Singapore: Springer Nature Singapore, 2023, pp. 213–259, ISBN: 978-981-16-5540-1. DOI: 10.1007/978-981-16-5540-1_4.
- [77] W. Franks, I. Schenker, P. Schmutz, and A. Hierlemann, “Impedance Characterization and Modeling of Electrodes for Biomedical Applications,” en, *IEEE Transactions on Biomedical Engineering*, vol. 52, no. 7, 2005, ISSN: 0018-9294. DOI: 10.1109/TBME.2005.847523.
- [78] J. R. Macdonald and W. B. Johnson, “Fundamentals of Impedance Spectroscopy,” in *Impedance Spectroscopy*. John Wiley & Sons, Ltd, 2005, ch. 1, pp. 1–26, ISBN: 9780471716242. DOI: 10.1002/0471716243.ch1.
- [79] C. Hill, “Impedance Spectroscopy,” vol. 20, pp. 289–305, 1992.
- [80] E. Barsoukov and J. R. Macdonald, *Impedance Spectroscopy: Theory, Experiment, and Applications*, 3rd. John Wiley Sons, 2018. DOI: 10.1002/9781119381860.
- [81] M. E. Orazem and B. Tribollet, *Electrochemical Impedance Spectroscopy*, 2nd. John Wiley Sons, 2017. DOI: 10.1002/9781119381877.
- [82] A. C. Lazanas and M. I. Prodromidis, “Electrochemical impedance spectroscopy—a tutorial,” *ACS Measurement Science Au*, vol. 3, pp. 162–193, 3 Jun. 2023, ISSN: 2694250X. DOI: 10.1021/acsmesuresciau.2c00070.
- [83] P. Fortin, R. Duclos, M. Lefebvre, N. Steiner, et al., “Multi-sine eis for early detection of pemfc failure modes,” *Frontiers in Energy Research*, vol. 10, p. 855985, 2022. DOI: 10.3389/fenrg.2022.855985.
- [84] Gamry Instruments, *Optieis™: A multisine implementation*, <https://www.gamry.com/assets/Uploads/OptiEIS-multisine-implementation.pdf>, Accessed: October 2025, 2011.
- [85] M. C. H. McKubre and D. D. Macdonald, “Measuring Techniques and Data Analysis,” in *Impedance Spectroscopy*. John Wiley & Sons, Ltd, 2005, ch. 3, pp. 129–204, ISBN: 9780471716242. DOI: 10.1002/0471716243.ch3.

- [86] F. Mivalt, V. Kremen, V. Sladky, J. Cui, et al., “Impedance rhythms in human limbic system,” *Journal of Neuroscience*, vol. 43, no. 39, 2023. DOI: 10.1523/JNEUROSCI.0241-23.2023.
- [87] S. M. Goetz, B. Center, J. A. Barnhorst, and J. M. Hartmann, *Automated impedance measurement of an mplantable medical device*, Oct. 2011.
- [88] G. S. M, B. J. A, and H. J. M, “Automated impedance measurement of an implantable medical device,” Granted Patent US 6978171 B2, Accessed: Jan. 31, 2025. [Online]. Available: <https://lens.org/187-995-404-800-507>.
- [89] M. Haas, J. Anders, and M. Ortmanns, “A bidirectional neural interface featuring a tunable recorder and electrode impedance estimation,” *Proceedings - 2016 IEEE Biomedical Circuits and Systems Conference, BioCAS 2016*, pp. 372–375, 2016. DOI: 10.1109/BIOCAS.2016.7833809.
- [90] H. Ko, T. Lee, J. H. Kim, J. A. Park, et al., “Ultralow-power bioimpedance ic with intermediate frequency shifting chopper,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 63, pp. 259–263, 3 Mar. 2016, ISSN: 15583791. DOI: 10.1109/TCSII.2015.2483258.
- [91] M. Zamani, Y. Rezaeiyan, O. Shoaie, and W. A. Serdijn, “A 1.55 μ w bio-impedance measurement system for implantable cardiac pacemakers in 0.18 μ m cmos,” *IEEE Transactions on Biomedical Circuits and Systems*, vol. 12, pp. 211–221, 1 Feb. 2018, ISSN: 19324545. DOI: 10.1109/TBCAS.2017.2776528.
- [92] C. W. Huang, C. H. Chung, R. S. Syu, and C. Y. Wu, “The design of cmos electrode-Tissue impedance measurement circuit using differential current switch with cmfb bias for implantable neuro-modulation socs,” *IEEE*, 2019, pp. 19–22, ISBN: 9781509006175. DOI: 10.1109/BIOCAS.2019.8919039.
- [93] S. Robinet, P. Audebert, G. Régis, B. Zongo, et al., “A low-power 0.7 μ v rms 32-channel mixed-signal circuit for ecog recordings,” *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 1, pp. 451–460, 4 Dec. 2011, ISSN: 21563357. DOI: 10.1109/JETCAS.2011.2180835.

- [94] C. S. Mestais, G. Charvet, F. Sauter-Starace, M. Foerster, et al., “Wimagine: Wireless 64-channel ecog recording implant for long term clinical applications,” *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, vol. 23, pp. 10–21, 1 Jan. 2015, ISSN: 15344320. DOI: 10.1109/TNSRE.2014.2333541.
- [95] K. A. Sillay, P. Rutecki, K. Cicora, G. Worrell, et al., “Long-term measurement of impedance in chronically implanted depth and subdural electrodes during responsive neurostimulation in humans,” *Brain Stimulation*, vol. 6, pp. 718–726, 5 Sep. 2013, ISSN: 1935861X. DOI: 10.1016/j.brs.2013.02.001.
- [96] *Rhs2116 digital electrophysiology stimulator/amplifier chip*, RHS2116, [Accessed: Jan. 31, 2025], IntanTechnologies, 2016. [Online]. Available: https://intantech.com/files/Intan_RHS2116_datasheet.pdf.
- [97] S. S. Wong, J. Ekanayake, Y. Liu, and T. G. Constandinou, “An impedance probing system for real-time intraoperative brain tumour tissue discrimination,” *2019 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, pp. 1–4, 2019.
- [98] E. Patrick, M. E. Orazem, J. C. Sanchez, and T. Nishida, “Corrosion of tungsten microelectrodes used in neural recording applications,” *Journal of Neuroscience Methods*, vol. 198, no. 2, pp. 158–171, 2011. DOI: 10.1016/j.jneumeth.2011.03.012.
- [99] P. Takmakov, K. Ruda, K. S. Phillips, I. S. Isayeva, et al., “Rapid evaluation of the durability of cortical neural implants using accelerated aging with reactive oxygen species,” *Journal of Neural Engineering*, vol. 12, no. 2, p. 026003, 2015. DOI: 10.1088/1741-2560/12/2/026003.
- [100] M. G. Street, C. G. Welle, and P. A. Takmakov, “Automated reactive accelerated aging for rapid in vitro evaluation of neural implant performance,” *Review of Scientific Instruments*, vol. 89, no. 9, 2018, ISSN: 10897623. DOI: 10.1063/1.5024686.
- [101] V. Manatchinapisit, A. Rapeaux, I. Williams, and T. G. Constandinou, “Accelerated testing of electrode degradation for validation of new implantable neural interfaces,” in *2022 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, IEEE, 2022. DOI: 10.1109/BioCAS54905.2022.9948555.

- [102] S. Meijs, M. Fjorback, C. Jensen, S. Sørensen, et al., “Influence of fibrous encapsulation on electro-chemical properties of tin electrodes,” *Medical Engineering & Physics*, vol. 38, no. 5, pp. 468–476, 2016, ISSN: 1350-4533. DOI: 10.1016/j.medengphy.2016.02.010.
- [103] K. Krukiewicz, “Electrochemical impedance spectroscopy as a versatile tool for the characterization of neural tissue: A mini review,” *Electrochemistry Communications*, vol. 116, p. 106 742, 2020, ISSN: 1388-2481. DOI: 10.1016/j.elecom.2020.106742.
- [104] A. S. Idil and N. Donaldson, “The use of tungsten as a chronically implanted material,” *Journal of Neural Engineering*, vol. 15, no. 2, p. 021 006, Feb. 2018.
- [105] G. Y. Fridman and C. C. Della Santina, “Safe direct current stimulation to expand capabilities of neural prostheses,” *Frontiers in Neuroscience*, vol. 7, p. 263, 2013. DOI: 10.3389/fnins.2013.00263.
- [106] W. F. Agnew and D. B. McCreery, “Considerations for safety in chronic stimulation of the central nervous system,” *IEEE Transactions on Biomedical Engineering*, vol. 22, no. 5, pp. 393–405, 1975. DOI: 10.1109/TBME.1975.324478.
- [107] K. J. Laidler, “The development of the arrhenius equation,” *Journal of Chemical Education*, vol. 61, no. 6, pp. 494–498, 1984. DOI: 10.1021/ed061p494.
- [108] M. C. Zaghdoudi and M. Fréchet, “Origin and justification of the use of the arrhenius relation in material ageing studies,” *Applied Sciences*, vol. 11, no. 9, p. 4075, 2021. DOI: 10.3390/app11094075.
- [109] D. Hukins, A. Mahomed, and S. Kukureka, “Accelerated aging for testing polymeric biomaterials and medical devices,” *Medical Engineering & Physics*, vol. 30, no. 10, pp. 1270–1274, 2008, ISSN: 1350-4533. DOI: 10.1016/j.medengphy.2008.06.001.
- [110] C. Boehler, S. Carli, L. Fadiga, T. Stieglitz, et al., “Tutorial: Guidelines for standardized performance tests for electrodes intended for neural interfaces and bioelectronics,” *Nature Protocols*, vol. 15, no. 11, pp. 3557–3578, 2020.
- [111] G. S. Kelsey, “The anodic oxidation of tungsten in aqueous base,” *Journal of The Electrochemical Society*, vol. 124, pp. 814–819, 1977. DOI: 10.1149/1.2133418.
- [112] M. Pourbaix, “Atlas of Electrochemical Equilibria in Aqueous Solutions,”

- [113] T. Fujimoto, T. Ando, K. Tokunaga, and R. Sakamoto, “Hydrogen blistering and cracking of tungsten exposed to high flux hydrogen plasma,” *Journal of Nuclear Materials*, vol. 294, no. 3, pp. 338–346, 2001.
- [114] S. Li, H. Liu, J. Chen, Z. Wang, et al., “Hydrogen embrittlement and fracture behaviour of tungsten wires under cathodic polarisation,” *Corrosion Science*, vol. 70, pp. 195–204, 2013.
- [115] J. Hu, X. Zhang, and G. Luo, “Hydrogen effects on the mechanical properties of tungsten: A review,” *Journal of Nuclear Materials*, vol. 519, pp. 1–14, 2019. DOI: 10.1016/j.jnucmat.2019.03.005.
- [116] M. J. Brady, “The electrochemical etching of tungsten and other refractory metals,” *Journal of the Electrochemical Society*, vol. 112, no. 12, pp. 1223–1229, 1965, PMID: 20604205, ISSN: 0013-4651. DOI: 10.1149/1.2423966. [Online]. Available: <https://doi.org/10.1149/1.2423966>.
- [117] R. A. Green, N. H. Lovell, and L. A. Poole-Warren, “Electrochemical impedance spectroscopy for monitoring neural interface stability,” *Biomaterials*, vol. 35, no. 25, pp. 7017–7033, 2014. DOI: 10.1016/j.biomaterials.2014.04.022.
- [118] A. Hassibi and T. H. Lee, “Modeling and measurement of electrode impedance changes during electrochemical degradation,” *IEEE Transactions on Biomedical Circuits and Systems*, vol. 12, no. 2, pp. 282–292, 2018. DOI: 10.1109/TBCAS.2018.2803021.
- [119] A. J. Bard and L. R. Faulkner, *Electrochemical Methods: Fundamentals and Applications*. John Wiley & Sons, 2001.
- [120] A. Lasia, *Electrochemical Impedance Spectroscopy and its Applications*. Springer, 2014.
- [121] K. Wang, C. Tian, and H. Zhang, “Impedance evolution of microelectrodes during long-term neural recording,” *Frontiers in Neuroscience*, vol. 14, p. 137, 2020. DOI: 10.3389/fnins.2020.00137.
- [122] V. Manatchinapisit and T. G. Constandinou, “A portable and low-cost electrochemical impedance spectroscopy platform for the characterisation of implantable electrodes,” in

- 2024 46th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC), 2024, pp. 1–5. DOI: 10.1109/EMBC53108.2024.10782309.
- [123] V. M. Woods, I. F. Triantis, and C. Toumazou, “Offset prediction for charge-balanced stimulus waveforms,” *Journal of Neural Engineering*, vol. 8, no. 4, p. 046032, 2011. DOI: 10.1088/1741-2560/8/4/046032.
- [124] P. Kassanos, I. F. Triantis, and A. Demosthenous, “A CMOS Magnitude/Phase Measurement Chip for Impedance Spectroscopy,” *IEEE Sensors J.*, vol. 13, no. 6, pp. 2229–2236, 2013, ISSN: 1530-437X, 1558-1748. DOI: 10.1109/JSEN.2013.2251628.
- [125] W. R. Lionheart, J. Kaipio, and C. N. McLeod, “Generalized optimal current patterns and electrical safety in eit,” *Physiological Measurement*, vol. 22, pp. 85–90, 1 Feb. 2001, ISSN: 0967-3334. DOI: 10.1088/0967-3334/22/1/311.
- [126] S. S. Wong, J. Ekanayake, Y. Liu, and T. G. Constandinou, “An impedance probing system for real-time intraoperative brain tumour tissue discrimination,” in *2019 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, Nara, Japan: IEEE, 2019, pp. 1–4, ISBN: 978-1-5090-0617-5. DOI: 10.1109/BIOCAS.2019.8918743.
- [127] Texas Instruments, “Analysis of improved howland current pump configurations,” Texas Instruments, Application Note SBOA437A, Oct. 2020, Rev. A, revised Feb. 2023. [Online]. Available: <https://www.ti.com/lit/an/sboa437a/sboa437a.pdf>.
- [128] Analog Devices, Inc., *Mt-031 tutorial: Op amp output phase-reversal and input over-voltage protection*, Application Note MT-031, Rev. 0, 2009. [Online]. Available: <https://www.analog.com/media/en/training-seminars/tutorials/MT-031.pdf>.
- [129] S. Franco, *Analog Circuit Design: Discrete and Integrated*. New York: McGraw-Hill Education, 2015, ISBN: 9780078028199.
- [130] P. Horowitz and W. Hill, *The Art of Electronics*, 3rd. Cambridge: Cambridge University Press, 2015, ISBN: 9780521809269.
- [131] S. S. Wong, J. Ekanayake, Y. Liu, and T. G. Constandinou, “An impedance probing system for real-time intraoperative brain tumour tissue discrimination,” in *2019 IEEE*

- Biomedical Circuits and Systems Conference (BioCAS)*, IEEE, 2019. DOI: 10.1109/BIOCAS.2019.8918743.
- [132] A. R. Harris, D. B. Grayden, and S. E. John, “Electrochemistry in a Two- or Three-Electrode Configuration to Understand Monopolar or Bipolar Configurations of Platinum Bionic Implants,” *Micromachines (Basel)*, vol. 14, no. 4, p. 722, Mar. 2023, ISSN: 2072-666X. DOI: 10.3390/mi14040722.
- [133] V. Manatchinapisit, P. Feng, L. Xie, and T. G. Constandinou, “An impedance characterisation circuit for implantable research platforms,” in *2024 19th Conference on Ph.D Research in Microelectronics and Electronics (PRIME)*, 2024, pp. 1–4. DOI: 10.1109/PRIME61930.2024.10559709.
- [134] A. Mifsud, J. Shen, P. Feng, L. Xie, et al., “A CMOS-based Characterisation Platform for Emerging RRAM Technologies,” in *2022 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2022, pp. 75–79. DOI: 10.1109/ISCAS48785.2022.9937343.
- [135] L. Xie, J. Shen, A. Mifsud, C. Wang, et al., “A wide dynamic range read-out system for resistive switching technology,” in *Proceedings - IEEE International Symposium on Circuits and Systems*, vol. 2022-May, Institute of Electrical and Electronics Engineers Inc., 2022, pp. 2003–2007, ISBN: 9781665484855. DOI: 10.1109/ISCAS48785.2022.9937616.
- [136] C. Wang, “High-resolution peripheral circuits for multi-state memristors and their related applications,” 2024. DOI: 10.25560/111923.
- [137] S. Yan, J. Hu, T. Song, and E. Sanchez-Sinencio, “Constant- $g_{\text{sub m}}$ techniques for rail-to-rail cmos amplifier input stages: A comparative study,” in *2005 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2005. DOI: 10.1109/ISCAS.2005.1465151.
- [138] V. Saxena and R. Baker, “Indirect feedback compensation of CMOS op-amps,” in *2006 IEEE Workshop on Microelectronics and Electron Devices, 2006. WMED '06.*, 2006, 2 pp.–4. DOI: 10.1109/WMED.2006.1678278.