A low-cost and efficient fault detection and location algorithm for LVDC microgrid

Chengwei Liu, Joan-Marc Rodriguez-Bernuz, Adrià Junyent-Ferré
Department of Electrical and Electronic Engineering
Imperial College London
cl820@ic.ac.uk

***Abstract*—Low voltage DC (LVDC) microgrids have many potential advantages for the electrification of rural developing areas. In the long term, these micro-grids could be interconnected to create local mini-grids, which would enhance resilience and power supply stability. Despite their advantages, effective protection of these networks remains a challenge that is holding back their adoption. Thus, this paper presents a low-cost and efficient fault detection and location algorithm for the interconnection of LVDC microgrids. This algorithm is specially tailored for rural areas of difficult access in developing countries since it relies on inexpensive auxiliary devices. To be specific, the algorithm locates the fault by coordinating power converters and relays. It only uses relays and does not require extra high sampling rate sensors, which simplifies implementation and cost-effectiveness. The communication bandwidth is also very low. The algorithm can be effective for both low impedance and high impedance faults. In addition, it could be easily adaptive to different topologies. A DC network with ring structure is set up in Simulink to test the proposed algorithm. The simulation results shows the effectiveness of the proposed algorithm for low and high impedance faults.**

***Index Terms*—LVDC microgrids, mini-grid, fault location method, low-cost**

I. Introduction

At present, there is still an estimated total of 1.1 billion people lacking access to electricity, which is of special concern in rural areas of developing countries, such as remote locations of Sub-Saharan Africa [1]. LVDC microgrids are gaining momentum in the electrification of rural areas due to several advantages, such as fewer conversion stages, and simpler control algorithms [2], [3]. In the long term, these microgrids could be integrated into a larger countrywide system such that electricity systems could be built following a bottom-up approach. This aggregation could bring benefits in terms of better utilization of the generation and energy storage units and enhanced resilience [4]. Despite numerous advantages, the use of the LVDC system also introduces new challenges on their deployment, especially on the protection. The short-circuit (SC) fault could occur on the connection lines, which can bring huge damage to the whole DC grid. On one hand, the DC systems cannot be effectively protected by AC protection schemes since DC current does not have a zero-crossing point [5]. The DC circuit breaker (DCCB) is rather expensive, which is not affordable for rural areas. On the other hand, it is hard to achieve system maintenance by human intervention for microgrids located in remote regions. How to detect and locate the fault autonomously with low cost is of high significance for the safe operation of the DC systems.

Up to now, different fault location methods have been proposed. The traveling-waves-based method can locate the fault by using the time taken by the traveling wave to propagate along the line [6], [7]. However, this method is only suitable for long transmission lines and requires expensive measurement equipment. Another strategy is the differential protection method, which can detect and isolate faults by distinguishing between the current magnitudes and direction in a specified time [8], [9]. This method is independent of fault impedance and suitable for different types of system topologies. However, it requires fast communications and precise current measurement synchronization, which would be expensive and, therefore, a drawback for their deployment in LV microgrids, especially in developing countries. By combination of unit and non–unit–based protection schemes, event-based protection methods have been proposed [10]. Compared to the differential protection method, it does not require fast date synchronization and communication. However, this method is unable to classify high impedance faults, which limits their applicability to the LVDC system. Alternatively, injection-based fault location methods have been proposed to locate the fault in the DC system. A non-iterative injection-based fault-location method using a probe power is proposed in [11]. It forms a second-order RLC discharging circuit and locates the fault by extracting the oscillation frequency of the RLC discharging circuit and the attenuation coefficient of the wave-form envelope. Based on [11], the method in [12] considers the effect of attenuation coefficient on the fault location results and reduces the fault location error. However, the operation process of the above method is tedious. Thus, it is difficult to realize the automatic fault location.

In this paper, a low-cost fault detection and location algorithm is proposed for the interconnection of LVDC microgrids, especially those located in areas of difficult access for maintenance. This algorithm does not require extra high sampling rate sensors, which permits the low cost. In addition, it locates the fault by coordinating the converters and relays instead of the DC circuit-breakers (DCCBs), which can decrease the cost further. This algorithm can detect and locate both low impedance and high impedance faults. Meanwhile, it is

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adaptive to different network topologies, showing high flexibility. The rest of the paper is structured as follows. Section II describes the characteristic of the mini-grid. Section III describes the proposed fault detection and location algorithm. Section IV shows simulation results. The paper ends with a conclusion in Section V.

II. System Description

The proposed algorithm is validated on a testing DC network that interconnects three independent microgrids into a ring structure as shown in Fig. 1. Note that each of these microgrids might be designed following different standards, requiring the use of power converters as interface devices. The resulting DC network permits the energy exchange between the interconnected systems, and an upper energy management system (EMS) can dictate the power transfer based on economical criteria [13]. It is assumed that each microgrid connected to the DC network is self-sufficient such that it can handle outages of the DC grid for a certain amount of time. Therefore, the proposed algorithm does need to isolate the fault and re-energize the DC grid instantaneously. In addition, it is assumed that each microgrid is located nearby so that connection distances are short. Thus, the algorithm only needs to locate the faulty line instead of determining the exact location of the fault. In the case of microgrids located in remote regions, the access to carry out the required system maintenance to continue normal operation might become a major handicap which might let the system inoperative over long periods of time. Therefore, the algorithm presented here is designed to permit an autonomous restoration of the DC network in case of a contingency, such that the system becomes operative in a relative short period of time without requiring human intervention. To do so, each of the DC grid lines is equipped with relays at each of its ends which permits to automate the connection and disconnection of lines. Notice that the purpose of these relays is not the protection of the DC grid in the event of a fault but merely to reconfigure the network once the fault is cleared. Likewise, the relay devices are assumed to account for some low-bandwidth communication (eg power line communication (PLC) [14]), which permits the exchange of simple messages amongst the grid-connected converters. Based on these features, the reconfiguration system based on relays is expected to be low cost; thus serving the purpose of designing advanced microgrid systems for remote locations in developing countries.

A. Interface converter

The dual active bridge (DAB) converter is considered as an interface device between the individual microgrids and the DC network due to its advantageous features such as galvanic isolation, bidirectional power flow, good power density, etc. [15]. The DAB is based on two full-bridges interconnected by a step-up transformer (Fig. 1). Each of these full-bridges generates a phase-shifted square AC waveform at the terminals of the transformer. The phase-shift (ϕ) of the voltages applied across the transformer leakage inductance (L_{lk}) determine

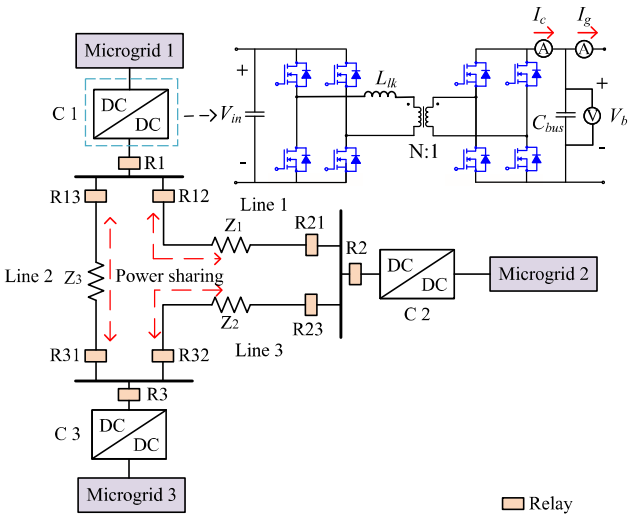

Fig. 1. Illustration of the three microgrid test system.

the converter's power flow. Besides, this converter permits to block fault current in case of contingency, property which is exploited in this work [16]. Finally, it is also assumed that each DAB is equipped with a low-bandwidth communication which permits to exchange of messages amongst the other DABs and the reconfiguration relays.

B. Converter control

The DAB is designed to present two main operating modes based on the state of the system:

1) Normal operation: The DAB operates following a standard single-phase modulation and a power droop regulator is used to permit the tacking of the power references determined by the EMS while distributing the regulation of the DC network across all the converters [4]. This control mode is based on an outer proportional regulator (K_{droop}) which adjusts the terminal voltage reference based on the output power deviation. Besides, an inner loop based on a proportional-integral (PI) regulator tracks the output voltage and determines the phase-shift (ϕ) between bridges. The schematic of this control mode is illustrated in Fig. 2.

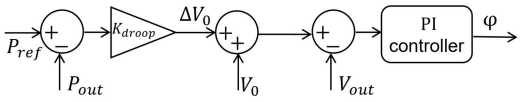

Fig. 2. Diagram of control algorithm in normal operation.

2) Contingency operation: The fault blocking capability of the DAB is used to implement a fault diagnosis strategy to locate faulty lines. Under this operating mode, the DAB's controller is switched to perform controlled current pulses injection into the DC network. The fault-blocking capability of the DAB permits to actively control the current injection in case of short-circuit faults on the DC grid. The current

pulse injection can be easily implemented as a peak current controller [17].

III. Fault detection and location algorithm

The algorithm is divided into two sub-algorithms: fault detection and fault location. The fault detection algorithm has the task of continuously monitoring the system and determining whether a fault has occurred. The following system states are measured: V_b, I_g and I_c (see Fig. 1). It should be highlighted that the sensors required to perform these measurements are integrated in the DAB, which implies that no additional hardware is required. The fault location system is triggered once a fault is detected, and has the objective of locating the faulty segment, isolating it, and re-energize the DC network autonomously.

A. Fault detection

The algorithm is designed to be able to identify both low- and high-impedance faults. Thus, the fault detection algorithm is composed of two different strategies to distinguish them. First, an overcurrent method is set to detect low-impedance faults. Besides, an integral power comparison method is designed to identify high impedance faults. Each of these strategies is run continuously and in parallel.

1) Overcurrent method: This strategy is based on identifying an overcurrent event as a result of a low-impedance fault in a line, which must be identified quickly to avoid a large current excursion that can damage the converter. This method is based on comparing the output current of the DAB against a threshold. This comparison is performed at frequency f_{sw} since this routine is integrated into the low-level controller of the DAB. The over-current criterion is as follows:

$$I_g > I_{th} \tag{1}$$

where I_g is the current injected into the DC grid and I_{th} is the over-current threshold. In this paper, the threshold is set as 1.2 times the rated converter current [18].

2) Integral power comparison method: Although the over-current strategy would detect large current deviations, it might happen that a high-impedance fault does not trigger the over-current condition since the current absorbed by the fault might be below the current threshold. This problem is addressed by introducing the integral power comparison method. During normal operation, the summation of the power entering the DC network must be close to the summation of power leaving the grid (note that a small error must be considered as a consequence of the system losses). Thus, the net sum of the power must be close to zero. This is easily put in place by designating one converter as a master, which would receive the power measurements of the other converter integrating the DC network. If a high impedance fault happened without triggering the overcurrent threshold, it would absorb a steady amount of power which would make that the net sum of power monitored by the master converter deviate from zero. Then, by comparing the summation of power with a predefined threshold that accounts for the system losses, the high impedance fault can be detected easily. However, it might happen that setpoint reference changes or disturbances create energy oscillation at converters terminals which makes the summation of instantaneous net power not add zero (eg. as a result of output capacitors storing/discharging energy during transients). Thus, the power comparison could be performed by integrating the power over a specified time window of time as follows:

$$P_{total} = \sum_{k=1}^{N_{conv}} P_{out_k} \tag{2}$$

$$\underbrace{\sum_{t=1}^{N_w} P_{total_t}}_{P_{int}} > P_{th} \tag{3}$$

where N_{conv} refers to the number of converters of the DC network and P_{out} is the output power of converter k. Next, N_w determines the number of samples considered in the integration window since the master converter receives power measurements from other converters at discrete intervals of time. Then, P_{int} is the aggregated power for the comparison window, and P_{th} is the threshold. Note that P_{th} depends on the integration window and system losses. It is noticeable that a high impedance fault would be detected with a delay because of the integration strategy. However, this is not seen as a drawback since high impedance faults would not draw large currents that could damage the system but rather increase system losses temporarily. As a consequence, low-bandwidth communications can be used to perform the integral power comparison since power checkpoints can be spanned over time.

B. Fault location

The fault location algorithm is designed to be valid with any grid topology. This is achieved by providing the algorithm with a connectivity matrix of the system, which mostly describes the location of the system relays, line segments, and buses. The connectivity matrix of the testing system shown in Fig. 1 is illustrated as an example in Fig. 3.

	Converter			L1		L2		L3		
	C1	C2	C3							
	R1	R2	R3	R12	R21	R13	R31	R23	R32	Relay
Bus B1	1	0	0	1	0	1	0	0	0	
Bus B2	0	1	0	0	1	0	0	0	0	
Bus B3	0	0	1	0	0	0	1	0	1	

Fig. 3. Illustration of the connectivity matrix of system in Fig. 1

The connectivity has as many rows (N) as buses integrate the network and as many columns (M) as relays (eg. N = 3 and M = 9). Then, the first N columns of the matrix refer to the relays interfacing converters, since it is assumed that there is only one converter connected per bus. The remaining number of columns refers to each of the line relays, where each couple of columns correspond to a connection line (ie.

each line has two relays, one at each end). In this matrix, the value '1' means that a specific relay is connected to the corresponding converter whereas '0' means that there is no connection between them. The steps followed by the algorithm to locate the fault and restore operation are described below.

1) Fault isolation: Once a fault is detected by the fault detection algorithm (see Section III-A), the DAB enters in fault-blocking mode and stops feeding current into the fault. Then, the energy stored in the DC network (mostly the energy stored in the converter's output capacitor) discharges through the fault, until the DC voltage of the grid collapses to zero. This could create a large current spike that travels from the output capacitors to the fault, although would not compromise the integrity of the power electronic components. Once the DC network voltage reaches 0 and there is no current between the converter terminals and the fault, all the system relays open to isolate the network lines (Figure 4). This process is shown in the flowchart provided in Fig. 4.

2) Fault Diagnosis: At this point, a fault diagnosis strategy based on a current injection method is started to locate the faulty line. This is achieved by coordinating the pulse current injection brought by the DAB and the relay devices. The algorithm gathers the information of the connectivity matrix and starts a sequential search of the system buses and lines by doing a sweep of columns and rows. Only one bus or line is checked at a time. The relays interfacing with the DABs are checked before the lines since they are placed on the first columns of the connectivity matrix. For example, the algorithm starts checking the first column. This position of the matrix indicates that bus one is connected to R1, which should be closed while all other relays remain open. The '1' is in the first row, showing that converter 1 is connected to R1. Then, converter 1 is required to inject controlled current pulses to determine whether there is a fault on this bus or not. If there is no fault, the bus voltage should increase and remain steady after the current injection. Otherwise, the bus voltage would decrease or even collapse towards 0. Thus, the system voltage can be compared with a threshold to decide whether there is a fault as follows:

$$V_{bus} > V_{th} \tag{4}$$

where V_{bus} is the DC bus voltage and V_{th} is the threshold value. The value of V_{th} is chosen based on the current pulses injected by the DAB and the size of the bus capacitor. By performing a sweep over the columns for the converter relays (eg. R1, R2, and R3), all buses could be checked. If there is no fault on buses, then the checking of the lines starts. It should be noted that all relays on buses are closed before starting the line checking. Besides, the reader should notice that each pair of columns refer to a single line since each line has two relays (see Fig. 3). Then, the sweep continues as with the buses. For example, when L1 is checked, the third and fourth columns of the matrix are considered. The first non-zero element (eg. position 1) implies that L1 is connected to converter 1. Thus, converter 1 is chosen to inject the pulse current into L1 to detect whether there is a fault or not. By performing a sweep over all columns, all lines could be checked.

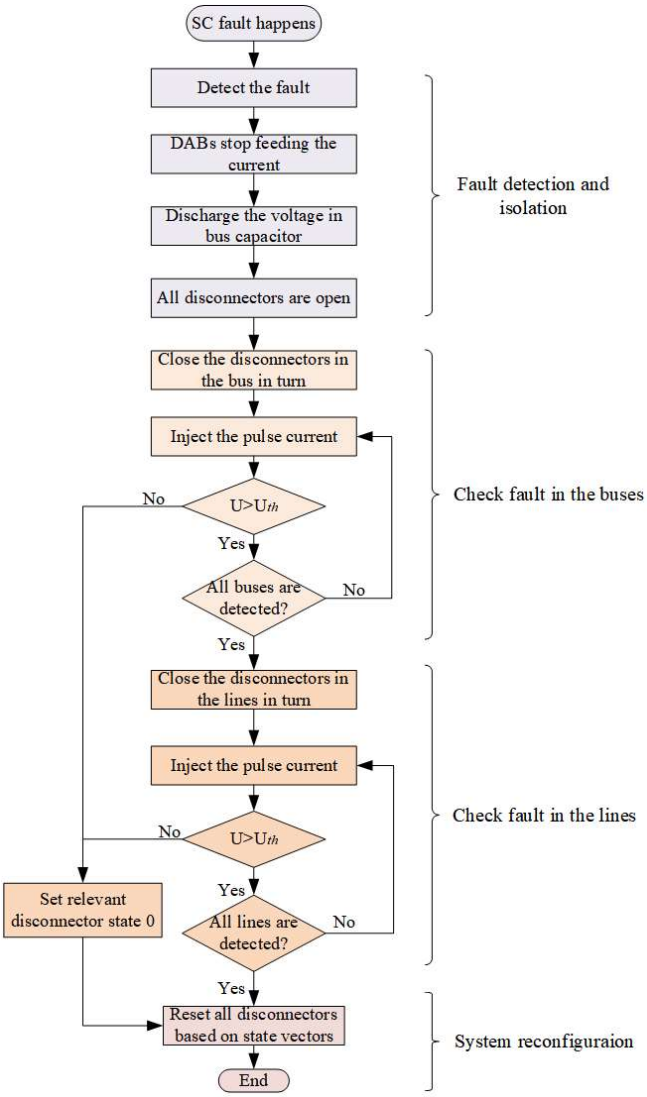

Fig. 4. The diagram of fault location

C. System reconfiguration

Once a fault is found, the algorithm stops, and the system is reconfigured to isolate the faulty element. This is easily performed by checking the corresponding row and column where the algorithm stopped on the connectivity matrix. Note that in the case of a fault located at a bus, all the relays located on the faulty bus could be found by finding the non-zero elements of the corresponding row. For instance, if the fault is on bus 2, the non-zero element in the second row point at relays 2, 21, and 23. If the fault is located on a line, the relays on the faulty line could be easily chosen by the finding corresponding pair of columns. Then, the system relays are returned to their initial status (ie. the status before starting the fault location algorithm) although those corresponding to the

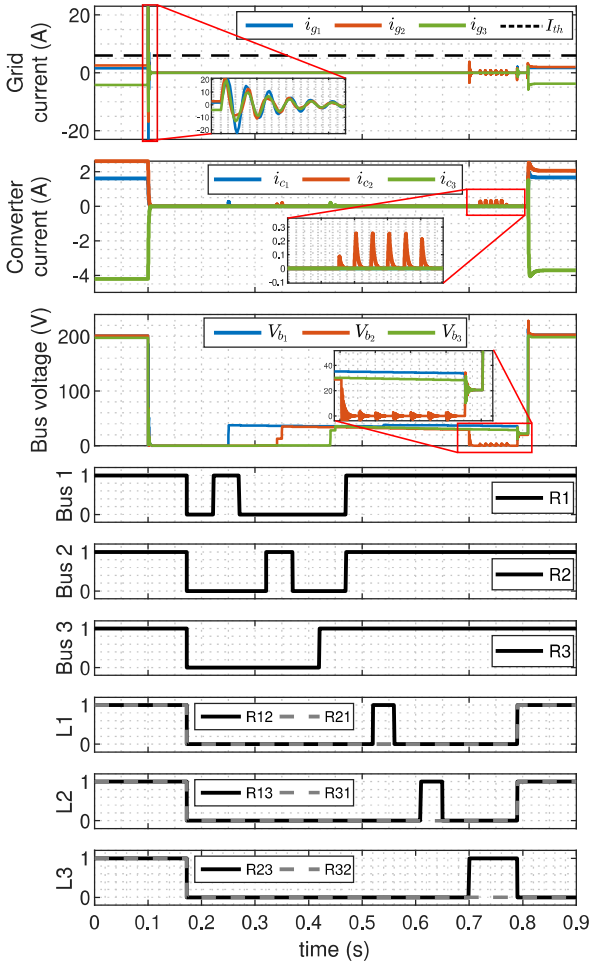

Fig. 5. Simulation results of the low-impedance fault

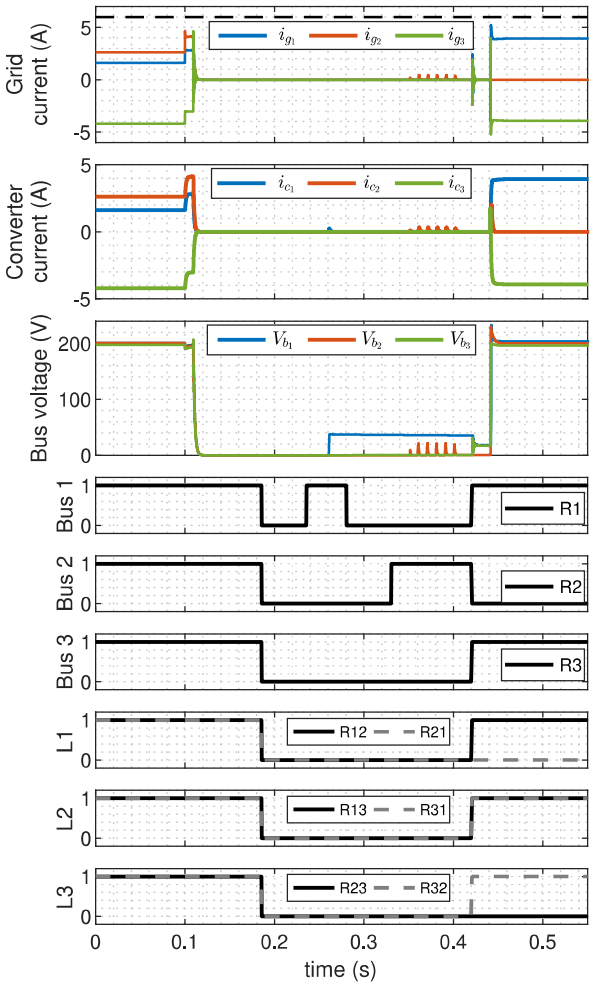

Fig. 6. Simulation results of the high-impedance fault.

faulty segment are kept open. After that, the converters can re-energize the DC bus and restore operation autonomously. The whole process is illustrated in Fig. 4.

IV. Simulation Results

The algorithm is tested in the DC system illustrated in Figure 1. The rated operating voltage of the DC grid is 200 V. Each converter is designed with a rating of 1 kW and a nominal operating current of 5 A. The output capacitor of the DABs is 1 μF. The switching frequency (f_{sw}) of DAB is 100 kHZ (ie. note that this is the sampling frequency for the over-current detection strategy). The length of lines L1, L2, and L3 are 520 m, 280 m, and 400 m respectively [19]. Based on the system ratings, a 10 mm^2 connection cable is considered, which has an equivalent impedance of 1.95 Ω/km and 1 mH/km [20]. Therefore, the resistance for L1 is 1.014 Ω, for L2 is 0.55 Ω and for L3 is 0.78 Ω. The inductance of L1, L2, and L3 are 0.52 mH, 0.28 mH, and 0.4 mH respectively. Converter 1 is set as a master controller and runs the algorithm. Based on the system parameters, the following thresholds are considered: I_{th} = 6 A (ie. 1.2 pu) and P_{th} = 9 W. The power threshold is obtained considering an integration time of 0.3 s. and nominal system losses of 6.8 W (note that converter losses have been neglected). Besides, based on the energy of the DAB's output capacitor, the current pulses of the converters during the diagnosis operation have been set with an amplitude of 0.5 A, a period of 1 ms, and a pulse width of 10%. Since low-bandwidth communications are considered, the different converters can exchange messages (eg. send system measurements) every 50 ms [21]. Besides, a communication delay of 0.02 s. from the master converter to the relays is considered. Note that the proposed algorithm could operate considering lower communications bandwidth and larger delays. However, the values above have been chosen to illustrate the algorithm performance with an acceptable time-scale on the simulation plots. To verify the effectiveness of the proposed algorithm, low- and high-impedance faults are simulated. Both simulations start from steady-state conditions, where microgrid 3 is absorbing 1 kW and microgrid 1 and microgrid 2 provide 400 W and 600 W respectively. These operating setpoints remain the same after the fault.

A. Low impedance fault on line

A low impedance SC fault (0.1 Ω) occurs on L3 at time 0.1 s, as shown as Fig. IV. It can be seen that the grid current i_g undergoes a current spike as a consequence of the low-impedance fault. Since it overpasses the threshold I_{th} (6.5 A), the overcurrent alarm trips, and the DAB follows the sequence presented in Section III. Note that this large current spike is not reflected in the current injected by the converters (ie. i_c). Then, the converters stop feeding to the fault, and the energy in the DC network discharges through the fault. All the relays open when the bus voltage collapses to 0. Then, the fault location process described in Section III-B starts. The three system buses are checked at first. Only R1 is closed to check bus 1. Note that there is a small delay from the relay opening to the injection of current from the DAB. It is seen that after the pulse current injection, V_{bus1} reaches the threshold (35 V) which means that this bus is not faulty. The diagnosis process for the other two buses is similar. After, the lines are checked. Relay 12 is closed to check line 1. Since the V_{bus1} does not discharge when connecting R12, it is concluded that L1 is not faulty. The process for checking L2 is similar to L1. When checking L3 (ie. closing R23), the DC-bus capacitor located in bus 2 will discharge through the fault, and the V_{bus2} will return to 0 V. It is seen that V_{bus2} only increases slightly after the injection of the current pulses. After several attempts of injecting current, the V_{bus2} cannot reach the threshold, denoting a fault on L3. Since the algorithm was sweeping the connectivity matrix to determine the openings and closing of relays, the position where the fault was found is recorded, and a '0' state is set for relays 23 and 32. Then, the system relays are reconfigured but keep relays 23 and 32 open. After that, the master converter can re-energize the system autonomously, and the system returns to normal operating as can be seen at time 0.8 s.

B. High impedance fault on bus

The next simulation presents a high-impedance fault (50 Ω) happening on bus 2 at time 0.1 s. (see Fig. IV). It can be seen that i_g does not present a large spike as happened in the short-circuit fault, but the system settles to a new steady-state point without reaching the over-current threshold. Under this scenario, the fault would be absorbing energy continuously, increasing system losses significantly. However, this situation can be taken into account by the integral power strategy described in Section III-A2. Fig. IV-B shows the summation of the net system power over the integration period of 0.3s. Note that the summation is reset after this time to avoid overflow. Besides, despite the faults happening at time 0.1 s, the net power deviation does not exceed the threshold until 0.15s, since system measurements are not transmitted instantaneously but are subject to communication bandwidth and system delays. This delay is labelled as δ in Fig. IV-B. Once the threshold is exceeded, the fault location process starts and follows the normal procedure. Then, when bus 2 is checked, only R2 is closed and the pulse current is injected by converter 2. The bus voltage acquires a value below the threshold and then returns to 0. Since the fault has been identified, the algorithm opens elements corresponding to that row (ie. relays 2, 21, and 23). Next, the system is reconfigured and the DC network can continue with the energy trading. Note that once the fault is cleared, the net power losses do not reach the threshold, as shown in Fig. IV-B.

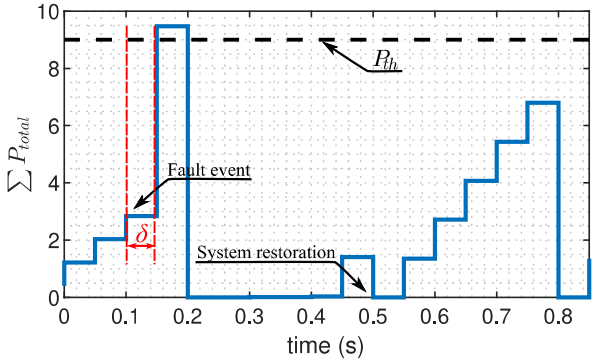

Fig. 7. Illustration of the integral power counter.

V. Conclusions

This paper presented a fault detection and location algorithm that can be used in LVDC systems that interconnect microgrids in rural areas of difficult access to carry out maintenance. The algorithm exploits the strengths of these systems using the converters to selectively inject current to test for the presence of faults in buses or lines individually. The algorithm benefits from the hardware of the interface converters, which is combined with a series of relays to reconfigure the system. This makes the algorithm suitable for meshed topologies while keeping the cost of hardware components low (eg no need for high-bandwidth and extra sensors). In addition, it is effective for both low and high impedance faults. The drawback of this algorithm is that it lacks backup protection if the communication fails. The feasibility of the proposed method is verified by a model in Simulink. It is shown that it can isolate the fault and restore the DC network when high and low impedance faults happen. Future work should demonstrate low-cost hardware suitable to implement the algorithm and discuss the most effective network topologies to enable backup protection and maximise availability.

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