A 0.35µm CMOS UWB-Inspired Bidirectional Communication System-on-Chip for Transcutaneous Optical Biotelemetry Links

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Abstract—In this paper we report on the fabrication, implementation and experimental characterization of an integrated bidirectional communication System-on-Chip (SoC) for transcutaneous bidirectional optical biotelemetry links. The proposed architecture implements a UWB-inspired pulsed coding technique and contains a transmitter and a receiver to achieve a simultaneous bidirectional link. The transmitter generates sub-nanosecond current pulses to directly drive off-chip pulsed vertical cavity semiconductor lasers by means of a digital data coding subsystem and all the needed bias and driving circuits. On the other hand, the receiver manages off-chip fast Si photodiodes and includes signal conditioning, detection and digital data decoding circuits to support high bit rate and energy efficient communication links. The entire solution designed at transistor level has been fabricated in AMS 0.35µm standard CMOS technology into a compact silicon footprint lower than 0.13mm² employing only 113 transistors and 1 resistor. A specific PCB has been developed together with a suitable test bench implemented on Xilinx Virtex-6 XC6V LX240T FPGA board to properly evaluate the performances and the main characteristics of the ASIC. Furthermore, a 6 GHz, 20 GS/s LeCroy WaveMaster 8600A digital oscilloscope has been employed to investigate the system time response. Preliminary experimental results validated the correct functionality of the overall integrated system demonstrating also its capability to operate, also in a bidirectional mode, at bit rates up to 250 Mbps with pulse widths up to 1.2ns and a minimum total power efficiency of about 160 pJ/bit in the conditions for which the transmitter and the receiver work simultaneously on the same chip. These results make the developed solution suitable for high performances bidirectional optical biotelemetry links to be applied, e.g., to implantable neural recording/stimulation transcutaneous platforms that generally require communication channels with high up- e down-link bit rates at extremely low energy levels.

Keywords—Bidirectional Link, System-on-Chip, Optical Wireless Communication, Transcutaneous Biotelemetry.

I. INTRODUCTION

Recent progress in implantable neural microsystems has enabled combining high density cortical recording, signal processing, decoding and communication for a variety of scientific and medical applications. Brain Machine Interfaces (BMIs) in the future will utilise this functionality for actuation and communication in individuals with neurological disease and injury. A key challenge however in implantable device technology for such applications is how to achieve a high bandwidth biotelemetry in an energy efficient manner at low supply voltage and reduced power consumption with compact size whilst optimising electromagnetic (e.m.) compatibility and signal integrity [1, 2]. There has already been a significant amount of work in implementing techniques mainly based on near and far field wireless data and/or power transfer. This includes carrier based, narrow band and Ultra-WideBand (UWB) radio frequency (RF) links [3]. These have predominantly been applied to neuromodulation devices that require the downlink to have a higher bandwidth than the uplink. Downlink data has included control commands and sensory data (into the patient body), whereas uplink data (out of the patient body) has been mainly designed for diagnostic purposes. However, for applications requiring high uplink bandwidths (e.g., required for BMIs) these methods face some fundamental limitations due to their relatively high-power consumption and low e.m. compatibility [4–6]. The recently proposed optical wireless biotelemetry links employ modulated or pulsed semiconductor lasers as data transmitters and photodiodes as data receivers. This kind of solution provides several desirable features such as an improved performance particularly in terms of device size, bit rate, power consumption and e.m. compatibility [2,7,8]. Some improvements have been achieved by increasing the laser power, employing photodiodes with larger sensitive area and/or using modified On-Off Keying (OOK) based modulations. Drawbacks of these approaches are the increase of the laser/emitter response time and of the signal-to-noise ratio that limit the effective system bandwidth and the maximum achievable data rate up to 100 Mbps with a power efficiency of 21 pJ/bit [2,8,9].

Recently, we have demonstrated an UWB-inspired optical wireless biotelemetry system implemented using commercial off-the-shelf components capable to overcome these limitations reaching data rate up to 250 Mbps and 24 pJ/bit power efficiency [10]. This solution has been further developed in [11] by proposing the design at transistor level of a full-custom ASIC implementation of a complete
bidirectional biotelemetry link reporting the post-layout simulations on the system functionality.

In this work, we report on the fabrication, implementation and experimental characterization of the integrated UWB-inspired bidirectional communication System-on-Chip (SoC) for transcutaneous optical biotelemetry links whose overall design is reported in [11]. The employed integrated technology is the commercial AMS 0.35μm standard CMOS. A suitably test bench has been developed to properly evaluate the main performances and characteristics of the fabricated ASIC. The reported preliminary experimental results validate the correct functionality of the overall integrated system demonstrating its capability to operate also in a bidirectional mode at bit rates up to 250 Mbps with pulse widths up to 1.2ns and a minimum total power efficiency of about 160μJ/bit with the transmitter and receiver simultaneously working onto the same chip.

II. OVERALL SYSTEM OVERVIEW

The block scheme representation of the developed system is illustrated in Fig. 1. The communication architecture implements an UWB-inspired optical pulsed modulation technique allowing for a high bit rate link with low power consumption [7]. The complete system includes a transmitter and a receiver within each of the implanted and external (body worn) modules. The transmitter takes, as input signals, the main clock CLK_IN and the bitstream DATA_IN to be coded/transmitted, whilst the receiver provides the recovered clock signal CLK_OUT and the decoded bitstream DATA_OUT. These two subsystems are completely independent and can work also at different operating frequencies (i.e., at different clock rates).

More in detail, the transmitter includes a ‘digital coding’ block to modulate the voltage pulses and a ‘laser driver’ block for biasing and driving the laser diode by converting voltage pulses into current pulses. On the contrary, the receiver includes a transimpedance amplifier (TIA) that converts current pulses into voltage pulses and a ‘digital decoding’ block that takes the received voltage pulses and performs the clock and data recovery. Moreover, in order to have the capability to manipulate very small amplitude current pulses (i.e., at very low-power operating conditions) an additional external voltage amplifier (AMPLIFIER) has been added (i.e., off-chip) so to properly increase the amplitude of the voltage pulses to be decoded by the ‘digital decoding’ block. Finally, the modulation approach implemented has been tailored for a Vertical Cavity Semiconductor Laser (VCSEL) to generate sub-nanosecond light pulses and a fast Si photodiode (PD) to generate the corresponding photocurrent pulses.

An example of a basic timing diagram is illustrated in Fig. 1. The clock and data signals are combined into a single current pulse based bitstream. A first pulse (i.e., the clock pulse) is always generated at the beginning of each bit period (i.e., in correspondence with the rising edge of the clock signal) independently from the symbol to be transmitted. This allows for the transmission of the clock needed for the transmitter–receiver synchronisation (i.e., the clock recovery). Then, after half a period, in correspondence with the falling edge of the clock signal, if the symbol ‘1’ must be transmitted, a second pulse is generated (i.e., the data pulse), while for the transmission of the symbol ‘0’ a further current pulse is not generated (i.e., the current remains at its minimum value).

Fig. 1. Overall system overview of the UWB-inspired optical communication bidirectional link implementing a pulsed data coding technique with an example of the timing diagram.

III. WORKING PRINCIPLE AND IMPLEMENTATION

A. Transmitter subsystem

The ‘digital coding’ block is based on simple combinational logic that, starting from the input clock signal CLK_IN (delaying its rising edges), generates voltage pulses with a variable width regulated by the control voltage VCBL_1 (for VCBL_1 = 0V, the minimum pulse width is achieved). According to Fig. 1, the provided pulse train incorporates both the CLOCK PULSE and DATA PULSE components. This signal then feeds the laser driver circuit, based on a current mirror stage, converting the VOLTAGE PULSES into CURRENT PULSES to directly drive the VCSEL. This block allows also for the regulation of both the pulse current amplitude and the DC current level through the two control voltages VCBL_AC and VCBL_DC, respectively. The employed VCSEL is a high-speed laser featuring compact size (even smaller than the ASIC), threshold current lower than 1mA, fast response (high bandwidth) to short pulsed current modulations with rise and fall times lower than 100ps. Moreover, VCSEL can be chosen to emit laser pulses at wavelengths λ ranging from 800 to 1000nm to minimise the issues related to the skin/tissue scattering, propagation and attenuation [12].

B. Receiver subsystem

Referring to Fig. 1, within the receiver subsystem, the main block is the PD conditioning circuit that is based on a TIA whose gain can be suitably regulated through an optional external resistor REXT. Moreover, the considered fast Si-based PD is a small sensitive area capable to suitably detect the short VCSEL pulses. The TIA converts CURRENT PULSES received from the PD and generates the VOLTAGE PULSES signal that, in turn, can be further amplified by an external amplifier (AMPLIFIER) block. This gain stage has been designed and simulated in AWR Microwave Office and implemented on a PCB with discrete off-the-shelf components. In particular, it has been developed through a cascade of two ERA-2SM+ InGaP HBT wideband monolithic Darlington pair operating at 3.3V single supply voltage [10]. The pulsed signal VOLTAGE PULSES feeds
the ‘digital decoding’ block that performs the data and clock recovery so providing the CLK_OUT and DATA_OUT outputs. In addition, since there is a fixed phase relationship between the CLOCK_PULSE and the DATA_PULSE signals (i.e., a time delay equal to one half of the clock period), a control voltage $V_{CTRL,n}$ allows to properly regulate their relative phase shift as a function of the working data rates (i.e., the different system operating frequencies). For this reason, this block provides a recovered clock signal with intrinsically a duty cycle higher than 50% (i.e., half a clock period plus an additional time delay). Moreover, two further control voltages, $V_{CTRL,U}$ and $V_{CTRL,D}$, allow for the pulse width extension of the received $VOLTAGE_PULSES$ signal so to properly operate the recovery of the data and clock.

C. Full-custom ASIC development

The overall system has been completely designed in Cadence Design Systems Virtuoso tool suite and fabricated in AMS 0.35µm (C35B4C3 process) standard CMOS technology as a single-chip full-custom ASIC in a very compact silicon footprint including all the components except the VCSEL and PD. In particular, the core of the chip implementing the complete system, occupies approximately 0.13mm² (i.e., the transmitter: 53 transistors and 1 resistor; the receiver: 60 transistors). All the circuits operate with a single 3.3V supply voltage. The design has been particularly optimised for high data throughput, low power consumption and small Si area. Moreover, all the blocks previously described have been designed targeting a full-duplex link for a bidirectional communication with up- and down-link transmissions at bitrates up to 250Mbps for each communication channel. The microphotograph of the fabricated ASIC including all the physical bondpads with the ESD protections, is reported in Fig. 2 (on the left) with the main blocks highlighted by red line boxes. The chip with an overall size of 1.6x2mm² has been encapsulated into a JLCC44 (44 pins) standard package. Fig. 2 (on the right) shows also the photo of the PCB fabricated for the ASIC experimental tests and characterizations and the additional PCB implementing the added external voltage amplifier (AMPLIFIER).

IV. EXPERIMENTAL CHARACTERIZATION OF THE ASIC AND ON-CHIP MEASUREMENT RESULTS

After the chip fabrication, as the first step, all the main blocks composing the system included in a single-chip have been properly tested and characterized through suitable analog/digital laboratory electronic equipment so achieving the preliminary results. The complete system has been characterized evaluating its capabilities to correctly transmit and receive data as well as to operate simultaneously in a bidirectional mode by employing a couple of the ASIC (see Fig. 1). Several measurements have been performed to fully characterise the system at different operating data rates and for different pulse widths so to assess the overall power consumption.

More in detail, an appropriate system characterization has been performed by employing a VCSEL-850 by Thorlabs ($\lambda=850$nm, 2.2mA threshold current) and a FDS-025 PD by Thorlabs (high-speed Si-based PD with 47ps response time and 250µm active area diameter). In addition, a suitable test-bench for the generation of bitstreams, master clocks and pulse trains, has been implemented on a Xilinx VIRTEX-6 XC6VLX240T FPGA board.

A photo of the experimental setup is shown in Fig. 3. In particular, according to the scheme reported in Fig. 1, two PCBs (shown in Fig. 2) have been mounted one facing the other so to implement a simultaneous bidirectional link by using two couples of VCSEL and PD. Two XYZ translation stages allowed for the proper optical alignment of the VCSEL and PD along the X- and Y-directions and for the regulation of their relative distance along the Z-direction.

Moreover, two 1.5mm thick diffusers ED1-C20-MD by Thorlabs have been inserted between the VCSELS and the PDs to emulate skin/tissue effects such as light attenuation, diffusion and scattering. Several measurements have been performed by using a 6GHz, 20GS/s LeCroy WaveMaster 8600A digital oscilloscope so to evaluate the main system parameters, characteristics and time responses under different operating conditions.

Fig.s 4-6 report examples of the experimental timing diagrams with the main system signals demonstrating the system capabilities to operate correctly, also in a bidirectional mode. In all the reported results, the coded pulse width is about 1.2ns with a maximum peak current level driving the VCSEL of approximately 24mA. Moreover, the transmitted bit stream is a repetition of a {0,1} bit sequence to quickly and better evaluate the correctness of the system operation and functionality. In particular, Fig. 4 shows only the uplink channel of the complete system (i.e., a transmitter and a receiver working on two different chips) operating at 250Mpbs bit rate. It is important to observe that the recovered clock signal presents a duty-cycle higher than 50% which, if required, could be simply compensated by a suitable duty-cycle correction circuit [13].
Moreover, concerning the results of Figs. 5 and 6, for both the uplink channel transmission bit rate is 250Mbps while the downlink channel bit rate is equal to 50Mbps and 125Mbps, respectively. Furthermore, referring to the block scheme of Fig. 1 and to the operating condition of the results shown in Fig. 6, the complete system implemented onto the CHIP 1 (i.e., the implantable unit) requires a maximum total power consumption of about 38mW (with both transmitter and receiver active) with a data rate of 250Mbps (uplink channel, transmitter) + 125Mbps (downlink channel, receiver) achieving a total power efficiency of about 214pJ/bit. In conclusion, these preliminary results demonstrate that the transmitted repeated bit sequence \{0,1\} is correctly decoded by the receiver and is properly synchronised with the recovered clock signal.

Table I summarises the power efficiencies of the transmitter and the receiver subsystems working at bit rates equal to 50 Mbps, 125 Mbps and 250 Mbps, a pulse width of 1.2ns and a pulse peak current of 24 mA. These results have been obtained considering the best optical alignment along X- and Y-directions and a maximum distance of 3mm between the VCSEL and PD along the Z-direction, including the diffuser that reduces the laser power by a factor 10.

V. CONCLUSION

This work reported on a CMOS integration of a full-duplex communication system, implementing an UWB-inspired pulse coding technique for an optical transcutaneous biotelemetry. Preliminary experimental results have validated and demonstrated the main functionality of the system-on-chip capable to operate, also in bidirectional mode, at bit rates up to 250Mbps with a minimum power efficiency of about 160pJ/bit. Its main performances would allow for integration with implantable intracortical recording systems [14,15] allowing for transmission of over 2,000 channels of raw data.

![Fig. 4. Experimental measurement: main signals related to an uplink communication channel operating at 250 Mbps and transmitting a repeated \{0,1\} bitstream.](image)

![Fig. 5. Experimental measurement: main signals related to a bidirectional communication link operating at 250 Mbps (uplink channel) and 50 Mbps (downlink channel) transmitting a repeated \{0,1\} bitstream.](image)

![Fig. 6. Experimental measurement: main signals related to a bidirectional communication link operating at 250 Mbps (uplink channel) and 125 Mbps (downlink channel) transmitting a repeated \{0,1\} bitstream.](image)

### TABLE I. POWER EFFICIENCY OF THE TRANSMITTER (TX) AND RECEIVER (RX) SUBSYSTEMS UNDER DIFFERENT OPERATING CONDITIONS.

<table>
<thead>
<tr>
<th>Data rate (Mbps)</th>
<th>Power efficiency (pJ/bit)</th>
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<tbody>
<tr>
<td>50</td>
<td>174</td>
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<tr>
<td>125</td>
<td>125</td>
</tr>
<tr>
<td>250</td>
<td>93</td>
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