SINGLE-SUPPLY PRE-BIASING CIRCUIT FOR LOW-AMPLITUDE ENERGY HARVESTING APPLICATIONS

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Abstract: Harvesters utilizing piezoelectricity as the transduction method have advantages over other designs in that the transducer output voltage and current tend to be in a more favourable range for input to a power electronic interface. However, typical devices often operate significantly below their fundamental maximum power because the transducer is unable to provide enough electrical damping. Consequently, circuits have been developed that allow increased damping, such as the SSHI techniques proposed by Guyomar et al., and the pre-biasing technique proposed by us. However, the performance of these circuits suffers significantly at low input voltages, which may occur at low harvester input excitation amplitudes. We present here a new circuit termed single-supply pre-biasing which is able to increase the power output from a piezoelectric harvester to a greater extent than previously possible at both low and high input voltages.

Keywords: energy harvesting, power extraction circuits, piezoelectric, transducers

INTRODUCTION

Energy harvesters utilizing piezoelectric transduction must extract energy from a current source with an inherent shunt capacitance, as shown in Fig. 1. The magnitude of the current I_o is proportional to the velocity at which the piezoelectric is excited by the external motion.

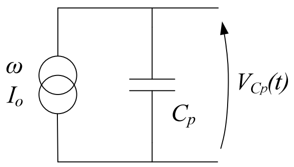

Fig. 1: Electrical model of piezoelectric device. The open-circuit magnitude of $V_{Cp}(t)$ is $V_{po.}$

The simplest load circuit that can extract real power is the resistive load, which can be optimised for the specific capacitance and operating frequency. However, the damping force presented by such a load is low – and well below the theoretical maximum [1]. Additionally, the majority of loads (such as wireless sensors, or further power conversion stages) require a DC voltage source.

The damping referred from the electrical load circuit to the mechanical system can be modified by placing a charge on the piezoelectric capacitance (C_p). When the piezoelectric is moved in one direction, the piezoelectric effect causes a charge on the capacitance. An externally applied charge of the same polarity creates a force that opposes the motion, so that the mechanical system must do more work in order to move the transducer.

Circuits like that of [2] achieve this increased damping effect by resonantly flipping the voltage at the end of each cycle, so that the next cycle starts with a higher bias voltage. However, the existence of diode drops in these circuits causes a reduction in efficiency when the generated voltage on the piezoelectric material is low. The diodes are either for rectification or to provide freewheeling paths. Whilst synchronous rectifiers could replace diodes in all of these circuits, this adds significantly to the complexity of the control system. Where diodes are used for free-wheeling paths this introduces inefficiency since the free-wheeling process is inherently lossy. We propose a circuit here (Fig. 2) based on the pre-biasing circuit introduced by us in [3], which has a single voltage source from which pre-charge is taken and into which generated energy is returned.

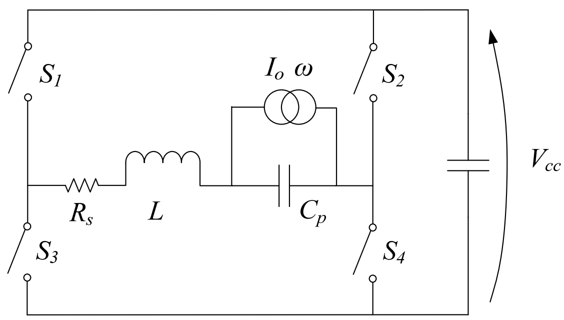

Fig. 2: Single-source pre-biasing circuit diagram

ANALYSIS

The basic principle of operation for a half cycle is that two pairs of switches, able to block and conduct in either direction, are used to pre-charge the piezoelectric capacitance C_p at the start of the mechanical cycle. Then the external motion causes the charge to increase further. Since the change in voltage due to the action of the current source is a constant, and the energy increases with the square of the voltage, a net energy gain is realized when all the energy is extracted at the end of each cycle.

At the end of the physical motion the same pair of switches is closed again to discharge the stored energy on the piezoelectric capacitance into the supply. In the positive cycle S_1 and S_4 are used, and in the negative cycle S_2 and S_3 are used. Fig. 3 shows the operational cycle in terms of the voltage on C_p at each point in the cycle.

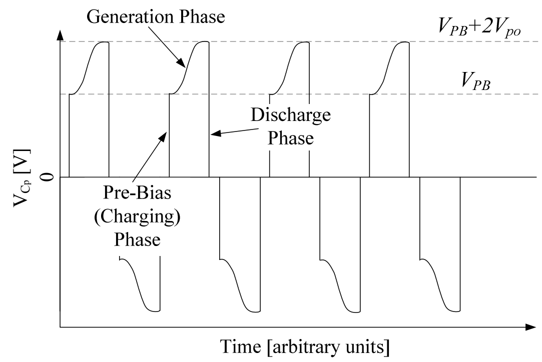

Fig. 3: Operational cycle showing charging and discharging of the piezoelectric capacitance C_p

The voltage on the piezoelectric capacitance C_p at the start of each cycle is 0. When the switches are closed, the circuit will begin to resonate at its damped natural frequency ω_n:

$$\omega_n = \sqrt{\frac{1}{LC_p} - \left(\frac{R_s}{2L}\right)^2} \tag{1}$$

The switch should therefore be closed for a time π/ω_n and then opened, the end of which coincides with a zero crossing of the current in the inductor. After this, neglecting losses, the voltage on C_p will be $-2V_{cc}$. The presence of inductor series resistance R_s means that the Q-factor of the inductive charging path is finite, and given by:

$$Q = \frac{1}{R_s}\sqrt{\frac{L}{C_p}} \tag{2}$$

The proportion of the voltage that is conserved after half of one resonant cycle of an RLC oscillator is:

$$\gamma = e^{\frac{-\pi}{2Q}} \tag{3}$$

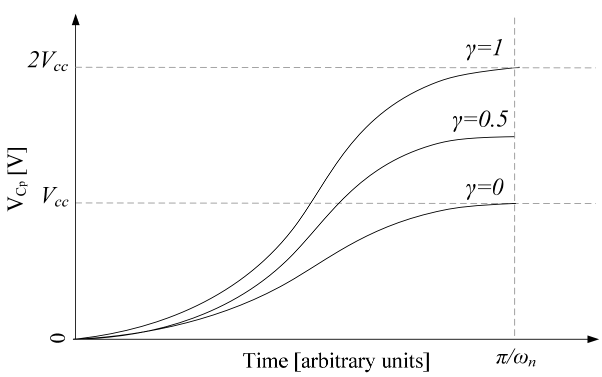

Fig. 4: Relationship between the loss coefficient γ and the final voltage after half a resonant charging cycle

Fig. 4 shows the relationship between the final voltage on C_p and the loss coefficient γ for a capacitor that is resonantly charged from a fixed source voltage V_{cc}. For a lossless device (corresponding to $\gamma=1$) the final voltage on C_p is exactly twice the supply voltage, and in the case where there is high damping (i.e. a high R_s/L ratio, or no inductance at all) the final voltage is $\approx V_{cc}$. The pre-bias voltage on C_p due to a resonant charge cycle from a supply voltage V_{cc} is thus:

$$V_{PB} = V_{cc}(\gamma + 1) \tag{4}$$

In delivering this pre-bias voltage an amount of charge $V_{PB}C_p$ is transferred between the voltage source V_{cc} and C_p, and hence the voltage source expends an amount of energy:

$$E_{ps} = V_{cc}(V_{PB}C_p) = V_{cc}^{\ 2}C_p(\gamma + 1) \tag{5}$$

After the mechanical motion half cycle the voltage on the piezoelectric capacitance is increased by the action of the current source I_o by $2V_{po}$ to $V_{PB}+2V_{po}$. To discharge this energy, the same set of switches is closed and the resonant cycle begins again – but this time the direction of the current is reversed so that C_p discharges into the power supply V_{cc}. The frequency (and hence time period) of the resonant discharge is not affected by the voltages of the voltage source and capacitor, so the final voltage on C_p after discharging for a time π/ω_n is:

$$\begin{aligned} V_{remain} &= V_{cc} - \gamma(V_{PB} + 2V_{po} - V_{cc}) \\ &= V_{cc} - \gamma(V_{cc}\gamma + 2V_{po}) \end{aligned} \tag{6}$$

To extract all the energy on C_p, the voltage V_{remain} must be zero. For this to hold, V_{cc} must take a value:

$$V_{cc} = 2V_{po}\left(\frac{\gamma}{1-\gamma^2}\right) \tag{7}$$

The energy transferred from C_p to the voltage source is the charge transferred, $C_p(V_{PB}+2V_{po})$, times the supply voltage V_{cc}:

$$E_{out} = V_{cc}C_p(V_{PB} + 2V_{po}) \tag{8}$$

The net energy output from the circuit per half cycle is the energy delivered to the supply during discharging minus the energy the supply uses in pre-biasing the piezoelectric capacitance:

$$\begin{aligned} \Delta E &= \left[V_{cc}C_p(V_{cc}(\gamma + 1) + 2V_{po})\right] \\ &\quad - \left[V_{cc}^{\ 2}C_p(\gamma + 1)\right] \\ &= 2V_{po}V_{cc}C_p \end{aligned} \tag{9}$$

Substituting V_{cc} for the value found in (7), and multiplying this expression by $2f_0$ (where f_0 is the mechanical excitation frequency) the power output from this circuit is:

$$P = 8V_{po}{}^2 f_0 C_p \left(\frac{\gamma}{1-\gamma^2} \right) \tag{10}$$

This expression can be approximated using the first-order expansion $\gamma=1-\pi/2Q$ as:

$$P \approx V_{po}{}^2 f_0 C_p \left(\frac{8Q}{\pi} \right) \tag{11}$$

COMPARISONS

The simplest circuit that provides a DC output voltage is the bridge rectifier shown in Fig. 5 [4]. This circuit produces less power than an optimised resistive load because on each cycle the current source must first discharge C_p, and then re-charge it in the opposite direction before the voltage magnitude is high enough to overcome the output voltage and diode drops, and hence deliver current to the output capacitor, which is modelled as a voltage source.

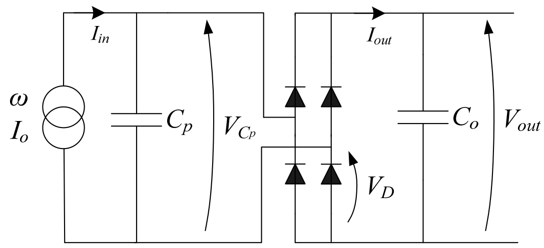

Fig. 5: Piezoelectric source with rectified DC load

The maximum power that can be extracted from this circuit, at the optimal value of V_{out}, can be shown to be:

$$P_{\max} = \frac{f_0 C_p}{\pi} \left(V_{po} - 2V_D \right)^2 \tag{12}$$

Therefore to deliver any power at all the voltage excitation must overcome two diode drops. As will be shown this is a significant limitation, particularly at low input excitations.

We now compare the proposed circuit with the best-performing SSHI circuit, which was identified in [2] as Parallel SSHI DC (Fig. 6).

At the start of each cycle (which corresponds to the zero crossings of the current source), the charge on the piezoelectric capacitance is flipped by the closing of the switch as shown in Fig. 7, so that the voltage on C_p goes from V_2 to V_3. The inefficiency of the charge-flipping path means that $V_3= -\gamma V_2$.

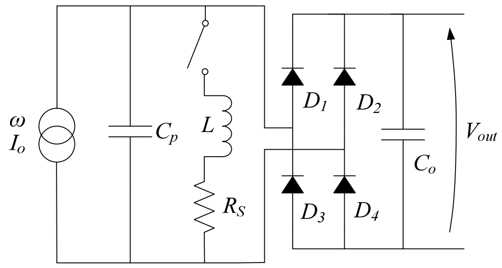

Fig. 6: Parallel SSHI with DC rectified output

During the generation phase the current source increases this voltage until it reaches $V_2=V_{out}+2V_D$, (where it is clamped) and the current source begins to deliver current to the output voltage source at a voltage V_{out}. During steady-state operation $V_3=-V_1$.

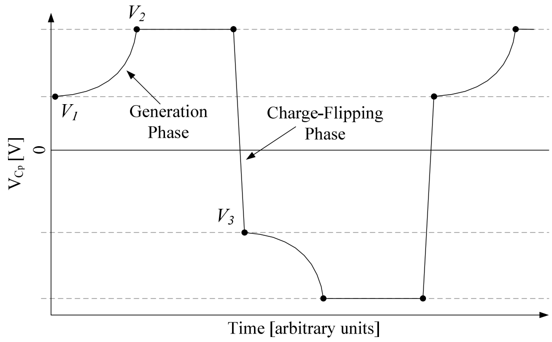

Fig. 7: Voltage waveform on Cp for Parallel SSHI DC

The circuit has a value of V_{out} which maximizes the power output of $V_{po}/(1-\gamma)-V_D$, and therefore the maximum power output can be shown to be:

$$P_{\max} = 2V_{po}{}^2 f_0 C_p \frac{\left(1-(1-\gamma)\frac{V_D}{V_{po}}\right)^2}{1-\gamma} \approx \frac{4Q}{\pi} V_{po}{}^2 f_0 C_p \left(1-\frac{\pi}{2Q}\frac{V_D}{V_{po}}\right)^2 \tag{13}$$

In the limiting case ($Q\rightarrow\infty$) this tends to:

$$P_{\max} \approx V_{po}{}^2 f_0 C_p \left(\frac{4Q}{\pi} \right) \tag{14}$$

This is at best a factor of 2 less than the power output of our circuit in (11). It can also be seen from this expression that to produce any power at all, we require that $V_{po}>\pi V_D/2Q$. Fig. 8 shows a comparison of the theoretical power output against open-circuit voltage V_{po} between the parallel SSHI DC circuit, the simple bridge rectifier and the proposed circuit for a range of high excitation voltages.

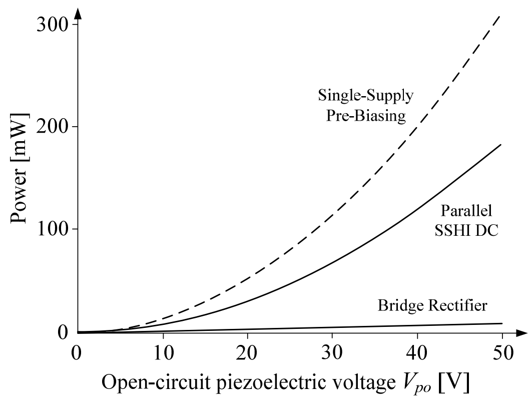

Fig. 8: Power comparison between circuits for: V_D=1 V; C_p=100 nF; f_0=100 Hz; Q=5

In the limiting case where V_{po} is large, and for sufficiently large Q factors ($\gamma \approx 1$) the proposed circuit has a power gain over the Parallel SSHI DC circuit of 2.

Fig. 9 shows a power comparison for low input excitation voltages, and demonstrates that a particular advantage can be had at these levels where the other circuits fail to produce any power, whereas the single-source pre-biasing circuit produces power across the entire range of excitation voltage.

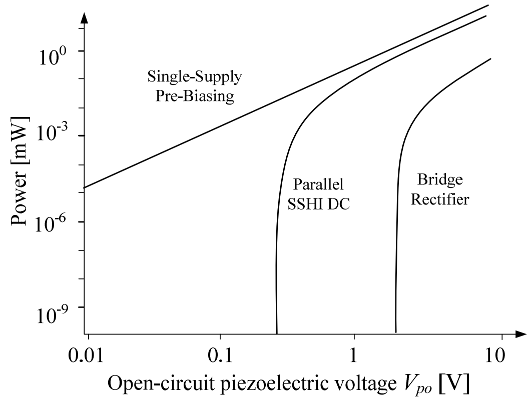

Fig. 9: Power comparison between circuits for low input excitation: V_D=1; C_p=100 nF; f_0=100 H; Q=5

SIMULATION RESULTS

Time-domain simulations were run using *PSpice* (Cadence *ORCAD* v16.3). The switches were modelled as perfect switches with on-state resistance 0.5 Ω as this is approximately the same as the components used, and this was added to the series resistance of the inductor to calculate the overall Q factor of the current path. The results agreed within 1% of the simulated values for a range of input excitation and component values.

EXPERIMENTAL RESULTS

The circuit was constructed on breadboard using production components. The circuit parameters and components used were: a iron core wire-wound inductor of 0.7 mH with series resistance 1.2 Ω and a piezoelectric bimorph with capacitance 0.9 nF. Fig. 10 shows the experimental waveform that was achieved by constructing the circuit from the above components, and using a PIC for the gate pulse timing.

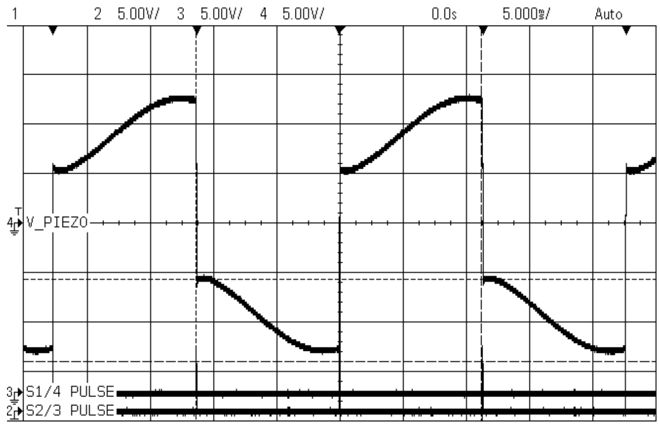

Fig. 10: Experimental waveform showing charging and discharging of piezoelectric capacitance, and gate pulses to achieve this.

As can be seen the voltage waveform on the piezoelectric capacitance agrees with the theoretical prediction.

CONCLUSIONS

A new interface circuit has been presented for piezoelectric energy harvesters operating at low amplitudes. Simulations indicate that the circuit is able to produce more power than previous power extraction circuits in the literature, and operation of the circuit was confirmed by an experimental prototype.

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REFERENCES

[1] P.D. Mitcheson, T.C. Green, E.M. Yeatman, and A.S. Holmes, “Architectures for vibration-driven micropower generators,” *Micro-electro-mechanical Systems, Journal of*, vol. 13, no. 3, pp. 429–440, 2004.

[2] D. Guyomar, A. Badel, E. Lefeuvre and C. Richard. (2005), *IEEE Trans. Ultrasonics, Ferroelectrics and Frequency Control*, Vol. 52, 584-595.

[3] J. Dicken, P.D. Mitcheson, I. Stoianov, and E. M. Yeatman, “Increased power output from piezoelectric energy harvesters by pre-biasing,” *PowerMEMS, Washington DC*, USA, December 1-4, pp. 75–78, 2009.

[4] G. Ottman, H. Hofmann, A. Bhatt, and G. Lesieutre, “Adaptive piezoelectric energy harvesting circuit for wireless remote power supply,” *Power Electronics, IEEE Transactions on,* vol. 17, no. 5, pp. 669 – 676, Sep 2002.