A Multi-MHz Wireless Power Transfer System With Mains Power Factor Correction Circuitry on the Receiver

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***Abstract*—This paper proposes the implementation of a new system topology for multi-MHz inductive power transfer (IPT) systems, which achieves unity power factor when fed from a mains power supply without traditional active circuitry in the front-end as a mains interface. Experiments were performed using an IPT-link which consists of two 20 cm two-turn air-core printed-circuit-board (pcb) coils separated by an air-gap of 13 cm. At the transmit side, a push-pull load-independent Class EF inverter fed from a rectified 60 Hz power supply with no bulk capacitor was designed to drive the transmit coil at 13.56 MHz. This inverter, which has two choke inductors between the voltage source and the two switches, similar to that of an interleaved boost converter, is suitable to be fed directly from a rectified mains source because it tolerates large changes on the input voltage. The IPT rectifier in the experiments was built using a dual current-driven Class D-based topology which allows for higher output voltage when the induced electromotive force (emf) on the receive coil is low. The final power conversion stage on the receive side is a power factor correction (PFC) boost converter that regulates the output voltage and shapes the current waveform at the input of the system. This stage is the only part of the system with closed-loop control. The end-to-end efficiency was measured at 73.3% with 99.2% power factor, when powering a load of 150 W.**

I. Introduction

Performing PFC at the receive side of an IPT system was proposed in [1] for a system operating at $20\,\mathrm{kHz}$, and capable of supplying $1\,\mathrm{kW}$ to the load, with the purpose of eliminating a mains-to-dc power conversion stage with PFC at the transmit side and reducing the size of the input capacitance of the inverter. Therefore, the inverter was required to operate with a fluctuating input voltage, shaped as the absolute value of a single-phase ac-voltage source. Improvements of that type of system can be found in the development of bidirectional wireless power transfer (WPT) systems in [2], [3]. One of the advantages of employing a PFC stage at the receive side, which was well addressed in the mentioned references, is that minimising or indeed eliminating the large capacitance across the dc-link at the transmit side, reduces the size of the circuitry and improves the reliability, as it is well known that large capacitor banks tend to compromise the reliability of the system [1]–[3].

These advantages were also analysed in [4], where a detailed comparison of IPT systems with the PFC stage at the transmit side before the inverter, and alternatively at the receive side after the rectifier, was performed for contactless IPT systems that operate in the kHz range. It was noted that the disadvantage of feeding a high frequency power converter directly from a rectified mains, which is an intrinsic disadvantage of alternating current, is that the peak voltages and currents reached are higher than those required for systems that operate in dc. Therefore, IPT systems with PFC circuitry on the receive side may require higher rated devices for a particular power level.

Most of the points made in the comparison in [4] are also applicable to systems that operate at MHz frequencies. Multi-MHz IPT solutions have been mostly proposed for low power applications where the design relays on an ideal dc-voltage source for power supply. These solutions therefore require a prior PFC stage when powered from the mains. With efficient higher power IPT systems demonstrated at MHz frequencies using wide-bandgap devices [5], [6], solutions integrating the mains-to-dc power conversion stage become more relevant. For example, a $100\,\mathrm{W}$ mains-connected $6.78\,\mathrm{MHz}$ full-bridge inverter combined with a totem-pole rectifier was proposed in [7]. In that work the two power conversion stages are unified, hence reducing the number of components and allowing to drive an IPT transmit coil with the inverter connected directly from the mains.

Unlike in [7] we propose a system that performs PFC at the receive side, which instead of using a full bridge inverter or a Class D, uses a single switch resonant inverter. This group of topologies is known to be simple to construct, efficient, and also suitable to operate with with large variations on the input voltage [8], [9]. This solution is different to those found in literature for lower frequencies because current-driven resonant inverters (i.e. Class E/EF) have a large input inductance as part of the topology, which then also serves as a filter and absorbs the line inductance. This type of inverter require only one low-side switch (or two in push-pull configurations), and are commonly operated in open loop, i.e. at constant frequency and duty cycle, in order to achieve soft switching, and hence optimum performance. Since the system we propose does not require power throughput control at the transmit side, the advantageous properties this type of inverters are fully exploited with the proposed system architecture.

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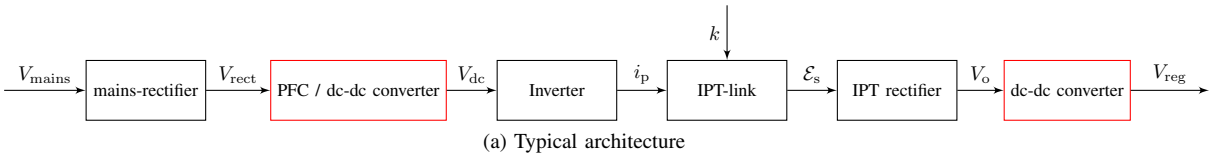
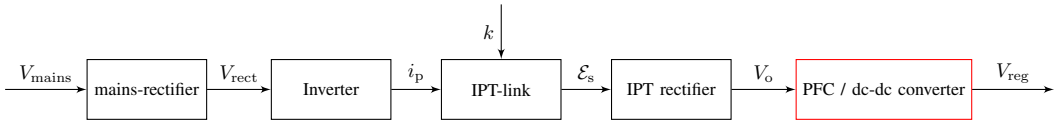


(a) Typical architecture



(b) Proposed architecture

Fig. 1. Multi-MHz IPT system architecture diagrams.

II. Proposed System Architecture

A typical multi-MHz IPT system architecture and the proposed alternative are represented as block diagrams in Fig. 1. The typical architecture includes a PFC stage at the transmit side which is not always accounted for but is conventionally required to produce a dc-voltage supply from the mains. A design example of a multi-MHz IPT system constructed using the typical architecture outlined in Fig. 1a can be found in [10].

The proposed system architecture in Fig. 1b eliminates the PFC stage at the transmit side resulting in a simplification and size reduction of the circuitry, especially considering single-phase PFC stages tend to have large output capacitances to filter out low-frequencies. Also, this allows for the transmit side to operate in open-loop, because the proposed type of inverter does not require changes in duty cycle and switching frequency. Therefore, power throughput control is required to be done exclusively on the receive side, which is a feature that can be beneficial since a communication link between both ends of the WPT system can be avoided.

The proposed system architecture operates as follows: a single-phase mains voltage source (V_{mains}) is rectified (mains-rectifier in Fig. 1b). The output voltage of this stage, V_{rect}, has a waveform that is the absolute value of V_{mains} minus the voltage drop on the diodes. This source is then connected to a Class E or a Class EF inverter. The amplitude of the output current of the inverter depends on V_{rect}; therefore, the transmit coil is driven by a high frequency (the frequency of operation of the inverter) output current (i_{p}), with a modulated amplitude determined by V_{rect}. The switching frequency and duty cycle of the inverter are kept constant. i_{p} produces an induced emf on the receive coil with an amplitude of:

$$\mathcal{E}_{\text{s}} = 2\pi f_{\text{i}_\text{p}} k \sqrt{L_{\text{p}} L_{\text{s}}} i_{\text{p}}, \tag{1}$$

where coupling (k) is:

$$k = \frac{M_{\text{ps}}}{\sqrt{L_{\text{p}} L_{\text{s}}}}, \tag{2}$$

f_{i_p} is the frequency of operation, L_{p} is the transmit coil self-inductance, L_{s} is the receive coil self-inductance, and M_{ps} is the mutual inductance. Detailed formulation relating parameters to optimise the link can be found in [11].

An IPT-rectifier (this block also includes the capacitance typically used to resonate the receive coil) is then integrated to rectify the high frequency emf induced on the receiving coil and filter out the high frequency component, but not the lower (twice the mains) frequency. The voltage waveform of V_{o} is therefore dc with a modulated amplitude determined by V_{rect} and the voltage-gain of the rectifier.

The final power conversion stage is a dc-dc converter, which not only shapes the system's input current to emulate a resistive load, but can also regulate the output voltage (V_{reg}). Thus, a single closed-loop switch-mode power supply at the receive side of the system is utilised to achieve unity power factor and regulate the output voltage of the system.

III. Case Study

An IPT system was developed to showcase an example of a multi-MHz IPT system that uses the proposed system architecture described in Fig. 1b. The IPT system under test operates at a fixed frequency of $13.56\,\text{MHz}$ and was designed to be capable of powering loads of up to $150\,\text{W}$ at couplings lower than $10\,\%$. The inverter is fed from a single phase $100\,\text{V}_{\text{rms}}$, $60\,\text{Hz}$ voltage source, and the receiver gives a regulated output voltage of $400\,\text{V}_{\text{dc}}$ and shapes the input current of the inverter from the receive by emulating a resistive load.

Figs. 2 and 3 show the circuit schematics of the transmit and receive side respectively, which together make up the proposed system architecture. The transmit side consists of a diode bridge mains-rectifier and a push-pull load-independent Class EF inverter. The receive side consists of a dual current-driven Class D rectifier and a boost converter for PFC and output voltage regulation. The values and description of the components chosen for the prototype are listed in Table I.

A. The IPT-link

The two $20\,\text{cm}$ air-core pcb coils (IPT link in Fig.1) used in the case study were characterised in [12] using electromagnetic simulation software and a Keysight E4990A impedance analyser. Coupling was also characterised in relation to distance and misalignment of the coils in [12], which allows calculating the induced emf on the receive coil as a function of i_{p} and

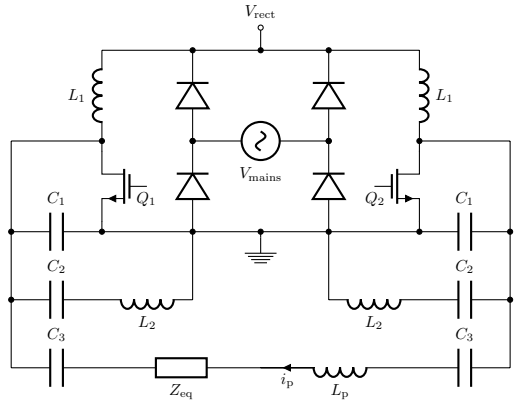


Fig. 2. Schematic of a Push-Pull Class EF inverter driving an IPT coil and a reflected impedance from a mains ac-source.

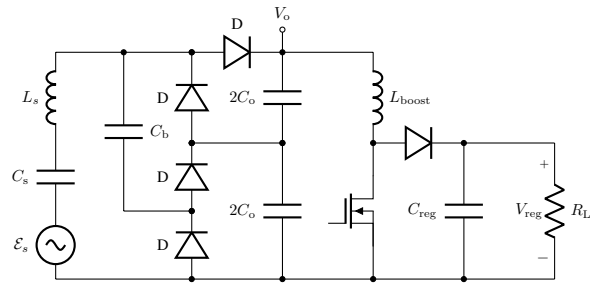


Fig. 3. Receiving end circuit.

TABLE I
COMPONENTS VALUES FOR THE INVERTER DESIGN

Component	Value	Description
C_1 (pF)	270+C_{oss}	Vishay QUAD HIFREQ
C_2 (pF)	470	Vishay QUAD HIFREQ
C_3 (pF)	256	Vishay QUAD HIFREQ
L_1 (μH)	88	Wurth Elektronik WE-PD
L_2 (nH)	66	Coilcraft 2014VS
L_{p} & L_{s} (nH)	1181	PCB coil
Q_1 & Q_2	GS66508B (650 V, 30 A) GaN FET	
C_s (pF)	117	Vishay QUAD HIFREQ
C_b (nF)	100	Vishay QUAD HIFREQ
C_o (nF)	500	Vishay QUAD HIFREQ
D_1 - D_4	C3D02060E-TR (600 V, 2 A) SiC diode	
PFC stage	LT8312EMS Demo Board	

k, (1), as also the reflected impedance on the transmit coil as $Z_{\text{eq}} = R_{\text{eq}} + jX_{\text{eq}}$, where:

$$R_{\text{eq}} = \frac{4\pi^2 f_{\text{i}_\text{p}}^2 k^2 L_{\text{p}} L_{\text{s}} \left(R_{\text{s}} + R_{\text{sec}}\right)}{\left(R_{\text{s}} + R_{\text{sec}}\right)^2 + \left(2\pi f_{\text{i}_\text{p}} L_{\text{s}} + X_{\text{sec}}\right)^2}, \tag{3}$$

$$X_{\text{eq}} = -\frac{4\pi^2 f_{\text{i}_\text{p}}^2 k^2 L_{\text{p}} L_{\text{s}} \left(2\pi f_{\text{i}_\text{p}} L_{\text{s}} + X_{\text{sec}}\right)}{\left(R_{\text{s}} + R_{\text{sec}}\right)^2 + \left(2\pi f_{\text{i}_\text{p}} L_{\text{s}} + X_{\text{sec}}\right)^2}, \tag{4}$$

R_{s} is the receiver-coil's equivalent-series-resistance, R_{sec} the rectifier's input resistance, and X_{eq} the rectifier's input reactance, positive if inductive and negative if capacitive.

B. Design of the Transmit-side Circuit

High-frequency single-switch resonant inverters, namely Class E and Class EF, are effectively current-source driven when the purpose of the input inductance (L_1 in Fig. 2) is not to be part of the resonant circuit (e.g. [13]) but to pass dc and block ac currents, i.e. an infinite choke [8]. A large inductance at the input of a power converter is convenient because it decouples the high frequency currents of the switch from the power source, and also absorbs residual line inductances. This feature of inherently continuous input current, is why boost converters, which have this same characteristic, are most often preferred for shaping the input current of a system connected to a single phase power supply [14].

The proposed inverter (Fig. 2) is a push-pull variation of the load-independent Class EF introduced in [15], which in this work is fed from a rectified ac-voltage source for the first time. The design was done following the load-independent guidelines in [15] in order to achieve zero-voltage-switching (ZVS) independent of the load resistance. The values and specifications of the components are listed in Table I. A push-pull variation, as opposed to a single-ended one (which could also be utilised in the proposed system architecture), is selected for this design in order to achieve higher currents in the transmit coil, and therefore allow for lower coupling. For the push-pull design, the transistors must be driven with a phase difference of $180°$, and the design of the passive components can be done as in [15], by taking into account that the inductance of the coil (L_{p} in Fig. 2) and the reflected load Z_{eq} are split between the two branches of the inverter.

The inverter operates at a constant frequency of $13.56\,\text{MHz}$ and a fixed duty cycle of $30\,\%$, which is the duty cycle that achieves the highest power output capability of the switching devices for this topology and tuning method [15]. Frequency and duty cycle were not altered throughout the experiments since the proposed system architecture does not require power throughput control on the transmit side.

C. Design of the Receive-side Circuit

Fig. 3 shows the selected IPT rectifier topology followed by a boost converter for PFC and output voltage regulation. C_{s} is the capacitance that resonates the receive coil and C_{b} is a dc-blocking capacitance to allow each current-driven Class D rectifier to operate at different voltage offsets. The output capacitance of the two current-driven Class D rectifiers are connected in series to achieve an open-circuit output voltage of three times $\mathcal{E}_{\text{s}}$, i.e. three times higher than the open-circuit output voltage of a current-driven Class D rectifier. This topology was chosen and designed so that the PFC stage would have a large enough input voltage at low coupling. The selected PFC stage requires a minimum input voltage of $90\,\text{V}_{\text{rms}}$, as do most of the commercially available universal-input PFC solutions.

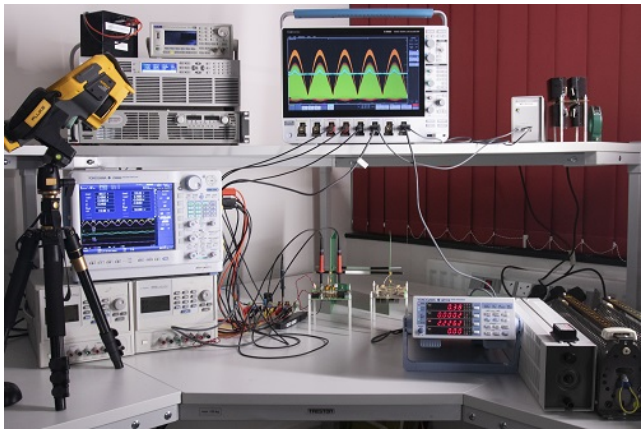


Fig. 4. Photograph of the experimental setup.

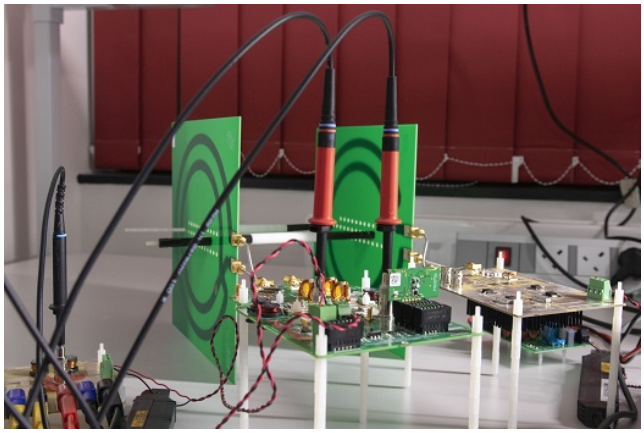


Fig. 5. Photograph of the IPT system under test.

The output capacitance of the IPT rectifier C_{o} was designed to filter out high frequencies ($\geq$13.56 MHz) but not the fundamental frequency of V_{rect}, which is twice the mains frequency, 120 Hz.

IV. Experimental Results

Photographs of the experimental setup and the IPT system are presented in Figs. 4 and 5 respectively. Experiments were performed using the following equipment: a Keysight AC6802A ac-power supply, a PX8000 precision power scope by Yokogawa to measure the input power of the inverter and the power factor at the source, a 5 Series Mixed Signal Oscilloscope by Tektronix to capture the drain voltage waveform of Q_1 and Q_2, and the waveforms of the inverter's input voltage (V_{rect}) and input current (i_{rect}), and a WT310 power meter by Yokogawa to measure the output power.

Three types of experiments were performed. First, the inverter was powered from dc at three different voltages and was loaded gradually at three steps to verify the power capabilities of the inverter. Second, the inverter was powered using a $100\,\mathrm{V_{rms}}$ 60 Hz voltage source, and was loaded as in the first experiment to verify that the proposed inverter can indeed be powered from an ac-source and achieve unity power factor when the inductively coupled load is resistive. Third, the inverter was powered from a $100\,\mathrm{V_{rms}}$ 60 Hz voltage source and was coupled to the designed receive side which can power a dc-load of up to 150 W at 400 V, and perform PFC at the source from the receive side.

The IPT load used in the first two experiments is an RLC circuit developed in [12] which reflects a resistive load on the transmit coil. The reflected load (R_{eq}) was calculated at $1.55\,\Omega$ when the IPT load is positioned at 18 cm from the transmit coil, and at $3.55\,\Omega$ when positioned at 15 cm.

A. First Experiment: Inverter's Performance from a dc-Source

The first experiment consisted of powering the inverter at different input dc-voltages to verify the effects produced by changes in voltage at different load ratings. The experimental waveforms on a time domain of 100 ns are shown in Fig. 6. The transistors' drain voltage waveforms show that as expected, the behaviour of the inverter is load-independent, i.e. the drain voltage converges to zero at turn-on (ZVS) independent of the load. The shape of the waveform is different for different input voltages, due to the voltage-dependent output capacitance of the transistors which affect the effective value of C_1. However, ZVS is achieved in all cases, and this should not therefore significantly affect the performance and efficiency of the inverter.

In these experiments, a maximum input power of 440 W was achieved when the input voltage was set to 120 V and the and the reflected load was calculated at $3.55\,\Omega$.

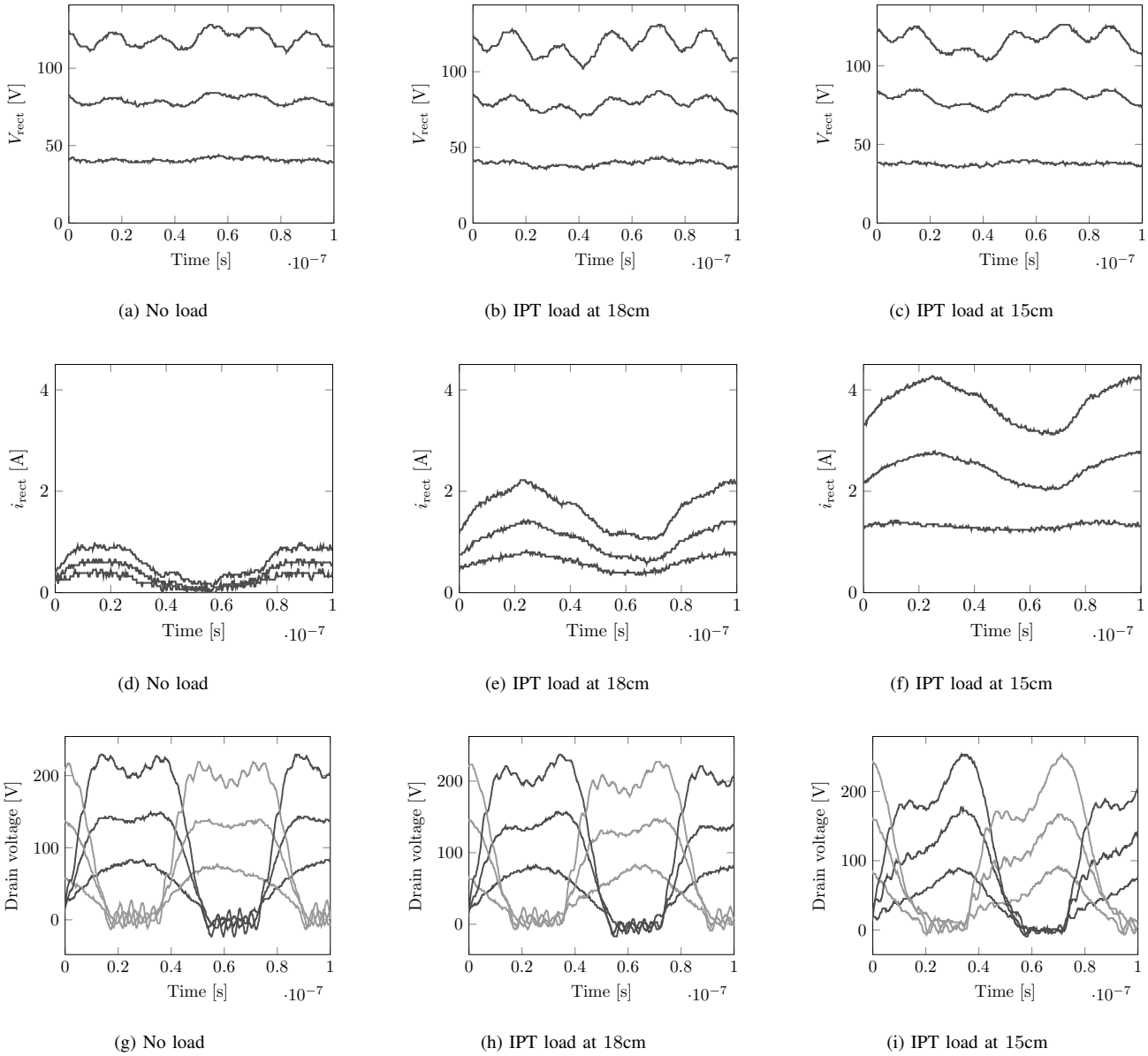
B. Second Experiment: Inverter's Performance from an ac-Source

After verifying that the inverter is capable of operating from 0 to $150\,\mathrm{V_{dc}}$ and that the power transfer capabilities are well over 150 W at $100\,\mathrm{V_{dc}}$, we proceeded to feed the inverter with a $100\,\mathrm{V_{rms}}$ 60 Hz voltage source. Fig. 7 shows the waveforms of V_{rect} and i_{rect} when the transmit side is loaded with the IPT load. In these experiments, a power factor of 99.7 % was measured at maximum load. At this point, the system's input power was measured at 293 W, which is congruent with the input power measured when the system was powered with $100\,\mathrm{V_{dc}}$ and the same load.

C. Third Experiment: System Performance from Mains-ac to Regulated-dc

The designed receive side was powered from the developed inverter in the third experiment. The system was tested at different air-gaps from 15 cm to 12 cm corresponding to a coupling range of 3 to 8 %. At lower coupling (<4 %), the system could only power up loads lower than 100 W, since as the load was increased, the PFC stage stopped regulating the output voltage at 400 V. The minimum coupling at which the system operated for the entire load range was at 5.3 %, when the coil separation was set at 13 cm. Results are shown in Fig. 8.

At full load, the system reached an end-to-end efficiency of 73.3 % and the power factor was measured at 99.3 %

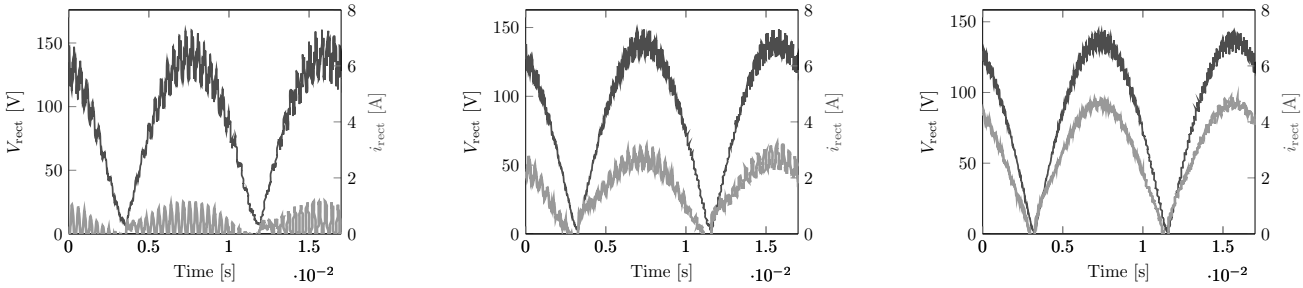


(a) No load (b) IPT load at 18cm (c) IPT load at 15cm

(d) No load (e) IPT load at 18cm (f) IPT load at 15cm

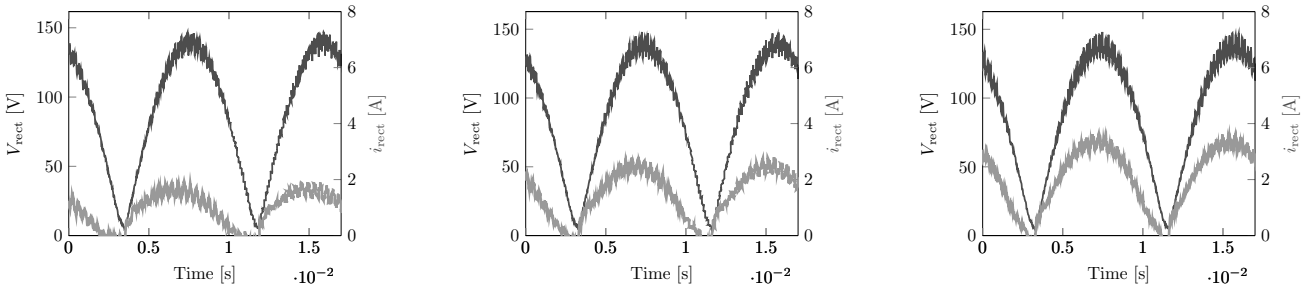
(g) No load (h) IPT load at 18cm (i) IPT load at 15cm

Fig. 6. Experimental waveforms of the inverter when fed from an dc-source, and loaded with an inductively coupled ac-load.



(a) No load, PF = 93.9 % (b) IPT load at 18cm, PF = 99.1 % (c) IPT load at 15cm, PF = 99.7 %

Fig. 7. Experimental waveforms from the input voltage and current of the inverter when fed from an ac-source, and loaded with an inductively coupled ac-load.



(a) P_{reg} = 50W, PF = 95.0 %

(b) P_{reg} = 100W, PF = 98.0 %

(c) P_{reg} = 150W, PF = 99.3 %

Fig. 8. Experimental waveforms from the input voltage and current of the inverter when fed from an ac-source, and loaded with the proposed rectifier followed by a PFC stage at the receiver and a dc-load.

V. Conclusions

A new multi-MHz IPT system architecture which can be fed directly from the mains voltage and achieve unity power factor was proposed and showcased using a push-pull load independent Class EF inverter fed from an ac-source. The proposed system architecture takes advantage of the inherently continuous input current of single switch resonant inverters that help filter out high frequencies at the source. A boost converter at the receive side, after the IPT-rectifier, was used to shape the input current of the multi-MHz IPT system in order to achieve unity power factor.

The operation of a prototype using the proposed system architecture was demonstrated experimentally at 13.56 MHz and 150 W. Results show a an end-to-end efficiency of 73.2 % and a power factor of 99.3 % when powering a 150 W load.

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