A Current Driven Class D Rectifier with a Resistance Compression Network for 6.78MHz IPT Systems

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***Abstract*—In maximal link efficiency IPT design, a fixed AC load value is required. For this reason, matching the value of the input impedance of the rectifier to the optimal AC load is necessary. This paper presents a current driven Class D rectifier with a resistance compression network for 6.78MHz IPT systems, in which the reflected AC load has a minimal variation for a wide range of DC output loads. Experimental results showed a resistance deviation of 31% for an output DC load varying from 10Ω to 80Ω while maintaining high efficiency. Recorded receiving end efficiency range from 96.5% to 88.2%. The achieved compression in resistance deviation could potentially maintain the efficiency of the hosting inductive link above 95%.**

***Index Terms*—Inductive Power Transfer, Class D Rectifier, Resistance Compression Networks.**

I. Introduction

Inductive power transfer (IPT) systems are often designed for maximal link efficiency. In [1], link efficiency is expressed as a function of the unloaded quality factor of both the transmitter and receiver coils Q_{L_S}, the coupling coefficient k, and α which is the ratio of the AC load to the reactance of the capacitor in the secondary resonant tank. The expression for the link efficiency in a series-resonant secondary is:

$$\eta_{\text{link}} = \frac{k^2 Q_{L_{S_1}} \alpha}{\left(\alpha + k^2 Q_{L_{S_1}} + \frac{1}{Q_{L_{S_2}}}\right)\left(\alpha + \frac{1}{Q_{L_{S_2}}}\right)} \tag{1}$$

where,

$$\alpha = \omega_{res} C_{sec} R_{AC}. \tag{2}$$

To achieve maximum link efficiency with given coils, frequency and coupling coefficient, an optimal AC load resistance can be found by equating the derivative of the link efficiency to zero with respect to α.

To achieve optimal load value in practice, it must be considered that to power either a DC or a mains compatible load with an IPT system, a power conversion stage is required. This stage, which is commonly composed by a rectifier and a regulator [1], [2], should reflect a resistive impedance with the optimal value to the IPT system; therefore, the input resistance of the rectifier must match the value of optimal load. To achieve this, current driven Class D and Class E rectifiers have been implemented in IPT systems with series tuned secondary resonant tank [3], [4]. Fig. 1 shows the circuit schematic of a current driven Class D half wave rectifier. This circuit is suitable for IPT, especially in high voltage operation, because

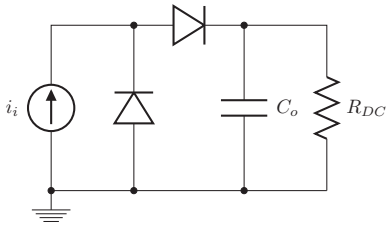

Fig. 1. Current driven Class D half-wave rectifier.

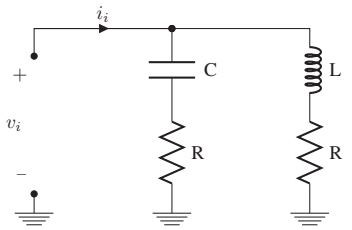

Fig. 2. Resistance compression network.

of its simplicity and low cost [3]. The input impedance of the topology can be modelled as a resistance because the first harmonic of the voltage and the current in the input source are in phase. The input resistance of this circuit is given by [5]:

$$R_{AC} = \frac{2R_{DC}}{\pi^2 \eta_r}. \tag{3}$$

If the rectifier's efficiency η_r is considered constant in (3), the resistance transformation between the DC load and the reflected load to the IPT system is linear. Contrarily, resistance compression networks show that a nonlinear resistance transformation can be achieved with passive components. Fig. 2 shows a circuit that works as a resistance compression network at the frequency where the equivalent impedance of the circuit is real. Equation (4) shows the equivalent impedance in function of the value of the resistor R for the circuit in Fig. 2:

$$\left.\frac{v_i}{i_i}\right|_{\omega=\frac{1}{\sqrt{LC}}} = Z_i\big|_{\omega=\frac{1}{\sqrt{LC}}} = R_i = \frac{L}{2RC}\left[1 + \frac{CR^2}{L}\right]. \tag{4}$$

The nonlinear transformation in (4), if designed properly, can minimize the variations of the input impedance of a circuit

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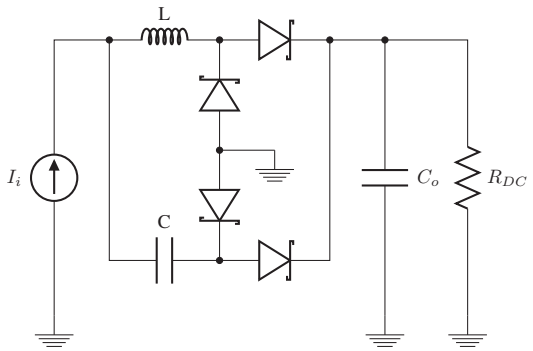

Fig. 3. Class D rectifier with a load compression network.

due to a change in the DC load. This feature is convenient for IPT systems, where a fixed AC load value is essential to achieve maximal link efficiency.

Resistance compression networks were introduced by [6] with a VHF (30-300MHz) resonant DC-DC converter using two Class E rectifiers with a load compression network. A similar approach was proposed in [7] with a 500kHz DC-DC converter with galvanic isolation making use of a resistance compression network in two separate Class D rectifiers.

II. Class D current driven rectifier with a load compression network

The proposed Class D rectifier with a load compression network, shown in Fig. 3, uses a current source in the input because in series-resonant secondary IPT systems, the source is modelled as a sinusoidal current at the resonant frequency of the secondary tank. This topology, with a novel approach for IPT rectifiers, uses the principle of resistance compression networks to achieve maximal link efficiency. Moreover, the objective of the topology is having a more steady value of reflected AC resistance; consequently, a consistent maximal efficiency in the IPT link can be achieved.

The proposed circuit has similar diode current waveforms as a full wave current driven Class D rectifier because both legs of the rectifier deliver power to the load, therefore the diodes show lower current or voltage stresses. This allows smaller faster silicon Schottky diodes in applications where load power is less than 500W. Unlike in a full bridge Class D rectifier, this configuration has a common ground reference for the load and the source. It can be concluded that the capacitor and inductor shift the phase of the current waveforms in opposite directions which can also help reduce the output ripple.

Load compression in the proposed circuit can be designed by introducing the value of the input resistance of a Class D rectifier (3) into the resistance compression network equivalent resistance (4). The equivalent AC resistance for the proposed class D rectifier is:

$$R_{AC} = \frac{\pi^2 L}{4CR_{DC}}\left[1 + \frac{4CR_{DC}^2}{\pi^4 L}\right]. \tag{5}$$

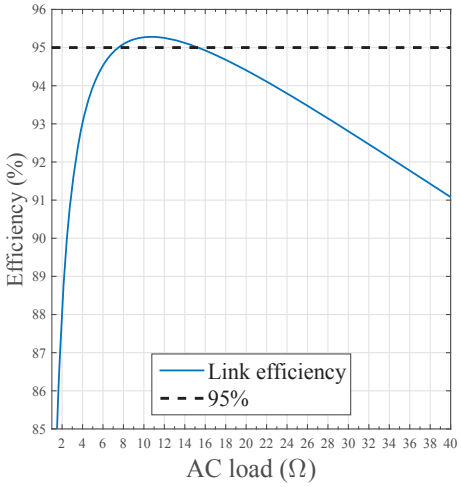

Fig. 4. Simulated link efficiency of an IPT system.

The minimum value of the input resistance of this circuit can be found in (6). This value is equivalent to the inductor's reactance:

$$R_{AC}\Big|_{\frac{\partial R_{AC}}{\partial R_{DC}}=0} = R_{AC\min} = \sqrt{\frac{L}{C}}. \tag{6}$$

Additionally, a resistive equivalent impedance is necessary, therefore the following must be met:

$$LC = \frac{1}{\omega^2}. \tag{7}$$

With these two equations and the required AC resistance, the inductance and the capacitance of the load compression network can be calculated. It can be noted from (7), that the size of the reactive components decrease with frequency ω. This makes this topology more suitable for high frequency applications.

III. Case study

The rectifier shown in Fig. 3 was tested for the IPT link developed in [2]. The receiving end of this IPT system has a series-resonant topology, which allows modelling the power supply as a current source at the frequency of resonance of the receiving end's resonant tank. The design of the resistance compression network is done so that the reflected resistance of the rectifier matches the optimal AC load of this particular IPT link.

The optimal load resistance was found for this configuration considering the following parameters: the inductance of the receiving IPT coil is 5.67μH and the series capacitor of the resonant tank is 81.6pF. These elements were tuned with the rectifier at a resonating frequency of 6.85MHz. The unloaded Q factor of the transmitting and receiving coil are 1270 and 1100 respectively at the given frequency, and a coupling coefficient of 3.5% was considered.

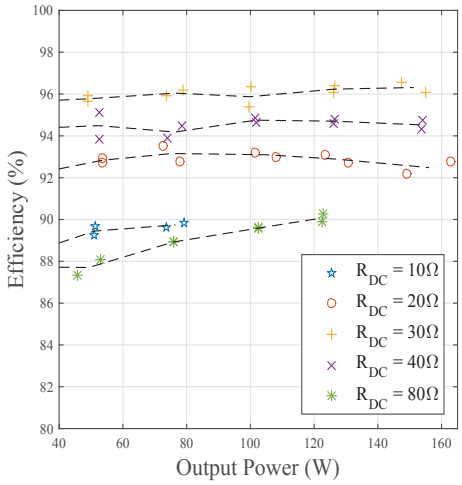

Fig. 5. Efficiency in the receiving end of an IPT system with a current driven Class D rectifier and a load compression network.

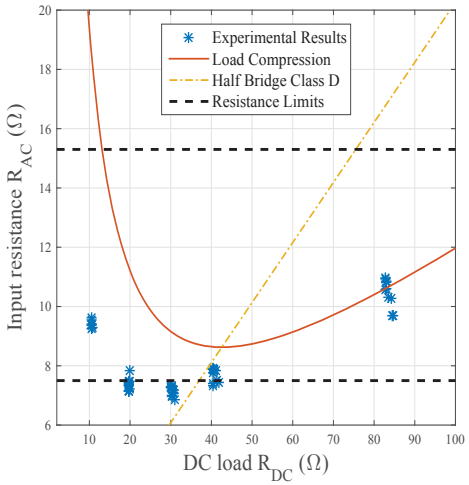

Fig. 6. Input resistance of the load compression current driven Class D rectifier.

For this particular configuration, according to (1), the efficiency of the wireless link depends only on the AC load. Fig. 4 shows how the link efficiency is affected by changes in the AC load, which in our experiment corresponds to the rectifiers input resistance. The maximal link efficiency in this case is achieved when the AC load is 10.71Ω. The rectifier was designed for a range of AC resistance values associated with link efficiencies higher than 95%. To meet this condition, the input AC load should range from 7.5Ω to 15.3Ω, which means that the reflected input resistance of the rectifier has to be in this range to achieve the desired link efficiency of 95% or higher.

The resistance compression network was designed considering equations (6) and (7) and built with a 200nH air-core inductor and a 2.688nF high-Q capacitor configuration. For the rectification stage, silicon Schottky diodes by STMicroelectronics (STPS8H100) were used.

The experiment was conducted with the testing rig presented in [3], [8] working at a frequency of 6.85MHz. The input DC voltage of this Class D inverter was set so that the load would dissipate the required power. Input DC voltages from 35.3V to 93.7V were applied to the Class D inverter throughout the experiment.

The circuit was tested for DC loads of approximately 10Ω, 20Ω, 30Ω, 40Ω and 80Ω with different output voltages so that the experiment would show the resistance transformation and efficiency for different power conditions. The efficiency of the receiving end of the IPT system was measured for all resistance values and different power conditions. The losses that are accounted in the experiment are the ohmic losses in the receiving coil, the series resonant capacitor, the resistance compression network, the rectifier and the output capacitor.

A notably high receiving end efficiency of over 92% was measured when a DC load of 20Ω-40Ω was applied at different output power levels, which suggests that the best receiving end efficiencies are achieved when the reflected AC resistance is closer to its minimal value Z_0. The results show that the IPT receiving end efficiency can reach values of over 96% with a DC load of 30Ω as can be seen in Fig. 5. The efficiency of the 10Ω and 80Ω load resistance, which recorded the lowest efficiencies in the experiment, ranged from 87% to 90%. When the 80Ω load was applied, a 19° phase shift between the voltage and the current of the source was observed, which means that the rectifier has a small reflected reactive component at these high resistance DC load values. This phase shift slightly detuned the series resonant tank, which increased the RMS current of the receiving end coil and therefore affected the efficiency. No reactive behaviour was noted for all other loads.

The proposed load compression rectifier showed consistently good efficiencies for all the DC load resistance values in the experiment which affirms the feasibility of this topology for a wide range of DC loads.

The reflected AC resistance measured in the experiments can be seen in Fig. 6. This figure shows the experimental results, the theoretical linear resistance transformation of a Class D rectifier and the mathematical nonlinear transformation of a load compression network. The experimental results were also compared to circuit simulation as shown in in Fig. 7. Experimental results show a nonlinear resistance transformation as expected from this topology, which proves that the concept of resistance compression applies for the proposed design. The values obtained differ slightly from the mathematical model in that the minimal value of the input resistance is lower than expected. Taking into account that the minimal input resistance of the load compression network is equal to the reactance of the inductor in the load compression circuit, the results suggest that the inductive leg of the rectifier has a lower reactance than calculated due to the parasitic characteristics of the reflected impedance of the current driven

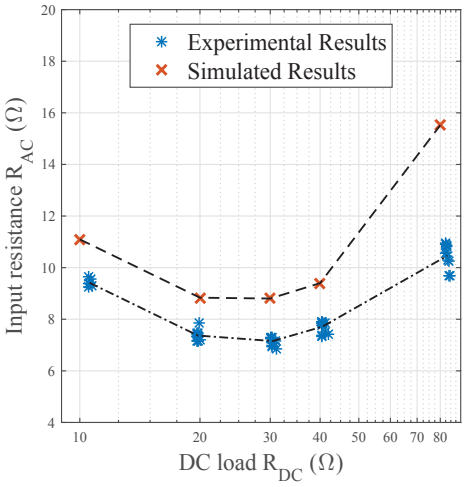

Fig. 7. Experimental and simulated results of input resistance of the load compression current driven Class D rectifier.

class D topology.

A 7.1Ω to 10.5Ω reflected resistance was obtained when changing the DC load from 10Ω to 80Ω, with the lowest reflected resistance encountered when the DC load was fixed at 30Ω. The resistance transformation from DC load to AC reflected resistance in the proposed circuit can be utilized to maintain a fairly constant AC resistance and therefore maintain a high link efficiency in an IPT system.

IV. Conclusion

A topology and design example of a Class D rectifier with a load compression network were presented for high frequency IPT applications. Experimental results show over 87% efficiency in a wide range of DC loads, with a small reactive element in the reflected impedance, only appreciable in the highest resistance value of the experiment. A consistent input resistance, which demonstrates resistance compression, was achieved. This rectification topology for series tuned secondary IPT circuits show promising results for 6.78MHz IPT because a fairly constant AC resistance was achieved in a wide range of DC loads while having an efficiency as high as 96%. The proposed circuit could be applied in higher frequency IPT systems such as 13.56MHz or 27.12MHz where load compression can be achieved with smaller passive components.

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