A Delta-Connected Modular Multilevel STATCOM with Partially-Rated Energy Storage for Provision of Ancillary Services

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***Abstract*—This paper proposes a delta-connected Modular Multilevel STATCOM with partially rated storage (PRS-STATCOM), capable of providing both reactive and active power support. The purpose is to provide short-term energy storage enabled grid support services such as inertial and frequency response, either alongside or temporarily instead of standard STATCOM voltage support. The topology proposed here contains two types of sub-modules (SM) in each phase-leg: standard sub-modules (STD-SMs) and energy storage element sub-modules (ESE-SMs) with a dc-dc interface converter between the SM capacitor and the ESE. A control structure has been developed that allows energy transfer between the SM capacitor and the ESE resulting in active power exchange between the converter and the grid. Injecting 3^{rd} harmonic current into the converter waveforms can be used to increase the amount of power that can be extracted from the ESE-SMs and so reduce the required ESE-SMs fraction in each phase-leg. Simulation results demonstrate that for three selected active power ratings, 1 pu, $\frac{2}{3}$ pu, & $\frac{1}{3}$ pu, the fraction of SMs that need be converted to ESE-SMs are only 69%, 59% & 38%. Thus, the proposed topology is effective in adding real power capability to a STATCOM without a large increase in equipment cost.**

***Index Terms*—Inertia, Energy Storage, Batteries, Supercapacitors, Frequency Response, STATCOM, AC-DC power conversion, DC-DC power conversion.**

I. Introduction

THE increasing penetration of distributed and intermittent renewable energy sources (RES) in the power transmission and distribution network has introduced significant challenges to the system operators in terms of secure and stable operation of the grid. A large proportion of the RES generation is connected to the grid at medium voltage (MV) or low voltage (LV) levels (e.g., photovoltaic, small wind turbines), commonly interfaced to the grid by means of power electronic conversion systems. As a result of increased penetration of such systems there has been a notable decommissioning of the conventional centralised generation that employ synchronous generators (with their governors, short-term over-rating and inherent inertia), potentially leading to a degradation in the overall quality (Voltage & Frequency) and stability of the network [1], [2]. There is an increased need for innovation and diversity of provision of frequency response and reserve services in order to deal with the inherent output uncertainty of RES and the reduced system inertia. Without these services, the power system could experience unacceptable low frequency events or the curtailment of output from wind & solar plants during low demand or high RES output so as to retain the use of synchronous machines for service provision. Such curtailment raises energy costs and leads to inefficient and inflexible power system operation. Energy Storage Systems (ESS), and in particular battery energy storage systems (BESS), are being considered as an alternative source of system services and, therefore, have attracted significant commercial and academic interest recently. ESS can substitute control services for the inflexible renewable generation such as managing peak power flows (deferral of network reinforcements), providing balancing services, arbitrage opportunities in the energy market and reactive power support [3], [4]. Batteries and ultra-capacitors (UC) are able to change their power output in a very short period of time and so are very well suited for services that require a quick response albeit with a relatively low overall energy provision such as inertial response and primary frequency response services [5].

This paper examines the design and operation of a multilevel power converter with partially-rated storage (PRS), designed to store power alongside other functions with only a fraction of the sub-modules (SM) needing to contain a battery or UC. The focus here is a circuit topology suitable for MV connection, allowing direct connection to a distribution network or to transmission network through a substation transformer tertiary winding. The main objective is provision of ancillary services such as primary frequency response alongside voltage support services as normally provided by a STATCOM. The design stage involves ascertaining the amount of energy storage required and the fraction of SM to be converted, in order to provide ancillary services without significantly increasing the footprint of the converter or the power losses during normal operation. The redundancy and reliability available through the modular structure is to be maintained.

II. Converter Topologies

Historically, most BESS have been operated at relatively low DC voltages and mostly used as uninterruptible power supplies (UPS). They have been interfaced to the AC grid through single-stage, 2- or 3-level converters [6]. In this type

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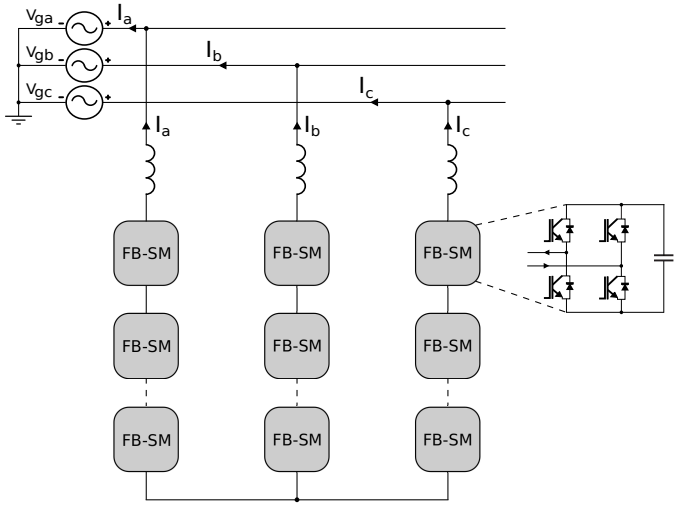
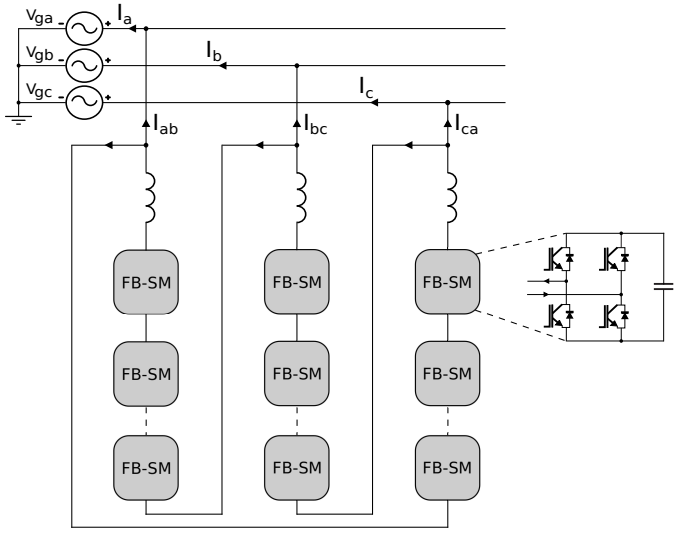
of converters, batteries are usually connected at the dc-link of the converter in the form of series strings. The strings are relatively long in order to obtain the necessary dc voltage and this leads to a substantial risk of the whole string failing through only a single battery cell becoming high impedance because of a failure [7]. Increasing the power rating of such system requires multiple units to be connected in parallel, leading to a increase in complexity. Large filters are also required to ensure that the total harmonic distortion (THD) is maintained in line with grid standards [8]–[10]. For use in MV distribution, a step-up transformer is required. Furthermore, lack of redundancy, design inflexibility and control complexity must also be accounted for when translating from LV to MV converter topologies.

Modular multilevel converters have recently been discussed as an attractive option for ESSs. These converters use multiple voltage levels to produce high quality AC output waveform, thus needing only a small filter or no output filter at all and they can readily attain sufficient voltage magnitude to connect to MV networks without a transformer [11], [12]. In [13], a classification has been presented, based on their circuit configuration. The Double Star Chopper-Cell (DSCC) topology, more commonly known as the Modular Multilevel Converter (MMC) has been extensively researched for applications at high voltage (HV) level, however at MV level this is still a subject of research [14]. In [15]–[17] the MMC was proposed for ESS application because of its advantage of modularity, where energy storage elements (ESEs) can be distributed at the SM level rather than the concentrated in a single group on the dc-link. This arrangement provides decoupling of ESE dc-voltage from the converter dc-link voltage, allowing ESEs to be connected at different voltage levels (depending on application) which in-turn improves reliability. Management of critical parameters such as state of charge (SoC) and state of health (SoH) of each ESE can also be potentially integrated within the converter control [18]. The benefits of modularity have been validated in [19], [20] where batteries were integrated as ESE in the upper arms and UC in the lower arms in the former and uneven distribution of batteries is demonstrated in the later. Analysis carried out by some of the authors of this work in [21], shows that for an MMC at HVDC scale, replacing 4% of the standard Half-Bridge (HB) SMs by Full-Bridge (FB) ESE-SMs, can result in an additional 0.1 pu (10%) power delivery capability, with the drawback that the ESE-SMs require approximately twice the capacitive energy storage of the STD-SM.

For MV level STATCOM solutions, Single Star and Single Delta Bridge Cells (SSBC & SDBC) Fig. 1(a&b) can considered to be more suitable candidates. The absence of a common dc bus means each FB-SM must have a separate or isolated dc source, preventing the use in HVDC. However, this arrangement makes both SSBC & SDBC extremely suitable for utility interface of ESEs i.e. batteries [22]. The SMs in both SSBC and SDBC topologies are of FB type, as both positive and negative voltages are required for the operation of the converter. SSBC has been widely proposed for ESS applications in the past, because of its lower SM count in comparison to SDBC (which has a requirement for blocking



(a) Single Star Bridge Converter



(b) Single Delta Bridge Converter

Fig. 1: SSBC and SDBC based STATCOMs.

the whole line-to-line grid voltage) [10], [23]. The SDBC has an advantage over the SSBC in that the presence of zero-sequence circulating current (I_o) (common current amongst all three phases) creates additional degrees of freedom for balancing SM voltage and managing SoC of the ESEs [18]. The high SM number is also countered by the lower branch currents, resulting in lower SM capacitance and current ripple for a given switching frequency and phase inductance [13], [24]. Furthermore, the SDBC possesses greater capability, compared to SSBC, for handling negative-sequence reactive current for unbalanced load compensation [25].

A. Delta STATCOM Topology

The ESS proposed in this paper is based on the Single Delta Bridge Cells topology. The main use of the SDBC to date has been as a static VAr compensator (STATCOM) for the purpose of regulating voltage and compensating load reactive current [22]. The SDBC has also been used as an energy storage interface [18] and seen commercial use under the name SVC PLUS ES by Siemens [26]. The proposal here is different in that it is designed and operated such that only a portion, not all,

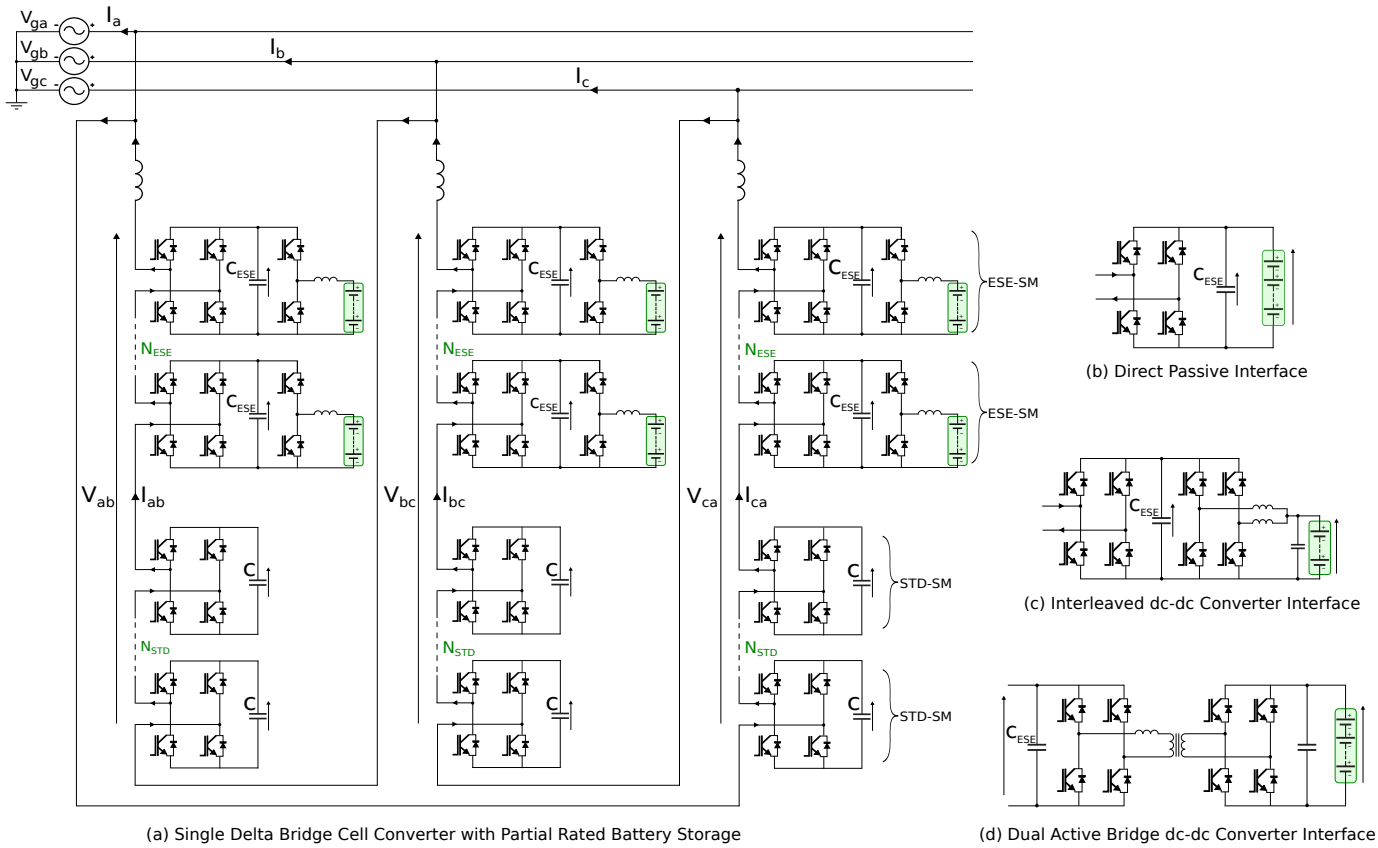


Fig. 2: A Delta-Connected Modular Multilevel STATCOM with Partially-Rated Energy Storage with an active interface in form of buck-boost dc-dc converter between the SM capacitor and the ESE. Other possible interface options presented on the right.

of SMs within each phase-leg need to be provided with energy storage. This we term a partially-rated storage STATCOM (PRS-STATCOM). The proposed topology is illustrated in Fig. 2. Each phase-leg of the converter comprises a series inductor and several cascaded FB-SMs with a mixture of Standard SM (STD-SMs) and SMs with an ESE (batteries or UC) attached (ESE-SMs). The motivation of avoiding having ESE attached to all SM is to avoid large numbers of interface converters. A second benefit is that a small number of connections at the nominal SM voltage gives a better voltage and current combination for interface to storage composed of low voltage cells. The overall PRS structure provides a degree of dual-use of existing converters such as STATCOMS. The battery or UC storage elements can be either directly or indirectly interfaced to the dc-link of a SM as depicted in Fig. 2. Indirect active interface such as buck-boost or interleaved buck-boost dc-dc converter provides decoupling between the SM capacitor and the battery pack, with additional benefit of matching low voltage batteries or batteries with a variety of voltages (e.g. second life batteries). A secondary advantage is a more straightforward implementation of SoC management. The apparent disadvantage is a reduction in round-trip efficiency of the energy storage because of power losses in the additional (dc-dc) conversion stage and need to be accounted for in the sizing and design. Where galvanic isolation is required, such as for electric vehicle (EV) chargers, isolated dc-dc converters such as the Dual Active Bridge (DAB) can be used. Indirect active connection with a non-isolated dc-dc converter is chosen for this study.

During normal STATCOM operation, that is, providing reactive power to regulate AC voltage, no exchange of power takes place between the SM capacitor and the ESE and therefore, both the STD-SMs and ESE-SMs operate in a very similar manner. In this case, there are no power losses arising from operation of dc-dc converters. When active power support is required, energy is transferred between the SM capacitor and the ESE through the dc-dc converters of the ESE-SMs. A key design parameter of this converter is the required number of SMs that need converting to ESE-SMs. It will be shown that this is a function of the maximum real power transfer that is to be added to the existing reactive power capability. This fraction also depends on how the control of the converter is accomplished and devising a control approach that minimises the fraction is beneficial. The analysis presented in next section will address these issues.

III. Analysis of PRS-STATCOM Operation

A simplified representation of a PRS-STATCOM is shown in Fig. 3. Each converter phase-leg comprises a chain of submodules which can generate a voltage (V_{stack}) which is the sum of a voltage generated by the ESE-SMs (V_{ESE}) and the STD-SMs (V_{cap}).

For a given active power rating (P_{rated}), the minimum required number of the ESE-SMs in each phase-leg, is determined by conducting a numerical analysis based on bisection method with the objective of achieving a per cycle net-zero

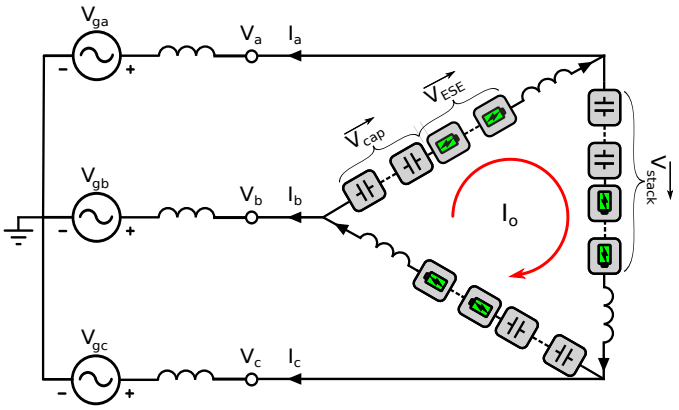


Fig. 3: Electrical model of PRS-STATCOM presenting ESE-SMs and STD-SMs as voltage sources within each phase-leg.

energy deviation in the STD-SMs. The analysis is similar to [21] with the principal difference being that in that study, the converter was an AC/DC MMC with half-bridge standard SMs whereas in the delta STATCOM considered here, the STD-SM are required to produce bi-polar voltages and must be full bridge. The case-study was conducted for a converter rated at 50 MVA in its original STATCOM form and designed for connection at MV level. When determining the ESE-SM fraction, the peak phase-leg current is maintained at the 1 pu value (714.25A) that existed for the STATCOM, similar to the case presented in [26], where active power provision is prioritised over reactive power provision during system frequency disturbances. Converter design cases where the current limit is higher than that required for providing the rated reactive set-point, or where reactive power provision capacity must be retained during active power provision, could also be possible but are not considered in this paper. Analytical waveform results for the considered 50 MVA PRS-STATCOM when its active power rating was set to 1 pu are shown in Fig. 4. In this case the required fraction of ESE-SMs was found using the numerical bisection to be approximately 80%. The bottom graph in Fig. 4 shows that over a complete cycle of operation the STD-SM have a net-zero energy exchange and the ESE-SM have a net energy delivery as expected when discharging the storage element. Note that the net energy exchange of the stack matches that of ESE-SMs (since it is zero for the STD-SM). This shows that there is sufficient amount of ESE-SMs within the converter to enable the specified active power rating.

The exchange of reactive & active power by the PRS-STATCOM must respect the instantaneous voltage restrictions set out in Fig. 4. The figure shows the key voltage and current waveforms of a converter rated at 1 pu active power. The ESE-SMs portion of the stack is set to output its maximum voltage as determined by the sum of SM capacitor voltages within the ESE-SMs ($\sum_{n=1}^{N_{ESE}} V_{c_n}$). The sign of E_{ESE} is chosen in combination with the sign of the phase current to give active power exchange in the desired direction (charge or discharge of the storage). The overall stack voltage, V_{Stack} is set to control the AC and internal circulating currents and the STD-SMs must produce a voltage V_{cap} which when added to V_{ESE} give the correct V_{Stack}. The voltage V_{cap} cannot exceed $\pm\sum_{n=1}^{N_{STD}} V_{c_n}$ so on occasion V_{ESE} has to be restricted so that V_{Stack} can still be met. An example of this restriction is seen

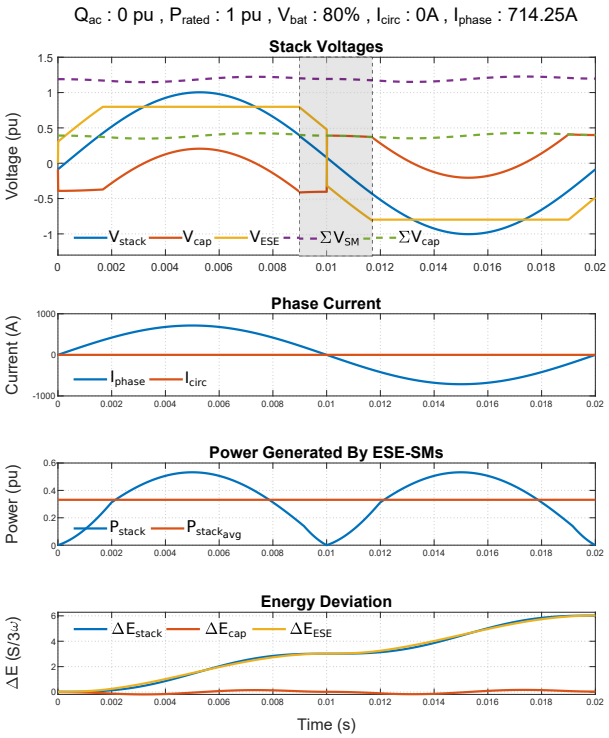


Fig. 4: Voltage, current, power and energy deviation waveforms of PRS-STATCOM delivering 1 pu active power.

between t=0.009s and t=0.01165s (shaded region) in Fig. 4. The maximum and minimum voltages that the ESE-SMs can generate in each phase-leg (ab, bc, ca), V_{ESE}^{max} and V_{ESE}^{min} are set out in (1) and (2). These voltages are dictated by the stack voltage ($V_{stack}(t)$), the available positive and negative voltages of the STD-SMs and sum of ESE-SM capacitor voltages (which are time-varying) $\sum_{n=1}^{N_{ESE}} V_{c_n}(t)$ within each phase-leg. Because the STD-SMs are full bridges, they can produce both positive and negative voltages up to the sum of their capacitor voltages.

$$V_{ESE}^{max}(t) = min\Big(\sum_{n=1}^{N_{ESE}} V_{c_n},\ -\Big(\sum_{n=1}^{N_{STD}} V_{c_n} - V_{stack}(t)\Big)\Big) \quad (1)$$

$$V_{ESE}^{min}(t) = max\Big(-\sum_{n=1}^{N_{ESE}} V_{c_n},\ \Big(\sum_{n=1}^{N_{STD}} V_{c_n} + V_{stack}(t)\Big)\Big) \quad (2)$$

A. Additional Current Injection

The converter waveform results presented in Fig. 4 show that in order to achieve a 1 pu active power rating approximately 80% of SMs within the phase-leg of the converter must be ESE-SMs. In an attempt to reduce the fraction of ESE-SMs required, this paper proposes a technique that involves injecting circulating current (I_{circ}), with the objective of extracting additional energy from the ESE-SMs that are present. This circulating current flows through the SMs but not the external phase connections. Intentionally adding circulating harmonic currents has previously been proposed and used to reduce capacitor voltage ripple in DSCC (2^{nd} order harmonic current injection) [27]. In [21] the authors demonstrated that the required number of ESE-SMs can be significantly reduced

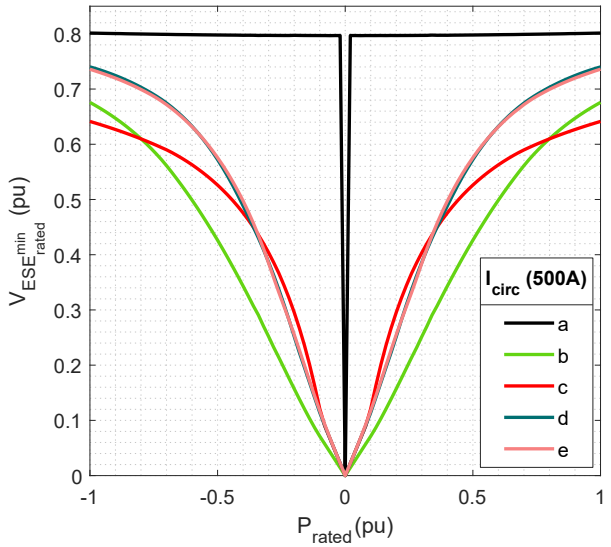


Fig. 5: Comparison of current injections with 500A (0.7 pu) magnitude (a) no circulating current injection. (b) dc current. (c) 3^{rd} harmonic. (d) 6^{th} harmonic. (e) 9^{th} harmonic.

by injecting 2^{nd} order harmonic currents in to the current waveform of the converter. In [28], the authors presented an analysis with a variety of circulating current injections in BESS-SDBC to eliminate battery ripple current and resulting in reduced size of the dc-interface filter.

A selection of current injections of various harmonic orders of current (dc, 3^{rd}, 6^{th} & 9^{th} order) were tested at an amplitude of 500A (0.7 pu) and results are shown in Fig. 5. The injected currents do not contain any fundamental component, only circulate within the phase-legs of the delta and therefore do not alter the positive and negative sequence grid currents or cause any disturbance in the overall energy balancing of the converter. Amongst the four currents tested, dc and 3^{rd} harmonic circulating currents exhibit the best performance in terms of reducing the required number of ESE-SMs. A dc circulating current facilities a lower fraction of ESE-SM than 3^{rd} order harmonic current up to approximately 0.8 pu real power transfer and thereafter 3^{rd} order harmonic is the better choice. Using dc current injection to increase power transfer also causes both the STD-SMs and ESE-SMs experience a significant increase in energy deviation where as injecting 3^{rd} order harmonic current reduces the energy deviation in both STD-SMs and ESE-SMs. This will be further discussed in Section V-A. There is also limited scope for utilising DC circulating currents at higher power set-points without increasing the peak allowable valve current. For the case of the harmonic circulating currents then it is possible to align the phases of both the circulating and the fundamental currents such that it initially reduces the peak valve current (similar to 3^{rd} harmonic voltage injection schemes).

Instead of injecting a constant magnitude 3^{rd} harmonic circulating current regardless of the active power set-point, a process is designed to ensure that the peak phase-leg current limit of the converter is not exceeded and the injected 3^{rd} harmonic circulating current given by (3) is proportional to the phase-leg current at any given power set-point.

$$I_{circ}^{3^{rd}}(\omega t) = \left(K_c \times \hat{I}_{phase}\right) \sin\left(3\omega t - \phi_{circ}\right) \tag{3}$$

where ϕ_{circ} is the phase of the circulating current relative to the fundamental AC component of the phase-leg current, which does not have any significant influence on the required minimum rated voltage of the ESE-SMs ($V_{ESE_{rated}^{min}}$) and K_c is the scaling factor, limiting the peak overall phase-leg current to the limit discussed above (714.25A). Results shown in Fig. 6 are based on the circuit parameters presented in Table. I (Converter 1) and illustrate how $V_{ESE_{rated}^{min}}$ varies with the scaling factor K_c (0 to 3) for various active power ratings.

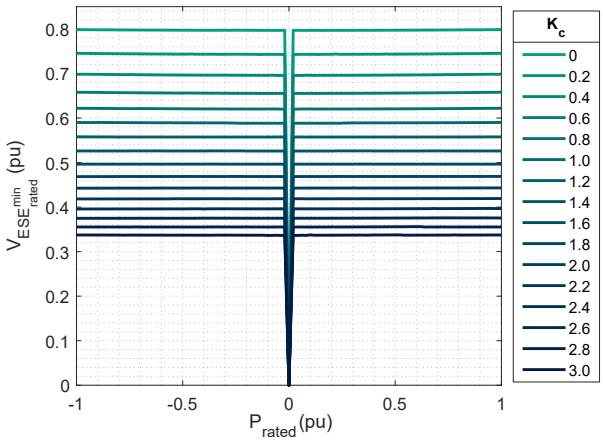


Fig. 6: Required minimum rated voltage of the ESE-SMs with variation in K_c (0 - 3).

This notion is also demonstrated in Fig. 7, where the converter is rated at 1 pu active power and the designed 3^{rd} harmonic circulating current injection is utilised. It is possible to reduce the required number of ESE-SMs from 13 to 11 (12.5%) by injecting 292A ($K_c = 0.41$) 3^{rd} harmonic circulating current without exceeding phase-leg current limit.

IV. Converter Control

The overall converter controller structure is presented in Fig. 8, where the current reference generation for each phase-leg of the converter takes place over three steps, which involves AC current, energy balance current and the additional 3^{rd} harmonic current reference. The AC current reference (I_{ac}) is set by the converter's power rating (S_{rated}) and the voltage of the AC grid (V_{ac}), given by (4).

$$I_{ac} = \frac{2\ S_{rated}}{\sqrt{3}\ V_{ac}} \tag{4}$$

The energy balance controller generates a current to maintain the energy in each phase-leg (close to the design value). This process takes place over two steps, where the first step involves generation of bulk balancing current reference, by balancing the energy of the converter as a whole, using a simple PI controller. Next, energy in the individual branch clusters is balanced, resulting in the reference generation of the zero sequence circulating current (I_o) given by (5), which is inherent to the SDBC topology [29].

$$I_o = \hat{I}_o \angle \left(\theta_{ab} - \phi_o\right) \tag{5}$$

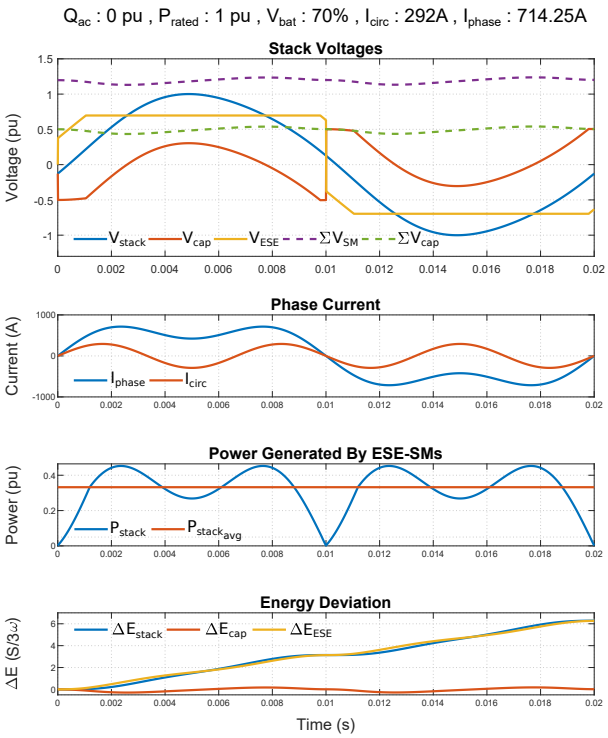


Fig. 7: Voltage, current, power and energy deviation waveforms of PRS-STATCOM with 3^{rd} harmonic current injection.

$$\phi_o = -arccot\left[\frac{2\ P_{ab}/P_{ca}+1}{\sqrt{3}}\right] \tag{6}$$

$$\hat{I}_o = \frac{2\ P_{ab}}{\sqrt{3}\ \hat{V}_{ac}\ cos(\phi_o - \frac{\pi}{6})} \tag{7}$$

where ϕ_o is the angle between the phase voltage (V_{ab}) and the circulating current (I_o), P_{ab} and P_{ca} are the phase-leg powers. The additional 3^{rd} order harmonic circulating current reference $I_{circ}^{3^{rd}}$ is generated based on (3) and the overall phase-leg current (I_{phase}) is given by (8).

$$I_{phase} = I_{ac} + I_o + I_{circ}^{3rd} \tag{8}$$

The current references are then fed in to the current controller based on a common LQR approach as seen in [30], which is a full state-feedback based current control, and is suitable for most modular multilevel converter circuits. No specific adaptions in the current controller were found to be required to make to account for the presence of the ESE-SMs. The current controller then determines the voltages that should be generated to achieve the required currents. The voltage references are then fed into the low-level controller, where the proposed voltage balancing technique is applied and SM gating signals are generated. The main challenge in relation to SM voltage balancing originates from the high ESE-SM ratio in comparison to [21]. A voltage balancing algorithm with the capability of handling both the STD-SMs and ESE-SMs together is developed and presented in Section IV-A.

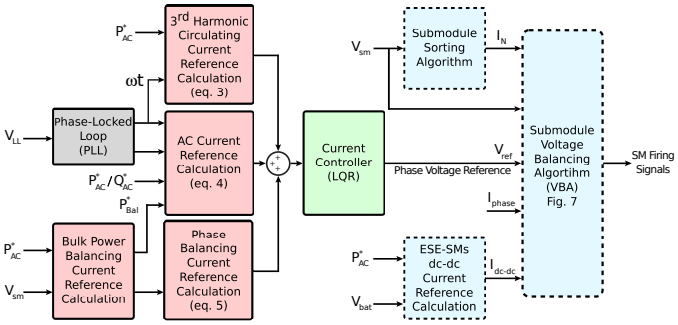


Fig. 8: Converter control scheme with low level control for a single phase-leg (dashed borders).

A. Voltage Balancing Algorithm (VBA)

This section will briefly explain the control method applied for the PRS-STATCOM, focusing on the low level control, where the proposed voltage balancing algorithm (VBA) is applied to translate the voltage references generated by the current controller into the firing signals for each SM. As each phase-leg consists of a mixtures of STD-SMs and ESE-SMs, a significant variation in voltage ripples may exist amongst the SMs, leading to an uneven charging and discharging of the SM capacitors. This unbalance is managed by a rotation algorithm [31], where the SMs are periodically rotated and sorted into a ranked index (I) based on their absolute deviation from the mean instantaneous SM voltage. The approach taken here is similar to the one presented for PRS-MMC in [21], however in comparison the PRS-STATCOM has substantially higher ratio of ESE-SMs to STD-SMs in comparison to the PRS-MMC. The VBA presented in [21], in which the ESE-SMs and STD-SMs are treated as separate groups for voltage balancing purposes, was found to be insufficient. In addition, the PRS-STATCOMs is further complicated by the addition of the negative voltage capability of all SMs. For these reasons a new VBA was developed, which controls the modulation and voltage balancing of all SMs within the converter and is presented by the flowchart in Fig. 9. The initial step involves importing all the required parameters into the voltage balancing controller, employing the algorithm. In order to ensure that the set voltage limits are not violated, the desired stack voltage V_{stack} to be achieved is initially set equal to the reference voltage V_{ref} generated by the current controller, whilst the available voltage V_{avail} in each phase-leg is set equal to the sum of all the SM capacitor voltages for each respective phase-leg. The next step involves calculation of the potential capacitor charging currents based on the three preferential output states (i.e. V_o = V_c , V_o = 0 & V_o = -V_c) and these are then ranked with respect to their individual SM voltage deviation from the mean instantaneous SM voltage. These output states are then tested to investigate for any potential voltage limit violation. The rejected output state is discarded from the sorted list of the preferential output states and consequently the subsequent state in the sort list is tested. Finally the values of V_{remain} and V_{avail} are updated once a preferential charging state is accepted. The process is then repeated until all SM in the sorted list are assigned an output state (i.e. $h == N$).

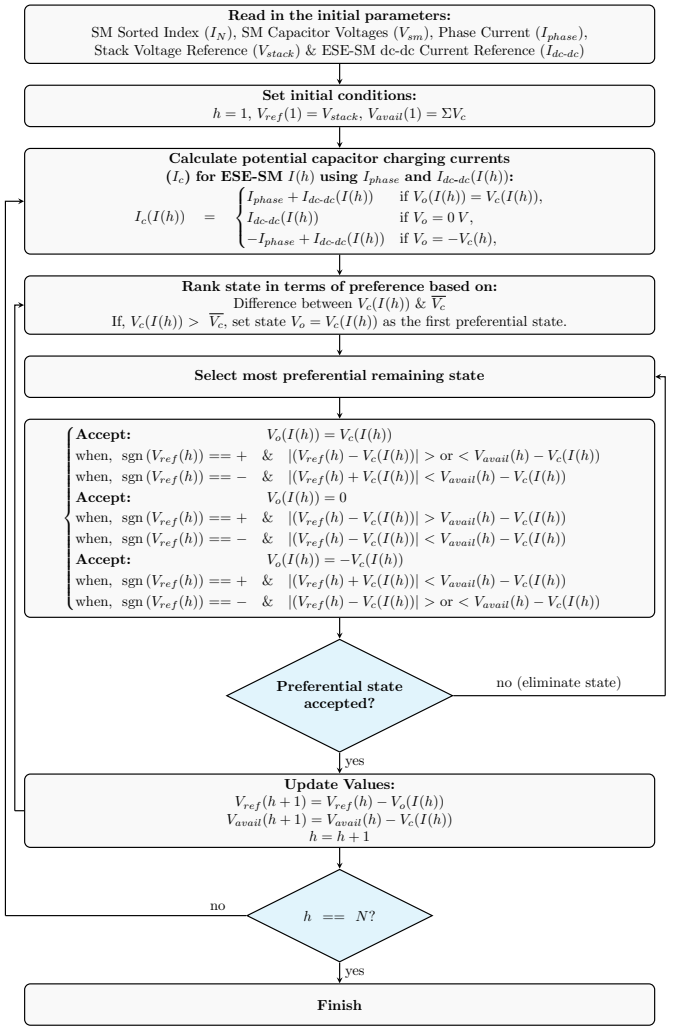


Fig. 9: Flowchart exhibiting the process followed by the voltage balancing algorithm (VBA) in terms of balancing SM voltages & generating firing signals for all SMs within each phase-leg of the PRS-STATCOM.

V. Simulation Results

To verify the design and operating principles of the PRS-STATCOM presented in the preceding sections, a simulation model was realised in Matlab/Simulink and used to assess three configurations of the converter at different active power ratings given in Table I. The fraction of ESE-SM for each of the three converter configurations was determined using the method presented in Section III-A. This resulted in 69% ESE-SMs required for 1 pu rated active power, 59% for $\frac{2}{3}$ pu and 38% for $\frac{1}{3}$ pu. The peak current amplitudes required in each converter for a range of actual active power transfer are presented in Fig. 10. The SM capacitance for both STD-SM and ESE-SM were chosen to suit the rated active power of each configuration and will be discussed further in Section V-A.

Time-domain simulation results are shown in Fig. 11 for the three configurations. For all three P_{rated} configurations, the converters manage satisfactory tracking of current and SM voltages are also well controlled (Fig. 11(c) & Fig. 11(d)). These results confirm that operation is as anticipated during the design optimisation process and that the choice of fraction of ESE-SM has been properly made. The current flowing from the energy storage (red) through dc-dc interface for one of the

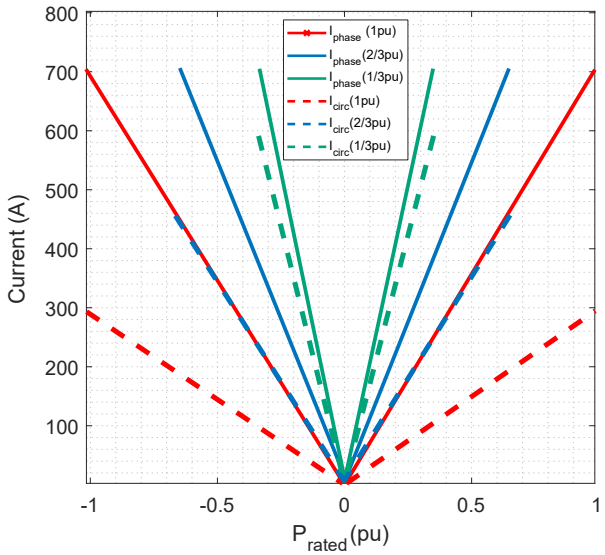


Fig. 10: Peak amplitudes of phase-leg current corresponding 3^{rd} harmonic current injection currents for three converter configuration of different power ratings.

TABLE I: Specification of Simulation Model

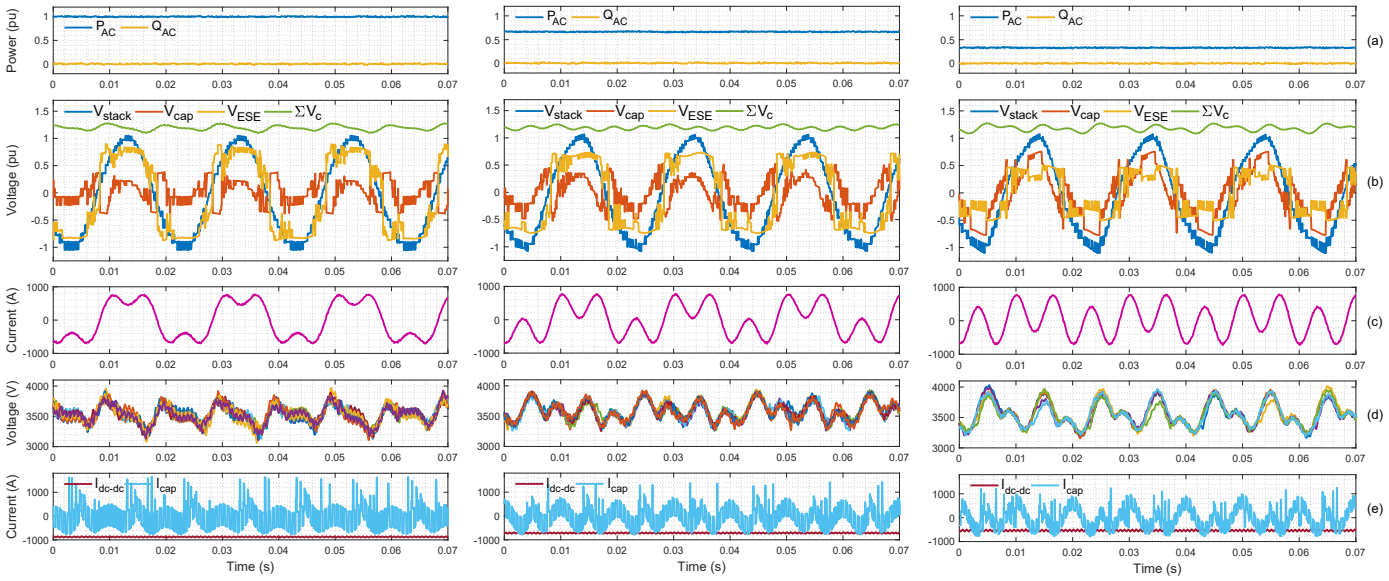
Parameters	Converter 1	Converter 2	Converter 3
Line to Line AC Voltage	33 kV	33 kV	33 kV
Power Rating	50 MVA	50 MVA	50 MVA
Energy Storage Rating	1 pu	$\frac{2}{3}$ pu	$\frac{1}{3}$ pu
Transformer Leakage Reactance	0.14 pu	0.14 pu	0.14 pu
Phase-leg Inductor	0.1 pu	0.1 pu	0.1 pu
Nominal SM Voltage	3467.6 V	3467.6 V	3467.6 V
Total SMs per Phase-leg	16	16	16
Number of STD-SMs	5	7	10
Number of ESE-SMs	11 (∼69%)	9 (∼59%)	6 (∼38%)
STD-SM Capacitor	2.5 mF	1.5 mF*	1.5 mF*
ESE-SM Capacitor	1.5 mF*	1.5 mF*	1.9 mF
Equivalent Stored Energy	10.5 kJ/MVA	8.5 kJ/MVA	9.5 kJ/MVA
Controller Frequency	10 kHz	10 kHz	10 kHz
Simulation Time-Step	1 μs	1 μs	1 μs

* 1.5 mF capacitance required for 1 pu reactive power support.

ESE-SM and the overall current through the SM capacitor (blue) is presented in Fig. 11(e). It can be seen that the amplitude of the low-frequency ripple in the current current is larger in the $\frac{1}{3}$ pu power case than the 1 pu case.

A. ESE-SM & STD-SM Capacitor Sizing

The selection process of SM capacitance is a trade-off between the capacitor size and the desired SM voltage ripple. The required energy storage (capacitor size) in modular converters is typically sized so that the magnitude of the voltage ripple created at the worst-case operating point is within a limit and that limit is often $\pm 10\%$ [32]. The capacitor voltage ripple is linearly dependent on energy deviation. During active power exchange and utilisation of 3^{rd} harmonic current injection, the ESE-SM and STD-SM within each phase-leg of the PRS-STATCOM experience different energy deviation waveforms. In order to evaluate this, the normalized peak-to-peak energy deviation of ESE-SMs (PDEB) and STD-SMs (PDEC), from the same phase-leg were compared with the normalized peak-to-peak energy deviation of SMs during STATCOM operation (1 pu reactive power). This comparison illustrates the required size of the ESE-SMs and STD-SMs capacitance relative to the SM capacitors ($C_{STATCOM}$) during STATCOM operation, for a given rated active power. To gain a better understanding



(a) 1 pu rated energy storage (∼69% ESE-SMs). (b) $\frac{2}{3}$ pu rated energy storage (∼59% ESE-SMs). (c) $\frac{1}{3}$ pu rated energy storage (∼38% ESE-SMs).

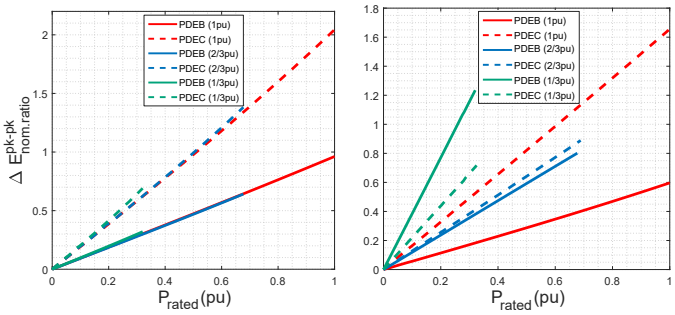
Fig. 11: PRS-STATCOM operating at various active power ratings, utilizing 1 pu 3^{rd} harmonic current injection (maximum 3^{rd} harmonic magnitude, while respecting the peak phase-leg current limit) for all three cases. (a) AC powers. (b) Phase-leg voltages and sum SM capacitor voltage. (c) Phase-leg current. (d) ESE-SM capacitor voltages. (e) Capacitor current (I_c) and dc-dc current (I_{dc-dc}) of an ESE-SM.

on the effects of 3^{rd} harmonic current injection, Fig. 12a illustrates the ratio between the peak-to-peak energy deviation values for the STD-SM and ESE-SM portion of the stack without any additional current and Fig. 12b with 3^{rd} order harmonic current injection. The plot was calculated using the technique described in Section III.

At 1 pu rated P_{ESE}, there is a 40% reduction in the normalized peak-to-peak energy deviation of the STD-SMs due to the injection of 3^{rd} harmonic current (increased STD-SMs percentage). However, the required capacitance (C) is still $\approx 60\%$ higher than ($C_{STATCOM}$). Also, at $\frac{1}{3}$ pu P_{rated}, the required ESE-SM capacitance (C_{ESE}) is $\approx 20\%$ higher than $C_{STATCOM}$. In an ideal scenario the energy deviation for all SMs at any given rated power would either be equal or less than the energy deviation when the converter is delivering reactive power at 1 pu and no alteration in capacitor size is required, as seen in case of $\frac{2}{3}$ pu P_{rated}. In case of 1 pu P_{rated} converter, the capacitance of the five STD-SMs should be increased by a factor of 1.6 to meet the voltage ripple limit. Similarly, for the converter rated at $\frac{1}{3}$ pu, a reduction in the magnitude of 3^{rd} harmonic injection current (Fig. 10) is able to bring the required capacitance in line with $C_{STATCOM}$ (increasing the number of ESE-SMs to 7 instead of 6). Other options involve limiting the maximum rated P_{rated} to 0.8 pu and enhancing the converter control to manage 3^{rd} harmonic injection magnitude with $C_{STATCOM}$ as a limiting factor.

VI. Discussion

This section provides some discussion on the suitability of the PRS-STATCOM for the provision of various ancillary services, as well as presenting a brief comparison between the PRS-STATCOM and a Fully Rated Storage (FRS)-STATCOM. In order to deal with reduced system inertia, a host of response



(a) No Current Injection (b) 3^{rd} Harmonic Current Injection

Fig. 12: Ratio of normalized peak-to-peak energy deviation of an ESE-SM and STD-SM during active power exchange at three different active power ratings to the normalized peak-to-peak energy deviation of SM during STATCOM operation (values above 1 indicate a requirement to increase the SM capacitance for limiting voltage ripple).

services e.g. enhanced frequency response (EFR) have been introduced by the grid operators, which has opened up new opportunities to either modify existing assets or develop new innovative solutions capable of providing active power response. This can be achieved by employing power conversion systems equipped with energy storage technologies. Modular multilevel converters have attracted significant research interest for this application. According to the literature, the common approach is to add ESE in each SM of the converter i.e. Fully Rated Storage (FRS) [4]–[6], [26]. Although the method is effective but not efficient in terms of overall cost and size, some differences are highlighted in Table II. In light of the above opportunities, this paper presents the PRS-STATCOM with the ability to serve on both fronts i.e. active and reactive power response. The topology presents a flexible design solution with a potential of reducing the outset cost and size.

TABLE II: FRS-STATCOM vs. PRS-STATCOM

Power Rating	**1 pu**		**$\frac{2}{3}$ pu**		**$\frac{1}{3}$ pu**	
Converter Type	FRS	PRS	FRS	PRS	FRS	PRS
Total SMs per Phase-leg	16	16	16	16	16	16
Number of STD-SMs	0	5	0	7	0	10
Number of ESE-SMs	16	11	16	9	16	6
STD-SM Capacitor (mF)	-	2.5	-	1.5	-	1.5
ESE-SM Capacitor (mF)	1.7	1.5	1.5	1.5	1.5	1.9
Equivalent Stored Energy (kJ/MVA)	9.5	10.5	8.5	8.5	8.5	9.5
Number of dc-dc Converters	16	11	16	9	16	6
dc-dc Converter Power Rating (MW)	1.04	1.51	0.69	1.23	0.35	0.93
Temperature Control System	16	11	16	9	16	6

* All values are for a single phase-leg of the STATCOM.

Apart from frequency response and voltage regulation, the PRS-STATCOM is also capable in participating in other ancillary services such as inertia emulation, short term operating reserves (STOR), energy arbitrage and power fluctuation cancellation in wind or solar farms. However, it must be highlighted that the topology may not be best solution for all these, in particular cases where the frequency of utilisation of the energy storage function is high, such as in energy arbitrage and power fluctuation cancellation applications. As the round-trip efficiency is expected to be low due to the large circulating current requirement. Taking inertia emulation for illustration purpose and using the swing equation (9) with RoCoF of 1 Hz/s in a 50 Hz system with an emulated inertia H of 7.5 s, gives 0.3 pu active power requirement, which is in line with the reduced rating discussed in Section V. This means that the STATCOM would be equivalent to a synchronous machine devoted to the provision of reactive power only.

$$\Delta P(pu) = \frac{df}{dt}\,\frac{2H}{f_o} \tag{9}$$

As discussed in Section II, one of the biggest design challenges in an MMC is the required capacitive energy storage, 35kJ/MVA – 40kJ/MVA [32] accounting towards approx. 50% of the total size of the SM and is shown to be higher in case of PRS-MMC [21], with a substantial impact on the overall cost. From Table II we can see that both the FRS and PRS-STATCOM require nearly 3.5 times less capacitive energy storage in comparison to an MMC. In PRS-STATCOM both the ESE-SMs and STD-SMs require different capacitance, depending on the rated active power. However, the overall required capacitive energy storage is broadly similar for both the FRS and PRS-STATCOM, as seen in Table II. In case of PRS-STATCOM the number of ESE-SMs is restricted by the peak phase-leg current required for rated reactive power set-point, however, it is possible to design converters where the current limit is higher. This would allow additional circulating currents to be safely injected into the converter, further reducing the required number of ESE-SMs. It should be noted that this would also impact the converter losses and SM capacitor sizing.

Moreover, from Table II it can been seen that apart from a significant reduction in number, the variance in power rating of interface converters from 1 pu to 0.33 pu rated power is considerably smaller compared to FRS-STATCOM. Therefore, from design perspective switching between various power ratings, potentially requires less customisation of any interfacing dc-dc converter in case of the PRS-STATCOM. A reduction in the required number of ESE-SMs may also be particularly attractive in cases where battery technology is used. This is because the degradation of battery energy storage technology is highly dependent on storage and operating temperature (30^oC–40^oC) [9]. A reduction in the number of ESE-SMs therefore would also translate to a reduction in the number of active refrigeration type temperature control systems. With the PRS-STATCOM designed for 0.33 pu, only 6 out of 16 SMs will need to be fitted with such systems, whereas in the case of FRS-STATCOM all 16 SMs will need to have temperature control systems. The PRS-STATCOM concept could also potentially increase the reliability/availability of the ESS by allowing continued operation with a reduced number of working ESE-SMs.

VII. Conclusion

A delta-connected modular multilevel STATCOM with partially-rated storage (PRS-STATCOM) has been proposed so that ancillary services that require real power, such as frequency response, can be added to normal STATCOM functions. This paper has considered the converter design case where active power provision is prioritised over reactive power provision and the converter current limit is based on the rated reactive power capability of the converter. Final practical sizing to account for other cases, such as when reactive power provision must be retained during active power provision or where the converter current limit is greater than that required for achieving rated reactive power, would require exact outer PQ envelope requirements to be specified and individual converter design investigation to be performed. For a given rated active power, only a fraction of the standard SMs in the base STATCOM design need to be equipped with energy storage (to become ESE-SM) which is why it is termed partially-rated storage and why it is considered to have potential to avoid some equipment cost. The active power rating of the converter can be scaled by adjusting the number of ESE-SMs included within each phase-leg. Reducing the fraction of ESE-SMs requires injecting additional current into each phase-leg of the converter. 3^{rd} order harmonic current was found to be the best option for the overall reduction in the number of ESE-SMs and the containment of SM energy deviations. There is, however, a trade off between the reduction of the ESE-SM fraction and the allowable amplitude of 3^{rd} order harmonic current. It was demonstrated that converters rated at 1, $\frac{2}{3}$ and $\frac{1}{3}$ pu require 69%, 59% and 38% of the SMs to be ESE-SMs with the designed K_c values of 0.41 (292A), 0.96 (457A) and 2.5 (591A) respectively. A voltage balancing algorithm was presented which ensures the energy exchange between the ESE and the AC grid is accurate and well controlled. Adding active power provision capability to the converter has an implication on the SM capacitive energy storage i.e. at 1 pu P_{rated} STD-SMs require an additional 65% capacitance while at $\frac{1}{3}$ pu, 25% additional capacitance is required by the ESE-SMs.

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