# A Scalable ISFET Sensing and Memory Array With Sensor Auto-Calibration for On-Chip Real-Time DNA Detection

Nicolas Moser, *Student Member, IEEE*, Jesus Rodriguez-Manzano, Tor Sverre Lande, *Fellow, IEEE*, and Pantelis Georgiou, *Senior Member, IEEE*

***Abstract*—This paper presents a novel CMOS-based system-on-chip with a 78 × 56 ion-sensitive field-effect transistor array using in-pixel quantization and compensation of sensor nonidealities. The pixel integrates sensing circuitry and memory cells to encode the ion concentration in time and store a calibration value per pixel. Temperature sensing pixels spread throughout the array allow temperature monitoring during the reaction. We describe the integration of the array as part of a lab-on-chip cartridge that plugs into a motherboard for power management, biasing, data acquisition, and temperature regulation. This forms a robust ion detection platform, which is demonstrated as a pH sensing system. We show that our calibration is able to perform readout with a linear spread of 0.3% and that the system exhibits a high pH sensitivity of 3.2 $\mu$s/pH. The complete system is shown to perform on-chip real-time DNA amplification and detection of lambda phage DNA by loop-mediated isothermal amplification.**

***Index Terms*—CMOS sensor, DNA detection, in-pixel quantisation, ISFET, memory array, offset cancellation, pH sensor, real-time, sensor array.**

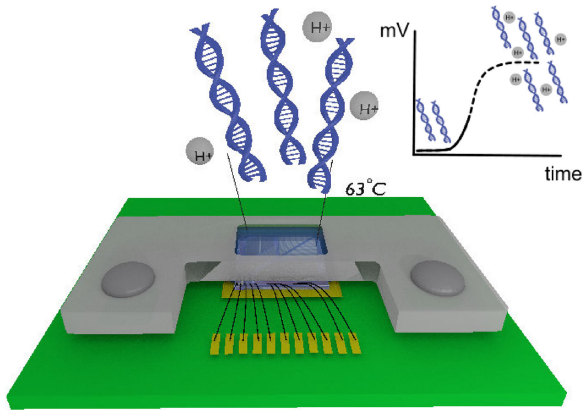


Fig. 1. The CMOS platform is used for on-chip real-time amplification and detection of DNA.

## I. Introduction

THE concept of CMOS-based Lab-on-Chip (LoC) platforms has appeared over a decade ago to designate the upward trend of implementing sensors on silicon. CMOS technology indeed enables the design of large sensor arrays as part of full System-on-Chips with integrated instrumentation for improved SNR, high speed sensing data acquisition with local digitisation and communication using standard readout protocols such as SPI. This technology has attracted attention in the rapidly growing field of Point-of-Care (PoC) diagnostics, particularly rapid tests for SNP identification [1], infectious diseases [2], cancer [3] and blood ion monitoring [4].

We consider the Ion-Sensitive Field-Effect Transistor (ISFET) for its integration on silicon as part of a large array capable of ion imaging. These sensors are placed on the same substrate as the instrumentation, allowing for local sensing and processing of the chemical signal. Since the device was first reported by Bergveld 45 years ago [5], there has been a wide range of proposed architectures for ISFET arrays [6]. We now propose to push sensor integration with instrumentation further as an opportunity to boost the SNR by quantising the signal in close proximity to the sensor i.e. inside the pixel in the case of an array. As a result, each pixel outputs a digital signal which is less affected by parasitics than previously reported arrays based on analogue readout [7]–[9]. This increase in digital instrumentation inside the pixel in turn enables several additional opportunities [10]. (1) The IC is now fully scalable to deeper process nodes, as state-of-the-art technology will decrease pixel size or allow for more in-pixel functionalities. (2) Additional gates increase the sensing area of the pixel which improves coupling to the solution and hence boosts SNR. (3) Digital schemes can be implemented to compensate for sensor non-idealities.

The chip is then embedded as part of a Lab-on-Chip platform for ion sensing. Implementation in standard CMOS technology provides the ISFET with an inherent sensitivity to pH, which has driven the push towards the DNA detection as its most popular application. In particular, it makes the technology a suitable candidate for diagnostic of infectious diseases. Real-time DNA detection involves measuring the amount of DNA copies in solution while running an amplification technique. In this work, we focus on loop mediated isothermal amplification (LAMP)

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The authors are with the Centre for Bio-Inspired Technology, Institute of Biomedical Engineering and the Department of Electrical and Electronic Engineering, Imperial College London, London SW7 2AZ, U.K. (e-mail: n.moser@imperial.ac.uk; j.rodriguez-manzano@imperial.ac.uk; t.lande@imperial.ac.uk; pantelis@imperial.ac.uk).

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for their operation at constant temperature, which relaxes requirements on the technology.

There are several challenges to overcome for the design of our LoC platform, ranging from device adaptation to application-driven requirements. Array challenges are dominated by sensor non-idealities, including mismatch between pixels due to trapped charge and temporal output drift [6]. There are two main types of schemes among previous systems, system compensation and device adaptation, which refer respectively to whether the feedback is applied on the ISFET to set its region of operation or externally on the signal originating from the sensor. We have previously argued the benefit of implementing a part of these schemes inside each pixel [10], and several analogue front-end topologies are compatible with this architecture. These include the PG-ISFET, whereby the floating gate is coupled to a bias voltage through an external capacitor which compensates for trapped charge [11], [12], although this leads to an attenuation of the input signal. An alternative is the reset to the gate approach [13], [14], which involves resetting the ISFET gate using a leaky switch, at the expense of increased electrical drift. However, both these techniques modify to some degree the floating gate voltage, which raises the challenge of finding a calibration scheme which does not degrade SNR. Since we are focusing on the design of a full Lab-on-Chip platforms, there are additional challenges in terms of fast data transmission, but also temperature regulation to guarantee proper DNA amplification.

In this work, following the idea of in-pixel quantisation and device adaptation, we present a novel integrated ISFET analogue sensing and digital memory array designed as a full SoC and embedded in a Lab-on-Chip platform. The in-pixel RAM is used to store a calibrated value to bias each sensor in the proper region of operation. We use temperature sensors spread throughout the array to monitor the temperature and perform regulation with a PID controller and an external heater. We then show an application of the system for the real-time amplification and detection of DNA on-chip, as illustrated in Fig. 1. In Section II, we provide a brief description of the ISFET physics and in Section III, we describe the ISFET pixel topology used for chemical sensing to encode the signal in time. Section IV integrates the array into the full system by providing further details on each component and Section V describes the fabricated system and implemented platform. We then present measured results for electrical and chemical characterisation respectively in Sections VI and VII. Lastly, the platform is demonstrated for on-chip DNA amplification and detection in Section VIII.

## II. The ISFET as Part of an Analogue Front-End

The ISFET is a solid-state sensor with a floating gate covered by an insulating membrane which exposes the device to a solution and an external Ag/AgCl reference electrode for biasing [16]. Implementation of the ISFET in standard CMOS technology is enabled through the extended-gate approach, whereby the polysilicon is connected to a top metal sensing area through stacked vias, as illustrated in the ISFET structure diagram of Fig. 2(a) [15], [17]. As such, the device can be modelled using an equivalent MOSFET and a series of capacitors on the floating gate to reflect surface effects, with the passivation capacitance $\mathrm{C_{pass}}$ originating from the $\mathrm{SiO_2}$ and $\mathrm{Si_3N_4}$ layers due to implementation in standard CMOS technology. The value of $C_{\mathrm{pass}}$

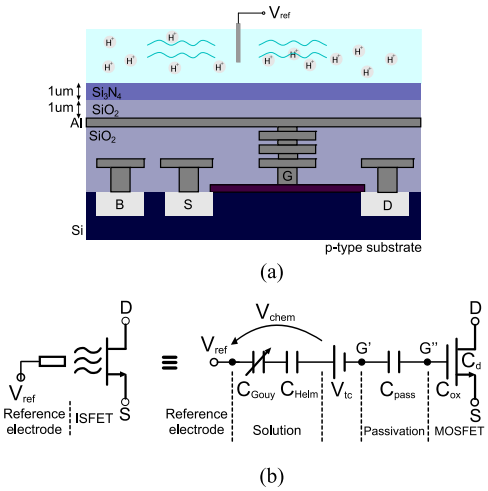



Fig. 2. Diagram of the ISFET fabricated in commercial CMOS technology [15]. (a) Cross-section diagram of the ISFET structure. (b) ISFET macromodel for characterisation as part of an analogue front-end.

essentially quantifies the coupling between the chemical signal at the surface of the chip and the floating gate of the ISFET. Its value can be estimated as a standard capacitance considering the stack of the two passivation layers [15]

$$C_{\mathrm{pass}} = (WL)_{\mathrm{chem}}\varepsilon_0 \frac{\varepsilon_{Si_3N_4}\varepsilon_{\mathrm{SiO_2}}}{\varepsilon_{Si_3N_4}t_{\mathrm{SiO_2}} + \varepsilon_{\mathrm{SiO_2}}t_{Si_3N_4}} \tag{1}$$

where $\varepsilon_0$ is the permittivity of vacuum, $\varepsilon_x$ is the permittivity of layer $x$, $t_x$ is the thickness of layer $x$ and $(WL)_{\mathrm{chem}}$ is the area of the top metal layer connected to the gate of the transistor, designated as the chemical sensing area. In the sensor model, $C_{\mathrm{pass}}$ causes signal attenuation between the floating gate voltage $V_{g''}$ and the surface voltage $V_{g'}$ due to capacitive division with the series capacitances $C_{ox}$ and $C_d$ of the transistor, as highlighted in the macromodel of Fig. 2(b) [15].

$$V_{g''} = \frac{C_{\mathrm{pass}}}{C_{\mathrm{pass}} + (C_{\mathrm{ox}}C_d)/(C_{\mathrm{ox}} + C_d)} \times V_{g'} \tag{2}$$

As such, the signal attenuation depends on the ratio between sensing area and transistor area. Minimising signal attenuation comes down to maximising the sensing area (maximising $C_{\mathrm{pass}}$) and minimising transistor area (minimising transistor capacitances). This justifies the approach taken in this paper to increase pixel area to achieve sufficient SNR and presents an opportunity to embed additional digital circuitry such as memory as shown in this work.

A change in ion concentration has the effect of shifting the floating gate voltage $\mathrm{V_{g's}}$ of the device [15] by a chemical contribution $\mathrm{V_{chem}}$ shown with the ISFET in Fig. 3 and expressed as

$$V_{\mathrm{chem}} = \gamma - \alpha S_N \ \log([A]) \tag{3}$$

where A is the considered ion, typically $\mathrm{H^+}$ in standard CMOS technology, $\gamma$ includes a grouping of constant terms which are not dependent on the ionic concentration and $\alpha$ reflects the deviation from the Nernstian sensitivity $S_N = 59$ mV.

Several non-idealities exist in ISFET sensors. In particular, charge trapped at the floating gate or on the passivation layer can result in offset voltage, which in turn induces mismatch between pixels of the arrays. Also, charge slowly accumulates at the

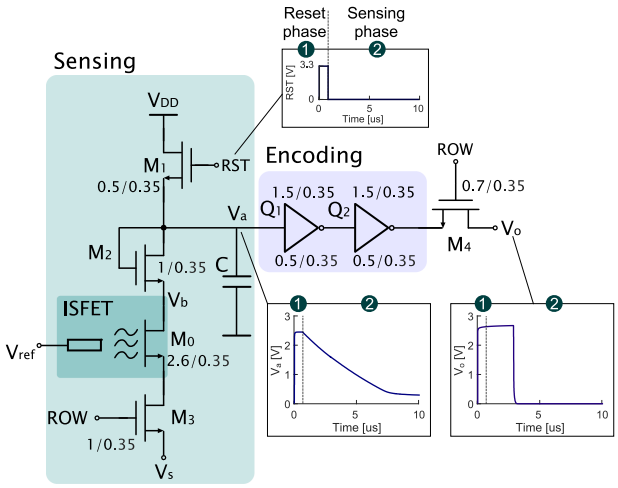



Fig. 3. Pixel architecture for the analogue sensing front-end with annotated sizes for the devices and simulated transient output signals.

interface between the solution and the semiconductor and causes drift in the threshold voltage of the device. Other deviations include temperature or light effects, which are common for all semiconductor devices.

## III. ISFET Pixel Architecture

In this section, we describe the pixel architecture shown in Fig. 4.

### A. Analogue Sensing Front-End

The analogue front-end is based on Active Pixel Sensor (APS) topologies commonly found in imagers and is shown in Fig. 3 with annotated sizes. The pixel operation consists in a reset phase and a readout phase, during which the current through the ISFET $\mathrm{M_0}$ determines the rate of discharge of node $\mathrm{V_a}$ through capacitor C, and hence the pulse width at the output $\mathrm{V_o}$. The topology performs in-pixel quantisation to reduce parasitics and signal degradation associated with long paths at a system level.

The ISFET is biased in weak inversion for low power operation by tuning the reference electrode voltage $\mathrm{V_{ref}}$. The discharge is defined by an exponential relationship between the current and the gate voltage

$$C\frac{dV_a}{dt} = -I_0 \exp\left(\frac{V_{g''s}}{nU_t}\right)\left[1 - \exp\left(-\frac{V_b - V_s}{U_t}\right)\right] \quad (4)$$

where $\mathrm{U_T}$ is the thermal voltage $kT/q$ and $\mathrm{V_b}$ is the voltage at the drain of the ISFET $\mathrm{M_0}$. In this equation we use $\mathrm{V_{g''s}}$ as the voltage at the gate of the equivalent MOSFET, hence at the floating gate of the ISFET. Assuming that $V_b - V_s > 4U_t$, which is valid for most of the discharge, we approximate the sensing phase as a linear discharge in time, starting from $V_{DD} - V_{th1}$ due to the soft reset of transistor $\mathrm{M_1}$ [18].

$$V_a(t) = (\mathrm{V_{DD}} - \mathrm{V_{th1}}) - At \quad (5)$$

where the discharge rate is given by

$$A = \frac{I_0}{C}\exp\left(\frac{V_{g''s}}{nU_t}\right) \quad (6)$$

Therefore, after quantisation by the inverters, the output is a pulse width modulated (PWM) signal with a pulse $\tau$

$$\tau \propto \exp\left(-\frac{V_{g''s}}{nU_t}\right) \Longrightarrow \tau \propto \exp\left(\frac{\alpha S_N \ \mathrm{pH}}{nU_t}\right) \quad (7)$$

and we obtain an exponential pH dependence of the pulse width.

We validate the pixel operation using Cadence Virtuoso in a standard 0.35 $\mu$m CMOS process. The ISFET is simulated using its aforementioned macromodel [15]. Fig. 5(a) illustrates the reset and readout phases for the encoding of the gate voltage in time. The exponential relationship is shown in Fig. 5(b).

The $\mathrm{V_{g''s}}$ term in (7) reflects several contributions according to the ISFET macromodel [6]

$$V_{g''s} = (\mathrm{V_{ref}} - V_{tc} - \mathrm{V_{chem}}) \times G_{\mathrm{chem}} - V_s \quad (8)$$

where $\mathrm{G_{chem}}$ is the scaling factor associated with the chemical attenuation due to voltage division between the passivation capacitance and the device capacitors $\mathrm{C_{ox}}$ and $\mathrm{C_d}$ [15]. The incidence of each of these terms on the circuit operation is now detailed.

1) $\mathrm{V_{ref}}$ is tuned to bias the ISFET in a given region of operation.
2) $\mathrm{V_{tc}}$ is a random offset for each pixel due to trapped charge.
3) $\mathrm{V_{chem}}$ is directly proportional to the pH, which yields the exponential relationship of (7).
4) $V_s$ is the only contribution which can be modulated independently to fix $\mathrm{V_{g''s}}$ to a desired value.

There are several non-idealities associated with the ISFET. To cancel the offset voltage $\mathrm{V_{tc}}$ mismatch between pixels, we integrate a calibration scheme to set $V_s$ inside each pixel. As a result, the output is constant for the whole array at the beginning of a measurement, without adding any circuitry to access the floating gate and hence degrading the signal. The choice of standard output is a trade-off between speed of operation and required sensitivity, as detailed in [18] and we have chosen a calibrated value of $\tau = 10$ $\mu$s, highlighted in Fig. 5(b). Section VII-H will discuss the extent of this choice in further detail. It should be noted that due to the quantisation by the inverters, the technique accounts for a trapped charge voltage swing of 1 V. Any variation in the switching threshold of the inverters will be included in the pixel calibration as pixel mismatch, and as such the range accounts for non-idealities related to the inverters. The same calibration scheme can also be applied periodically to cancel drift.

Similarly, in an attempt to reduce gain mismatch between pixels, capacitor C is implemented as a physical poly capacitor, which improves over the use of the parasitic capacitance in our previous work [18]. Its value was chosen as an order of magnitude higher than the parasitics capacitance evaluated from post layout simulations i.e., 39.173 fF.

The passivation capacitance induces chemical attenuation which is translated as a scaling factor $\mathrm{G_{chem}}$ for the chemical dependent voltage $\mathrm{V_{chem}}$ in (8). Minimising the attenuation requires a large $\mathrm{C_{pass}}$ i.e., a large sensing area with respect to the electrical area of the ISFET. In the case of this topology, a small $\mathrm{C_{pass}}$ compared to the gate-drain capacitance $\mathrm{C_{gd}}$ of the device also leads to coupling between the drain and the gate of the ISFET. $\mathrm{M_2}$ is used as a shield to reduce the coupling effect of the discharging node $\mathrm{V_a}$ to the floating gate $\mathrm{V_{g''}}$, providing a

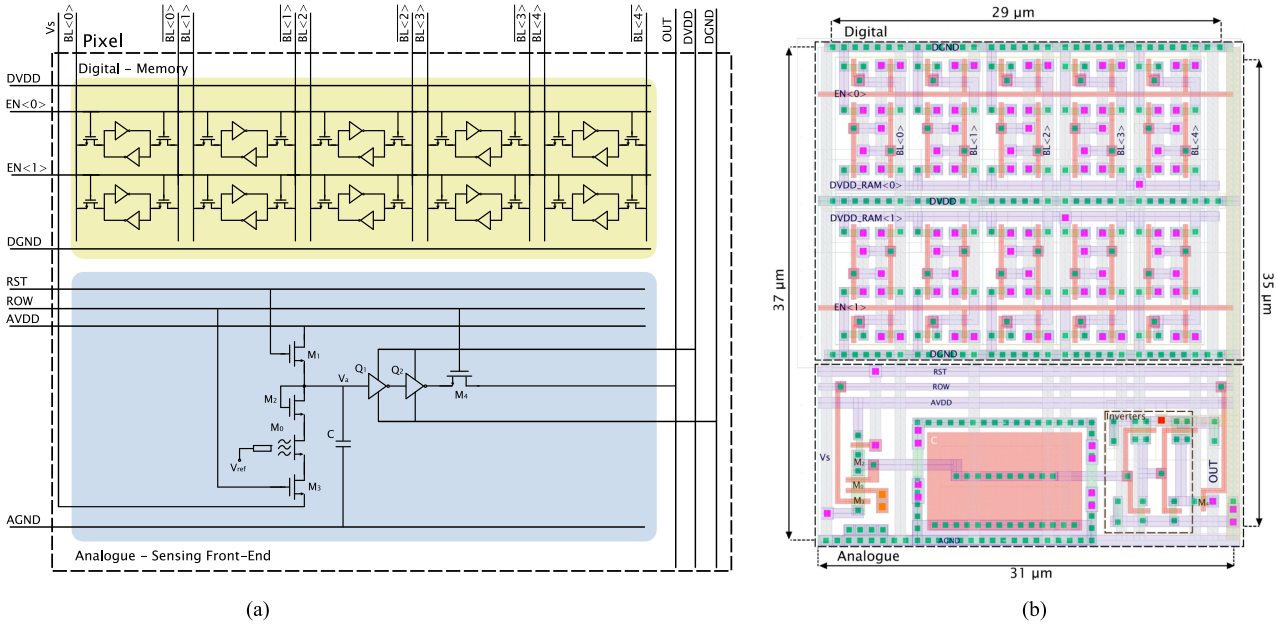



Fig. 4. Pixel topology containing both the analogue sensing front-end and the digital memory. (a) Pixel implementation with annotated ports. (b) Pixel layout with annotated pixel size and sensing area.

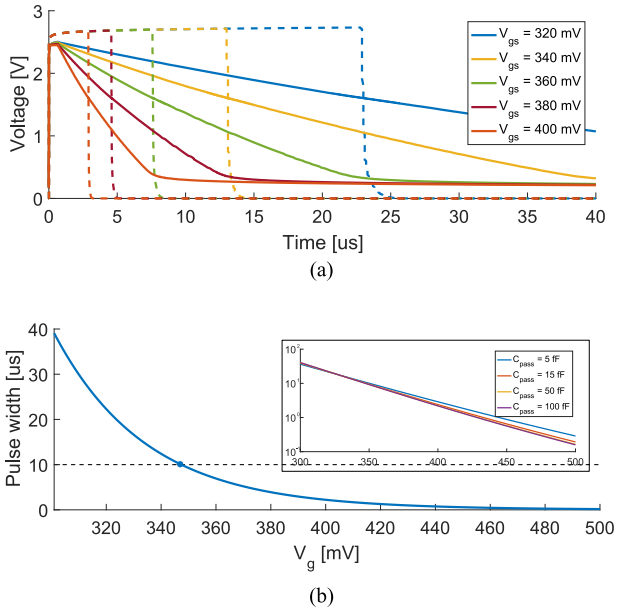



Fig. 5. Simulations for the pixel operation. (a) Pixel operation including the reset and readout phases. (b) The pulse width is an exponential function of pH. The top right graph shows improved sensitivity for higher values of $C_{\mathrm{pass}}$

current-dependent voltage drop

$$V_b = V_a - nU_t \ln\left(\frac{I}{I_0}\right) \tag{9}$$

The transistor is designed as a wide device to minimise the voltage drop and hence avoid limiting the readout range. The overall effect of the passivation capacitance is illustrated in the graph at the top right of Fig. 5(b), where the higher value of $\mathrm{C_{pass}}$ induces improved sensitivity.

### *B. Digital Memory*

The compensation algorithm requires to digitally store one value of ISFET source voltage $\mathrm{V}_s$ per pixel. Since the ISFET sensor requires a wide sensing area to minimise chemical attenuation, there is benefit to adding this memory inside the pixel to improve SNR. This also allows scalable of the sensor array with the process node. The stored digital value will be converted to analogue to provide a source voltage $V_s$ driving the ISFET in a specific region of operation. Since the exponential relationship of the front-end provides inherent high sensitivity to the chemical signal, the source voltage $V_s$ needed to control the ISFET requires a resolution 1 mV. As a result, the voltage is quantised as 10 bits, for a supply voltage of 3.3 V.

We implement a 10-bit in-pixel RAM designed as a standard double-ended 6T SRAM with each cell structured as two rows, which amounts to 10 bitlines per pixel and 2 enable lines. The transistors in the SRAM are all minimum size devices (nMOS $0.5/0.35$ $\mu$m and pMOS $1.5/0.35$ $\mu$m). The in-pixel digital memory is shown in Fig. 4. The bitlines are connected on a column level to a standard precharge and equalisation circuit as well as a sense amplifier.

### *C. Fully-Integrated and Scalable Pixel*

With the integration of the ISFET and the RAM, the reported array is now both a sensing and a memory array, with a system-level DAC interfacing analogue and digital contributions. The resulting pixel shown in Fig. 4 is now fully scalable, which is a requirement for today's large-scale integrated platforms, reaching more than a million sensors. As a result of this drive for large arrays, in-pixel memory offers self-sufficient pixels which do not suffer from increasing need for memory when scaling up. Furthermore, we leverage on the increase of the passivation capacitance $\mathrm{C_{pass}}$ with wider sensing area to provide

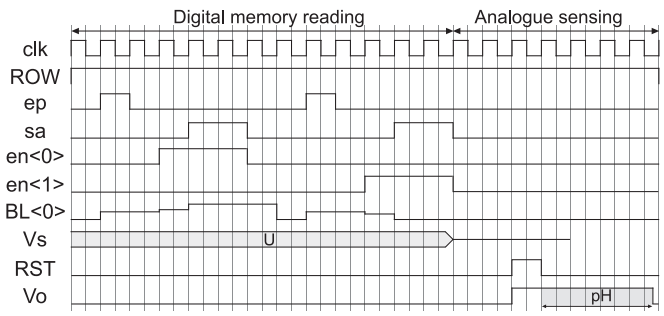



Fig. 6. Pixel readout operation for the RAM access and chemical sensing.

an opportunity to embed in-pixel digital memory and hence improve chemical coupling, boosting SNR.

The pixel operation is detailed in Fig. 6 for a standard pixel readout. First the in-pixel RAM is addressed to read the $V_s$ value. Due to the separation of the RAM cells in two rows, the five LSBs and five MSBs are respectively read sequentially. In each case, `ep` triggers the precharge of all bitlines to $V_{DD}/2$, `en` enables the current memory row and `sa` activates the sense amplifier to read the output from the latches. The 10 bits are then sent to the DAC and the analogue voltage is applied to the ISFET source. The analogue readout finally encodes the pH in time, as discussed previously.

Beyond scalability, designing in-pixel circuitry as opposed to system level blocks leads to a wider sensing area, which increases $C_{pass}$ and hence reduces the attenuation. This highlights a trade-off between SNR and spatial resolution, and justifies the use of wider pixels with more functionalities than simple ISFET readout [10].

## IV. System Implementation

The pixel is integrated as part of a full system to build the on-chip ion imaging platform, shown as a diagram in Fig. 7(a). We now provide further description of the block-level implementation.

### A. ISFET Array

The system includes a 78 × 56 pixel array. The pixels are arranged symmetrically in clusters of four so that the sensitive analogue parts is grouped together. At the centre of every cluster of 9 pixels sits a temperature pixel so that the temperature profile of the chip can be mapped accurately. The arrangement of the array is highlighted in Fig. 7(a).

The temperature pixel is a pixel with the same topology as the sensing pixel, however a MOSFET biased with a voltage $V_{temp}$ replaces the ISFET. This enables a sub-array of pixels imaging the temperature throughout the array, while being independent of any chemical change. This amounts to 3874 chemical pixels and 494 temperature pixels.

Several decoders are used to select pixels : (1) Row decoders provide the `EN` and `RST` signals, (2) Column decoders address the bitlines for read and write operation, and (3) One-hot decoders generate one-hot signals at both row and column levels.

At the bottom of the array, a row of sense amplifiers and a row of precharge and equalising circuits guarantee proper operation of the SRAM, as mentioned previously.

### B. Digital Core and SPI

The array timing is handled by an on-chip synthesised FSM, which allows to cycle through the pixels sequentially, fetch the digital $V_s$ value stored in RAM, acquire the output from the time-to-digital decoder and send it through a 16-bit SPI. The FSM also performs calibration in each pixel by sweeping the source voltage and storing the 10-bit value in the in-pixel memory. As detailed in [19], there are three parameters for calibration : `out_std` is the calibrated value, `tol` is the tolerance on that value and `step` is the step change at each iteration. A discussion on these parameters in views of the measurement results is provided in Section VII-H. Following calibration, the readout is then performed by sampling the pixel output sequentially with the $V_s$ value stored in the RAM.

### C. DAC and Buffer

We use a 10-bit DAC based on resistive dividers and provided as a standard cell by the Austrian Micro Systems foundry (AMS). The DAC converts the digital Vs value stored in the active pixel into an analogue source voltage for the same pixel. Its output operates between 0 V and 1.2 V.

### D. Time-to-Digital Converter

The digitisation of the pulse width is achieved through a ring oscillator-based time-to-digital converter (TDC) and a counter, which provide an asynchronous, accurate and high resolution conversion for the pixel output to be integrated as part of our calibration scheme [19]. The circuit implementation is shown in Fig. 8.

The circuit is inherently fast and requires size adaptation of the gates to match the noise resolution of the pixel and avoid saturating the counter. Each AND gate is implemented as a NAND gate (nMOS : 3 $\mu$m × 1 $\mu$m/pMOS : 4.5 $\mu$m × 1 $\mu$m) and an inverter (nMOS : 1.5 $\mu$m × 1 $\mu$m/pMOS : 4.5 $\mu$m × 1 $\mu$m). The sizes are made larger than minimum requirements to decrease oscillation frequency and hence resolution. The additional inverter is of smaller size (nMOS : 1.5 $\mu$m × 0.35 $\mu$m/pMOS : 0.5 $\mu$m × 0.35 $\mu$m).

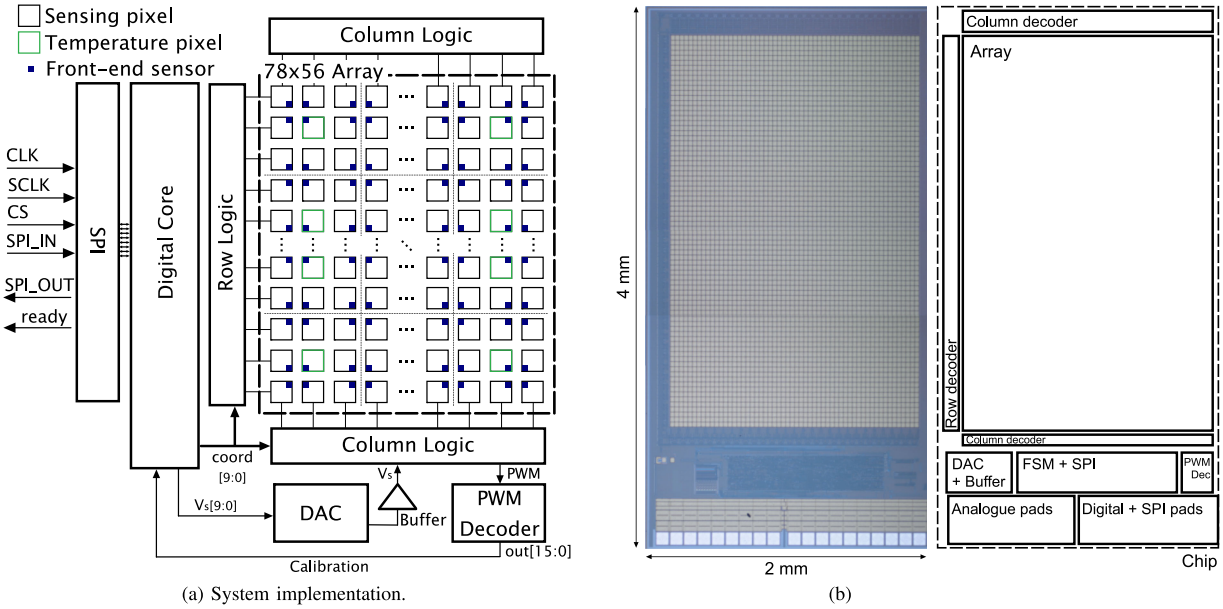
The multiplexer allows to select the resolution of decoding externally through frequency modulation. This enables to tune the resolution depending on the requirements given by the application.

## V. Fabricated System

We now describe the platform which has been used to take the measurements presented in the next sections.

### A. CMOS Prototype

The 4 × 4 mm chip was fabricated in AMS 0.35 $\mu$m and the microphotograph is shown in Fig. 7(b). The array occupies most of the chip area, with the peripheral circuits at the bottom. The pads are placed on one side of the chip to facilitate wire bonding and encapsulating, with the analogue and digital pads separated respectively on the left and right.




(a) System implementation. (b)

Fig. 7. System architecture with the 78 × 56 ISFET array. (a) System implementation. (b) Layout of the chip.

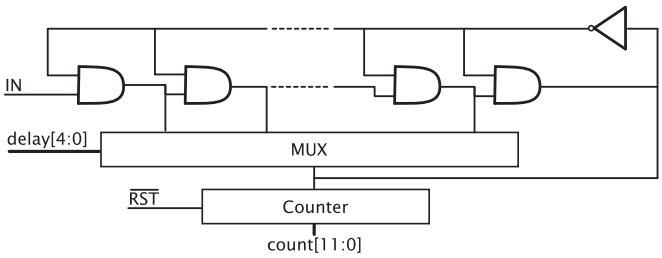



Fig. 8. Asynchronous time-to-digital converter.

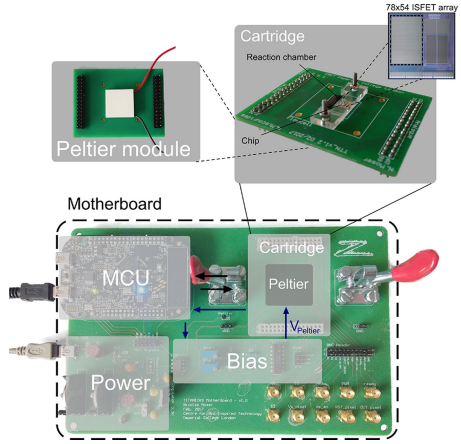



Fig. 9. PCB platform for monitoring of chemical reactions. The chip and the Peltier module are mounted on a disposable cartridge plugged into the motherboard, which handles power and data transmission.

### B. Cartridge

The die is glued on the ground plane of a 65 × 50 cm PCB cartridge with headers on each side for analogue and digital connections, shown in Fig. 9. After wire bonding, bio-compatible epoxy is used to cover the wire bonds of the chip. An acrylic manifold is then screwed on the chip, exposing as many pixels of the array as possible. This forms a reaction chamber for the monitoring of static chemical reactions.

A Peltier module is attached to a metal plane at the bottom of the cartridge. Vias provide a metal path between the bottom plane and the top ground plane to maximise heat conduction between the Peltier and the chip.

### C. Experimental Platform With Temperature Control

The cartridge is then plugged onto the motherboard depicted in Fig. 9. The power can be provided from a 5 V mini USB or from two 3 V coin cell batteries. The analogue bias voltages for the temperature pixels, the RAM and the DAC are generated using resistive dividers and buffers. The microcontroller (MCU) provides a clock for the chip at 1.5 MHz. Additionally, it accesses the SPI at 10 MHz to acquire the output data from the array and send it to MatLab using UART.

A controller is implemented on the MCU to acquire the data from the temperature pixels and apply a voltage to the Peltier module to perform temperature regulation of the system.

## VI. Electrical Characterisation

We start by characterising the dry performance of the system.

### A. Time-to-Digital Converter

We first characterise the TDC in terms of resolution and accuracy. For this purpose, the microcontroller provides a pulse width of 20 $\mu$s to the time-to-digital converter and reads the output. The period of the internal oscillator, and hence the ADC resolution, was measured throughout 8 dies and the results are shown in Fig 10 for the 32 values of the multiplexer. The resolution ranges from 12.8 ns to 33.1 ns, allowing to tune between fine and coarse readout, and shows an average standard deviation of 0.8% across dies around the mean value.

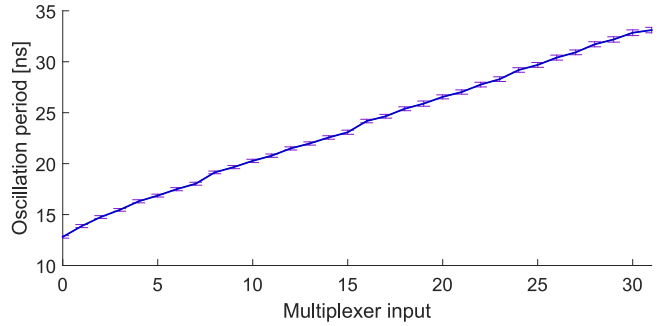



Fig. 10. Tunable resolution of the TDC across 8 dies.

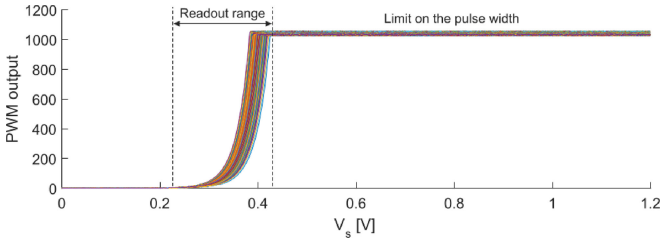



Fig. 11. Calibration curves of temperature pixels in dry conditions with gate voltage $V_g = 800$ mV.

For the upcoming measurements, we will consider the finest resolution (MUX = 0) and discuss the trade-off in Section VII-H, as there is a relation between maximum pulse width, number of bits in the counter and the resolution of the TDC.

### B. Temperature Pixels

The temperature pixels spread across the array are now characterised electrically as a sub-array. The output of each temperature pixel is monitored for a fixed gate voltage $V_{temp} = 800$ mV and a variable source voltage $V_s$ which represents the DAC range (from 0 V to 1.2 V).

The resulting calibration curves of Fig. 11 shows the expected exponential relationship and highlights the narrow readout range of around 150 mV. To avoid slowing down the system significantly, the FSM limits the pulse width to 20 clock cycles or 13.33 $\mu$s, which can be tuned accordingly. The graph highlights the variation between pixels. Denoting $V_{s\tau}$ as the calibrated $V_s$ value to reach an output of 10 $\mu$s, we characterise its statistical variation with a mean of 396.8 mV and variance of 12.6 mV. This mismatch is addressed by the initial calibration and therefore does not impact the system operation.

In order to characterise the temperature response of the sensors, we place the chips in a *Veriti Thermal Cycler* from Applied Biosystems and sweep the temperature from 30 °C to 80 °C. A thermocouple sensor is placed inside the liquid to measure accurately the temperature of the solution. The average output of the temperature array is shown in Fig. 12. The thermal transfer function can be approximated as

$$\tau = A\exp(-BT) \text{ where } A = 76.35 \text{ and } B = 0.06 \qquad (10)$$

This relationship will find useful when regulating the temperature across the array for several applications.

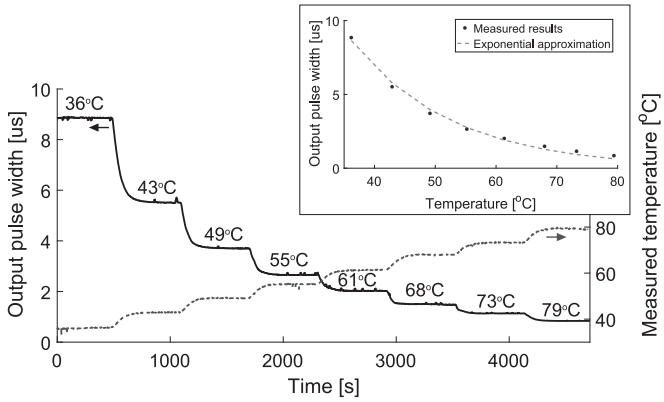



Fig. 12. Exponential variation of the temperature array output with temperature.

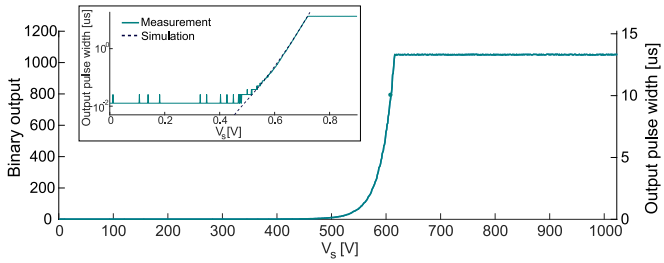



Fig. 13. Calibration curves for a chemical pixel on a linear (main) and logarithmic (top left) scale.

## VII. Chemical Characterisation

Having previously considered the dry parts of the system, we now expose the chip surface to a solution of pH 7 and observe the wet characteristics. In particular, we study the effect of all non-idealities such as trapped charge and drift, and demonstrate the compensation mechanisms of the platform.

### A. Pixel Calibration Curve

We isolate pixels of the array and show the calibration curve in Fig. 13, where once again the exponential dependence is highlighted. The pixel is also simulated with Cadence Virtuoso as a MOSFET with a floating gate voltage of 1.244 V, which matches its value at 10 $\mu$s. For direct comparison, the measured and simulated results are shown on the top left corner of the figure on a logarithmic scale. This highlights a good fit for the range of readout and a limit of detection which is the resolution of the TDC. Once again, the maximum value for the pulse width is limited by the FSM to guarantee fast operation of the system.

### B. Attenuation

The reference electrode voltage $V_{ref}$ is now swept while monitoring the reaction of the sensor. To ensure maximal range during the experiment, we continuously calibrate the system and define the attenuation as the variation in source voltage $V_s$ to maintain an output of 10 $\mu$s as a result of step changes of 1 V in $V_{ref}$, while taking into consideration the source-drain follower attenuation between gate and source voltages. The initial value of $V_{ref}$ does not matter due to the linear relationship between

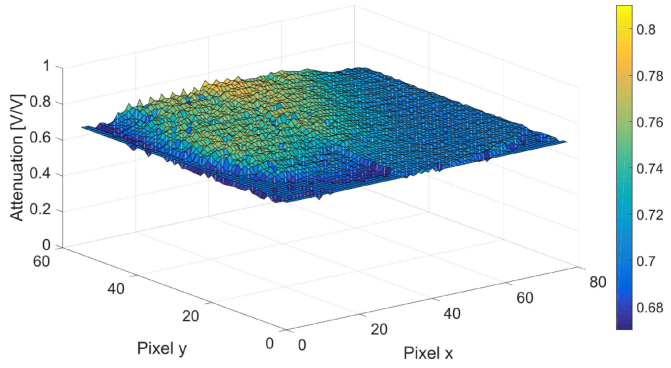



Fig. 14. Chemical scaling factor $\mathrm{G_{chem}}$ due to attenuation throughout the sensing array.

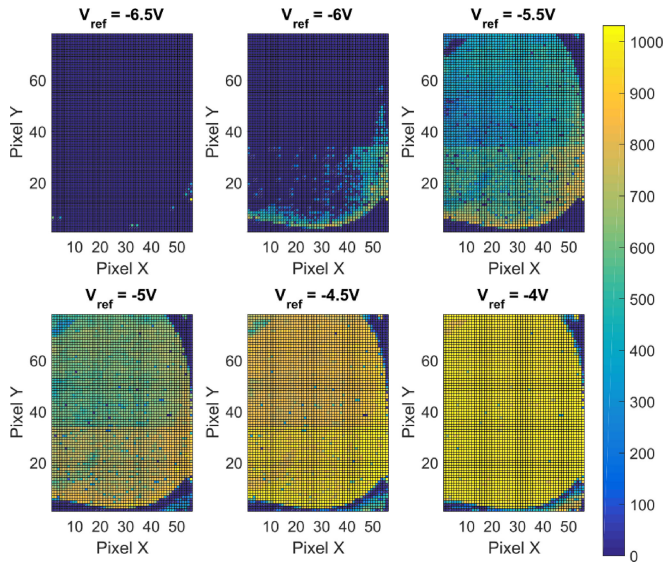



Fig. 15. Mapping of the calibrated source voltage $\mathrm{V_{s\tau}}$ for the $78 \times 56$ pixels with the temperature sub-array biased at $\mathrm{V_{temp}} = 800$ mV.

gate and source voltages, as long as the output stays within range of readout.

The result throughout the array is shown in Fig. 14. The average gain is $G_{\mathrm{chem}} = 0.72$ with a standard deviation of 0.027, which is shown to be spatially dependent. This demonstrates that the passivation layer of the commercial AMS technology is not perfectly uniform throughout the whole array, leading to minor discrepancies in SNR throughout the array. This can be compensated for during actual measurements by first deriving automatically the attenuation for all the pixels of the array with a simple $\mathrm{V_{ref}}$ sweep.

### C. Trapped Charge Mapping

Trapped charge has been identified as a challenge for floating gate sensors, particularly since the spread is essential for the proper operation of the calibration scheme presented in this work.

We now characterise the trapped charge by mapping the calibrated source voltage $\mathrm{V_{s\tau}}$ in the array when sweeping $\mathrm{V_{ref}}$. The array images of Fig. 15 show that for $\mathrm{V_{ref}} = -6$ V, all the

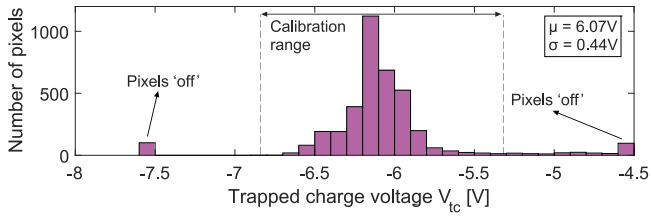



Fig. 16. Histogram of the trapped charge voltage $\mathrm{V_{tc}}$ of all the pixels in the array.

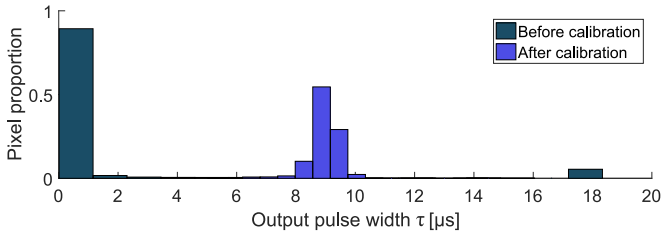



Fig. 17. Histogram of the array output for the 'on' pixels before and after calibration.

ISFETs have a small gate-source voltage $\mathrm{V_{g''s}}$ and increasing $V_s$ will not set the pixel in range. Hence $\mathrm{V_{s\tau}} = 0$V. As $\mathrm{V_{ref}}$ is increased, some pixels gradually reach a slower discharge as the calibration yields non-zero $\mathrm{V_{s\tau}}$ until $\mathrm{V_{g''s}}$ becomes too large and the opposite effect occurs. The last frame also depicts the location of the temperature pixels, which are biased at $\mathrm{V_{temp}} = 0.8$ V and hence independent of $\mathrm{V_{ref}}$. Furthermore, pixels at the edge of the array are covered with epoxy for proper encapsulation of the device, inducing a reduction in array efficiency. It can be observed that there is a similar spatial dependence to the attenuation profile of the array, suggesting that trapped charge is similarly affected by the non-uniformity of the fabrication process. This justifies the use for a calibration to set the bias of all the sensing devices.

We are now able to quantify the spread of trapped charge by referring the previous results back to the floating gate, using the average value of attenuation obtained previously. Fig. 16 shows the histogram illustrating the spread centered around $-6.07$ V. Considering that we can compensate for a range of 1 V at the floating gate, we are able to read from pixels with a trapped charge with a spread of $1\,V/G_{\mathrm{chem}} = 1.5$ V. Assuming that about 400 pixels are covered by epoxy due to chip encapsulation, the calibration scheme is able to read 95 % of the sensing array i.e., roughly 3350 pixels.

### D. Array Calibration

The calibration scheme described in [19] is applied successfully to the array to store the compensated source voltage values $\mathrm{V_{s\tau}}$ inside each pixel. The calibration is performed when the sensors are exposed to a solution of pH 7 and at $\mathrm{V_{ref}} = -1.49$ V. As discussed in the previous section, the calibration applies to all pixels in the range of trapped charge and not covered with epoxy. The output of the remaining pixels is shown in Fig. 17. As can be seen, most pixels exhibit a high $\mathrm{V_{gs}}$ at the start due to trapped charge, and the compensation sets the proper operating

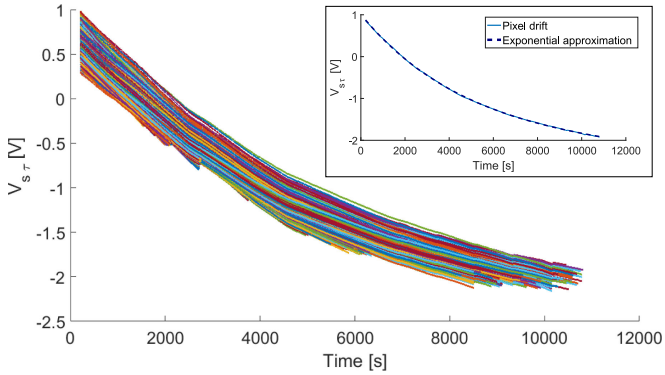



Fig. 18. Output drift for all pixels of the array with $V_{ref} = -1.5$ V and $V_s = 0$ V. Top right : average drift curve.

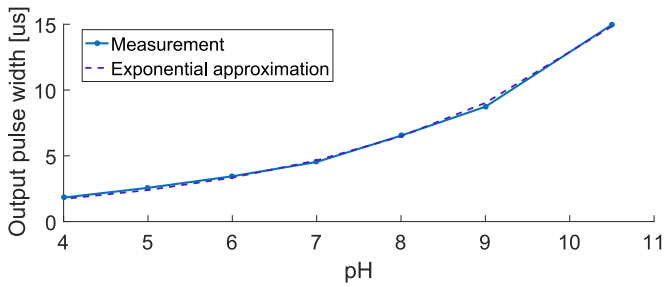



Fig. 19. Average array output when the chip is exposed to a solution of pH 4 to 10.5 with drift removal.

range of the ISFET with a mean of 9 $\mu$s with a standard deviation of 370 ns. When referred back to the source voltage $V_s$, which is a linear scale, sums up to a 0.3% spread.

### E. Chemical Drift

To characterise the impact of sensor drift, we consider a new die which is exposed to pH 7 for the first time and monitor the array output for 3 hours. Once again, for increased range, we operate the readout through the source voltage $V_{s\tau}$. For this experiment, we set $V_{ref} = -1.5$ V and yield the temporal output variation of Fig. 18. The gate voltage of the ISFETs is shown to drift on average by $-49.2$ mV/min during the first hour of the experiment, before settling.

### F. pH Sensitivity

In order to test the pH sensitivity of the array, we replace the manifold with a flow cell clamped on top of the chip. A peristaltic pump is connected to the inlet for constant flow of solution. We use various buffer solutions with pH ranging from 4 to 10.5 for full characterisation of the chip chemical response. The buffers are prepared using 3M KCl (Sigma Aldrich 60137), 1M Tricine (Sigma Aldrich T0377) and DI water. They are then brought to the suitable pH by adding 1M HCl (Sigma Aldrich 318949) or 1M NaOH (Sigma Aldrich 71463).

The results are shown in Fig. 19. The measurement was performed after the drift characterisation of Section VII-E. Considering the sampled drift rate of 0.01 mV/s by the end of the experiment, we post-process the data to remove the effect of drift for an accurate characterisation of the pH response of the sensor.

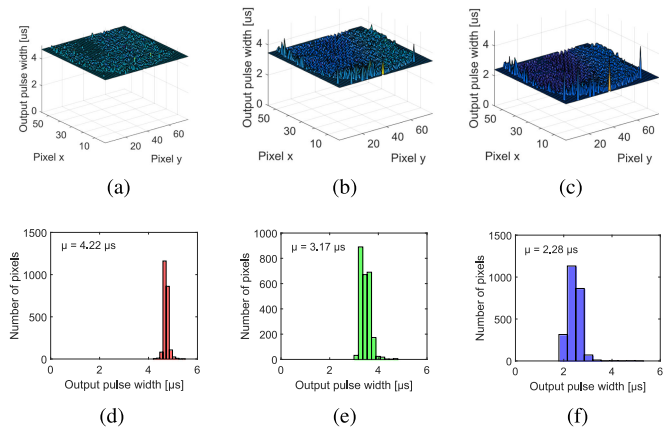



Fig. 20. Output variation of the array for a change of pH from 7 to 6 and 5 with corresponding histogram. (a) pH 7. (b) pH 6. (c) pH 5. (d) pH 7. (e) pH 6. (f) pH 5.

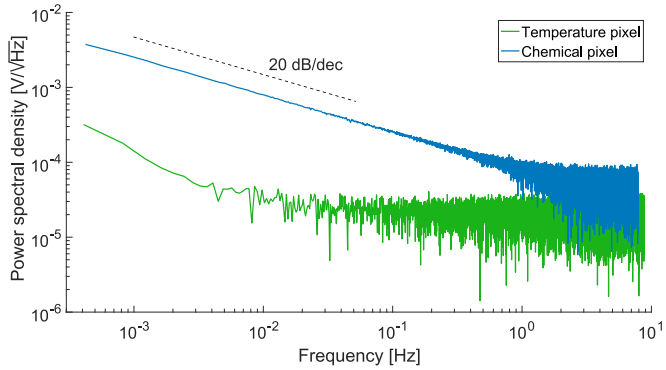



Fig. 21. Input-referred noise for a temperature and a chemical pixel in the array, demonstrating the noise originating from the sensing surface.

The average intrinsic pH sensitivity of the ISFETs is 11.91 mV/pH with a standard deviation of 1.57 mV/pH, due to spatial non-uniformity. This translates to a sensitivity of 3.31 $\mu$s/pH at the calibrated value of 10 $\mu$s, given by the inherent exponential dependence of the sensing front-end.

Fig. 20 shows the array when the pH is varying from pH 7 to 5. Baseline frame calibration was performed at pH 7 for improved accuracy of the readout. The experiment shows a uniform change in pH in the flow cell, with the standard deviation related to the spatial distribution mentioned previously. We demonstrate that the array output indeed reflects the pH variation inside the flow cell.

### G. Pixel Noise and pH Resolution

In this experiment, we select pixels of the array exposed to the solution of pH 7, one temperature pixel and one chemical sensor. The pixels are calibrated and sampled continuously for 40 minutes. The input-referred noise for each pixel is shown in Fig. 21, demonstrating the larger contribution of chemical noise compared to electrical noise, originating from the dangling bonds at the surface due to the impurity of the passivation layer.

TABLE I
TRADE-OFF FOR THE STANDARD OUTPUT DURING CALIBRATION

| `out_std` [$\mu$s] | Sensitivity [$\mu$s/pH] | Resolution [ns] | TDC MUX | Calib time [s] | Frame rate [fps] |
|---|---|---|---|---|---|
| 1 | 0.33 | 6.3 | 0 | 50 | 0.75 |
| 5 | 1.66 | 31.5 | 21 | 100 | 0.53 |
| 10 | 3.31 | 62.9 | 31 | 120 | 0.23 |
| 20 | 6.63 | 126 | 31 | 150 | 0.17 |
| 100 | 33.28 | 632.3 | 31 | 200 | 0.1 |

Flicker noise exhibits a difference of one order of magnitude, which validates the result previously obtained by Liu *et al.* [20]. The thermal noise, which has never been characterised before, is shown to have less significant discrepancies between ISFET and MOSFET which in turns increases significantly the corner frequency of the chemical pixel to 1 Hz compared to 10 mHz for the temperature pixel. This reduces the benefit of array averaging on the SNR.

Since a pH reaction generally occurs in the order of magnitude of 100 s, we integrate the measured noise from 10 mHz to 8 Hz and yield a value of 0.06 mV and 0.23 mV for the temperature and chemical pixels respectively. Considering the pH sensitivity, this amounts to a resolution of 0.019 pH for the sensors. It should be noted that the chemical resolution could be improved by averaging, at the expense of spatial resolution or frame rate.

### *H. Discussion : Trade-Off for the Calibrated Value*

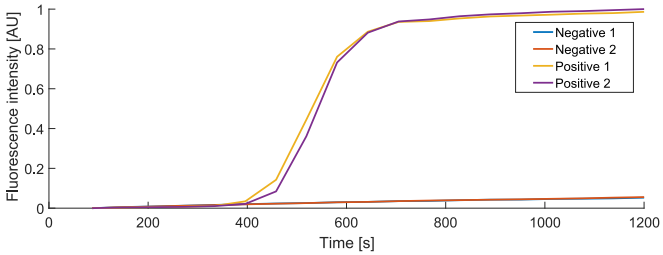
We now discuss the value of calibrated output, which is the main parameter for the system operation. Due to the exponential dependence, it is clear for instance that the pH sensitivity between pH 8 and 9 is significantly higher than between pH 5 and 6, hence the calibration can be set to maximise sensitivity for the range of interest. However, increasing readout sensitivity comes at the cost of lower speed of operation due to the time encoding and higher power consumption due to the slower discharge. Similarly, the choice of calibrated value justifies the tunable resolution for the TDC. At the standard output of 10 $\mu$s, the minimum resolution of TDC is still higher than the noise resolution, but at higher values of calibrated outputs, the oscillator can be slowed down to compensate for the increase in the pixel power consumption.

Table I shows the results for several calibrated value `out_std` in terms of pH sensitivity, calibration time and frame rate. The time resolution to match the sensor noise floor of 0.23 mV is also included, highlighting that the TDC can be tuned to operate at a higher resolution between standard values of 1 $\mu$s and 10 $\mu$s.

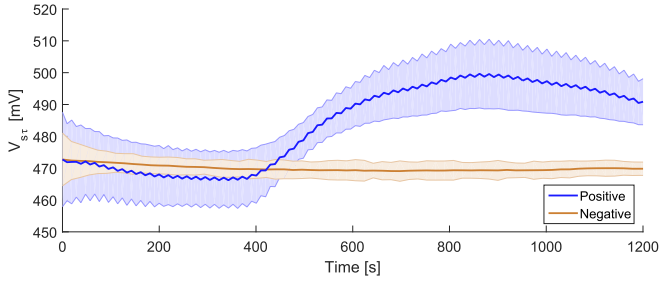
This illustrates the flexibility of the array to different applications, with the user able to tune operation depending on required sensitivity and frame rate.

## VIII. ON-CHIP DNA AMPLIFICATION AND DETECTION

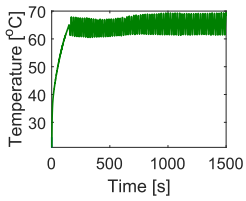
In this section, we present the platform as a PoC device by demonstrating its capabilities towards simultaneous amplification and detection of specific DNA sequences on-chip.




(a)




(b)




(c)

| | Yield [ng/ul] | | pH | |
|---|---|---|---|---|
| | Pre | Post | Pre | Post |
| Neg | 13.7 | 12.83 | 8.4 | 8.62 |
| Pos | 14.87 | 874 | 8.74 | 7.84 |

(d)

Fig. 22. Results for the DNA amplification in the benchmark instrument and on-chip. (a) Positive and negative pH LAMP reactions performed in a LightCycler 96 System. (b) Positive and negative pH LAMP reactions performed on-chip, filtered to smooth the small temperature variations. (c) Temperature profile during DNA amplification. (d) DNA yield and pH variation measured for in tube reactions pre- and post-LAMP.

For this specific example, pH LAMP is used to amplify lambda phage DNA while generating a pH variation which is measured by the chip. LAMP primers specifics for phage lambda were developed as described in [21]. 12 $\mu$L of the amplification solution was loaded into a microfluidic chamber on top of the chip and the Peltier module was mounted on the bottom of the cartridge. The following on-chip operations were carried out immediately after:

1) The temperature array is calibrated at ambient temperature and the $V_{s\tau}$ values are stored as the temperature footprint of the chip.
2) The chemical array is calibrated with the optimal reference electrode voltage $V_{ref}$ to maximise the number of active pixels.
3) The temperature is elevated at 63 °C using the Peltier module as heater, the temperature array as sensors and the MCU as the controller.
4) The array output is continuously sampled and at each frame, the controller adjusts the Peltier input to maintain constant temperature.

Positive (with $10^8$ genomic copies/$\mu$L of lambda phage DNA) and negative (without DNA) amplification solutions are

TABLE II
PERFORMANCE OF THE SYSTEM

| | |
|---|---|
| Technology | AMS 0.35 $\mu$m |
| Pixel size | 37 $\mu$m $\times$ 31 $\mu$m |
| Chip size | 4 mm $\times$ 2 mm |
| Number of chemical pixels | 3874 |
| Number of temperature pixels | 494 |
| Maximum drift rate | 6.5 mV/min |
| Offset compensation range | 1 V |
| Pixels in range | 95% |
| Calibration | $\mu = 9$ $\mu$s, $\sigma = 370$ ns |
| pH sensitivity | 11.91 mV/3.31$\mu$s for 1 pH @ 10 $\mu$s |
| Measured input referred noise | 0.23 mV |
| Resolution of ADC | 12.8 ns |
| pH resolution | 0.019 pH |
| Power consumption | 7.5 mW @ 3.3 V |

TABLE III
COMPARISON OF ISFET SENSING ARRAYS

| Ref. | [22] | [23] | [24] | [9] | **This work** |
|---|---|---|---|---|---|
| Technology | 0.18 $\mu$m | 0.35 $\mu$m | 0.35 $\mu$m | 0.35 $\mu$m | 0.35 $\mu$m |
| Pixel Size | 20 $\mu$m $\times$ 2 $\mu$m | 150 $\mu$m $\times$ 150 $\mu$m | 10.2 $\mu$m $\times$ 10.2 $\mu$m | 50 $\mu$m $\times$ 50 $\mu$m | 37 $\mu$m $\times$ 31 $\mu$m |
| Array Size | 8 $\times$ 8 | 8 $\times$ 8 | 64 $\times$ 64 | 32 $\times$ 32 | 78 $\times$ 56 |
| Trapped charge compensation | No | PG-ISFET | No | Gate switch | Source voltage |
| Temperature monitoring | No | No | No | No | Yes |
| SNR @ pH 7 | – | 5.01 dB | – | 23.65 dB | 34.16 dB |

also loaded into 0.2 mL PCR tubes and heated at 63 °C for 20 minutes on a conventional real-time PCR instrument (LightCycler 96 System, Roche Diagnostics) for validation purposes and direct comparison with on-chip reactions. A fluorescent DNA-detecting intercalation dye (SYBR Green) was added to the tubes for the detection of dsDNA products during pH LAMP.

The results obtained from the benchmark instruments and the chips are shown respectively in Fig. 22(a) and (b), where the chip reading is shown from the source voltage to linearise the response. The experiments were repeated three times and these results were validated. The temperature profile of the chip is also depicted in Fig. 22(c) to demonstrate that the controller maintains the temperature around 63 °C during the reaction. A slight variation around 63 °C justifies the choice of LAMP as a DNA amplification method, demonstrating that the reaction does not require temperature cycles like with PCR, but also that it offers tolerance around the absolute temperature. We can observe that the DNA amplification adopts the same profile in both situations, leading to a time-to-positive of 400 seconds, which suggests that DNA can be reliably amplified on-chip and DNA quantification based on amplification kinetics is possible. Fig. 22(d) shows the variation in DNA yield and pH pre- and post-amplification in the tube, averaged over three reactions. These results demonstrate a change of 0.9 pH with pH LAMP, while the chip output varies by 30 mV during the reaction which amounts 2.22 pH. It is expected that the increased drift with higher temperature and change in pH added up to the contribution of the pH change and boosted the sensitivity of the sensor. Overall, the platform demonstrated proper DNA detection through pH LAMP.

## IX. CONCLUSION AND FUTURE WORK

We have reported the design of a self-calibrating Lab-on-Chip platform in 0.35 $\mu$m CMOS technology which integrates an analogue sensing ISFET and a digital memory array. The pixel achieves in-pixel quantisation which improves robustness and encodes the pH in time with a high exponential sensitivity. The digital approach in the pixel design enables scalability of the system to sub-micron technology. The topology calibrates the sensor in-pixel to cancel offset and drift, which are common issues known to the sensor. Temperature pixels are spread throughout the array to monitor the temperature during the reaction. The 78 $\times$ 56 array has been integrated as part of a full system which includes a time-to-digital converter, an embarked FSM and an SPI for interface to an external microcontroller. Lastly, the system was demonstrated for on-chip DNA detection.

The system performance is summarised in Table II. The average sensitivity of 3.2 $\mu$s/pH along with a high resolution TDC. The calibration achieves 95% pixel efficiency with 4% standard deviation which can be corrected with baseline frame calibration. Overall, the system is capable of pH and temperature monitoring for various on-chip reactions.

The platform is compared with previous work in Table III, building upon the work carried out in [9]. We show that the platform is the first large array with automatic calibration of trapped charge and temperature monitoring to exhibit a high and tunable exponential pH sensitivity. We also consider the ratio of sensitivity and resolution as a metric for comparison of sensing array topologies, and show that our system achieves the highest SNR reported so far.

The results presented in this paper drive the push towards future use as a Lab-on-Chip platform. More importantly, it paves the way to opening CMOS technology to Point-of-Care diagnostics of infectious diseases, which can now be integrated as part of portable and robust devices. As such, this platform can now be investigated towards a wide range of new applications in the fields of real-time monitoring and diagnostics.

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**Nicolas Moser** (S'15) received the B.Sc. degree in electronic and chemical engineering from the Université Catholique de Louvain, Louvain-la-Neuve, Belgium, in 2013, the M.Sc. degree in analog and digital integrated circuit design from the Department of Electrical and Electronic Engineering, Imperial College London, London, U.K., in 2014, and the M.Res. degree in advanced computing from Imperial College London, London, U.K., in 2015 He is currently working toward the Ph.D. degree at the High Performance Embedded and Distributed Systems EPSRC Centre for Doctoral Training, within the Centre for Bio-Inspired Technology, Department of Electrical and Electronic Engineering, Imperial College London.

His research interests include the design of mixed-signal integrated circuits for Lab-on-Chip applications, with a specific focus on ion imaging using ISFET arrays. He was the recipient of the Hertha Ayrton Prize 2015 for the Best M.Sc. project with significant original contribution to the topic area and the Outstanding Achievement Prize for the analog and digital integrated circuit design in M.Sc.

**Jesus Rodriguez-Manzano** received the B.Sc. degree in biological sciences and the Ph.D. degree in biotechnology and environmental microbiology from the University of Barcelona, Spain, in 2005 and 2012, respectively.

He is currently a Research Fellow with the Department of Electrical and Electronic Engineering, Centre for Bio-Inspired Technology, Imperial College London. His background in microbiology and molecular biology was followed by a three-year Postdoctoral position with the Division of Chemistry and Chemical Engineering, California Institute of Technology, where he was developing cutting edge Point-of-Care diagnostic technologies for infectious diseases. He is the author or coauthor of 25 scientific publications and 3 international patents with more than 1200 citations. His research interest focuses on the interface of biology and engineering, including: development of low-cost sample preparation methods, innovative molecular tools for detection, quantification and typing of microbial pathogens, microfluidics, isothermal nucleic acid amplification chemistries, and digital single-molecule analysis.

**Tor Sverre Lande** (M'93–SM'06–F'10) is currently a Professor in micro/nanoelectronics with the Department of Informatics, University of Oslo, Oslo, Norway, and a Visiting Professor with the Institute of Biomedical Engineering, Imperial College, London, U.K. He is the author or coauthor of 150 scientific publications with chapters in two books. He is serving as an Associate Editor for several scientific journals. His primary research is related to analog and digital microelectronics. His research interests include neuromorphic engineering, analog signal processing, micropower circuit and system design, biomedical circuits and systems, and impulse radio for wireless and radar.

He has served as a Guest Editor of special issues including the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS PARTS I AND II, as well as a special issue on Biomedical Circuits and Systems. In 2006, he was appointed as a Distinguished Lecturer of the IEEE Circuits and Systems Society and an elected member of CAS Board of Governors. He was the first Editor-in-Chief for the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS (2007–2010). He is also the cofounder of the spin-off company Novelda AS.

**Pantelis Georgiou** (AM'05–M'08–SM'13) received the M.Eng. degree in electrical and electronic engineering and the Ph.D. degree from Imperial College London (ICL), London, U.K., in 2004 and 2008, respectively.

He is currently a Reader with the Department of Electrical and Electronic Engineering, ICL, where he is also the Head of the Bio-Inspired Metabolic Technology Laboratory, Centre for Bio-Inspired Technology. He has made significant contributions to integrated chemical-sensing systems in CMOS, conducting pioneering work on the development of ion-sensitive field-effect transistor sensors, which has enabled applications, such as point-of-care diagnostics and semiconductor genetic sequencing and has also developed the first bioinspired artificial pancreas for treatment of Type I diabetes using the silicon-beta cell. His research interests include bioinspired circuits and systems, CMOS-based lab-on-chip technologies, and application of microelectronic technology to create novel medical devices. He was the recipient of the IET Mike Sergeant Medal of Outstanding Contribution to Engineering in 2013. In 2017, he was also the recipient of the IEEE Sensors Council Technical Achievement Award. He is a member of the IET and serves on the BioCAS and Sensory Systems Technical Committees of the IEEE CAS Society. He is also the CAS representative on the IEEE Sensors council and the IEEE Distinguished Lecturer in circuits and systems.