Analysis and Investigation of Internal AC Frequency to Minimize AC Current Magnitude and Reactive Power Circulation in Chain-Link Modular Multilevel Direct DC-DC Converters

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***Abstract*—Chain-link modular multilevel direct dc-dc converters (CLMMCs) have attracted much interest recently in for dc power systems because they achieve higher device utilization, lower power losses and they are physically more compact than the alternative front-to-front modular multilevel dc-ac-dc converters (FFMMCs). The CLMMCs rely on circulating an internal ac current to manage energy balance of the sub-module (SM) stacks but this current inevitably contributes to extra current stresses for circuit components and can also lead to excess reactive power circulation within the converter. This paper presents a circuit analysis that there exists a frequency value for the internal ac components that may minimize the current stresses and avoid excessive reactive power circulation. For illustration, the circuit analysis is applied to one of the base formats, the buck-boost CLMMC as an example. The key relationship between the CLMMC and the standard dc-ac modular multilevel converter is explored and established. The equivalent circuits for their dc and ac components with consideration of SM capacitance and SM voltage ripples are created and analyzed in detail, and a full derivation is provided for the specific ac frequency. From this example, this analytical method is extended and applied to other base formats of CLMMCs. The theoretical analysis and results are verified by a set of full-scale simulation examples and down-scaled experiments on a laboratory prototype.**

***Index Terms*—Power electronics, circuit analysis, dc-dc conversion, internal ac frequency, reactive power circulation.**

I. Introduction

IN SEVERAL regions of the world, the use of point-to-point dc links has grown rapidly in the last decade and has led to strong interest in interconnecting such links into dc networks and dc grids [1]–[4]. This interest has turned into reality with examples at medium-voltage or high-voltage dc networks being brought into operation or reaching an advanced planning phase [5]–[11]. However, in the absence of standard utility codes for dc power system, the voltage adopted for dc has been tailored to specific projects and thus a wide variety of dc voltages are seen [12]–[15]. This voltage variety presents an obstacle to interfacing point-to-point dc links and small dc networks together to form larger dc grids, and that obstacle will need to be overcome by power electronics based dc voltage transformation equipment [16]–[18]. These high-power dc-dc converters will play the key role for the interconnections of several dc links with different voltages and also provide benefits for the power flow control in the multi-terminal dc networks and dc grids [19]–[21].

The modular multilevel converter (MMC) [22] has become the favored format for dc-ac conversion in dc transmission and distribution thanks to its advantages of scalability, reliability and controllability [23]–[25]. It is also the inspiration for dc-dc conversion and many proposals have been put forward [26], [27]. The front-to-front modular multilevel dc-ac-dc converters (FFMMCs) [28], [29] can inherit all of the operational benefits of the classic MMC and the dc-ac-dc arrangement provides the converters with dc-fault blocking capability but the double-conversion arrangement leads to low power device utilization, high power losses and large physical volume. The chain-link modular multilevel direct dc-dc converters (CLMMCs) were proposed [30] and it attracted much attention in recent years. The key concept is that a phase leg or multi-phase legs of a classic dc-ac MMC is rearranged to perform single-stage direct dc-dc conversion. The topologies of the single-phase CLMMCs were presented [31], [32], including the original one-phase leg version and the two-phase leg push-pull version. The three-phase variations with basic operation principles were given [33] for higher power rating requirement, and the bipolar circuits with control strategy were further studied [34] to satisfy various system configurations in dc networks and dc grids. Hybrid and full-bridge variants of the CLMMC are also known [35] and they are the dc-dc counterparts of hybrid and full-bridge dc-ac MMC [36]. The presence of sufficient full-bridges in these converters allows them to block or control the passage of fault

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current in the event of dc fault. Practical circuit design for CLMMCs has been analyzed and the filters of passive and active choices also discussed [37]. The CLMMCs gives a large reduction in the total number of sub-modules (SMs) compared to the FFMMCs with clear advantages in overall cost, conversion efficiency and system footprint [38].

However, the CLMMCs rely on circulating an internal current to balance the stack energy and this current must be ac to make its energy transfer independent of the main input-to-output transfer of the dc currents [26], [27]. Inevitably, this internal ac current contributes to extra current stress for circuit components and can also lead to undesirable reactive power circulation within the converter. In principle, the frequency of the internal ac components could be freely chosen in a CLMMC for energy balance purpose but in fact the frequency makes important effect on the extent of extra ac current stress and excess reactive power circulation in the circuit [30], [39].

To date, there is insufficient study of the choice on internal ac frequency to manage the current stress and reactive power for CLMMCs, and the ac frequency value in many examples is arbitrarily selected except some preliminary concepts were presented in conference proceedings [39], [40]. This paper sets out a detailed analysis for this frequency through quantifying the internal ac current magnitude and reactive power circulation in the principal circuit. For illustration, the circuit analysis is applied to one of the base formats, the buck-boost CLMMC as an example. The relationship to and comparison with the single-phase dc-ac MMC are discussed and analyzed in Section II. The dc and ac current components with consideration of SM capacitance and SM voltage ripples are investigated through equivalent circuits in Section III, and a full derivation is provided for a specific frequency that may minimize the internal ac current magnitude and avoid excess reactive power circulation. From this example, the analytical method is extended in Section IV and applied to other base formats of CLMMCs, such as the buck CLMMC and boost CLMMC. The theoretical analysis and results are verified through a set of full-scale simulation examples in Section V and further verified by experimental tests on a down-scaled prototype in Section VI.

II. Circuit Operation and Current Loops

This section presents analysis of circuit operation and current loops for the single-phase dc-ac MMC and the buck-boost CLMMC. The two formats are compared and contrasted in detail. Specific technical challenges in design and operation of the chain-link dc-dc converters are raised at the end of this section.

Fig. 1 shows the single-phase dc-ac MMC circuit with two stacks of SMs on the right, a balanced pair of dc sources on the left and a passive ac load placed centrally [22]. The black arrows define the reference directions of the branch currents, the symbols "+" and "–" in black define the voltage directions. The blue arrow is the loop path of the dc current and the red arrows are the two paths contributing ac current to the load and all are shown in the expected directions for operation as an inverter.

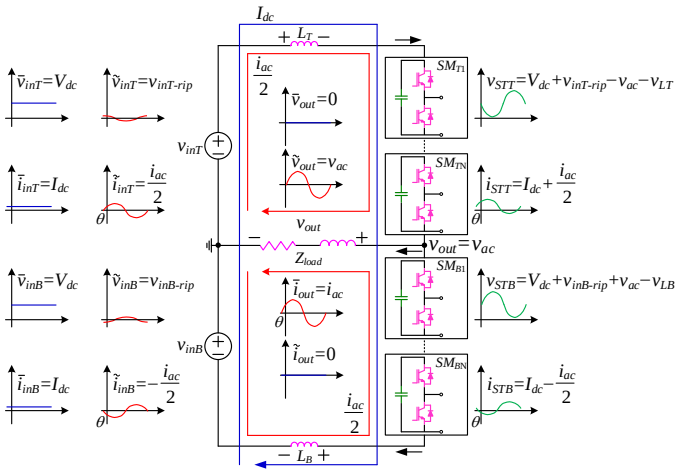


Fig. 1. Current loops in the single-phase dc-ac MMC (modified from [40]).

If this dc-ac MMC is properly controlled, no dc current flows in the load and dc currents through the two input sources, $\bar{\imath}_{inT}$ and $\bar{\imath}_{inB}$, are the same, as indicated by the outer blue loop, I_{dc}. The dc current is seen to be a common mode component of the top and bottom stack currents. The ac output current, $\tilde{\imath}_{out}$, indicated by i_{ac}, divides into two equal parts, $\frac{i_{ac}}{2}$, through the red loops and have different directions with respect to their respective stack current references. They are seen as differential mode components of the top and bottom stack currents. Since the stack energy must be balanced, the net energy deviation over an ac cycle, T, caused by the combination of ac and dc voltages and currents of the stacks should be zero, as expressed in (1) and (2),

$$\int_0^T v_{STT}(t)i_{STT}(t)dt = \int_0^T \left[V_{dc} + v_{inT-rip} - v_{ac}(t) - v_{LT}(t)\right]\left[I_{dc} + \frac{i_{ac}(t)}{2}\right]dt = 0 \quad (1)$$

$$\int_0^T v_{STB}(t)i_{STB}(t)dt = \int_0^T \left[V_{dc} + v_{inB-rip} + v_{ac}(t) - v_{LB}(t)\right]\left[I_{dc} - \frac{i_{ac}(t)}{2}\right]dt = 0 \quad (2)$$

where v_{STT} and i_{STT} are the voltage and current of top stack, v_{STB} and i_{STB} are the voltage and current of bottom stack, v_{LT} and v_{LB} are the inductor voltage of top arm and bottom arm, V_{dc} and I_{dc} are the dc component voltage and current from the input dc sources v_{inT} and v_{inB} ($\bar{v}_{inT} = \bar{v}_{inB} = V_{dc}, \bar{\imath}_{inT} = \bar{\imath}_{inB} = I_{dc}$), $v_{inT-rip}$ and $v_{inB-rip}$ are the small ac component voltage on the input dc sources v_{inT} and v_{inB} ($\tilde{v}_{inT} = v_{inT-rip}, \tilde{v}_{inB} = v_{inB-rip}$), v_{ac} and i_{ac} are the ac component voltage ($\tilde{v}_{out}(t) = v_{ac}(t) = V_{ac}\sin\omega t$) and current ($\tilde{\imath}_{out}(t) = i_{ac}(t) = I_{ac}\sin(\omega t + \theta)$) through the ac load Z_{load}. V_{ac} and I_{ac} are the magnitude of ac load voltage and current, ω is the angular frequency of the ac components ($\omega = 2\pi f = \frac{2\pi}{T}$) and θ is the phase difference between them. The illustrative waveforms for these voltages and currents have been also provided in Fig. 1 at appropriate locations.

Evaluating the dc and ac components of (1) and (2) leads to (3), which is the required relationship between the ac and dc terms for energy balance. A modulation index m has been defined between V_{ac} and V_{dc} such that $V_{ac} = mV_{dc}$ and for half-

bridge SM stacks $m \leq 1$.

$$V_{dc}I_{dc} = \frac{1}{4}V_{ac}I_{ac}\cos\theta = \frac{1}{4}mV_{dc}I_{ac}\cos\theta \quad (3)$$

This single-phase dc-ac MMC can be repurposed into the buck-boost CLMMC without changing SM stack arrangement, as shown in Fig. 2. This converter can be considered to be one of the base formats from which other topologies can be found a family of CLMMCs formed [26], [27]. Thus, this buck-boost CLMMC serves as an example in this and the following sections to explain the proposed analysis for the internal ac frequency.

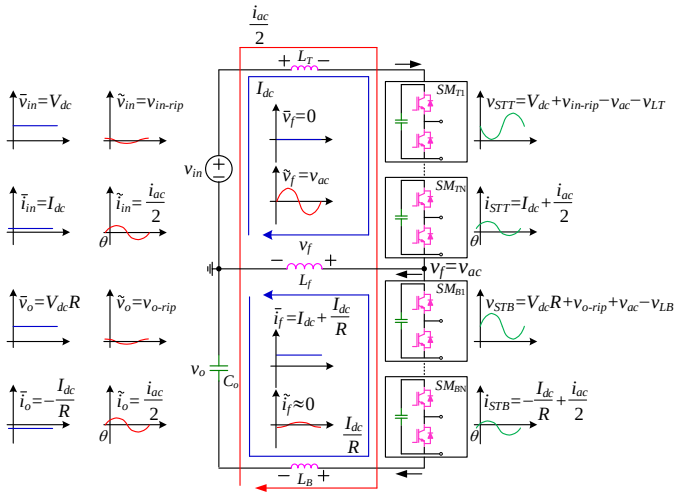


Fig. 2. Current loops in the buck-boost CLMMC (modified from [40]).

In this chain-link dc-dc format, v_{inT} is still the input dc source voltage, designated as v_{in}, but v_{inB} of Fig. 1 has become the output dc load voltage v_o in Fig. 2. A consequence of this change is that the dc current has divided into two loops (dc current is still shown with blue arrow) with different directions respect to the stack current references and they becomes differential mode components of the stack currents. The voltage step-ratio between the dc component values of v_o and v_{in} is defined as $R = \frac{\bar{v}_o}{\bar{v}_{in}}$ ($\bar{v}_{in} = V_{dc}, \bar{v}_o = V_{dc}R, \tilde{v}_{in} = v_{in-rip}, \tilde{v}_o = v_{o-rip}$). The ac load Z_{load} in Fig. 1 becomes an inductive filter L_f in Fig. 2 and its role is to supress ac current component in this path. This chain-link dc-dc converter relies on ac components in the stack voltages and also an ac current through the stacks to keep both SM stacks balanced during power transfer. This ac current must be driven by a net ac voltage present in the sum of the two stack voltages. In conventional dc-ac MMC conversion the sum of the two stack voltages is made equal to the dc link voltage but in this dc-dc format the sum has to support the dc link voltage plus provide an extra ac voltage to drive the ac current through the inductance of the internal path. This ac current is a common mode component of the stack currents (ac current is still shown with red arrow). The combination of the ac current and the ac components of the stack voltages provides an energy transfer in each ac cycle to offset the energy that is transferred to the stacks by the dc current. The arm inductor voltages $v_{LT}(t)$ and $v_{LB}(t)$ in this direct dc-dc conversion always act in the same direction due to the common ac current whereas they act in different directions in the dc-ac MMC. Because of the ac component in stack voltage, the voltage at middle point of the two stacks, v_f, is an ac voltage ($v_f(t) = v_{ac}(t) = V_{ac}\sin\omega t$), just as it was in the dc-ac MMC of Fig. 1. The term m is still useful in the dc-dc format for expressing the ratio between V_{ac} and V_{dc}.

Comparing the roles of the dc and ac current loops in Fig. 1 and Fig. 2, it is clear that the roles have been exchanged. In the dc-dc format of Fig. 2, the ac current, designated as $\frac{i_{ac}}{2}$, flows in an outer loop and is common to the top and bottom stacks, whereas there are different dc currents, I_{dc} and $\frac{I_{dc}}{R}$, flow through the two stacks with opposite directions, returning via filter L_f. The conditions imposed by the need for energy balance for top and bottom stacks in this dc-dc conversion are given in (4) and (5). The dc and ac components in this dc-dc conversion also need comply the relationship as (3) to maintain overall balance.

$$\int_0^T v_{STT}(t)i_{STT}(t)dt = \int_0^T \left[V_{dc} + v_{in-rip} - v_{ac}(t) - v_{LT}(t)\right]\left[I_{dc} + \frac{i_{ac}(t)}{2}\right]dt = 0 \quad (4)$$

$$\int_0^T v_{STB}(t)i_{STB}(t)dt = \int_0^T \left[V_{dc}R + v_{o-rip} + v_{ac}(t) - v_{LB}(t)\right]\left[-\frac{I_{dc}}{R} + \frac{i_{ac}(t)}{2}\right]dt = 0 \quad (5)$$

In the case of a dc-ac conversion, the frequency, magnitude and phase of the ac components of the stack voltages and currents are usually decided by the external utility grid and the power reference. For the chain-link dc-dc conversion, there is freedom to choose the magnitude, frequency and phase of ac components of the stack voltages to suit circuit design purposes. The magnitude, frequency and phase of the ac current can be set by the choice of the ac components of the stack voltages (the sum of the two stack voltages) acting on the internal passive network. This freedom of choice provides an opportunity, but also raises the challenge, to manage the component stresses and losses within the circuit. Proper design and operation of the chain-link dc-dc circuit requires detailed circuit analysis, as undertaken in next section.

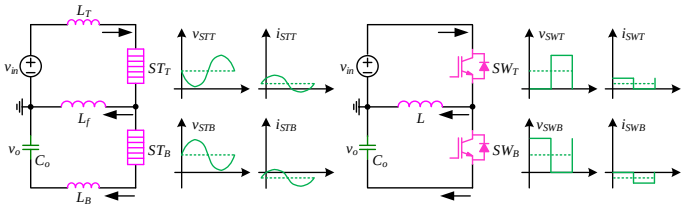
III. Equivalent Circuit and Internal AC Frequency

The approach is to create separate equivalent circuits to analyze the dc and ac components of Fig. 2 respectively, and these can be subsequently combined through superposition.

A. Equivalent Circuit of DC Components

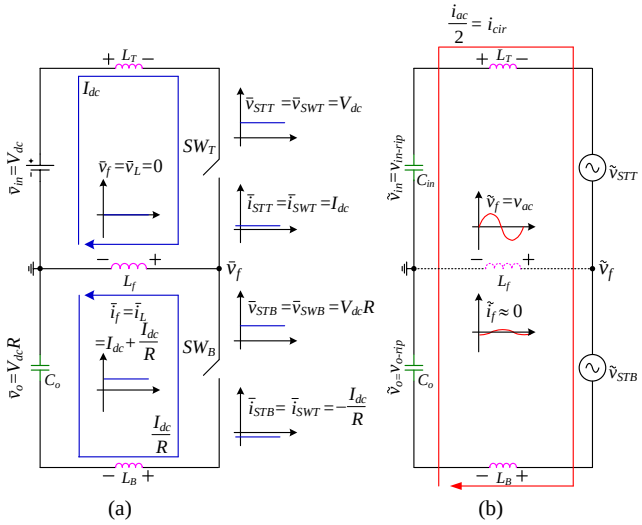
Considering the dc components of voltages and currents in Fig. 2, it can be found that the quantitative relationships between them are the same as they are in the classic buck-boost converter [41], [42]. This is illustrated further through the analysis and comparison between the buck-boost CLMMC and the classic switch-mode buck-boost converter in Fig. 3. The dc components of the stack voltages and currents ($\bar{v}_{STT} = V_{dc}, \bar{i}_{STT} = I_{dc}, \bar{v}_{STB} = V_{dc}R, \bar{i}_{STB} = -\frac{I_{dc}}{R}$) in Fig. 3 (a) are analogous to the average values of the switch voltages and currents ($\bar{v}_{SWT} = V_{dc}, \bar{i}_{SWT} = I_{dc}, \bar{v}_{SWB} = V_{dc}R, \bar{i}_{SWB} = -\frac{I_{dc}}{R}$) in Fig. 3 (b). Also, the dc components of the voltage and current of the reactor ($\bar{v}_f = 0, \bar{i}_f = I_{dc} + \frac{I_{dc}}{R}$) in Fig. 3(a) are also

analogous to the average values of the voltage and current of the inductor ($\bar{v}_L = 0, \bar{i}_L = I_{dc} + \frac{I_{dc}}{R}$) in Fig. 3(b).



(a) (b)

Fig. 3. Analysis and comparison of dc voltages and currents.
(a) Buck-boost CLMMC. (b) Classic switch-mode buck-boost converter.



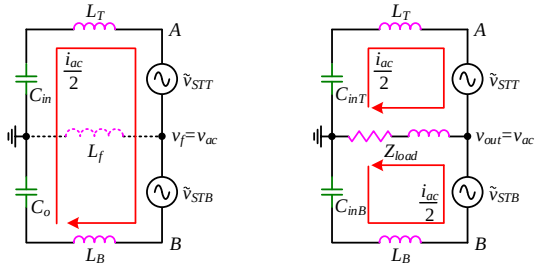
(a) (b)

Fig. 4. Equivalent circuit analysis of the buck-boost CLMMC.
(a) DC components. (b) AC components.

Thus, the equivalent circuit applying to dc components in Fig. 2 is shown in Fig. 4(a) with the specific quantitative expressions and illustrative waveforms at appropriate locations.

B. Equivalent Circuit of AC Components

Turning now to the ac components of Fig. 2, the equivalent circuit is shown in Fig. 4(b). It can be seen that there is no input ac voltage but the stacks act together and in sum they create an ac voltage that drives an ac current around a single loop comprising of the two arm inductors, L_T and L_B, and the input and output dc capacitor C_{in} and C_o.



(a) (b)

Fig. 5. Analysis and comparison of ac voltages and currents.
(a) Buck-boost CLMMC. (b) Single-phase dc-ac MMC.

This ac current analysis is illustrated in Fig. 5(a) and for comparison the paths in the single-phase dc-ac MMC are shown in Fig. 5(b). The top and bottom stack voltages in the dc-ac MMC also need to provide an extra ac voltage (besides the main ac voltage v_{ac}) to generate ac voltages at points *A* and *B* to drive the two ac current components through the arm inductors. These two ac currents flow with different directions when they go through their respective arm inductor and SM stack, so the required extra ac voltages for top stack and bottom are opposite and the sum of them should be 0 (*i.e.*, the ac voltage between point *A* and *B* is 0), which avoids creation of internal circulating current. However, the ac current in the case of this chain-link direct dc-dc conversion has to circulate within the circuit in order to keep the stack energies balanced, so the sum of the extra ac voltages of the top and bottom stack in this dc-dc conversion should not be 0 (*i.e.*, the ac voltage between point *A* and *B* is not 0).

The expression for these two stack voltages can be expressed in terms of the SM capacitor voltages and modulation ratios. The ac current, $\frac{i_{ac}}{2}$, that flows around the main loop is also referred to as the internal circulating current ($i_{cir} = \frac{i_{ac}}{2}$).

C. Internal AC Frequency with Consideration of SM Capacitance and SM Voltage Ripples

The energy stored in the top and bottom stacks, $e_{SMT,SMB}(t)$, is expressed in (6) as the sum of an average (dc) term, $\bar{e}_{SMT,SMB}$, and a ripple (ac) term, $\tilde{e}_{SMT,SMB}(t)$.

$$e_{SMT,SMB}(t) = \bar{e}_{SMT,SMB} + \tilde{e}_{SMT,SMB}(t)$$
$$= \frac{C_{SM}}{2N_{T,B}} v_{SMT,SMB}{}^2(t) = \frac{C_{SM}}{2N_{T,B}} \left[\bar{v}_{SMT,SMB} + \tilde{v}_{SMT,SMB}(t)\right]^2$$
$$\approx \frac{C_{SM}}{2N_{T,B}} \bar{v}_{SMT,SMB}{}^2 + \frac{C_{SM}}{N_{T,B}} \bar{v}_{SMT,SMB} \tilde{v}_{SMT,SMB}(t) \quad (6)$$

where $v_{SMT,SMB}(t)$ is sum of voltages in the $N_{T,B}$ capacitors of top or bottom stack and each capacitor has a value of C_{SM}. This voltage can be divided in dc components $\bar{v}_{SMT,SMB}$ and ac components, $\tilde{v}_{SMT,SMB}(t)$. The ac component is the sum of ripples appearing on each SM capacitor, and it is commonly less than 10% of the sum of nominal dc voltage on each SM capacitor [43], [44]. Thus, when examining the squares of the terms, $\tilde{v}_{SMT,SMB}(t)^2$ is typically about 1% of the value of $\bar{v}_{SMT,SMB}{}^2$ and it can be regarded as negligible in equation (6).

The ac components of the sum of SM capacitor energy, $\tilde{e}_{SMT,SMB}(t)$ are related to the instantaneous power exchange of the stack during the circuit operation, and they can be expressed as (7) and (8).

$$\tilde{e}_{SMT}(t) = \int_0^t \left[V_{dc} + v_{in-rip} - v_{ac}(t) - v_{LT}(t)\right] \left[I_{dc} + \frac{i_{ac}(t)}{2}\right] dt \quad (7)$$

$$\tilde{e}_{SMB}(t) = \int_0^t \left[V_{dc}R + v_{o-rip} + v_{ac}(t) - v_{LB}(t)\right] \left[-\frac{I_{dc}}{R} + \frac{i_{ac}(t)}{2}\right] dt \quad (8)$$

Substituting (7) and (8) into (6), it yields the ac components of the sum of SM capacitor voltage, $\tilde{v}_{SMT}(t)$ and $\tilde{v}_{SMB}(t)$, as noted in (9) and (10) where the small energy deviation within the passive network has been neglected.

$$\tilde{v}_{SMT}(t) = \frac{N_T}{C_{SM}\bar{v}_{SMT}} \tilde{e}_{SMT}(t) = \frac{N_T V_{dc} I_{dc}}{2\omega C_{SM} \bar{v}_{SMT}}$$
$$\cdot \left(\frac{4}{m} tan\,\theta\, sin\,\omega t + \frac{2m^2 - 4}{m} cos\,\omega t + sin\,2\omega t + tan\,\theta\, cos\,2\omega t\right) \quad (9)$$

$$\tilde{v}_{SMB}(t) = \frac{N_B}{C_{SM}\bar{v}_{SMB}} \tilde{e}_{SMB}(t) = \frac{N_B V_{dc} I_{dc}}{2\omega C_{SM} \bar{v}_{SMB}}$$
$$\cdot \left(\frac{4R}{m} tan\,\theta\, sin\,\omega t + \frac{2m^2 - 4R}{mR} cos\,\omega t - sin\,2\omega t - tan\,\theta\, cos\,2\omega t\right) \quad (10)$$

The dc components of the sums of the SM capacitor voltages in the top and bottom stacks, $\bar{v}_{SMT,SMB}$, should be sufficient to match the externally imposed dc voltages (V_{dc} in the top loop and $V_{dc}R$ in the bottom loop) and through modulation of the stack create the required V_{ac} as shown in (11) and (12). Terms δ_T and δ_B are defined as the redundancy ratio for the dc components of stack voltages ($\delta_T \leq 1, \delta_B \leq 1$).

$$\delta_T \bar{v}_{SMT} = V_{dc} + V_{ac} = (1+m)V_{dc} \tag{11}$$

$$\delta_B \bar{v}_{SMB} = V_{dc}R + V_{ac} = (R+m)V_{dc} \tag{12}$$

The ratio between V_{dc} and $\bar{v}_{SMT}$ and the ratio between $V_{dc}R$ and $\bar{v}_{SMB}$ are defined as the SM stack dc modulation m_{dcT} and m_{dcB}, shown in (13). It is worth noting here that m is the ratio between V_{ac} and V_{dc}, which can be seen as the SM stack ac voltage modulation.

$$m_{dcT} = \frac{V_{dc}}{\bar{v}_{SMT}} = \frac{\delta_T}{1+m}, \quad m_{dcB} = \frac{V_{dc}R}{\bar{v}_{SMB}} = \frac{\delta_B R}{R+m} \tag{13}$$

Thus, the stack voltages can be expressed in (14) and (15) by SM capacitor voltages and modulation ratios. The sum of their ac components, $\tilde{v}_{sum}(t)$, is given in (16), and it can be observed that the main ac voltages, $-v_{ac}(t)$ and $v_{ac}(t)$ for top stack and bottom stack have been offset in the sum voltage of (16), and the extra ac voltages drive the internal ac current through the arm inductors. Considering the arm inductance are usually small compared to the phase filter, these extra ac voltages would be normally much smaller than the main ac voltages for both stacks in the circuit operation.

$$v_{STT}(t) = (m_{dcT} - m_{dcT} m \sin\omega t)[\bar{v}_{SMT} + \tilde{v}_{SMT}(t)] \tag{14}$$

$$v_{STB}(t) = \left(m_{dcB} + \frac{m_{dcB}}{R} m \sin\omega t\right)[\bar{v}_{SMB} + \tilde{v}_{SMB}(t)] \tag{15}$$

$$\tilde{v}_{sum}(t) = \tilde{v}_{STT}(t) + \tilde{v}_{STB}(t) = -v_{ac}(t) + A + v_{ac}(t) + B = A + B \tag{16}$$

Where

$$A = (m_{dcT} - m_{dcT} m \sin\omega t)\tilde{v}_{SMT}(t), B = \left(m_{dcB} + \frac{m_{dcB}}{R} m \sin\omega t\right)\tilde{v}_{SMB}(t)$$

The relationship between this ac voltage sum and the internal circulating ac current shown in Fig. 4(b) is provided in (17), and the magnitude of this current is given in (18), where C_{DC} is the equivalent dc-link capacitance ($C_{DC} = \frac{C_{in}C_o}{C_{in}+C_o}$).

$$\vec{\imath}_{cir} = \frac{1}{2}\vec{\imath}_{ac} = \frac{-j\omega C_{DC}}{1-\omega^2(L_T+L_B)C_{DC}}\vec{\tilde{v}}_{sum} \tag{17}$$

$$I_{cir} = \frac{1}{2}I_{ac} = \left|\frac{-j\omega C_{DC}}{1-\omega^2(L_T+L_B)C_{DC}}\right| \cdot max(A+B) \tag{18}$$

Substituting the results of (9) and (10) into (16) and (18), the general expression for this circulating ac current magnitude can be found as shown in Appendix (A–1). Here, analysis specific to the case of unity ratio conversion without voltage redundancy ($\bar{v}_{in} = \bar{v}_o = V_{dc}, N_{T,B} = N_{arm}, L_{T,B} = L_{arm}, m_{dcT,dcB} = \frac{1}{1+m}$) is shown in (19) as an example.

$$I_{cir} = \frac{1}{2}I_{ac} = \left|\frac{-jC_{DC}N_{arm}I_{dc}}{2C_{SM}(1-2\omega^2 L_{arm}C_{DC})(1+m)^2}\right| \cdot max\left(\frac{m^2+8}{m} tan\theta \sin\omega t + \frac{3m^2-8}{m} cos\,\omega t + m\cos 3\omega t - m\tan\theta \sin 3\omega t\right) \tag{19}$$

Considering the effect of harmonic components is negligible, (19) can be simplified as (20), and this term needs to satisfy the energy balancing condition in (3). Thus, the required internal ac frequency can be determined according to (21).

$$I_{cir} = \frac{1}{2}I_{ac} = \frac{N_{arm}I_{dc}C_{DC}}{2C_{SM}(2\omega^2 L_{arm}C_{DC}-1)(1+m)^2 m} \cdot C \tag{20}$$

$$f = \frac{\omega}{2\pi} = \frac{1}{2\pi}\sqrt{\frac{1}{2L_{arm}C_{DC}} + \frac{N_{arm}\cos\theta}{8L_{arm}C_{SM}(1+m)^2} \cdot C} \tag{21}$$

Where

$$C = \sqrt{(tan^2\theta+9)m^4 + (16\tan^2\theta - 48)m^2 + 64\tan^2\theta + 64}.$$

The expression (20) has a minimum value which for the case $\theta = 0$ is expressed in (22) in terms of the passive component values and the voltage modulation index. This minimum value occurs at the frequency given in (23).

$$I_{cir-min} = \frac{1}{2}I_{ac-min} = \frac{N_{arm}I_{dc}C_{DC}(8-3m^2)}{2C_{SM}(2\omega^2 L_{arm}C_{DC}-1)(1+m)^2 m} \tag{22}$$

$$f = \frac{1}{2\pi}\sqrt{\frac{1}{2L_{arm}C_{DC}} + \frac{N_{arm}(8-3m^2)}{8L_{arm}C_{SM}(1+m)^2}} \tag{23}$$

This frequency guarantees that there is no phase difference between the internal ac current and the main ac voltage of bottom stack and that there is 180° phase difference between the internal ac current and the main ac voltage of top stack, which means they only generate active power for stack energy balance, but it is also worth noting here there would be still some trivial reactive power circulating in the circuit which is caused by the internal ac current and the small extra ac voltages for both stacks which have to exist to generate the internal ac current as the analysis in (16) and (17).

With the same method for circuit analysis, the relevant results of the minimum current magnitude and associated ac frequency for the case of non-unity ratio conversion ($\bar{v}_{in} = \bar{v}_o R, N_{T,B} = N_{arm}, L_{T,B} = L_{arm}, m_{dcT} = \frac{1}{1+m}, m_{dcB} = \frac{R}{R+m}$) are also derived and provided in Appendix (A–2) and (A–3).

During the circuit design process for this buck-boost CLMMC, the total number of SM in each stack was determined by the maximum voltage required from the stack during operation and the voltage rating (adjusted by a de-rating factor) of the power devices selected. The choice of voltage rating for the devices of the SM is a trade-off between waveform quality and total costs as the device rating is varied, as it is in the classic dc-ac MMC [45], [46]. The capacitors are sized in accordance with the allowed voltage deviation of the SM and the deviation of the total stack energy for the worst-case operating condition [43], [44]. The arm inductance and dc link capacitance should be chosen with reference to (23) or (A–3) such that the required ac frequency falls into the medium frequency range (roughly 300 Hz–1000 Hz) because this gives a good trade-off between the device power losses and system volume [26].

During the operation (once the circuit parameters have been decided), the modulation index should be kept relatively high and the ac frequency needs to respect the specific result in (23) or (A–3) in order to operate at the minimum ac current stress and avoid excessive reactive power circulation. A poor choice of frequency could result in a higher magnitude of ac current than is necessary for energy balancing and it would also lead to undesirable and excessive reactive power flowing around the loop which in turn causes extra power losses and a decrease in efficiency.

A control structure for this buck-boost CLMMC that can regulate both dc and ac components is presented in Fig. 6 in a classic combination of outer voltage control loops setting references for inner current control loops. Considering the circuit model of the CLMMCs can be readily linearized [47], [48], the relatively straightforward linear controllers were

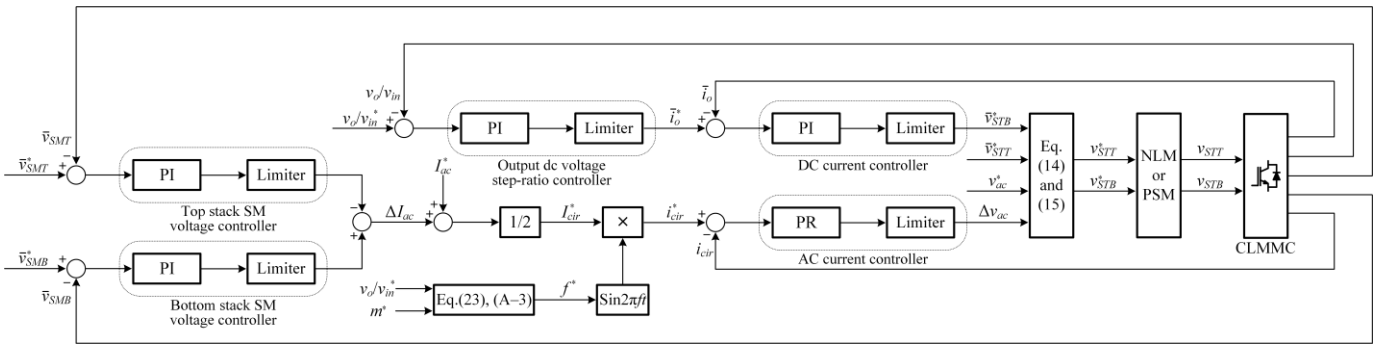


Fig. 6. Control structure for the buck-boost CLMMC.

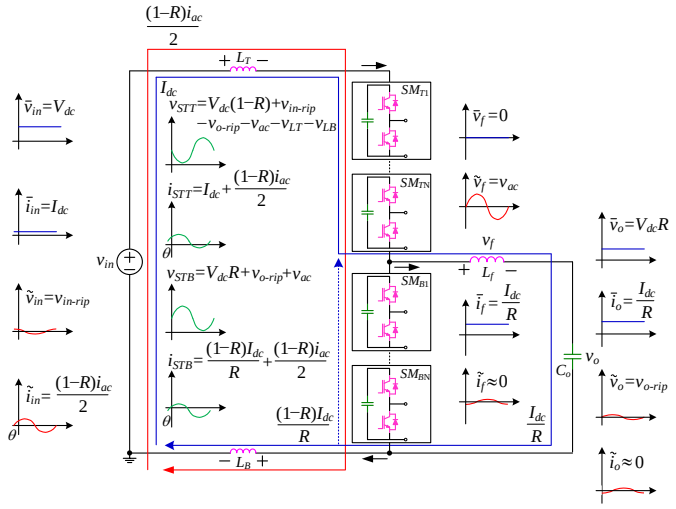


Fig. 7. Current loops in the buck CLMMC.

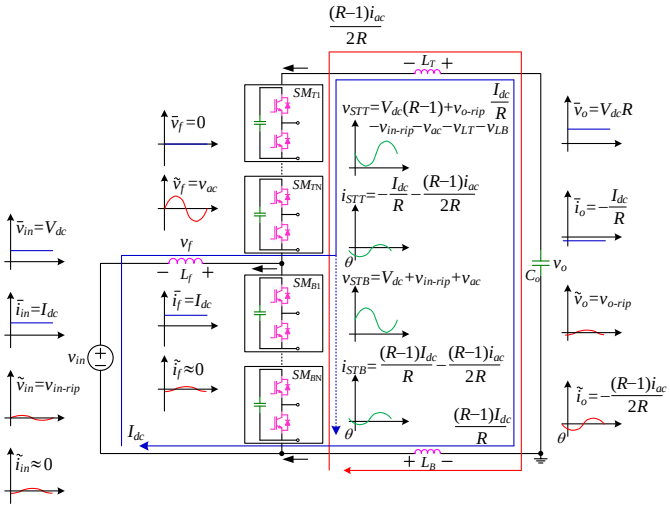
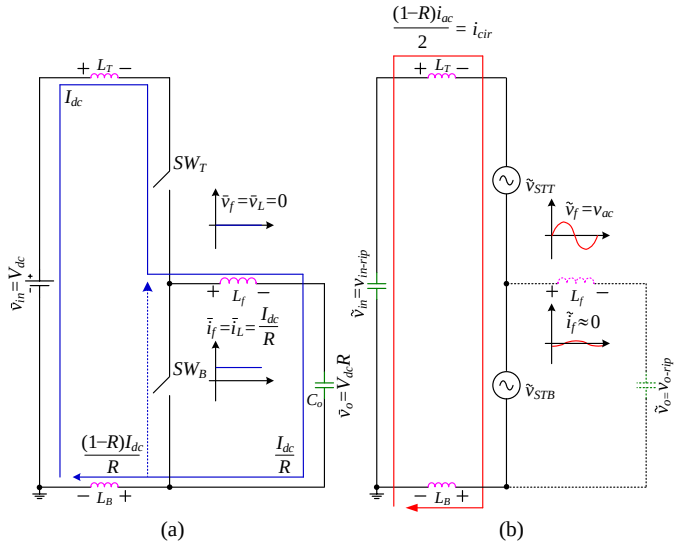
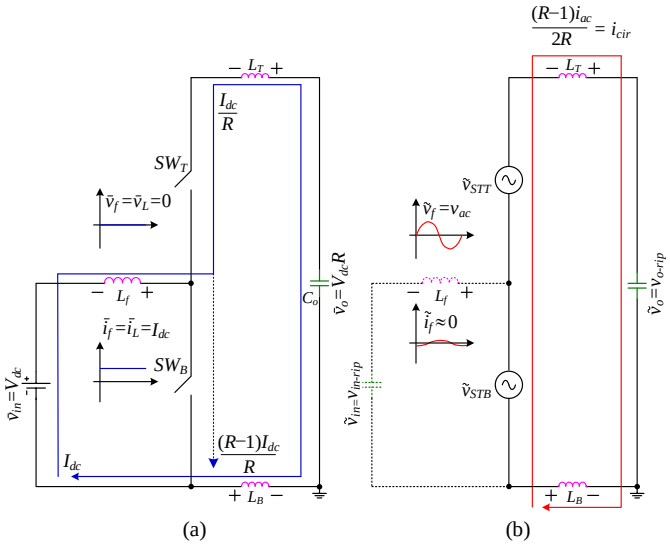


Fig. 9. Current loops in the boost CLMMC.



(a) (b)

Fig. 8. Equivalent circuit analysis of the buck CLMMC.
(a) DC components. (b) AC components.



(a) (b)

Fig. 10. Equivalent circuit analysis of the boost CLMMC.
(a) DC components. (b) AC components.

chosen as a simple and effective example for regulation: a proportional–integral (PI) controller is used to regulate the dc current and proportional-resonant (PR) controller for the ac current. Other more sophisticated controllers such as sliding-mode or passivity-based control might bring some advantage to achieve whole system stability when multiple CLMMCs are interconnected with series or parallel relationship [49] but PI and PR were sufficient to illustrate operation and ensure stability of a single CLMMC. The output voltage control loop, itself a PI controller, set the reference for the dc current. The regulation of total voltages of the top and bottom stacks, again PI controllers, create adjustments to ac circulating current magnitude. The required SM stack voltages are calculated from the various controller terms using (14) and (15) and the switching signals for the SMs can be created by a modulator using either classic nearest level modulation (NLM) [22] or

phase shift modulation (PSM) [50] with sorting and selection processes to ensure each individual SM capacitor voltage well-balanced within their own stack.

IV. Analysis of Other Base Formats of CLMMCs

The buck-boost CLMMC has served as an illustrative example in Section II and III to analyse the internal ac current and its associated frequency in CLMMCs. The analytical method can be extended and applied to other base formats of CLMMCs [26], [27], such as the buck CLMMC and boost CLMMC.

If the input dc source is connected across the pair of stacks rather than across the top stack only, as shown in Fig. 7, the converter becomes a buck CLMMC and its equivalent circuits are given in Fig. 8. The dc circuit is analogous to a standard switch-mode buck converter [51], [52], and the ac circuit is comprised of two controllable ac voltage sources, two arm inductors and the input dc capacitor. The minimum current magnitude and the associated ac frequency can be derived by the same step-by-step process as presented in Section III, and the general analytical result for the internal ac current magnitude is provided as (A–4) in Appendix.

If the input dc source is connected across the bottom stack and the output capacitor is connected across the pair of stacks, as shown in Fig. 9, the circuit becomes a boost CLMMC. The equivalent dc and ac circuits are given in Fig. 10, where the dc circuit is analogous to a standard switch-mode boost converter [53], and the ac circuit is comprised of two ac voltage sources, two arm inductors and the output dc capacitor. Based on the analytical method in Section III, the result for its current magnitude is derived and given in Appendix (A–5).

Summarizing the circuit analysis and calculation in Section III and IV, the equivalent circuits and theoretical results for all the base format of CLMMCs are given here in Table I.

Table I. Analysis summary for all the base formats of CLMMCs

Formats	Current Loops	DC and AC Circuits	Internal AC Current
Buck-boost	Fig. 2	Fig. 4	(A–1)
Buck	Fig. 7	Fig. 8	(A–4)
Boost	Fig. 9	Fig. 10	(A–5)

V. Simulation Verification

After the detailed circuit analysis in Section I to III, this section presents a set of simulations to verify the theoretical analysis and results on internal ac frequency of the CLMMC in medium-voltage examples.

It is based on the buck-boost CLMMC with the parameters recorded in Table II. The dc voltage and operating power in simulation examples are chosen at around 11 kV and 3 MW to be representative of the range of voltage rating and power rating used in various practical medium-voltage dc projects with different utility standards around the world [6]. The input and output voltages and the available power device rating lead to a choice of 9 SMs for each stack. A SM capacitance of 1.0 mF was chosen to achieve a capacitor voltage variation of less than 10%. In the simulation itself the 18 SM capacitance were given 10% variation to reflect manufacturing tolerance. The value of arm inductance and dc link capacitance chose at 150 μH and 300 μF respectively to ensure that the required ac frequency falls into the middle frequency range and the required extra ac voltage for both stacks are very small. The modulation index varied according to different voltage step-ratio in the operation, but it kept high value choice for each conversion case.

Table II. Simulation parameters of the buck-boost CLMMC

Symbol	Description	Value
P	Operation Power	3 MW
v_{in}	Input DC Voltage	11 kV
v_o	Output DC Voltage	5.5 kV–11 kV
R	Voltage Step-ratio	0.5:1–1:1
L_f	Filter Inductance	5 mH
C_{DC}	DC Link Capacitance	300 μF
L_{arm}	Arm Inductance	150 μH with ±5% variation
N_{arm}	SM Number per Stack	9
S	SM Power Switches	ABB 5SNA1500E330305
C_{SM}	SM Capacitance	1.0 mF with ±10% variation
δ_{SM}	SM Capacitor Voltage Tolerance	10%

A unity ratio conversion ($R = v_o/v_{in} = 1:1$) was demonstrated as the first example. The modulation index was chosen to be 0.8 in this case. The ac frequency was set according to the analysis in (23) to achieve the minimum ac current magnitude and avoid excessive reactive power circulation. Given the circuit parameters in Table II, a value of 800 Hz was found. The first result to be discussed is the output dc voltage v_o shown in Fig. 11 and this confirms that the step-ratio is 1:1. The stack voltages in the same figure show that the top stack voltage v_{STT} and bottom stack voltage v_{STB} contain the same dc term as each other but have ac components that are phase-shifted by approximately 180°. The input dc current $\bar{\imath}_{in}$ in Fig. 12 confirms that operation is at 3 MW and the two stack currents, in the same figure, have the same ac component with opposite polarity dc components. It can be seen that the phase difference between voltage and current for top stack is approximately 180° and the phase difference for bottom stack is approximately 0°. These observations are in agreement with the theoretical analysis in Section III and verify that there is nearly no reactive power associated with the ac energy balancing loop and that the ac components have been almost fully utilized for stack energy balancing. The magnitude of the ac current observed in Fig. 12 is about 696 A which agrees reasonably well with the theoretical value of 689 A obtained from (22) and this demonstrates that i_{STT} and i_{STB} are both almost at their minimum values in this case. Fig. 13 and Fig. 14 show individual SM capacitor voltages for the top and bottom stacks respectively. The voltage deviations are well regulated and remain within 10% of the nominal SM voltage of 2.2 kV, and the sum of the dc components of SM capacitor voltages in each stack is 19.8 kV, which nearly matches the maximum value of the stack voltage in Fig. 11.

A non-unity ratio conversion ($R = v_o/v_{in} = 0.83:1$) was chosen for the next example to verify that the proposed analysis for internal ac frequency is generally applicable for various

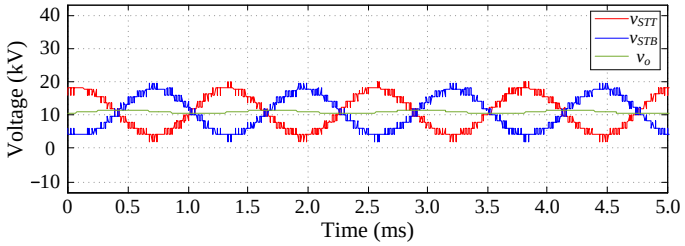


Fig. 11. Stack voltages v_{STT}, v_{STB} and output dc voltage v_o in unity ratio conversion.

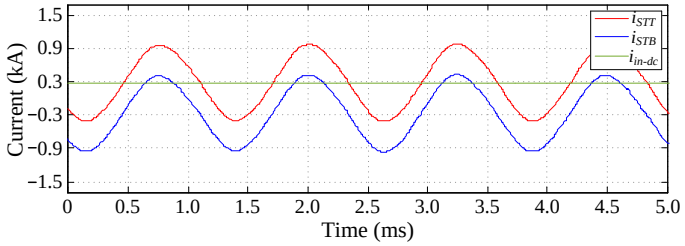


Fig. 12. Stack currents i_{STT}, i_{STB} and input dc current i_{in-dc} in unity ratio conversion.

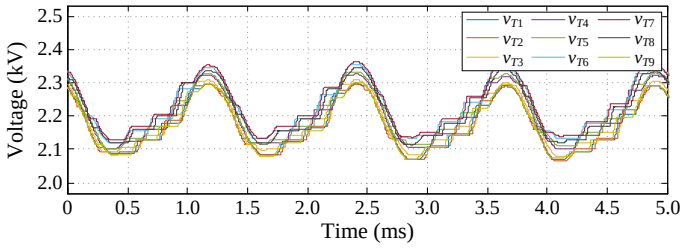


Fig. 13. SM voltages in top stack in unity ratio conversion.

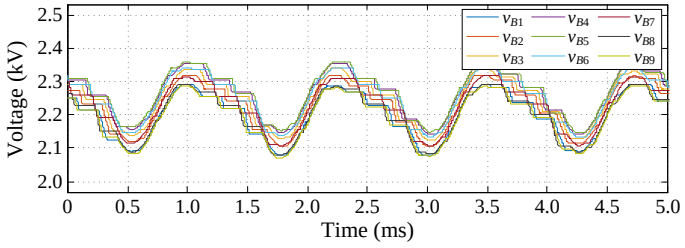


Fig. 14. SM voltages in bottom stack in unity ratio conversion.

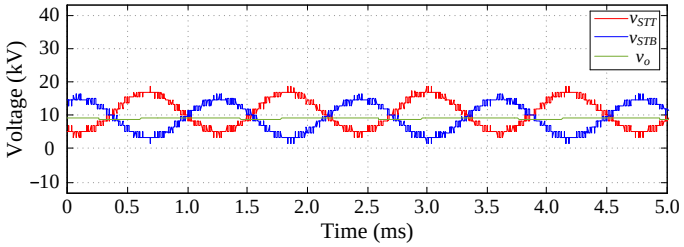


Fig. 15. Stack voltages v_{STT}, v_{STB} and output dc voltage v_o in non-unity ratio conversion.

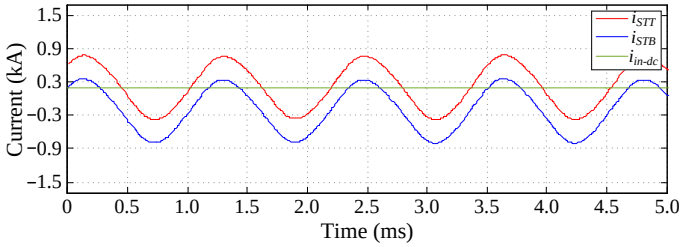


Fig. 16. Stack currents i_{STT}, i_{STB} and input dc current i_{in-dc} in non-unity ratio conversion.

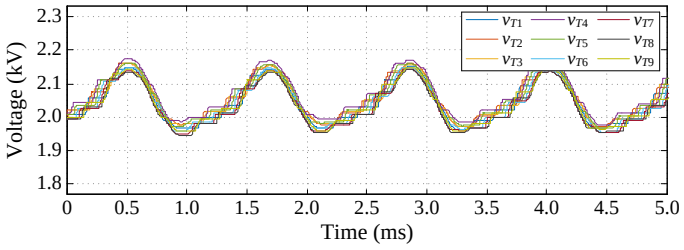


Fig. 17. SM voltages in top stack in non-unity ratio conversion.

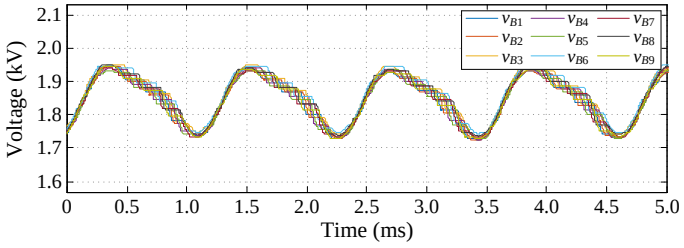


Fig. 18. SM voltages in bottom stack in non-unity ratio conversion.

step-ratio cases. Since the dc component of the bottom stack voltage is lower than the unity ratio conversion case, the modulation index was adjusted to 0.66, but it is still a high value choice for this step-down conversion case. Using the analysis in Appendix (A–3), the ac frequency was set at 850 Hz. The output dc voltage and input dc current in Fig. 15 and Fig. 16 confirm that the step-ratio has been changed to 0.83:1 and the power throughput is 2.0 MW. Moreover, Fig. 15 and Fig. 16 show that the ac components of stack voltages are phase-shifted by nearly half cycle and the stack ac currents are equal for the two stacks, but the dc components of stack voltages and currents are different because of the non-unity conversion ratio. The values of dc and ac components in Fig. 15 and Fig. 16 agree with the theoretical analysis in Fig. 3–Fig. 5, and there is also almost no reactive power in the ac energy balancing loop. The ac current is about 579 A, and which is close to the theoretical minimum value of 568 A predicted by the analysis in Appendix (A–2). Fig. 17 and Fig. 18 show the SM voltages are balanced around an average value of 2.05 kV in the top stack but around a value of 1.85 kV in the bottom stack, as expected for a step-down ratio of 0.83:1. The sum of dc components in Fig. 17 and Fig. 18 also approximately matches the maximum value of their respective stack voltage in Fig. 15.

The third simulation tests the boost format CLMMC with the same converter parameters in Table II for a step-up voltage conversion ($v_{in} = 11\ kV, v_o = 22\ kV, R = 2{:}1$) at 3 MW. Firstly, the output dc voltage v_o in Fig. 19 demonstrates the step-up ratio is 2:1 and the input dc current in Fig. 20 verifies the operation power is 3 MW. From Fig. 19 and Fig. 20, it can be observed that the phase difference between voltage and current for top stack is approximately 0° and the phase difference for bottom stack is approximately 180° as expected from Fig. 9 and Fig. 10, which is different with the results in Fig. 11 and Fig. 12 but there is also nearly no reactive power circulating in the ac

energy loop. The dc component of the stack current is about -136 A for the top stack and 136 A for the bottom stack, and the amplitude of the internal ac current for both stacks is around 349 A which also closely matches the theoretical minimum result of 344 A from (A–5). The results shown in Fig. 19 and Fig. 20 validate the presented analysis for internal ac frequency also applicable for other base formats of CLMMCs.

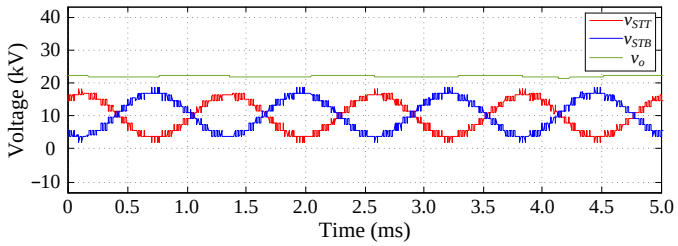


Fig. 19. Stack voltages v_{STT}, v_{STB} and output dc voltage v_o in boost CLMMC.

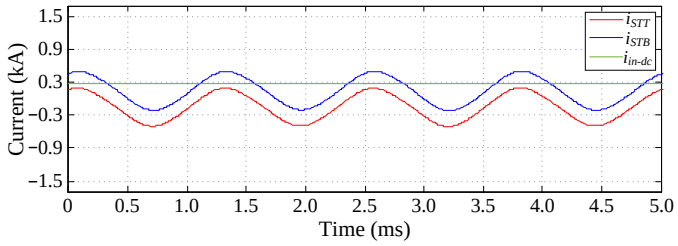


Fig. 20. Stack currents i_{STT}, i_{STB} and input dc current i_{in-dc} in boost CLMMC.

VI. Experimental Verification

To further validate the theoretical analysis of the internal ac frequency and to provide reassurance that the simulations included all the relevant features of the circuit, a down-scaled prototype of the buck-boost CLMMC was designed and built as shown in Fig. 21 with the circuit parameters listed in Table III.

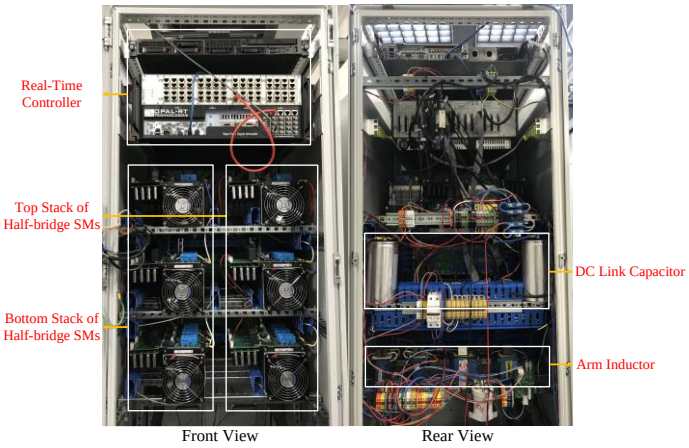


Fig. 21. Down-scaled laboratory prototype of the buck-boost CLMMC.

The scaling factor for the laboratory-scale prototype was considered so that the key parameters correspond to those in the full-scale simulation examples, notably, maintaining 9 SM per stack and similar normalised stored energy (≈14 kJ/MVA) in the SM capacitors. This results in the required ac frequency value for which the internal ac current is a minimum being 800 Hz for unity ratio operation ($R = v_o/v_{in} = 1{:}1$) which corresponds well with the case study in Fig. 11 to Fig. 14. The stack voltages and stack currents recorded from the experiment are presented in Fig. 22 for the case of $R = 1{:}1$. There is some distortion observed in the current and this is attributed to the on-state voltage drops of IGBTs which are disproportionately large in the laboratory experiment because the IGBTs have been over-sized for robustness and safety in the laboratory. In a commercial medium-voltage or high-voltage design, the on-state voltage drop would be very small compared to the system voltage and the current distortion would be negligible. The voltages of the top and bottom stacks in Fig. 22 confirm that (i) their dc components are consistent with conversion of 150 V input to 150 V output and (ii) their ac components are phased-shifted by approximately 180° with respect to each other. The two stack currents confirm that (i) the dc components have opposite polarity with operation at about 1 kW and (ii) the ac components of the two stacks are equal. Furthermore, the phase-displacement between voltage and current for the top stack is 191.7° and the phase-displacement for the bottom stack is 11.7° thereby confirming that there is little reactive power circulation within the converter. In general, the values of the dc and ac components of the stack voltages and currents agree with the analysis in Section III, notably, that the ac current magnitude is approximately 17.5 A in the experiment against a prediction from the theory (22) that a minimum value would be 16.7 A achieved at the selected frequency. Fig. 23 and Fig. 24 show that the top stack and bottom stack SM capacitor voltages are all well- balanced in this unity ratio conversion and the sum of their dc components also approximately match the maximum value of their respective stack voltage in Fig. 22.

The experimental results in Fig. 22–Fig. 24 verify the theoretical derivation developed from the equivalent circuits of Fig. 4 and the simulation results in Fig. 11–Fig. 14.

Table III. Experimental parameters of the buck-boost CLMMC.

Symbol	Description	Value
P	Operation Power	1 kW
v_{in}	Input DC Voltage	150 V
v_o	Output DC Voltage	75 V–150 V
R	Voltage Step-ratio	0.5:1–1:1
L_f	Filter Inductance	5 mH
C_{DC}	DC Link Capacitance	300 μF
L_{arm}	Arm Inductance	150 μH with ±5% variation
N_{arm}	SM Number per Stack	9
S	SM Power Switches	Mitsubishi CM300DX-24S
C_{SM}	SM Capacitance	1.0 mF with ±10% variation
δ_{SM}	SM Capacitor Voltage Tolerance	10%

A non-unity ratio conversion was also tested experimentally with $R = v_o/v_{in} = 0.83{:}1$ chosen to correspond to that used in Fig. 15 to Fig. 18. To accommodate this ratio, the ac frequency was changed to 850 Hz which is the value the analysis in Appendix (A–3) predicts will give minimum ac current magnitude and avoids excess reactive power circulation and it is the same value as used in Section V for this conversion ratio. The same load was used as that in tests at unity ratio conversion, so the power throughput is reduced. The experimental results

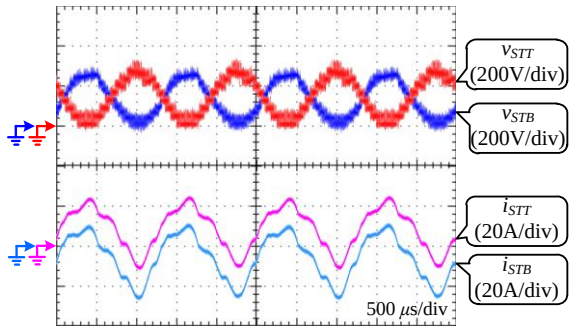


Fig. 22. Stack voltages and stack currents in unity ratio conversion.

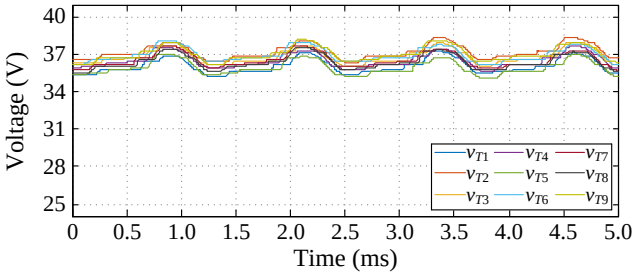


Fig. 23. SM capacitor voltages in top stack in unity ratio conversion.

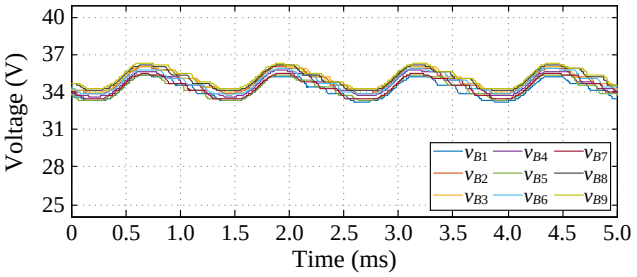


Fig. 24. SM capacitor voltages in top stack in unity ratio conversion.

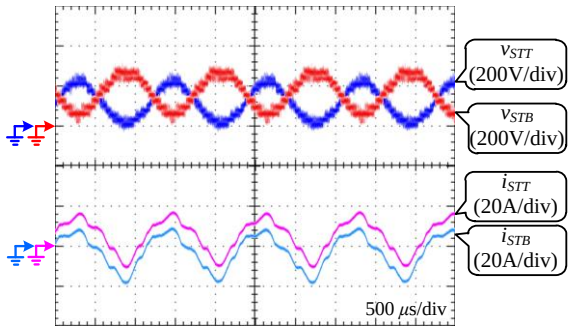


Fig. 25. Stack voltages and stack currents in non-unity ratio conversion.

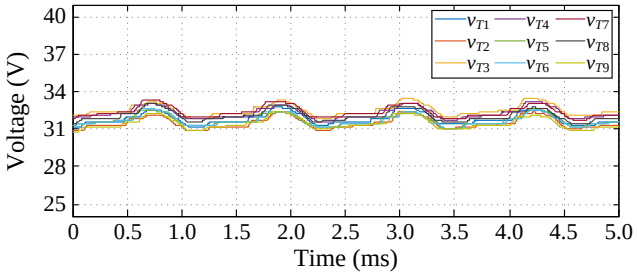


Fig. 26. SM capacitor voltages in top stack in non-unity ratio conversion.

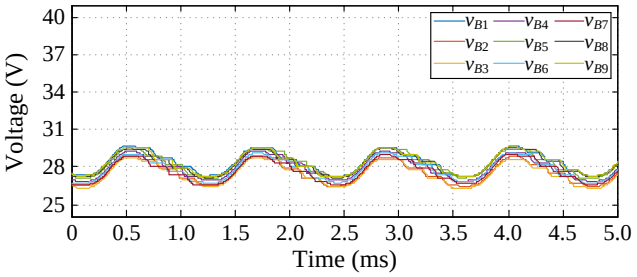


Fig. 27.SM capacitor voltages in bottom stack in non-unity ratio conversion.

for this step-down conversion are shown in Fig. 25–Fig. 27. In Fig. 25, the difference in the dc components of the two stack voltages confirm the step-ratio is 0.83:1, and the dc components of the two stack currents demonstrate that the operation power is at about 0.65 kW. As in the previous case, the ac components of stack voltages are phase-shifted by nearly half cycle and the ac currents are almost equal for the two stacks. The phase angles of the currents with respect to the voltages indicates very little reactive power in the circulation. Operation at 850 Hz was expected to minimize the ac current magnitude to a value of 13.2 A calculated from Appendix (A–2) and the observed value is in reasonable agreement at about 14 A. Fig. 26 and Fig. 27 present the SM capacitor voltages in this non-unity ratio conversion case and they are seen to be well-balanced within each stack. Compared with the unity ratio conversion case in Fig. 23 and Fig. 24, the dc values in top and bottom stacks have dropped to around 32 V and 28 V respectively since the output dc voltage in this step-down conversion is smaller and the ac modulation index had been decreased from 0.8 to 0.66 as well.

The experimental results in Fig. 25–Fig. 27 correspond well with the simulation results in Fig. 15–Fig. 18 and verify that the presented analysis is applicable for non-unity ratio conversion.

A further experimental test was conducted to validate the control scheme in Fig. 6 using a step-change from the non-unity conversion ($R = v_o/v_{in} = 0.83:1$) to the unity conversion ($R = v_o/v_{in} = 1:1$) and the results shown in Fig. 28.

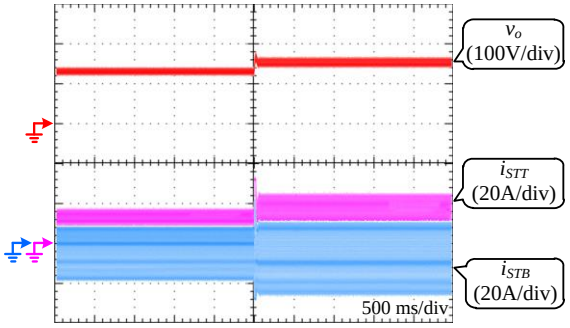


Fig. 28. Step-change test from non-unity conversion to unity conversion.

The input dc voltage was kept constant at 150 V and the output dc voltage was set at 125 V initially for the non-unity conversion and increased to 150 V halfway through the observation period for the unity conversion. In the non-unity conversion period, it can be seen that the magnitude of the bottom stack current is about 1 A higher than that of the top stack, which is consistent with the result in Fig. 25 where the step-down voltage conversion leads to a larger dc current component in the bottom stack. After the change of the step-ratio, the output dc voltage rises to 150 V and holds steady at

this value. Also, the magnitudes of the two stack currents become equal at a value of about 24 A, consistent with the result shown in Fig. 22 for the unity conversion. The dc and ac values of the stack currents during the non-unity period and unity period are different, but they all match the theory and are close to the minimum magnitude values observed in the steady operation results in Fig. 22 and Fig. 25.

Lastly, a more general verification of the internal ac current magnitude at the selected frequency in steady-state operation were conducted. The converter was tested for a range of conversion ratios at $R = 0.5{:}1$, $R = 0.67{:}1$, $R = 0.83{:}1$ and $R = 1{:}1$ with the internal ac frequency adjusted to the values of 1025 Hz, 925 Hz, 850 Hz and 800 Hz respectively in accordance with the analytical results in (23) and (A–3).

For the first test, the input dc voltage was varied from 50 V to 250 V in steps of 50 V and the step-ratio value keeps constant in the four respective tests. The observed output voltage plotted in Fig. 29 is seen to vary linearly with the input voltage for all the step-ratio cases and the individual results agree very well with the theoretical values. For the second test, the input voltage was then held at 150 V with the four different step-ratios and the load was varied from 0.25 kW, 0.5 kW 0.75 kW to 1.0 kW for each step-ratio case. The ac current magnitude in the experiments are recoded in Fig. 30 and the individual results show very close agreement to the respective theoretical minimum values from (22) and (A–2).

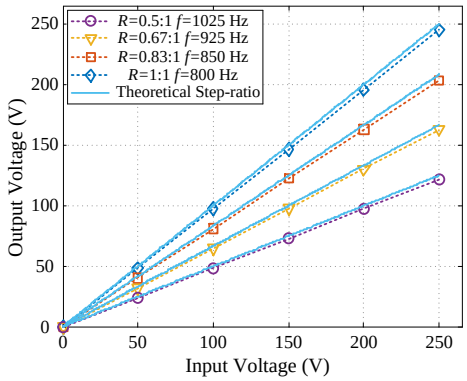


Fig. 29. Output voltage in the full-range operation test.

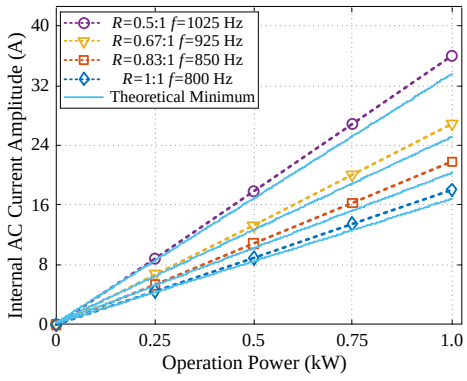


Fig. 30. Internal ac current magnitude in the full-range operation test.

The experimental results in Fig. 29 and Fig. 30 demonstrate the general validity of the presented analysis on internal ac frequency to minimize the ac current magnitude and avoid excess reactive power circulation.

Overall, the experiment testing in this section closely match the theoretical study in Section III and simulation results in Section IV. They confirm that the mathematical calculation in Section III and simulation model in Section IV represents all the key features pertinent to this analysis. By extension, the simulation results in Fig. 19 and Fig. 20 can be also seen as realistic and therefore used to confirm the analysis Section IV for other base formats of CLMMCs.

VII. Conclusion

This paper presented circuit analysis and investigation of the internal ac frequency for chain-link modular multilevel dc-dc converters (CLMMCs). The analysis facilitates the minimization of internal ac current stresses and reactive power circulation within the converter and can lead to an enhanced circuit design and better operation. For illustration, the analysis was applied to one of the base formats, the buck-boost CLMMC as an example and comparisons are drawn between the roles of the dc and ac current components in the CLMMC and the standard dc-ac MMC. Equivalent circuits were formed for the dc and ac components with consideration of SM capacitance and SM voltage ripples, and a step-by-step process was provided to derive the specific ac frequency that can minimize the internal ac current magnitude and avoid excess reactive power circulation. From this illustrative example, this analytical method was extended and applied to other base formats of CLMMCs. This theoretical analysis has been verified by both simulation examples and experimental tests. The simulation and experimental results all closely matched the mathematical derivation, and they demonstrated the validity of the analysis presented in this paper. The analysis presented here could be extended in further work to find good choices of internal ac frequency for three-phase hybrid and full-bridge CLMMCs, which will facilitate the dc interconnection for high power high voltage applications and address the dc fault issues in the dc interconnection.

Appendix

A. General Circulating Current Analysis for the Buck-Boost CLMMC

Substituting the results of (9) and (10) into (19) and (21), the general expression of the internal ac current magnitude for buck-boost CLMMC is given in (A–1).

$$
\begin{aligned}
I_{cir} = \frac{1}{2} I_{ac} = max\Bigg\{ & \left| \frac{-jC_{DC} N_T I_{dc} \delta_T^2}{2C_{SM}[1-\omega^2(L_T+L_B)C_{DC}](1+m)^2} \right| \left[\frac{m^2+8}{2m} \tan\theta \sin\omega t \right. \\
& + \frac{3m^2-8}{2m} \cos\omega t + (-m^2+3)\sin 2\omega t + 3\tan\theta\cos 2\omega t \\
& \left. - \frac{m}{2}\tan\theta\sin 3\omega t + \frac{m}{2}\cos 3\omega t \right] \\
& + \left| \frac{-jC_{DC} N_B I_{dc} \delta_B^2}{2C_{SM}[1-\omega^2(L_T+L_B)C_{DC}](R+m)^2} \right| \left[\frac{m^2+8R^2}{2m} \tan\theta \sin\omega t \right. \\
& + \frac{3m^2-8R}{2m} \cos\omega t + \frac{m^2-2R-R^2}{R} \sin 2\omega t - 3R\tan\theta\cos 2\omega t \\
& \left. - \frac{m}{2}\tan\theta\sin 3\omega t + \frac{m}{2}\cos 3\omega t \right] \Bigg\}
\end{aligned}
\qquad (A-1)
$$

B. Non-unity Ratio Conversion Analysis for the Buck-Boost CLMMC

The minimum ac current magnitude in the non-unity ratio conversion case ($\bar{v}_{in} = \bar{v}_o R, N_{T,B} = N_{arm}, L_{T,B} = L_{arm}, m_{dcT} = \frac{1}{1+m}, m_{dcB} = \frac{R}{R+m}$) for the buck-boost CLMMC is given in (A–2), and the corresponding ac frequency is presented in (A–3).

$$I_{cir-min} = \frac{1}{2} I_{ac-min} = \frac{N_{arm} I_{dc} C_{DC}[(8-3m^2)(R+m)^2 + (8R-3m^2)(1+m)^2]}{4C_{SM}(R+m)^2(1+m)^2 m(2\omega^2 L_{arm} C_{DC} - 1)} \quad (A-2)$$

$$f = \frac{1}{2\pi}\sqrt{\frac{1}{2L_{arm}C_{DC}} + \frac{N_{arm}[(8-3m^2)(R+m)^2 + (8R-3m^2)(1+m)^2]}{16 L_{arm} C_{SM}(R+m)^2(1+m)^2}} \quad (A-3)$$

C. General Circulating Current Analysis for the Buck CLMMC

The general expression of the internal ac current magnitude for buck CLMMC is given in (A–4). δ_T and δ_B are still the redundancy ratio for the dc components of stack voltages, but the expressions for SM stack dc modulation m_{dcT} and m_{dcB} have been changed in this buck format. ($V_{ac} = mV_{dc} \le min[V_{dc}(1-R), V_{dc}R]$, $R \le 1$, $m_{dcT} = \frac{\delta_T(1-R)}{1-R+m}, m_{dcB} = \frac{\delta_B R}{R+m}, \delta_{T,B} \le 1$). Further, C_{DC} still represents the equivalent dc link capacitance, but it directly equals the input capacitance C_{in} in this configuration ($C_{DC} = C_{in}$).

$$\begin{aligned} I_{cir} &= \frac{1-R}{2} I_{ac} \\ &= max\left\{\left|\frac{-jC_{DC}N_T I_{dc}\delta_T^2(1-R)}{2C_{SM}[1-\omega^2(L_T+L_B)C_{DC}](1-R+m)^2}\right|\left[\frac{m^2+8(1-R)^2}{2m}tan\,\theta\, sin\,\omega t\right.\right. \\ &+ \frac{3m^2-8(1-R)^2}{2m}cos\,\omega t + \frac{-m^2+3(1-R)^2}{1-R}sin\,2\omega t \\ &\left.\left. + 3(1-R)tan\,\theta\, cos\,2\omega t - \frac{m}{2}tan\,\theta\, sin\,3\omega t + \frac{m}{2}cos\,3\omega t\right] \right. \\ &+ \left|\frac{-jC_{DC}N_B I_{dc}\delta_B^2 R}{2C_{SM}[1-\omega^2(L_T+L_B)C_{DC}](R+m)^2}\right|\left[\frac{(m^2+8R^2)(1-R)}{2mR}tan\,\theta\, sin\,\omega t\right. \\ &+ \frac{(3m^2-8R^2)(1-R)}{2mR}cos\,\omega t + \frac{(m^2-3R^2)(1-R)}{R^2}sin\,2\omega t \\ &\left.\left. -3(1-R)tan\,\theta\, cos\,2\omega t - \frac{m}{2R}(1-R)tan\,\theta\, sin\,3\omega t + \frac{m}{2R}(1-R)cos\,3\omega t\right]\right\} \end{aligned} \quad (A-4)$$

D. General Circulating Current Analysis for the Boost CLMMC

The general expression of the internal ac current magnitude for boost CLMMC is given in (A–5). ($V_{ac} = mV_{dc} \le min[V_{dc}(R-1), V_{dc}], R \ge 1, m_{dcT} = \frac{\delta_T(R-1)}{R-1+m}, m_{dcB} = \frac{\delta_B}{1+m}, \delta_{T,B} \le 1, C_{DC} = C_o$).

$$\begin{aligned} I_{cir} &= \frac{R-1}{2R} I_{ac} \\ &= max\left\{\left|\frac{-jC_{DC}N_T I_{dc}\delta_T^2(R-1)}{2C_{SM}[1-\omega^2(L_T+L_B)C_{DC}](R-1+m)^2}\right|\left[\frac{-m^2-8(R-1)^2}{2mR}tan\,\theta\, sin\,\omega t\right.\right. \\ &- \frac{3m^2-8(R-1)^2}{2mR}cos\,\omega t + \frac{m^2-3(R-1)^2}{R(R-1)}sin\,2\omega t \\ &\left.\left. - \frac{3(R-1)}{R}tan\,\theta\, cos\,2\omega t + \frac{m}{2R}tan\,\theta\, sin\,3\omega t - \frac{m}{2R}cos\,3\omega t\right] \right. \\ &+ \left|\frac{-jC_{DC}N_B I_{dc}\delta_B^2}{2C_{SM}[1-\omega^2(L_T+L_B)C_{DC}](1+m)^2}\right|\left[-\frac{(m^2+8)(R-1)}{2mR}tan\,\theta\, sin\,\omega t\right. \\ &- \frac{(3m^2-8)(R-1)}{2mR}cos\,\omega t + \frac{(-m^2+3)(R-1)}{R}sin\,2\omega t \\ &\left.\left. + \frac{3(R-1)}{R}tan\,\theta\, cos\,2\omega t + \frac{m(R-1)}{2R}tan\,\theta\, sin\,3\omega t - \frac{m(R-1)}{2R}cos\,3\omega t\right]\right\} \end{aligned} \quad (A-5)$$

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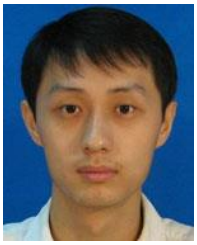

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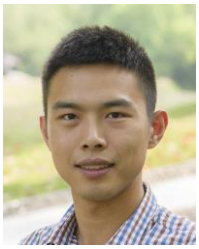

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