A 300 Mbps, 37 pJ/bit pulsed optical biotelemetry

Andrea De Marcellis[1] *Member, IEEE,* Guido Di Patrizio Stanchieri[1] *Student Member, IEEE,* Marco Faccio[1], Elia Palange[1], and Timothy G. Constandinou[2] *Senior Member, IEEE*

***Abstract*—This paper reports an implantable transcutaneous telemetry for a brain machine interface that uses a novel optical communication system to achieve a highly energy-efficient link. Based on an pulse-based coding scheme, the system uses sub-nanosecond laser pulses to achieve data rates up to 300 Mbps with relatively low power levels when compared to other methods of wireless communication. This has been implemented using a combination of discrete components (semiconductor laser and driver, fast-response Si photodiode and interface) integrated at board level together with reconfigurable logic (encoder, decoder and processing circuits implemented using Xilinx KCU105 board with Kintex UltraScale FPGA). Experimental validation has been performed using a tissue sample that achieves representative level of attenuation/scattering (porcine skin) in the optical path. Results reveal that the system can operate at data rates up to 300 Mbps with a bit error rate (BER) of less than 10^{-10}, and an energy efficiency of 37 pJ/bit. This can communicate, for example, 1,024 channels of broadband neural data sampled at 18 kHz, 16-bit with only 11 mW power consumption.**

***Index Terms*—Data telemetry, optical communication, transcutaneous telemetry, wireless link.**

I. Introduction

THIS past decade has seen significant new interest in developing innovative neurotechnologies for observing large scale activity from the brain and nervous system. This has been in part due to global initiatives (e.g. US BRAIN Initiative, EU Human Brain Project, etc) but also thanks to modern capability of microtechnology, and opportunities this brings. Key recent applications have included research tools for studying the brain (e.g. electrophysiology) [1]–[5], brain machine interfaces (BMIs) [6]–[8] and closed-loop neuromodulation [9]–[11]. The new feature in such devices is the ability to record, and subsequently detect and decode neural activity. This can be used directly to communicate, or control an external device (e.g. prosthetic) [12], [13] or to modulate (or 'titrate') stimulation (e.g. in deep brain stimulation) [10]. Particularly in BMI applications, there has been a strong desire to scale (i.e. extend) the number of concurrent recording channels [14] towards improving the underlying information transfer rate. For implanted systems, this poses a significant challenge in power consumption, to ensure any thermal dissipation does not cause damage to tissue. This places extremely tight constraints on the overall power budget of any instrumentation electronics, processing and subsequent wireless communication that is essential for implantable applications. For the wireless communication additionally, several other key factors such as noise requirements and signal integrity, biocompatibility, system volume, transmission error, electromagnetic interference (EMI) need to be taken into account [15]–[24].

A common approach used a number of conventional implantable medical devices such as cochlear implants for example, combines the power and data telemetries using inductive (near field) coupling [25], [26]. The downlink (external to implant) communication uses encoding schemes such as frequency or phase shift keying (FSK or PSK) to embed the downlink data within the power carrier. The uplink (implant to external) on the other hand typically use amplitude shift keying (ASK). An inductive biotelemetry however has two fundamental limitations: (1) the downlink data rate is tied to the carrier frequency that is limited (<10 MHz) to minimise absorption of electromagnetic (EM) energy; and (2) the uplink achieves a lower data rate to the downlink. There have been significant efforts reported in the literature towards addressing these limitations. These include using multiple carriers (i.e. separating the power and data links) [27] or advanced encoding schemes, for example, pulse harmonic modulation [28]. Although such methods have achieved uplink data rates of the order of 10 Mbps, this does not meet the demands of modern high bandwidth brain machine interfaces [7], [8].

Conventional (far field) radio that uses narrowband (carrier-based) electromagnetic radiation is also used for wireless communication within active implantable medical devices. This typically uses the MICS (Medical Implant Communication System) or ISM (Industrial, Scientific and Medical) bands that utilise carriers spanning from ≈400 MHz to ≈5 GHz, with lower frequencies being desirable to limit absorption losses. The maximum achievable data rate of different relevant wireless RF protocols (e.g. bluetooth, WBAN, proprietary [29]–[32]) are however limited to a few Mbps at best. Ultra-wideband (UWB) radio on the other hand uses pulse-based encoding to transmit data without needing a carrier. By utilising pulses with steep transitions (e.g. a short rise time), the EM energy is spread across an ultrawide spectrum allowing for high bandwidth data transmission with good energy efficiency [17], [33]–[36]. There exist challenges however also with UWB-based wireless including the antenna size and efficiency [37]–[39], losses through tissue and receiver complexity/power requirements.

Although there has been significant effort in the research community, it remains a major challenge to achieve a high

A. De Marcellis, G. Di Patrizio Stanchieri, M. Faccio and E. Palange are with the Electronic and Photonic Integrated Circuits and Systems (EPICS) Laboratory, Department of Industrial and Information Engineering and Economics, University of L'Aquila, L'Aquila 67100, Italy (e-mail: andrea.demarcellis@univaq.it).

T. G. Constandinou is with the Centre for Bio-Inspired Technology, Department of Electrical and Electronic Engineering, Imperial College London, London SW7 2AZ, UK, and also with the Care Research & Technology Centre, UK Dementia Research Institute.

Manuscript received XXX; revised XX, YY.

bandwidth and energy-efficiency transcutaneous telemetry for BMI applications. Existing neural recording systems with high channel counts (i.e. 100s to 1000s) thus generally employ one of two strategies: (1) using a wireline interface for data communication (e.g. SPI) [3], [5]; or (2) implement local processing to facilitate data reduction (e.g. spike detection, spike sorting, etc) [2], [33], [40] for subsequent low bandwidth wireless transmission.

An alternative, relatively recent approach towards realising a high bandwidth wireless telemetry has been to apply optical methods [41], [42]. An optical link potentially provides several desirable features, including: reduced size (i.e. compared to an antenna or coil), high transmission bandwidth (i.e. bitrate), low bit error rate, low power consumption (i.e. energy per bit) and good electromagnetic compatibility.

Previous work has seen optical telemetries developed for retinal prostheses, exploiting the fact that the eye provides a transparent optical window [43]. The challenge when applying this to other implantable applications (e.g. those requiring a transcutaneous link) is the relatively high attenuation (and scattering) of light when propagating through tissue. This attenuation however decreases with increasing wavelength [42]. Optical telemetries have thus been developed that utilise near infra-red (NIR) wavelengths (i.e. >800 nm) [16], [44]–[49]. These systems typically employ a semiconductor laser for transmission, and a photodiode (PD) for receiving the data. In the literature, performance has been improved by optimising optical wavelength (to reduce losses), increasing laser power (to improve the signal-to-noise ratio, SNR), applying modulation/encoding schemes (to maximise robustness) and increasing the photodiode active area (to improve link efficiency and also allow some tolerance to misalignment). Previous work has reported data rates up to 100 Mbps with an energy requirement of 21 pJ/bit [16], [41], [50], [51].

The work presented herein describes a high bandwidth optical telemetry that employs a specific pulsed data coding technique using sub-nanosecond laser pulses. This builds on our previous work [48], [49], by improving: (i) the front-end analog (laser drive and photodiode interface) circuit performance (bandwidth, power consumption); and (ii) the digital circuits (encoding, decoding, processing) capability using high performance reconfigurable logic (FPGA). These innovations increase the achievable data rate compared to the state-of-the-art whilst minimising BER and power consumption. This paper extends the preliminary work reported in [49] providing additional technical detail (design implementation, results, analysis) and experimental data using biological tissue.

The remainder of this paper is organised as follows: Section II provides the system overview and describes the data coding concept; Section III details the circuit implementation; Section IV presents the experimental results; and Section V concludes this work.

II. System Overview

The overall system architecture of the transcutaneous optical biotelemetry link is shown in Fig. 1. The system is composed of two sub-systems separated by the tissue/skin

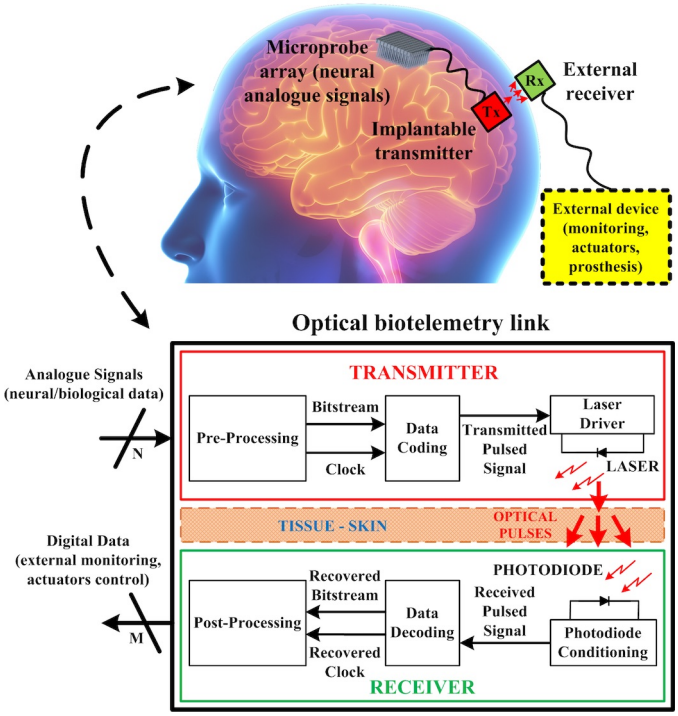


Fig. 1. Proposed transcutaneous optical telemetry system concept.

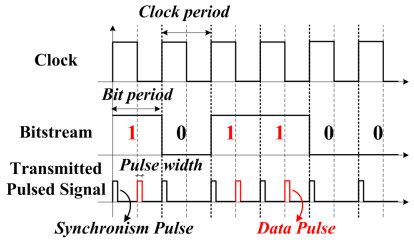


Fig. 2. Timing diagram showing data coding process using OOK modulation.

layer: an implantable platform including the transmitter and an external unit containing the receiver. The two units function to communicate the high bandwidth bitstream across the tissue layers, whilst also handling the clock signal. More specifically, the transmitter takes the conditioned (analog) neural recording, digitizes, serializes and encodes this and emits optical pulses via the semiconductor laser. The receiver then detects these optical pulses using the PD, recovers the clock and decodes the bitstream by de-serializing the digital data. Referring to Fig. 1, the transmitter unit is composed of: (i) digital circuits to pre-process and encode the data; (ii) analog circuits for driving the laser; and (iii) a high bandwidth Vertical Cavity Surface Emitting Laser (VCSEL) that generates sub-nanosecond light pulses in the near infrared region of the EM spectrum. The receiver unit on the other hand includes: (i) a fast silicon PD used to detect the received optical pulses; (ii) analog circuits for biasing/conditioning the PD (converting the photocurrent to voltage pulses); (iii) digital circuits to decode and post-process the received pulses to recovered clock and data.

A timing diagram is shown in Fig. 2 illustrating the data coding process that uses synchronous On-Off Key (OOK) modulation to combine the input bitstream and clock signals. For each bit that is transmitted there are two phases: (i) the synchronization phase that always inserts a pulse on the rising

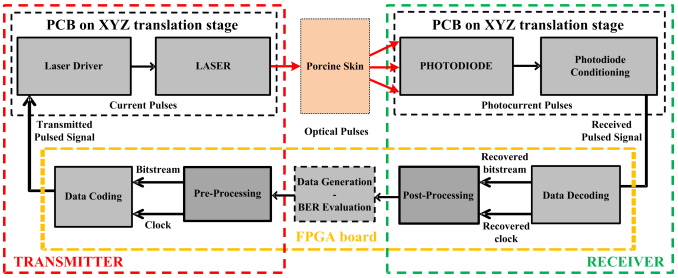


Fig. 3. Top-level system architecture of the implemented optical biotelemetry highlighting the transmitter and receiver sub-systems.

edge of the clock; and (ii) the data transmission phase that inserts the data pulse (i.e. symbol $\{0\}$ or $\{1\}$) on the falling edge of the clock. It should however be noted that even with no pulse (i.e. a $\{0\}$ signal) being transmitted, a subthreshold bias is maintained to the VCSEL to ensure a fast transition is then possible when transmitting a pulse.

III. Circuit Implementation

The top-level system architecture is shown in Fig. 3. This illustrates the specific circuit blocks implemented for the test platform described herein.

A. Analog circuits for optoelectronic interfacing

These circuits are to interface with the optoelectronic components (i.e. emitter and detector). The emitter uses a VCSEL device (VCSEL-850 by Thorlabs) with emission wavelength λ=850 nm and 2.2 mA threshold current. The detector uses a fast silicon PD (FDS-025 by Thorlabs) with 47 ps response time and 250 μm active area diameter including a coupling ball lens having a diameter of 1.5 mm.

Both the laser driver and photodiode conditioning circuits operate from a single VCC=5 V supply voltage. The design, optimization and simulation of both circuits have been performed through AWR Microwave Office tools. The circuits have been implemented using a printed circuit board (PCB) prototype. The PCB uses a TLX8 (high volume fiberglass reinforced microwave) substrate to minimise parasitics and discrete commercial off-the-shelf (COTS) components (i.e., transistors for high-frequency/RF applications).

1) Laser driver circuit: The laser driver circuit (within the transmitter sub-system) is based on a single transistor stage, shown in Fig.. 4. This uses a BFG520 NPN 9 GHz wideband bipolar RF transistor (C1=100 nF, C2=1.8 pF, R1=82 Ω, R2=50 Ω, RTRIM1=5 kΩ). This operates to convert the input voltage pulses (i.e. the encoded signal to be transmitted) into current pulses for driving the VCSEL. This regulates the amplitude of the pulsed current (i.e., the resulting laser pulse peak value) through the resistive trimmer RTRIM1.

2) Photodiode conditioning circuit: The photodiode conditioning circuit (within the receiver sub-system) is based on a multi-stage transimpedance amplifier, shown in Fig. 5. This uses a cascade of four (wideband ERA-1SM+InGaP HBT monolithic) Darlington pair stages to convert the received photocurrent pulses into voltage pulses. A very high gain is essential here to ensure that the voltage pulses generated have an amplitude higher than the digital logic threshold needed for

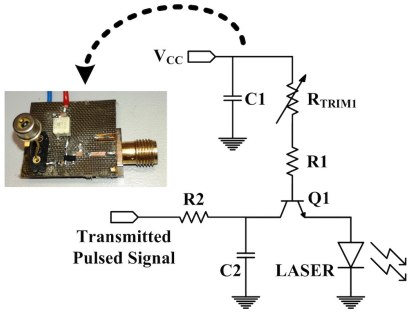


Fig. 4. Laser driver circuit schematic and PCB implementation.

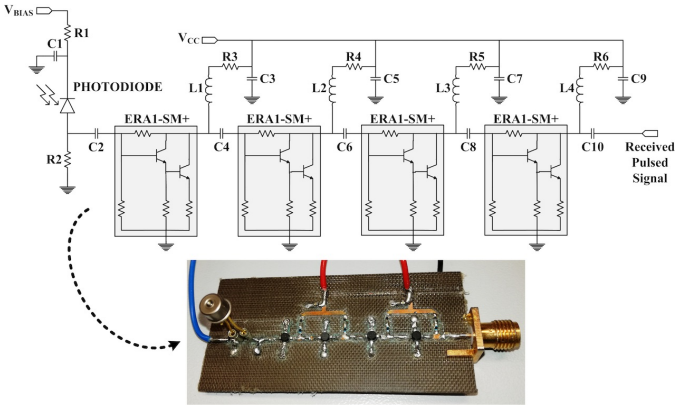


Fig. 5. Photodiode conditioning circuit schematic and PCB implementation.

a correct detection of a "high" logic level by the subsequent Data Decoding block. The circuit configuration is as follows: VBIAS = VCC = 5 V, L1 = L2 = L3 = L4 = 33 nH, C1 = C3 = C5 = C7 = C9 = 100 nF + 100 pF, C2 = C4 = C6 = C8 = C10 = 470 pF, R1 = 1 kΩ, R2 = 50 Ω, R3 = R4 = R5 = R6 = 180 Ω.

Simulation results for the laser driver and photodiode conditioning circuits are shown in Fig. 6. First, a transient response of the laser driver circuit shows the generated current pulses for the circuit operating at 300 Mbps (i.e., a transmission of a repeated sequence of bits $\{0\}$ corresponding to the generation of only the synchronization pulses). Secondly, a frequency response (i.e., the S21 parameter corresponding to the total gain of the amplifier) of the photodiode conditioning circuit shows a high gain across a wide frequency bandwidth with a maximum value of about 44 dB. Thirdly, the stability factor K of the photodiode conditioning circuit shows a value that is always higher than 1, demonstrating the stability condition of this amplification stage.

B. Digital circuits for signal processing

In addition to the analog circuits described in the previous section that are used for optoelectronic interfacing, the system requires high speed digital logic for data management and to ensure robust communication. This has been divided into 4 functional blocks (2 in transmitter and 2 in receiver), in addition to an ad-hoc test circuit that is used to evaluate performance. This is shown in the lower portion of Fig. 3. Within the transmitter, the data acquisition circuit (i.e. front end neural recording system) feeds the digital samples into the pre-processing block that serializes the stream. This is then passed to the data coding block that combines the data

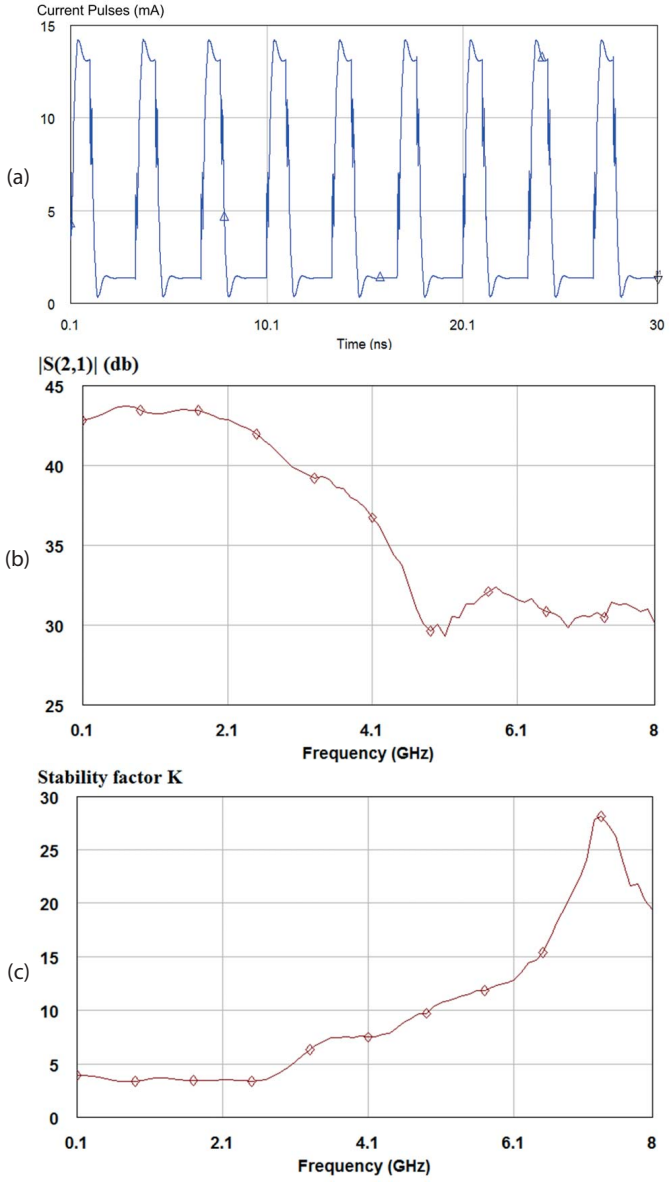


Fig. 6. Simulation results of the analog circuits: (a) time response of the laser driver circuit; (b) frequency response (i.e., the S21 parameter); and (c) stability factor K of the photodiode conditioning circuit.

stream with clock signal using a pulse-based encoding scheme. This directly feeds the laser driver circuit described previously to emit the optical pulses. On the side of the receiver, the photodiode conditioning circuit provides a recovered voltage-mode stream of pulses. This feeds the data decoding and clock recovery circuits that recovery a clock signal and synchronized datastream. Finally, this is fed to the post-processing circuit that converts the bitstream into valid data packets.

All the digital circuits have been implemented using a commercially-available FPGA development board (Xilinx KCU105 with Kintex UltraScale XCKU040-2FFVA1156E FPGA). The I/O general-ports are configured to LVCMOS18 compatibility (1 V digital logic threshold) with 16 mA maximum output current.

1) Pre-processing circuit: The pre-processing circuit is shown in Fig. 7. This also illustrates a typical neural data acquisition system (DAS, top right) which consists of low

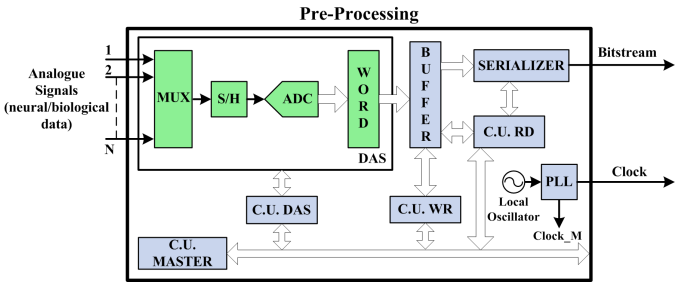


Fig. 7. Pre-processing circuit showing the organisation of the different control units (CUs) for the data acquisition system (DAS), parallel word register (WR), and read data (RD) serializer. Implemented on FPGA.

noise biopotential amplifier, filters, and data converter, e.g. [4], [40], [52]. The function of the pre-processing circuit is to generate a single bitstream from multichannel sampled data by interleaving the different channels/samples using time-division multiplexing (TDM). This has been designed to take in up to 1,024 channels of data sampled at 18 kHz with 16-bit resolution. The pre-processing circuit operates as follows: for each sample, the DAS control unit (C.U. DAS) sequences through all the data channels storing each 16-bit sample in the word register (FIFO-type PIPO buffer). The word length is thus $2\times$ 8-bit bytes. The initial portion of this register is pre-loaded with a preset start sequence that forms the *Header* of the data packet. Each packet contains a single sample across all 1,024 channels (i.e. 2,048 bytes) in addition to the start sequence. In order to ensure the output is a continuous bitstream (i.e. a continuous serialization of the composed data packages), the master control unit (C.U. master) coordinates the timing of all the operations/functions (i.e. data acquisition, data read and data write) of the overall pre-processing block. Additionally, a local oscillator provided on the FPGA board allows implementation of a phase-locked loop (PLL) block, to provide an internal reference clock (i.e. Clock_M @ 300 MHz) for system synchronization.

2) Data encoding circuit: The data encoding circuit is shown in Fig. 8. This takes in the clock and serial data bitstream (from pre-processing circuit) and combines these to generate the pulsed output signal for modulating the transmission. The output encodes the clock as a synchronisation pulse on the rising edge of the clock, whereas the data (i.e. $\{0\}$ or $\{1\}$ bit symbol) is pulsed on the falling edge of the clock. This circuit operates as follows: firstly, the clock input signal drives the PLL that generates two signals (A and B) with pulses on the rising and falling clock edges respectively. These signals (A and B) have a pulse repetition frequency of 300 MHz (3.33 ns pulse interval), with a phase difference of 180deg (i.e. half clock period, $\approx$1.67 ns) and a duty cycle of 25% the clock period (i.e. 0.83 ns pulse width). Signal A (the synchronisation pulse) is then combined (using an OR logic gate) with the data pulse (obtained by gating the serial data bit with signal B) to generate the output signal that modulates the laser driver.

3) Data decoding circuit: The data decoding circuit is shown in Fig. 9. This takes in the received signal that is generated by the photodiode conditioning circuit and recovers the clock and serial data stream. This operates as follows:

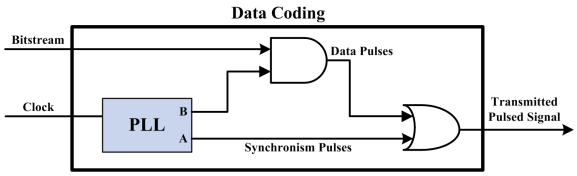


Fig. 8. Data encoding circuit that combines clock and data into a single pulse stream. Implemented on FPGA.

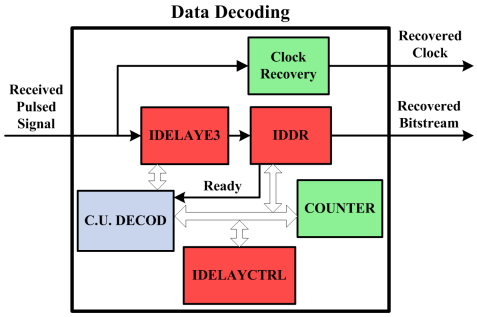


Fig. 9. Data decoding circuit that recovers the clock and data from the received pulse stream. Implemented on FPGA.

both the clock recovery and IDELAYE3 blocks share the input signal. IDELAYE3 is a programmable delay line that adds a finite and discrete delay (up to 512 delay taps, each ranging from 2.5 ps to 15 ps) to the input pulsed signal. The IDDR block then takes in the delayed (through IDELAYE3) signal together with the recovered clock, and generates two outputs, capturing the input signal on the rising and falling edges of the recovered clock. The first output (*ready* signal) is high if correctly capturing the synchronization pulse (on the rising edge). The second output (recovered bitstream) thus captures the serial data (on the falling edge) providing the synchronisation pulse is correctly aligned. The decoder control unit (C.U. DECOD) ensures correct alignment by varying the programmable delay until the *ready* signal remains in the 'high' logic state for at least 50 clock periods (≈166.5 ns). Furthermore, the IDELAYCTRL block has been included to provide further compensation (to the programmable delay) to supply voltage and/or temperature variations.

4) Clock recovery circuit: The clock recovery circuit (within the data decoding circuit described above) is shown in Fig. 10. This consists of a D-type flip-flop (D-FF), a PLL and a latch. This operates as follows: The input signal feeds the D-FF clock (with D input set to high) such that the Q output is asserted high whenever a pulse is detected. The latch then provides a finite 'delay' before resetting the D-FF. Specifically, the output Q remains in the high logic state for a time interval T_{FF} given by:

$$T_{FF}(Q=1) = T_{Loop} + T_{Latch} + T_{RST} \quad (1)$$

where T_{Loop} is the physical time delay introduced by the feedback loop that connects the D-FF output Q to the latch and the latch to the RST input of the D-FF, T_{Latch} is the response time of the latch and T_{RST} is the time necessary to the D-FF to make effective the reset operation.

This overall 'delay' is intentionally selected to be ≈75% the clock period (τ=3.3 ns) such that if a data $\{1\}$ is received, the synchronisation and data pulses are effectively merged into

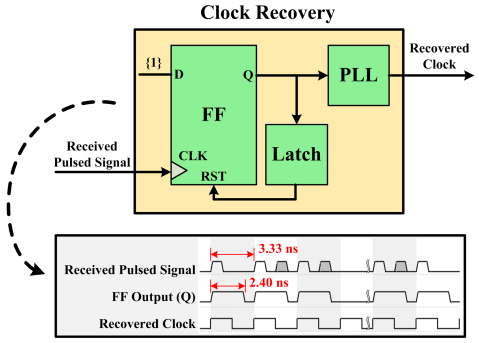


Fig. 10. Clock recovery circuit that recovers a symmetrical clock from the received pulse stream. Implemented on FPGA.

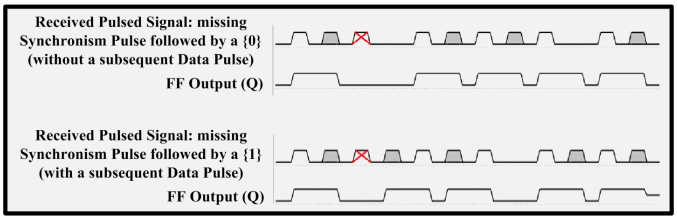


Fig. 11. Example showing the impact of transmission errors to the clock recovery circuit.

one longer pulse. For this, a 2.4 ns time interval is achieved using a manual place & route operation for the implementation of the clock recovery circuit. This time interval ensures that for each clock period only one pulse will generated, irrespective of the data that has been encoded. The subsequent PLL then completes the clock recovery by adjusting this to have a 50% duty cycle whilst also reducing jitter.

The employed PLL (integrated within the FPGA board) is capable of managing and locking to input signals with an operating frequency ranging from 70 MHz to 933 MHz providing a 50% duty-cycle output signal with the best precision of 200 ps (i.e. the maximum error that can affect the output duty-cycle).

However, since transmission errors can occur (e.g. introduced by the communication channel), it is important to evaluate the impact this may have to clock recovery. Fig. 11 gives an example showing the transient response of the clock recovery circuit in the presence of different transmission errors (i.e. missing synchronisation pulses). This can result in one of following two events: (1) if the next pulse is another synchronization pulse (i.e. without a subsequent data pulse), then there will be no low-to-high transition at the D-FF output (input to PLL) (see top, Fig. 11); or (2) if there is a subsequent data pulse, the D-FF output (input to PLL) will have a phase shift of 180deg until a further data $\{0\}$ (i.e. missing data pulse) occurs (see bottom, Fig. 11). Tests conducted on the FPGA board have however demonstrated that, in both cases, the output of the PLL maintains the recovered clock locked at 300 MHz. This remains the case also in the presence of multiple repeated errors that occur at the PLL input, thus guaranteeing good robustness for the overall communication system.

5) Post-processing circuit: The post-processing circuit is shown in Fig. 12. The synchronous serial data that has been recovered is firstly stored in a SIPO register (serial-to-parallel converter (SPC)). The master control unit (C.U. MASTER)

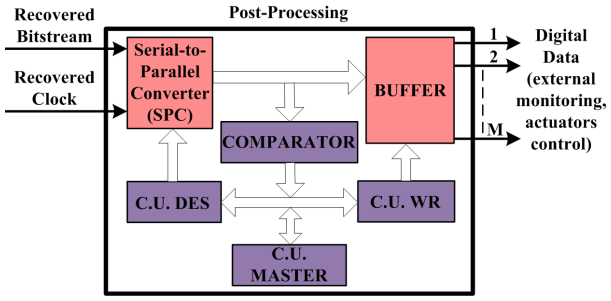


Fig. 12. Post-processing circuit that recovers the individual channel data. Implemented on FPGA.

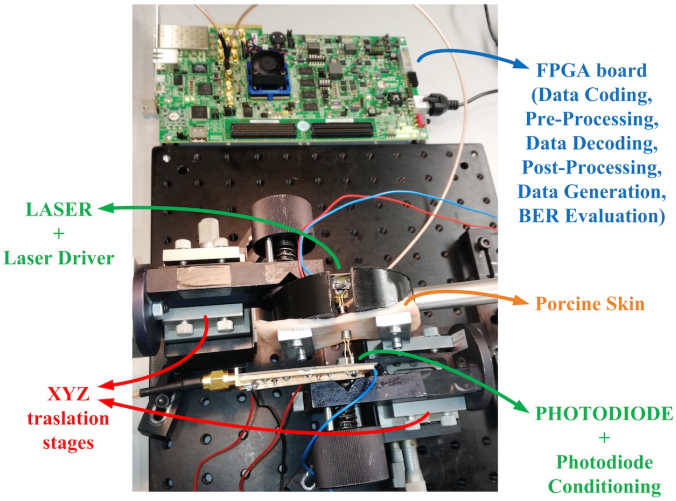


Fig. 13. Photograph showing the experimental setup for characterizing the optical biotelemetry.

continuously verifies and checks the received data packets using the comparator block. When the *Header* that defines the beginning of the transmitted data packet is correctly identified, the C.U. MASTER activates the control units (C.U. WR and C.U. DES). These then allow the serial data packets to be split into individual channel data and saved in the register *buffer* that provides the output. This operation is continuously performed and repeated for each data packet that is received and identified by the *Header*.

IV. Experimental Results

The experimental setup for overall system characterization is shown in Fig. 13. This is used for both individual block level test and also system evaluation using a tissue sample (porcine skin). The optoelectronic components (i.e. emitter and detector) are each mounted on their respective PCBs on either side of the tissue samples. These are initially positioned to be perfectly aligned and in close contact with the tissue (without pressing onto). The relative positions are then adjusted accordingly to characterize the optical link.

A. Optical characterization

A simplified schematic describing the optical characterization setup is in Fig. 14. The tissue sample used here was a section of cleaned porcine skin that was gently tensioned using a custom made holder so as to mimic the human skin layers [16], [41]. This consisted of the epidermal, dermal and adipose

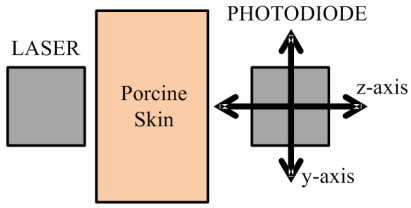


Fig. 14. Schematic showing the experimental setup for characterizing the optical biotelemetry. The emitter (laser) and tissue sample (porcine skin) are both fixed whereas the detector (photodiode) is mounted on an XYZ-translation stage for precise adjustment.

layers with an average thickness of approximately 3.5 mm. The emitter (VCSEL), i.e. laser driver PCB was mounted at a fixed position whereas the detector (PD), i.e. photodiode conditioning PCB was attached to a XYZ-translation stage with micropositioners allowing for precise adjustment (20 μm resolution, approximately 1/10th the active area of the PD).

The setup is first calibrated by first ensuring the porcine tissue sample is in close contact with the emitter. The emitter is then driven with pulses whilst the detector is adjusted in the XY-plane such as to maximize the received optical signal (i.e. thus perfectly align the two). The Z-axis of the detector is then adjusted to also bring the detector in contact with the porcine skin sample. The overall link performance is then assessed by its ability to correctly detect emitted pulses. Specifically, any pulse that is detected (at the output of the PD conditioning circuit) to be above 1 V can be robustly sampled by the FPGA. Pulses received to be below 1 V on the other hand are not always detected and thus result in the generation of errors.

The first set of tests were performed to assess the sensitivity to lateral misalignment and proximity between emitter and detector. Lateral misalignment was characterised by adjusting the detector in the Y-axis at different proximities between emitter and detector (i.e. Z-axis displacements). The results are given in Fig. 15. The tests were repeated for misalignment in the X-axis that gave identical results to the Y-axis misalignment tests. During all measurements the VCSEL position remained fixed and the maximum instantaenous pulsed optical power was maintained at below 2 mW, with a pulse width of about 900 ps and at a pulse repetition rate of 300 MHz. For the measurements taken for Z=0, the receiver is adjusted to be in contact with the dermal sample without pressing it. In this position, the minimum distance between the VCSEL and the Si photodiode is approximately 3.5 mm, corresponding to the approximate thickness of the porcine skin sample.

The results show (as expected) that as the lateral misalignment (or proximity between emitter and detector) increases, the recovered voltage pulse amplitude decreases. The range of operability (reliable detection of voltage pulses) thus depends on both lateral misalignment but also the proximity between optoelectronic components and skin surface. The trade-off in the range of operability (i.e. when the received pulses are exactly 1 V) between lateral misalignment and proximity to the tissue sample is shown in Fig. 16. It is observed that this trade-off ranges between a lateral misalignment of 0.65 mm and vertical misalignment (i.e. proximity between detector and sample) of 0.75 mm.

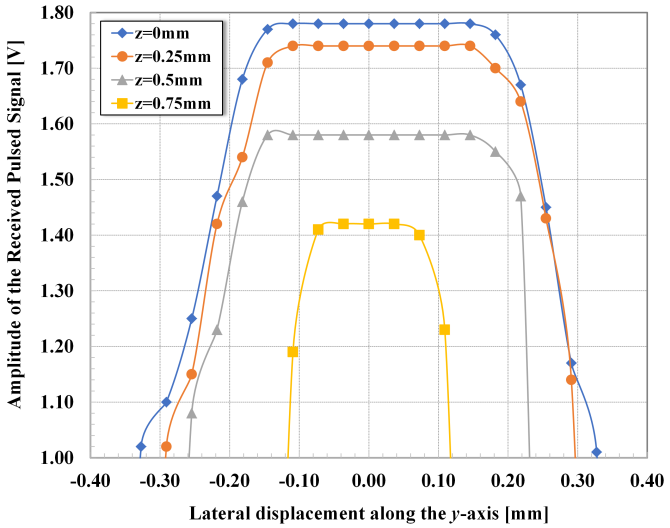


Fig. 15. Sensitivity of lateral misalignment showing the amplitude of the received pulses as a function of the lateral displacement along the Y-axis for different Z-axis proximities (distance between detector and tissue sample).

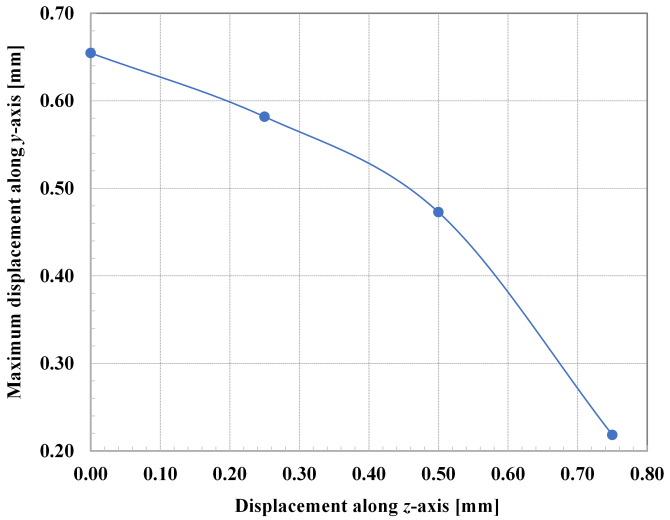


Fig. 16. Receiver operability range (i.e. maximum displacement along Y-axis) as a function of its proximity from the tissue sample. Based on data measured in Fig. 15.

B. End-to-end communication

In order to completely characterize the overall system operating at 300 Mbps (i.e., a 3.33 ns bit period) the experimental setup the same experimental setup described previously was used. All measurements have been taken using a digital storage oscilloscope (LeCroy Wavemaster 8600A). In order to emulate the digitization of the DAS within the pre-processing circuit and quantify performance (i.e. BER, power consumption, etc), a 2^{31}-1 bit pseudo-random bit sequence (PRBS) has been generated using the FPGA providing the test signal. This was included during the system implementation (see Fig. 3).

More specifically (referring to Figs. 3 and Fig. 7), in order to emulate the DAS operation, a sequence of random 16-bit words, composed using the 2^{31}-1 bit PRBS, are generated and inserted in the PIPO register (WORD) thus bypassing the DAS. The BER can then be evaluated by comparing the transmitted and received data streams. A captured waveform (using oscilloscope) of the system operating at 300 Mbps is

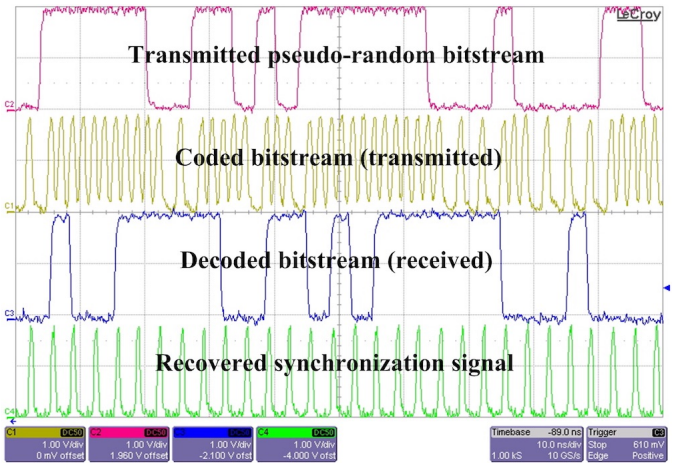


Fig. 17. Captured waveform showing the main signals during transmission of the pseudo-random bitstream at 300 Mbps. Signals shown (from top to bottom) are: (in purple) the input bitstream of pseudo-random data; (in yellow) the transmitted coded pulses; (in blue) decoded data; and (in green) recovered clock signal.

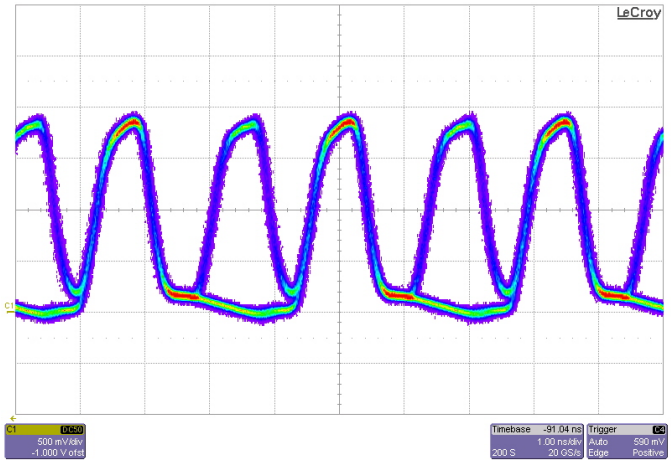


Fig. 18. Captured waveform showing multiple acquisitions of the transmitted signal (i.e. coded pulses).

shown in Fig. 17. This demonstrates the correct operation by observing the matching between the received PRBS (i.e. decoded bitstream) and the transmitted data. This measured results show a latency of less than 12 ns, between the transmitted and the recovered bitstreams. This is due to the execution of the clock recovery and data decoding processes.

To assess the quality of the transmitted signal (i.e. coded pulses), multiple acquisitions are captured in the waveform shown in Fig. 18. The measured amplitude variation and jitter in phase are lower than 150 mV and 150 ps, respectively.

To assess the quality of the received signal (i.e. recovered bitstream), an eye diagram is captured shown in Fig. 19. The measured amplitude variation and jitter in phase are lower than 150 mV and 200 ps, respectively.

C. Electromagnetic compliance

It is important to note that although the proposed system uses pulse-based encoding, this is different to impulse radio (IR) UWB modulation, nor is this transmitted using an UWB antenna. However, due to the steep pulse transitions the internal signals comply with standard UWB specifications since the

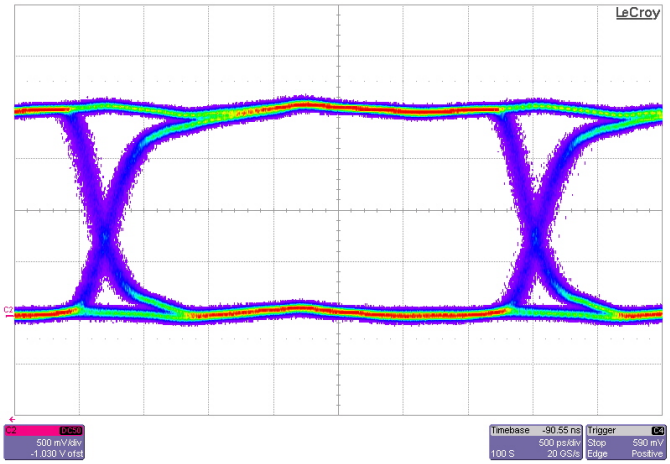


Fig. 19. Eye-diagram of the received signal (i.e. recovered bitstream).

laser pulses have a duration of under 1 ns and a transition time of less than half the pulse width. Therefore, any energy that is potentially emitted into the electromagnetic spectrum needs to comply with the relevant regulations. The power spectrum of the transmitted signal is given in Fig. 20. This shows both the electrical (output of laser driver) and optical (emitted by VCSEL) power spectral densities in subfigures (a) and (b) respectively. These show that the emitted energy fulfills the Federal Communications Commission (FCC) standard mask on the power spectrum of modulated/pulsed signals (i.e., the signal power emission limits for communication systems) [53]. Specifically, the results show a 1 GHz bandwidth primary lobe (higher than 500 MHz, the lower limit for the classification of a UWB device as defined by the FCC), corresponding to the inverse of the laser pulse duration, and this validates the theoretical expectations. In addition, the optical power spectral density is always lower than –41.3 dBm/MHz that is the FCC emission limits for the communications in the considered operating frequency and bandwidth (i.e. <0.96 GHz).

D. Overall system performance

Through the experimental measurements, it has been demonstrated that the proposed optical biotelemetry is able to achieve a BER lower than 10^{-10} and overall system power consumption of less than 11 mW. Operating at 300 Mbps, this corresponds to an energy efficiency of 37 pJ/bit. These results have been obtained by optimizing both the laser pulse width – set to 900 ps (via the PLL shown in Fig.8) and pulsed laser drive current – set to 10 mA (via RTRIM1 resister in Fig. 4 to 10 mA with a null DC laser bias current).

V. Conclusion

This paper has reported the design, fabrication and characterization of an optical communication system employing a custom pulsed-based coding technique. The system is able to achieve high data rates with good energy efficiency, targeting biomedical applications such as high bandwidth implantable brain machine interfaces. These applications are extending the number of recording channels and as such are demanding high bandwidth, low power wireless communication. The system has been validated through a series of experimental

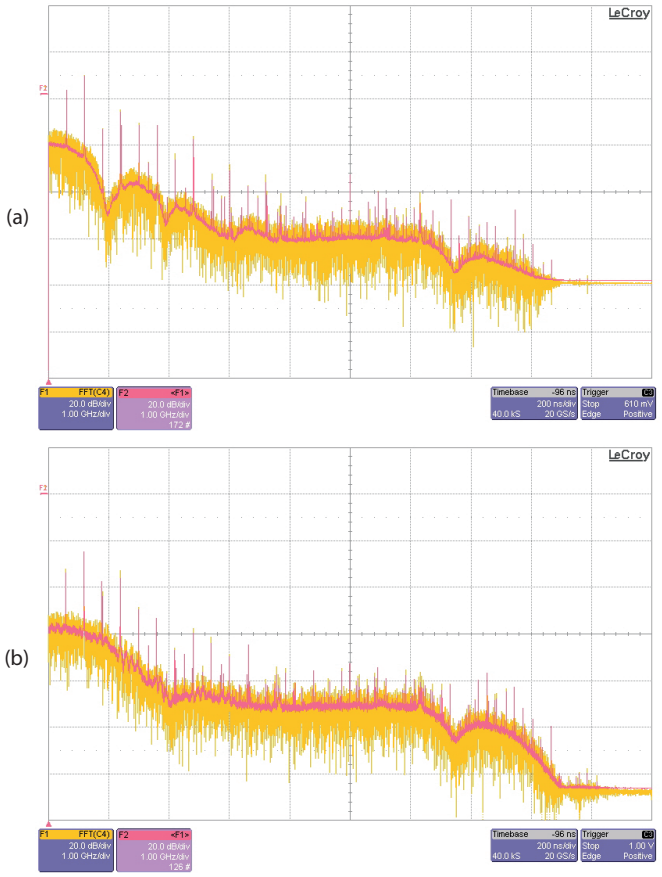


Fig. 20. Measured power spectrum of (a) the transmitted pulse signal; (b) the optical emissions (by VCSEL). The orange traces show the measured signal whereas the purple traces show the average values.

measurements using a tissue sample placed in the optical path. These have demonstrated operation at 300 Mbps with an energy efficiency of 37 pJ/bit and minimum BER of 10^{-10}. Optical characterization has revealed a relatively high sensitivity to misalignment ($\pm 325\,\mu$m in XY-plane) and limited proximity between emitter and detector (3.5 mm+$<750\,\mu$m in Z-axis). The achieved system performance is compared to the current state-of-the-art in Table I. Ongoing work is focused on technology integration, implementing detector (photodiode), front-end circuits (laser driver, photodiode conditioning), and signal processing in a monolithic integrated circuit. This will significantly reduce both size and power consumption. The inclusion of optics (e.g. lens) can act to improve misalignment sensitivity and/or improve received SNR.

Acknowledgment

The authors would like to acknowledge “Carni Bianche” (Roseto Degli Abruzzi, Teramo, Italy) for providing samples of the porcine skin used for the experimental measurements.

References

[1] H. Miranda *et al.*, “HermesD: a high-rate long-range wireless transmission system for simultaneous multichannel neural recording applications,” *IEEE Trans. Biomed. Circuits Syst.*, vol. 4, no. 3, pp. 181–191, 2010.

[2] S. Luan *et al.*, “Compact standalone platform for neural recording with real-time spike sorting and data logging,” *Journal of Neural Engineering*, vol. 15, no. 4, p. 046014, 2018.

TABLE I
COMPARISON WITH THE STATE-OF-THE-ART

Reference	Year	Bitrate [Mbps]	Energy Efficiency [pJ/bit]	BER	Implementation	Telemetry	Range [mm]	Coding
[20]	2004	80	563	$<10^{-14}$	Discrete	Optical	5	NRZ
[32]	2007	40	108	$<10^{-5}$	Discrete	Optical	3	NRZ
[19]	2010	136	22	$<10^{-3}$	0.18 μm CMOS	RF	200	OOK
[22]	2011	1	1640	$<10^{-5}$	90 nm CMOS	IR-UWB	1500	S-OOK
[21]	2013	135	10	N.A.	0.13 μm CMOS	IR-UWB	120	PPM
[34]	2014	100	21	$<10^{-7}$	Integrated Tx Discrete Rx	Optical	2.5	N.A.
[8]	2015	100	32	N.A.	Discrete	Optical	2	N.A.
[18]	2015	67	30	$<10^{-7}$	Integrated Tx Discrete Rx	IR-UWB	500	OOK
[30]	2016	128	36	$<10^{-9}$	Discrete	Optical	4	Custom OOK
[31]	2017	250	24	$<10^{-9}$	Discrete	Optical	3	Custom OOK
[23]	2017	11	370 (Tx only)	N.A.	0.13 μm CMOS	RF	N.A.	QPSK
[24]	2018	0.106 (U/L)	140	$<10^{-4}$	0.18 μm CMOS	Inductive	10	LSK
		0.211 (D/L)	1027	$<10^{-5}$				BPSK
[25]	2019	0.125	50400 (Tx only)	N.A.	Discrete	RFID	50	LSK
This work	**2020**	**300**	**37**	$<\mathbf{10^{-10}}$	**Discrete**	**Optical**	**4.25**	**Custom OOK**

[3] G. N. Angotzi *et al.*, "SiNAPS: an implantable active pixel sensor CMOS-probe for simultaneous large-scale neural recordings," *Biosensors and Bioelectronics*, vol. 126, pp. 355–364, 2019.

[4] S. Wang *et al.*, "A compact quad-shank cmos neural probe with 5,120 addressable recording sites and 384 fully differential parallel channels," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 6, 2019.

[5] J. Putzeys *et al.*, "Neuropixels data-acquisition system: A scalable platform for parallel recording of 10,000+ electrophysiological signals," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 6, pp. 1635–1644, 2019.

[6] N. Ahmadi *et al.*, "Towards a distributed, chronically-implantable neural interface," in *IEEE/EMBS Conf. on Neural Engineering (NER)*, 2019, pp. 719–724.

[7] E. Musk *et al.*, "An integrated brain-machine interface platform with thousands of channels," *Journal of Medical Internet Research*, vol. 21, no. 10, p. e16194, 2019.

[8] A. M. Obaid *et al.*, "Massively parallel microwire arrays integrated with CMOS chips for neural recording," *bioRxiv*, p. 573295, 2019.

[9] C.-H. Cheng *et al.*, "A fully integrated 16-channel closed-loop neural-prosthetic CMOS SoC with wireless power and bidirectional data telemetry for real-time efficient human epileptic seizure control," *IEEE J. Solid-State Circuits*, vol. 53, no. 11, pp. 3314–3326, 2018.

[10] S. Stanslaski *et al.*, "A chronically implantable neural coprocessor for investigating the treatment of neurological disorders," *IEEE Trans. Biomed. Circuits Syst.*, vol. 12, no. 6, pp. 1230–1245, 2018.

[11] R. Ramezani *et al.*, "On-probe neural interface ASIC for combined electrical recording and optogenetic stimulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 12, no. 3, pp. 576–588, 2018.

[12] M. J. Vansteensel *et al.*, "Fully implanted brain–computer interface in a locked-in patient with als," *New England Journal of Medicine*, vol. 375, no. 21, pp. 2060–2066, 2016.

[13] M. Capogrosso *et al.*, "A brain–spine interface alleviating gait deficits after spinal cord injury in primates," *Nature*, vol. 539, no. 7628, pp. 284–288, 2016.

[14] I. H. Stevenson and K. P. Kording, "How advances in neural recording affect data analysis," *Nature Neuroscience*, vol. 14, no. 2, p. 139, 2011.

[15] H. Yuan and B. He, "Brain–computer interfaces using sensorimotor rhythms: current state and future perspectives," *IEEE Trans. Biomed. Eng.*, vol. 61, no. 5, pp. 1425–1435, 2014.

[16] T. Liu, J. Anders, and M. Ortmanns, "Bidirectional optical transcutaneous telemetric link for brain machine interface," *Electronics Letters*, vol. 51, no. 24, pp. 1969–1971, 2015.

[17] K. Duncan and R. Etienne-Cummings, "Selecting a safe power level for an indoor implanted UWB wireless biotelemetry link," in *IEEE BioCAS Conf.*, 2013, pp. 230–233.

[18] A. D. Rush and P. R. Troyk, "A power and data link for a wireless-implanted neural recording system," *IEEE Trans. Biomed. Eng.*, vol. 59, no. 11, pp. 3255–3262, 2012.

[19] A. Kiourti and K. S. Nikita, "A review of in-body biotelemetry devices: Implantables, ingestibles, and injectables," *IEEE Trans. Biomed. Eng.*, vol. 64, no. 7, pp. 1422–1430, 2017.

[20] W. Li, Y. Duan, and J. Rabaey, "A 200-Mb/s energy efficient transcranial transmitter using inductive coupling," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 2, pp. 435–443, 2018.

[21] Y. Antonenko *et al.*, "Wireless charger for implantable biotelemetry system," in *IEEE UWBUSIS Conf.*, 2018, pp. 260–263.

[22] I. Ghotbi *et al.*, "A wireless pulsed-current battery charger for implantable biomedical stimulators," in *IEEE MWCAS Conf.*, 2016, pp. 1–4.

[23] D. Nikolayev, M. Zhadobov, and R. Sauleau, "Immune-to-detuning wireless in-body platform for versatile biotelemetry applications," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 2, pp. 403–412, 2019.

[24] Y. Rezaeiyan, M. Zamani, O. Shoaei, and W. A. Serdijn, "Mixed-signal IC with pulse width modulation wireless telemetry for implantable cardiac pacemakers in 0.18-μm CMOS," *IEEE Trans. Biomed. Circuits Syst.*, vol. 12, no. 3, pp. 589–600, 2018.

[25] J. Georgiou and C. Toumazou, "A 126 μw cochlear chip for a totally implantable system," *IEEE J. Solid-State Circuits*, vol. 40, no. 2, pp. 430–443, 2005.

[26] A. Javan-Khoshkholgh and A. Farajidavar, "An implantable inductive near-field communication system with 64 channels for acquisition of gastrointestinal bioelectrical activity," *Sensors*, vol. 19, no. 12, p. 2810, 2019.

[27] M. Ghovanloo and S. Atluri, "A wide-band power-efficient inductive wireless link for implantable microelectronic devices using multiple carriers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 10, pp. 2211–2221, 2007.

[28] F. Inanlou, M. Kiani, and M. Ghovanloo, "A 10.2 Mbps pulse harmonic modulation based transceiver for implantable medical devices," *IEEE J. Solid-State Circuits*, vol. 46, no. 6, pp. 1296–1306, 2011.

[29] P. D. Bradley, "An ultra low power, high performance medical implant communication system (MICS) transceiver for implantable devices," in *IEEE BioCAS Conf.*, 2006, pp. 158–161.

[30] O. Omeni, A. C. W. Wong, A. J. Burdett, and C. Toumazou, "Energy efficient medium access protocol for wireless medical body area sensor networks," *IEEE Trans. Biomed. Circuits Syst.*, vol. 2, no. 4, pp. 251–259, 2008.

[31] J. Jung *et al.*, "22-pJ/bit energy-efficient 2.4-GHz implantable OOK transmitter for wireless biotelemetry systems: In vitro experiments using rat skin-mimic," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 12, pp. 4102–4111, 2010.

[32] K.-H. Teng and C.-H. Heng, "A 370-pJ/b multichannel BFSK/QPSK transmitter using injection-locked fractional-N synthesizer for wireless biotelemetry devices," *IEEE J. Solid-State Circuits*, vol. 52, no. 3, pp. 867–880, 2017.

[33] M. S. Chae *et al.*, "A 128-channel 6 mW wireless neural recording IC with spike feature extraction and UWB transmitter," *IEEE Trans. Neural Syst. Rehabil. Eng.*, vol. 17, no. 4, pp. 312–321, 2009.

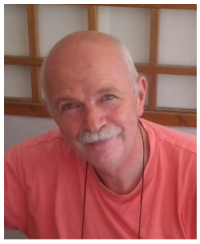
[34] M. Crepaldi, C. Li, J. R. Fernandes, and P. R. Kinget, "An ultra-wideband impulse-radio transceiver chipset using synchronized-OOK modulation," *IEEE J. Solid-State Circuits*, vol. 46, no. 10, pp. 2284–2299, 2011.

[35] M. Elzeftawi and L. Theogarajan, "A 10 pJ/bit 135 Mbps IR-UWB transmitter using pulse position modulation and with on-chip LDO regulator

in 0.13 μm CMOS for biomedical implants," in *IEEE BioWireleSS Conf.*, 2013, pp. 37–39.
[36] A. Ebrazeh and P. Mohseni, "30 pJ/b, 67 Mbps, centimeter-to-meter range data telemetry with an IR-UWB wireless link," *IEEE Trans. Biomed. Circuits Syst.*, vol. 9, no. 3, pp. 362–369, 2014.
[37] M. Haas, B. Schweizer, J. Anders, and M. Ortmanns, "A miniaturized UWB antenna for implantable data telemetry," in *IEEE EMBS Conf.*, 2017, pp. 1086–1089.
[38] J. Kang *et al.*, "A miniaturized implantable dual-band platform design for wireless power transfer and biotelemetry," in *IEEE APMC*, 2017, pp. 330–333.
[39] Y. Zhang *et al.*, "A wideband circularly polarized implantable antenna for 915 mhz ISM-band biotelemetry devices," *IEEE Antennas Wireless Propag. Lett.*, vol. 17, no. 8, pp. 1473–1477, 2018.
[40] Y. Liu *et al.*, "A 64-channel versatile neural recording SoC with activity-dependent data throughput," *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 6, pp. 1344–1355, 2017.
[41] D. M. Ackermann Jr *et al.*, "Designing the optical interface of a transcutaneous optical telemetry link," *IEEE Trans. Biomed. Eng.*, vol. 55, no. 4, pp. 1365–1373, 2008.
[42] K. S. Nikita, *Handbook of Biomedical Telemetry*. John Wiley & Sons, 2014.
[43] W. Liu *et al.*, "Challenges in realizing a chronic high-resolution retinal prosthesis," in *Artificial Sight*, 2007, pp. 129–149.
[44] D. M. Ackermann Jr, "High speed transcutaneous optical telemetry link," Ph.D. dissertation, Case Western Reserve University, 2008.
[45] D. A. Borton, M. Yin, J. Aceros, and A. Nurmikko, "An implantable wireless neural interface for recording cortical circuit dynamics in moving primates," *Journal of Neural Engineering*, vol. 10, no. 2, p. 026010, 2013.
[46] T. Liu *et al.*, "In vivo verification of a 100 Mbps transcutaneous optical telemetric link," in *IEEE BioCAS Conf.*, 2014, pp. 580–583.
[47] D. M. Kuchta *et al.*, "A 71-gb/s NRZ modulated 850 nm VCSEL-based optical link," *IEEE Photon. Technol. Lett.*, vol. 27, no. 6, pp. 577–580, 2015.
[48] A. De Marcellis *et al.*, "A pulsed coding technique based on optical UWB modulation for high data rate low power wireless implantable biotelemetry," *Electronics*, vol. 5, no. 4, p. 69, 2016.
[49] A. De Marcellis *et al.*, "A 250 Mbps 24 pJ/bit UWB-inspired optical communication system for bioimplants," in *IEEE BioCAS Conf.*, 2017, pp. 1–4.
[50] Y.-H. Wen and K.-M. Feng, "A simple NRZ-OOK to PDM RZ-QPSK optical modulation format conversion by bidirectional XPM," *IEEE Photon. Technol. Lett.*, vol. 27, no. 9, pp. 935–938, 2015.
[51] K. Chi, Y.-h. Zhu, X. Jiang, and V. C. Leung, "Energy-efficient prefix-free codes for wireless nano-sensor networks using OOK modulation," *IEEE Trans. Wireless Commun.*, vol. 13, no. 5, pp. 2670–2682, 2014.
[52] D. Y. Barsakcioglu *et al.*, "An analogue front-end model for developing neural spike sorting systems," *IEEE Trans. Biomed. Circuits Syst.*, vol. 8, no. 2, pp. 216–227, 2014.
[53] US Federal Communications Commission (FCC), "Revision of part 15 of the commissions rules regarding ultra-wideband transmission systems," *First Report and Order, ET Docket*, pp. 98–153, 2002.

Andrea De Marcellis received the degree in electronic engineering and the Ph.D. degree in microelectronics from the University of L'Aquila, Italy, in 2005 and 2009, respectively. He is currently an Associate Professor of Electronics and a member of the Electronic and Photonic Integrated Circuits and Systems (EPICS) Laboratory at the Department of Industrial and Information Engineering and Economics, University of L'Aquila, Italy. His main research activities concern the design of mixed-signal electronic and optoelectronic integrated circuits and systems for signal conditioning, data processing, optical sensing and communication links for biomedical applications. He has co-authored a book, a book-chapter and more than 160 scientific publications in international journals and conference proceedings. He is Chair of the Technical Committee "Optoelectronic sensing systems" of the IEEE Italy Sensors Chapter and is a member of the Editorial Board of Universal Journal of Electrical and Electronic Engineering (Horizon Research Publishing Corporation, USA).

Guido Di Patrizio Stanchieri received the master degree (cum laude) in electronic engineering from the University of L'Aquila, L'Aquila, Italy, in 2017. Starting from 2016 he joined an external scientific collaboration with the Department of Industrial and Information Engineering and Economics, University of L'Aquila, L'Aquila, Italy, where currently is a Ph.D. student. His main research activities concern the design and implementation of digital electronic circuits and systems for signal processing and data communication in biomedical and robotics integrated applications.



Marco Faccio received the Laurea degree in electrical engineering from the University of L'Aquila, Italy, in 1979. In 1989, he joined as an Assistant Professor of Applied Electronics with the Department of Electrical Engineering, University of L'Aquila, Italy, where currently he is an Associate Professor with Digital Electronic Systems. His research interests include hardware architectures for fast signal processing, hardware design of algorithms, and co-design methodologies as well as A/D conversion for smart sensor applications, digital filtering architectures, digital architectures for bio-implant communication and low voltage digital systems. Further topics regard the design of internal control units and interfaces for N and MLC flash memories. He has coauthored more than 90 international papers.

Elia Palange (Laurea Degree in Physics – Sapienza University of Rome) is currently Associate Professor of Physics and Nanophotonics and the Supervisor of the Electronic and Photonic Integrated Circuits and Systems (EPICS) Laboratory at the Department of Industrial and Information Engineering and Economics, University of L'Aquila, Italy. During his scientific activities, he carried out research on laser physics and on the linear and nonlinear optical properties of bulk semiconductors and of nanometer-sized quantum semiconductor heterostructures. His current topics of research are the design and implementation of novel photonics multifunctional devices, sensors based on the linear and nonlinear optical properties of metamaterials, functionalized metasurfaces combined with high-sensitive optoelectronic detection systems.

Timothy G. Constandinou (AM'98–M'01–SM'10) received the B.Eng. and Ph.D. degrees in electronic engineering from Imperial College London, in 2001 and 2005, respectively. He is currently a Reader of Neural Microsystems within the Circuits and Systems Group, Department of Electrical and Electronic Engineering at Imperial College London and also the Deputy Director of the Centre for Bio-Inspired Technology. His current research interests include neural microsystems, neural prosthetics, brain machine interfaces, implantable devices, and low-power microelectronics. He is a fellow of the IET, a chartered engineer, and member of the IoP. Within the IEEE, he serves on several committees/panels, regularly contributing to conference organization, technical activities, and governance. He chairs the IEEE Sensory Systems Technical Committee, is a member of the IEEE BioCAS Technical Committee, IEEE Brain Initiative Steering Committee, and serves on the IEEE Circuits and Systems Society Board of Governors for the term 2017–2019. He was the technical program Co-Chair of the 2010, 2011 and 2018 IEEE BioCAS conferences, General Chair of the BrainCAS 2016 and NeuroCAS 2018 workshops, Special Session Co-Chair of the 2017 IEEE ISCAS Conference, and Demonstrations Co-Chair of the 2017 BioCAS Conference. He is currently Associate Editor-in-Chief of the IEEE Transactions on Biomedical Circuits and Systems.