A New Protection Scheme for an SSSC in an MV Network by Using a Varistor and Thyristors

Erfan Bashar, *Student Member, IEEE*, Dan Rogers, *Member, IEEE*, Ruizhu Wu, Li Ran, *Senior Member, IEEE*, Mike Jennings, Timothy C. Green, *Fellowr Member, IEEE,* and Philip Mawby, *Senior Member, IEEE*

***Abstract*— To control power flow and manage fault level in meshed MV networks, back-to-back voltage source converters (B2B-VSCs) are being used. However, their high cost and relatively low efficiency are of concerns. Partially rated series compensators, such as SSSCs or UPFCs, are desired but come with the challenge of protecting the device during grid faults. Their potential of use has been limited in comparison with the fully rated back-to-back converters. This paper proposes a new system topology including thyristor crowbars and a varistor to protect the SSSC in an MV network and improve the reliability and flexibility of the network operation. Using the proposed method, the time required for isolating the series compensator from the grid is reduced from at least 20 ms, corresponding to the interruption time of conventional circuit breakers, down to 3 μs in the worst case in addition to the grid fault detection delay. The performance is evaluated by simulation. A small-scale single-phase prototype operating at 230 V/16 A is tested in order to demonstrate the concept.**

Index term — Power system reliability, power system fault, protection, static synchronous series compensator, power semiconductors, thyristor, varistor

I. INTRODUCTION

Low-carbon distributed generation (DG) continues to be added to medium voltage (MV) networks, presenting challenges to the control of busbar voltage, branch power and operation of relays & circuit breakers. To increase the ability of the network to accommodate embedded generation, power electronic compensators could play important roles by making the network more flexible and controllable. Potential technologies include voltage source converters in different combinations. Figure 1 shows a typical medium-voltage distribution network with DG. The feeders are usually separated at the primary busbars, and the further ends are connected only when one of the feeders has lost connection to the mains supply. With increasing DG, it is desirable to join the feeders at appropriate positions using devices based on power electronics, such as a static synchronous series compensator (SSSC) as shown in Figure 1. Issues such as busbar voltage fluctuation, branch overloading, and excessively high fault levels are some of the main challenges to operate the system with increasing

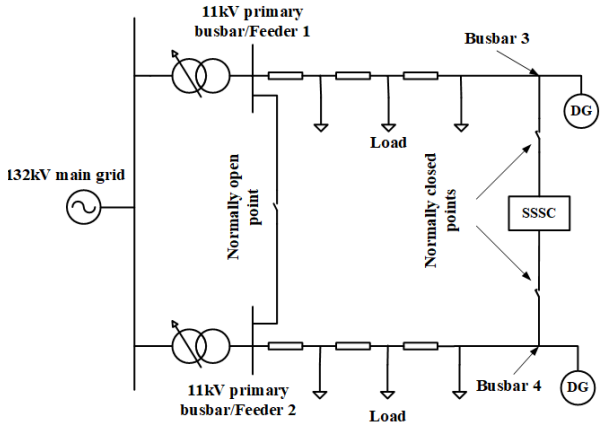

Figure 1 Typical MV network with multiple feeders including SSSC-Convectional protection mechanism

DG. Other network management techniques to ease these situations include the unified power flow controller (UPFC), static VAR compensator (SVC), soft-open point and transformer on-load tap changing. The UPFC is described as 'universal' due to its ability to independently control the real and reactive power flows [1]. The series insertion of a voltage, like in an SSSC, is most effective and many studies have been carried out to find the optimal sizing and allocation in terms of cost and dynamic response [2, 3].

Managing some of the devices under system fault conditions has been difficult, especially those injecting a series voltage for control and compensation. Mechanical switches are too slow. Therefore, solid-state circuit breakers (SSCBs) or other power electronics-based schemes have attracted research attention in recent years involving thyristors, GTOs or IGBTs [3, 4]. However, the high capital cost and large operational power loss have limited their deployment [5, 6]. Furthermore, increasing DG may cause large DC current offset which may delay the zero-crossing of the fault current and increase the duties of the power semiconductors [7, 8]. Therefore, estimating the dynamic response is potentially important when designing a protection scheme [9, 10]. Much of the existing literature focusses on the potential applications of series compensators by considering their cost and efficiency. Series compensators are

Erfan Bashar, Robert Wu, Li Ran, and Philip A. Mawby are with the School of Engineering, the University of Warwick, Coventry, CV4 7AL, U.K. (E-mail: e.bashar@warwick.ac.uk; Ruizhu.Wu@warwick.ac.uk; l.ran@warwick .ac.uk; p.a.mawby@warwick.ac.uk).
Mike Jennings is with the College of Engineering, Swansea University, Bay Campus, Fabian Way, Swansea, SA1 8EN, Wales, U.K. (E-mail: m.r.jennings@swansea.ac.uk).
Dan Rogers is with the Department of Engineering Science, the University of Oxford, Parks Road, Oxford, OX1 3PJ, U.K. (E-mail: dan.rogers@eng.ox. ac.uk).
Timothy C. Green is with the Department of Electrical and Electronic Engineering, Imperial College, South Kensington, London, U.K. (E-mail: t.green@imperial.ac.uk).

inherently vulnerable to short circuit faults in the grid. But only a few studies have been conducted regarding the protection of the series compensator itself, which were related to the mitigation of voltage dip [11, 12], limiting the fault current [13, 14] using a fault current limiter or different control designs integrated with the static series compensator. This paper presents a fast-acting scheme for protecting the SSSC, which provides series voltage insertion using power electronics.

Table 1 compares the studied protection mechanisms with the proposed method that is detailed next in the paper.

Table 1: Comparison of different protection mechanisms

Categories	Main components	Advantages	Disadvantages
Fast breaking switches [15],[16]	Fuses	Small size, low cost	Poor maintenance, unclear melting time
	Fast mechanical switch	Small size, low power loss	Electric arc with contact erosion, low speed
	Hybrid circuit breakers/solid-state circuit breakers	Fast, small arcing	Complex structure, relatively high cost
Fault current limiter [15], [17]	Switched superconductor devices	Auto-limiting with the resistive current	High cost, large size
	PWM control	Simple structure, resistive current	High power dissipation of MOV
	Gate voltage control	Simple structure, resistive current	High power dissipation of semiconductors
	Controlled bridge with inductor	Controllable current, no additional heat	High current harmonics with thyristors
	Static synchronous series compensators	No additional heat, controllable current, low total harmonic distortion	Complex structure, capacitor charging issues
MOV-gap mechanism [18-20]	MOV and spark gap	Small size, low cost, relatively fast, no harmonics	Coordinating MOV and spark gap, high initial voltage, difficult turning-off process in cases
Proposed thyristor crowbar-varistor mechanism	Thyristor and MOV	Small size, low cost, very fast, simple coordination, no arc issue, low power loss, no harmonics	Thyristor temperature during surge condition

II. STATIC SYNCHRONOUS SERIES COMPENSATOR

The network topology shown in Figure 1 is selected as the target system. Feeder 1 is connected to 3 load groups evenly distributed along the 5 km cable and Feeder 2 also has 3 load groups evenly distributed along the 10 km cable. The cable resistance and inductance are 0.06 ohm/km and 0.134 mH/km, respectively. An SSSC is then installed between Busbars 3 and 4 as the connection at the further ends of the two adjacent feeders to control the power transferred across them and manipulate the voltage or loss profiles. The following extreme case is selected to determine the compensation scheme: Feeder 2 is heavily loaded, 17 MW in total with a power factor of 0.98,

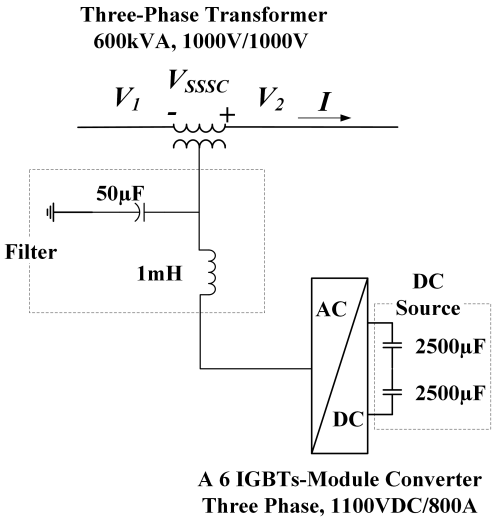

Figure 2: Configuration of the SSSC in the power system

and Feeder 1 is lightly loaded with only 1 MW load of the same power factor. It is assumed that a load of 8 MW needs to be transferred from Feeder 2 to Feeder 1 to balance the two Feeders. Balance of DG can be similarly achieved.

The SSSC is a partially rated compensating device, which by injecting a voltage orthogonal to the current can manipulate the power flow and damp power oscillation in the grid. Figure 2 shows the connection of the compensator in the power system. The network determines the required injection voltage, in this study an 1100 V_{DC} converter is utilised to control the power flow. The ABB HiPak IGBT module 5SNE 0800M170100, which has the ratings of V_{ce}=1700 V and I_c=800 A, is selected for building the converter. A three-phase 500 kVA, 1000 V to 1000 V coupling transformer is included in the SSSC, corresponding to a maximum of 6.5% compensation level which is usually enough for a local distribution network with low impedance. When transferring the 8 MW active power, the converter is at the maximum operating point and its output current magnitude is about 520 A. Therefore, under the full load condition, one IGBT module for each arm and 6 modules in total are sufficient. The SSSC does not use any active power source, as long as the injected voltage stays in quadrature with the line current. This is guaranteed by the closed-loop control. By varying the magnitude (V_q) of the injected voltage, the SSSC acts as a controllable reactance compensator, either capacitive

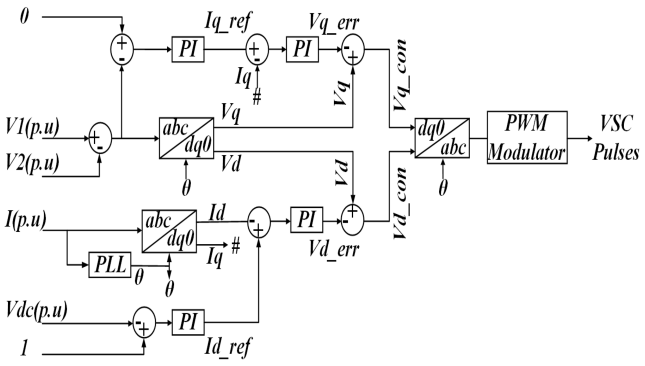

Figure 3: Closed-loop controller for voltage-sourced converter (VSC)

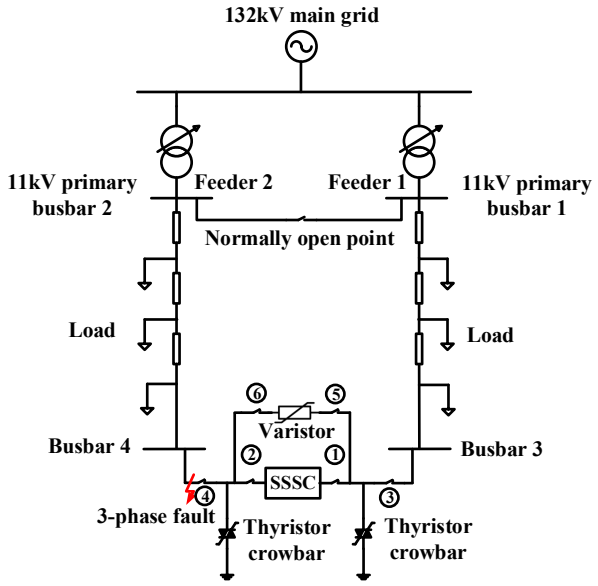

Figure 4: Schematic of proposed method by using both thyristor crowbars and varistor

or inductive. A low-pass LC filter is utilised to suppress the switching harmonics and electromagnetic interference. In addition, a closed-loop control system is used to synthesize the appropriate sinusoidal voltage waveform of the voltage-source converter that is applied to the grid. The control system tries to keep the injected voltage in quadrature with the reference line current and keep the DC link voltage constant. The voltage loop controls the voltage difference between Busbars 3 and 4 and determines the amplitude of the injected voltage on the q-axis.

III. THYRISTOR-BASED PROTECTION SCHEME WITH VARISTOR

A major challenge is to protect the series compensator during a grid short circuit fault; in this case, a large current will flow, and the voltage applied to the series compensator will rise to the full grid voltage. When a three-phase-to-ground fault occurs close to an unprotected SSSC, as shown in Figure 4, the voltage across the SSSC will immediately rise to the full line voltage of 11 kV (while the device voltage rating of the converter is only 1700 V) and the current will also rise rapidly to several thousand amperes (while the continuous current rating of the converter is only 800 A). Over-voltage and over-current of such magnitudes will simply destroy the converter and conventional mechanical circuit breakers are not able to respond rapidly to prevent damage. Using thyristors to provide a faster response could be a potential solution. This paper proposes a new thyristor-based protection scheme, which also includes a varistor, as shown in Figure 4, to protect the SSSC in the MV distribution network. Thyristor crowbars have previously been used to mitigate unbalanced voltage dips under grid fault conditions for SSSCs [11, 12] but they have not been used for protecting the device during grid short-circuit faults.

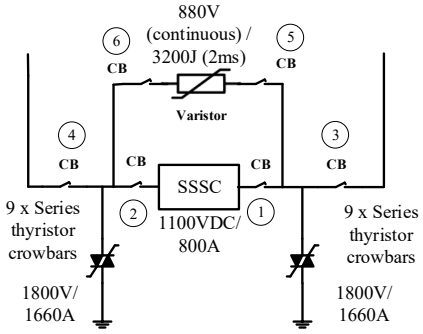

Figure 5: Protection circuit schematic

The protection principles are that the thyristor crowbars create another phase-to-ground current path upon the fault, preventing the fault current from passing through the SSSC. Before the thyristor crowbar is turned on due to fault detection time delay of the relay, the voltage across the SSSC will be limited by the varistor. The protection process is described in detail in the following subsections.

A) Protection system design

Some details of the protection scheme are expanded in Figure 5. The protection process is as follows. When a fault occurs on either side of the SSSC, the voltage across the SSSC will increase to the clamping voltage of the varistor. At this point, the varistor allows a current to pass through it and keeps the voltage at this level. Therefore, it prevents the voltage across the SSSC from rising excessively high, and this allows the control of the SSSC current. The threshold voltage of the protection relay is set to 50% of the varistor clamping voltage. After detecting the fault, a delay of 1 ms is assumed before the thyristor crowbars are gated on. Thyristors operate very quickly (<3 μs [21]) compared to the mechanical CBs, whose opening time delay is uncertain and at least 20 ms [22, 23]. By turning on the thyristors, the varistor comes out of the clamping state and the fault current will pass through them instead of the visitor and SSSC whose current is controlled to discharge the DC link capacitor and the current will eventually be zero; circuit breakers ①, ②, ⑤ and ⑥ are then opened. At this point, the SSSC is completely isolated from the grid and the thyristor crowbars can be gated off. This technique can decrease the effective response time of the SSSC protection from >20 ms to about 3 μs. Circuit breakers ③ and ④ are backup of ① and ② in case of failure for the thyristors to turn off. All CBs except ③ and ④ are of very low breaking duties. Stresses on the SSSC are immediately released.

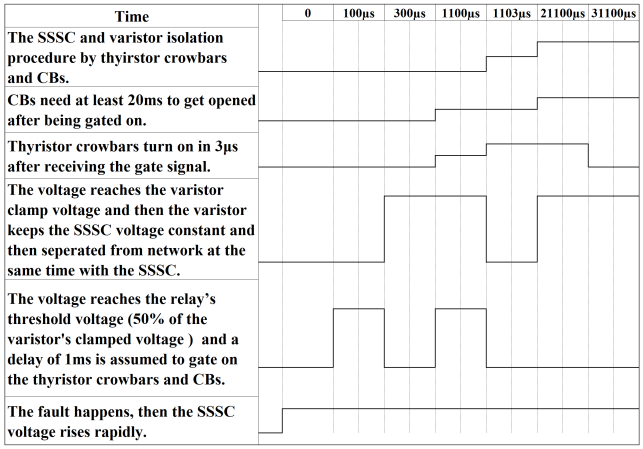

Figure 6: A timing diagram of the protection system procedure

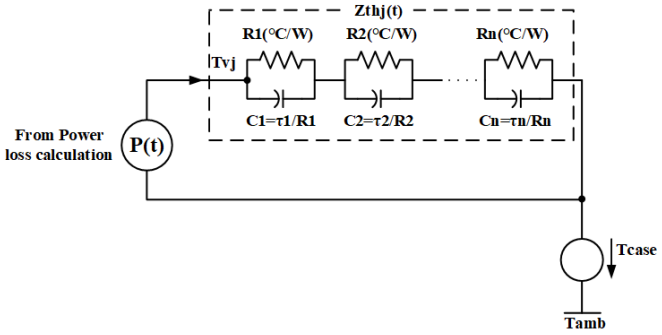

Figure 7: A typical Foster thermal model for IGBT, PiN diode and Thyristor

B) Timing diagram

The procedure of this protection scheme from the fault detection to isolating the SSSC can be summarised in the timing diagram in Figure 6. It shows the proposed protection scheme and also the required timing in sending the gate signals to the thyristor crowbars and CBs that have to be at the same time, otherwise any delay could cause severe damage to the thyristors and definitely the SSSC. In order to keep the turning on delay of thyristor crowbars as low as possible, no voltage crossing detection is used in the control system.

IV. THERMAL MODELS AND DEVICE LIMITS

A) Thermal model

All devices must be kept below their maximum allowable temperatures. The thermal behaviours of the IGBT chips, PiN diodes, and thyristors are modelled using Foster networks [24, 33] as shown in Figure 7.

R_i is the thermal resistance and τ_i is the time constant of each section in the Foster network, which are provided in the device datasheets ($\tau_i = R_i C_i$) and as shown in Table 2. The junction temperature can be calculated as follows:

$$T_{vj}(t) = \int_0^t P(t) \times \dot{Z}_{thj}(t-\tau) \times d\tau + T_{case}(t),\ Z_{thj}(t) = \sum_{i=1}^{n} R_i(t) \times (1 - e^{\frac{-t}{\tau_i}}) \quad (1)$$

where $Z_{thj}(t)$ is the total thermal impedance, T_{case} is the case temperature, T_{vj} is the junction temperature and P(t) is the power loss. For the IGBT:

$$P_{IGBT}(t) = P_{conduction}(t) + P_{switching}(t) \quad (2)$$

where $P_{conduction}(t)$ refers to the transistor power loss when it conducts the current and $P_{switching}(t)$ is the summation of turn-on and turn-off switching losses of the transistor.

Table 2: Thermal impedance

Model	i	1	2	3	4
IGBT-5SNE 0800M170100-ABB	R_i(K/kW)	15.2	3.6	1.49	0.74
	τ_i(ms)	202	20.3	2.01	0.52
PiN diode-5SNE 0800M170100-ABB	R_i(K/kW)	25.3	5.78	2.6	2.52
	τ_i(ms)	210	29.6	7.01	1.49
Thyristor- 5STP 18F1800-ABB	R_i(K/kW)	10.350	3.760	2.290	0.670
	τ_i(ms)	0.3723	0.0525	0.0057	0.0023

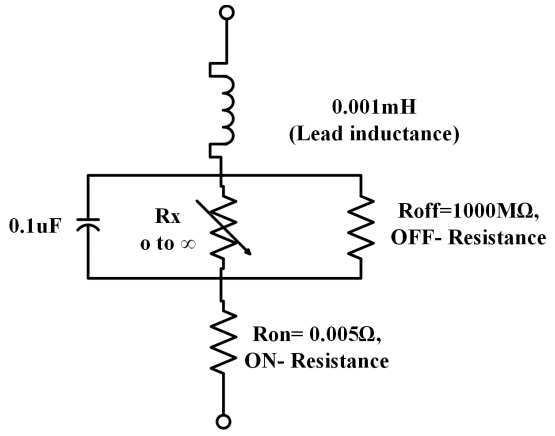

Figure 8: An equivalent circuit of a varistor (V881BA60, LittelFuse)

For the PiN diode:

$$P_{PiN\ DIODE}(t) = P_{conduction}(t) + P_{reverse\ recovery}(t) \quad (3)$$

where $P_{reverse\ recovery}(t)$ refers to the reverse recovery loss.

For the thyristor:

$$P_{THYRISTOR}(t) = P_{conduction}(t) \quad (4)$$

Varistor devices demonstrate fairly complicated electrical behaviour and their modelling can be approached in several ways. The most common representation of the impedance is an equivalent circuit as shown in Figure 8 [25], which is added to the clamping voltage depending on the current direction. To simplify varistor modelling the following equation is often used [26-28]:

$$I = I_0 \times (V/V_0)^{\alpha} \quad (5)$$

For the varistor used in this paper, I_0, V_0 and α are 1000 A, 2450 V and 35, respectively. *V* is the voltage across the varistor and V_0 is the clamping voltage, so R_X is derived as follows:

$$R_x = \frac{V}{I} = \frac{V}{I_0 \times (V/V_0)^{\alpha}} \quad (6)$$

A varistor is typically pulse rated: as long as the peak current and the absorbed energy do not exceed the datasheet specifications the varistor will remain intact [27, 29]. Therefore, a Foster thermal network model is not used for the varistor. The energy absorbed by the varistor is obtained by:

$$E = \int_0^T V_c(t) I(t) dt \quad (7)$$

where $V_c(t)$ is the component voltage, and I(t) the current.

B) Device limits

According to the IGBT module datasheet, the maximum withstanding junction temperature is 150°C for both of the IGBT and the PiN diode and the maximum surge current of the IGBT module is 6.6 kA for a 10 ms-pulse, when the junction temperature is 125°C.

In terms of the thyristor surge current, junction temperature, and voltage rating, the device utilised in this simulation can endure 17.5 kA during one pulse and 14.2 kA during two pulses, when the initial junction temperature is 125°C where each pulse

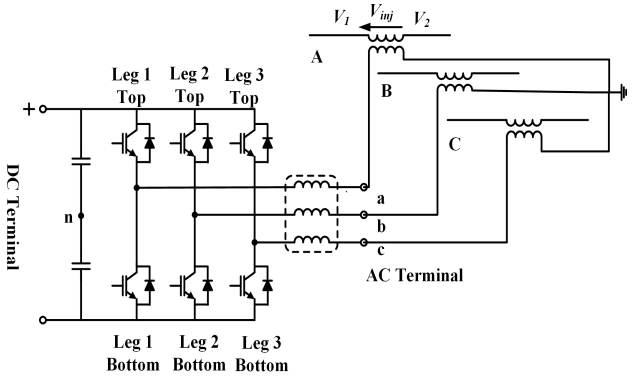

Figure 9: A schematic of three phase VSC-SSSC connected to the network through a three-phase coupling transformer

is 10 ms, 50Hz, half sine wave. Since it is only used within the fault condition, the initial junction temperature can be assumed to the ambient temperature; in this simulation, it is set at 40°C. The thyristor's maximum non-repetitive withstanding temperature during surge is 289°C, with T_{vj}=125°C and $V_{R\&D}$=0.6V_{RRM}; where $V_{R\&D}$ and V_{RRM} are the thyristor voltage after the surge current and the rated reverse blocking voltage, respectively.

Regarding the varistor, a metal-oxide, e.g. ZnO, varistor made by Littelfuse (V881BA60) is used. It can absorb 3200 J and endure 1 kA or 1.5 kA within a 1 ms- or 0.7 ms-pulse, respectively. Because the varistor is used for up to 1 ms (the required time delay for the relay to gate on the thyristors), the mentioned data shows its ability during this period. The limited energy capacity of a varistor means that it cannot be used alone to protect the SSSC. It is instead hybridized with the thyristor crowbars to work in the system. Similarly, a spark-gap, which is also intended for short pulses, is not by itself sufficient for the targeted application.

V. SELECTION OF THYRISTOR AND VARISTOR

Selecting proper thyristor and varistor is important for the effectiveness of the proposed protection scheme. A bad choice could lead to failure of the concept.

A) Selection of thyristor

The following aspects should be considered:

1. the maximum short circuit current level including the DC offset;
2. the maximum number of surge current pulses that the thyristor has to conduct;
3. the peak voltage that the thyristor has to withstand after fault clearance.

The making fault level of an 11 kV system is managed below 600 MVA, meaning that the maximum rate of current rise in the thyristor is about 14 A/μs (assuming 50 Hz). This can be easily satisfied and hence the main constraint will be the temperature rise of the device under the current surges. If the number of the current surge pulses to be carried by the thyristor increases, the amplitudes of the pulses have to reduce.

The maximum peak voltage determines the number of series thyristors in the crowbar. As an 11 kV system is usually neutral unearthed, two strings of thyristors should always withstand the peak line-to-line voltage, to work in different fault types.

Table 3: Network Properties

		Feeder 2	Feeder 1
Voltage level		11kV	11kV
Source fault level		250MVA	250MVA
Cable Impedance	Resistance	0.06Ω/km	0.06Ω/km
	Inductance	0.134mH/km	0.134mH/km
Cable length		10km	5km
Load		17MW	1MW
SSSC-Transformer		1100V_{DC}/800A-600kVA,1kV/1kV	
Varistor		880V (continuous), 2450V (clamping)	
Thyristor		1800V/1660A	

B) Selection of varistor

The procedure of selecting the varistor is as follows:

1. determine the clamping voltage of varistor according to the SSSC maximum peak voltage in normal condition;
2. determine the operating time of the varistor;
3. calculate the surge current through the varistor;
4. calculate the energy to be dissipated in the varistor.

VI. SIMULATION RESULTS

The parameters of the case study system are shown in Table 3 and a schematic of the three-phase SSSC is shown in Figure 9. The proposed method of protection is compared with an unsuccessful conventional protection method using mechanical switches.

A) Conventional protection method

Figure 1 has shown previously the structure of the conventional protection mechanism that only uses mechanical circuit breakers. In this case, it is supposed that a fault happens at t=1.58 s and voltages across the SSSC in phases A, B and C will reach the threshold voltage (0.5 × 2450 V) of the relays at 0.205 ms, 0.230 ms and 2.625 ms after the fault inception. 1 ms after that, relays will send the tripping command to the CBs which will then cut off the current after a further 20 ms. For instance, regarding phase A, the entire cutting off time is 0.205 ms+1 ms+20 ms. Figures 10 and 11 show the current and voltage of a closed-loop SSSC during the fault. The fault current level through the SSSC can rise to 7 kA which can severely harm the IGBTs. Moreover, the voltage overshoot is around 18 kV which can saturate the transformer, causing large core losses and differential relays to trip [30].

Regarding the calculation of IGBT module temperature, the converter and IGBT modules mentioned in Section II are used in this simulation and the initial junction temperature is about 90˚C, changing within a fundamental cycle. As can be seen in Figure 10, phase B has the highest peak current of 7 kA which exceeds the permissible surge current (6.6 kA). Subsequently, phase A current peak reaches to 6 kA which causes the temperature of the IGBT modules to exceed or become very close to the maximum allowable temperature 150°C as shown in Figures 12 and 13 for the worst cases. Figures 12 and 13 show

the temperature response of an IGBT (blue line) and PiN diode (orange line), as it can be seen that the temperature in these legs has exceeded 150°C for both the IGBT, and PiN diode chips, especially in cases where the CBs need longer time to get opened (three cycles or more), which is not shown here. It means that the conventional method is not fast enough to protect the SSSC.

B) Proposed protection method

In the second case, thyristor crowbars are used in shunt to the SSSC and a varistor is in parallel with the SSSC as shown in Figure 4. The voltage and current ratings of the SSSC semiconductors are 1700 V and 800 A respectively. Figure 14 shows the voltage across the SSSC and varistor, which are identical because they are in parallel. Figure 15 shows the SSSC current. Figure 16 shows the thyristor crowbar schematic.

In this simulated case study, a three-phase-to-ground fault occurs at t=1.58 s and the voltage across the varistor and SSSC increases immediately but is limited at the varistor clamping voltage, 2450 V (Figure 14). Varistors in phases B and C will be activated after 0.275 ms and in phase A after 2.275 ms. Therefore, until the thyristor crowbars are turned on, the varistor will pass the current through itself so as to limit the SSSC voltage and current; the transformer impedance will limit the current surge into the converter. During this period, the voltage of the varistor is similar to the SSSC, Figure14, and the varistor current is shown in Figure 17. Furthermore, the absorbed energy is around 700 J, as shown in Figure 18. It can be seen that the energy and also current are below the allowable limits so it can be claimed that the varistor temperature will certainly be lower than 125°C, its maximum allowable value. Voltages in phases A, B and C will reach the threshold voltage (0.5 × 2450 V) of relays at 0.095 ms, 0.230 ms, and 1.655 ms after the fault. Then after a further 1 ms, the required time for detecting the fault and sending the gate signals, the crowbars are turned on and then most of the fault current passes through them because of the thyristor's low turn-on impedance. For example, the required time to turn the thyristor on in phase A is 0.095 ms+1 ms. Figure 19 shows the thyristor current waveforms. As mentioned, the surge current is an indicator of the thyristor crowbar capability in tolerating the fault. Phase A has the highest surge current which also repeats twice for thyristor leg 1. The absorbed energy for this thyristor is calculated to be around 400 J.

Figure 20 shows the thyristor temperature response for phase A, legs 1 & 2, that are supposed to be the worst-case compared with other thyristors in the system. It can be concluded that no thyristor temperature will exceed its allowable limit. In parallel with thyristors' operation, after 20ms of detecting the fault, circuit breakers 1 and 2 are opened, and then the firing pulse is removed from the thyristor crowbars' gates in order to turn them off. It is worth mentioning that the required thyristor blocking voltage after the operation has a great effect on its

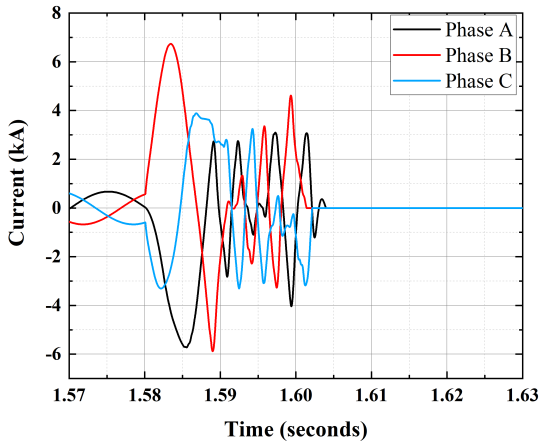

Figure 10: The fault current passing through SSSC- Conventional method

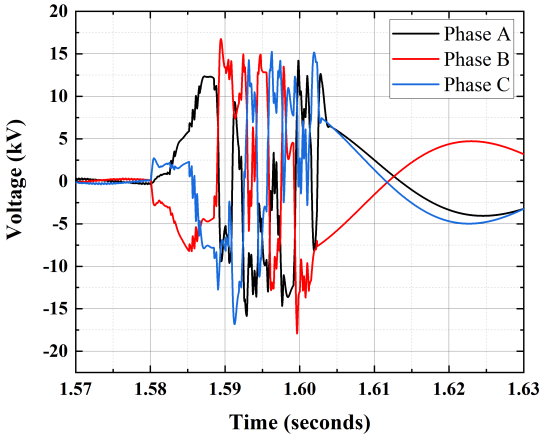

Figure 11: The voltage of SSSC during the fault- Conventional method

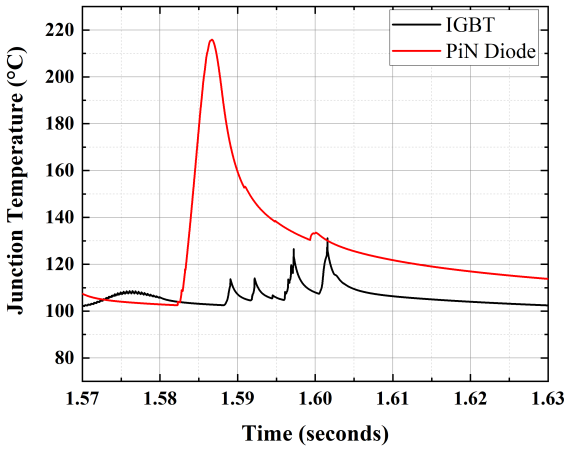

Figure 12: IGBT temperature in leg 1 top- Conventional method

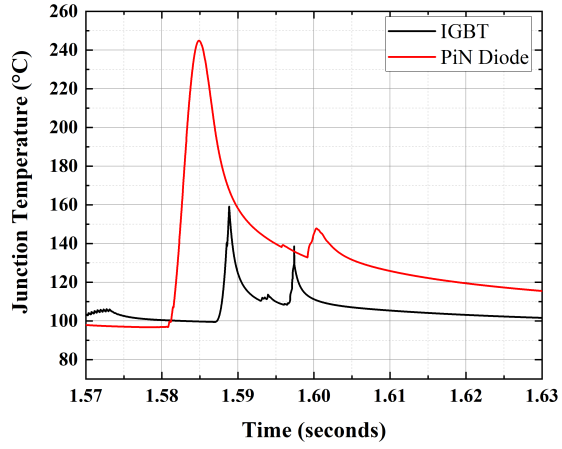

Figure 13: IGBT temperature in leg 2 bottom- Conventional method

surge-tolerance ability. As mentioned, after the surge current, the voltage is applied across the thyristor must be 0.6 V_{RRM} (0.6 × 1800 V). Therefore, in this case, since the voltage peak value is 9 kV, as shown in Figure 21, at least 9 thyristor crowbars for each phase are required in series. The thyristors turn on and turn off relatively slowly, in µs, therefore connecting thyristors in series, driven by the same gating signal, is much easier than IGBTs. Snubbers are usually used to assist dynamic voltage sharing, as in HVDC systems [34]. The pulse transformer and the optically coupled firing methods can also be used [35]. Moreover, the thyristor current DC offset duration which is generated during a fault is sufficiently less than one cycle (20 ms) in medium voltage networks and thus has no influence on the turning-off process of the thyristor crowbars [8].

Consequently, as it was expected the short circuit current passing through the SSSC is limited to 3 kA (peak value), Figure 15, which is less than half of the previous value (7 kA, peak value) and its duration is also reduced to only 4 ms, with rising time of 1 ms. Besides, the voltage across the SSSC as mentioned before is clamped by the varistor so that its value is limited to 2450 V compared to 18 kV in the previous case study.

Regarding the IGBT temperature, first of all, the maximum current passing through the devices is 3 kA which is much smaller than their maximum allowable surge current (6.6 kA). Also the phase B current is the worst case during this fault situation, so the temperature of IGBT module leg 2 (lower leg) will have the highest rise compared to other IGBTs and the result is shown in Figure 22. As expected, the PiN diode temperature is 128°C which is well below the 150°C limit of the module for either IGBT or PiN diode.

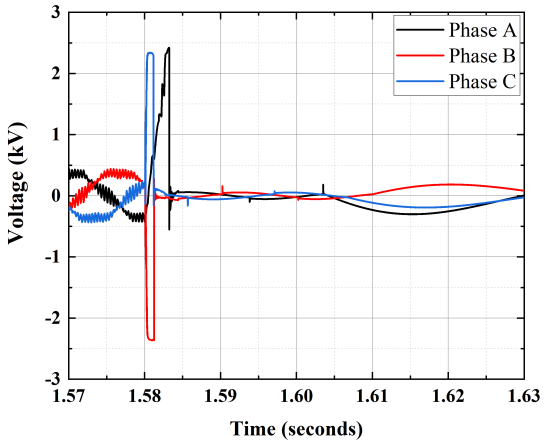

Figure 14: Voltage of SSSC & Varistor- Proposed method

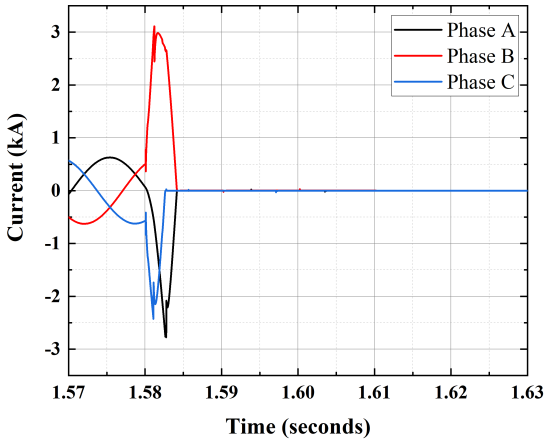

Figure 15: SSSC Current- Proposed method

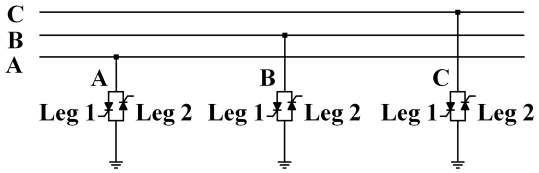

Figure 16: Thyristor crowbars schematic on one side of SSSC

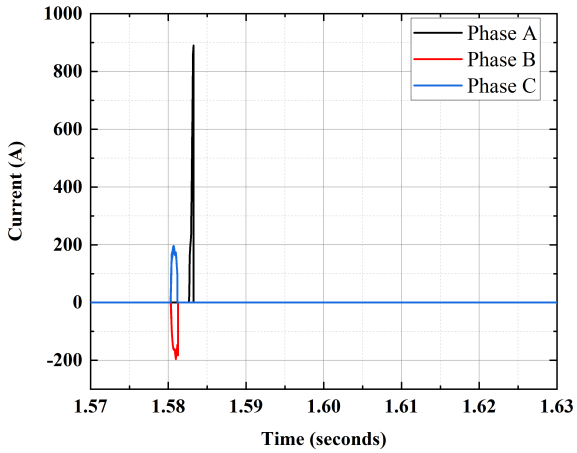

Figure 17: Varistor current- Proposed method

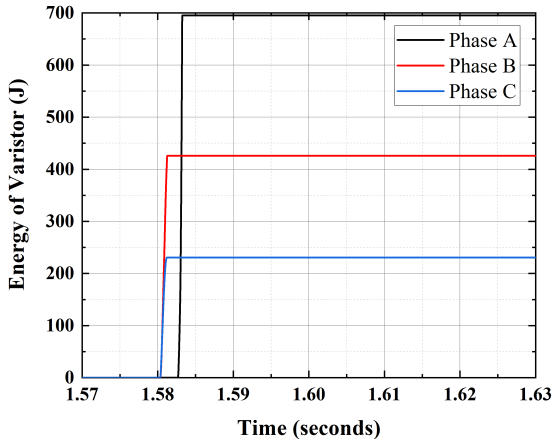

Figure 18: Varistor energy- Proposed method

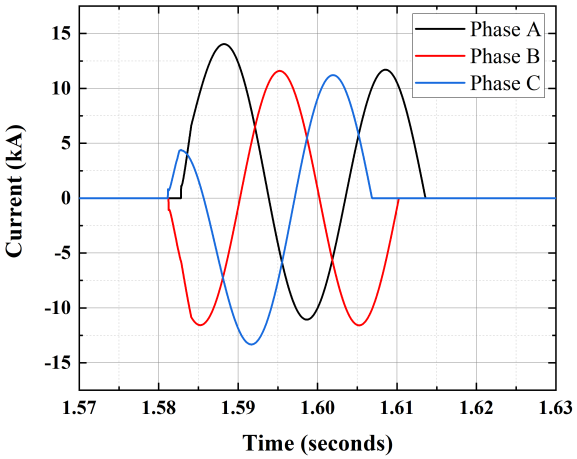

Figure 19: Thyristor current during fault- Proposed method

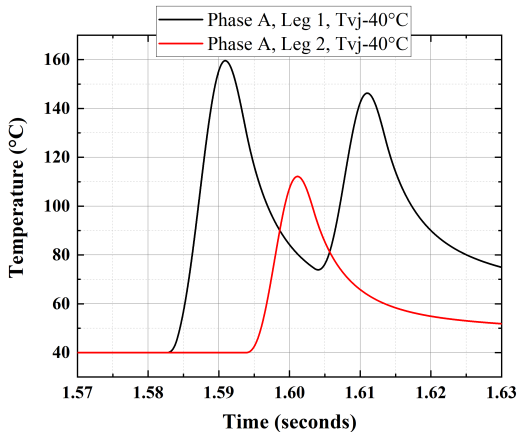

Figure 20: Thyristors' temperature in phase A- Proposed method

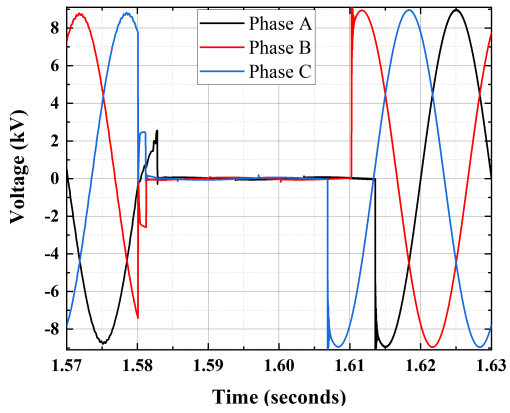

Figure 21: Thyristor Voltage- Proposed method

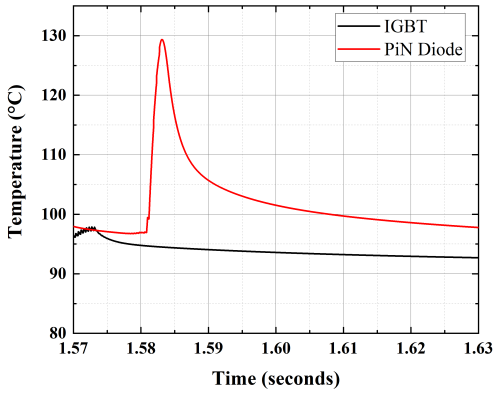

Figure 22: Temperature of IGBT in leg 2 bottom- Proposed method

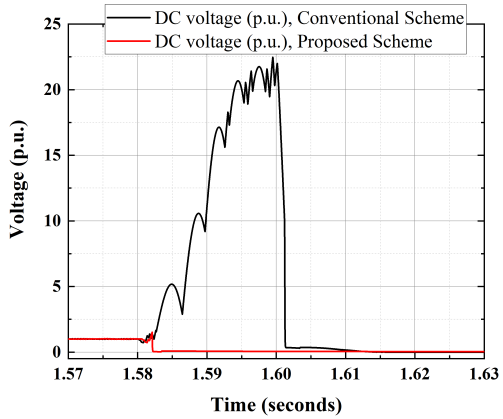

Figure 23: Capacitor voltage of the converter- DC side

Apart from the IGBT and PiN diode protection, the capacitor utilised on the DC side of the converter could be severely damaged during the fault if the protection system does not act fast enough. Figure 23 shows that the capacitor voltage could reach to 22 p.u. in the conventional protection scheme but by using the proposed method, it can be limited to 1.5 p.u. when the original DC voltage is 1100 V_{DC}.

VII. EXPERIMENTAL RESULTS

To demonstrate the protection concept, a scaled-down single-phase lab model has been considered as illustrated in Figures 24 and 25. However, in this case, instead of using two thyristor crowbars in shunt to the SSSC, one thyristor crowbar in parallel has been used. In fact, the difference between these two methods is the control of the short-circuit level at the fault point, meaning that by bypassing all current to the same side the fault level would now be almost twice.

A single-phase H-bridge voltage source converter is connected to the line via a 1:1 series-coupling transformer, which mimics the SSSC. A 230 V_{AC} 50Hz single-phase voltage source mimics the grid. A resistor bank is connected between the transformer and voltage source to create a relative phase shift [31, 32] at Bus 3 by passing the current through the interconnecting impedance. The measured voltages at Buses 1

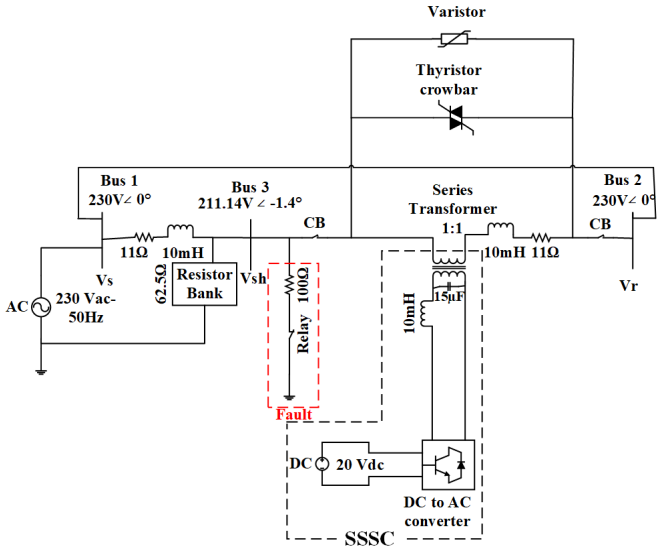

Figure 24: Single-phase protection scheme

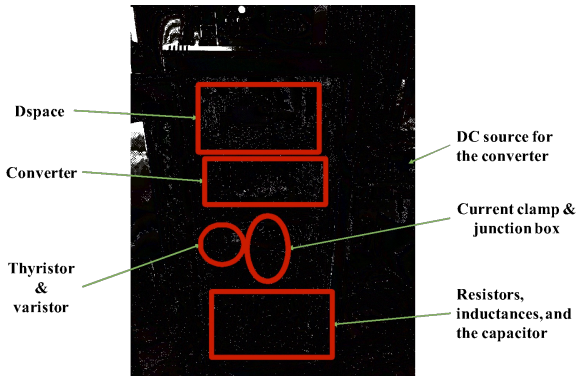

Figure 25: Laboratory prototype

and 3 are equal to $230\,\mathrm{V}\angle 0^{\circ}$ and at Bus 2 is $204.71\,\mathrm{V}\angle -2.48^{\circ}$ without the SSSC, and $211.14\,\mathrm{V}\angle -1.4^{\circ}$ with the SSSC.

A) Conventional protection method

In the absence of thyristor and varistor, a high-resistance fault happens in the network in order to check the current, voltage and temperature response of the converter. For monitoring the temperature, a thermocouple is applied to the converter heatsink to record the temperature variation. In this case, a fault happens at t=64 ms and then circuit breakers are opened after 20 ms. The obtained results are shown in Figures 26 and 27. The utilised IGBT in this test is SEMIKRON SK35GD126ET, and its heatsink temperature variations during the fault is shown in Figure 27.

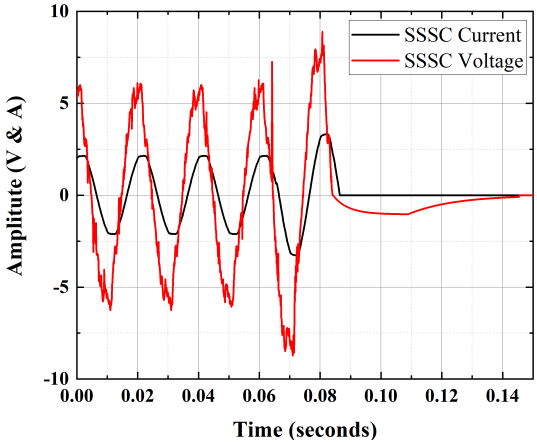

Figure 26: SSSC Voltage & Current- Conventional method

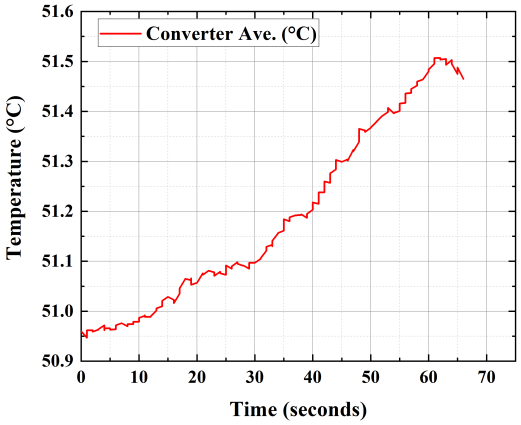

Figure 27: Temperature variation of IGBT- Conventional method

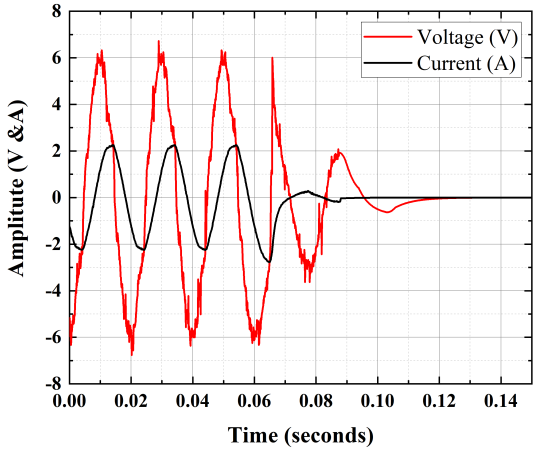

Figure 28: SSSC Voltage & Current - Proposed method

B) Proposed protection technique

In the second case, the varistor and thyristor crowbar are used to prove the effectiveness of the proposed technique. The used

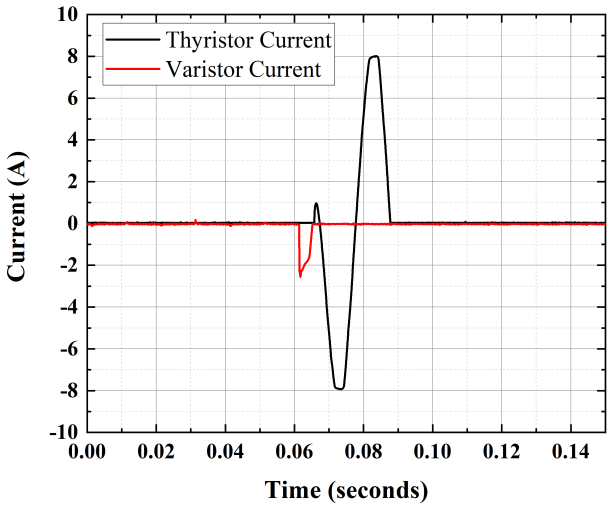

Figure 29: Thyristor & Varistor's Current- Proposed method

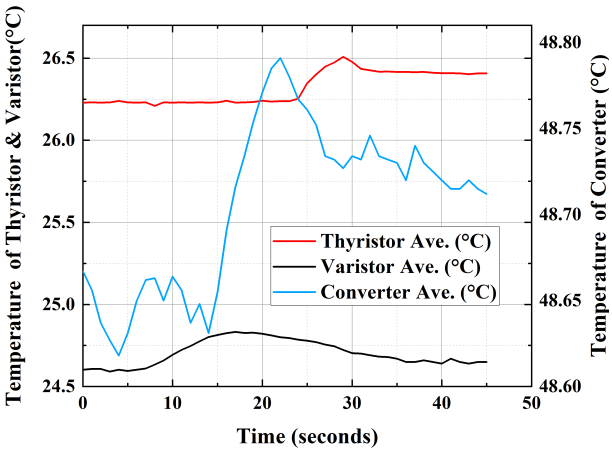

Figure 30: Temperature variation of IGBT, varistor & Thyristor- Proposed method

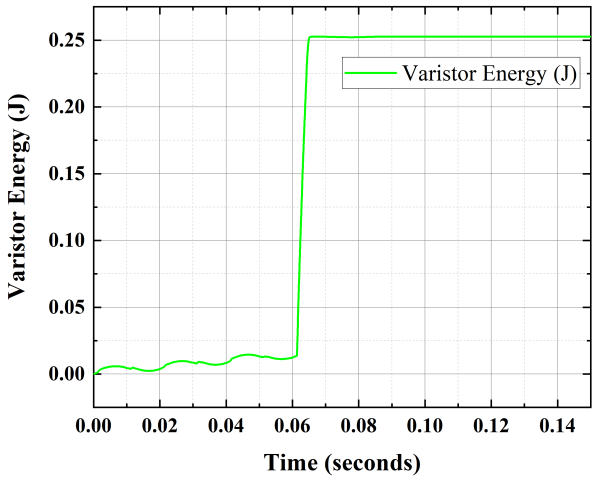

Figure 31: Varistor energy- Proposed method

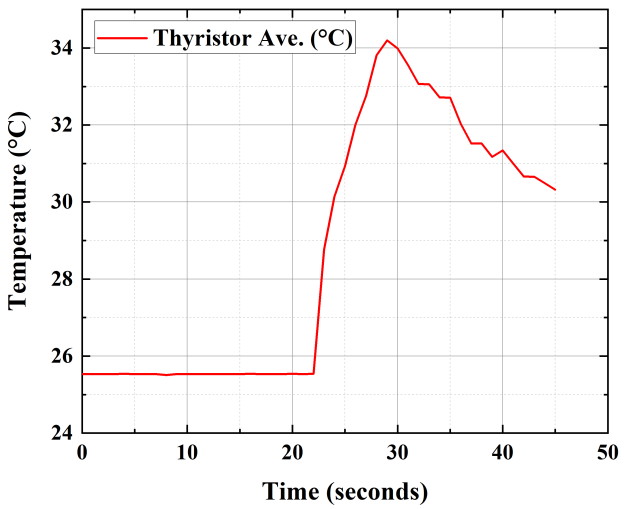

Figure 32: Thyristor temperature response- Proposed method

thyristor crowbar and varistor are SEMIKRON SKKT 273 and TDK metal oxide varistor B72210S0140K101. In this case, fault happens at t=64 ms, and after 2 ms delay, the thyristors are gated on. During the 2 ms, the varistor will limit the voltage across the SSSC, providing a path for the fault current. After 20 ms, the CBs interrupt the current. For measuring the temperature, a thermal copper is again connected to the converter heatsink, thyristor crowbar heatsink and varistor body. The results are presented in Figures 28 to 31.

These experimental results indicate that the proposed technique can reduce the temperature variations of IGBTs within the safe operating range. Although in Figure 27 the case temperature is not changing significantly, in comparison with Figure 30, by cutting off the current passing through the converter, it can be seen that the temperature increase, Figure 30, has been considerably reduced. Moreover, the voltage variations of the SSSC, as shown in Figure 28 is well controlled by using the proposed technique compared to Figure 26 corresponding to the conventional method. Also. Figure 31 shows the varistor energy absorption that is very low.

In roder to analyse the temeprature behaviour of the thyristor during the fault more accurate, the test has been repeated with a smaller thyristor pair (Philips BT151) with a lower current rating. In this case, the temeprature variation of the thyristor becomes significantly higher as shown in Figure 32. Due to limitation of our laboratory, the experimental work has not been conducted towards the limit of the devices.

VIII. CONCLUSION

Although SSSC has significantly higher efficiency during normal operation and an exceptional performance-cost ratio, its application is restricted due to its currently poor ability to survive network fault conditions. In this paper, a protection scheme has been proposed and its behaviour verified by simulation and demonstrated by experiment. The circuit consists of parallel thyristor crowbars that draw the fault current and a varistor, which limits the voltage rise across the SSSC before the thyristors are turned on. Simulation results show that the voltage across and current through the SSSC are controlled during the whole fault event. Components can be realistically selected for an SSSC in an 11 kV network. The SSSC's IGBT module temperature is maintained below its maximum operating temperature. In addition, the proposed protection scheme is also safe from temperature rise and transient over-voltage points of view.

The simulation and experiment have focussed on symmetrical three-phase faults. But the number of series devices and their voltage ratings are selected such that the proposed scheme can also work in other grid fault types. Series connection of thyristors has been made in industry with the help of snubbers for dynamic voltage sharing. It is expected that the study could provide a stepping stone towards commercial development of SSSC and its protection schemes for medium voltage grids which are under pressure for accommodating more low carbon distributed generation.

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