A 32x32 ISFET Sensing Array With In-Pixel Digitization And Column-Wise TDC For Ultra-Fast Chemical Sensing

***Abstract*—This paper presents a 32x32 ISFET sensing array with in-pixel digitization. By driving a common-control signal with a triangular waveform, the pH response of the ISFETs are converted within a fixed timing window, while dynamic range is enhanced in the time domain to tolerate sensor offset. A 15 bit asynchronous column-wise time-to-digital converter is implemented, which enables fast sensor readout with minimal silicon area. Parallel output of 32 TDC interfaces are serialized for fast data though-put. This system is implemented in a standard 0.18um standard CMOS technology, with a pixel size of 26um x 26um and a TDC of 26um x 180um. Simulation results demonstrate that chemical sampling of 5k frames per second is achievable with a clock frequency of 160MHz and a TDC resolution of 190pS. The total power consumption of the overall system is 7.34mW.**

I. Introduction

Within the last decade, we have witness the significant impact of micro-fabrication and microelectronics in biomedical applications, such as electro-chemical lab-on-chip devices, neural interfaces and DNA sequencing platforms [1]–[3]. Large-scale arrays with miniaturized sensors or electrodes can be implemented in reliable processes with low fabrication cost, and integrated low noise analogue front-ends with direct conversion for further processing in the digital domain. These technologies enable integration of large-scale lab-on-chip platforms, which reduce the sensor interface parasitics, improve the sensitivity, but also provide rapid and parallel sensing for diagnostics and instrumentation purposes.

Among these, Ion-Sensitive Field Effect Transistors (ISFETs) as a class of CMOS-compatible potentiometric chemical sensors, have been extensively studied and implemented for DNA sequencing or SNP detection [2], [4]. Owing to the decreasing feature size which enables large scale arrays, millions of μm-size ISFETs can be integrated into a mm-size silicon chip, with full on-chip interfacing and processing circuitry [2], [5]–[7]. High density integration of ISFETs in CMOS greatly reduces the cost, but also introduce design challenges for scalability of the sensor interface [8].

Conventional analogue-based ISFET readouts have limitations in scaling due to the circuit complexity needed to compensate non-idealities and speed as a result of parasitics [9]. Therefore in-pixel biasing and sensing circuitry are limit small pixel sizes for large-scale arrays. APS based readouts simplify the in-pixel structure and rely on the CDS to readout sensor output and reduce mismatch [6], [7], [10]. These essentially convert the voltage on the floating gate to current, whilst charging the sampling capacitor via a source-follower or common source configuration, introducing however speed limitations and non-linearity. Moreover compensation schemes for sensor offset are usually performed via resetting the floating gate voltage or biasing reference electrode, which provides difficulties for continuous monitoring with fully on-chip biasing [6], [7], [11].

On the other hand, a complete time based ISFET readout provides possibility for ultra-minimal sensor readout and overcomes speed limitations. However the PWM output, generally used in these readouts, needs special consideration for readout synchronization, and parasitics due scaling to a large array and large sensor offset should be considered and compensated [12].

In this paper, we introduce a compensation scheme and design considerations for a fully time-based ISFET array. In the proposed scheme, a sensor pixel was designed to compensate $\pm 5V$ sensor offset with a 0.01pH resolution. To convert the PWM output, an asynchronous 15 bit time-to-digital converter is designed to provide fast and direct sensor output conversion. A 32 x 32 sensor array was implemented with a maximum sampling rate of 5k frame per second. Due to the fully digital configuration both interface and sensors can be aligned, allowing scaling for larger and faster array implementations.

This paper is organized as follows: Section II describes the design considerations for offset compensation and fast chemical readout in the pH-To-Time sensor interface; Section III explains the asynchronized TDC; Section IV shows the system implementation; Section V provides simulation results followed by a conclusion in Section VI.

II. pH-Time sensor for fast sampling

An ISFET is essentially a potentiometric sensor, in which the sensed potential directly relates to the ion-concentration [13] of the pH solution it is measuring. Most readout circuits rely on the transconductance of the ISFETs from the floating gate to form basic amplifiers, i.e. common-source, source follower as shown in Fig.1 [a,b,d]. The conversion from sensed floating gate voltage to current or even to voltage again could introduce extra noise or mismatch sources, and requires a careful compensation scheme for both sensor and readout offset.

However ISFETs in unmodified CMOS are essentially a floating gate devices. This introduces new understanding to the pH-Time converter in [12], shown in Fig.1 [d]. The signal in

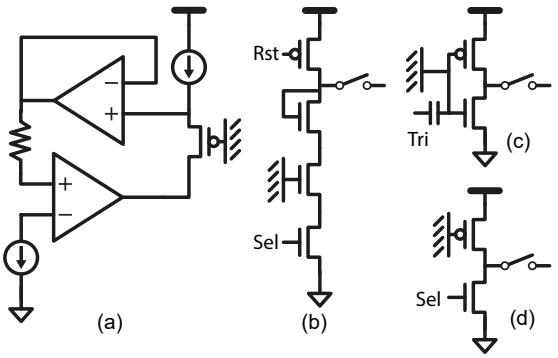

Fig. 1. Typical ISFETs readout circuits: (a) Source drain follower [13]; (b) time based readout with current discharging output nodes [6]; (c) PWM based interface with time output [12]; (d) in-pixel common-source configuration with external interface [10].

the sensing membrane of ISFETs, i.e. one of the control gates, is capacitively compressed to the floating gate. This increase the dynamic range of the sensor if the noise of transistor is well below the sensor noise [8]. Moreover, this capacitively coupled floating gate inverter performs level-crossing based comparison on the floating gate via the capacitors, which exhibits lower mismatch and non-linearity.

The floating gate voltage of the ISFET can be defined as [8]:

$$V_{FG} = \frac{C_{pass}V_{chem} + C_{pg}V_{pg} + C_{gd}V_{out}}{\sum C_{FG}} + k \qquad (1)$$

Where C_{pass} is the equivalent capacitance for chemical and passivation interface, V_{chem} is the chemical potential induced by the ion concentration, C_{pg} and V_{pg} are the capacitance and voltage for the programmable gate, C_{gd} and V_{out} are the total equivalent gate drain voltage and drain voltage, k is the DC term including the reference voltage, trapped charge in both passivation and floating gate, and parasitic influence from source voltage, and $\sum C_{FG}$ is the total capacitance seen at the floating gate node [8]. To simplify analysis, C_{gd} is assumed to be constant. This can be realized by a fast changing V_{pg} with large amplitude.

With reduced size of sensors and thickness of gate-dioxide for a smaller technology node, parasitic capacitance in transistors become more dominant and attenuate the chemical signal. The source-drain follower was normally used to reduce the parasitic effects and necessitate many transistors in the in-pixel readout [9], [13]. However for pH-To-Time readout in ISFET inverters [12], with parasitics included the pulse width output can be defined by two transitions of the output, i.e. falling and rising:

$$\begin{aligned} T_{out} &= T_{0\to1(V_{FG}<V_M)} + T_{1\to0(V_{FG}<V_M)} \\ &= \frac{T_{trig}C_{pass}}{V_{rr}C_{pg}}V_{chem} + \frac{T_{trig}}{V_{rr}C_{pg}}k + \frac{T_{trig}C_{gd}}{V_{rr}C_{pg}}V_{dd} \end{aligned} \qquad (2)$$

Where V_{rr} is the rail voltage of the triangular signal, V_{dd} is the supply voltage of the inverters, V_M is switching point of the inverters [12].

It should also be noted that the following condition should be fulfilled:

$$\begin{aligned} \frac{V_{rr}C_{pg}}{C_{fg}} &> V_{dd} - NM_n - NM_p \\ V_{FGmin} &< NM_n \\ V_{FGmax} &> NM_p \end{aligned} \qquad (3)$$

Where NM_n and NM_p are noise margin for the inverter [14].

Compared to other readout schemes, this one relies on the capacitive ratio and DC operation condition of the transistors, therefore high-linearity can be achieved, moreover, the transition, i.e. where the chemical signal get sampled, is driven by the switching of the transistors at the maximum transconductance point, therefore, the noise of readout can be further be minimized. Last but not least, the power consumption of array can be easily estimated by:

$$P_{array} = n * Fps * (C_{out}V_{dd}^2 + C_{pg}V_{rr}^2) \qquad (4)$$

where n is the array size, and Fps is the frame per seconds for the entire array.

Compared to analysis from previous work [12], [15], Eq (1),(2),(3) emphasis the effect of the parasitics, and indicates that with smaller devices, the chemical readout is only related to the period, amplitude of triangle signal and ratio between the passivation capacitance and the programmable gate capacitance. The parasitic capacitance and offset are presented as DC offset of the pulse width. Moreover, the output induced parasitics behave as hysterisis, with the window size defined by the supply voltage of the inverters and C_{gd}, and only introduce a DC offset for the time signal output. Certain design considerations should be taken in order to create a clear transition and prevent the inverter from saturation, i.e. fully on or fully off as in Eq.(3).

III. Asychronous TDC

Previous TDCs used in ISFET interfaces rely on the synchronized triggering signal [6], [7], [15]. However due the nature of the level crossing, the transition of the pixel output can not be synchronized to a clock. Using a fully delay line based configuration requires large silicon area and power consumption. In this work, an asynchronized TDC for ISFETs output is proposed, as shown in Fig.2

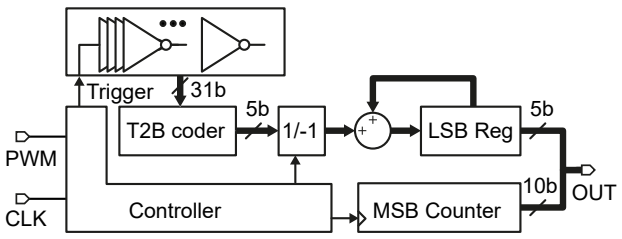

Fig. 2. TDC Structure

A. Resolution requirement

To accommodate large DC offset and parasitics induced by the output swing, without reducing the resolution of the pH sensing, the required TDC resolution should be defined by:

$$n_{TDC} = \frac{(kC_{FG} + V_{dd}C_{gd})}{\alpha pH_{min}C_{pass}} \tag{5}$$

where α is the coefficient for Nernstian sensitivity. This suggested that with a smaller sensing membrane, and large parasitics C_{gd}, the dynamic range of the TDC has to be large enough to recover small chemical signal.

By assuming the offset referred to the reference electrode is $\pm$ 5V with all the capacitance extracted from the sensor pixel layout, the resolution of the TDC should be larger than 12 bits, to achieve 0.1pH resolution. Considering linearity of the TDC and possible offset of the transistors, a 15-bits configuration was chosen. Therefore the pH resolution of this scheme is given by:

$$pH_{min} = \frac{C_{pass}}{2^{10}V_{rr}C_{trig}}\alpha \tag{6}$$

B. Course and Fine conversion

To reduce the total area, a coarse-fine structure is used to implement the multi-bit TDC [15]. In this design a 10 bits coarse converter was designed using a 10-bits asynchronized counter to reduce the total number of logic gates, and the fine converter was based on a 31-stages current starved delay line. The delay was controlled by global voltage biasing, generated by external current source. These enable a wide-tunning for the LSB of the TDC from 180pS to 9.5nS with clock for counter ranging from 3.2MHz to 164.8Mhz. The mismatch between the LSB of the coarse converter and the dynamic range of the fine converter, is adjusted externally by tunning the reference current input or the clock of the counter.

C. Asychronous Logic

Since the edge of the PWM waveform is not aligned to the clock synchronization, the control logic of the TDC will detect and divide the PWM signal to three parts and initialize conversion by using either coarse or fine conversion. A detailed conversion timing diagram is shown in Fig. 3

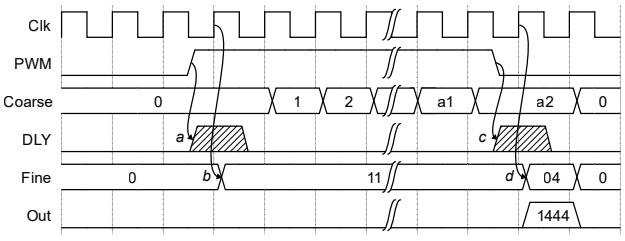

Fig. 3. Timing diagram of TDC

Once a rising edge of PWM is detected at time a, the controller will pass the rising edge to the delay line and initialize the edge propagation; the screen shot of the delay line status, i.e. the timing information, will be captured by the next clock rising edge at b; from b the counter will be enabled and increments every rising edge of clock, until PWM falls; the falling edge of the PWM at time of c will be inverted and fed into delay line again; the delay line value between the PWM falling edge c and immediate next rising edge d of the clock will be captured and substracted from the pre-stored $T_{a\to b}$; the value stored in the MSB counter and LSB register($T_{a\to b} - T_{c\to d}$) will be combined to give valid output results of 16 bits (10bits unsigned and 6 bits signed).

1) Scalability of the TDC: The proposed inverter delay line can be replaced by a standard delay line with minimum sized inverters if a smaller and fixed LSB value is desired. This fully digital implementation can be easily scaled according to different sampling speed and area requirements. The frame sampling speed is limited by the dynamic range of the TDC, also related to frequency of triangle signal:

$$\begin{aligned} Fps &= \frac{n_{row}}{T_{trig}} \\ &\leq \frac{n_{row}}{LSB \times DR} \end{aligned} \tag{7}$$

where n_{row} is the number of row elements, DR is the dynamic range of TDC and is related to the number of bits as defined in Eq.(5), and LSB is the minimum propagation delay in the delay line, and can be scaled to pS level when advanced technology is used. This suggested that a sampling rate of kilo-frames per second can be achieved in large arrays. Moreover the physical implementation of the TDC is only limited by the pitch size of the digital core cells, therefore makes colomn-wise implementation is feasible even for pixels with μm high.

IV. System Implementation

A. Overview

The system diagram is shown in Fig.4, which is divided into three parts: 1) A 32x32 sensor array with in-pixel digitization generates 32 bit digital pulse width output ; 2) 32 column-wise 15bit coarse-fine Time to digital converters directly convert the pulse width to a parallel digital output; 3) 32 x 15 b digital output are fed in parallel to top level digital controller for a parallel-in-serial-out interface. The top level logic was shared with other test circuits and synthesized into a single block. The system is implemented in a typical $0.18\mu m$ CMOS technology, with layout dimension shown in Fig.5.

B. Sensor pixel

The inverter based sensor pixel is based on a tri-state inverter. The common gate the inverter is raised to the top metal plate with size of 22x22 μm^2, which acts as the base of the sensing membrane. A MIM cap of 40fF was used as the programmable gate. The output of the inverter is followed by a transmission gate, which is controlled by the row selection signal. Output from all the pixel within the same colomn are joined together and connected to the colomn-wise TDC. The pixel layout can be found in Fig.5.

TABLE I
COMPARISON OF ISFETS SENSING ARRAY

Specifications	This work	[10]	[7]	[11]	[6]	[5]	[16]
Process	0.18	0.35	0.18	0.35	0.35	0.35	0.35
Supply (V)	1.8	3.3	3.3	3.3	3.3	3.3	3.3
Frame rate	5000	100	1250	9.3	0.75	7.8	3000
Offset Compensation	$\pm$ 5	N/A	Yes	Yes	Yes	Yes	Yes
pH resolution per bits	0.01 [a]	N/A	0.1 - 0.025	0.066	0.019	0.101	N/A
Array size	32 x 32	64x64	64x64	32x32	78x56	64x200	128x128
Sensor sizeμm^2	22 x 22	N/A	22.3	N/A	N/A	6.5x7.8	18x12.5
Pixel sizeμm^2	26 x 26	10.2x10.2	10x10	50x50	37x31	6.5x7.8	18x18
Entire Area	0.9	0.49	12.5	6.345	8	1.9	5.72
Sensor Pixel Power Consumption uA	0.01[b]	16	N/A	0.6	Varing	0-200	Varing
Total Power Consumption mw	7.34@4K	N/A	32@100	10.12@9.3	7.5	N/A	N/A

[a] Linearity ignored.
[b] Average Power consumption within 1 sample.

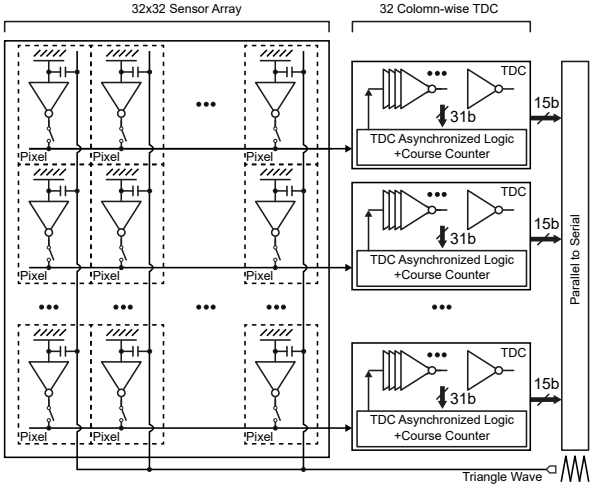

Fig. 4. Overview of the sensing system with inverter based sensing pixels and colomn-wise asynchornized coarse-fine TDC.

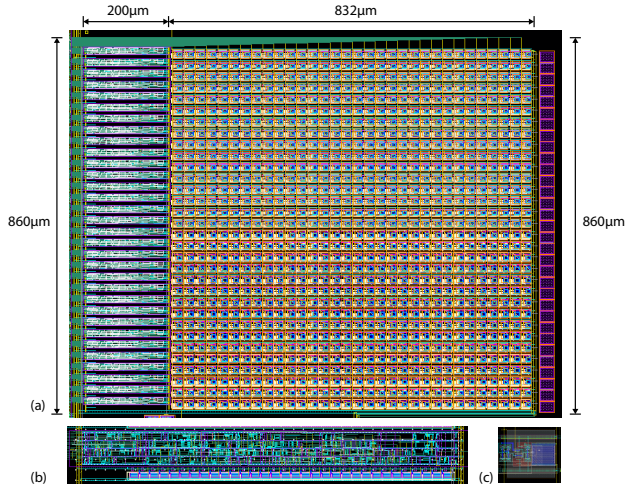

Fig. 5. Layout of the implemented system excluding the top level shift register for serial outputs, a) Entire system with size of 860x1032μm^2, b)TDC with size of 26x200μm^2, Sensor pixel with size of 26x26μm^2

V. SIMULATION RESULTS

The simulated performance of TDC is shown in Table.II and the specification of the entire system presented in Table.I. It should be noted that compared to previous works, the proposed system can be mostly synthesised to analyse the influence of parasitics, and the simulated results for both sensors and TDCs are mostly digital. The distribution of the delay interval for delay lines under different biasing conditions was analyzed by using Monte-Carlo simulation. The mismatch between different stages is well below the LSB or minimum chemical sensitivity required.

TABLE II
TDC PERFORMANCE

Specifications	Values
Supply (V)	1.8V
Clock frequency	3.3MHz - 163MHz
TDC resolution	15
TDC LSB	$\pm$ 9.54n - 190p
TDC DR	$\pm$ 67dB (Mismatch included)
TDC size	26 x 196
TDC Power Dissipation (uW)	159@100MHz

VI. CONCLUSION

In the paper, we presented a 32x32 ISFET chemical sensing array with asynchronized column-wise time to digital converters. With direct pH-to-Time conversion and digital pulse width output, the sensor interface can be greatly simplified. The Design consideration for fast sampling in deep-sub micron technologies is discussed. The asynchronous TDC structure simplifies the pulse to digital conversion, provides faster conversion and more dynamic range compared to previous works. The entire system is implemented in a 0.18 μm CMOS process. Overall a 5000 frame per second was achieved in simulation, with a minimum pH resolution of 0.01.

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