A robust ISFET pH-measuring front-end for chemical reaction monitoring

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***Abstract*—This paper presents a robust, low-power and compact ISFET sensing front-end for pH reaction monitoring using unmodified CMOS. Robustness is achieved by overcoming problems of DC offset due to trapped charge and transconductance reduction due to capacitive division, which commonly exist with implementation of ISFETs in CMOS. Through direct feedback to the floating gate and a low-leakage switching scheme, all the unwanted factors are eliminated while the output is capable of tracking a pH reaction which occurs at the sensing surface. This is confirmed through measured results of multiple devices of different sensing areas, achieving a mean amplification of 1.28 over all fabricated devices and pH sensitivity of 42.1mV/pH. The front-end is also capable of compensating for accumulated drift using the designed switching scheme by resetting the floating gate voltage. The circuit has been implemented in a commercially-available 0.35 μm CMOS technology achieving a combined chemical and electrical output RMS noise of 3.1mV at a power consumption of 848.1 nW which is capable of detecting pH changes as small as 0.06 pH.**

***Index Terms*—ISFET, reaction monitoring, pH sensor, chemical sensor, sensor array, DNA**

I. Introduction

ISFETs (Ion Sensitive Field Effect Transistors), introduced in 1970, are ion-selective chemical sensors that have recently been adopted in various lab-on-chip and health-care applications [1] [2], due to their potential for large-scale integration in addition to fabrication using an unmodified CMOS process [3]. Being derived from a simple MOSFET using an extended gate to the top passivation layer as illustrated in figure 1(a), has allowed for sensor scaling and integration density to be dictated by Moore's law as with any semiconductor process. In particular, this has shown great promise in next generation semiconductor based DNA sequencing technology, where over millions of ISFETs sensors have been integrated on a single chip capable of pH detection without the need for bulky optics, to sequence a human genome quickly and affordably [4] [5].

ISFETs fabricated in CMOS, however, experience similar challenges to the floating-gate MOSFETs from which they are made, both suffering from the trapped charge induced DC offset and attenuation of the input due to capacitive division of the transconductance by the floating gate capacitor, the effects of which are shown in figure 2. As reported in [6], a threshold voltage variation of $-1.32\ V$ due to trapped charge and a loss of half transconductance efficiency (g_m/I_D) were observed. Additionally they suffer from severe drift due to the non-ideal nature of the passivation which also degrades the sensor performance [7]. This is especially problematic when long-term measurement is required as it has been reported to vary from $1.5\ mV$ to $8.5\ mV$ per hour in CMOS [8].

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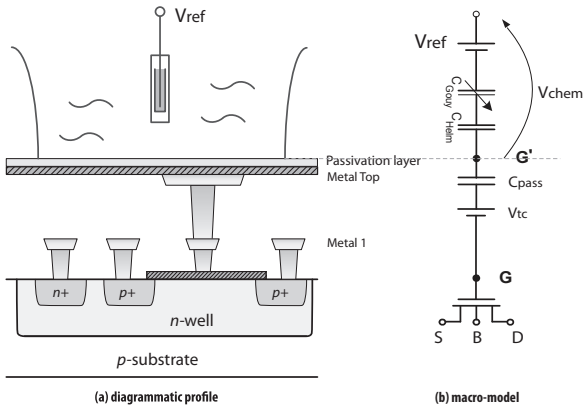


Fig. 1: Illustration of an ISFET in an unmodified CMOS technology and its macro-model

All these non-ideal characteristics which exist can be difficult to compensate because of their random and inconsistent nature. For removing trapped charge in the device, ultraviolet (UV) radiation has been widely used, but this requires an external source for compensation [10]. Other reported methods such as applying bulk-substrate bias to change the conduction and valence band levels or using the Programmable-Gate technique requires relatively bulky auxiliary circuits and also sacrifices sensitivity [10], [11]. To compensate for the loss in transconductance due to the capacitive division between passivation capacitor and gate-source capacitor, a constant-voltage-constant-current (CVCC) readout has been used which bootstraps the capacitor, but this requires at least two more amplifiers [12], [13]. Another interesting approach using a switched-capacitor amplifier (SCA) has also been used, but

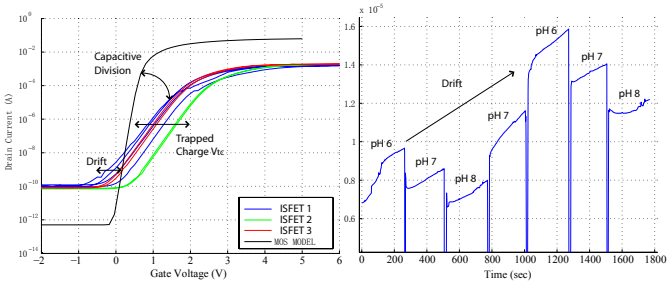


Fig. 2: Non-ideal effects present in CMOS based ISFETs [9]

requires a complicated clocking scheme [14]. Reduction of sensor drift due the passivation surface has also been shown [15], but this requires a differential structure consisting of an ISFET and a reference in separate chambers.

In this paper, we propose a novel, compact and low-power ISFET front-end readout circuit which through direct capacitive feedback, is capable of compensating issues of trapped charge, pixel offset voltage, and capacitive division of the input signal, which until now have made ISFET application in sensor arrays challenging. The application of the proposed interface is for reaction monitoring, tracking changes in pH to confirm positive reactions in ISFET arrays. The paper is organised as follows: Section II introduces the structure of the proposed readout circuit and analysis of it's functionality. Subsequently in Section III, we show its fabrication in CMOS followed by the experimental validation in Section IV proving it's capability when integrated in a lab-on-chip platform. We conclude with a discussion on it's future potential.

II. A NOVEL ISFET READOUT CIRCUIT

A. The ISFET model

The ISFET macro-model is shown in figure 1(b), which comprises of the MOSFET plus the associated passivation capacitance, C_{pass} formed by the contact of the top metal sensing layer with the pH sensitive insulator (Si_3N_4 in unmodified CMOS), and the chemical double layer capacitance comprised of the Gouy-Chapman, C_{Gouy}, and Helmholtz, C_{Helm} capacitances [6]. The passivation capacitor C_{pass} always tends to be a more than an order of magnitude smaller and thus the dominant of the three. The effects of trapped charge in the insulator or floating gate causing an offset voltage are represented by V_{tc}.

The pH[1] dependancy of the ISFET is described by the chemical potential V_{chem} which can be grouped with the reference electrode voltage, V_{ref}, and trapped charge effects, V_{tc}, to give a simplified equation for the floating gate voltage $V_{g'}$ as [6]:

$$\begin{aligned} V_{chem} &= \gamma + \frac{2.3\alpha kT}{q} pH \\ V_{g'} &= V_{ref} - V_{chem} - V_{tc} \end{aligned} \tag{1}$$

where γ comprises of all non-chemically related potentials, α is a scaling factor ranging from 0 to 1 describing the reduction of sensitivity from the ideal nernstian response and k, T, q represents the Boltzmann constant, absolute temperature and electrical charge of the electron respectively.

B. System Analysis

We use direct feedback to the gate to form a compact topology which can deal with the issues of trapped charge and division of transconductance due to passivation capacitance. Figure 3 shows the structure of the proposed interface, where MP_0 is the transistor used as the ISFET and C_p is its passivation capacitor. The switch S_0 is a low-leakage switch which allows the system to have resetting and sensing phases.

[1] pH is a measure of the hydrogen ion activity $pH = -log[\alpha_{H^+}]$ whereby $[\alpha_{H^+}] \approx [H^+]$ for dilute solutions.

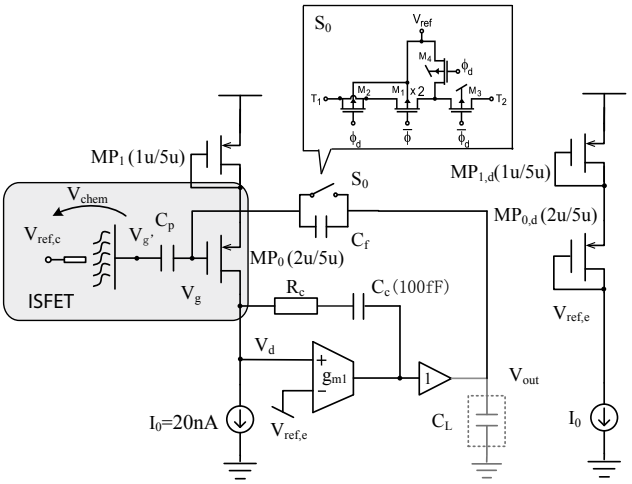


Fig. 3: Schematic of the robust ISFET interface

By adopting this structure, an average leakage of $45\ aA$ can be achieved [16].

The principle of the operation is that the gate voltage of transistor MP_0, V_g, is always locked to a certain value which makes the drain voltage of MP_0, V_d virtual ground to the negative input of the OTA through feedback. As a result when the switch S_0 is closed, which is the resetting phase, the output signal is always fixed to a specific value regardless of value of chemical reference $V_{ref,c}$ and the amount of trapped charge on the passivation capacitor; in the sensing phase however, S_0 is opened and the feedback is now established through the capacitor C_f. Hence, to lock the gate voltage according to the capacitive weighting between the passivation and feedback capacitors, the output voltage will compensate the voltage variation due to a pH change. This results in the output voltage V_{out} always oppositely tracking the chemical change from a fixed reference. Assuming the chemically dependant voltage V_{chem} to be the input, the DC gain due to the capacitive weighting can be derived as:

$$A_{dc} = \frac{C_p}{C_f} \tag{2}$$

Additionally, because all of the four terminals of the ISFET transistor MP_0 are locked to fixed values, it works in a similar fashion to CVCC readout, making it immune to any capacitive division which effects the transconductance.

C. Simulated System Operation

The circuits functionality during chemical reaction monitoring is depicted in figure 4. We used retrospective data from a pH reaction acquired from two ISFET sensors, separated by a DC offset of 20 mV due to trapped charge. Shown is the output response of two readouts interfaced to these two ISFETs. For the resetting phase (ϕ_1, S0 turned on) we see that both outputs are locked to a fixed potential reference of 1.75 V. Then during the sampling phase (ϕ_2, S0 turned off) both successfully track the chemical reaction, immune to the effects of any trapped

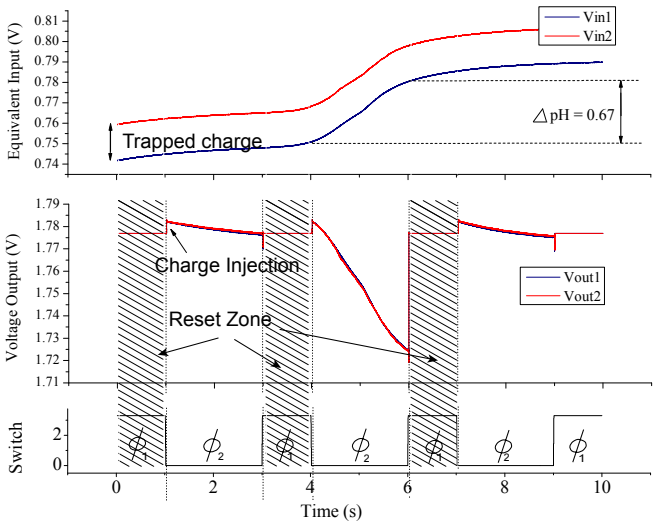


Fig. 4: Transient response of the system in two different phases

charges and pixel offset. Furthermore, by using this switching scheme we can guarantee the output will always begin from a fixed reference, which is set during phase ϕ_1 indicated as the reset zone in figure 4, avoiding issues due to ISFET voltage drift.

This approach provides a difference in value from the previous sample rather than an absolute, which has advantages in allowing resetting to a fixed potential and compensating for drift. The reference value of measurement is therefore always the starting pH value, and from this the total change in pH can be deduced. This makes it ideal for monitoring chemical reaction changes rather than absolute values which is suitable for applications involving DNA hybridisation. The absolute pH however can always be deduced if needed in these applications as the initial pH of the sample is always known because it is set to the ideal conditions for the DNA reaction to take place [17].

D. Stability analysis

The first thing to note is that we add a buffer after the OTA to drive the feedback capacitor. It not only simplifies the stability analysis due to its uni-directional signal path, but also increases the drivability for potential scaling of the ISFET array to a larger system which brings large load capacitance to the output stage. We proceed to analyse the transfer function of the system in sensing phase only, as in the resetting phase, the circuit forms a well known simple two-stage amplifier.

Although the real input of the system is at the floating gate, we shall break up the feedback loop at the drain of transistor M_{P0} to analyse the systems stability, using the model shown in figure 5 where g_{m1} is the transconductance of the feedback OTA and g_{m2} is the transconductance of the ISFET. Y represents the electric admittance of all components, with Y_f, Y_p and Y_C , representing the feedback capacitor C_f, passivation capacitor C_p and the compensation capacitor C_C and resistor R_C connected in series respectively. Additionally, Y_{L1} and Y_{L2} represent the parallel combination of the output impedance and capacitive load of the OTA and ISFET respectively. The

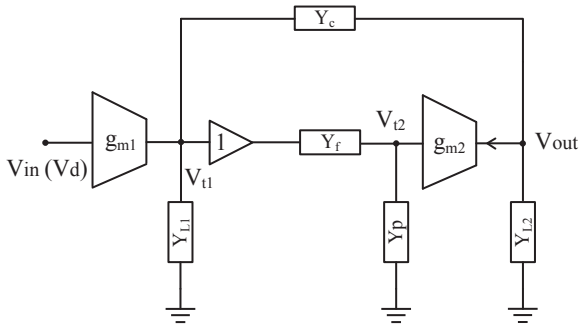


Fig. 5: Open-loop model for stability analysis

transfer function of the circuit is given by:

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}(Y_c - g_{m2}\frac{Y_f}{Y_f+Y_p})}{Y_cY_{L2} + Y_cY_{L1} + Y_{L1}Y_{L2} + Y_cg_{m2}\frac{Y_f}{Y_f+Y_p}} \tag{3}$$

and by considering $G_{L1} = 1/R_{L1}$, and the gain of the second stage $A_2 = gm_2 \times R_{L2}$, indicates the existence of poles and zeros in the system at:

$$\begin{aligned} p_1 &= -\frac{G_{L1}}{A_2C_c}\frac{C_f+C_p}{C_f} \\ p_2 &= -\frac{C_cg_{m2}}{C_cC_{L1} + C_cC_{L2} + C_{L1}C_{L2}}\frac{C_f}{C_f+C_p} \\ z_1 &= \frac{1}{C_c(\frac{1}{g_{m2}}\frac{C_f+C_p}{C_f} - R_c)} \end{aligned} \tag{4}$$

Recalling that the dominant pole of a two stage amplifier with compensation capacitor is $-\frac{G_{L1}}{A_2C_c}$, when comparing with our equation, we see that the dominant pole is increased by a ratio of $\frac{C_f+C_p}{C_f}$. At the same time however, the DC gain is attenuated by the same factor of $\frac{C_f+C_p}{C_f}$, leading to the gain-bandwidth-product remaining unchanged.

Furthermore, the second pole is decreased by the same ratio while the zero could be either positive or negative depending on the overall sum of the denominator of z_1. As there is a sudden introduction of this ratio on the poles and zeros after switching from the resetting to the sensing phase, compensation of the zero for both phases cannot be achieved. It is therefore desirable to give more attention to cancelling out the decreased non-dominant pole in sensing phase. This can be accomplished by making the influence of the ratio factor negligible, which can be achieved by making C_f dominant.

E. Noise analysis

To describe the noise performance of the system, we focus on the variation of electronic noise due to the addition of the feedback capacitor. The equivalent transformation for the noise analysis is shown figure 6, where the amplifier A symbolises the whole system excluding the feedback capacitor C_f, with $V_{n,a}^2$ being the equivalent input referred noise of amplifier A as it would appear on the floating gate of the ISFET device. $V_{n,i}^2$ is the equivalent input referred noise of the system

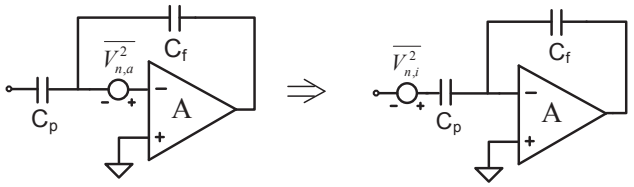


Fig. 6: Schematic for analysing noise equivalence

considering the two capacitors, C_p and C_f. Since capacitors do not contribute any noise, the majority of the amplifier noise $V_{n,a}^2$, as defined by noise figure, is dominated by the first stage, which in this case is the ISFET stage. The input referred noise contribution can therefore be derived as:

$$V_{n,o}^2 = V_{n,a}^2(\frac{C_p + C_f}{C_f})^2 = V_{n,i}^2(\frac{C_p}{C_f})^2 \tag{5}$$

$$\Rightarrow V_{n,i}^2 = (\frac{C_p + C_f}{C_p})^2 V_{n,a}^2 \tag{6}$$

As can be seen, to optimise the noise performance, we need to make the passivation capacitor dominant, which is however in contradiction with the requirement for stability.

F. Leakage analysis

With an ideal switch, the output signal should respond to the input signal scaled by a ratio of $-C_p/C_f$. In reality, however, the leakage current from the gate node will change the value of the floating gate voltage, V_g and consequently cause deviation in the output voltage, V_{out}. The change of gate voltage due to the leakage can thus be represented as:

$$\Delta V_{g,leak} = \frac{\Delta Q}{C_{tot}} = \frac{I_{leak} \cdot \Delta t}{C_{tot}} \tag{7}$$

and the corresponding output deviation as a result of this is:

$$\Delta V_{out,leak} = \frac{C_{tot}}{C_f} \Delta V_{g,leak} = \frac{I_{leak}}{C_f} \Delta t \tag{8}$$

where C_{tot} stands for the total capacitance seen from the gate node. We note that the amplitude of output signal also depends on the feedback capacitor, C_f. So when measuring chemical changes which are medium-to-long-term (a few seconds), measurement of the minimum detectable change is determined by leakage current when the passivation capacitor is fixed. Quantified as the signal-to-(leakage)drift ratio (SDR) below, this is maximised by keeping leakage to a minimum when the reaction is slow:

$$SDR = \frac{\Delta V_{out,sig}}{\Delta V_{out,leak}} = \frac{\Delta V_{in,sig} \cdot A_{dc}}{\Delta V_{out,leak}} = \frac{C_p}{I_{leak}} \frac{\Delta V_{in,sig}}{\Delta t} \tag{9}$$

G. Design tradeoff when choosing capacitors

As has been shown in the previous sections, there is a trade off when choosing the sizes of capacitors for the ISFET interface which can be clearly described with the aid of figure 7 to assist the design process. Choosing a large feedback capacitor C_f has benefits of stability and matching whereas choosing a smaller one is improves electronic noise performance and amplitude response. The choice of the two capacitors should therefore based on the specifications required for a given application.

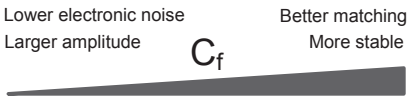


Fig. 7: Tradeoff in choosing the value of feedback capacitor

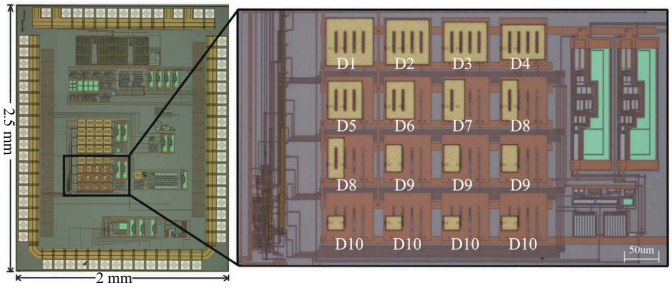


Fig. 8: Microphotograph of fabricated array

III. Design and Fabrication

The system was designed and fabricated in a commercially available $0.35\ \mu m$ 2P4M technology provided by AMS. The passivation layer of the given technology is made of Silicon Nitiride, Si_3N_4, which allows its use for pH sensing without the need for post-processing. The objective of the fabricated system was to validate the functionality of proposed ISFET interface over a variety of sensing areas and verify it's robustness to the non-ideal effects of trapped charge and passivation capacitance explained previously. To do so the ratio of the passivation capacitor to feedback capacitor was chosen to be close to unity to allow consistency in the output response over all pixel sizes and devices for comparison. The passivation coefficient given by the foundry is $22.65\mu f/m^2$ which allows an approximate calculation of passivation capacitance, and necessary feedback capacitor to achieve the desired gain. The transistor sizes for the devices used in the front-end are shown in figure 3. The amplifier and buffer used are the standard differential pairs and source follower. The system was optimised for low-power consumption, 848.1 nW for a single front-end with a 3.3 V supply, and minimum area, 60x70 μm^2. Figure 8 shows a microphotograph of the 2x2.5 mm^2 fabricated device containing ISFET sensors of increasing geometry which interface to the passivation using the top-metal (Metal 4) which forms the passivation capacitor, C_p, whose value is determined by this metal area.

We have fabricated 16 test devices labelled D1-D10 in figure 8 with a subset of ten different top metal areas realising different passivation capacitances. Devices under test in this

TABLE I: List of fabricated ISFET devices under test

Devices	Top metal area (Dimension) (μm^2)	Feedback cap (inc. parasitics) (fF)	Ratio (um^2/fF)
D1	4624 (68×68)	100 (104.6)	44.2
D2	3968 (62×64)	90 (94.4)	42.0
D3	3534 (62×57)	80 (84.06)	42.0
D4	3100 (62×50)	70 (74.02)	41.9
D5	2646 (49×54)	60 (63.44)	41.7
D6	2214 (41×54)	50 (53.86)	41.1
D7	1770 (30×59)	40 (43.76)	40.1
D8	1334 (23×58)	30 (33.58)	39.7
D9	893 (23×39)	20 (23.57)	37.9
D10	460 (23×20)	10 (13.68)	33.6

array are listed in Table I, whereby the feedback capacitor C_f has been scaled according to the sensing top-metal area to approximate a similar gain over all devices. Unless the passivation capacitance is very small, e.g. 20 fF, certain slots in top metal are required to be inserted to satisfy the metal stress-relief rules of the given CMOS technology (part of the Design-Rule-Checks), which is required to avoid delamination. Also shown in Table I is the effective feedback capacitor, which is derived through post-layout simulation. As can be seen, there is around 4 fF extra capacitance for all the devices due to the coupling of metal routing.

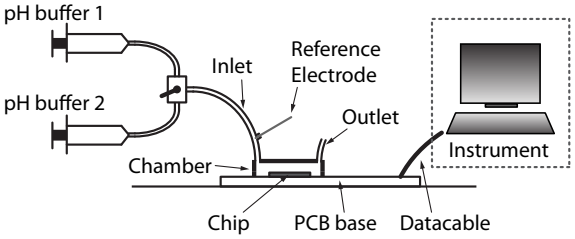
IV. Measured Results

A. Test setup

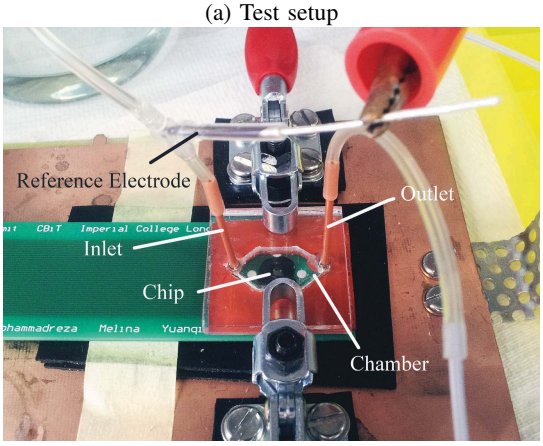
In order to test the fabricated device, we bond the bare CMOS die and epoxy encapsulate the wire-bonds on a PCB which is then integrated into a micro-fluidic flow cell. The test setup is shown in figure 9. The whole chip is immersed in the solution whose flow is controlled by a syringe connected with the inlet of the chamber. An Ag/AgCl reference electrode is placed at the inlet pipe to bias the devices. Because the chamber is fully sealed except for the inlet and outlet, new solution coming from inlet will expel any previous solution rather than reacting with it and the solution volume used is large enough to ensure this. As a result, the pH concentration the chip senses is the same with that kept in the syringe when the chamber is flushed. Tricine 1M KCl pH buffers have been used for the subsequent experimental tests.

B. Test of immunity to capacitive division

In this section we show how each device shown in Table I is immune to gain reduction due to the mentioned decrease of transconductance as a result of capacitive division of the floating gate voltage through the passivation capacitance which exists with ISFETs in CMOS. As described for the ISFET model in Section II-A, the voltage potential at the floating gate of transistor, $V_{g'}$ is a linear combination of reference electrode, V_{ref} and chemical voltages, V_{chem}. Therefore to test the gain of each ISFET interface and prove there is no gain attenuation due to capacitive division, we change the voltage value of the reference electrode to mimic a pH variation and measure the total amplification from a known source. A 100 mV_{pp}, 100 Hz sinusoidal signal is superimposed on the reference voltage, and the output signal is then measured, to derive the gain of the system by taking the ratio of these two



(a) Test setup



(b) Photo of experiment setup

Fig. 9: Experimental Setup

signals. Tests were verified in pH 4, 7 and 10 buffer solutions yielding identical results.

The measured amplification capability of all the ISFET DUT for 5 different CMOS chips is depicted in figure 10. What we see is that the proposed ISFET interface is immune to any capacitive division effects keeping its gain over all ranges of capacitance. We notice that for a single die, the amplification values of devices with the same passivation and feedback capacitance match very well as can be seen from Table II for the smallest device, achieving a standard deviation of σ=0.0058 for n=4 devices. However the trend in amplification is not constant over all devices which will be justified in the next section due to the value of the passivation capacitance which is not linear with size. We also see that the amplification values for a specific device on different chips varies by about 10%. We argue that it is largely due to the poor control of passivation layer using unmodified CMOS which can vary up to 20% from die to die. This however could be normalised using standard pH calibration. The measured results of mean and standard deviation of ISFETs with different capacitance are summarised in Table III.

TABLE II: Individual Die statistics for C_f=10fF

D10	Chip1	Chip2	Chip3	Chip4	Chip5
Amp. (n=4)	1.308± 4.6m	1.276± 4.6m	1.2155± 2.5m	1.2625± 7.2m	1.2240± 6.5m

Non-linear passivation capacitance

In Table I, the ratio of top metal area to feedback capacitor ideally should be linearly proportional to the designed gain.

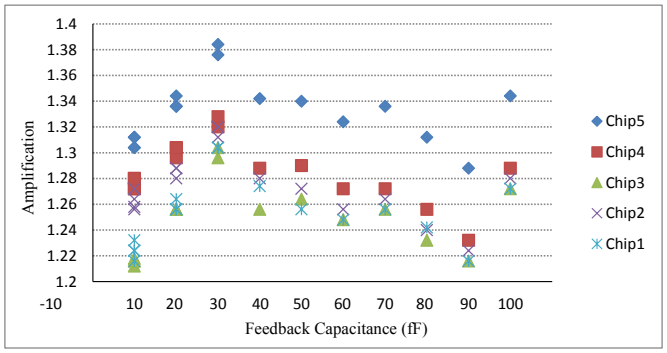


Fig. 10: Amplification of ISFETs for 5 different chips

Passivation capacitance in ISFETs however is generally poorly defined due to the fact that it's not a conventional two plate capacitor but top metal in contact with an insulator which is in contact with an ionic solution as shown in figure 1. We therefore expect the effects of fringe capacitance and the existence of metal slots in the top metal to play significant role in determining the actual passivation capacitance.

Since the coefficient of passivation capacitance per unit area is unclear, in order to do a relative comparison between devices and deduce the actual expected trend in gain which is measured in figure 10, a more detailed analysis of passivation capacitance is required. To do so, we apply a capacitor model which takes into account the geometry of the top metal to factor in the existing fringe capacitance and metal slots and more accurately estimate the passivation capacitance [18]. The passivation capacitance using this model can defined as:

$$C_p = 1.15\epsilon_{eff}\frac{A}{d} + 1.4(\frac{T}{d})^{0.222}\cdot P + 4.12(\frac{T}{d})^{0.728}\cdot d \quad (10)$$

where ϵ_{eff} is the effective permittivity of double layer passivation, A the area of top metal, T the thickness of top metal, P the perimeter of top metal and d the distance between two plates. The third term in above equation represents the contribution of the four corners. Using this we re-calculate the expected passivation capacitance and gain according using effective feedback capacitance. The results are shown in table III. What we see is that the calculated and measured results of estimated gain match quite well with an average deviation of 2.74% over all devices confirming the fringe capacitance and existence of metal slots play a crucial role in defining the actual passivation capacitance.

C. Test of pH sensitivity

To test the pH sensitivity of our ISFET sensing front-end, we flow the different pH buffers on top of the device using the flow cell shown in figure 9, flushing the chamber with new pH each time to expel the previous solution. Device D1 has been used for all chemical experiments. Since the system has the capability to reset the output voltage to it's original DC value during the sensing phase, a pH change from this point is always measured, using a buffer of pH 7 as the starting reference. Figure 11 shows the step response due to an infused

TABLE III: Summary of amplification meausrements over all dies

Device	Samples	Mean	Standard deviation	Estimated Gain	Deviation(%)
D1	5	1.2572	0.0353	1.294	+2.85
D2	5	1.2880	0.0317	1.242	-3.72
D3	5	1.3248	0.0307	1.251	-5.92
D4	5	1.2880	0.0324	1.257	-2.43
D5	5	1.2844	0.0335	1.264	-1.64
D6	5	1.2696	0.0319	1.266	-0.33
D7	5	1.2768	0.0338	1.279	-0.13
D8	10	1.2564	0.0323	1.232	-1.97
D9	15	1.2352	0.0303	1.280	+3.53
D10	20	1.2912	0.0303	1.231	-4.86

pH change for values 7 to 5, 6, 8 and 9. The change in output voltage for the different pH solutions is summarised in Table IV.

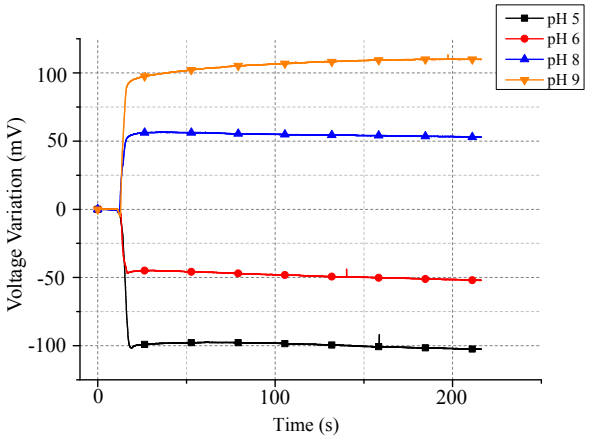


Fig. 11: Step output change from pH 7 for pH 5,6,8 and 9

TABLE IV: Voltage variation corresponding to pH changes

pH values	5	6	7	8	9
voltage change(mV)	-102.1	-56.35	0	51.9	102.05

A $53.1mV$ change per pH is measured which gives linear sensitivity as shown in the derived calibration curve from the two repeat tests in figure 12. Given that the gain of the front-end is approximately *1.26*, an input referred pH sensitivity of $42.1\ mV/pH$ is observed for the silicon nitride in this CMOS process. This is slightly lower than nernstian sensitivity (α=0.7) but expected due to the deposition method of the silicon nitride in CMOS [6]. An average accuracy of 91.63% is measured for the two repeats when compared with the linear fit in figure 12.

D. Test of long-term drift

To test the drift response of our front-end and the capability to reset the output, thus always initialising a starting point for the system, we conducted a 3 hour experiment in a pH 7 buffer solution. The measured results are shown in figure 13, where we can see that the output always starts from the same point after we reset the system and it also drifts at the same rate. The single-ended drift was measured to be $0.21\ mV/sec$. The

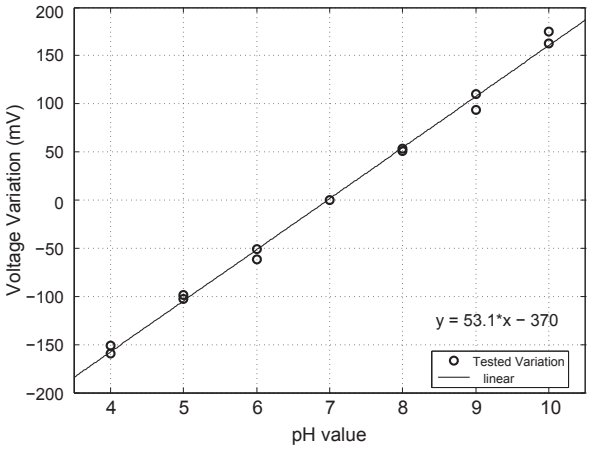


Fig. 12: pH sensitivity curve

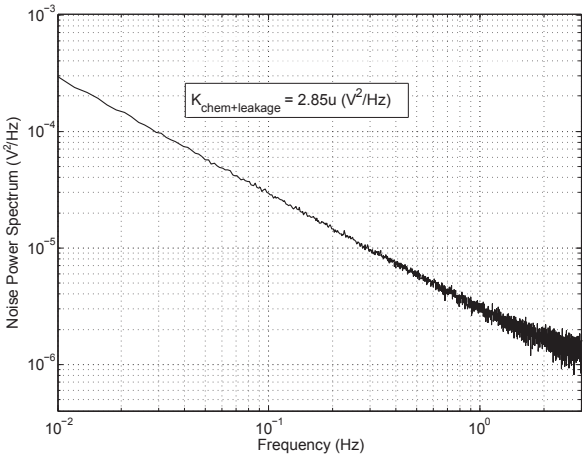


Fig. 14: Measured output noise power spectrum

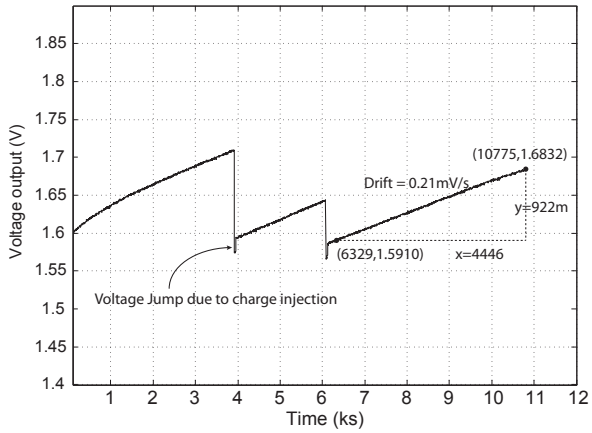


Fig. 13: Long term drift response and the effects of resetting

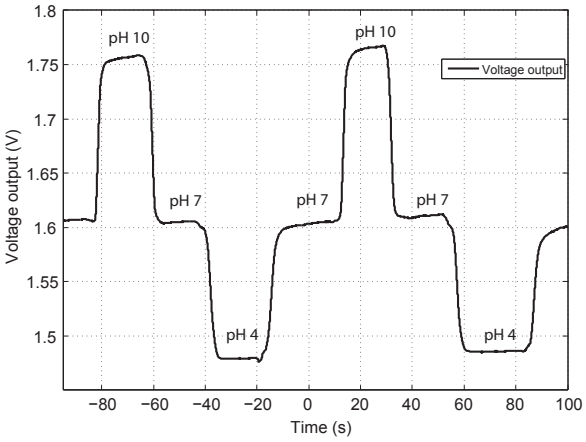


Fig. 15: Transient response to pH variation

effect of this can be regarded as a type of noise and will be analysed in the next section. Resetting the signal also allows us to counteract the effects of chemical drift, which would otherwise cause a deviation in output.

E. Noise measurement

As chemical reactions are generally slow in nature, ranging from seconds to minutes, the signals of interest are very low in frequency and thus we only consider noise at the same spectrum. To measure the noise in sub-Hz range, we record the data for over 10 minutes in a constant pH 7 solution and carry out an FFT calculation to get the noise spectrum. The noise test is carried out in wet conditions since chemical noise due to the sensing interface plays an important role. The total noise contributions which are measured are a sum of the chemical, electrical and drift due to leakage:

$$Noise_{total} = Noise_{elec} + Noise_{chem} + Noise_{drift} \quad (11)$$

The results of the measured noise are shown in figure 14, which is mainly dominated by flicker $(1/f)$ noise always present at these low frequencies. A relatively large K value (annotated in the figure) is as expected due to the chemical solution-to-semiconductor interface of the sensors which adds additional chemical noise not present in dry conditions. It is important to note that noise calculated is for a differential output which largely alleviates the leakage due to the switches. The coefficient of flicker noise $K_{chem+leakage}$ is found to be $2.85\mu V^2/Hz$. The output integrated noise from $100mHz$ to $3.5Hz$ is $3.2mV_{RMS}$, which equivalently gives us $60.3m\ pH$ resolution.

F. Chemical reaction monitoring

We experimentally validate the system's capability for reaction monitoring which would emulate a scenario for a reaction which produces a pH change such as that of DNA base incorporation [17].

We firstly carry out a pH sensitivity flow cell experiment to measure the transient response of the system. To do so we firstly infuse a starting of pH 7 and then change the pH by infusing different solutions (pH 4, 7, 10) to ramp up and down the pH values, allowing each pH to settle for 20 seconds. The measured results are shown in figure 15. What we observe is good sensitivity over multiple repeats and minimum hysteresis when the pH is brought back down to 7.

Following on from this we conduct a diffusion experiment. We sink the complete ISFET chip in a beaker containing

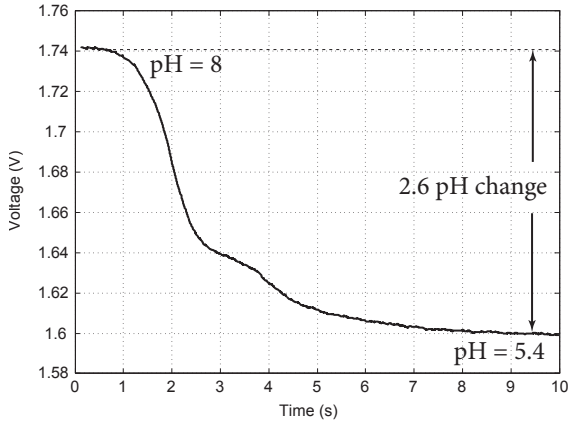


Fig. 16: Chemical reaction monitoring of a pH diffusion process

water solution at pH 8. We then manually infuse a high concentration of acid solution and wait for the concentration of the solution to reach equilibrium through the diffusion process. To accelerate the diffusion process we use a magnetic stirrer. The results are shown in figure 16. What we see it that the system tracks the reaction, reliably measuring a 2.6 pH change in the time span of 8 seconds.

V. System Summary

The achieved performance of the proposed interface with a 100fF feedback capacitance is summarised in Table V. The system achieves amplification, with a measured output of 53.1mV/pH and is capable monitoring chemical reactions as low as 0.06 pH with a signal-to-noise ratio of 24.67dB over 1 pH change and a dynamic range of 1.92V which is capable of monitoring over the entire pH range (1-14)[2]. Furthermore it has been designed for low-area ($60 \times 70um^2$) and low-power operation consuming an overall power consumption of 848.1nW for a 3.3V supply which is one of the lowest reported.

Table VI compares our system with other works reported in the literature. This is the first capable of combined compensation for trapped charge (TC comp.), Capacitive division (C_{pass} comp.), drift (drift comp.) and in-pixel amplification(Amp.).

TABLE V: Achieved system specification

Tech.	AMS-0.35μm
Supply voltage	3.3 V
ISFET Bias Current	100 nA
Feedback Cap	100fF
Area	60$\times$ 70 μm^2
Amplification	1.257
Power	848.1 nW
GBP	85.8k
pH sensitivity	42.1 mV/pH
Output Noise (2m-3.5 Hz)	0.348 mV_{rms}
pH sense resolution (53.1 mV/pH)	0.06pH
Dynamic Range (1%THD)	1.92 V

[2]Nernst equation can be expressed in terms of concentrations (pH values) only in dilute solutions, valid only for the range from pH 3 to 10 [19]

TABLE VI: Comparison of ISFET readouts with integrated compensation schemes

Year	Tech. (μm)	Size (μm^2)	TC comp.	C_{pass} comp.	drift comp.	Amp.	Ref.
2008	0.35	163	Yes	Yes	No	No	[10]
2010	0.35	3000	Yes	No	No	Yes	[11]
2011	0.35	2500	Yes	No	No	Yes	[20]
2012	N/A	4-202M	No	No	No	Yes	[21]
2013	0.35	460-4624	Yes	Yes	Yes	Yes	This work

VI. Discussion

In this paper we proposed a low-power, compact sensor interface which overcomes some of the undesirable factors which are present with ISFETs in unmodified CMOS. By applying a feedback to the gate directly from output terminal, factors such as trapped charge can be removed and drift can be eliminated periodically. The feedback inherently locks the gate voltage of ISFET, realising a constant-voltage-constant-current structure which bypasses the capacitive division. Thanks to this mechanism, the sensitivity is maintained well even for capacitor values as low as 10 fF.

The design considerations were investigated, and a tradeoff was derived for gain, stability and noise. Because of its simple structure and low-frequency requirement, the interface consumes low-power, which facilitates implementations for large arrays which has potential use for DNA microarrays. The choices of both passivation and feedback capacitors should be ultimately determined by the specification of the application. For example we can keep increasing the top metal area to realise large passivation capacitor which allows long-term monitoring, typically a few minutes, or use a small top metal yielding a compact pixels footprint which can be implement larger arrays but would work for short-term monitoring applications in duration of seconds such as DNA sequencing [4].

In our system the gain is determined by the ratio of passivation to feedback capacitance. This can potentially limit our control over the gain accuracy, given the passivation capacitance is determined by uncontrollable fabrication parameters such as thickness and conformality. We have also shown through analysis the effect of fringe capacitance and the slots in top metal also play a role in determining the passivation capacitance and found that our estimation of passivation capacitance accurately explains the measured gains in our devices. These aforementioned issues can potentially cause a deviation in amplification for different devices. The in-pixel amplification, however, is still achieved reliably and given it can be tuned by changing the ratio of C_p to C_f, if required, capacitive trimming can be added to reduce mismatch in gain.

For a given device however the amplification is fixed and bears no impact in degrading the overall result. The unmodified pH sensitivity (42.1 mV/pH) is always constant and the output voltage achieved after gain can be calibrated to pH using calibration curves such as the one derived in figure 12. In terms of noise, the system is mainly restricted by the chemical flicker noise. Although the electronic leakage is regarded as a noise source which may influence the result, differential configurations could be used to cancel this out. Nevertheless, we still obtain quite high pH sense resolution (0.06 pH).

The proposed interface has compensated for a number of challenges which hinder the application of ISFET sensors when used in unmodified CMOS. We have designed our front end for a low power consumption of 848.1nW and conservative area of 60x70μm^2 as summarised in Table V. Comparing our front end with other reported works ([12], [13]) we achieve total compensation of trapped charge and capacitive division effects using a single OTA stage with a minimal amount of circuits without a significant impact on power consumption. This practically enables an implementation of a medium sized array of 1000 pixels or more with reasonable chip area, by using multiplexing mechanisms for each pixel as reported in previous ISFET arrays [4], [22]. Furthermore, the use of the reset phase allows the opportunity for cancellation of any unwanted offset in the measurement through schemes such as correlated double sampling [23], in addition to measurement from a fixed reference which is ideal for monitoring of a pH change where we expect a certain chemical reaction to occur. Through our novel interface and compact design we have achieved a potentially scalable scalable system that can be applied to a number of sensing applications ranging from the use of simple single or differential pH monitoring for on the spot measurement in point-of-care systems, to medium-scale DNA micro-arrays for DNA hybridisation detection and potentially with further design larger arrays of 10,000 pixels for target specific DNA sequencing.

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