Towards an Inductively Coupled Power/Data Link for Bondpad-less Silicon Chips

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Abstract—This paper explores the concept of developing a bondpad-less fully-integrated inductive link for power/data transfer between a CMOS Integrated Circuit (IC) and a PCB. A key feature of the implemented system is that it requires no off-chip components. The proposed chip uses a standard 0.35 µm process and occupies an area of 2.5 mm × 2.5 mm and an on-chip inductor occupies an area of 1.5 mm × 1.5 mm. At 900 MHz, 9 mW was designed to be provided to the chip (up to 22.5 mW with a total efficiency of 5%). Binary Phase Shift Keying (BPSK) and Load shift keying (LSK) are used for the the PCB-to-chip and chip-to-PCB link respectively for half-duplex communication. An Injection-Locked-Oscillator-based BPSK demodulator is implemented on-chip to save power. The maximum data rate for the PCB-to-chip link is 10 Mb/s. The estimated area of the circuitry was designed to be provided to the chip (up to 22.5 mW with a total efficiency of 5%). Binary Phase Shift Keying (BPSK) and Load shift keying (LSK) are used for the the PCB-to-chip and chip-to-PCB link respectively for half-duplex communication. An Injection-Locked-Oscillator-based BPSK demodulator is implemented on-chip to save power. The maximum data rate for the PCB-to-chip link is 10 Mb/s. The estimated area of the circuitry. Of these, inductive coupling is preferable since optical technique require light emitters or modulators which cannot be realised in standard CMOS, and capacitive techniques require electrostatic coupling to the top surface which would limit application (e.g. for imager chips or chemical sensing).

I. INTRODUCTION

Commercially-available ICs, such as the Central Processing Units (CPU), typically connect power and data galvanically through package pins. This standard method (i.e. bondwire connection) places an overhead on silicon area (for bondpads, ESD protection structures, etc) and poses potential reliability issues in certain applications. For example, in chemical sensing, the surface is typically exposed to the electrolyte, which must be isolated from the bondwires to prevent system failure. In a bondpad-less silicon chip, the power and data can be transferred through a wireless connection, therefore improving reliability for such applications.

Traditionally, wireless power/data transfer has been used in biotelemetry and RFID systems; however, due to the requirement of off-chip discrete components (e.g. inductors), these solutions are not fully-integrated [1], [2]; however, wireless inter-chip communication systems are fully integrated and can be categorised into three groups: optical, capacitive, and inductive. Of these, inductive coupling is preferrable since optical technique require light emitters or modulators which cannot be realised in standard CMOS, and capacitive techniques require electrostatic coupling to the top surface which would limit application (e.g. for imager chips or chemical sensing).

Using a wireless inter-chip connection allows post-fabrication reconfigurability of System-in-Package (SiP) systems [3]. It has been shown that bandwidths as high as 1Tb/s can be achieved through an inductive link [4], which is orders of magnitude higher than 40Gb/s for traditional high speed interconnections [5]. Also, ICs can be tested on-wafer by providing a power/data link using inductive coupling [6]. All these same advantages apply to a bondpad-less system.

To the best of our knowledge, the first chip demonstrating the feasibility of inductive coupling for power and data transfer with on-chip inductors was reported in 1989 [7]. Here, the chip was tested with ferrite yokes and the size of inductor was relatively large, and no tests were carried out between the PCB and chip. After that, inductive coupling techniques have been applied to inter-chip interconnection for SiP systems to fill the increasing gap between the system bandwidth and the I/O throughput [8]. Although successful experiments have been reported on wireless power transfer within SiP systems [3], results on power transfer between the PCB and chip showed limited power efficiency due to the mismatch between the PCB and CMOS processes [6]. Since this, no further work has been found to investigate the feasibility of inductive coupling to wirelessly connect a chip to a PCB. In this paper, an inductively coupled PCB/IC link with a fully-integrated, dedicated transceiver system is presented. The paper is organised as follows: Section II, describes the full system; Section III details the implementation of the inductive link and on-chip circuits; Section IV presents the simulated results and finally, Section V presents the conclusion.

II. SYSTEM OVERVIEW

The block diagram of the proposed system is shown in Fig. 1. On the PCB, the carrier wave is generated, modulated and power amplified for transmission via the inductive link. This signal is then received on-chip through the parallel LC tank that resonates at this carrier frequency. The signal is then full-wave rectified and regulated to provide 9 mW power to the on-chip components with a steady output voltage of 3 V. At a carrier frequency of 900 MHz, BPSK and LSK are used...
for the PCB-to-chip\textsuperscript{1} and chip-to-PCB links respectively for half-duplex communication.

III. IMPLEMENTATION

A. Inductive Link

Although a higher carrier frequency is preferable in order to achieve higher communication bandwidth and lower on-chip supply ripple, the maximum frequency is limited by the parasitic inductances/capacitances and power dissipation of the circuits working at higher frequency. As a trade off between data-rate, frequency limitations, and the ISM bands available in the UK, 900 MHz (866-906 MHz) is chosen for this work [9]. This also provides the opportunity for longer-range wireless applications in the future.

The chip occupies an area of 2.5 mm \( \times \) 2.5 mm with a single on-chip square inductor implemented using metal 4. The chip is mounted to the PCB substrate using die attach epoxy, therefore defining the communication distance to be 400 \( \mu \)m.

To evaluate the inductive link, Microwave Office\textsuperscript{®} was used to simulate the inductor pair together with Cadence IC Design Framework. The inductor simulation results were confirmed by comparison to the foundry-supplied process documentation.

As the impedance of the PCB series resonant circuit becomes low when in resonance (for 1 mm diameter, 1 \( \Omega \) is found through simulation), a large current (\( \sim 1 \) A) is expected. With a track thickness of 70 \( \mu \)m, the minimum external track width is 200 \( \mu \)m according to manufacturer guidelines, which provides a good margin for a 1 A current [10].

Since the on-chip inductor does not use thick metal (due to process limitations), a track width of 35 \( \mu \)m is used to increase the quality factor. Although wider tracks are possible with metal slotting, their effect on inductor performance is unknown and adds unnecessary complexity in modelling. By using the minimum metal-to-metal spacing, the inner diameter is maximised to enhance the coupling.

The inductor pair is simulated, starting from 1 mm \( \times \) 1 mm\textsuperscript{2} to 2.5 mm \( \times \) 2.5 mm\textsuperscript{2} with intervals of 0.5 mm \( \times \) 0.5 mm\textsuperscript{2}. With each increase, the number of turns of the on-chip inductor increases by 0.25 each time. The best inductor is then chosen.

\textsuperscript{1}This will be referred as down-link and chip-to-PCB as up-link in future.

B. Power Supply Module

The power supply consists of 3 components: the full-wave rectifier, bandgap voltage reference (BGR) and low dropout (LDO) linear voltage regulator.

1) Rectifier: The MOSFET-based full-wave rectifier used is shown in Fig. 3. P1 and P2 serve as switches while N1 and N2 serve as diodes to block the reverse current. The dropout voltage, \( V_{\text{drop}} \), is defined as the difference between the peak voltages of the rectifier input and output. This is given by:

\[ V_{\text{drop}} = |V_{\text{thn}}| + \sqrt{\frac{2I_d}{\rho_pC_{\text{ox}}(W/L)p_1/p_2}} \tag{1} \]

where \( V_{\text{thn}} \) is the NMOS threshold voltage which (0.5V) and \( \rho_pC_{\text{ox}} \) is a process parameter for PMOS. \( I_d \) is the DC load current at the output. By increasing the aspect ratio of P1 and P2, \( V_{\text{drop}} \) is only limited by \( V_{\text{thn}} \).

2) Bandgap Voltage Reference: A BGR circuit is used to provide a temperature and supply independent output voltage for the regulator. The power supply rejection (PSR) of the BGR needs to be kept below at least -20dB up to 900MHz. \( C_1 \) and \( C_2 \) in Fig. 4 is used to increase the PSR at high frequencies while a PSR boost cell [11] is used to increase the PSR at low to medium frequencies and feed the supply ripple directly to the gate of P1 and P2 to ensure a constant \( V_{gs} \).

3) Regulator: The full schematic of the regulator is shown in Fig. 5. The power PMOS has a large aspect ratio in order to provide the low dropout characteristic. For the same reason described in the BGR circuit, the PSR boost cell is used here (performance shown in section IV-B). The LDO is compensated by \( R_1, C_1 \) and \( C_2 \).

C. Communication Module

1) BPSK demodulator: A BPSK signal uses two phases of the carrier to represent the bit ‘0’ and ‘1’. Usually, the two phases are in anti-phase to maximise the phase noise margin.
Since conventional demodulators need to use power-hungry circuitry to recover the carrier, a demodulator using a second-harmonic-injection-locked-oscillator (SH-ILO)-based demodulator is used to save power [12], [13] (Fig. 6). The SH-ILO1 has a free running frequency at 446MHz while SH-ILO2 has a free running frequency at 454MHz. The incoming 900MHz BPSK signal is first split into two branches and is then injected into the corresponding SH-ILO which is locked to the injected signal with output frequency of 450MHz. Assuming the output of the two SH-ILOs are in phase at first, when there is a 180° phase change of the BPSK signal, SH-ILO1 will have a +90° phase shift and SH-ILO2 will have a -90° phase shift after relock. This causes the two outputs to be out of phase, which can be combined to generate an Amplitude Shift Keying (ASK) signal for further processing. The power splitter and combiner need to provide sufficient isolation between the two branches.

The SH-ILOs are implemented using voltage controlled differential ring oscillators with self-replica-biasing [14] (Fig. 7). By increasing the biasing current and reducing the width of the MOSFET, the splitter in [12] and voltage combiner in [15] are modified to work up to 900MHz. Since high bandwidth (up to 450 MHz) analogue differential to single-ended conversion is hard to implement (in 0.35μm technology), a circuit based on standard logic gates is proposed to achieve this. The differential outputs are first shaped by the inverters (preserving their relative phase relation) and then a XOR gate performs differential to single-ended conversion generating the ASK signal. A simple 1st order low pass RC filter (with cut off at 16MHz) is used to detect the envelope of the ASK signal. A simple 1st order low pass RC filter (with cut off at 16MHz) is used to detect the envelope of the ASK signal. The power consumption of the demodulator is 3 mW.

2) LSK modulator: Although the system is half-duplex, LSK is used for the up-link as it can allow full-duplex communication and saves power. The LSK modulator comprises a single MOSFET switch which can change the impedance of the on-chip LC tank by shunting the rectifiers output current. This will also cause a change in the voltage of the PCB-inductor due to the inductive link. The drawback is that the large supply ripple introduced on the on-chip power supply may effect the operation of the BPSK demodulator. The required modulation index on the PCB-inductor voltage depends on the link speed. The faster the link, the higher this index should be.

IV. SIMULATION RESULTS

A. Inductive Link

Fig. 8 (a) shows a comparison of the simulated inductors as mentioned in section III-A. The performance of the chosen inductor is summarised in Table I. An electromagnetic simulation has also been done to investigate the effect of alignment offset (Fig. 8 (b)). It is worth noticing that with an offset of ±100 μm, the coupling coefficient remains above 0.2, therefore ensuring the coupling strength.

B. Power Supply Module

For the rectifier, with (W/L)_{P1,P2} = 400, V_{drop}=1.1 V was observed (Fig. 9). The PSR boost cell shows about 30 dB improvement for the BGR and LDO (Fig. 10).
The transient response of the startup of the on-chip power supply with a BPSK signal transmitted is shown in Fig. 11. The output voltage is approx 3.04 V with a 4.2 mV ripple. The maximum delivered power simulated is 22.5 mW with a total efficiency of 5%.

C. Communication Module

The transient response of the BPSK demodulation is shown in Fig. 12. Trace (a) shows the BPSK data while (c) is the low pass filtered ASK signal (b). The maximum supply ripple allowed for correct demodulation is found to be ±10 mV which is sufficient in comparison to the 4.2 mV ripple. The maximum data-rate tested is 10 Mb/s and to reduce the error-rate, differential BPSK is often preferred.

For LSK (Fig. 12), the power supply ripple (f) increases to 20 mV when the modulation index on the PCB-inductor is 1% (e), permitting only half-duplex communication.

V. CONCLUSION

We have introduced the concept of a bondpad-less PCB/IC link and outlined the implementation using inductive-coupling without off-chip components. The complete inductor and circuit design is presented for a fully-integrated, dedicated transceiver system. Simulation results comprehensively demonstrate the operation of this implementation and provide good justification to the feasibility of the concept. Considering the size, process and carrier frequency of the system, this system has achieved a competitive design trade-off within the state-of-the-art. A system summary is shown in Table II.

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