A Bio-Implantable Platform for Inductive Data and Power Transfer with Integrated Battery Charging

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Abstract—This paper describes a mixed signal subsystem for the inductive transfer of power and data to a fully-implantable medical device. The design includes circuits for the inductive power recovery and energy storage (charging), in addition to data recovery and demodulation. The data link is used to upload (at a data rate of up to 180Kbps) calibration and configuration data to the implanted device and integrates both error detection and correction on the recovered bitstream. The system incorporates an implanted Li-Ion micro-battery with supporting charging hardware to provide an uninterrupted power supply for autonomous deployment. This is to provide continuous operation without the requirement for an externally worn unit and additionally ensures registry (i.e. patient calibration) settings are maintained. The circuit has been implemented in a commercially available 0.35µm CMOS technology without requiring high-voltage device options.

Index Terms—neural prosthesis, inductive telemetry, implanted device, data recovery, power recovery, battery charging

I. INTRODUCTION

Medical devices that interface with neural pathways for sensory or motor rehabilitation have recently enjoyed significant interest [1]. This is partially due to the huge successes of cochlea implants but also the semiconductor industries relentless progress on integration density. This enabling technology has provided medical devices the opportunity to implement advanced systems at miniature scale suitable for implantation. Furthermore, modern submicron CMOS technologies make it possible for such systems to be implemented using highly energy efficient circuits and systems. Coupled with advances in rechargeable battery technology makes the notion of totally implantable prosthetic devices technically feasible.

Conventional neuroprosthetic technology, for example, commercially-available cochlear implants are generally based on a two module device comprising of the implanted unit and a body-worn unit (housing the battery and processing electronics). Power and data are typically transferred through the skin using a transcutaneous inductive link [2], [3]. An emerging breed of new autonomous and fully-implantable devices will aim to combine these in one implanted unit and use a body-worn device simply for charging and calibration. However, such devices would introduce new design challenges [4], for example, including an implanted battery and optimising the prosthesis electronics to operate on a limited power budget.

In this paper, we present a data and power management system for such a transcutaneous link, combining traditional circuits for data and power recovery together with new requirements for voltage regulation and recharging. All circuits have been implemented using a standard (i.e. non-high voltage) CMOS technology.

II. SYSTEM OVERVIEW

The overall system consists of three main blocks: the power recovery/management circuit, the data recovery circuit and the charger circuit. The system architecture is shown in Fig. 1.

The transcutaneous link allows to transmit both power and data to the implant by using ON/OFF keying with Pulse Width Modulation (PWM) [3]. This is achieved using a pair of coupled inductors (one implanted and one external) that form part of an LC tank tuned to a carrier frequency of 2MHz (for minimum absorption in water). The primary LC tank (i.e. external unit) is based on the discrete circuit reported in [2]. The secondary LC tank (i.e. implanted unit) connects to the circuit described herein feeding both the power and data recovery blocks. The power recovery block (see Fig. 1(a)) rectifies and limits the AC signal to provide the DC supply for the voltage reference and regulation circuits. The data recovery block (see Fig. 1(d)) limits, envelope detects, integrates and thresholds the signal to demodulate the data. The charging circuit implements a two phase charge cycle (constant current and constant voltage) to efficiently load the implanted battery.

III. IMPLEMENTATION

The circuit has been implemented in a commercially-available 0.35µm CMOS technology without requiring high-voltage device options. This has been achieved by using parasitic pn junction diodes (n-well/p-diffusion) for the rectification and voltage limiting circuits thus to ensure all MOS devices are shielded from possible overvoltage fluctuations.

A. Inductive Coupling

The planar coils have been fabricated using a standard FR4 laminate (i.e. 35µm copper on a 0.8mm epoxy-resin substrate). The design specifications are given in Table I and the fabricated prototypes are shown in Fig. 2.

B. Power Recovery Circuit

The block diagram of the power recovery circuit is shown in Fig. 1(a). The input (i.e. connection to LC tank) feeds a high-voltage tolerant full-wave rectifier that has been implemented...
Fig. 1. System architecture of the bio-implantable platform. Shown is: (a) the power recovery block, (b) the PWM demodulator, (c) top-level organisation and (d) the data recovery block.

| TABLE I  
| COIL SPECIFICATIONS |
|---------------------|----------------|
| Parameter           | Quantity | Unit |
| Outer, inner diameter | 20, 6 mm |
| Track width, separation | 150, 150 µm |
| Track length          | 1.27 m    |
| RDC/Rs               | 3.9/5.6 Ω |
| Track capacitance     | 3.47 pF   |
| Q for no load, 500Ω, maximum load | 21.9, 3.4, 122.4 |
| Impedance (Parallel capacitance) | 22.935 KΩ |
| Coil self-resonance   | 27.3 MHz  |
| Capacitance (LC resonance of 2MHz) | 647 pF |

Fig. 2. Prototype planar coils fabricated on standard FR4 substrate.

(a) Test platform (coupling) (b) Single coil of 300µm pitch

using p-diffusion/n-well diodes (in 0.35µm CMOS these tend to have a reverse breakdown voltage of over 30V whilst having a low junction potential of about 0.5V). This is followed by DC voltage clamp to ensure proceeding stages are protected from over-voltage conditions that may arise due to varying coupling efficiency. This may be caused by changing the coil-to-coil spacing (implanted and external) in addition to patient-to-patient variation depending on surgical implantation.

The unregulated DC supply is smoothed using an off-chip miniature SMT capacitor (0402, 10µF, 6.3V) to provide a supply of around 5.5V. This powers the master voltage reference (see Fig. 3) which provides a bandgap reference of approximately 1.20V. Particular attention has been given to power supply rejection and process variation whereas temperature variation is not an issue (implanted devices benefit from the bodies regulation of core body temperature). In turn this bandgap reference is used to provide regulated supplies of +5V (to power the battery charging circuit) and +3.3V (to power the underlying medical device) using standard voltage regulator topologies.

C. Implantable Battery and Charging Circuit

1) Rechargeable Battery: Modern Lithium-Ion technology provides good characteristics for implantable rechargeable
batteries including high energy density and voltage, low self-discharge rate and no memory effects compared to other technologies [5]. Drawbacks however are that the capacity decreases with increasing charge cycles and overcharges [6]. We have chosen to base our design on the Contego Series of Li-Ion batteries by EaglePicher Technologies. These typically have an operating voltage of 3.7V with maximum charge potential of 4.1V and minimum discharge to 3V. This series is available in capacities from 500µAh to 350mAh and are rated for >1000 charge cycles whilst operating at 37°C.

2) Charging Strategy: A common charging strategy to ensure a fast charge time, efficient energy delivery and maintain battery health is the constant-current(CC)/constant-voltage(CV) method. This allows the battery to reach close to 100% its capacity at the end of the charge, delivering approximately 65% during the first phase (CC) and 35% during the second phase (CV). For the selected series of Li-Ion batteries, these phases are defined as follows:

- For $V_{batt} < 4.1V$: CC phase- to be maintained at a rate between 0.1C to 1C (C=capacity).
- For $V_{batt} \geq 4.1V$: CV phase- to be maintained at 4.1V until the charge current reaches 5% the initial [7].

3) Charging Circuit: The circuit implementation to the charger is shown in Fig. 4. The voltage $V_{phase}$ is the control signal for the CC/CV phases and the voltage $V_{soc}$ flags the end of charge signal. For the CC phase, a charge rate of C/3 has been chosen to strike a good trade-off between high charge current, shorter charge time and minimising battery heat dissipation. For a battery of capacity 115mAh, this equates to a 38mA CC level. This is derived from a PTAT reference with current scaled up using a high current drive mirror. It is essential that the output impedance of the driver stage is as high as possible so as to maintain a constant current with varying battery voltage, i.e. increasing from 3.3 V to 4.1 V. To achieve a high output impedance a regulated cascode output stage [8] has been implemented. For the CV phase, it is crucial (to avoid damage to the Li-Ion cell) that the bias does not exceed the maximum charge rating of the battery (4.1V). Thus the voltage bias that provides the 4.1V reference has been designed to achieve a 3σ variation of under 50mV.

D. Data Recovery Circuit

To recover the data from the inductively coupled signal data recovery hardware is required within the implanted unit. The external unit (before modulating within the 2MHz carrier) first applies Hamming(12,8) encoding and then modulates the data as a 33% (data “0”) or 66% (data “1”) duty cycle. A Hamming(12,8) scheme is used to allow for the correction of all 12 possible single errors and simultaneously detect eight of the nine double adjacent errors.

The data recovery circuit is shown in Fig. 1(d). This takes the LC tank signal, recovers the envelope, demodulates the data and then applies a Hamming decoder to detect/recover errors. The LC tank voltage is first scaled down through a potential divider to provide a safety margin to voltage surges. This feeds the PWM demodulator (Fig. 1(b)) that is based on the design reported in [3]. Within the PWM demodulator, the envelope detector first recovers the modulating signal by using a charge pump that charges/discharges a NMOS gate capacitance. A phase generator [9] then uses the envelope to control two integrators that feed comparators to determine a data “0” or “1” and the clock signal is recovered by extracting the PWM period. The raw bitstream is then loaded serially into a 12-bit parallel register which feeds the Hamming decoder that can detect and recover a single-bit error. This is achieved by using a Hamming encoder to recalculate the check bits using the demodulated data bits and then comparing this to the raw bitstream to determine the position of the error. The 8-bit (error corrected) word is then resynchronised using a gray-counter based control register and streamed out serially to the underlying medical device.

IV. Simulation Results

The circuit was simulated using the Cadence Spectre (5.1.41lisr1) simulator with foundry supplied BSIM3 models. Transient simulation results illustrating the power recovery, data recovery and charging are shown in Figs. 5, 6 and 7 respectively:

- Power recovery (Fig. 5), illustrating the power supply start-up on application of the carrier stimulus on the primary coil (external unit) with a 1KΩ load. The start-up time to reach within 0.1% the final unregulated voltage output is approximately 20ms, mainly due to the off-chip smoothing capacitor charge time. However, the bandgap reference (+1.2V) and regulated +3.3V/+5V supplies are stable within 5ms.
- Battery Charging (Fig. 6), illustrating the CC (Fig. 6(a)) and CV (Fig. 6(b)) phases. This has been configured for a 115mAh battery which has been simulated by a voltage source increasing from 3.0V to 4.1V (CC phase) and a current source decreasing from 38mA to 0mA (CV phase). During the CC phase, at t=1s, $V_{phase}$ signals 5V indicating that the CC phase is finished. The CV phase is
V. DISCUSSION AND CONCLUSION

This paper has described an integrated platform for transmitting power and data to a fully-implantable device including circuitry for efficient battery charging.

This system provides the underlying medical device with a +3.3V power source in addition to the recovered clock and data (bitstream) input for uploading of calibration or patient data. In order to reliably load control data to the end-device it is preferable to implement an input serial-shift register that triggers a parallel data load to the core registers when the input bitstream is perfectly aligned. This can be implemented using a bitstream preceded by flush bits and a start sequence as reported in [10].

On removal of the external supply (i.e. the body worn unit), the implanted battery is connected to the +3.3V supply using a forward-biased diode (at nominal current consumption) to drop the battery supply from +4.1V to +3.3V. For a static load, this would provide a stable level, however for varying loads and/or circuits sensitive to supply variation additional regulation would be required. Also, for applications requiring a higher voltage supply (eg. neural stimulators), a voltage boosting circuit can be driven from the +3.3V supply.

The system has been developed to work with low cost FR4-based planar planar coils and can achieve a maximum data rate of 180Kbps using a 2MHz carrier, additionally including a Hamming(12,8) decoder to enhance data integrity. The integrated battery charger can be easily configured to operate with a series of implantable Li-Ion batteries from 500µAh to 350mAh capacities. Finally, the integrated circuit has been implemented in a commercially-available 0.35µm CMOS technology without the requirement for high-voltage devices (>5V).

ACKNOWLEDGMENT

The authors would like to acknowledge EPSRC grants EP/F04612X/1 and EP/I000569/1 for supporting this work.

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