Comparative Analysis of an MV Neutral Point Clamped AC-CHB Converter with DC Fault Ride-through Capability

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***Abstract*—The AC side cascaded H-bridge converter with a two-level main bridge has previously been proposed as a fault tolerant converter for HVDC. This paper explores the benefits of replacing the two-level bridge with a neutral point clamped three-level (NPC) bridge for MVDC applications and defines the optimum operating conditions for this case. By modifying the topology to include an NPC main bridge, the peak stack voltage during normal operation is decreased considerably which results in a 58% reduction in the required number of sub-modules (SM), thereby significantly increasing efficiency. However, this sacrifices the fault ride-through capability as the stacks are no longer able to support the AC voltage and thus two new SM topologies are proposed. The proposed topologies function as single full-bridges with two capacitors in parallel during normal operation. Under fault conditions, the SMs divide into two series connected full-bridges to enable DC fault ride-through. Reverse-blocking IGCTs or ultra-fast mechanical switches are used to bypass the IGBTs which are unused in normal operation and therefore the topology maintains a high efficiency. Simulation results are shown, and the proposed topologies are compared with more conventional designs in terms of efficiency, energy storage requirement and device count.**

***Index Terms*—DC-AC power converters, Modular multilevel converters, MVDC**

I. Introduction

ENVIRONMENTAL concerns are driving a rise in the penetration levels of distributed generators (DGs), such as wind turbines and photovoltaics, on the medium voltage (MV) network. This change poses several problems for distribution network operators; such as, the increased risk of over-voltages [1] and rising short circuit current levels [2]. 'Soft' normally open points (SOPs) have been proposed as a solution and have been shown to increase the penetration of DGs [3]. SOPs consist of two back-to-back converters and can provide active and reactive power control. Placing SOPs on the MV network facilitates meshing and allows for power transfer between previously unconnected feeders. Furthermore, SOPs have been shown to have a strategic value due to their high flexibility [4]. To successfully employ SOPs, it is important to establish which converter topology provides the best performance in terms efficiency, cost and physical volume at MV levels. Improving efficiency has obvious benefits in terms of life-time cost but also for the cooling requirements of the substation. Limited space at substations requires very compact designs so minimization of the required energy storage components, such as capacitors, is also important. It is also important to consider the device count as this will have a negative impact on the initial cost of the converter.

Multilevel voltage source converters, such as the modular multilevel converter (MMC) [5], have been a popular choice for both HVDC and MVDC systems due to their scalability and low AC filtering requirement. Other multilevel converter topologies have been proposed such as: the Hybrid MMC [6] [7], the Alternate Arm Converter (AAC) [8], and the AC-side Cascaded H-Bridge converter (2L-AC-CHB) [9].

The MMC has been studied extensively and can be composed with various sub-module (SM) topologies [10], the most common of which are the full-bridge (FB) and half-bridge (HB) SMs. The HB-MMC has the higher efficiency and lower device count; however, the FB-MMC is capable of DC fault ride-through. DC fault ride-through is an attractive trait as it has been suggested that this could lead to a reduction in the DC circuit breaker requirement in DC networks [11]. Furthermore, DC fault ride-through capability enables the converter to remain operational during faults and so the converter can provide reactive power as well as being able to re-energize the DC network and resume power flow without the delay of restarting the converter. The hybrid MMC contains a combination of FB and HB SMs and has been shown to provide an improved efficiency compared to the FB-MMC whilst still providing DC fault ride-through [6]. However, all MMC topologies require a high level of energy storage, in the form of SM capacitors, to minimize SM voltage ripple [12]; this results in a large penalty in terms of volume and cost. The AAC uses director switches to alternate the conduction period of each arm resulting in a reduced number of SMs [8] and lower energy storage requirement compared to the MMC [12], whilst also being able to provide DC fault ride-through. The 2L-AC-CHB consists of a slow switching two-level (2L) main bridge followed by a stack of cascaded H-bridge SMs on the AC side which provide the required harmonic elimination. The 2L-AC-CHB features a very small energy storage requirement [12], a low number of SMs and is also capable of providing fault ride-through. Despite

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a much lower number of SMs compared to the MMC, large losses in the 2L-bridge result in a low efficiency [13]. In [14], an AC-CHB with a three-level neutral point clamped main bridge (NPC-AC-CHB) has previously been proposed for use in industrial drives and demonstrated experimentally in [15]. More recently this topology has been proposed for use in MVDC systems [16]. It has been shown that by increasing the size of the stack, DC fault ride-through can be achieved [16]. However, an analysis of the optimum operating conditions for the minimization of energy storage and losses has not been addressed.

This paper analyses the relative benefits of replacing the 2L main bridge with an NPC-bridge in the AC-CHB in the context of MV applications and identifies the optimum operating conditions for the NPC case. The AC-CHB with NPC main bridge (NPC-AC-CHB) is compared to the MMC (FB, HB and hybrid), AAC and 2L-AC-CHB topologies in terms of efficiency, energy storage requirement and device count.

Using an NPC-bridge reduces the peak voltage that the stack of SMs is required to produce during normal operation [16] and, as will be shown in this paper, this reduces the required number of SMs and, in turn, improves the efficiency. Furthermore, it will be shown that the lower voltage produced by the stack reduces the total energy storage requirement to approximately half that of the 2L case. The benefits of small SM capacitors are thought to be more relevant at MV than at HV, because the reduced insulation clearances mean that SM capacitor size represents a larger proportion of the total converter volume; and so, the NPC-AC-CHB is thought to be well suited to MV applications.

However, this paper shows that if the SM stacks are sized such that they are only capable of producing sufficient voltage during normal operation, the NPC-AC-CHB is unable to provide DC fault ride-through. The number of SMs can be increased to provide fault ride-through capability but this sacrifices the improved efficiency of the NPC case. Thus, a new SM topology is required.

This paper also proposes two new Divisible SM (DSM) topologies which act as a single FB SM with two capacitors in parallel during normal operation and divide into two series connected FB SMs during faults. Thereby, doubling the stack voltage capability, enabling DC fault ride-through. One topology uses low conduction loss reverse-blocking IGCTs (RB-IGCTs) to bypass the switches which are unused during normal operation; whereas the other topology uses ultra-fast mechanical switches. In this way, the converter can operate at a high efficiency during normal operation, whilst also being capable of DC fault ride-through.

II. Topology Description

Fig. 1 shows the circuit schematic for one phase of the NPC-AC-CHB. The NPC-bridge contains four main bridge switches and two sets of clamping diodes per phase, each consisting of several series connected devices to provide the required voltage rating. While this is not a particularly attractive solution, it is considerably easier to achieve this at MV compared to HV as the number of series connected devices required is substantially lower. Alternatively, series connected H-bridges with small snubber like capacitors could be used, as in [17], to ease the

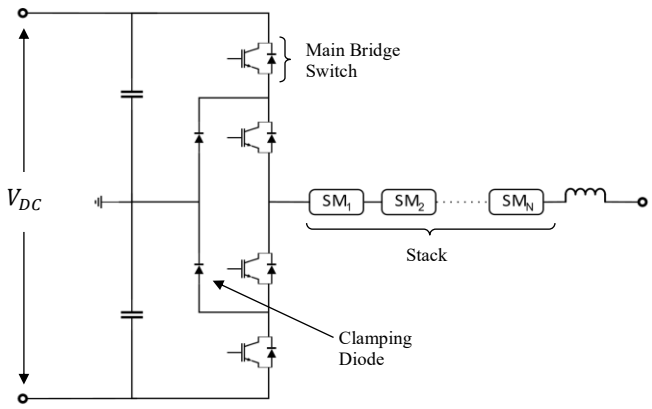

Fig. 1. Circuit schematic for one phase of the AC-CHB with a neutral point clamped main bridge. Main bridge switches and clamping diodes are made up of several series connected devices to provide sufficient voltage rating.

issue of dynamic voltage sharing during switching; however, this doubles the device count of the main bridge. The NPC-bridge produces a quasi-square-waveform while the SM stack produces a multilevel approximation of the waveform required for harmonic cancellation. The number of SMs can be scaled to provide a high-level output with low harmonic distortion. A filter inductor is then used to attenuate the switching frequency in the line current. Typical waveforms for the NPC-bridge voltage and the stack voltage are shown in Fig. 2.

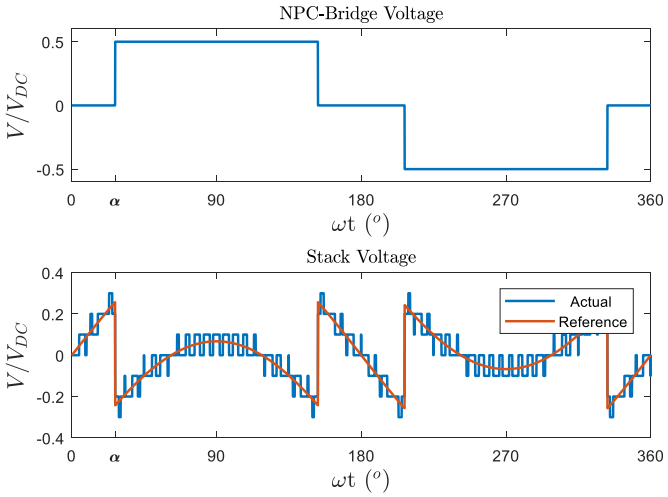

Fig. 2. Typical per phase waveforms for the NPC-bridge voltage and the stack voltage under normal conditions. α denotes the switching angle of the NPC-bridge.

The stack must be capable of producing both negative and positive voltages and therefore requires FB SMs. The stack voltage refence is given by

$$V_{stack} = \hat{V}_{AC} \sin(\omega t) - V_{\mathrm{NPC}}\,, \tag{1}$$

where $\hat{V}_{AC}$ is the peak AC voltage reference given by the controller and V_{NPC} is the voltage produced by the NPC-bridge.

The choice of the switching angle of the NPC-bridges, α, will affect the stack voltage waveform and will in turn affect the energy exchange in the stack, the required number of SMs, and the energy storage requirement of the stack. The sections below

describe the relationship between α and these design parameters, and they are then followed by a discussion of the optimum value for α.

A. Energy Balancing

To successfully control SM capacitor voltage, it is necessary that the energy flow into the stack is equal to the energy flow out of the stack. To achieve this energy balance, the converter must operate with a modulation ratio, m, of [16]

$$m = \frac{\hat{V}_{AC}}{V_{DC}} = \frac{2}{\pi}\cos(\alpha)\,, \tag{2}$$

where V_{DC} is the DC-link voltage. This condition is similar to the 'sweet spot' operation of the AAC; however, in this case α can be chosen to give a desired operating condition.

B. Number of Sub-Modules

The number of SMs per stack, N, will impact the cost, size and efficiency of the converter. Thus, it is important that the factors which affect N are understood so that it can be suitably chosen. The minimum number of SMs required is dependent on the peak stack voltage, $\hat{V}_{stack}$, and the SM voltage, V_{SM}, and is given by

$$N \geq \hat{V}_{stack}/V_{SM}, \tag{3}$$

V_{SM} is a parameter to be chosen by the designer and will be dependent on the desired number of voltage levels, losses and device cost and availability. For reduction of conduction power loss, the largest voltage SM feasible with IGBTs chosen for low switching loss is the favored choice. Under normal conditions the peak stack voltage is dependent on α and is given by

$$\hat{V}_{stack} = \max\left[\ \hat{V}_{AC}\sin(\alpha),\ \ \hat{V}_{AC}\sin(\alpha) - \frac{V_{DC}}{2}\ \right]. \tag{4}$$

During a DC fault, the voltage of one or both DC poles falls to zero. If DC fault ride-through is desired, the stack must be capable of producing the full AC voltage waveform and therefore $\hat{V}_{stack} = \hat{V}_{AC}$.

For some values of α, the difference between the required number of SMs during normal operation and during DC faults can be quite large; therefore, providing DC fault ride-through capability can represent a high cost in terms of efficiency and device count.

C. Energy Storage Requirement

In this section, the energy storage requirement for the NPC-AC-CHB is derived using the technique demonstrated in [12]. SM capacitors represent a significant contribution to the total converter size and weight. In a typical MMC for HVDC, SM capacitors account for 50% and 80% of the total converter size and weight respectively [18]. Therefore, it is desirable to design the converter such that the SM capacitor size is minimized. The minimum total capacitance within a stack that is required to prevent the SM voltage from breaching a specified deviation limit, ΔV (in per unit), is given by [12]

$$C_{stack} \geq \frac{\Delta E_{stack}^{max}}{2\ {V_{SM}}^2\ \Delta V}\,, \tag{5}$$

where ΔE_{stack}^{max} is the maximum energy deviation of the stack for the defined operating range of the converter. V_{SM} is limited by component voltage ratings and ΔV is limited to prevent over-voltage; however, ΔE_{stack}^{max} is dependent on the stack voltage waveform and can thus be minimize by choosing an appropriate value for α.

By considering (1) and (2), and performing a Fourier series expansion of V_{NPC}, the stack voltage is found to be

$$V_{stack} = \frac{V_{DC}}{\pi}\sum_{n=2}^{\infty}\frac{(-1)^n-1}{n}\cos(n\alpha)\ \sin(n\omega t)\,. \tag{6}$$

This can then be used to determine the stack energy waveform;

$$E_{stack} = \int_0^t V_{stack}\ I_{AC}\ dt \tag{7}$$

$$= \frac{|S|}{3\,\omega}\sum_{n=2}^{\infty}\frac{2}{mn\pi}\frac{(-1)^n-1}{n^2-1}\cos(n\alpha)\,[\sin(n\omega t)\cos(\,\omega + \phi)\ - n\,cos(n\omega t)sin(\omega t + \phi) + n\,sin\phi], \tag{8}$$

where S is the rated apparent power and $I_{AC} = \hat{I}_{AC}\sin(\omega t + \phi)$. ΔE_{stack} is defined as the difference between the maximum and minimum stack energy for a given value of α and ϕ. ΔE_{stack}^{max} is then determined by finding the maximum value of ΔE_{stack} within the operating range of ϕ (i.e. worst-case scenario) for a fixed value of α. A ratio, $K_{\Delta E}$, can be defined such that the energy storage requirement of various converter designs can be compared easily, where

$$\Delta E_{stack}^{max} = K_{\Delta E}\frac{|S|}{3\omega}\,. \tag{9}$$

D. Third Harmonic Cancelation

For cases in which a delta-connected transformer is used for grid interconnection, the transformer can be used to remove the third harmonic component. This can be utilized to reduce the energy storage requirement of the stack and the required number of SMs. *During normal operation*, the third harmonic component of the NPC waveform does not need to be cancelled by the stack, this removes the $n = 3$ component in (6). As will be shown later, this reduces the energy storage requirement of the stack. *During DC faults*, third harmonic injection can be used to reduce $\hat{V}_{stack}$ and thus reduce the required number of SMs for fault ride-through. The optimum magnitude for the third harmonic in this case is $\hat{V}_{AC}/6$, which gives $\hat{V}_{stack} = \sqrt{3}/2\ \hat{V}_{AC}$.

For the wye-connected case, the third harmonic component of the NPC waveform must be cancelled by the stack voltage waveform as described in (6).

E. Reliability

For the converter to remain operational despite internal device faults, it is important to design redundancy into the converter. In the main bridge, redundancy can be achieved by adding extra devices to the series strings that already form the main bridge switches and selecting devices which are known to consistently fail into a short-circuit condition such as press pack IGBTs [19]. A failure of one switch will raise the voltages on the others but sufficient margin will have been included for a given level of redundancy. Extra SMs can also be added to provide redundancy in the SM stacks. At MV, there are only a

few devices in the main bridge switches and only a few SMs in the stack, and so adding redundancy will incur an increase in losses that is more significant than in HV converters. However, this disadvantage is common to all MV converters. To avoid high levels of redundancy, and the associated losses, it may be preferable to use reactive maintenance rather than scheduled maintenance for MV converters [20].

III. Optimum Operating Conditions

This section will discuss the optimum value for α in terms of the minimization of the number of SMs and the energy storage requirement for both the wye and delta-connected cases.

A. Energy Storage Requirement

As discussed previously, $K_{\Delta E}$ provides a measure by which the energy storage required to limit SM voltage ripple of different converter designs can be compared. Fig. 3 shows the relationship between $K_{\Delta E}$ and α; this can be used to select a value for α which minimizes the energy storage requirement. $K_{\Delta E}$ has been calculated for the worst-case scenario across the full range of ϕ; however, in practice it is possible to define a more limited operating range.

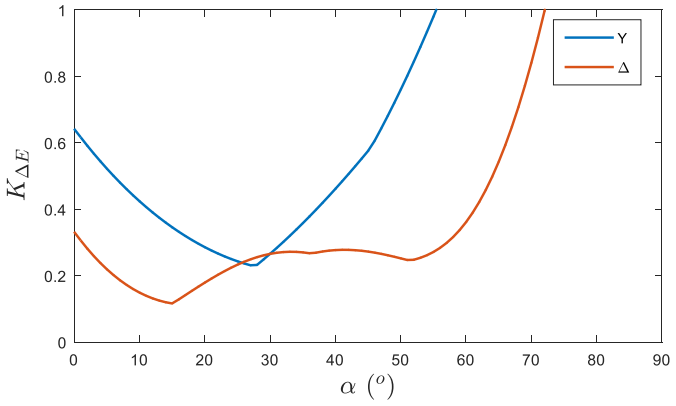

Fig. 3. The relative level of energy storage required, $K_{\Delta E}$, for different values of switching angle, α. The delta (Δ) and wye (Y) connected cases are both shown. The method used for the calculation of $K_{\Delta E}$ is described in section II.C.

For the wye-connected case, it is found that the energy storage requirement is minimized at $\alpha = 27°$; giving $K_{\Delta E} = 0.23$. For the delta-connected case, it is found that the energy storage requirement is minimized at $\alpha = 15°$; giving $K_{\Delta E} = 0.12$. For both cases this is a very small stack capacitor requirement in comparison with that of an MMC, as will be shown in Section V. At such low levels of energy deviation, capacitor voltage ripple during normal operation may no longer be the limiting factor and instead voltage deviation during faults may need to be considered. However, this is dependent on the operating range of the converter and the external circuitry in the system and so is not considered here. Alternatively, chopper resistors could be installed to protect SM from over-voltage during fault transients.

B. Number of Sub-Modules

In section II.B the method for determining the minimum number of SMs required, N, was described and it was shown that $\hat{V}_{stack}$ is proportional to N for a given SM voltage. Fig. 4 shows the relationship between $\hat{V}_{stack}$ and α, from which the value of α that minimizes N can be determined.

For the case *without* fault ride-through capability, the stack is sized only to meet the requirement under normal conditions. For the case *with* fault ride-through capability, the stack must be sized such that the requirements under fault condition and normal conditions are met.

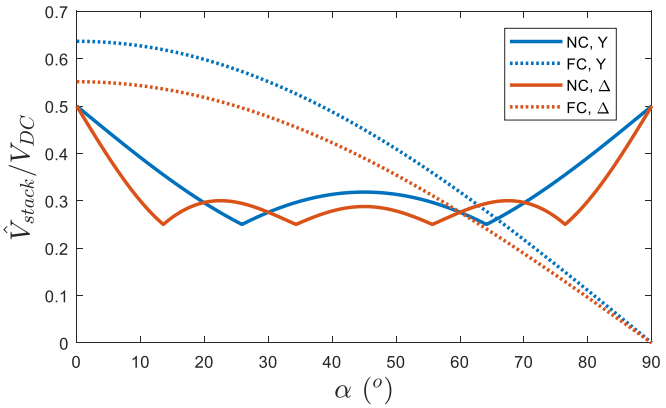

Fig. 4. The relationship between the maximum stack voltage, $\hat{V}_{stack}$, and the NPC switching angle, α. Both normal conditions (NC) and DC fault conditions (FC) are shown for cases with delta (Δ) and wye (Y) connections.

C. Summary

The previous sections have outlined the operating conditions which minimize the energy storage requirement and the number of SMs required. However, when choosing an appropriate value for α, both of these factors must be considered simultaneously.

For the case *without* DC fault ride-through, there exists a choice of α that effectively minimizes both energy storage requirement and the number SMs; $13.5° - 15°$ and $26° - 27°$ for the delta and wye-connected cases respectively.

For the case *with* DC fault ride-through, there is no such optimum value and instead there exists a trade-off between the number of SMs and the energy storage requirement. The choice of α then depends on what is of greater priority to the designer, efficiency or capacitor size. Another factor to be considered is the modulation ratio, m. It is impractical to operate with large values of α as this corresponds to small values of m, see (1), this further limits the minimization of N.

To break away from the inherent compromise between efficiency and capacitor size when providing DC fault-ride through capability, two alternatives to the classical FB SM topology will be presented in the next section.

IV. Divisible Sub-Module Topologies

DC fault ride-through is a highly valuable property; however, as shown in the previous section, this results in compromised operation of the NPC-AC-CHB. Two new SM topologies aim to increase the voltage capability of the stack during faults to provide fault ride-through while also being able to operate with a high efficiency during normal operation. One topology utilizes reverse-blocking IGCTs and the other uses ultra-fast mechanical switches but the principle behind the two topologies is the same.

A. Reverse-Blocking IGCT Topology

This topology utilizes reverse-blocking IGCTs (RB-IGCTs) which have been proposed for use in solid-state DC circuit breakers [21], and are capable of blocking both forward and reverse voltages, but can only conduct forward currents [22]. RB-IGCTs have also been shown to have very low conduction losses, with a voltage drop of just 0.9 V at 1 kA/125 °C for the 2.5 kV version [22].

A circuit schematic of the proposed Divisible SM (DSM) topology is shown in Fig. 5. Note that because the RB-IGCT can only conduct forward currents, two devices need to be placed in anti-parallel.

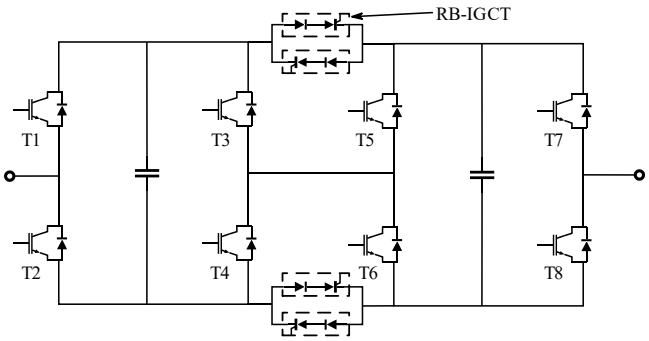

Fig. 5. Circuit schematic for the proposed Divisible sub-module topology with reverse-blocking IGCTs. Note that the reverse-blocking IGCT is made of a single die but is displayed as two components in the circuit.

During normal operation; the RB-IGCTs are on, the central four IGBTs (T3-6) are off, and the four outer IGCTs (T1-2 and T7-8) operate as the left and right bridge of a regular FB SM. In this way, the SM is effectively a single FB with two capacitors in parallel.

When a fault is detected; the RB-IGCTs turn off and the central four IGBTs become active. This divides the SM into two series connected FBs and doubles the voltage capability of the SM; therefore, DC fault ride-through can be achieved with half the number of SMs.

Following the clearance of a fault, the two FBs are merged to resume the normal operating mode through placing their capacitors back into parallel connection. Care must be taken when merging SMs as differences in capacitor voltages will result in a large inrush current. This can be solved by using sorting algorithms to bring the capacitor voltages close together before merging and by inserting a small impedance in series with the capacitors with an optional contactor to by-pass the impedance once the voltages have completely equalized.

The low conduction losses of the RB-IGCT and the fact that the central IGBTs are not in the conduction path during normal operation means that there is only a small rise in the conduction losses compared to a FB SM. Furthermore, the RB-IGCTs are not switching during normal operation so there is no increase in switching losses, but there is a penalty in terms of device count.

The voltage doubling capability of this topology could also be used to provide redundancy in the SM stack without a loss of efficiency. In the event of a SM failure, another SM could divide in order to compensate for the loss of voltage from the failed SM. However, the loss of capacitance in the stack as a result of the failure would mean that the rated power would have to be reduced. Furthermore, the loss of a DSM would remove DC fault ride-through capability until the faulted SM is replaced. If these constraints are unacceptable then an extra DSM would be required.

B. Mechanical Switch Topology

This topology uses ultra-fast mechanical switches which have been proposed for use in DC circuit breakers and have been shown to be capable of switching times below 1 ms [23]. A circuits schematic for the proposed topology is shown in Fig. 6.

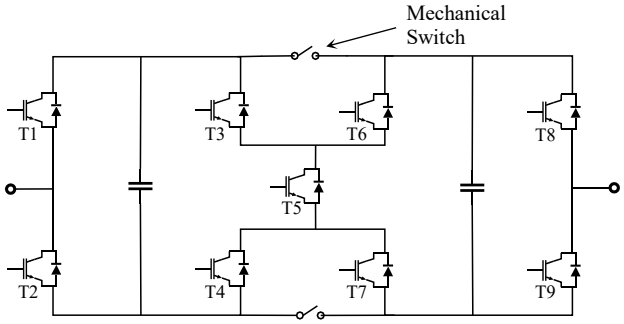

Fig. 6. Circuit schematic for the proposed Divisible sub-module topology with mechanical switches.

During normal operation, the mechanical switch is closed and the five central IGBTs (T3-7) are off; and so, the SM acts as a single FB with two parallel capacitors.

When a fault is detected, the center-most IGBT, T5, remains off but the other four central IGBTs (T3, T4, T6 and T7) turn on. The mechanical switch is then opened commutating the current into the bypass current paths created by T3 and T6, and T4 and T7. Once the mechanical switch has successfully opened, the center-most IGBT turns on creating two series connected FBs.

The bypass current paths prevent arcing in the mechanical switches by providing a low inductance conduction path for the current to commutate into while the switch is in the process of opening. The fault current will continue to rise until the stack can provide sufficient voltage to oppose the AC voltage without the DC voltage present; therefore, fast mechanical switches are required to prevent the fault current from damaging the components before it is brought under control. The rate of rise of fault current, and therefore the minimum opening time, will depend on the inductance in the circuit and the fault conditions. However, the sub-millisecond switching of ultra-fast mechanical switches is thought to be sufficient for most applications. The arc-less commutation into low inductance paths has been demonstrated experimentally for a mechanical switch at 4.5 kV/1.5 kA in [23]. Note that the auxiliary circuitry in [23] is not needed in the proposed SM as the SM IGBTs are used to provide the bypass current paths. It was shown that through the use of ultra-fast mechanical switches an opening time of just 300 µs can be achieved [23]. The main benefit of using mechanical switches over RB-IGCTs is that they have negligible conduction losses but require an extra IGBT per SM.

V. Topology Comparison

In this section the previously discussed topologies will be compared in terms of efficiency, energy storage requirement and device count. The following variations of the NPC-AC-CHB will be considered:

(1) FB SMs with DC fault ride-through,

(2) Divisible SMs with RB-IGCTs,

(3) Divisible SMs with mechanical switches,

(4) FB SMs without DC fault ride-through,

all at $\alpha = 27°$. These topologies are also compared to the following established multilevel topologies: FB-MMC, Hybrid MMC (with $m = 0.6$ [7]), AAC, 2L-AC-CHB, and HB-MMC.

The topologies will be compared for a transformer-less wye-connection to an 11 kV/50 Hz AC grid; therefore, there will be differences in the DC voltage used to accommodate the optimum voltage ratio of the different designs. A comparison for the delta-connected transformer case with a constant DC voltage is given in the appendix. The characteristics considered for the topology comparison are summarized in Table 1.

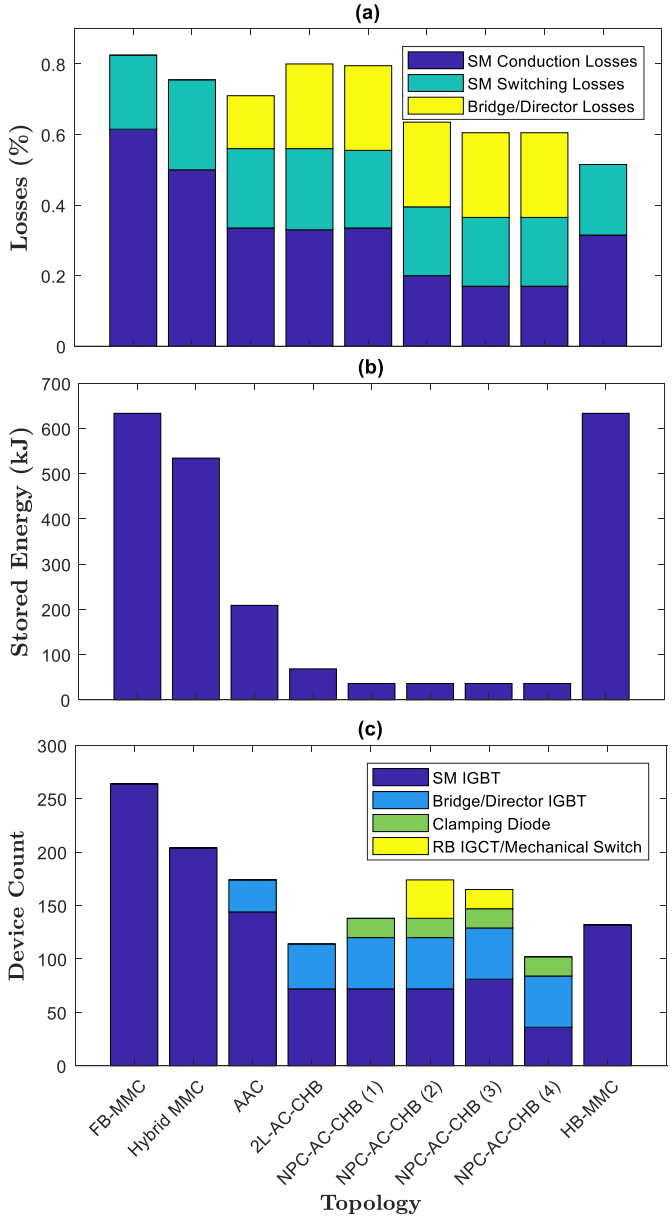

Fig. 7. The (a) losses, (b) total energy storage and (c) device count for various wye-connected converter topologies for the 11 kV, 20 MVA case study.

TABLE 1
CONVERTER CHARACTERISTICS

Characteristic	Value
AC Grid Voltage	11 kV
MVDC Voltage	17 – 22 kV
Sub-Module Voltage	2 kV
Apparent Power Rating	20 MVA
Operating Range for ϕ	$0° - 360°$

A. Losses

Power losses were estimated through simulation in Matlab/Simulink® by using linear approximations of the V-I characteristics given in the datasheet of the semiconductor devices used. 3.3 kV/1.5 kA IGBTs (FZ1500R33HE3) from Infineon were selected for the SM IGBTs in all topologies, 4.5 kV/2.0 kA StakPak IGBTs (5SNA 2000K450300) from ABB were selected for director switches and main bridge switches, and 6 kV/1.7 kA standard recovery diodes (5SDD 17F6000) were used for the clamping diodes. The V-I characteristics of the RB-IGBTs was taken from [22] and the losses in the mechanical switches were assumed to be negligible. Losses are calculated for the case when the converter is operating at 20 MW and 0 MVAr and are shown in Fig. 7.a The HB-MMC has the highest efficiency of all the compared topologies but the NPC-AC-CHB (3) has the lowest losses of the topologies with DC fault ride-through. The Divisible SM topologies, (2) and (3), provide a significant reduction in SM conduction losses compared to the NPC-AC-CHB (1) because of the reduced number of devices in the conduction path but the NPC-bridge losses and SM switching losses are unchanged.

B. Energy Storage Requirement

The energy storage requirement of the various converter designs was calculated by extending the method used in section II.C to all the compared topologies, as is shown in detail in [12]. The energy deviation per stack for the compared topologies is shown for different phase angles, ϕ, in Fig. 8. The total converter energy storage requirement for a worst-case voltage deviation of 10% ($\Delta V = 0.10$) is shown in Fig. 7.b for the case-study converter specification. Note that all four of the NPC-AC-CHB topologies have the same energy storage requirement, this is because they are all operated at $\alpha = 27°$. The energy storage requirement of the NPC-AC-CHB topologies is approximately half that of the 2L-AC-CHB and one eighteenth that of the MMC. The AAC also has a relatively small energy storage requirement, around one third that of the MMC.

C. Device Count

The total converter device count was compared for the various converter designs. Inductors and capacitors were not included in the device count as the size of such devices varies greatly depending on the device rating. A comparison of capacitor size is given in section B. No comparison is made in terms of inductor size in this paper, although it is worth noting that the 2L and NPC-AC-CHB do not require arm inductors. Fig. 7.c shows a comparison of the converter topologies in

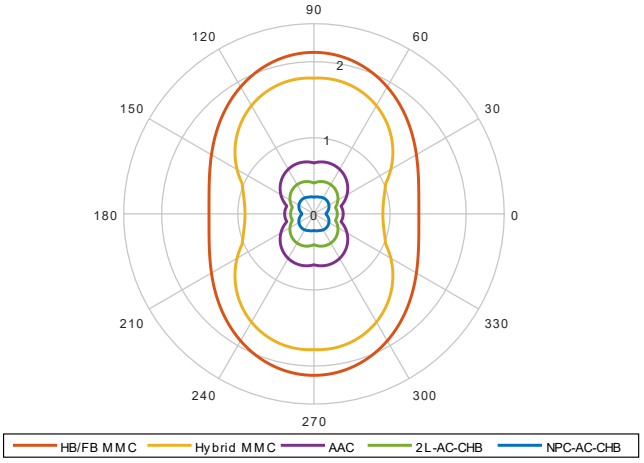

Fig. 8. Polar plot showing the energy deviation per stack in kJ/MVA on the radial axis against phase angle, ϕ, for various converter topologies. The NPC-AC-CHB calculation was made at $\alpha = 27°$ and is the same for all four variants.

terms of device count. The NPC-AC-CHB (4) topology has the lowest device count of all the compared topologies, whereas the 2L-AC-CHB has the lowest device count of those with fault ride-through capability. Note that Fig. 7.c does not consider the relative size of devices.

D. Summary

For the case *with* DC fault ride-through; the NPC-AC-CHB topologies are the most compact solutions due to their low energy storage requirement. However, the NPC-AC-CHB (1) suffers from a low efficiency. Through the use of DSMs, the losses are reduced by 32 kW for the RB-IGCT case and by 38 kW for the mechanical switching case; however, this comes at a cost of an increased device count. Taking the cost of electricity to be 0.1 £/kWh and a discount rate of 2.5% to account for interest rates and inflation [24], the total savings equate to £704,000 and £836,000 respectively over the 40-year lifetime of the converter and thus can be expected to outweigh the cost of 36 and 27 devices respectively. Furthermore, the lower losses will reduce the costs associated with cooling. Therefore, the NPC-AC-CHB with DSM topologies look to be an attractive solution to DC fault-ride through both in terms of cost and volume.

For the case *without* DC fault ride-through; the NPC-AC-CHB (4) looks to be very attractive in terms of volume, with a much lower energy storage requirement and reduced device count compared to the HB-MMC. However, there is a cost in terms of efficiency. Therefore, the NPC-AC-CHB (4) is best suited for uses in which volume is a priority.

VI. Simulation Results

The simulation results for the NPC-AC-CHB (2), which has Divisible RB-IGCT SMs, during both an unbalanced AC fault and a DC fault will now be shown for proof of concept. The simulation results for the other NPC-AC-CHB topologies will not be shown as the operation is essentially the same. The simulation was built in Matlab/Simulink® using the Power Systems toolbox with the characteristics shown in Table 1. The converter was connected to an 11 kV/50 Hz three-phase grid without a transformer. Operating with $\alpha = 27°$ gives a modulation ratio of 0.567 and thus a DC voltage of 19.4 kV was selected. This gives a maximum stack voltage of 5 kV during normal operation, see Fig. 4, and 11 kV during DC faults. Thus, the converter was designed with three 2 kV DSMs giving a maximum stack voltage of 6 kV during normal operation and 12 kV during DC faults. RB-IGCTs were modelled as a diode and a thyristor in series. SM capacitors were sized using (5) with $\Delta V = 0.10$, giving two 1 mF capacitors per SM to make a total stack capacitance of 6 mF.

A. Unbalanced AC Fault

In this scenario one of the AC voltages drops to 0.3 pu at 0.05 s before rising back to 1.0 pu at 0.35 s; simulation results are shown in Fig. 9. The converter is still functional despite this large deviation from normal operation and can provide reactive power to the grid during the fault. No real power can be supplied under these conditions because the converter is not operating at the energy balancing point defined in (2). SM voltages are controlled both during and at the instance of the fault. DC voltage is unaffected, so peak stack voltage need not exceed 6 kV, this means that even the NPC-AC-CHB (4) can operate under AC faults. Note that the maximum reactive power that can be supplied during an AC fault is well below 1.0 pu; this is because the operating point is far from optimum, resulting in a greater level of energy deviation.

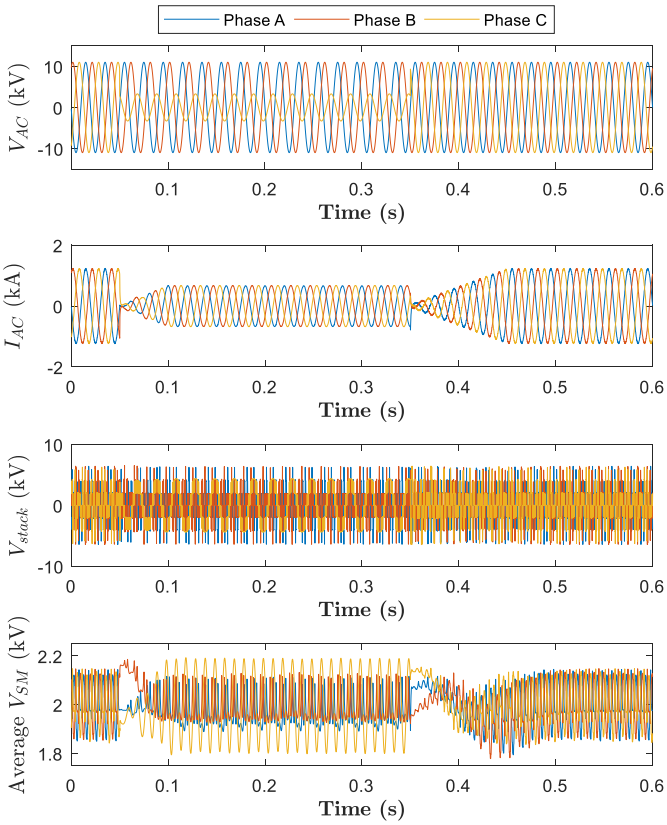

Fig. 9. Simulation results showing the operation of a 20 MW NPC-AC-CHB during a single-phase AC fault.

B. DC Fault

In this scenario the DC voltage drops to 0.0 pu at 0.05 s before ramping back to 1.0 pu at 0.35 s; simulation results are shown in Fig. 10. As with the previous scenario, the converter can provide a limited amount of reactive power during the fault.

The stack is now producing the full AC voltage waveform and so to limit the voltage deviation to within 10%, the reactive power cannot exceed 0.23 pu. SM voltages are controlled both during and at the instance of the fault. Note that since the DC voltage has dropped, the peak stack voltage has increased, requiring the DSMs to divide. It can be seen that there is no flow of fault current from AC to DC side. The NPC-AC-CHB (4) is not capable of providing sufficient voltage to control the fault current, so a DC circuit breaker would be required.

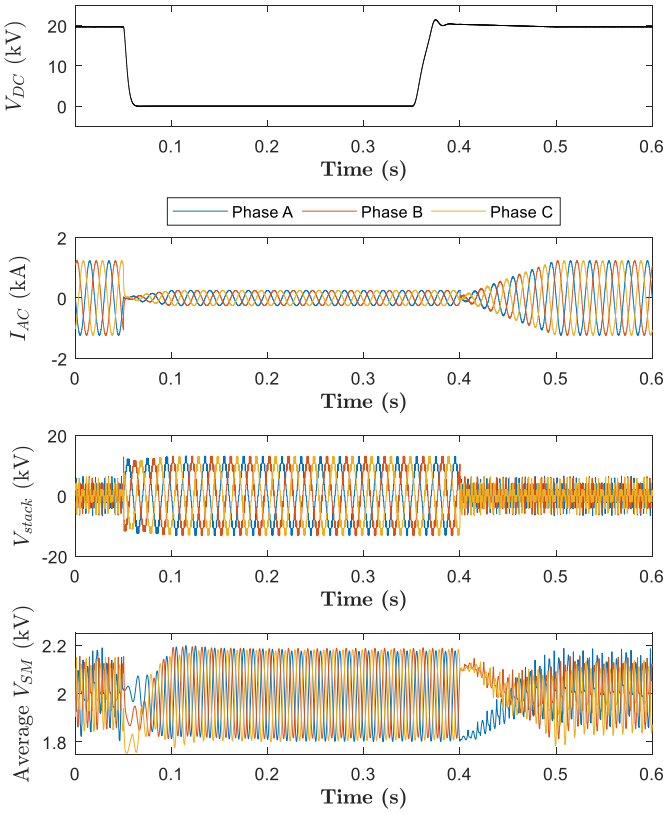

Fig. 10. Simulation results showing the operation of a 20 MW NPC-AC-CHB during a single-phase DC fault.

C. Mechanical Switching

In the RB-IGCT topology, the SM is able to divide instantly. In contrast, the non-instantaneous opening time of the mechanical switch means that the process of SM division is more complex in its case and will be described in detail here. Figure 11 shows detailed simulation results for the opening of the mechanical switches in a DSM when a fault occurs during the worst-case scenario. The worst-case scenario is when the fault occurs when the grid voltage and SM current are at their peak value and of opposite sign, such that a reduced blocking voltage results in a rising fault current. Details concerning the opening and commutation times of the mechanical switch are based on experimental results presented in [23].

Before the fault, the displayed SM is in the zero-voltage state (seen in bottom graph of Figure 11) and all the current is conducted through T1, T8 and the upper mechanical switch (MS+).

At point A, the fault occurs, and the SM enters the blocking state. The SM current is then shared between the two mechanical switches as it passes through both capacitors in parallel producing a blocking voltage of 2 kV. At the same time, the IGBTs creating the bypassing current paths are switched on. Only a small amount of current is conducted through the bypassing IGBTs at this stage as they have a high on-state resistance relative to the mechanical switches. An opening signal is also sent to the mechanical switches, but these remain closed due to a mechanical time delay of 180 µs. During this time, the SM current begins to rise as there is insufficient blocking voltage in the stack.

At point B, the mechanical switches begin to open and a small arc voltage (< 5 V) commutates the current into the bypassing current paths.

At point C, the current has fully commutated into the bypassing current paths. The current continues to be conducted through the bypassing IGBTs to allow time for the mechanical contacts to separate far enough to be able to support the SM voltage.

At point D, the bypassing current paths are blocked, forcing the current through both capacitors in series via T3, T5 and T7, giving a blocking voltage of 4 kV. The SM stack is now capable of blocking the grid voltage and so the SM current begins to reduce.

After the fault is cleared and normal operation is resumed the SMs are merged, this process is independent of the closing time of the mechanical switch as it can be completed by the bypassing current paths. The mechanical switches can later be closed to resume high efficiency operation.

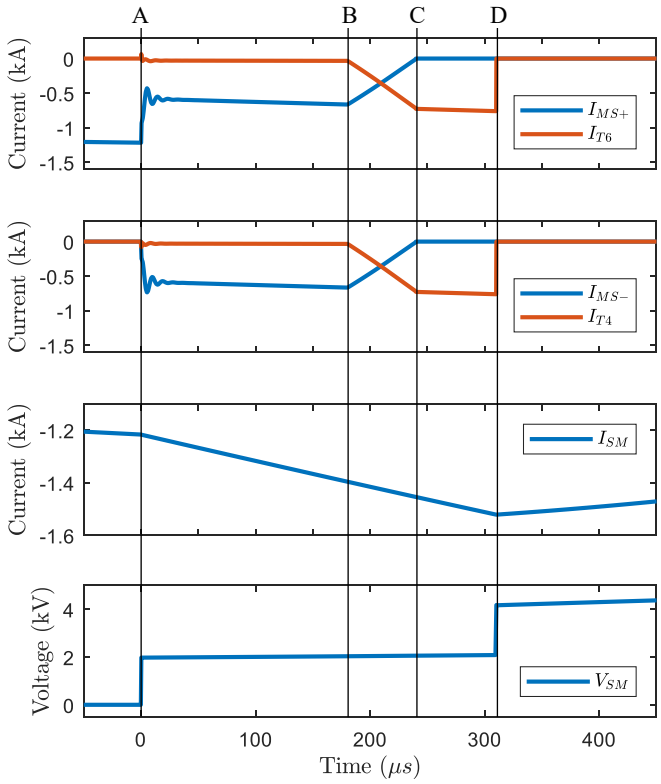

Figure 11. Simulations results for the dividing of a DSM with mechanical switches following a DC fault at $t = 0\ \mu s$. I_{T6} and I_{T4} are the currents through T6 and T4, see Figure 6. I_{MS+} and I_{MS-} are the currents through the upper and lower mechanical switches respectively. I_{SM} and V_{SM} are the SM current and voltage.

VII. Conclusion

This paper has analyzed the AC-CHB converter with an NPC main bridge and compared it with other topologies in the context of MVDC applications. The optimum operating conditions for NPC-AC-CHB have been defined and its operation has been demonstrated through simulation. Divisible SM topologies, which can provide DC fault ride-through capability without compromising efficiency, have been proposed. The proposed topologies have been compared to established designs, such as the MMC, AAC and 2L-AC-CHB, in terms of efficiency, energy storage requirement and device count. For cases in which DC fault ride-through is not desired, the NPC-AC-CHB appears to be a compact solution with a very small energy storage requirement and low device count, but marginally higher losses compared to the half-bridge MMC. For cases in which fault ride-through is required, the NPC-AC-CHB with Divisible SMs has been shown to have the highest efficiency and the lowest energy storage requirement when compared to the other topologies studied. Thus, the NPC-AC-CHB has been shown to be a promising solution for AC-DC conversion in MVDC systems.

Appendix

A comparison of the topologies for the case in which the converter is connected to the 11 kV grid via a delta-connected transformer was also made. All topologies have a DC voltage of 20 kV, and the turns ratio in the transformers was used to compensate for the varying modulation index of the different topologies. NPC-AC-CHB topologies were operated at $\alpha = 15°$. All other converter parameters are consistent with the description in section V. Figure A.1 shows the losses, stored energy, and device count for the various converter topologies.

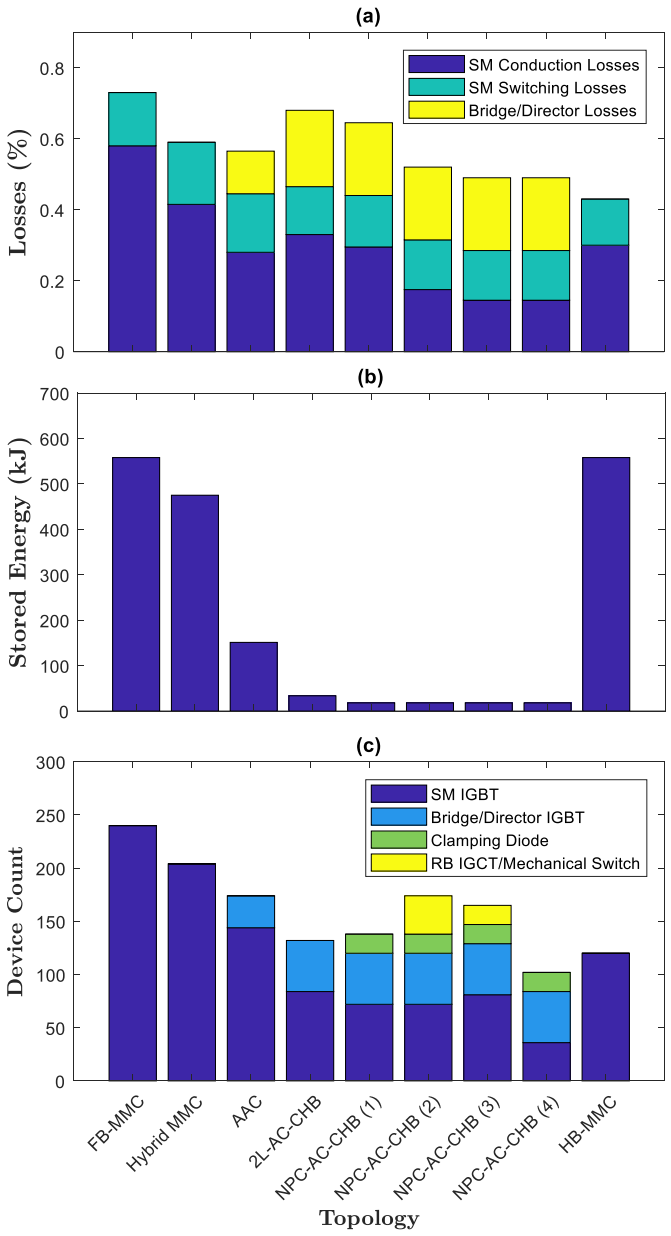

Figure A.1. The (a) losses, (b) total energy storage and (c) device count for various delta-connected converter topologies for the 11 kV, 20 MVA case study.

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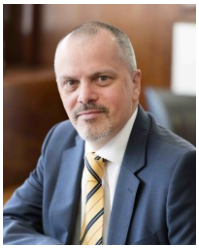

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