An Ultra-Wideband-Inspired System-on-Chip for an Optical Bidirectional Transcutaneous Biotelemetry

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***Abstract*—This paper describes an integrated communication system, implementing a UWB-inspired pulsed coding technique, for an optical transcutaneous biotelemetry. The system consists of both a transmitter and a receiver facilitating a bidirectional link. The transmitter includes a digital data coding circuit and is capable of generating sub-nanosecond current pulses and directly driving an off-chip semiconductor laser diode including all bias and drive circuits. The receiver includes an integrated compact PN-junction photodiode together with signal conditioning, detection and digital data decoding circuits to enable a high bit rate, energy efficient communication. The proposed solution has been implemented in a commercially available 0.35 μm CMOS technology provided by AMS. The circuit core occupies a compact silicon footprint of less than 0.13 mm^2 (only 113 transistors and 1 resistor). Post-layout simulations have validated the overall system operation demonstrating the ability to operate at bit rates up to 500 Mbps with pulse widths of 300 ps with a total power efficiency (transmitter + receiver) lower than 74 pJ/bit. This makes the system ideally suited for demanding applications that require high bit rates at extremely low energy levels. One such application is implantable brain machine interfaces requiring high uplink bitrates to transmit recorded data externally through a transcutaneous communication channel.**

I. Introduction

Recent progress in implantable neural microsystems have enabled combining high density cortical recording, signal processing, decoding and communication for a variety of scientific and medical applications. Applications for Brain Machine Interfaces (BMIs) in the future will utilise this functionality for actuation and communication in individuals with neurological disease and injury. A key challenge however in implantable device technology for such applications is how to achieve a high bandwidth biotelemetry in an energy efficient manner. These systems need also to operate with reduced size at low supply voltage and reduced power consumption whilst optimising electromagnetic (e.m.) compatibility and signal integrity [1], [2].

There has already been a significant amount of work in implementing a number of techniques mainly based on near and far field wireless data and/or power transfer. This includes carrier-based, narrow band and Ultra-WideBand (UWB) radio frequency (RF) links. These have however predominantly been applied to neuromodulation devices that require the downlink to have a higher bandwidth than the uplink. Downlink data has included control commands and sensory data (into the body), whereas uplink data (out of the body) has been mainly for diagnostic purposes. However for applications requiring high uplink bandwidths (e.g., required for BMIs) these methods face some fundamental limitations due to their relatively high-power consumption and low e.m. compatibility [3]–[6]. Optical biotelemetry links have been proposed that employ modulated or pulsed diode lasers as data transmitters and photodiodes as data receivers. These provide several desirable features such as an improved performance particularly in terms of device size, bit rate, power consumption and e.m. compatibility [2], [7]–[9]. Some improvements have been achieved by increasing the laser power, employing photodiodes with larger sensitive area and/or using modified On-Off Keying (OOK) based modulations. These approaches however tend to increase the laser/emitter response time and the signal-to-noise ratio thus limiting the system bandwidth and the maximum achievable data rate up to 100 Mbps with a power efficiency of 21 pJ/bit [2], [8], [10]. Recently, we have demonstrated an UWB-inspired optical wireless biotelemetry system implemented using commercial off-the-shelf components that is able to overcome these limitations reaching data rate up to 250 Mbps and 24 pJ/bit power efficiency [11].

This work develops this approach further by proposing a full-custom ASIC implementation of the complete bidirectional biotelemetry link. This integrates both the transmitter and receiver including all digital coding/decoding blocks as well as a laser diode driver and a photodiode transimpedance amplifier. The only external component required is the laser diode. The integrated circuit has been designed in AMS 0.35 µm CMOS technology (C35B4C3), with core circuit occupying a compact silicon footprint of only 0.13 mm^2 (113 transistors and 1 resistor). Post-layout simulations demonstrate the desired system functionality to achieve data rates up to 500 Mbps at an overall power efficiency of less than 74 pJ/bit.

II. System Overview

The proposed system is illustrated in Fig. 1. The communication architecture implements an UWB-inspired optical pulsed modulation technique allowing for a high bit rate link with low power consumption [7]. The system includes both a transmitter and a receiver within each of the implanted and external (body worn) modules. The transmitter takes, as input signals, the main clock *CLK_IN* and the bitstream *DATA_IN* to be coded/transmitted, whilst the receiver provides the recovered clock signal *CLK_OUT* and the decoded bitstream *DATA_OUT*.

The transmitter includes a *'digital coding'* block to modulate the voltage pulses and a *'laser driver'* block for biasing and driving the laser diode, converting the voltage into current pulses. The receiver includes a transimpedance amplifier (TIA) that converts current pulses into voltage pulses and a *'digital decoding'* block that takes the received voltage pulses and

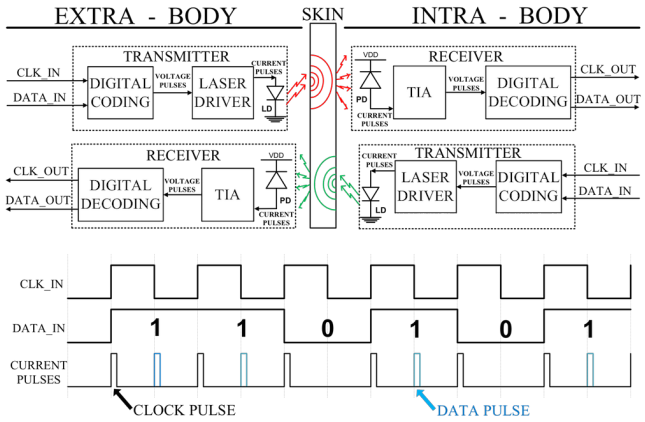


Fig. 1. System overview of the UWB-inspired optical communication link implementing a pulsed data coding technique with example timing diagram.

performs the clock and data recovery. Finally, the modulation approach implemented has been tailored for a semiconductor laser diode (LD) to generate the sub-nanosecond light pulses and a fast silicon photodiode (PD) to respond with corresponding current pulses.

A basic timing diagram is also illustrated in Fig. 1. The clock and data signals are combined into a single current pulse-based bitstream. A first pulse (i.e., the clock pulse) is always generated at the beginning of each bit period, independently of the symbol to be transmitted, allowing for the transmission of the clock needed for the transmitter-receiver synchronisation (i.e., clock recovery). Then, after half a period, if the symbol *'1'* is to be transmitted, a second pulse (i.e., the data pulse) is generated, while for the transmission of the symbol *'0'* there is not further current pulse (i.e., the current preserves its minimum value).

III. Circuit Implementation

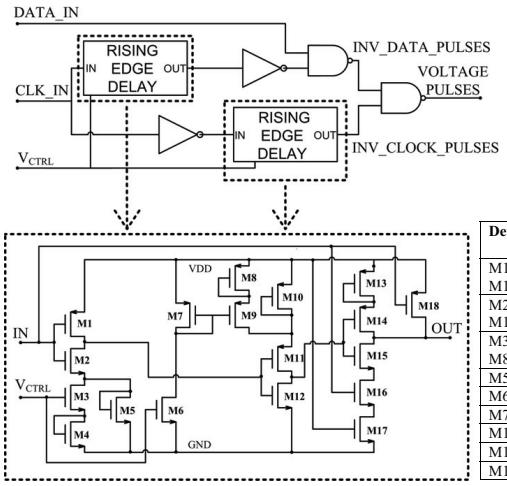
The core system including all components (except laser diode) has been implemented in AMS 0.35 µm CMOS technology. The design has in particular been optimised for data throughput, power consumption and silicon area.

A. Transmitter Circuits

The *'digital coding'* block is based on simple combinational logic, consisting of 2× NOT, 2× NAND and 2× rising edge triggered pulse generators, shown in Fig. 2. Starting from the clock input *CLK_IN*, the *'rising edge delay'* block generates voltage pulses with a variable width that is regulated by the control voltage V_{CTRL}. This is based on three inverter stages formed by the transistor pairs *M1–M2*, *M11–M12* and *M14–M15*. This operates as follows:

- When V_{CTRL}=*0 V*, diode-connected transistor *M5* defines the maximum resistance in the pull-down network of the *M1–M2* inverter stage. In a similar fashion diode-connected transistor *M10* sets the maximum resistance in the pull-up network of the *M11–M12* inverter stage. Under this operating condition the maximum delay is achieved.
- By increasing the value of V_{CTRL}, transistor *M3* and current mirror *M6–M7–M9* progressively turn on. This, in turn increases the current flowing through transistors *M4–M8*, resulting in an overall reduction in the delay between the rising edges of the input and the output signals.
- The circuit however is designed to directly respond to a falling edge of the input clock signal. This is achieved through transistor *M18* such that only the input rising edge is delayed by the *'rising edge delay'* block.

Referring now to the overall *'digital coding'* block, the input *CLK_IN* follows two different paths that provide pulse trains with a relative phase delay equal to 180° (i.e., half a clock period). These signals are then combined with the input data stream *DATA_IN* through the NAND gates so as to provide a single output pulse train incorporating both the *CLOCK_PULSE* and *DATA_PULSE* components (see Fig. 1).



Device	W (µm)	L (µm)
M1, M11, M14, M18	15	0.35
M2, M12, M15, M16	6	0.35
M3, M4, M8, M9	24	0.35
M5	6	12
M6	12	0.35
M7	15	100
M10	15	20
M13	15	10
M17	6	1

Fig. 2. Circuit schematic of the *'digital coding'* block.

This signal then feeds the laser driver circuit, shown in Fig. 3. This is based on a current mirror stage formed by transistors *M4–M5*, converting the *VOLTAGE_PULSES* into *CURRENT_PULSES* to directly drive the LD. Moreover, this allows for the regulation of both the pulsed current amplitude and the DC current level through the two control voltages DC_{CTRL} and AC_{CTRL} that act on transistors *M2* and *M3*, respectively.

The LD to be employed will be wire-bonded directly to the ASIC. This will be a high-speed Vertical Cavity Surface Emitting Laser (VCSEL), featuring compact size (even smaller than the ASIC) and fast response (high bandwidth) to pulsed modulations. The required VCSEL specifications are as follows: emitting wavelength λ in the range 800–1000 nm, a maximum output light power less than 2 mW, a beam diameter lower than 500 µm, a threshold current lower than 1 mA, rise and fall times lower than 100 ps (e.g., Philips ULM850-05-TN-N0101L [Online]). The wavelength (800–1000 nm) has been selected specifically to minimise issues related to scattering, propagation and attenuation due to the presence of the skin/tissue [12]. In this spectral region, an optical penetration depth higher than 2.5 mm and an absorption coefficient lower than 1.1cm^{-1} are achieved. Moreover, to avoid/reduce channel-crosstalk between the external and implanted devices during simultaneous bidirectional communication, two different LD emitting wavelengths λ of 850 nm and 980 nm have been chosen to be used in the external and implanted transmitters, respectively.

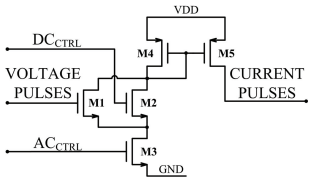
B. Receiver Circuits

Within the receiver subsystem, the main block is the PD interface circuit, shown in Fig. 4. This converts *CURRENT_PULSES* received from the PD and generates the *VOLTAGE_PULSES* signal. This is based on a single stage transimpedance amplifier (TIA) implemented by the transistors *M1–M5*, with resistor *R1* defining the transimpedance gain. Additional gain is provided through a cascade of three CMOS inverter stages implemented by transistor pairs *M6–M7*, *M8–M9* and *M10–M11*, generating the output signal *VOLTAGE_PULSES*. Furthermore, the R_{EXT} terminal allows for the overall gain to be precisely adjusted through an optional external resistor (i.e., connected in parallel with *R1*).

The proposed ASIC design additionally includes five different integrated PN-junction photodiode devices that target the following specifications: maximum responsivity>0.5 A/W (at λ=850 nm), junction capacitance<1 pF, rise/fall times<100 ps, reverse bias voltage<3.3 V (e.g., similar to Philips ULMPIN-10-TT-N0101U [Online]). The five photodiode prototypes have been designed to test different PN-junctions (n-well/p-substrate, n+/p-substrate) and geometries (single junction, multiple parallel-connected junctions). The single junction structures have active area 200×200 µm^2. The multi-junction structures tesselate 120× small unit cells aiming to minimise transit time (and thus maximise the bandwidth), with total active area 140×140 µm^2. All the prototype photodiode structures include an external guard-ring to uniformly biasing the underlying p-substrate.

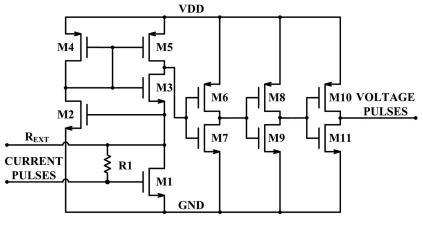
Resuming, the *VOLTAGE_PULSES* signal generated by the PD interface circuit then feeds the *'digital decoding'* block that performs the data and clock recovery (i.e., generating the *CLK_OUT* and *DATA_OUT* outputs). The circuit schematic is shown in Fig. 5. This consists of 2× D-type Flip-Flops (FF_D), 2× inverters, 1× *'rising edge delay'* block (described previously) and 1× *'phase control'* block. This operates as follows:

- The *VOLTAGE_PULSES* signal drives the clock input *CLK* of the first FF_D, with the data input *D* fixed to logic level *1*. In this way, the first incoming *CLOCK_PULSE* sets the output of the FF_D to a high logic level and thus any further *DATA_PULSE* cannot affect the FF_D output.



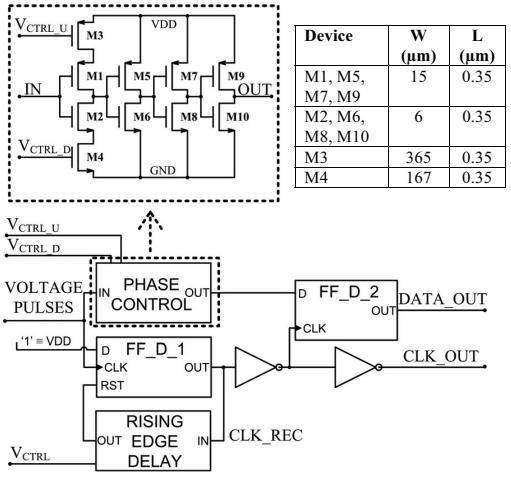
Device	W (µm)	L (µm)
M1, M3	12	0.35
M2	6	7
M4	18	0.35
M5	240	0.35

Fig. 3. Circuit schematic of the *'laser driver'* circuit (laser diode connected to the output node *CURRENT_PULSES* as shown in Fig. 1).



Device	W(µm)	L(µm)
M1, M2	500	0.35
M3	60	0.35
M4	100	0.35
M5	85	0.35
M6, M8, M10	18	0.35
M7, M9, M11	6	0.35
R1 = 600Ω	-	

Fig. 4. Schematic of photodiode interface circuit (photodiode connected to the input node *CURRENT_PULSES* as shown in Fig. 1).



Device	W (µm)	L (µm)
M1, M5, M7, M9	15	0.35
M2, M6, M8, M10	6	0.35
M3	365	0.35
M4	167	0.35

Fig. 5. Circuit schematic of the *'digital decoding'* block.

- The output signal of the FF_D_1 is then maintained through the *'rising edge delay'* block. After this fixed time delay, the *'rising edge delay'* triggers the FF_D's asynchronous reset pin *RST* to toggle its output back to the low logic level *0*. The system is now ready to accept the next *CLOCK_PULSE*.
- Since there is a fixed phase relationship between the *CLOCK_PULSE* and *DATA_PULSE* signals, it is essential to adjust through the *'rising edge delay'* block the pulse delay for different data rates such that: *T/2<pulse delay<T*, where T is the clock period (i.e., period between two consecutive *CLOCK_PULSE* signals).
- Consequently, the output of the first FF_D provides the recovered clock signal *CLK_REC* but with a duty cycle higher than 50% (i.e., half a clock period plus the additional pulse delay).
- The second FF_D then receives the inverted *CLK_REC* and acquires the data input provided by *DATA_PULSES*. In order to avoid a metastable state in FF_D_2, a *'phase control'* has been included to guarantee the FF_D_2 setup and hold times. Referring to Fig. 5, the *'phase control'* block consists of 4× inverter stages implemented by transistor pairs *M1–M2*, *M5–M6*, *M7–M8* and *M9–M10*. Also, transistors *M3–M4* are driven by control voltages V_{CTRL_U} and V_{CTRL_D} that allow for the pulse width of the received *VOLTAGE_PULSES* signal to be extended.
- Finally, FF_D_2 provides the decoded data *DATA_OUT* signal with a stable value corresponding to the rising edges of the recovered clock signal *CLK_OUT*.

IV. Post-Layout Simulation Results

The overall system has been developed using the Cadence Design Systems Virtuoso tool suite using foundry-provided simulation and physical verification models. All the blocks described previously have been integrated into a single integrated circuit design targeting a full-duplex (concurrent up- and downlink transmissions) bitrate of 500 Mbps. The complete system layout including integrated photodiodes and physical bondpads (with ESD protections) is shown in Fig. 6.

The overall size of complete test chip design is 1.6×2 mm^2. It should be noted that the core circuits themselves only occupy approximately 0.13 mm^2 (the transmitter: 53 transistors and 1 resistor; the receiver: 60 transistors). The circuit operates

from a single 3.3 V supply voltage, requiring a maximum total power consumption (with both transmitter and receiver active) of less than 37 mW at a data rate of 500 Mbps and a pulsed signal width of 300 ps. Fig. 7 shows a post-layout simulation (transient analysis) demonstrating the system operating with a clock signal of 500 MHz (i.e., 500 Mbps data rate). The transmitter uses a pulse width (i.e., for *CURRENT_PULSES*) of 300 ps with minimum and maximum current levels of approximately 1 mA and 25 mA, respectively (for driving the LD). On the other hand, the receiver takes a *CURRENT_PULSE* input signal of about 70 µA (emulating the expected PD photocurrent based on our previous measurements [7], [11]). It is important to observe also that the recovered clock signal presents a duty-cycle of about 70% which, if required, could be suitably compensated by a duty-cycle correction circuit [13].

These results demonstrate that the transmitted repeated bit sequence $\{0,1\}$ is correctly decoded by the receiver and is in synchronisation with the recovered clock signal. Moreover, multiple post-layout simulations have been performed to fully characterise the system at different operating frequencies (i.e., different data rates) in addition to varying pulse widths – to assess the overall system power consumption. Table I summarises the simulated power efficiencies of both the transmitter and receiver blocks for frequencies of 125 MHz, 250 MHz and 500 MHz, and pulse widths of 300 ps and 500 ps for a fixed pulse current of 25 mA.

TABLE I
POWER EFFICIENCY OF TRANSMITTER (TX) AND RECEIVER (RX) SUB-SYSTEMS UNDER DIFFERENT OPERATING CONDITIONS.

Data rate (Mbps)	**Pulse width = 300 ps**		**Pulse width = 500 ps**	
	Tx (pJ/bit)	**Rx (pJ/bit)**	**Tx (pJ/bit)**	**Rx (pJ/bit)**
125	85	121	94	121
250	57	67	65	67
500	34	40	41	40

V. CONCLUSION

This work has reported a CMOS integration of a full-duplex communication system, implementing an UWB-inspired pulse coding technique, for an optical transcutaneous biotelemetry. Post-layout simulations have shown that the developed system is capable of transmitting data rates up to 500 Mbps with a 74 pJ/bit total energy efficiency. This capability (both the data throughput but also power levels) would allow for future integration with implantable intracortical recording systems [14]–[16] allowing for transmission of over 2,000 channels of raw data. The full custom integrated circuit is currently in fabrication.

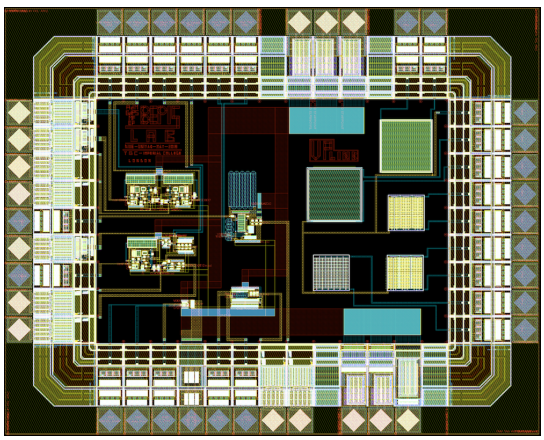


Fig. 6. Complete layout design of the optical biotelemetry system.

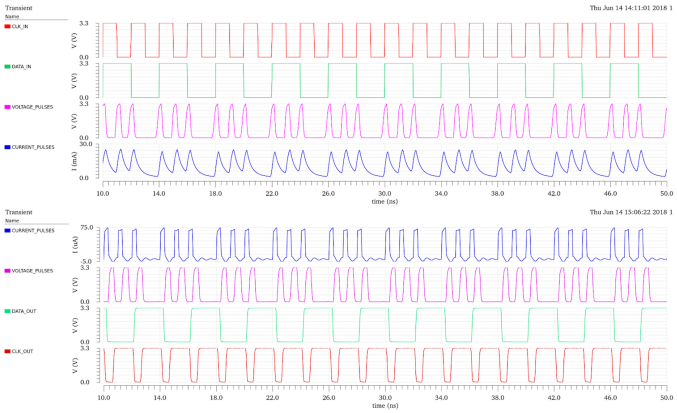


Fig. 7. Post-layout simulation results: key signals within the communication system operating at 500 Mbps and transmitting a repeated $\{0,1\}$ bitstream.

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