Analysis on Circulating Current Frequency of Chain-link Modular Multilevel DC-DC Converters for Low Step-Ratio High-Power MVDC Applications

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***Abstract*—The direct chain-link modular multilevel dc converter has raised great interest recently in medium/high-voltage dc-dc conversion due to the high power device utilization and lower power losses than the front-to-front configurations of modular multilevel converter. This paper introduces a single-phase chain-link modular multilevel buck-boost converter for medium voltage dc applications and presents an analysis methodology on its internal circulating current frequency. Its connection and comparison with the classic dc-ac modular multilevel converter are given first, and its dc and ac components are analyzed in the respective equivalent circuits. Then, the derivation methodology for the proper circulating current frequency with lowest internal reactive power is provided, which could minimize the current stress and decrease the power losses. Also, this method can be directly applied in the derivative topologies and further configurations to satisfy various conversion requirements. The theoretical analysis is verified by a set of full-scaled simulations and further verified against experimental tests on a down-scaled prototype.**

Keywords—modular multilevel converter, dc-dc conversion, multi-terminal networks, MVDC

I. INTRODUCTION

The rapid development of renewable energy in recent year has attracted more and more attention in medium voltage dc (MVDC) networks. The MVDC collection and distribution may reshape the future power system structure, which can accommodate higher penetration of renewable generators and provide greater power capacity than traditional ac networks [1]–[3]. However, MVDC system faces the natural difficulties in dc voltage transformation [4], [5]. One of the serious challenges needed to be addressed soon is the low step-ratio high-power dc-dc conversion, often termed as 'dc transformer', which will play a key role to realize the power flow between two or more MVDC networks with different voltages or different configurations [6]–[8].

The dc-dc conversion in low voltage level (LV) has been extensively investigated for many years [9], [10], but the single switch configuration and high switching frequency make them difficult in the medium voltage (MV) applications. The multi-module concept can be applied to the classic dc-dc converters [11] and develop the applications to MV scope by utilizing input-series-output-parallel (ISOP) or input-parallel-output-series (IPOS) arrangements, but they are more suitable to accomplish the extremely high step-ratio dc-dc conversion, and the isolation between large number of module transformer would be another concern in practical applications. The modular multilevel converter (MMC) technology opens a new road for medium/high-voltage dc-dc conversion, and its front-to-front configuration has been regarded as the most competitive solution to interface two different high voltage dc (HVDC) links due to the good modularity, controllability and flexibility [12]. However, this dc-ac-dc conversion use two MMCs to transfer only one unit power, resulting in higher capital cost and lower power efficiency, which would undermine its advantages in MVDC applications.

Apart from the above-mention well-known converters, some emerging topologies are proposed in last three years through the combination of MMC principles with the classic dc-dc circuits [13]–[15], forming the chain-link dc-dc topology family for medium/high-voltage dc network interconnection. Sub-modules (SMs) in the stack are utilized on both high-voltage side and low-voltage side, leading to a higher power device utilization and less power losses. Also, these arrangement considerably reduce the total number of stacks in the overall conversion system, which could substantially reduce system footprint for highly-compact and low-cost dc-dc conversion. However, the chain-link modular multilevel configurations still need to create a circulating ac current to balance the stack energy although there is no independent ac stage in the conversion flow. This current will cause extra amplitude stresses and power losses for both SM switches and filters [16], [17] in the operation, and it needs a specific analysis and management before these chain-link converters could be applied in the practical dc systems.

To analyse these negative effects in chain-link converters, this paper introduces a single-phase chain-link modular multilevel buck-boost converter and presents an analysis methodology on its circulating current frequency, which provides a possibility to minimize the internal reactive power and circulating current amplitude, facilitating the low step-ratio high-power dc-dc conversion for MVDC network connection.

The connection and comparison between the chain-link dc-dc converter and the classic dc-ac MMC are analysed first, and

the equivalent circuits for dc and ac components are investigated in the respective equivalent circuits. Then, the derivation methodology for the proper circulating current frequency with consideration of SM capacitor voltage ripple is provided in detailed, and it can be also direct applied in the derivative topologies and further configurations to satisfy various conversion specifications. The theoretical analysis is verified against a set of full-scaled simulations and further verified against experimental tests on a down-scaled prototype.

II. Circuit Analysis and Circulating Current Frequency

Fig. 1 shows the single-phase MMC topology with a passive ac load. The black arrow defines the reference of current directions. The blue arrow and red arrow denotes the actual dc and ac current direction respectively. If the converter is properly controlled, the dc current flows through the outer blue loop as the internal common component for top stack and bottom stack currents while the ac current is split to circulate within two small inner red loops as the external differential component for stack currents. Since the stack energy needs to be balanced in the circuit, the net ac energy and dc energy deviation over each ac cycle T ($T = 2\pi/\omega$) should be zero, as shown in (1).

$$\int_0^T v_{stT,B}(t) i_{stT,B}(t) dt = \int_0^T [V_{dc} \mp v_{ac}(t)] \left[I_{dc} \pm \frac{1}{2} i_{ac}(t) \right] dt = 0 \quad (1)$$

$$V_{dc} I_{dc} = \frac{1}{4} V_{ac} I_{ac} \cos\theta = \frac{1}{4} m V_{dc} I_{ac} \cos\theta \quad (2)$$

Thus, the relationship between ac components and dc components is derived in (2). The dc voltage V_{dc} comes from the dc voltage source v_T or v_B while the ac amplitude voltage V_{ac} is dictated by the stack modulation index m ($V_{ac} = mV_{dc}$). The dc current I_{dc} and ac current I_{ac} are dependent on the passive ac load. ω is the angular frequency of the ac voltage and current, and θ is the phase difference between them.

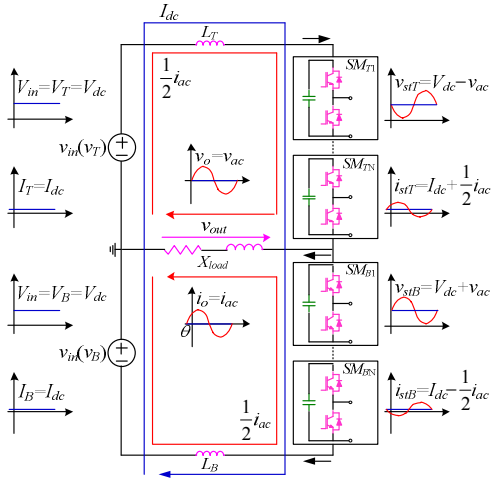

Fig. 1. Current loops in the classic single-phase dc-ac MMC

This classic single-phase MMC achieves dc-ac conversion. If the dc current and ac current exchanged their roles in the conversion, the circuit can be modified to a single-phase chain-link modular multilevel buck-boost converter for dc-dc conversion, as shown in Fig. 2. v_T still serves as the dc source voltage while v_B changes to be the dc load voltage, and R is defined as the voltage step-ratio between them. In this dc-dc circuit, the ac current is running through the outer loop as the internal common component for stack currents while the dc current is split into the two inner loops with different directions as the external differential component for stack currents.

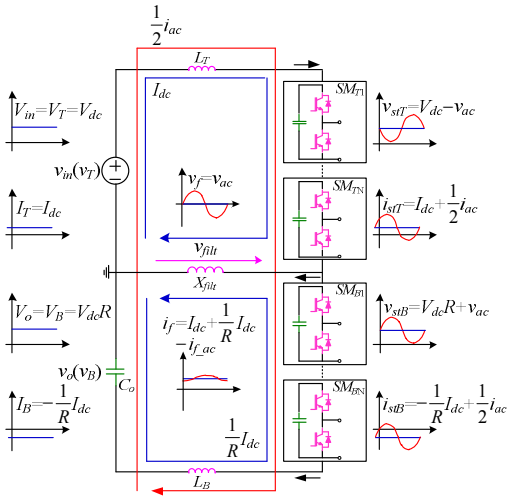

Fig. 2. Current loops in the chain-link buck-boost converter

The energy deviation for both stacks is given in (3) and (4), and their results are still both 0, which means that this arrangement could also keep the stack energy balanced for dc-dc conversion. More importantly, unlike the dc-ac conversion in which the ac component frequency is dependent on the external frequency when it is connected to utility grids, this dc-dc conversion could independently choose the proper internal circulation ac frequency to decrease the circuit current stresses and avoid unnecessary ac power losses.

$$\int_0^T v_{stT}(t) i_{stT}(t) dt = \int_0^T [V_{dc} - v_{ac}(t)][\frac{1}{2} i_{ac}(t) + I_{dc}] dt = 0 \quad (3)$$

$$\int_0^T v_{stB}(t) i_{stB}(t) dt = \int_0^T [V_{dc}R + v_{ac}(t)][\frac{1}{2} i_{ac}(t) - \frac{I_{dc}}{R}] dt = 0 \quad (4)$$

Analysing the dc components of this chain-link dc-dc converter, it can be found that the dc equivalent circuit is based on the classic negative output buck-boost converter, shown in Fig. 3(c). $D_{T,B}$ are defined as stack equivalent duty-cycle, which equals the ratio between stack average voltages and stack peak-to-peak voltage, shown in (5), and the step-ratio of this converter is expressed as (6). By adjusting the dc component value of stack voltage in modulation, the converter is capable of wide-range operation to satisfy various step-ratio requirements.

$$D_{T,B} = \frac{\overline{v_{stT,B\_dc}}}{v_{stT,B\_pp}} = \frac{v_{stT,B\_dc}}{\widehat{v_{stT,B}} - \widehat{v_{stT,B}}} = \frac{V_{T,B}}{2mV_{dc}} \quad (5)$$

$$R = \frac{V_B}{V_T} = \frac{D_T}{D_B} \quad (6)$$

On the other hand, the ac equivalent circuit can be seen as an LC passive network supplied by two controllable ac voltage sources, shown in Fig. 3(b). The value of the ac voltage sources is modulated from the ac components of the sum of SM capacitor voltages.

The stack energy expression with dc and ac components all included is presented in (7) given the assumption that the high frequency ac component value is much smaller than the dc

component.

$$e_{SMT,B}(t) = \frac{C_{SM}}{2N_{T,B}} v_{SMT,B}{}^2(t) = \frac{C_{SM}}{2N_{T,B}} [V_{SMT,B\_dc} + v_{SMT,B\_ac}(t)]^2$$

$$\approx \frac{C_{SM}}{2N_{T,B}} V_{SMT,B\_dc}{}^2 + \frac{C_{SM}}{N_{T,B}} V_{SMT,B\_dc} v_{SMT,B\_ac}(t)$$

$$= E_{SMT,B\_dc} + e_{SMT,B\_ac}(t) \quad (7)$$

where $e_{SMT,B}(t)$ and $v_{SMT,B}(t)$ are the sum of SM capacitor energy and voltage in top or bottom stack, C_{SM} is the SM individual capacitance and $N_{T,B}$ is the number of SMs in the top or bottom stack. The ac component value of the sum of SM capacitor energy, $e_{SMT,B\_ac}(t)$, is dictated by the stack power exchange, and it is expressed as (8).

$$e_{SMT,B\_ac}(t) = \int_0^t v_{stT,B}(t) i_{stT,B}(t) dt \quad (8)$$

Substituting (8) into (7), the ac components of the sum SM capacitor voltage, $v_{SMT\_ac}(t)$ and $v_{SMB\_ac}(t)$ are described in (9) and (10).

$$v_{SMT\_ac}(t) = \frac{N_T}{C_{SM} V_{SMT\_dc}} \int_0^t v_{stT}(t) i_{stT}(t) dt = \frac{N_T V_{dc} I_{dc}}{2\omega C_{SM} V_{SMT\_dc}}$$

$$\left(\frac{4}{m}\tan\theta \sin\omega t + \frac{2m^2-4}{m}\cos\omega t + \sin 2\omega t + \tan\theta \cos 2\omega t\right) \quad (9)$$

$$v_{SMB\_ac}(t) = \frac{N_B}{C_{SM} V_{SMB\_dc}} \int_0^t v_{stB}(t) i_{stB}(t) dt = \frac{N_B V_{dc} I_{dc}}{2\omega C_{SM} V_{SMB\_dc}}$$

$$\left(\frac{4R}{m}\tan\theta \sin\omega t + \frac{2m^2-4R}{mR}\cos\omega t - \sin 2\omega t - \tan\theta \cos 2\omega t\right) \quad (10)$$

Since the dc components of the sum SM capacitor voltage V_{SMT,B_dc} should be able to provide the maximum value of stack voltage for modulation, $m_{iT,B}$ is defined as the internal modulation index to denote the voltage ratio between V_{ac} and V_{SMT,B_dc} ($V_{ac} = m_{iT,B} V_{SMT,B\_dc}$). Thus, the value of the two voltage sources in ac equivalent circuit can be given in (11) and (12), and the ac circulating current in the circuit is derived in (13).

$$v_{sorceT}(t) = \left(\frac{m_{iT}}{m} - m_{iT}\sin\omega t\right) v_{SMT\_ac}(t) \quad (11)$$

$$v_{sorceB}(t) = \left(\frac{m_{iB}}{m} R + m_{iB}\sin\omega t\right) v_{SMB\_ac}(t) \quad (12)$$

$$i_{cir}(t) = \frac{j\omega C_o}{1-\omega^2(L_T+L_B)C_o} [v_{sourceT}(t) + v_{sourceB}(t)] \quad (13)$$

Substituting the results of (11) and (12) into (13), the general expression of this ac current is provided in Appendix and the specific analysis for the most common case of minus/plus symmetrical conversion with full internal modulation ($V_T = V_B, N_{T,B} = N_{arm}, L_{T,B} = L_{arm}, m_{iT,B} = \frac{m}{1+m}$) is shown in (14).

$$i_{cir}(t) = \frac{jC_o N_{arm} I_{dc}}{2C_{SM}(1-2\omega^2 L_{arm} C_o)(1+m)^2} \left[\frac{m^2+8}{m}\tan\theta \sin\omega t\right.$$

$$\left. + \frac{3m^2-8}{m}\cos\omega t + m\cos 3\omega t - m\tan\theta \sin 3\omega t\right] \quad (14)$$

Its fundamental frequency amplitude is expressed in (15), and it also needs to satisfy the power balancing conditions in (3) and (4). Thus, the fundamental frequency of this circulating ac current is derived in (16), which is also the stack modulation frequency for this dc-dc converter.

$$I_{cir} = \frac{N_{arm} I_{dc} C_o}{2C_{SM}(2\omega^2 L_{arm} C_o - 1)(1+m)^2 m} \cdot A \quad (15)$$

$$f_{cir} = \frac{1}{2\pi}\sqrt{\frac{1}{2L_{arm}C_o} + \frac{N_{arm}\cos\theta}{8L_{arm}C_{SM}(1+m)^2}\cdot A} \quad (16)$$

where $A = \sqrt{(\tan^2\theta + 9)m^4 + (16\tan^2\theta - 48)m^2 + 64\tan^2\theta + 64}$.

The minimum value of (16) is achieved in (17) with $\theta = 0$ in the operation given the passive component value and modulation index have been decided in the design process, and the corresponding ac frequency is presented in (18).

$$I_{cir\_min} = \frac{N_{arm} I_{dc} C_o (8-3m^2)}{2C_{SM}(1+m)^2 m(2\omega^2 L_{arm} C_o - 1)} \quad (17)$$

$$f_{ac} = \frac{1}{2\pi}\sqrt{\frac{1}{2L_{arm}C_o} + \frac{N_{arm}(8-3m^2)}{8L_{arm}C_{SM}(1+m)^2}} \quad (18)$$

This circulating ac frequency could avoid reactive ac power in the circuit and the ac current amplitude is also minimized, which increases the overall efficiency and also decrease the current stress for both SM switches and circuit filters.

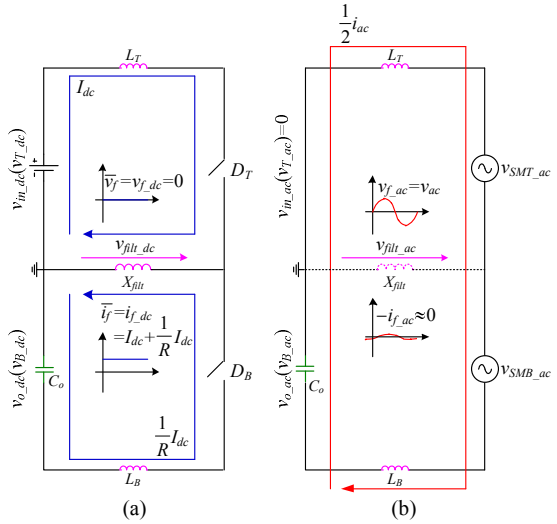

Fig. 3. Equivalent circuit analysis of the chain-link buck-boost converter. (a) DC components. (b) AC components.

III. Further Configurations And Derivative Topologies

The circuit in Fig. 2 is a buck-boost configuration with negative output, which can be used to interconnect monopolar dc system with bipolar dc system, shown in Fig. 4(a). If the dc source in the top changes position with the dc capacitor in the bottom, the converter is modified to a symmetrical arrangement with positive output, presented in Fig. 4(b). It can be applied to connect two monopolar dc systems of different voltages. Although the dc and ac current directions will be in the opposite sense with that in Fig. 2, the operation principle is same and the ac current analysis also follows (17) and (18).

Moreover, the chain-link dc-dc converters in Fig. 4(a) and Fig. 4(b) can be also employed as module circuits for the derivative arrangements and topologies. The series and parallel design could be implemented directly to accomplish the higher power rating and higher voltage rating conversion.

On the one hand, the positive-out configuration or negative-output configuration can be paralleled and developed to the corresponding push full-bridge topologies, shown in Fig. 5(a). Each phase is operated as a single circuit and the switching sequence keeps a half-cycle phase-shift with respect to the

parallel phase, which increases the power rating twice and decreases the voltage ripples on dc-link capacitor at the same time. One the other hand, the positive-out configuration and negative-output configuration can be also connected in series, forming the bipolar topology in Fig. 5(b). The switching sequences for positive leg and negative leg are modulated with half-cycle phase-shift angle. In this manner, the top stack current of the positive leg will approximately equal the bottom stack current of the negative leg, and the currents going through the bottom stack of the positive leg all flows into the top stack of the negative leg. The inner two neighboring stacks can be regarded as a unity, and the grounding at the stack is removed. It develops the voltage rating twice and also accommodates the low step-ratio power connection between two bipolar dc systems.

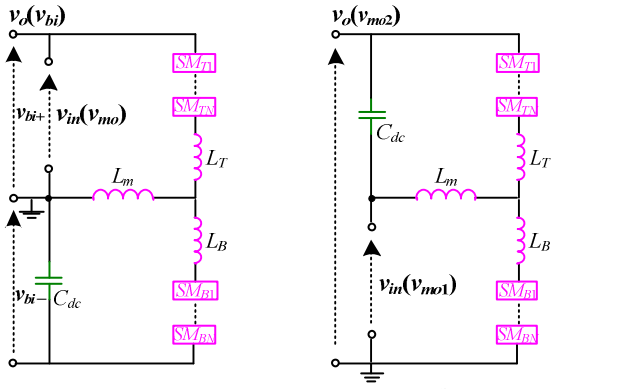

Fig. 4. Different configurations of the chain-link modular multilevel buck-boost converters. (a) Negative-output configuration. (b) Positive-output configuration.

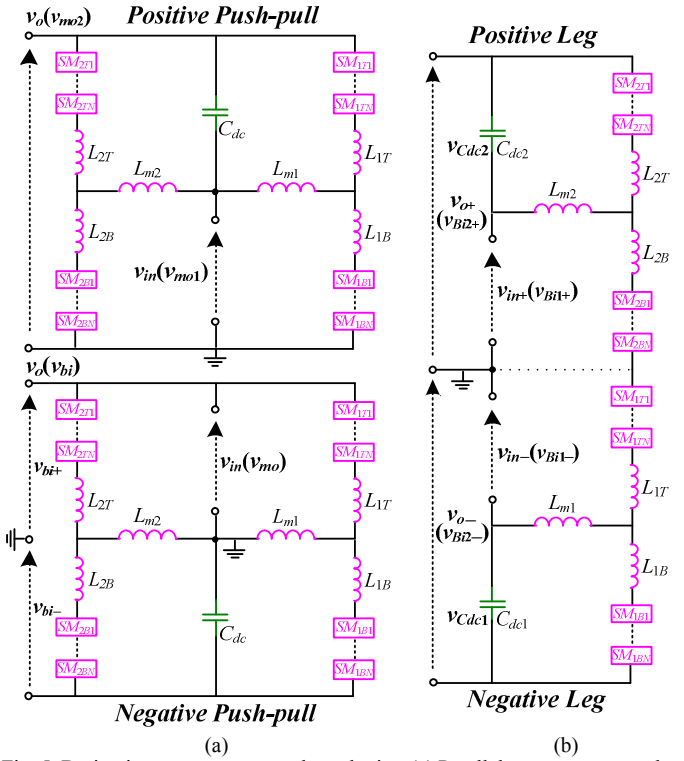

Fig. 5. Derivative arrangements and topologies. (a) Parallel arrangement: push-pull topology. (b) Series arrangement: bipolar topology.

IV. Medium Voltage Application Examples

This section presents a set of full-scaled chain-link dc-dc simulations to verify the theoretical analysis and explore application examples for MVDC network interconnections. The simulation parameters for the negative-output buck-boost configuration are provided in Table I (with respect to the terminology in Fig. 4(a)). The SM capacitances and arm inductance are set with 10% variations to simulate the tolerances in practical conversion.

TABLE I. Simulation Parameters in the Full-Scale Application Examples

Parameter	Description	Value
P	*Power Rating*	3 MW
$v_{in}(v_{mo})$	*Input Positive-pole Voltage*	11 kV
v_{bi-}	*Negative-pole Voltage*	4 kV–11 kV
R	*Step-ratio* (v_{Bi-}/v_{in})	0.33:1–1:1
$v_o(v_{bi})$	*Output Bipolar Voltage*	15 kV–22 kV (±11 kV)
C_{dc}	*DC capacitance*	300 μF
L_m	*Filter Inductance*	20 mH
L_{arm}	*Arm Inductance*	150 μH with ±10% variation
N_{arm}	*SM Number per Stack*	9
C_{SM}	*SM Capacitance*	1.0 mF with ±10% variation
S	*SM Power Switches*	ABB 5SNA1500E330305
δ_{SM}	*SM Capacitor Voltage Range*	5%

The minus/plus symmetrical conversion ($R = 1$) is discussed first, and the modulation index is chosen at 0.8 in this study ($m = 0.8$). The dc equivalent duty-cycle of the top stack and bottom stack is set at an equal value ($D_T = D_B = 0.625$) for this symmetrical conversion, and the ac modulation frequency is designed at 800 Hz to minimize the internal reactive power and circulating current amplitude according to the analysis in (18). The stack voltages in Fig. 6(a) show that the ac components of the top stack voltage v_{stT} and bottom stack voltagev_{stB} are phase-shifted with 180° but the dc components are the same, and the stack currents in Fig 6(b) illustrate that the ac components of the two stack currents i_{stT} and i_{stB} keep the same value but their dc components are opposite. It can be seen that the phase difference between voltage and current for both stacks is almost either 0° or 180°, so there is nearly no reactive power in the ac energy loop, which means the ac components have been fully utilized for stack energy balancing. Furthermore, the amplitude of the circulating ac current is about 680 A, which reaches good agreement with the result of (17) and demonstrates that i_{stT} and i_{stB} have both achieved the minimum value in this simulation case. In the meantime, the SM voltages in top stack and bottom stack are both well controlled. The maximum voltage deviation is limited within 5% of the nominal value of 2.2 kV, shown in Fig. 6(c) and Fig. 6(d), and the sum of the dc components of SM capacitor voltages in each stack also matches the maximum stack voltage value.

Then, the asymmetrical voltage conversion ($R = 0.67$) is shown in Fig. 7 to demonstrate the validity of this ac frequency analysis in more general application cases. The ratio of the dc equivalent duty-cycle between bottom stack and top stack is set as 0.67:1 ($D_B/D_T = 0.67$), and the modulation index is accordingly adjusted to 0.54 to accommodate the negative-pole voltage in this case. It is worth noting that the power conversion is reduced to 1.33 MW, and the ac frequency is operated at 925

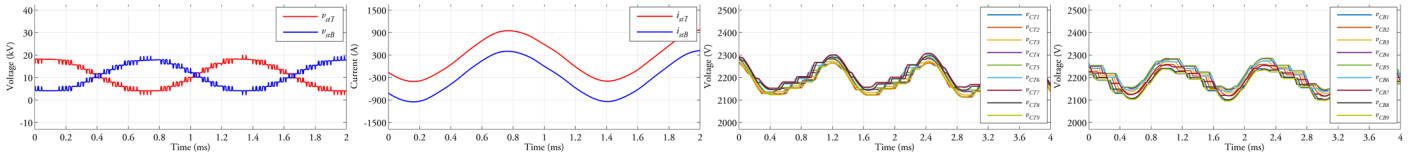

Fig. 6. Simulation results for the symmetrical conversion in negative-output buck-boost configuration. (a) Stack voltages (v_{stT}, v_{stB}). (b) Stack currents (i_{stT}, i_{stB}). (c) SM voltages in top stack ($v_{CTk}, k = 1 \dots 9$). (c) SM voltages in bottom stack ($v_{CBk}, k = 1 \dots 9$).

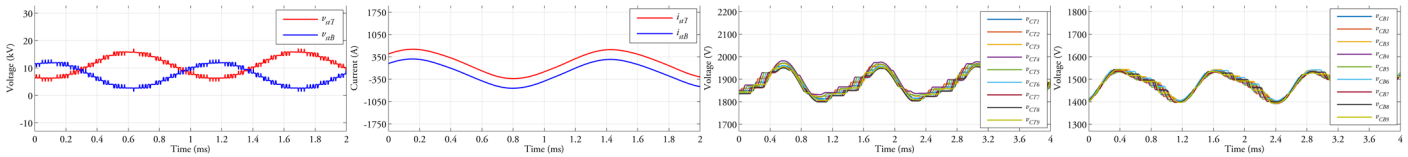

Fig. 7. Simulation results for the asymmetrical conversion in negative-output buck-boost configuration. (a) Stack voltages (v_{stT}, v_{stB}). (b) Stack currents (i_{stT}, i_{stB}). (c) SM voltages in top stack ($v_{CTk}, k = 1 \dots 9$). (c) SM voltages in bottom stack ($v_{CBk}, k = 1 \dots 9$).

Hz following the equation in Appendix (B–2) for general step-ratio case analysis. From Fig. 7(a) and Fig. 7(b), the ac component amplitude of both voltages and currents are equal for the two stacks, but their dc components are different due to this asymmetrical conversion. The value of dc and ac components correlates the theoretical analysis in Section II, and there is also no ac reactive power in the energy loop. The circulating current achieves the minimum value of 450 A, which further validates the effectiveness of (B–1). Also, the SM voltages in Fig. 7(c) and Fig. 7(d) show that the voltage balancing is still effective. The SM voltages in the top stack are balanced around 1.9 kV, and the SM voltages in the bottom stack are balanced around 1.5 kV. The sum of their dc components equals the maximum value of the corresponding stack voltage.

V. Experimental Results Assessment

To further verify the theoretical analysis and simulation results, a down-scaled prototype of the chain-link negative-output buck-boost converter was designed and built, and the relevant parameters are listed in the Table II.

TABLE II. Experimental Parameters in the Down-Scaled Prototype

Parameter	Description	Value
P	*Power Rating*	1.2 kW
$v_{in}(v_T)$	*Input Positive-pole Voltage*	150 V
v_{bi-}	*Negative-pole Voltage*	50 V–150 V
R	*Step-ratio* (v_{Bi-}/v_{in})	0.33:1–1:1
$v_o(v_{bi})$	*Output Bipolar Voltage*	200 V–300 V (±150 V)
C_{dc}	*DC Capacitance*	300 μF
L_m	*Filter Inductance*	5 mH
L_{arm}	*Arm Inductance*	150 μH
N_{arm}	*SM Number per Stack*	9
C_{SM}	*SM Capacitance*	1.0 mF

The key capacitance and inductance in the prototype choose the same value as those in simulation analysis, so the internal ac frequency is also operated at 800 Hz for the minus/plus symmetrical conversion. The stack voltages and currents are presented in Fig. 8. It should be noted that the current distortion is caused by low-voltage operation of SM IGBTs in the lab, which can be easily solved in high voltage rating practical operation. It can been seen that the ac component of top stack voltage has a phased-shift value of 180° with respect to that of bottom stack voltage while the dc components also have the same value. In the meantime, the ac currents are equal for the two stacks, but the dc currents are in the opposite direction as expected. The phase-shift between stack voltage and current is nearly is 0° or 180°, so the reactive power is very small. Moreover, the dc and ac component value of the stack voltage and current follow the theoretical analysis in Section II, and the ac current amplitude is about 20 A, which is well-matched with the results of (17) and means that the stack currents also achieved the minimum value in this experiment. Further, the top stack and bottom stack SM capacitor voltages are all well balanced in this case, shown in Fig. 9. The maximum and minimum SM capacitor voltage are both controlled within 5% of the nominal voltage of 30 V, and the sum of the SM voltage capacitor voltages in each stack also equals the maximum value of the stack voltage. These results further validate the theoretical derivation in Fig. 2 and simulation assessment in Fig. 6 for the symmetrical interconnection between a monopolar dc system and the matching bipolar dc system.

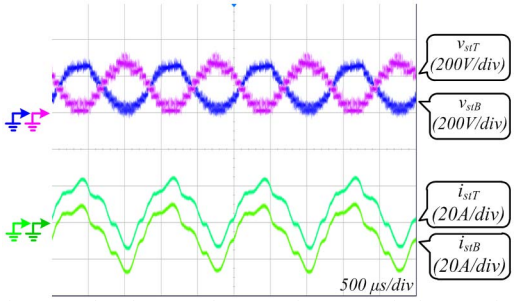

Fig. 8. Stack voltages and currents in symmetrical conversion

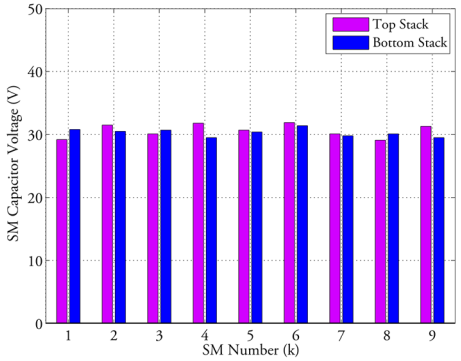

Fig. 9. SM voltages in symmetrical conversion case

Then, a variable step-ratio test is given in Fig. 10 and Fig. 11 to illustrate the capability of asymmetrical conversion ($R = 0.67$) and the controllability of the output voltage $v_o(v_{bi})$. The input positive-pole voltage keeps constant at 150 V, and the reference value for the output voltage is set at 250 V first and changed to 300 V at the midpoint of the time period. The result shows that the output voltage follows the regulation command accurately both before and after the change of the reference value, and the stack currents also respond quickly to match the load power. The converter is operated well in both asymmetrical case and symmetrical case, and the SM capacitor voltages results in asymmetrical period is presented in Fig. 11. Compared with the results in Fig. 9, the SM voltages in top stack are decreased to around 25.5 V because the modulating index is adjusted for the negative-pole voltage. The SM voltages in bottom stack are balanced around 20 V, and the sum of them also matches the maximum value of the bottom stack voltage. These results demonstrate the controllability and adjustability of the output voltage in this down-scaled prototype.

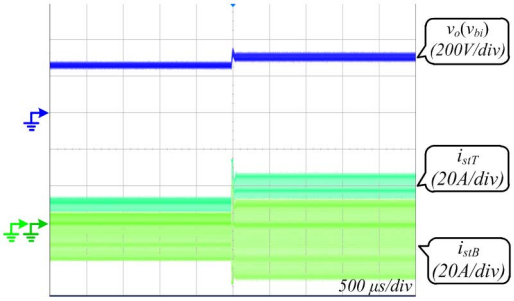

Fig. 10. Variable step-ratio test

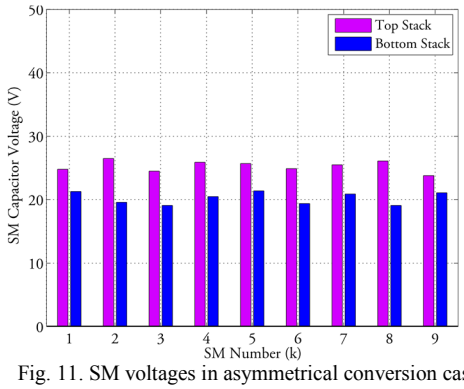

Fig. 11. SM voltages in asymmetrical conversion case.

VI. Conclusion

A direct chain-link modular multilevel buck-boost converter was introduced for MVDC network interconnection and an analysis methodology on its internal ac frequency was provided to avoid the reactive power in the circuit and minimize the circulating current amplitude.

The connection and comparison between the chain-link dc-dc converter and the classic dc-ac MMC are presented first, and the dc and ac components are analyzed in the respective equivalent circuit. Then, the derivation process for the proper circulating frequency is given in detail, which provide the possibility to minimize the reactive power losses and current amplitude stresses in this single stage dc-dc conversion. Also, this method can be further applied in the derivative topologies for different conversion requirements. The theoretical analysis is verified against a set of full-scaled simulations and further verified against experimental tests on a down-scaled prototype. The simulation and experimental results are well-matched with the mathematical analysis, and they demonstrate the validity of this analysis method.

References

[1] A. Alfares, E. Afshari, M. Amirabadi and B. Lehman, "A modular SCR-based DC-DC converter for medium-voltage direct-current (MVDC) grid applications," *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, 2017, pp. 5170-5177.

[2] B. Zhao, Q. Song, J. Li, Q. Sun and W. Liu, "Full-Process Operation, Control, and Experiments of Modular High-Frequency-Link DC Transformer Based on Dual Active Bridge for Flexible MVDC Distribution: A Practical Tutorial," in *IEEE Trans. on Power Electronics*, vol. 32, no. 9, pp. 6751-6766, Sept. 2017.

[3] D. Jovcic and L. Zhang, "LCL DC/DC Converter for DC Grids," *IEEE Trans. on Power Del.*, vol. 28, no. 4, pp. 2071-2079, Oct. 2013.

[4] C. D. Barker, C. C. Davidosn, D. R. Trainer, and R. S. Whitehouse "Requirements of DC–DC converters to facilitate large DC grids," Cigre, *SC B4 HVDC and Power Electronics*, 2012.

[5] X. Xiang, X. Zhang, G. P. Chaffey and T. C. Green, "An Isolated Resonant Mode Modular Converter With Flexible Modulation and Variety of Configurations for MVDC Application," in *IEEE Trans on Power Del.*, vol. 33, no. 1, pp. 508-519, Feb. 2018.

[6] I. A. Gowaid, G. P. Adam, S. Ahmed, D. Holliday and B. W. Williams, "Analysis and Design of a Modular Multilevel Converter With Trapezoidal Modulation for Medium and High Voltage DC-DC Transformers," in *IEEE Trans. on Power Electron.*, vol. 30, no. 10, pp. 5439-5457, Oct. 2015.

[7] G. J. Kish, "On the Emerging Class of Non-Isolated Modular Multilevel DC-DC Converters for DC and Hybrid AC-DC Systems," in *IEEE Transactions on Smart Grid*, vol. PP, no. 99, pp. 1-1.

[8] X. Xiang, X. Zhang, T. Luth, M. M. C. Merlin and T. Green, "A Compact Modular Multilevel DC-DC Converter for High Step-ratio MV and HV Use," in *IEEE Trans on Ind. Electron.*, vol. 65, no. 9, pp. 7060-7071, Sept. 2018.

[9] W. Li and X. He, "Review of Non-isolated High-Step-Up DC/DC Converters in Photovoltaic Grid-Connected Applications," *IEEE Trans. on Ind. Electron.*, vol. 58, no. 4, pp. 1239-1250, April 2011.

[10] K. Sano and H. Fujita, "Improving dynamic performance and efficiency of a resonant switched-capacitor converter based on phase-shift control," *2009 IEEE Energy Conversion Congress and Exposition (ECCE)*, San Jose, CA, 2009, pp. 3509-3515.

[11] B. Zhao, Q Song, W. Liu and Y. Sun, "Overview of Dual-active-bridge Isolated Bidirectional DC-DC Converter for High-frequency-link Power-Conversion system," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4091– 4106, Aug. 2014.

[12] S. Debnath, J. Qin, B, Bahrani, M. Saeedifard and P. Barbosa, "Operation, Control, and Applications of the Modular Multilevel Converter: A Review," *IEEE Trans. Power Electron*, vol. 30, no. 1, pp. 37-53, Jan. 2015.

[13] A. Schön and M. M. Bakran, "A new HVDC-DC converter with inherent fault clearing capability," *2013 15th European Conference on Power Electronics and Applications (EPE)*, Lille, 2013, pp. 1-10.

[14] G. J. Kish, M. Ranjram, and P. W. Lehn, "A modular multilevel dc/dc converter with fault blocking capability for HVDC interconnects," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 148–162, Jan. 2015.

[15] S. H. Kung; G. J. Kish, "A Modular Multilevel HVDC Buck-Boost Converter Derived from its Switched-Mode Counterpart," in *IEEE Trans on Power Del.*, vol.PP, no.99, pp.1-1

[16] S. Du, B. Wu, K. Tian, D. Xu, and N. R. Zargari, "A novel medium-voltage modular multilevel dc-dc converter," *IEEE Trans. on Ind. Electronics*, vol. 63, no. 12, pp. 7939–7949, Dec 2016.

[17] G. P. Adam, I. A. Gowaid, S. J. Finney, D. Holliday and B. W. Williams, "Review of DC–DC Converters for Multi-terminal HVDC Transmission Networks," *IET Power Electron.,* vol. 9, no. 2, 2016.

APPENDIX

A. General Current Analysis for Buck-boost Configuration

Substituting the results of (11) and (12) into (13), the general expression of the internal ac current is expressed in (A–1),

$$i_{cir}(t)=\frac{jC_oN_TI_{dc}\delta_T^2}{2C_{SM}[1-\omega^2(L_T+L_B)C_o](1+m)^2}[\frac{m^2+8}{2m}\tan\theta\sin\omega t+\frac{3m^2-8}{2m}\cos\omega t+(3-m^2)\sin 2\omega t+3\tan\theta\cos 2\omega t$$
$$-\frac{m}{2}\tan\theta\sin 3\omega t+\frac{m}{2}\cos 3\omega t-2\tan\theta]+\frac{jC_oN_BI_{dc}\delta_B^2}{2C_{SM}[1-\omega^2(L_T+L_B)C_o](R+m)^2}[\frac{m^2+8R^2}{2m}\tan\theta\sin\omega t+\frac{3m^2-8R}{2m}\cos\omega t$$
$$+\frac{m^2-2R-R^2}{R}\sin 2\omega t-3R\tan\theta\cos 2\omega t-\frac{m}{2}\tan\theta\sin 3\omega t+\frac{m}{2}\cos 3\omega t+2R\tan\theta] \quad (A-1)$$

where $\delta_{T,B}$ is the redundancy ratio for the dc components of stack voltage ($m_{iT}=\frac{m\delta_T}{1+m}, m_{iB}=\frac{m\delta_B}{R+m}m\delta_B, \delta_{T,B}\le 1$).

B. Asymmetrical voltage conversion for Buck-boost Configuration

The minimum current amplitude of the fundamental frequency component in the asymmetrical conversion ($V_B=V_TR, N_{T,B}=N_{arm}, L_{T,B}=L_{arm}, m_T=\frac{m}{1+m}, m_B=\frac{m}{R+m}, \delta_{T,B}=1$) is given in (B–1), and the corresponding ac frequency is provided in (B–2).

$$I_{cir\_min}=\frac{N_{arm}I_{dc}C_o[(8-3m^2)(R+m)^2+(8R-3m^2)(1+m)^2]}{4C_{SM}(R+m)^2(1+m)^2m(2\omega^2L_{arm}C_o-1)} \quad (B-1)$$

$$f_{ac}=\frac{1}{2\pi}\sqrt{\frac{1}{2L_{arm}C_o}+\frac{N_{arm}[(8-3m^2)(R+m)^2+(8R-3m^2)(1+m)^2]}{16L_{arm}C_{SM}(R+m)^2(1+m)^2}} \quad (B-2)$$