Buck-Boost Single-Inductor Multiple-Output (SIMO) High-Frequency Inverters for Medium-Power Wireless Power Transfer

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***Abstract*—In this paper, a non-isolated buck-boost single-inductor multiple-output (SIMO) DC-AC inverter for driving multiple independent high-frequency AC outputs of medium power, is proposed. Compared with traditional bridge-type inverters, the proposed buck-boost SIMO inverter achieves (i) a smaller component count, (ii) fully independent power control of its outputs, (iii) better scalability in increasing the number of AC output channels, and (iv) higher power efficiency. Operating in pseudo-continuous conduction mode (PCCM), the rated power of each output channel of this inverter can be high while attaining zero cross-regulation. The scalability factor of the proposed inverter is formally investigated and the theoretical maximum number of AC outputs is analytically derived. The targeted application of this SIMO-based inverter is for driving multiple transmitter coils to realize versatile multi-device medium-power wireless power transfer. A hardware prototype of a single-inductor three-output (SITO) buck-boost inverter delivering a medium power of 8.4 W per output channel has been constructed. It is experimentally verified that precise and independent current regulation of individual transmitter coil is achievable with the proposed inverter.**

***Index Terms*—Single-inductor multiple-output (SIMO), Buck-boost, DC–AC power conversion, high-frequency inverter, Pseudo-Continuous Conduction Mode (PCCM), Discontinuous Conduction Mode (DCM), Continuous Conduction Mode (CCM), Cross-regulation.**

I. INTRODUCTION

Wireless power transfer (WPT) is undoubtedly one of the most rapidly emerging technologies, which has gained tremendous interests from academia and industry in recent years. It enables wireless power delivery to a myriad of consumer electronic devices such as mobile phones, tablets, laptops, wearable sensors, and even biomedical implants.

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Conventionally, a simple two-coil approach is used to realize WPT which consists of a pair of transmitter coil and receiver coil. However, a major limitation of such a two-coil system is that only one single device can be charged at any point in time. It also suffers from unpredictable inductive link performance since the power transfer efficiency is highly dependent on the actual coil alignment and the operating distance between the transmitter and receiver coil [1]–[4]. In addition, a conventional two-coil WPT system provides a very limited set of design parameters (e.g. Q-factors and coupling k) for tuning the currents in the magnetic coils, which need to be optimized in order to attain sufficient power transfer efficiency (typically ≤ 40 %). Recently, a multi-coil approach has become increasingly popular for a broader range of WPT applications such as the concurrent charging of multiple devices. In this approach, the transmitter contains multiple coils which are often arranged as a coil array. Fig. 1 shows the PCB view of a real four-coil wireless power transmitter which is in full compliance with the Qi standard [5], [6].

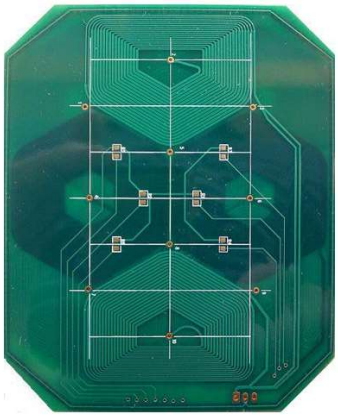
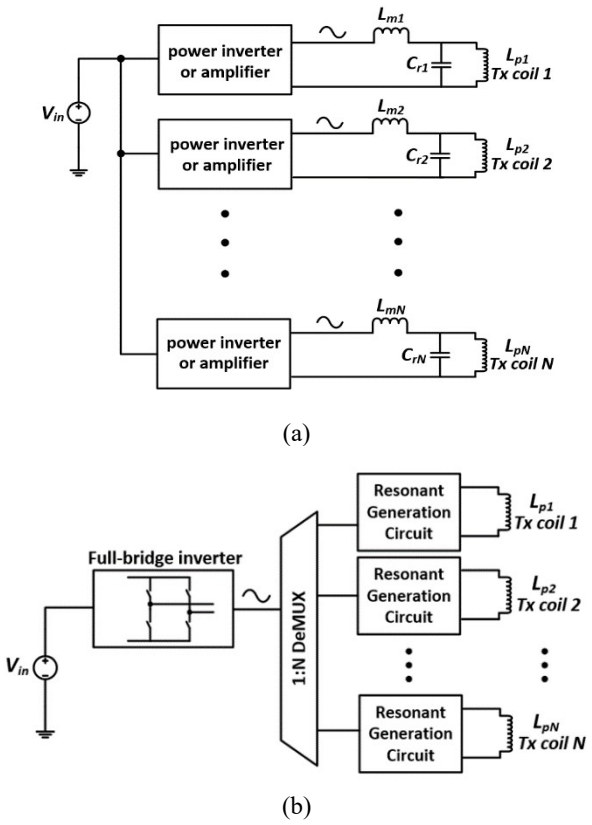


Fig. 1. A PCB view of a Qi-compliant four-coil wireless power transmitter (courtesy of Convenient Power Limited).

A key advantage of using multiple coils is that it increases the likelihood that one of the transmitter coils on the wireless charger aligns properly with the receiving coil on the end device. It significantly improves the freedom of positioning of the end device without sacrificing power transfer efficiency. More importantly, simultaneous charging of multiple electronic devices is made possible with such a multi-coil charging system. It allows scalability and flexibility of the wireless charger which caters for charging multiple devices rated at different power levels and charging speed. Nonetheless, a major challenge of using multiple transmitter coils in a multi-coil WPT system is

that it substantially increases the design complexity and build-of-material (BOM) cost of the wireless power transmitter.

A simple approach of implementing a multi-coil wireless transmitter is to use multiple independent power inverters or amplifiers, one for each transmitter coil [7]–[11]. Fig. 2(a) shows the system architecture of this conventional multiple-inverter topology.



(a)

(b)

Fig. 2. System architecture of (a) the conventional multiple-inverter topology and (b) the conventional three-stage power conversion topology for a multi-coil wireless transmitter.

The power stage of each transmitter is made up of a single-phase power inverter and its corresponding LCL resonant network. Each inverter is powered from a single DC voltage supply and the energy is delivered to the receiver coil by means of an electromagnetic field, which is generated by LCL resonant tank comprising the matching inductor (L_m), the resonant capacitor (C_r), and the primary transmitter coil (L_p). In practice, the power inverter can be implemented in several ways. For example, a highly-efficient switched-mode class-E power amplifier is used to drive each transmit coil [7], [8] due to its simplicity and higher output power at the same supply voltage, as compared with the classical bridge-type class-D amplifier [9]. In [10], the power inverter is actually implemented as a high-speed low-power amplifier because of its flexibility to change the amplitudes and phases of the voltages being applied to the transmit coils. On the other hand, it has also been realized as a traditional full-bridge (or half-bridge) inverter for energizing each transmit coil [11]. Regardless of the actual implementation, a major issue with this multi-inverter topology is that the number of power inverter increases linearly with the number of transmitter coils. This is very inefficient and costly as it forbids any sharing of components among the inverters. On the other hand, a three-stage power conversion architecture for driving multiple coils has been reported [11]–[15], as shown in Fig. 2(b). The first stage is characterized by a single full-bridge inverter which performs DC-AC conversion. The second stage consists of a 1-by-N power de-multiplexer which selects one of the LC resonant circuits to be connected to the preceding inverter while the third stage is represented by a parallel combination of resonant circuits and the corresponding transmitter coils. Even though only one full-bridge inverter is used in this configuration, the implementation of the power de-multiplexer is more complicated since it requires many discrete relays such as solid-state relays or FET switches. With a growing number of transmitter coils, a greater number of active devices is therefore required which inevitably leads to a larger form factor, increased power loss, and higher costs. In addition, this topology requires two different sets of controllers, i.e., one for full-bridge inverter and another for the power de-multiplexer. A larger number of coils will significantly complicate the controller design. In view of this, a low-power multi-channel wireless transmitter based on a single-inductor three-output (SITO) boost-type inverter has recently been reported [17]. This topology enables a single-stage power conversion from a single DC power supply into multiple AC outputs by employing only one main inductor in the power stage, as illustrated in Fig. 3.

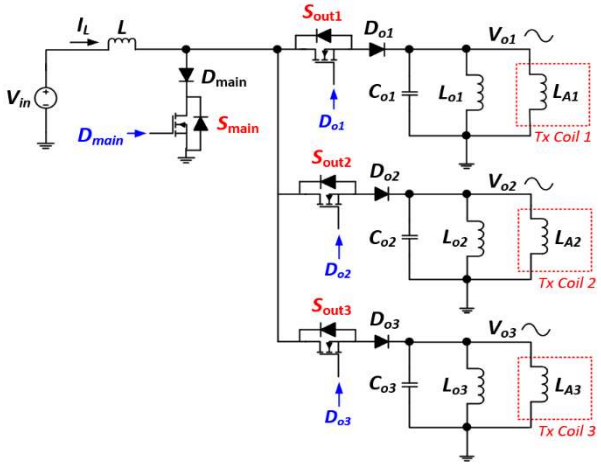


Fig. 3. Circuit topology of the previously-reported boost-only single-inductor three-output (SITO) inverter [14].

Compared with the existing inverter topologies [7]–[16], [18]–[24], this SITO-based inverter topology requires a smaller number of power switches, gate drivers, and other passive components. In addition, only a single controller is needed to simultaneously regulate all the AC outputs. Despite its advantages, this topology suffers two major drawbacks: (i) the maximum output power is only 2 W per channel which is insufficient to cope with the increasing power demands for future wireless charging pads and/or charging base stations, and (ii) the RMS value of the sinusoidal output voltage must always be higher than the DC value of the input voltage which

unnecessarily restricts the types of load devices.

Hence, in this paper, a buck-boost Single-Inductor Multiple-Output (SIMO)-based inverter topology is proposed which enables a DC-AC power conversion from a DC power source (e.g. 12 V lithium-ion battery) into multiple independently-controlled sinusoidal AC voltages with a wide load range. It is capable of delivering medium power levels with improved efficiency. Basically, the proposed SIMO inverter combines the function of an inverting buck-boost DC-DC SIMO topology and that of a parallel network of LC resonant tanks (which forms the DC-AC stage) into a single stage. It should be noted that the output voltage is negative with respect to ground since the inverting buck-boost topology is chosen for the power stage. Yet, the polarity of the output voltage is insignificant in this case since the outputs of the proposed inverter are sinusoidal in nature. The only subtle difference is that there is a 180° phase shift in the sinusoidal output voltage by reversing the output polarity. In principle, the functionality of the SIMO inverter remains unaffected regardless of whether an inverting buck-boost or a non-inverting buck-boost topology is chosen for the power stage. But, the inverting buck-boost topology is actually more preferable than the non-inverting buck-boost topology because the former requires fewer number of power switches and diodes, which implies a smaller component count, lower BOM cost, ease of implementation, simplified control scheme, and higher power efficiency. By connecting a pair of free-wheeling switches across the main inductor, the inductor current could stay above zero which allows the SIMO inverter to operate in Pseudo-Continuous Conduction Mode (PCCM) [25]–[27]. As a result, the output power can be further increased while still achieving minimal cross-interference among the individual output channels. This paper is organized as follows. Section II presents the circuit topology of the proposed buck-boost SIMO inverter and its operating principle is discussed in Section III. Section IV provides a theoretical analysis of the SITO inverter. Section V presents the simulated results and the experimental results are included in Section VI. Finally, Section VII concludes our research efforts.

II. CIRCUIT TOPOLOGY OF THE SINGLE-STAGE BUCK-BOOST INVERTER

This section presents the circuit topology of the proposed buck-boost SIMO inverter. Fig. 4 provides a graphical illustration of the derivation of this topology. Fundamentally, the proposed topology is created through proper integration of an inverting buck-boost DC-DC converter [see Fig. 4(a)] and a parallel network of LC resonant tanks [see Fig. 4(b)]. Specifically, the ideal current source for driving the parallel resonant tanks can be replaced by the main inductor L in the buck-boost converter since the latter acts as a current source which delivers the storage energy to each of the AC outputs sequentially. Since an inverting buck-boost topology is used, the current in the resonant tanks actually flows from ground to the output node via the resonant tank. The buck-boost DC-AC SIMO inverter with a total number of N sinusoidal AC outputs can therefore be obtained [see Fig. 4(c)]. Only one single inductor L is required in the power stage to drive any number of the AC outputs. Indeed, the buck-boost converter and the resonant tanks can be combined naturally and easily to form a single stage as the two circuits share a common ground.

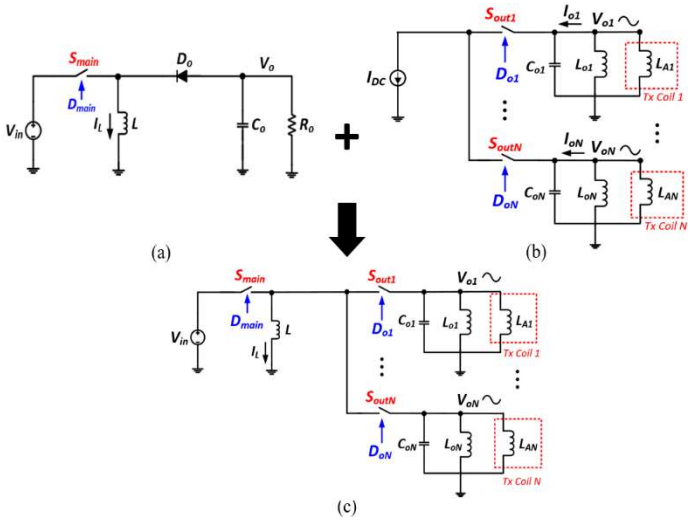


Fig. 4. Derivation of a single-stage buck-boost DC-AC SIMO inverter. (a) An inverting buck-boost DC-DC converter. (b) A current source driving a parallel network of LC resonant tanks. (c) A single-stage buck-boost DC-AC SIMO inverter.

Without loss of generality, the circuit topology of a single-stage buck-boost single-inductor three-output (SITO) inverter with the inductor peak-current and valley-current control is shown in Fig. 5.

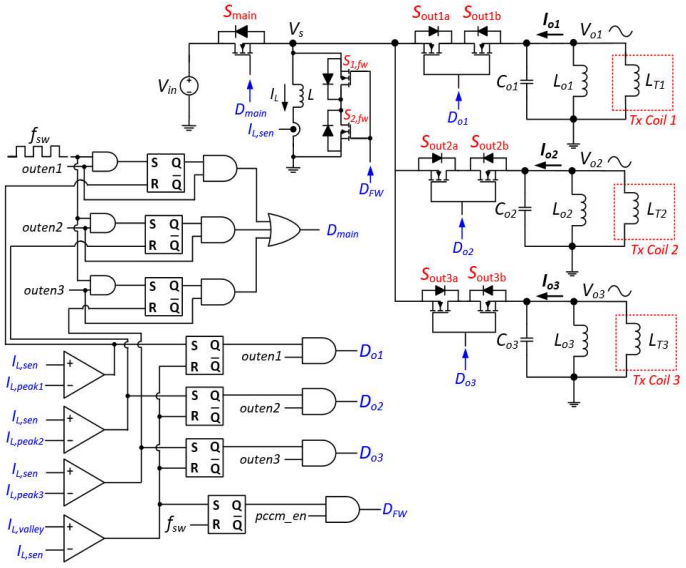


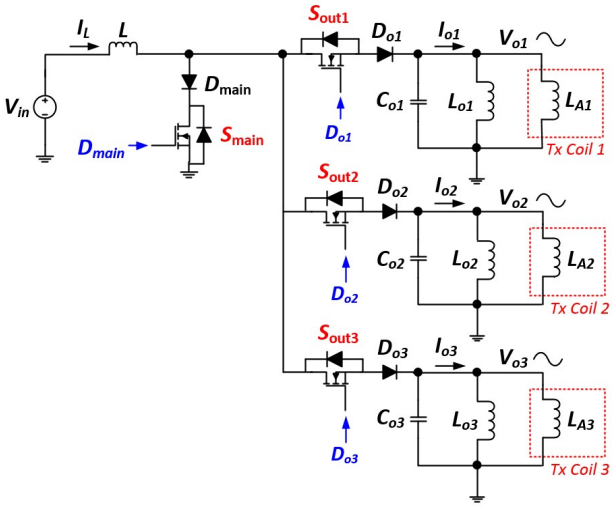
Fig. 5. Circuit diagram of the proposed single-stage buck-boost single-inductor three-output (SITO) inverter.

The proposed SITO inverter transforms a single DC input voltage V_{in} into three independent AC output voltages, namely V_{o1}, V_{o2} and V_{o3}, and their RMS values can be configured to be either above or below V_{in} by adjusting the on-time duty ratio of the main switch (S_{main}). This inverter requires a total of nine power switches, i.e., one main switch (S_{main}), three pairs of output switches [(S_{out1a}, S_{out1b}), (S_{out2a}, S_{out2b}), (S_{out3a}, S_{out3b})], and

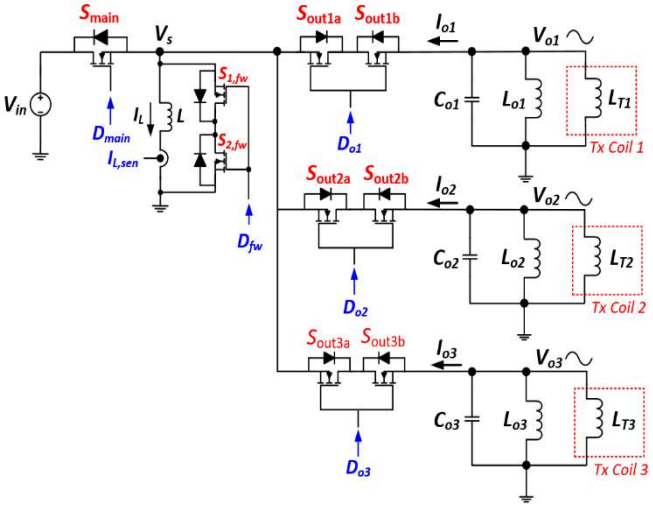
a pair of free-wheeling switches across the main inductor L ($S_{1,fw}$, $S_{2,fw}$). The output currents flowing across S_{out1}, S_{out2}, S_{out3} are designated as I_{o1}, I_{o2}, and I_{o3}, respectively. The current flowing through the main inductor is represented by I_L. Each of the three output branches consists of a parallel LC resonant tank (L_{oi}, C_{oi}), which forms an integral part of the power stage, and an inductive load (L_{Ti}) for modeling the wireless transmission coil, where i is the output index.

By enabling the two free-wheeling switches ($S_{1,fw}$, $S_{2,fw}$) properly, the proposed SITO inverter can operate in PCCM [25]–[27] with a free-wheeling period during which the inductor current stays above zero. This SITO inverter in PCCM is capable of delivering larger load currents than that in DCM while still achieving zero cross-regulation. It is worth noting that the two back-to-back free-wheeling switches are needed in order to prevent a direct short between the switching node V_s and ground via the body diode of the free-wheeling switch. Imagine there is only one free-wheeling switch across the main inductor L (i.e., the top free-wheeling switch $S_{1,fw}$ is removed and only the bottom free-wheeling switch $S_{2,fw}$ stays connected across L). When S_{out1} is turned ON and the sinusoidal output voltage V_{o1} attains a negative value in the second subinterval of PCCM (or DCM), V_s will also become negative which causes an unwanted reverse current from ground to V_s via the body diode of $S_{2,fw}$ (even though this switch is turned OFF). Obviously, this is not the intended circuit behavior. Consequently, two back-to-back free-wheeling MOSFETs with their body diodes pointing at each other are essential for the proposed SITO inverter.

For comparison purpose, Fig. 6 shows the power stage topology of the previously-reported boost-only SITO inverter in DCM [17] versus that of the proposed buck-boost SITO inverter in PCCM.



(a)



(b)

Fig. 6. Comparison of (a) power stage topology of the previously-reported boost-only SITO inverter in DCM versus (b) that of the proposed buck-boost SITO inverter in PCCM.

In the boost-only SITO inverter [17] from Fig. 6(a), a main diode D_{main} is used to block an unwanted opposite current flow from ground to the negative output via the body diode of S_{main} in the second subinterval of PCCM (or DCM). However, D_{main} is no longer required in the proposed SITO inverter, as shown in Fig. 6(b), because an *inverting* buck-boost topology is employed in the power stage. During the second sub-interval when the output switch is turned ON, the sinusoidal output voltage (and also the voltage at the switching node V_s) has a negative value with respect to ground which is also less than the input voltage V_{in}. In the absence of an undesirable current flow from V_s to V_{in} via the body diode of S_{main}, there is no need to connect D_{main} in series with S_{main} in the proposed inverter. In addition, Fig. 6(b) shows that in each of the three output branches, two back-to-back MOSFETs (e.g. S_{out1a}, S_{out1b}) with their body diodes pointing toward each other are used in order to prevent an unwanted current flow from V_{in} to the output node during the first subinterval. Suppose S_{out1b} is removed and only S_{out1a} remains connected in the first output branch. When S_{main} is switched ON in the first subinterval and the instantaneous value of V_{o1} becomes lower than V_{in}, an undesirable current will flow from V_{in} to V_{o1} via the body diode of S_{out1a} (even when S_{out1a} is OFF). Two back-to-back output MOSFETs are therefore required at each output branch. Since the proposed inverter does *not* require any blocking diodes, it incurs no diode conduction losses which help improve the overall power efficiency. In general, for a total of N outputs, the power stage of the proposed buck-boost SIMO inverter requires a total of $(2N + 3)$ power switches in PCCM or $(2N + 1)$ power switches in DCM. On the other hand, the current-sensing circuit for the inductor current in the proposed inverter is much simplified because the main inductor L is referenced to ground, as depicted in Fig. 6(b). Hence, no differential op amp is needed for sensing the inductor current. The current sensor can simply be implemented by using a small current-sensing resistor between L and ground. The voltage across this resistor can then be used as a feedback signal for detecting the peak-crossing and valley-crossing of the inductor current. The inductor peak-current

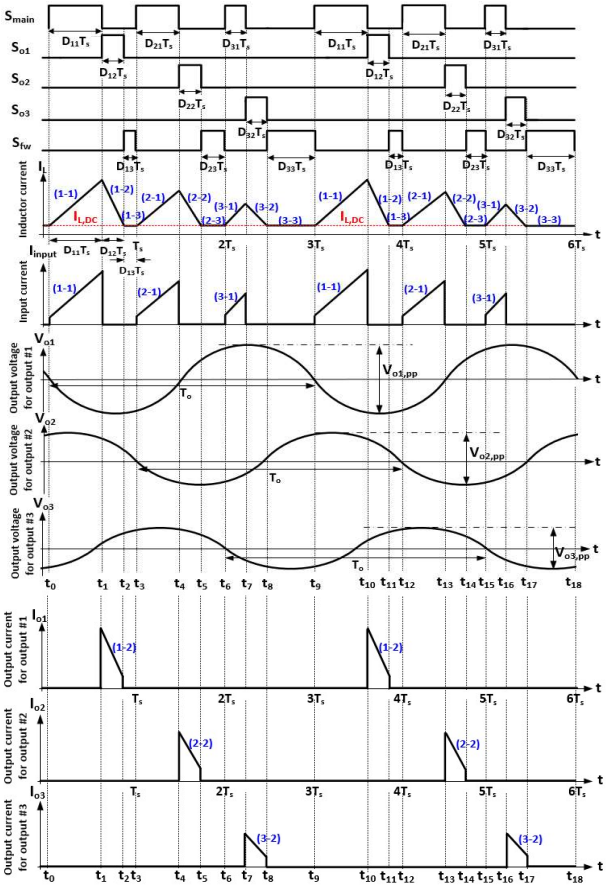
limits for the three outputs are denoted as $I_{L,peak1}$, $I_{L,peak2}$, and $I_{L,peak3}$, respectively. The valley-current limit for all three outputs is represented by $I_{L,valley}$. In PCCM, $I_{L,valley}$ has a positive value whereas in DCM, $I_{L,valley}$ is zero.

III. OPERATING PRINCIPLE

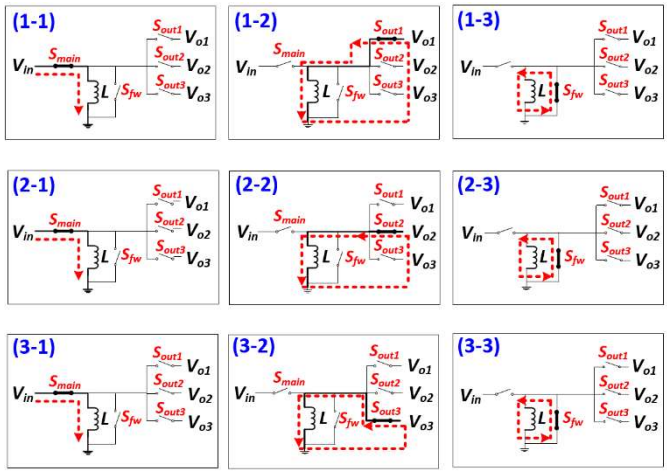
In this section, the operating principle of the proposed buck-boost single-inductor three-output (SITO) inverter is explained in detail. The same principle can easily be extended to a buck-boost SIMO inverter with a total of N outputs.

A. Waveforms and Equivalent Circuits

Fig. 7(a) shows the ideal waveforms of the ON/OFF status of all the switches, the inductor current, the input current, the output voltage, and the output current. The proposed SITO inverter is assumed to operate in PCCM at a fixed frequency with a switching period T_s. Unlike DCM, the inductor current is non-zero (with a positive DC offset of $I_{L,DC}$) during the *third* sub-interval in each switching period, i.e., (1–3), (2–3), and (3–3). Note that the first number within the parenthesis represents the output number and the second number represents the mode of operation. The proposed inverter can also operate in DCM in which the inductor current returns to zero in the third sub-interval. Fig. 7(b) shows the corresponding switching sequence of all the power switches.



(a)



(b)

Fig. 7. (a) Ideal timing diagram of the main switch, output switches, freewheeling switch, inductor current, input current, output voltage and output current for each of the three outputs and (b) the corresponding switching sequence of the proposed SITO inverter operating in PCCM.

For ease of discussion, the two back-to-back freewheeling MOSFETs in the actual circuit are modeled with a single ideal switch (S_{fw}). Likewise, the two back-to-back output MOSFETs in each output branch are represented by a single ideal switch (i.e., S_{out1}, S_{out2}, or S_{out3}). Here, the on-time duty ratios of the main switch (S_{main}) corresponding to the first, second and third outputs are uniquely represented as D_{11}, D_{21}, and D_{31}, respectively. The duty ratio is primarily determined by the peak limit of the inductor current. Fig. 7(a) illustrates the general case of the inverter having *unique* peak limits of the inductor current associated with the three individual outputs. The three output voltages also exhibit different peak-to-peak amplitudes. Hence, different output power levels can be generated for the SITO inverter which is also referred to as unbalanced load condition. For the special case of balanced load, identical power levels will be generated for the three AC outputs. This is made possible by ensuring that the inductor peak current limit is the same for all the outputs. On the other hand, the valley limit of the inductor current is determined by the DC offset of the inductor current, i.e., $I_{L,DC}$ as depicted in Fig. 7(a). All the outputs are assumed to have the same valley limit of the inductor current. It is interesting to note the direction of the output current during the second sub-interval, namely (1–2), (2–2), and (3–2), when the main inductor releases its stored energy to the corresponding AC output. Since an inverting buck-boost topology is used in the power stage, the output current actually travels in the opposite direction, i.e., from ground to each of the output node (V_{o1}, V_{o2}, and V_{o3}), during the second sub-interval.

B. Operating Modes

For the proposed SITO inverter operating in PCCM, there are *three* unique modes of operation in each switching period T_s. Without loss of generality, the first output is used as an example for illustrative purpose.

- Mode 1 (from time t_0 to t_1): The main switch S_{main} is turned

ON and the other switches are turned OFF. The inductor current I_L ramps up with a rising slope of $m_1 = V_{in}/L$. At the end of Mode 1, the inductor current reaches its peak value $I_{L,pk}$, and can be mathematically expressed as

$$I_{L,pk} = m_1 D_{11} T_s + I_{L,DC} = \left(\frac{V_{in}}{L}\right) D_{11} T_s + I_{L,DC} \quad (1)$$

where D_{11} is the on-time duty ratio of the first output and $I_{L,DC}$ is the DC offset of the inductor current. When the inductor current reaches its peak value $I_{L,pk}$, the inverter transitions from Mode 1 to Mode 2. Mode 1 for the first, second and third output are annotated as (1-1), (2-1), and (3-1), respectively, as shown in Fig. 7(a) and 7(b).

- Mode 2 (from time t_1 to t_2): The main switch S_{main} is turned OFF and the first output switch S_{out1} is turned ON while the other two output switches, i.e., S_{out2} and S_{out3}, are OFF. The inductor current I_L decreases with a falling slope of $m_2 = \frac{V_{o1}(t)}{L}$ until it becomes equal to $I_{L,DC}$. $V_{o1}(t)$ is the instantaneous value of the sinusoidal voltage of the first output, as depicted in Fig. 7(a). Since the inductor current (or output current) flows in the opposite direction from ground to the output node, m_2 has a negative value which indicates a falling slope. In reality, m_2 varies with the instantaneous value of the sinusoidal output voltage. As a first-order approximation, $V_{o1}(t)$ can be largely represented by the average value of the sinusoidal output voltage $V_{o1,avg}$ during Mode 2 which can be obtained as follows.

$$V_{o1,avg} = \frac{1}{D_{12}T_s} \int_{D_{11}T_s}^{(D_{11}+D_{12})T_s} V_{o1}(t)dt = \frac{1}{D_{12}T_s} \int_{D_{11}T_s}^{(D_{11}+D_{12})T_s} V_m \sin(\omega_o t + \beta) dt \quad (2)$$

where V_m is the amplitude of the sinusoidal output voltage V_{o1}, ω_o is the resonant frequency in radians, and β is the phase angle in radians.

It is important to realize that the switching period T_s is one-third of the resonant period T_o in the proposed SITO inverter, as depicted in Fig. 7(a). Hence, T_s can be expressed as

$$T_s = \frac{T_o}{3} = \frac{2\pi}{3\omega_o} \quad (3)$$

In general, for the SIMO inverter, $T_s = T_o/n$, where n is the number of AC outputs.

Therefore, by combining (2) and (3) and assuming zero phase angle ($\beta = 0$), $V_{o1,avg}$ can be written as

$$V_{o1,avg} = \frac{nV_m}{2\pi D_{12}} (\cos\theta_1 - \cos\theta_2) \quad (4)$$

where $\theta_1 = \frac{2\pi D_{11}}{n}$ and $\theta_2 = \frac{2\pi(D_{11}+D_{12})}{n}$.

Equation (4) can be re-expressed in terms of the sine function as follows.

$$V_{o1,avg} = \frac{nV_m}{2\pi D_{12}} \left[\sin(\frac{\pi}{2} - \theta_1) - \sin(\frac{\pi}{2} - \theta_2) \right] \quad (5)$$

Equation (5) can be simplified by assuming that $\left(\frac{\pi}{2} - \theta_1\right)$ and $\left(\frac{\pi}{2} - \theta_2\right)$ are relatively small. Typically, the small-angle approximation is applied for angles less than 0.2443 radians (or about 14°) which produces a 1% error. In other words, $\left(\frac{\pi}{2} - \theta_1\right)$ and $\left(\frac{\pi}{2} - \theta_2\right)$ must be no greater than 0.2443 which implies that an additional design constraint $\frac{D_{11}}{n} \geq 0.2111$ must be satisfied. By default, D_{11} is always smaller than 1. Hence, for a SITO inverter ($n = 3$), this design constraint is met as long as $0.6333 \leq D_{11} < 1$. In principle, by increasing the peak limit of the inductor current for a particular switching period T_s, a larger value of D_{11} can therefore be obtained.

Hence, by applying the small-angle approximation, Equation (5) can be reduced to

$$V_{o1,avg} = \frac{nV_m}{2\pi D_{12}} (\theta_2 - \theta_1) \approx -V_m \quad (6)$$

Equation (6) shows that the average value of the output voltage in Mode 2 is negative due to the fact that the *inverting* buck-boost topology is chosen for the power stage. In addition, the average value of the output voltage in Mode 2 can be largely represented by the amplitude of the output voltage. Intuitively, this approximation is valid if the time duration of Mode 2 is much shorter than the resonant period T_o, i.e., $D_{12}T_s << T_o$. This occurs when either the value of D_{12} is relatively small or the total number of outputs n in the SIMO inverter becomes large. In other words, the average value of the output voltage in Mode 2 remains nearly constant at around V_m. Consequently, the down-slope of the inductor current m_2 can be mathematically written as

$$m_2 \approx -\frac{V_{o1,avg}}{L} = \frac{V_m}{L} \quad (7)$$

The output switch S_{out1} remains ON until the non-zero valley current limit of the inductor is detected in PCCM (or zero current in DCM). At the end of Mode 2, S_{out1} is turned OFF and the inverter then transits from Mode 2 to Mode 3. In Fig. 7, Mode 2 of the first, second and third output are annotated as (1-2), (2-2), and (3-2), respectively.

- Mode 3 (from time t_2 to t_3): The main switch S_{main} and all the output switches (S_{out1}, S_{out2}, S_{out3}) are OFF. Only the free-wheeling switch (S_{fw}) is ON in order to maintain a positive DC inductor current $I_{L,DC}$ during Mode 3 (which is also known as the free-wheeling cycle in PCCM). In Fig. 7, Mode 3 of the first, second, and third outputs are annotated as (1-3), (2-3) and (3-

3), respectively. In particular, the proposed SITO inverter can operate in DCM by allowing the inductor current to return to zero in Mode 3. In this case, all the switches (including S_{fw}) remain OFF.

It is important to realize that the main inductor L is connected to the output circuit only during Mode 2 in which the storage energy in L is injected into the output load. However, in Mode 1 and 3, the output circuit is self-resonating because it is fully decoupled from L. The above switching sequence is repeated for the second and third output in the next two switching cycles during which S_{out1} remains OFF while S_{out2} and S_{out3} are alternatively switched ON. Only one output switch can be turned ON at any switching cycle. The storage energy in L is distributed across the three outputs sequentially in a time-interleaving manner. In general, the same switching sequence can be scaled conveniently for any number of AC outputs in a SIMO inverter. The energy being transferred from the shared inductor to each of the AC output loads can be independently controlled by adjusting the peak value of the inductor current corresponding to a particular output.

C. Switching Frequency

For the proposed SIMO inverter with n AC outputs, the switching frequency f_{sw} is n times larger than the resonant frequency of the LC resonant tank f_o. Mathematically, it can be expressed as follows.

$$f_{sw} = nf_o = \frac{n\omega_o}{2\pi} = \frac{n}{2\pi\sqrt{L_oC_o}} \tag{8}$$

where ω_o is the resonant frequency in radians, L_o and C_o are the resonant inductor and resonant capacitor in each output resonant tank, respectively.

For wireless power transfer applications, the switching (or resonant) frequency follows that of the required standards, e.g. Qi wireless power standard ranges between 80 kHz and 300 kHz for medium-power Qi chargers [5], [6]. At a particular resonant frequency, the appropriate values of L_o and C_o in the output resonant tank can be determined.

IV. THEORETICAL DERIVATIONS

The analytical proof of sinusoidal oscillations of the output voltage in each of the three operating modes of the proposed buck-boost SITO inverter will be provided in this section. Without loss of generality, only the first output phase of the proposed SITO inverter is initially considered in the theoretical analysis. A general expression of the sinusoidal output voltage will then be derived which can be applied to any of the three output phases of the SITO inverter. In addition, the scalability of SITO inverter to SIMO will be closely examined. A theoretical maximum number of AC outputs in the proposed SIMO inverter operating in either PCCM or DCM will be derived analytically.

A. Mode 1-Proof of Sinusoidal Oscillation

Fig. 8 shows the SITO inverter in Mode 1 operation.

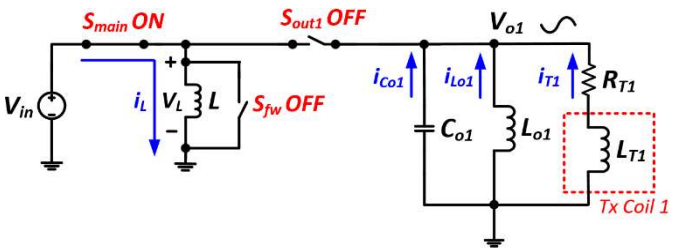


Fig. 8. Circuit diagram of the proposed buck-boost SITO inverter operating in Mode 1 for the first output phase.

Since the output switch (S_{out1}) is OFF, the output resonant circuit is completely separated from the DC voltage source (V_{in}). Since an inverting buck-boost topology is employed in the inverter, the branch current in the resonant tank (i.e., i_{Co1}, i_{Lo1}, and i_{T1}) actually flows from ground to the output node (V_{o1}). By invoking KCL at the common ground node, the sum of branch currents in the resonant tank can therefore be expressed as

$$i_{Co1}(t) + i_{Lo1}(t) + i_{T1}(t) = 0 \tag{9}$$

Equation (9) can also be re-written in the s-domain as follows.

$$I_{Co1}(s) + I_{Lo1}(s) + I_{T1}(s) = 0 \tag{10}$$

Since C_{o1} and L_{o1} are connected in parallel, $V_{co1}(t) = V_{Lo1}(t) = -V_{o1}(t)$. The current flowing across the resonant capacitor $i_{co}(t)$ can be written as

$$i_{Co1}(t) = C_{o1}\frac{dv_{Co1}(t)}{dt} = -C_{o1}\frac{dv_{o1}(t)}{dt} \tag{11}$$

By applying Laplace transform to (11), we have

$$I_{Co1}(s) = C_{o1}\left[sV_{Co1}(s) - V_{co1}\right] = -C_{o1}\left[sV_{o1}(s) + V_{o1}\right] \tag{12}$$

where V_{co1} and V_{o1} represent the initial values of the resonant capacitor voltage and output voltage (i.e., at time = t_0), respectively. That is, $V_{co1} = v_{co1}(t_0)$ and $V_{o1} = v_{o1}(t_0)$.

Similarly, the current through the resonant inductor in the s-domain can be expressed as

$$I_{Lo1}(s) = \frac{V_{Lo1}(s)}{sL_{o1}} + \frac{I_{Lo1}}{s} = -\frac{V_{o1}(s)}{sL_{o1}} + \frac{I_{Lo1}}{s} \tag{13}$$

where I_{Lo1} is the initial value of the resonant inductor current, i.e., $I_{Lo1} = i_{Lo1}(t_0)$.

In Fig. 8, the AC load consists of the resistor R_T connected in series with the inductance of the transmit coil L_T. Hence, the current flowing across the AC load can be written as

$$I_{T1}(s) = \frac{-V_{o1}(s) + L_{T1}I_{To1}}{R_{T1} + sL_{T1}} \tag{14}$$

where I_{To} is the initial current value through L_T, i.e., $I_{To} = i_T(t_0)$.

Now, by substituting (12), (13) and (14) into (10), we have

$$-C_{o1}\left[sV_{o1}(s)+V_{o1}\right]-\frac{V_{o1}(s)}{sL_{o1}}+\frac{I_{Lo1}}{s}+\frac{L_{T1}I_{To1}-V_{o1}(s)}{R_{T1}+sL_{T1}}=0 \quad (15)$$

By re-arranging the terms in (15), $V_{o1}(s)$ can be solved as follows.

$$V_o(s)=\frac{-sC_{o1}V_{o1}L_{o1}(R_{T1}+sL_{T1})+L_{o1}I_{Lo1}(R_{T1}+sL_{T1})+sL_{o1}L_{T1}I_{To1}}{s^2L_{o1}C_{o1}(R_{T1}+sL_{T1})+s(L_{o1}+L_{T1})+R_{T1}} \quad (16)$$

Assuming $L_T >> L_o$, Equation (16) can be reduced to

$$V_o(s)=K_1\frac{s}{s^2+\omega_o{}^2}+K_2\cdot\frac{1}{s^2+\omega_o{}^2}+K_3\cdot\frac{1}{s+\frac{R_T}{L_T}}$$

(17)

where $K_1=-V_{o1}+\frac{R_{T1}L_{o1}L_{T1}I_{To1}}{R_{T1}{}^2L_{o1}C_{o1}+L_{T1}{}^2}$ (18a)

$$K_2=\frac{I_{Lo1}}{C_{o1}}+\frac{L_{T1}{}^2I_{To1}}{C_{o1}(R_{T1}{}^2L_{o1}C_{o1}+L_{T1}{}^2)}$$

(18b)

$$K_3=\frac{-R_{T1}L_{o1}L_{T1}I_{To1}}{R_{T1}{}^2L_{o1}C_{o1}+L_{T1}{}^2} \quad (18c)$$

and $\omega_o=\frac{1}{\sqrt{L_oC_o}}$ (18d)

By invoking inverse Laplace transform to (17), the output voltage can be expressed in the time domain as follows.

$$v_{o1}(t)=a_1\cos(\theta_1)+b_1\sin(\theta_1)+c_1e^{-\left(\frac{R_{T1}}{L_{T1}}\right)t} \quad (19)$$

where $a_1 = K_1$, $b_1 = K_2\omega_o{}^{-1}$, $c_1 = K_3$, and $\theta_1 = \omega_o t$.

As the time t ultimately becomes large enough in steady-state condition, $e^{-\frac{R_{T1}}{L_{T1}}t}$ tends toward zero which means that the last term in (19) drops out. Hence, (19) can be further reduced to the following form.

$$v_{o1}(t)=a_1\cos(\theta_1)+b_1\sin(\theta_1) \quad (20)$$

Let $\sin(\beta_1)=\frac{a_1}{\sqrt{a_1{}^2+b_1{}^2}}$ and $\cos(\beta_1)=\frac{b_1}{\sqrt{a_1{}^2+b_1{}^2}}$. Equation (20) can thus be re-expressed as

$$v_{o1}(t)=\left(\sqrt{a_1{}^2+b_1{}^2}\right)\left[\cos(\theta_1)\sin(\beta_1)+\sin(\theta_1)\cos(\beta_1)\right]$$
$$=\left(\sqrt{a_1{}^2+b_1{}^2}\right)\sin(\theta_1+\beta_1)=\left(\sqrt{a_1{}^2+b_1{}^2}\right)\sin(\omega_o t+\beta_1) \quad (21)$$

From (21), it is proven that when the SIMO inverter operates in Mode 1, the output voltage $v_{o1}(t)$ is a pure sinusoidal signal whose frequency is identical to the resonant frequency ω_o of the $L_{o1}C_{o1}$ resonant circuit.

B. Mode 2-Proof of Sinusoidal Oscillation

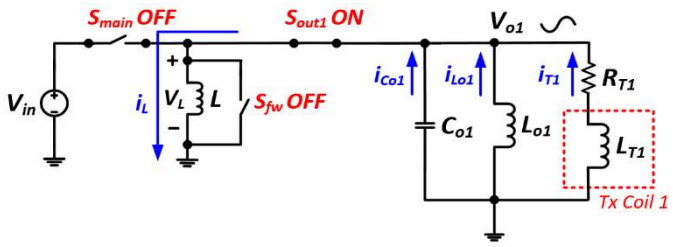


Fig. 9. Circuit diagram of the proposed buck-boost SITO inverter operating in Mode 2 for the first output phase.

Fig. 9 shows the inverter in Mode 2 operation. Unlike the boost-only SIMO inverter [17], the DC voltage source V_{in} is disconnected from the output node V_{o1} in Mode 2 since the main switch S_{main} is OFF. By using KVL, we have

$$v_L(t)+v_{o1}(t)=0 \quad (22)$$

where $v_L(t)$ is the instantaneous voltage across the main inductor L and $v_{o1}(t)$ is the instantaneous AC output voltage in the time domain. By applying Laplace Transform, Equation (22) can be re-expressed as

$$L\left[sI_L(s)-I_{L,peak}\right]+V_{o1}(s)=0 \quad (23)$$

where I_L(s) is the inductor current, $I_{L,peak}$ is the peak value of the inductor current, and V_{o1}(s) is the output voltage in the frequency domain.

Since $I_{L,peak}=\frac{D_{11}T_sV_{in}}{L}$, Equation (10) can be rewritten as

$$sLI_L(s)-D_{11}T_sV_{in}+V_{o1}(s)=0 \quad (24)$$

where D_{11} denotes the on-time duty ratio pertaining to Mode 1 for the first output.

By invoking KCL at the common ground node (as shown in Fig. 8), we have

$$i_L(t)=i_{Co1}(t)+i_{Lo1}(t)+i_{T1}(t) \quad (25)$$

where $i_L(t)$ is the inductor current, $i_{Co1}(t)$ is the current through the resonant capacitor C_{o1}, $i_{Lo1}(t)$ is the current through the resonant inductor L_{o1}, and $i_{T1}(t)$ is the current through the transmitter coil L_{T1}.

By applying Laplace Transform to (25), we have

$$I_L(s) = C_{o1}\left[sV_{o1}(s) - V_{o1}\right] + \frac{V_{o1}(s)}{sL_{o1}} + \frac{I_{Lo1}}{s} + \frac{V_{o1}(s) + L_{T1}I_{To1}}{L_{T1}s + R_{T1}} \quad (26)$$

where $V_{o1} = v_{o1}(t_1)$, $I_{Lo1} = I_{Lo1}(t_1) = I_{L,peak}$, $I_{To1} = i_{T1}(t_1)$, and $t_1 = t_0 + D_{11}T_s$.

By substituting (26) into (24) and then re-arranging, we have

$$V_{o1}(s) = \frac{1}{LC_{o1}}\left(V_{o1} - \frac{L_{T1}I_{To1}}{C_{o1}(R_{T1} + sL_{T1})}\right)\left(\frac{s}{s^2 + \frac{1}{LC_{o1}} + \frac{1}{L_{o1}C_{o1}}}\right) + \frac{1}{LC_{o1}}\left(\frac{I_{L,peak}}{C_{o1}} - \frac{I_{Lo1}}{C_{o1}}\right)\left(\frac{1}{s^2 + \frac{1}{LC_{o1}} + \frac{1}{L_{o1}C_{o1}}}\right) \quad (27)$$

Let $\omega_1^2 = \frac{1}{LC_{o1}} + \frac{1}{L_{o1}C_{o1}}$, Equation (27) can be expressed in terms of ω_1 as follows.

$$V_{o1}(s) = \frac{V_{o1}}{LC_{o1}}\left(\frac{s}{s^2 + \omega_1^2}\right) + \frac{1}{LC_{o1}^2}\left(I_{L,peak} - I_{Lo1}\right)\left(\frac{1}{s^2 + \omega_1^2}\right) - \frac{L_{T1}I_{T01}}{LC_{o1}^2}\left(\frac{1}{R_{T1} + sL_{T1}}\right)\left(\frac{s}{s^2 + \omega_1^2}\right) \quad (28)$$

Now, by performing partial fraction expansion on the last term of (28) and re-arranging, we have

$$V_{o1}(s) = \frac{V_{o1}}{LC_{o1}}\left(\frac{s}{s^2 + \omega_1^2}\right) + \frac{1}{LC_{o1}^2}\left(I_{L,peak} - I_{Lo1} - I_{To1}\right)\left(\frac{1}{s^2 + \omega_1^2}\right) + \frac{I_{T01}R_{T1}L_{o1}}{C_{o1}(L + L_{o1})}\left(\frac{1}{R_{T1} + sL_{T1}}\right) \quad (29)$$

Finally, by applying inverse Laplace transform to (29), the output voltage in the time domain can be expressed in the following form.

$$v_{o1}(t) = a_2\cos(\theta_2) + b_2\sin(\theta_2) + c_2 e^{-\left(\frac{R_{T1}}{L_{T1}}\right)t} \quad (30)$$

where $a_2 = \frac{V_{o1}}{LC_{o1}}$, (31a)

$$b_2 = \frac{1}{\omega_1 LC_{o1}^2}\left(I_{L,peak} - I_{Lo1} - I_{To1}\right), \quad (31b)$$

$$c_2 = \frac{I_{To1}R_{T1}L_{o1}}{L_{T1}C_{o1}(L + L_{o1})}, \quad (31c)$$

and $\theta_2 = \omega_1 t$. (31d)

Note that in steady-state condition, $e^{-\frac{R_T}{L_T}t}$ tends to zero which implies that the third term in (30) can be neglected.

So, Equation (30) becomes

$$v_{o1}(t) = a_2\cos(\theta_2) + b_2\sin(\theta_2) \quad (32)$$

Let $\sin(\beta_2) = \frac{a_2}{\sqrt{a_2^2 + b_2^2}}$ and $\cos(\beta_2) = \frac{b_2}{\sqrt{a_2^2 + b_2^2}}$.

Equation (32) can therefore be re-written in the following form.

$$v_{o1}(t) = \left(\sqrt{a_2^2 + b_2^2}\right)\left[\cos(\theta_2)\sin(\beta_2) + \sin(\theta_2)\cos(\beta_2)\right] = \left(\sqrt{a_2^2 + b_2^2}\right)\sin(\theta_2 + \beta_2) = \left(\sqrt{a_2^2 + b_2^2}\right)\sin(\omega_1 t + \beta_2) \quad (33)$$

Hence, it is proven that when the proposed buck-boost SIMO inverter operates in Mode 2, the output voltage $v_{o1}(t)$ is a pure sinusoidal signal whose frequency is given by $\omega_1 = \sqrt{\frac{1}{LC_{o1}} + \frac{1}{L_{o1}C_{o1}}}$. In particular, when $L >> L_{o1}$, $\omega_1 \approx \omega_0$, i.e., the frequency of the sinusoidal output voltage in Mode 2 is approximately equal to the resonant frequency of the LC resonant tank when the value of the main inductor L is much larger than that of the resonant inductor L_{o1}.

C. *Mode 3-Proof of Sinusoidal Oscillation*

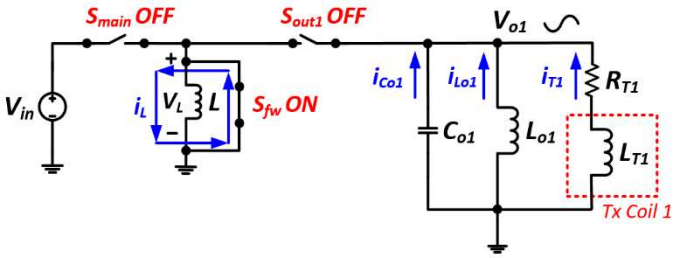


Fig. 10. Circuit diagram of the proposed buck-boost SITO inverter operating in Mode 3 for the first output phase.

Fig. 10 shows the proposed buck-boost inverter operating in Mode 3. Both S_{main} and S_{out1} are in their OFF position which means that the resonant tank is completely separated from the main inductor L. Despite the fact that there is a free-wheeling current across the inductor (in PCCM), the circuit analysis in Mode 3 remains the same as that in Mode 1. The only difference between these two modes is that the initial values for the output voltage and the resonant current in Mode 3 are obtained at time t_2 (instead of t_0), as depicted in Fig. 7(a). As a result, the proof of sinusoidal oscillation in Mode 1 continues to apply to Mode 3 and it follows that the frequency of the sinusoidal output voltage in Mode 3 is identical to that in Mode 1, i.e., $\omega_o = \frac{1}{\sqrt{L_{o1}C_{o1}}}$.

D. *Generalized Mathematical Description for the Sinusoidal Output Voltage*

The mathematical expressions of the output voltage for the three operating modes derived above correspond to the *first*

output phase only, i.e., from time t_0 to t_3 [see Fig. 7(a)]. Without loss of generality, the circuit parameters in the resonant tank are assumed to be the same for *all* the outputs. In general, the output voltage for the three operating modes can be expressed for any output phase in the following manner.

Mode 1:

$$\text{For } t\in(t_0+nT,t_1+nT)\ v_o(t)=\left(\sqrt{a_1^2+b_1^2}\right)\sin(\omega_o t+\beta_1) \tag{34}$$

$$\text{where } a_1=-v_o(t_0+nT)+i_T(t_0+nT)\left(\frac{R_T L_o L_T}{R_T{}^2 L_o C_o+L_T{}^2}\right),$$

$$b_1=\frac{1}{\omega_0}\left[\frac{i_{Lo1}(t_0+nT)}{C_o}+\frac{i_T(t_0+nT)}{C_o}\left(\frac{L_T{}^2}{R_T{}^2 L_o C_o+L_T{}^2}\right)\right],$$

$$\beta_1=\sin^{-1}\left(\frac{a_1}{\sqrt{a_1^2+b_1^2}}\right),$$

and n is an integer.

Mode 2:

$$\text{For } t\in(t_1+nT,t_2+nT),\ v_o(t)=\left(\sqrt{a_2^2+b_2^2}\right)\sin(\omega_1 t+\beta_2) \tag{35}$$

$$\text{where } a_2=\frac{v_o(t_1+nT)}{LC_o},$$

$$b_2=\frac{1}{\omega_0}\left[\frac{i_{Lo1}(t_1+nT)}{C_o}+\frac{i_T(t_1+nT)}{C_o}\left(\frac{L_T{}^2}{R_T{}^2 L_o C_o+L_T{}^2}\right)\right],$$

$$\text{and}\quad \beta_2=\sin^{-1}\left(\frac{a_2}{\sqrt{a_2^2+b_2^2}}\right).$$

Mode 3:

$$\text{For } t\in\{t_2+nT,(t_0+T)+nT\},\ v_o(t)=\left(\sqrt{a_3^2+b_3^2}\right)\sin(\omega_o t+\beta_3) \tag{36}$$

$$\text{where } a_3=-v_o(t_2+nT)+i_T(t_2+nT)\left(\frac{R_T L_o L_T}{R_T{}^2 L_o C_o+L_T{}^2}\right),$$

$$b_3=\frac{1}{\omega_o}\left[\frac{i_{Lo1}(t_2+nT)}{C_o}+\frac{i_T(t_2+nT)}{\omega_o C_o}\left(\frac{L_T{}^2}{L_T{}^2+R_T{}^2 L_o C_o}\right)\right],$$

$$\text{and}\quad \beta_3=\sin^{-1}\left(\frac{a_3}{\sqrt{a_3^2+b_3^2}}\right).$$

E. Extension from SITO to SIMO inverter

An important property of the proposed inverter architecture is its extension (or scalability) of SITO to SIMO with N number of AC outputs. In practice, only a finite number of AC outputs can be realized in a SIMO inverter mainly because of the fixed energy storage in the main inductor L and the chosen resonant frequency. A theoretical upper limit of the total number of AC outputs for the proposed SIMO inverter architecture will be formally investigated here.

Fig. 11 shows the timing diagram of the inductor current in a SIMO inverter. To maximize the number of outputs for a given resonant period T_o, the SIMO inverter operates at the boundary condition between PCCM and CCM with no freewheeling period. This allows the inductor current to reach its maximum peak value at a particular switching frequency T_s. Hence, for a given $I_{L,DC}$, maximum storage energy in the main inductor will be transferred to each AC output sequentially in a time-multiplexing manner. For ease of discussion, the SIMO inverter is assumed to operate under balanced load condition in which the same power is delivered from the main inductor to each output channel.

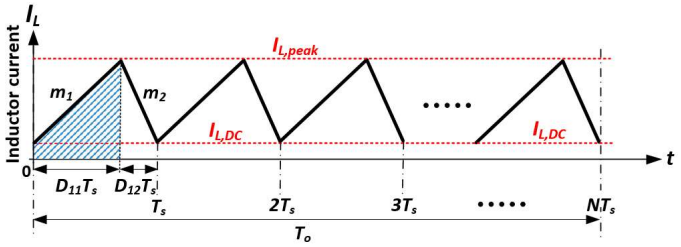


Fig. 11. Timing diagram of the inductor current of the SIMO inverter.

In Mode 1 of each output phase, the input current (or the average inductor current) is given by

$$I_{in}=\overline{I_L}=\frac{1}{T_o}\int_{nT_s}^{(n+D_{on})T_s} i_L(t)dt \tag{37}$$

where n is a positive integer ranging from 0 to (N-1) and D_{on} is the on-time duty ratio. Since the peak value of the inductor current is identical for all the outputs due to the balanced load condition, D_{on} has the same value across all the outputs, i.e., $D_{on} = D_{11} = D_{21} = \ldots = D_{N1}$. Notice that the integral in (37) is represented by the blue shaded area as shown in Fig. 11. Hence, (37) can be expressed as

$$\overline{I_L}=\frac{V_{in}D_{on}{}^2T_s^2+2D_{on}LI_{L,dc}T_s}{2LT_o} \tag{38}$$

First, the ideal SIMO inverter is assumed to be lossless. Hence, the input power P_{in} can be written as

$$P_{in}=V_{in}I_{in}=V_{in}\overline{I_L}=\frac{V_{in}{}^2D_{on}{}^2T_s^2+2V_{in}D_{on}LI_{L,dc}T_s}{2LT_o} \tag{39}$$

Since $P_{in} = P_{out}$ for a lossless SIMO inverter (where P_{out} is the output power per channel), we have

$$P_{in}=P_{out}=\frac{V_{in}{}^2D_{on}{}^2T_s^2+2V_{in}D_{on}LI_{L,dc}T_s}{2LT_o} \tag{40}$$

By re-arranging the terms in (40) and applying $T_o = nT$, the following quadratic equation can be obtained.

$$2LP_{out}n_{\max}{}^2-2V_{in}D_{on}LI_{L,DC}n_{\max}-V_{in}{}^2D_{on}{}^2T_o=0 \tag{41}$$

where n_{max} is the maximum possible number of outputs.

The discriminant Δ of (41) is given by

$$\Delta=4D_{on}{}^2V_{in}{}^2\left(L^2I_{L,dc}{}^2+2LP_{out}T_o\right)>0 \tag{42}$$

Since Δ always takes a positive value, it implies that the quadratic equation in (41) has two real roots (r_1, r_2) which can be represented as

$$r_1, r_2 = \frac{D_{on} V_{in} I_{L,dc} \left(1 \pm \sqrt{1 + \frac{2 P_{out} T_o}{L I_{L,dc}^{\ 2}}} \right)}{2 P_{out}} \tag{43}$$

Since n_{max} must be a positive integer, the negative root is therefore eliminated. Hence, we have

$$n_{\max} = floor \left(\frac{D_{on} V_{in} I_{L,dc} \left(1 + \sqrt{1 + \frac{2 P_{out} T_o}{L I_{L,dc}^{\ 2}}} \right)}{2 P_{out}} \right) \tag{44}$$

Equation (44) defines the theoretical maximum total number of AC outputs in the proposed SIMO inverter operating at the boundary condition of PCCM and CCM. In periodic steady state, the net change of the inductor current I_L in zero [see Fig. 11]. Hence, by invoking volt-second balance, we have

$$m_1 D_{on} T_s = m_2 (1 - D_{on}) T_s \tag{45}$$

Since $m_1 = V_{in}/L$ and $m_2 \cong V_m/L$, the on-time duty ratio D_{on} can be expressed as

$$D_{on} = \frac{V_m}{V_{in} + V_m} \tag{46}$$

where V_m is the amplitude of the sinusoidal output voltage and V_{in} is the DC input voltage.

By substituting (46) into (44), we have

$$n_{\max} = floor \left(\frac{V_{in} V_m I_{L,dc} \left(1 + \sqrt{1 + \frac{2 P_{out} T_o}{L I_{L,dc}^{\ 2}}} \right)}{2 (V_{in} + V_m) P_{out}} \right) \tag{47}$$

From (47), the theoretical *maximum* number of outputs for the proposed SIMO inverter operating at the boundary condition of PCCM and CCM can be analytically derived. For simplicity, each output of the SIMO inverter is assumed to be connected to a pure resistive load R_L, the real power P_{out} can be expressed in terms of V_m and R_L as follows.

$$P_{out} = \frac{V_{o,rms}^{\ 2}}{R_L} = \frac{V_m^{\ 2}}{2 R_L} \tag{48}$$

where $V_{o,rms}$ is the RMS value of the output voltage and $V_{o,rms} = \frac{V_m}{\sqrt{2}}$. Hence, for a particular output power P_{out}, V_m can be easily determined from (48) for a fixed value of R_L. As an example, the scalability of the proposed SIMO inverter is examined with these parameter values: $I_{L,dc}$ = 2 A, T_o = 10 µs, L = 6 µH, and R_L = 50 Ω. The relationship between n_{max} and P_{out} for three different values of the input voltage, i.e., V_{in} = 5 V, 12 V and 24 V, can be obtained from (47) which is graphically represented in Fig. 12.

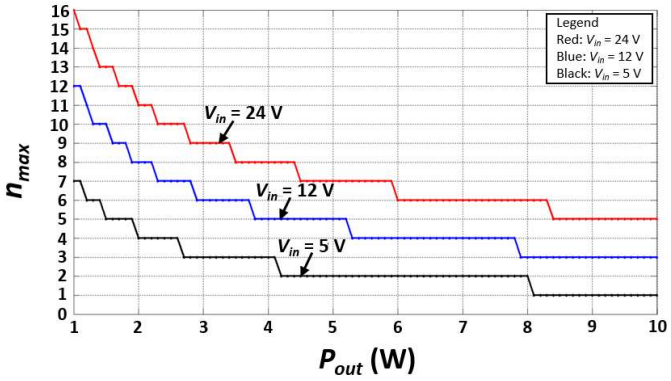


Fig. 12. Plot of the theoretical maximum number of outputs (n_{max}) versus output power per channel (P_{out}) of the proposed SIMO inverter operating at the boundary condition between PCCM and CCM.

Fig. 12 shows a general trend that the maximum achievable number of outputs decreases with increasing output power per channel. Intuitively, since the maximum amount of energy being stored in the main inductor is fixed, increasing the output power level means that fewer number of output channels can be attained in the SIMO inverter. Additionally, as the input voltage (or input power) is increased for a given output power, a larger number of outputs can be achieved in the SIMO inverter. Indeed, Fig. 12 is beneficial to a practical SIMO design because the maximum possible number of outputs at a given output power can be conveniently extracted from the plot.

In reality, the presence of the parasitic resistances (such as the ESR of the inductor or capacitor, the on-resistance of the power switch, etc.) in a practical SIMO inverter reduces the power conversion efficiency (η), i.e., $P_{out} = \eta P_{in}$, where $0 < \eta < 1$. Likewise, by applying $P_{in} = P_{out}/\eta$ to (39) and then solving for n_{max}, we have

$$n_{\max} = floor \left(\frac{\eta V_{in} V_m I_{L,dc} \left(1 + \sqrt{1 + \frac{2 P_{out} T_o}{\eta L I_{L,dc}^{\ 2}}} \right)}{2 (V_{in} + V_m) P_{out}} \right) \tag{49}$$

Equation (49) gives a more realistic scalability model for the proposed SIMO inverter which takes into consideration the effects of the power efficiency. For a given output power, as the power efficiency decreases, the maximum achievable number of outputs will also be reduced. Fig. 13 contains a 3-D plot of the theoretical maximum number of AC outputs (n_{max}) versus the output power per channel (P_{out}) and the power efficiency (η).It can be seen from Fig. 13 that for a fixed output power per channel, an increasing number of outputs can be achieved in the proposed SIMO inverter by improving the power efficiency. Specifically, given an output power of 6 W per channel, the total number of outputs can be increased from 3 to 4 when the power efficiency is increased from 80% to 90% or above. Likewise, at a particular power efficiency, an increasing number of outputs can be realized

by reducing the output power level per channel. For instance, at a power efficiency of 85%, the total number of outputs can be increased from 3 to 5 when the output power per channel reduces from 9 W to 4 W.

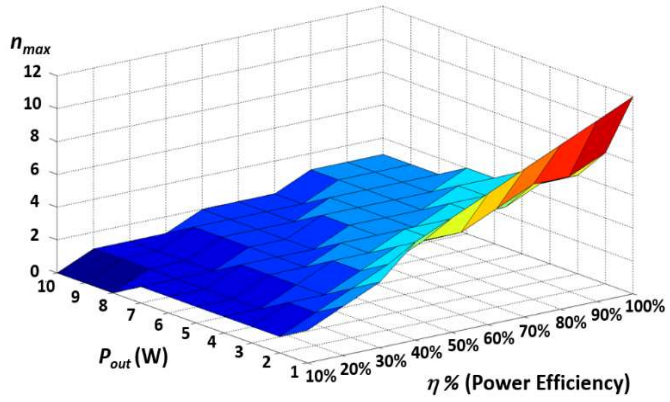


Fig. 13. A 3-D plot showing the relationship between the theoretical maximum number of outputs (n_{max}) and the output power per channel (P_{out}) and the power conversion efficiency (η).

In particular, when there is no DC offset in the inductor current, i.e., $I_{dc} = 0$, the SIMO inverter operates in Boundary Conduction Mode (BCM) which is special case of DCM with no freewheeling period. Hence, by substituting $I_{L,dc} = 0$ and $P_{in} = P_{out}/\eta$ into (39), we have

$$n_{\max} = floor\left(\frac{V_{in}V_m}{(V_{in}+V_m)} \sqrt{\frac{\eta T_o}{2LP_{out}}} \right) \qquad (50)$$

Equation (50) defines the maximum total number of AC outputs in the proposed SIMO inverter operating in BCM.

V. SIMULATION VERIFICATION

Real-time simulations are conducted using the PSIM software in order to verify the functionality of the proposed buck-boost SITO inverter. The design specifications of the proposed SITO inverter are listed in Table I. For illustration purpose, the following simulation verifications assume that each of the three outputs is connected to a pure resistive load, namely R_{T1} or R_{T2} or R_{T3}.

TABLE I. DESIGN SPECIFICATIONS OF THE PROPOSED BUCK-BOOST SITO INVERTER.

Design Parameter	Value
Input voltage (V_{in})	12 V
Switching frequency (f_{sw})	300 kHz
Output resonant frequency (f_o)	100 kHz
Main inductor (L)	6 µH
ESR of the main inductor (measured at 300 kHz)	90 mΩ
Capacitor in the resonant tank (C_{o1}, C_{o2}, C_{o3})	0.22 µF
ESR of the resonant capacitor (measured at 100 kHz)	30 mΩ
Inductor in the resonant tank (L_{o1}, L_{o2}, L_{o3})	11.5 µH
ESR of the resonant inductor (measured at 100 kHz)	12 mΩ
Load resistor (R_{T1}, R_{T2}, R_{T3})	22 Ω

First, the SITO inverter operating in PCCM under the balanced load condition is examined in which the three sinusoidal output voltages have the same frequency and magnitude. Fig. 14 shows the simulated waveforms of the buck-boost SITO inverter with three identical resistive loads.

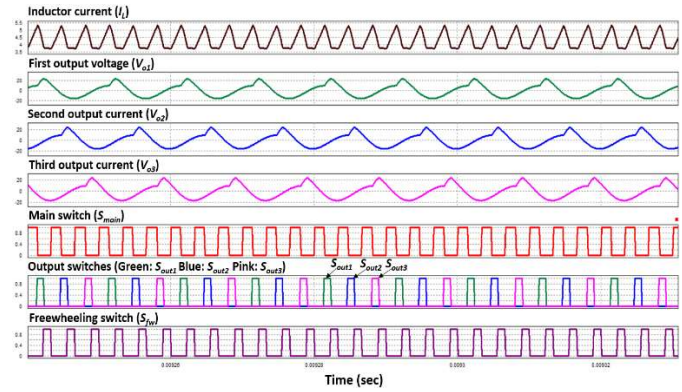


Fig. 14. Simulated waveforms of the proposed buck-boost SITO inverter with three identical resistive loads.

The simulated results show that each of the three inverter output voltages has a sinusoidal-like shape with an RMS value of around 11.5 V and a fundamental frequency of 100 kHz. It is interesting to note that there is some distortion in the output voltage during the transition from Mode 1 to Mode 2. This is mainly due to the fact that the value of the main inductor (L = 6 µF) is *not* much larger than that of the resonant inductor (L_o = 11.5 µF) which causes the frequency in Mode 2 to be slightly greater than that in Mode 1. This has been mathematically verified in Section IV Part B. Also, notice that the phase difference between any two outputs is 120°. In general, for a SIMO inverter, the phase difference between any two outputs is $2\pi/n$, where n is the total number of AC outputs. The simulated results also verify that the proposed SITO inverter operates in PCCM since the inductor current I_L has a non-zero DC offset of around 3.75 A during the freewheeling period. On the other hand, the SITO inverter operating in PCCM under the unbalanced load condition is also investigated. In this scenario, the three sinusoidal-like output voltages have the same frequency but different RMS values. Fig. 15 shows the corresponding simulated waveforms.

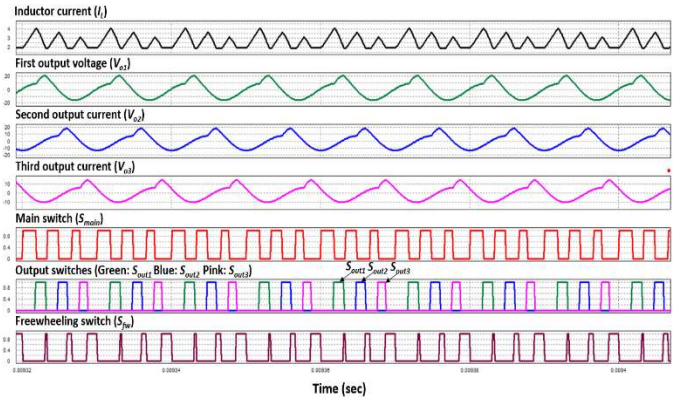


Fig. 15. Simulated waveforms of the buck-boost SITO inverter with three distinct output voltages.

For a fixed DC input voltage of 12 V, the simulated RMS voltage

values of the first, second and third output are 11.50 V, 9.89 V, and 7.57 V, respectively. In contrast with the case of balanced load, the inductor current I_L exhibits distinct peak values for each of the three outputs in this unbalanced load scenario [see Fig. 15]. With a fixed DC offset of the inductor current, the output power in each individual channel is regulated by adjusting the peak threshold of the inductor current. Hence, the simulated results verify that the proposed SITO inverter is capable of producing 100 kHz sine waves with low distortion regardless of whether the output load is balanced or unbalanced.

VI. EXPERIMENTAL VERIFICATION

Based on the design specifications from Table I, a hardware prototype of the proposed SITO inverter [see Fig. 16] is constructed for experimental verification. The power stage of the SITO inverter is implemented on a single printed circuit board (PCB) which contains discrete components and ICs, of which the part numbers are listed in Table II. This PCB has two layers with a copper thickness of 2 oz for reducing the trace resistance. For the custom-made main inductor (L), the core material is N41. Its coil has a total of 4 turns and is made up of 240 strands of 38 AWG (0.1 mm) wires. For each of the three custom-made resonant inductors (L_{o1}, L_{o2}, L_{o3}), the core material is T35. Its coil has a total of 8 turns and is made up of 60 strands of 38 AWG (0.1 mm) wires. In addition, three pairs of the off-the-shelf transmitting coil [28] and receiving coil [29] are used [see Fig. 16]. Each transmitting coil has only one layer and it has an inductance of 24 µH, a DC resistance (DCR) of 70 mΩ, and a rated current of 6 A. Each receiving coil also has one layer and it has an inductance of 7.3 µH, a DCR of 200 mΩ, and a rated current of 2.5 A.

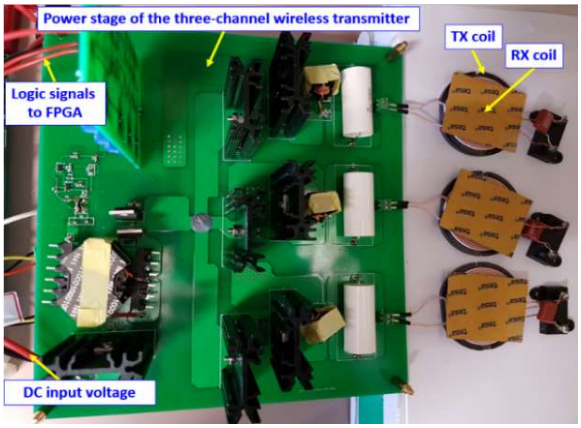


Fig. 16. Experiment setup of the proposed buck-boost SITO inverter.

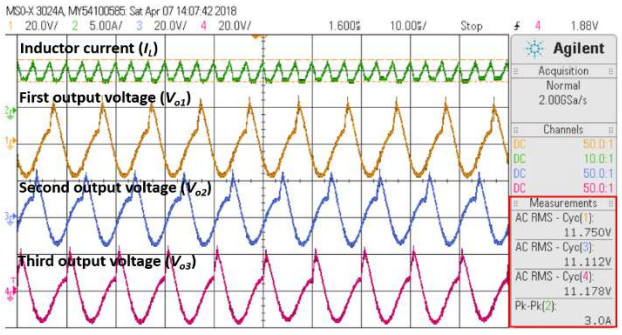
In the experiment setup, the digital control logic [see Fig. 5] is realized using Xilinx Spartan-3E FPGA [30]. By detecting the peak-crossing and valley-crossing events of the inductor current, the digital controller generates the appropriate gate drive signals for all the power switches. A very small 50 mΩ current-sensing resistor is connected in series with the main inductor for sensing the inductor current. The voltage across the current-sensing resistor is amplified by a wide-bandwidth op amp [31] which has a unity-gain bandwidth of 200 MHz. A 4-ns fast comparator [32] is subsequently used to compare the output voltage from the op amp against the peak (or valley) threshold for each output channel in order to generate the logic signals to the FPGA.

The component count and the per-unit cost of each component are also listed in Table II. The total BOM cost of the power stage of the SITO inverter, excluding the receiver side and the feedback controller, is estimated to be around US$57.51 per unit. The actual BOM cost can be reduced for higher volume production.

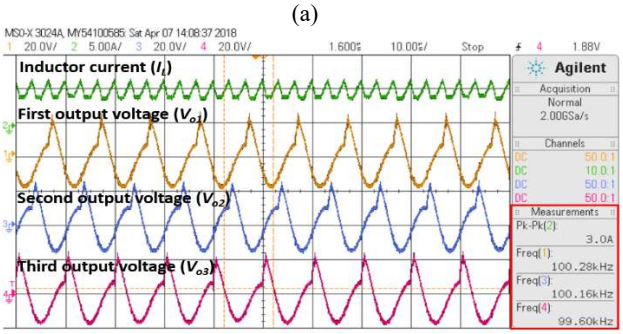
TABLE II. LIST OF COMPONENTS USED IN PROTOTYPE.

Component	Part No.	Quantity	Est. cost per unit (in USD)
Power Stage			
Main Inductor (L)	Custom-made	1	2.25
Power MOSFET	IPP083N10N5AKSA1	9	0.94
Gate Driver	SI8261BAC-C-IS	5	1.37
Current-Sensing Resistor	MP930	1	2.42
Resonant Capacitor (C_{o1}, C_{o2}, C_{o3})	940C10P22K-F	3	2.25
Resonant Inductor (L_{o1}, L_{o2}, L_{o3})	Custom-made	3	0.74
Transmitting (TX) Coil	760308100110	3	9.52
Receiving (RX) Coil	760308103211	3	6.18
Output Resistor (R_{L1}, R_{L2}, R_{L3})	RCH25S22R00JS06	3	6.74
Feedback Circuits			
Operational Amplifier	OPA354	1	0.832
Comparator	AD8611	4	2.48
Xilinx FPGA	Spartan-3E (XC3S250E)	1	26.67

In the first experiment, a balanced load condition is investigated in which the three sinusoidal output voltages of the SITO inverter have the same amplitude. Each of the three outputs is initially connected to a pure resistive load of the same value (i.e., 22 mΩ). Fig. 17 shows the measured waveforms of the inductor current I_L and the corresponding output voltage (V_{o1}, V_{o2} or V_{o3}) in each of the three independently-driver outputs. Even though the waveforms shown in Fig. 17(a) and Fig. 17(b) are identical, their measurements are different. In particular, Fig. 17(a) shows that the measured RMS values of the three output voltages which are 11.75 V, 11.112 V, and 11.178 V, respectively. Fig. 17(b) shows that the three output voltages have the same frequencies which are around 100 kHz with a phase difference of 120°. In either of these figures, the actual measurement values are indicated by the red box in the lower right corner. It is experimentally verified that the proposed SITO inverter produces three nearly identical sinusoidal-like output voltages of the same amplitude and frequency. No voltage spikes are observed in the three output voltages. Some distortion is seen in output voltage waveforms only when the SITO inverter makes a transition from Mode 1 to Mode 2, which is consistent between simulation and experiment. The measurement results clearly indicate that the SITO inverter operates in PCCM since the measured inductor current has a non-zero offset with a peak-to-peak value of 3.0 A.



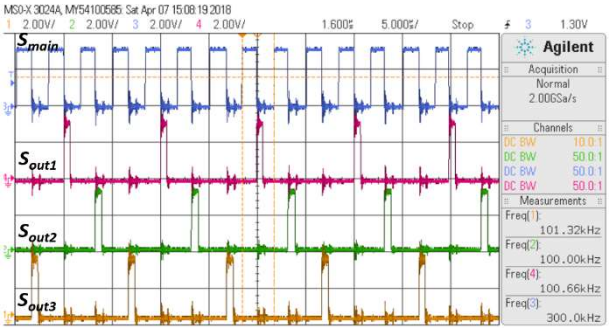
(a)



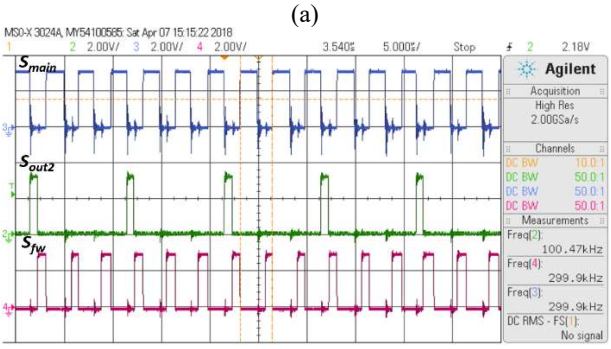
(b)

Fig. 17. Measured waveforms of the inductor current I_L and the three output voltages (V_{o1}, V_{o2}, V_{o3}) with (a) comparable RMS values and (b) same frequencies under the balanced load condition.

Fig. 18(a) shows the actual switching sequence for the gate drive signals of the main switch (S_{main}) and the three output switches (S_{out1}, S_{out2}, S_{out3}). Fig. 18(b) shows the switching order for the gate drive signals of the main switch (S_{main}), the second output switch (S_{out2}), and the freewheeling switch (S_{fw}).



(a)



(b)

Fig. 18. Measured waveforms of (a) the switching sequence for the gate drive signals of the main switch (S_{main}) and the three output switches (S_{out1}, S_{out2}, S_{out3}) and (b) the switching sequence for the gate drive signals of the main switch (S_{main}), the second output switch (S_{out2}), and the freewheeling switch (S_{fw}).

In the second experiment, an unbalanced load condition is examined in which the SITO inverter produces different peak voltage amplitudes among the three outputs. Fig. 19 shows the measured waveforms of I_L, V_{o1}, V_{o2}, and V_{o3}. Obviously, the three sinusoidal output voltages are shown to have distinct RMS values. The measured RMS values of V_{o1}, V_{o2} and V_{o3} are 11.372 V, 9,185 V, and 7.975 V, respectively. Also, from Fig. 19, it is observed that the measured inductor current has distinct peak values across the three output channels.

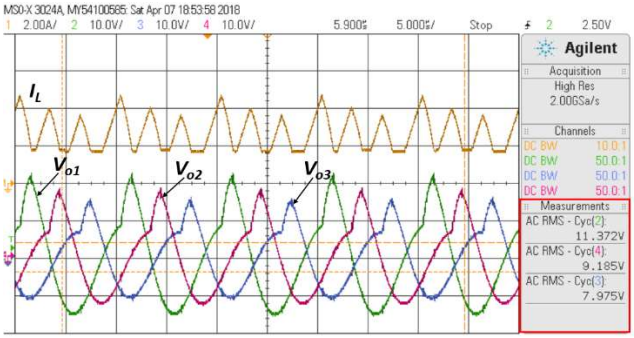
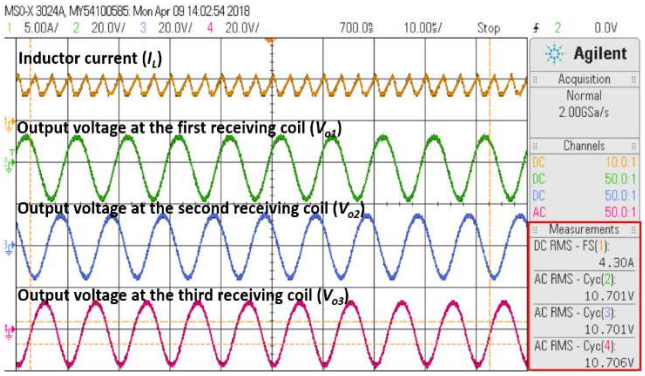
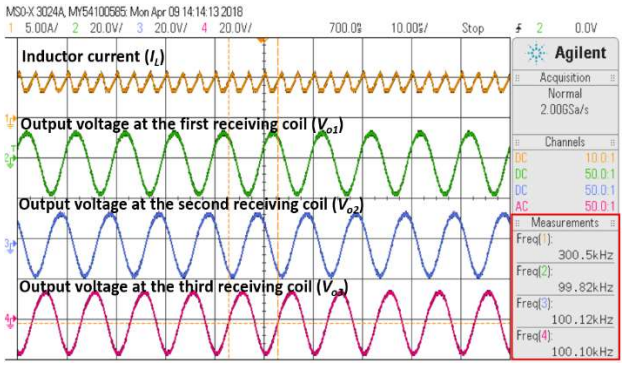


Fig. 19. Measured waveforms of the inductor current I_L and the three output voltages (V_{o1}, V_{o2}, V_{o3}) with distinct RMS values in the proposed SITO inverter operating under the unbalanced load condition.

For practical applications of wireless power transfer, each of the three individual outputs in the proposed SITO inverter is now connected to an off-the-shelf transmitter coil that is tightly coupled with a loaded receiver coil [see Fig. 15]. Basically, the SITO inverter acts as a three-channel wireless power transmitter. Fig. 20 shows the measured waveforms of the output voltage corresponding to the first, second and third wireless channel under the balanced load condition. The output voltage is measured at the loaded receiving coil. The measured RMS values for the three sinusoidal output voltages are in very close agreement with each other (i.e., the RMS values of V_{o1}, V_{o2}, and V_{o3} are 10.701 V, 10.701 V, and 10.706 V). It is experimentally verified that the output voltage in each channel is a smooth sine wave with a fundamental frequency of around 100 kHz. No voltage spikes are observed in the measured output voltage waveforms. Table III contains the measured RMS amplitude of the first harmonic (i.e., the fundamental frequency) as well as the first five harmonics of the fundamental. The measured total harmonic distortion (THD) is around 5.87%.



(a)



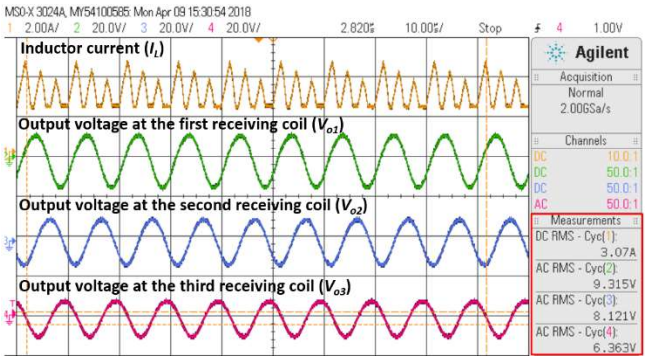
(b)

Fig. 20. Measured waveforms of the inductor current I_L and the output voltages (V_{o1}, V_{o2}, V_{o3}) at the receiving coils with (a) identical RMS values and (b) the same frequencies under the balanced load condition.

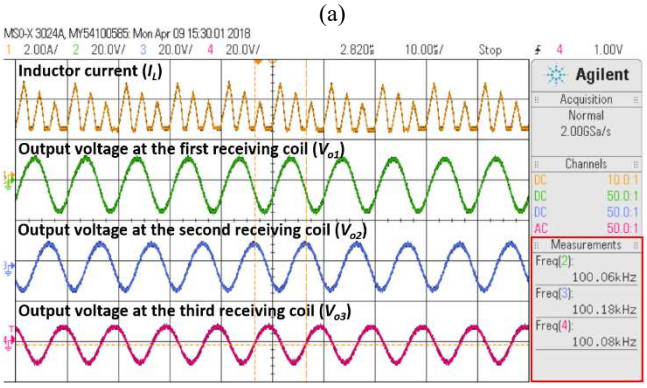
TABLE III. MEASURED HARMONIC CONTENTS OF THE OUTPUT VOLTAGE WAVEFORM.

Frequency (kHz)	Harmonic #	Measured V_{rms} (V)
100	1	9.975500
200	2	0.576050
300	3	0.100464
400	4	0.039917
500	5	0.011597
600	6	0.013794

The unbalanced load scenario is also examined by employing the same experiment setup as shown in Fig. 16. Fig. 21 shows that the measured waveforms of the three sinusoidal output voltages have different RMS values. The output voltage waveform continues to appear as a clean sine wave with a fundamental frequency of 100 Hz.



(a)



(b)

Fig. 21. Measured waveforms of the inductor current I_L and the three output voltages (V_{o1}, V_{o2}, V_{o3}) of the SITO inverter with (a) distinct RMS values and (b) same frequencies under the unbalanced load condition.

In summary, the experimental results demonstrate that the proposed SITO inverter is capable of generating three sinusoidal output voltages with independent peak values from a single DC power supply. No noticeable cross-regulation is observed in the SITO inverter operating in PCCM. The functionality of the digital controller is also experimentally verified. The inductor current flowing into each of the three output channels is independently regulated by using the peak and valley current control. Given an input power of 29.88 W, the measured power efficiency of the proposed SITO inverter at the rated output power of 8.4 W per channel (i.e., total output power of 25.2 W) is around 84.3%.

Table IV compares the power stage of the proposed SITO inverter topology with that of the prior art [7]–[10], [14], [15], in terms of the number and type of amplifier or inverter, the number of transmitting (TX) or receiving (RX) coils, the total output power as well as the total number of switches and passive components being used.

TABLE IV. COMPARISON OF THE PROPOSED SITO INVERTER TOPOLOGY WITH THE PRIOR ART.

	No. & Type of Power Amplifier or Inverter	No. of TX Coils	No. of RX Coils	Total Output Power
Nguyen et al. [7]	2 Class-E Power Amplifier	2	2	6 W
Waters et al. [8]	2 Class-E Power Amplifier	2	1	5 W
Shi et al. [9]	6 Class-D Power Amplifier	6	1	18 W
Johari et al. [10]	5 Low-voltage Amplifier	2	1	< 1 W
NXP MWCT1200DS [14]	1 Full-bridge Inverter	3	1	5 W
NXP WCT1001(03)A [15]	1 Full-bridge Inverter	3	1	5 W
This Work	**SITO**	**3**	**3**	**25 W**

TABLE IV (Continuation). COMPARISON OF THE PROPOSED SITO INVERTER TOPOLOGY WITH THE PRIOR ART.

	No. of Switches	No. of Resonant Inductors	No. of Resonant Capacitors
Nguyen et al. [7]	2	6	6
Waters et al. [8]	2	6	6
Shi et al. [9]	24	3	3
Johari et al. [10]	8	4	2
NXP MWCT1200DS [14]	10	0	1
NXP WCT1001(03)A [15]	7	2	2
This Work	**9**	**3**	**3**

For a fair comparison, the total number of switches listed in Table IV includes not only the power transistors inside the power amplifier (or inverter) but also any discrete switches in the power stage of the wireless power transmitter (e.g. the switches in the coil selection or power multiplexer circuit).

According to Table IV, the proposed SITO inverter uses a reasonable number of switches and passive components, compared to the prior arts. For an increased output power level (> 15 W), the SITO inverter topology employs a much smaller number of power switches than the multiple power amplifier topology reported in [9]. Both topologies use the same number of resonant inductors and resonant capacitors. Compared with its counterparts, the SITO inverter produces the highest total output power of 25 W (or more than 8 W per channel). It also supports a larger number of RX coils (i.e., 3 RX coils) which enables the charging of three independent devices simultaneously.

VII. CONCLUSIONS

This paper proposes a single-stage DC-AC buck-boost SIMO inverter which employs only a single inductor in the power stage to generate multiple independent high-frequency sinusoidal output voltages. By adjusting the peak and valley current limits of the inductor current, the output power of each individual output channel can be independently controlled. The scalability of the SITO inverter to SIMO is formally investigated, which leads to a general mathematical model for predicting the maximum achievable number of AC outputs in the SIMO inverter. Compared with the previous boost-only SITO inverter, the proposed buck-boost SITO inverter can achieve a significantly higher output power rating of 8.4 W per channel. A useful application of this inverter is that it can act as a multi-channel wireless transmitter for a multi-device wireless transfer system with low-to-medium power ratings. Both the simulated and experimental results confirm the effectiveness of the single-inductor three-output (SITO) inverter in achieving precise and independent power control across the three individual outputs with zero cross-regulation.

ACKNOWLEDGMENT

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