A NANO-POWER TUNEABLE EDGE-DETECTION CIRCUIT

Timothy G Constandinou[1], Julius Georgiou[1,3] and Chris Toumazou[1,2]

[1] EEE Dept, Imperial College of Science, Technology and Medicine, London, SW7 2BT, UK.
[2] Toumaz Technology Limited, Culham Science Centre, Abington, Oxfordshire, OX14 3DB, UK.
[3] Geosilicon Limited, 7 Thessalonikis Avenue, Strovolos, Nicosia 2020, Cyprus.

ABSTRACT

A useful nanopower circuit is presented for edge detection in integrated vision systems. Based on a compact front-end of only five MOS devices, this circuit features a tunable threshold and discrete output; ideal for interfacing to digital electronics.

1. INTRODUCTION

In next generation vision systems, the traditional software-based processing is being transferred to the front-end as custom in-built hardware. This provides the advantage of real-time operation; a necessity in many vision applications. This processing includes tasks such as edge detection [1], contrast enhancement and localised automatic gain control [2]. For these tasks to be realised in hardware; the circuits must fulfil three criteria; ultra-low power consumption, optimised circuit simplicity and robustness. These are all crucial for these circuits require to be implemented in every pixel, as illustrated in the organisation shown in Fig. 1.

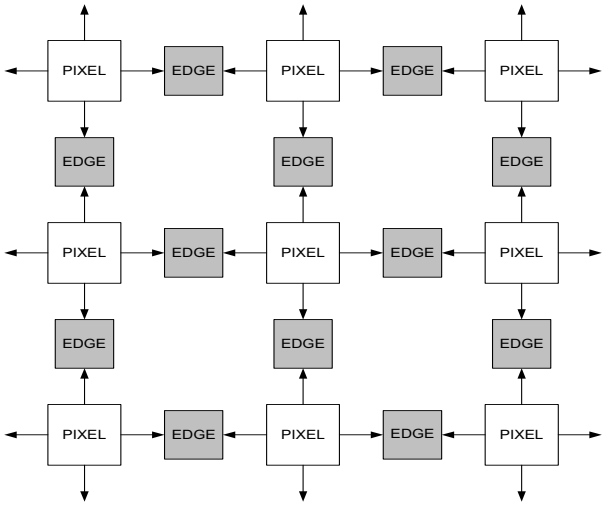

Fig. 1 Typical organisation of a first-order pixel-level edge detection architecture.

In this paper a circuit block based on an unconventionally biased differential pair is presented for the task of real-time edge detection. The circuit core is based on only five devices; all biased in weak inversion for nano-power operation. Furthermore, quantitative analysis of subthreshold matching confirms reliable and robust operation of this circuit block.

2. CIRCUIT DESCRIPTION

The schematic shown in Fig. 2 illustrates two neighbouring pixels with interconnected edge detection circuitry. Included are the photodetector circuits (one required per pixel,) the edge detection circuit (shaded in grey,) and the bias current generator and copying circuits.

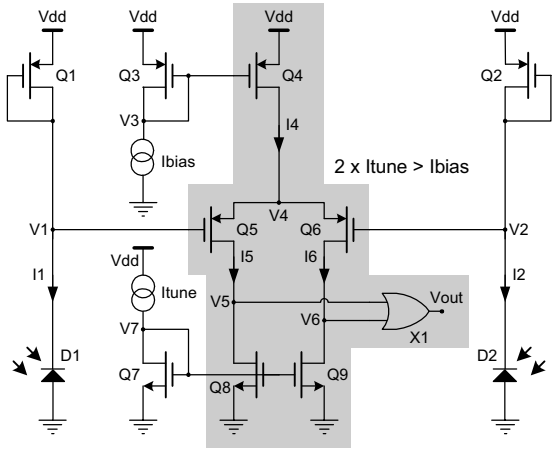

Fig. 2 Circuit schematic of the micropower discrete edge detector; the shaded area representing the devices repeated per edge detection element.

Devices D1, Q1 and D2, Q2 form the continuous-time logarithmic photodetector circuits for the two neighbouring pixels. The photocurrents I_1 and I_2 develop logarithmically related voltages (V_1 and V_2) across the diode-connected devices (Q1 and Q2 respectively.) This differential voltage (V_1, V_2) is connected to the PMOS differential pair (Q5 and Q6) sourced by the current I_4 (mirrored from the bias current; I_{bias}.) The differential pair

tail currents are sunk via the current mirror (Q7, Q8 and Q9) which is controlled by the tuning current; I_{tune}.

The operation is as follows:

- I_{bias} is chosen to be the same order of magnitude as the minimum value of photocurrents I_1 and I_2 in order to ensure devices Q4, Q5 and Q6 are in saturation and operating in weak inversion.

- I_{tune} is adjusted to lie in between $I_{bias}/2$ and I_{bias} and sets the allowed tolerance before indicating an edge and flagging it up. This will set the gate-source voltages of devices Q8 and Q9. This voltage will in turn determine the maximum current that can be sunk from the drains of Q8 and Q9 (I_{d8max} and I_{d9max} respectively). Assuming devices Q5 and Q6 are ideally matched, this circuit operates in one of two states:

  1. **$V_1=V_2$:** Since $I_{bias}/2 < I_{tune} < I_{bias}$ then $I_5 < I_{d8max}$ causing device Q8 to be in the ohmic region. This in turn will cause V_5 to sit barely above ground and similarly Q9, I_6 and V_6 will behave in the same way. As a result of V_5 and V_6 both being low, V_{out} will also output low indicating there is no edge.

  2. **$V_1 \neq V_2$:** For example, if $V_1 < V_2$ such that $I_5=I_{d8max}$ then device Q8 is in saturation and V_5 rises to just below V_{dd}. However $I_6<I_{d9max}$ so device Q9 is still in the ohmic region, keeping V_6 low. This will result in V_{out} outputting high indicating there is an edge.

3. CIRCUIT ANALYSIS

A general expression describing the basic operation of the MOS transistor in the weak inversion region is:

$$I_D = I_0 \cdot \exp\left(-\frac{V_G}{nV_T}\right)\left(\exp\left(-\frac{V_S}{nV_T}\right)-\exp\left(-\frac{V_D}{nV_T}\right)\right) \quad (1)$$

Assuming devices Q5 and Q6 are operating in saturation, the following expression can be derived, expressing the output current (differential.)

$$I_5 - I_6 = I_{bias} \cdot \tanh\left(\frac{V_1 - V_2}{2nV_T}\right) \quad (2)$$

This can be split as to provide the single-ended tail current expressions.

$$I_5 = \frac{1}{2} I_{bias}\left[1+\tanh\left(\frac{V_1 - V_2}{nV_T}\right)\right] \quad (3)$$

$$I_6 = \frac{1}{2} I_{bias}\left[1-\tanh\left(\frac{V_1 - V_2}{nV_T}\right)\right] \quad (4)$$

From (2,) the large and small signal transconductance of the differential pair can be derived [3].

$$G_m = \frac{d(I_5 - I_6)}{d(V_1 - V_2)} = \frac{I_{bias}}{2nV_T}\sec^2\left(\frac{V_1 - V_2}{2nV_T}\right) \quad (5)$$

$$g_m = \frac{I_{bias}}{2nV_T} \quad (6)$$

Expression (5) can be used to express the range of values for which the circuit will flag an edge detected.

$$I_{tune} - \left(G_m\left(V_{ERR} + |V1 - V2|\right)\right) < 0 \quad (7)$$

Where V_{ERR} is the error term expressing the total mismatch error in the differential pair as an input referred voltage.

4. MATCHING

An instrumental design issue for ensuring circuits operating in weak inversion will work is device matching. The device mismatch arises from process parameter variations mainly in gate oxide thickness and doping concentrations, resulting in device threshold voltage and drain current variations. Since the gm/I ratio is at a maximum for devices operating in weak inversion, this signifies that subthreshold circuits are those most affected by device mismatch [4]. Therefore for robust high performance circuits with good manufacturing yields; the micropower designer must not rely on absolute model parameters but rather on good matching between identically designed and carefully laid out devices. For example, in device pairs closely separated, the threshold voltage mismatch dependence on the active area [5] is given by the following expression:

$$\sigma\Delta V_{th} = \frac{A_{vt}}{\sqrt{W \times L}} + C_o \quad (8)$$

Where: $\sigma\Delta V_{th}$ is the standard deviation in threshold voltage, W x L is the device active area and A_{vt} and C_o are fit constants. Simulating using a threshold voltage spread of ($V_{th}\pm 2\sigma\Delta V_{th}$) covers 96% of mismatch deviations and therefore gives a good indication of mismatch related performance variations in addition to circuit robustness.

Device Pair [Separation]	WL	$2\sigma\Delta V_{th}$ (mV)	Local error (%Current)	Input ref. err. ($\sigma\Delta V_{in}$/mV)	Effect of mismatch
Q1, Q2 [S=100µm]	9	2.462	6.80	1.055	Fixed pattern noise (FPN) will cascade to other blocks.
	25	1.456	4.41	0.625	
	100	0.700	2.30	0.301	
Q3, Q4 [S=10µm]	9	1.904	5.67	3.960	Variation in tunability amongst identical blocks.
	25	1.298	4.76	3.010	
	100	0.842	3.85	1.706	
Q5, Q6 [S=10µm]	9	1.904	1.77	0.816	Asymmetric operation, i.e. non-linear distortion.
	25	1.298	1.66	0.557	
	100	0.842	0.77	0.361	
Q7, Q8, Q9 [S=10µm]	9	2.830	9.09	3.894	Variation in tunability amongst identical blocks.
	25	1.780	5.26	2.029	
	100	1.026	2.74	0.978	

Table 1 Simulation data for critically matched device groups with corresponding mismatch errors for various sizes; providing both local and input referred error. Assuming devices are of equal areas with I_{bias}=5nA and I_{tune}=3nA. The shaded entries represent the selected device dimensions to be used.

5. DESIGN TARGETS

The target design specifications for the nano-power tunable edge-detection cell are listed in table 2.

Sub-block	Log Pixel	Edge Detector	Current Copiers
Device count	2 large area	5 large area 6 digital	2 large area
Active area (µm²)	1000	276	50
Mismatch error (max.)	4.21%	2.35%	6.82%
Current consumption (per unit cell)	Typically 10nA	5nA	7.5nA
Power consumption (per unit cell)	18nW	9nW	13.5nW
Power consumption (n x m matrix)	18nW*(n)(m)	9nW*(n-1)m + 9nW*(m-1)n	13.5nW*n

Table 2 Target hardware design specifications for edge-detector cell

6. SIMULATIONS

This circuit was simulated using the Spectre simulator under the Cadence IC design environment with foundry supplied models for a standard 0.18um CMOS process. Figure 3 illustrates the tunability of this circuit, i.e. for different values of I_{tune}, by plotting the output voltage (V_{out}) versus the differential input voltage (V_1-V_2.) Since V_1 and V_2 are logarithmic compressions of photocurrents I_1 and I_2, the differential input voltage (V_1-V_2) represents the ratio of the photocurrents (I_1/I_2.) This is further illustrated in Figure 4, showing the operating regions for V_{out}=low and V_{out}=high.

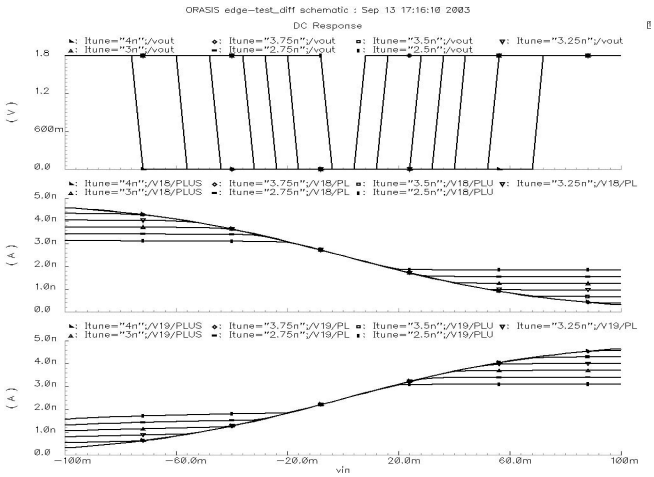

Fig. 3 Simulation results of output voltage (V_{out}) plotted against input differential voltage (V_1-V_2) for different values of I_{tune}; illustrating the tunable sensitivity. Assuming perfectly matched devices with I_{bias}=5nA.

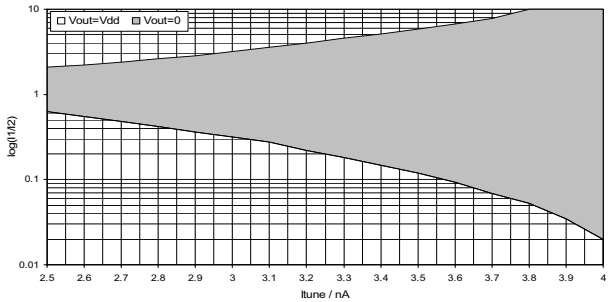

Fig 4. Simulation results showing the photocurrent ratio (I_1/I_2.) versus the tuning current illustrating the operating regions for V_{out}=low (no edge) and V_{out}=high (edge.)

The device pairs (or groups) requiring to be well-matched in the presented circuit are listed in Table 1, including simulated results for different device sizes and their corresponding mismatch errors.

7. CONCLUSION

Presented is an elegant circuit cell for implementing a core processing task; edge detection in early vision systems. This technique not only offers a reduced circuit complexity to alternative methods but also the versatility of being able to dynamically tune the sensitivity. Using careful layout techniques, device mismatch has been kept to the critical minimum to guarantee both robustness and high manufacturing yield. As edge-detection is a fuzzy computation, for example this is to be used to determine boundaries of biological cells [6]; any mismatch will usually translate to a shifting of the edge by a pixel or two. Most importantly, having been designed to operate from a 1.8v supply requiring only 7nA current, the total power consumption per block is under 13 nano-watts!

8. ACKNOWLEDGEMENTS

The authors wish to acknowledge the Basic Technology grant (UKRC GR/R87642/02) and the AMx technology grant (EPSRC GR/R96583/01,) in addition to Toumaz Technology Limited for sponsoring this research.

9. REFERENCES

[1] M. D. Rowley, J. G. Harris, “A comparison of three one-dimensional edge detection architectures for analog VLSI vision systems,” IEEE ISCAS’97, Proceedings of, Vol. 3, pp. 1840-1843, 1997.

[2] T. Delbruck, C. A. Mead, “Analog VLSI adaptive logarithmic wide-dynamic-range photoreceptor,” IEEE ISCAS’94, Proceedings of, pp. 339-342, 1994.

[3] J. Georgiou “Micropower Electronics for Neural Prosthetics,” PhD Thesis, Imperial College London, UK, 2002.

[4] A. Papasovic, A. G. Andreou, C. R. Westgate, “Characterisation of Subthreshold MOS Mismatch in Transistors for VLSI Systems,” Analog IC’s & Signal Processing, Proceedings of, 6, pp. 75-85, 1994.

[5] K. R. Lakshmikumar, R. Hadaway, M Copeland, “Characterization and modelling of mismatch in MOS transistors for precision analog design,” IEEE Journal of Solid-state circuits, Vol. SC-21, pp. 1057-1066, Dec. 1986.

[6] T. G. Constandinou, T. S. Lande, C. Toumazou, “Bio-pulsating architecture for object-based processing in next generation vision systems,” IEE Electronics Letters, Vol. 39, No. 16, pp. 1169-1170, 2003.