

Bandgap States in Solution-Processed Semiconductors

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This thesis describes the work carried out during the period of September 2012 to March 2017 within the Department of Physics, Imperial College London. The material presented herein is the product of my own work, except where explicit references have been made, and has not been previously submitted in whole or in part for an award of a degree at this or any other institutions.

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Abstract

The field of plastic electronics has opened up a new material set with which to produce microelectronics including metal oxides, polymers and small molecules. These materials are versatile in properties and processing techniques, already outmatching amorphous silicon. Thin film transistors (TFTs) produced from these materials state mobility as the highest figure of merit; while ignoring the effect that trap states on charge transport. The two are inextricably linked though as regularly observed in the gate dependence of measured field effect mobilities.

This thesis presents an in-depth analysis of bandgap trap states within low-temperature, and solution-processed, high performance phototransistors and low voltage TFTs. This thesis first discusses the Grünewald bandgap analysis method used to calculate semiconductor bandgap states from a single TFT measurement. The second section demonstrates solution-processed, low temperature (≤ 200 °C) dyed-sensitized thin-film phototransistors consisting of indium oxide (In_2O_3) and the organic dye D102. Devices exhibit an ultrahigh photosensitivity of 10^6 and responsivity of 2×10^3 A/W. Bandgap analysis identified photoinduced n-doping of the channel as the likely mechanism. The final section presents a direct comparison of four high-k dielectric layers used as insulators within In_2O_3 based TFTs. An identical low-temperature (≤ 200 °C), solution-processed route was used to produce aluminium oxide (AlO_x), hafnium oxide (HfO_x), yttrium oxide (YO_x), and zirconium oxide (ZrO_x) films. The usage of AlO_x , HfO_x & ZrO_x dielectric layers resulted in functioning TFTs with on/off ratios of 10^5 , operating below 3 V. The In_2O_3 mobility exhibited a dielectric dependence with average values of 2.0, 6.4, and 18.7 cm^2/Vs for AlO_x , HfO_x and ZrO_x respectively. The bandgap analysis was used to eliminate trap states as a possible cause for this dielectric dependent mobility.

In conclusion, bandgap analysis of current semiconducting materials greatly improves the understanding of potential candidates for future high performance solution processed microelectronics.

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1 Introduction

Only four copies of this thesis will ever be printed by the author. Therefore, to read this work on a piece of paper it is likely that you have used a computer connected to the internet¹ and printer to create a physical copy. Hence, the need to explain the importance of electronics within our modern world is definitely superfluous. The electronic devices required to simply read this paragraph on paper span from logic circuits, memory and microprocessors to sensors and actuators. All of which have been heavily influenced by the development of current semiconductor physics.

1.1 Conventional Electronics

The basic building blocks of logic circuits and microprocessors are transistors, which are solid state switches. The power of a microprocessor is dependent on both the operating speed of its clock and the number of individual transistors, which is controlled by the size of an individual transistor and the size of the chip it is developed on. To illustrate the development speed of microprocessors; since 1971 clock speeds of central processing units (CPUs) produced by the chip behemoth 'Intel' have increased by 10^4 (as reported in **Table 1.1**). Not only have the operating frequencies increased, but the number of transistors on a single chip has increased by 10^7 (as included in **Table 1.1**), aided by increased manufacturing resolution.

Table 1.1: Progress of Intel chips from 1971 to 2012.²

Chip Name	Year	Clock Speed	# Transistors	Manufacture Size
Intel 404	1971	108 kHz	2300	10 μm
Intel 286	1982	6 MHz	134×10^3	1.5 μm
Intel Pentium	1993	66 MHz	3.1×10^6	800 nm
Intel Pentium II	1998	300 MHz	7.5×10^6	250 nm
Intel Pentium 4	2000	1.5 GHz	42×10^6	180 nm
Intel Core 2 Duo	2008	2.4 GHz	410×10^6	45 nm
2 nd Gen Intel Core	2010	3.8 GHz	1.16×10^9	32 nm
3 rd Gen Intel Core	2012	2.9GHz	14×10^9	22 nm

Silicon is the basis of the modern semiconductor industry. Silicon can be doped to become N or P type, hence having majority electron or majority hole carriers. This along with its ability to form the high bandgap dielectric (SiO_2) upon oxidation, allows the creation of complementary metal-oxide-semiconductor (CMOS) circuits from a single material. Yet, the limitations of the material system of silicon and silicon dioxide have already started to show, such as silicon dioxide's low dielectric constant of 3.9 and silicon's limited electron and hole mobilities of $\sim 1000 \text{ cm}^2/\text{Vs}$ and $\sim 400 \text{ cm}^2/\text{Vs}$ respectively.³ Higher dielectric constants lead to lower power consumption when switching CMOS circuits compared to low permittivity dielectrics. This is due to the lower voltages that the circuits can be operated at. In addition, the electron mobilities are lower than other semiconductors such as the newer III-V semiconductor of GaAs at $\sim 9000 \text{ cm}^2/\text{Vs}$.⁴ Even though silicon should be fully replaced by newer combinations of materials, the established knowledge of manufacture and control technologies developed for silicon means that new materials, which are being developed to supersede silicon, are nevertheless often being integrated with silicon wafers.

Until recently, the modern industry of microprocessor design and manufacture was based around standardized memory and logic devices. Application specific integrated circuits (ASIC), custom built with a specific purpose, were often based on standardized logic and memory devices with the need to integrate those devices after manufacture. The design costs, manufacture specific requirements and limited performance of these products and placed system performance in the hands of the manufacturers.⁵

In the last decade, this design and manufacturer relationship has changed, mainly due to foundry services offering integrated system on chip (SoC) and system in a package (SiP) devices⁵. This, coupled with the increased frequency with which new semiconductor technologies are being brought to market, has allowed companies such as ARM Holdings plc, ARC International plc and Imagination Technologies Group plc to flourish. These companies are based on a business model (at the time of writing) of creating licenses and intellectual property based on designs for various graphical processing units and system on chips (SoCs), while never manufacturing a single device.

1.2 Plastic Electronics

The field of plastic electronics provides a new material and processing set that can create a market inaccessible by conventional electronics. The field's name originates from its focus on the development of semiconducting organic molecules, epitomized by the Nobel Prize of Heeger, MacDiarmid and Shirakawa "for the discovery and development of conductive polymers"⁶. As a field, it more loosely encompasses the development of electronics using unconventional materials, processes or structures. The work in this thesis focuses on metal oxide TFTs, using conventional materials such as hafnium oxide (HfO_x) (currently touted as a potential successor to the technologically aged silicon dioxide (SiO₂)) and indium oxide (In₂O₃) (commonly used in its doped form as transparent contacts within display technologies). Although these materials are neither organic, nor plastic; the organic ligand based precursors and organic solvents used to solution process these layers bring them neatly into the remit of this field.

Plastic electronics is very unlikely to provide a technological competitor to silicon or III-V semiconductors used in high-end processors. The unique selling point of plastic electronics, however, is its flexibility: flexibility in processing methods, flexibility in material properties and physical flexibility. By processing semiconductors, insulators and conductors from solution, new additive manufacturing techniques are now accessible. Two examples of promising production methods that highlight the manufacturing advantages of plastic electronics over conventional electronics are the high-throughput roll-to-roll (R2R) systems and the easily accessible ink-jet printing.

Starting with R2R processing, R2R systems can use multiple techniques including gravure printing, rotary screen printing and evaporation all in a single setup. The ultimate aim of roll-to-roll is to produce large area electronics, such as solar cells, both rapidly and at lower costs than conventional electronics. Another target product is the mass manufacture of disposable electronics, such as radio-frequency identification (RFID) tags. The commercial aim is to drive the cost of a single RFID tag low enough that it is financially viable to monitor all stock items using an individual RFID tags included on the packaging at manufacture.

Ink-jet printing may be used to produce electronics at high quantities. But, like conventional ink-jet printing, the power of this technique is the ability to program a new pattern into the printer for each new production. This makes it an ideal system for producing custom made devices with limited-performance, or rapid prototyping. If successfully developed it could

be to small companies and hobbyist electronics what the advent of 3D printing is to manufacturing⁷.

This thesis covers the development of materials, via experimental fabrication, characterisation and theoretical-based analysis, for future upscaling. The majority of the experimental work in this thesis is grounded in TFT structures produced from solution processed metal oxides with a limited maximum processing temperature of 200 °C. When developing semiconducting materials for TFTs, the field effect transistor (FET) mobility, is often held as the highest figure of merit.⁸⁻¹¹ In comparison, the effect of trap states within the bandgap of a semiconductor is often ignored or used flippantly without analysis to describe trends in FET mobility. To rectify this, this thesis will provide a systematic analysis of the electronic structure of semiconductors being studied, specifically indium oxide. From this approach, extra evidence vital in elucidating possible charge transport and energetic mechanisms was gained. Finally, from the experimental work produced for this thesis and the subsequent analysis, three guidelines for the further development of metal oxide TFTs from solution will be outlined.

1.3 Thesis Outline

The structure of this thesis starts by introducing the experimental techniques used to fabricate and characterise the devices produced. Following this is a general discussion of important theoretical models for TFTs, and semiconductor transport. The theoretical models discussed are included to provide a background for the first chapter of work by the author. Chapter 4 discusses a model of bandgap states, a method to analyse bandgap states, and the application of that method during four separate collaborations. The first experimental section, Chapter 5, reports on the experimental results of phototransistors fabricated with In_2O_3 . While the second and final experimental section, Chapter 6, presents a comparative study of four materials used to produce the dielectric layer within TFT structures. After the conclusion, additional information on calculation derivations, and other supplementary information is included as appendices.

2 Experimental Techniques

2.1 Fabrication Techniques

Current research into electronics broadly splits into two categories: that of high-performance conventional electronics and also novel unconventional electronics. Conventional state-of-the-art microprocessors are produced from extremely pure materials via patterning techniques such as photolithography and maskless e-beam lithography. Research into these conventional techniques is attempting to improve the resolution of photolithography by using extreme UV light sources and also trying upscale e-beam as a technique by progressing to multiple e-beam lithography.⁵

In this work the term unconventional electronics is used to describe novel materials, new fabrication routes or both. The new materials involved range from metal oxides¹² and nanostructures¹³ (such as nanowires and nanotubes) to small organic molecules and polymers¹⁴. The fabrication methods being developed include lab scale processes such as spin-casting¹⁵ and adhesion lithography¹⁶ and large scale techniques like spray coating¹⁷ and gravure printing¹⁸.

Within this work I have focused on facile processing techniques; reducing the specialist equipment required and hence manufacturing costs if translated to industry. Following this ethos, ideal devices would be produced outside of clean rooms, within ambient air, at temperatures compatible with the use of plastic substrates (≤ 200 °C). Also the work was performed with the aim of using inexpensive, non-hazardous, and environmentally friendly precursor materials when possible. These guiding principles were followed throughout this work, though exceptions had to be made to deposit metallic contacts.

2.1.1 Spin-Casting

Spin-casting is a method of creating uniform thin films of liquid on a substrate. If the liquid is an appropriate solution, sol-gel or dispersion it may be converted into a solid film via evaporation, annealing or other similar process. The solution is dispensed onto the substrate, which is attached to the spin caster chuck either mechanically or by a weak vacuum. The chuck is then rotated, normally using speeds from 100 – 6000 rpm, spreading the solution over the substrate due to the centrifugal force.

The three most important parameters when spin-casting are the rotational acceleration, the final rotational speed and the length of time of the spin-casting.¹⁹ The final rotational speed is the most important factor in controlling the thickness of the liquid film, decreasing film thickness with increased revolutions per minute. It also affects the uniformity of the film, with higher rotational speeds increasing uniformity.¹⁵ The solution itself is very important in determining both the thickness of the liquid film and any solid film formed from the liquid. The length of the spin-casting time should be enough that the forces acting on the solution on the substrate reach an equilibrium.

2.1.2 Annealing & Conversion

Film annealing, of a liquid film, is the process of driving of liquid from a dispersion (whether it be a colloidal suspension or solution) to leave behind a solid film. It can also refer to the heating of a solid film to provide energy to alter the material's microstructure, often resulting in an increase in crystallinity of the material. On the other hand, conversion describes processes that use the applied thermal energy to induce or accelerate a chemical reaction within the solution. Within this thesis, the majority of films are metal oxides produced from precursor solutions, where applied heat to the solution will both drive off the solvent and cause chemical conversion of the precursor. Therefore, annealing acts to both anneal the film and convert the precursor, though for simplicity from here on it shall be labelled as just annealing.

In_2O_3 is the most commonly used semiconductor within this work. It was formed from a solution of the metal complex indium (III) nitrate hydrate in either deionized water or 2-methoxyethanol using a concentration of 40 mg/ml. Specific solution compositions and concentrations for the experimental work conducted by the author as part of this thesis can be found in Sections 5.2.1 and 6.2.2. The following process can be used to describe film formation of In_2O_3 , but also can be generalized to most metal oxide film formations within this thesis. The metal complex solute dissolves in the solvent (either deionized water or 2-methoxyethanol) due to the organic ligands surrounding the central metal ion. Within the solution it is then possible for a sol-gel to form as the precursor undergoes hydrolysis and polycondensation.²⁰ After being deposited on a substrate, via a process such as spin-casting, the film can be annealed. The thermal energy will drive off the remaining solvent and ligands, and assists in the formation of a thin layer of metal oxide.

The temperature required to convert a metal complex fully can be gained from thermogravimetric analysis (TGA). This measures the change in mass of a sample as a function of applied temperature. To convert a precursor fully, normally requires high temperatures (> 400 °C), but even a partial conversion at a temperature lower than the conversion temperature can produce effective films. For example **Figure 2.1** shows the TGA of indium nitrate hydrate where complete conversion does not occur till around 400 °C.²¹ Yet it has previously been shown that effective devices have been made at lower temperatures (~ 250 °C), with performance decreases at higher temperatures.²² Possible causes of the performance decrease at higher processing temperatures are due to the effect that heat will have on microstructure, optical properties and electrical properties.²²⁻²⁶

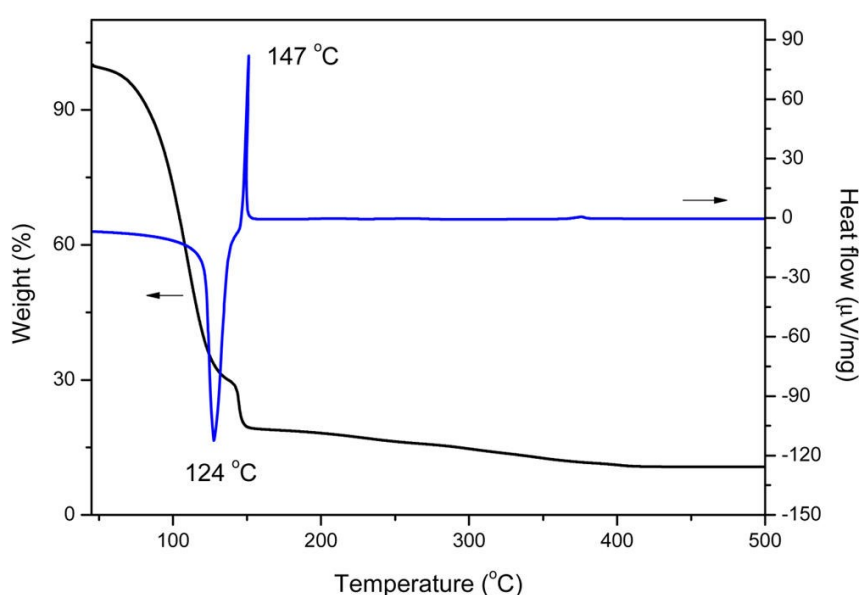


Figure 2.1: Thermogravimetric analysis of indium nitrate hydrate in 2-methoxyethanol as performed by J. Lee et al.²¹ (Reprinted with permission from Lee et al.²¹. Copyright 2013, American Chemical Society.)

2.1.3 Self-Assembled Monolayers

Self-assembled monolayers (SAMs) are spontaneously formed assemblies of organic molecules on a surface, attached via adsorption. The molecules used to form a SAM consist of a head group that allows chemisorption onto the chosen surface, and a functionalizing group. The head group is chosen for its ability to form a strong bond with the material surface: for example, using a phosphonic acid group²⁷ to attach the SAM to a metal oxide film. The functionalizing group can

serve one of many purposes, from changing the wetting properties²⁸ to reducing electronic traps at semiconductor-dielectric interfaces²⁹.

In this work the SAM hexamethyldisilazane (HMDS) was used to help pattern the semiconducting layer within some devices. HMDS dissociates and bonds with the silicon dioxide (SiO_2) surface, decreasing the wettability of the surface with water.³⁰ By applying it to the entire surface of a substrate and then selectively removing it from chosen areas, it is possible to control where the precursor solution wets the substrate as demonstrated in **Figure 2.2**.

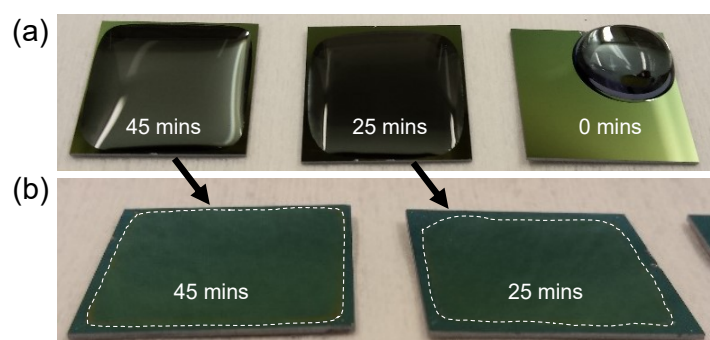


Figure 2.2: SiO_2 substrates exposed to HMDS with the SAM removed from the center by UV-Ozone cleaning, leaving a thin border of HMDS around the edge. Images show (a) the wetting of water on the HMDS and SiO_2 surface that have been UV-Ozoned for 45, 25 and 0 mins (from left to right). (b) The In_2O_3 films deposited from an indium nitrate hydrate and deionized water solution, with the area of deposition highlighted by white dashed lines.

Substrates were patterned using the following method. First 1 ml of HMDS solution was placed into a closed petri dish with samples raised from the base of the dish. The petri dish was then heated to 80 °C for 20 mins, allowing for vapour phase deposition and the HMDS to dissociate, releasing ammonia and depositing hydrogenated carbon on to the SiO_2 surface.³⁰ Next the samples were rinsed in IPA and dried to remove any excess surfactants or HMDS. The samples were then placed into a holder, with a shadow mask placed on top to cover areas of the substrate where a SAM layer was desired. The masked samples were then exposed within a UV-Ozone cleaner for 45–60 mins. The reactive ozone removes the hydrogenated carbon from the unmasked areas, leaving cleaned SiO_2 and improving the substrates' hydrophilic nature. By immediately spin-casting after this process the deposited film is contained within the unmasked area as demonstrated in **Figure 2.2**. This simple technique is excellent for reducing the gate current leakage seen in some devices where the semiconductor seeps over the edge of the gate dielectric, making contact with the gate.

It is important to realise that this method is only useful for broad scale patterning where features are larger than 2 mm. This limitation is due to the imprecision caused by using a UV-Ozone cleaner to remove unwanted SAM. Another issue specific to spin-casting, is that the edges of the substrate cause an uneven profile in the solution thickness. The presence of the SAM causes similar issues leading to an accumulation of solution next to the SAM covered area during the spin-casting process.

2.1.4 Dye-Functionalization

Dye-functionalization is the process of modifying a surface by attaching an optically active molecule that also electronically interacts with the device. If the dye forms a monolayer bonded to the surface via chemisorption, it may be considered a form of SAM. Within this work the small molecule organic dye D102 (shown in **Figure 2.3**) was used to modify the surface of the semiconductor In_2O_3 producing phototransistors as reported in Chapter 5.

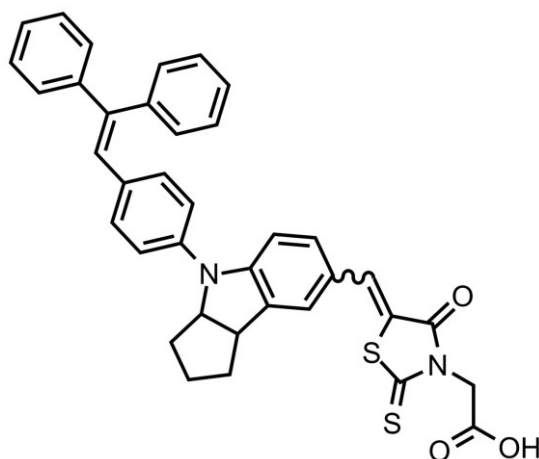


Figure 2.3: Chemical structure of the small organic molecular dye D102 used within this work to produce dye-sensitized phototransistors.

D102 is an indoline dye mainly used in the field of dye-sensitized solar cells (DSSCs) ^{31,32} that has a peak in absorption at ~ 500 nm giving it an orange colour in solution ³³. The head group of the molecule is a carboxylic acid that allows it to bond to the surface of most metal oxides in one of multiple configurations as shown in **Figure 2.4**.³⁴

To functionalize the surface the following process was employed. Devices were submerged for one minute in a 0.8 mM solution of D102 in a 50:50 vol % mixture of acetonitrile and tert-butanol. Excess solution was then rinsed off with deionized water and the samples were dried with nitrogen. The dye bonds rapidly to the surface (on the scale of a few

seconds/minutes), so very short immersion of 1 min was used to minimize the possibility of solvent damage to the semiconductor surface. In addition, although rinsing the devices with water removed any excess solution from the surface, it cannot ensure that the devices will be left with only a monolayer of D102.

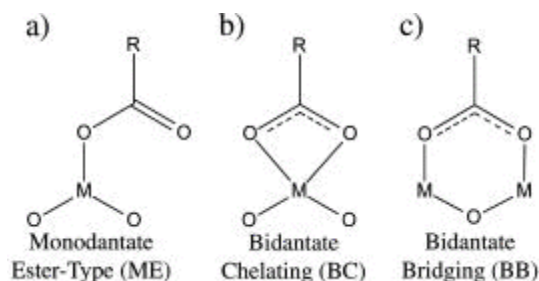


Figure 2.4: Examples of three possible bonding mechanisms of carboxylic acids on metal oxide surfaces. (Adapted and reprinted with permission from Moreira et al.³⁴. Copyright 2009, American Institute of Physics.)

2.1.5 Thermal Evaporation

Aluminium, deposited via thermal evaporation, was the predominant metal used for contacts in this work. Thermal evaporation uses a boat with high current flowing through to heat a small crucible of the source material. The crucible acts to direct the evaporated material towards the substrates. In addition, shadow masks may be placed between the source and substrate to pattern the deposited thin film of metal. The rate of evaporation is controlled by the current flowing through the boat using a proportional, integral, and differential (PID) controller.

When evaporating metals, the rate used is measured as the thickness of material deposited in Ångströms per second (Å/s), with common rates being between 0.5-5 Å/s. The rate of evaporation controls the roughness and crystal size of the films being produced as discussed in Section 6.2.1.³⁵

Contacts used for the work in this thesis were deposited using a Kurt J. Lesker evaporator pumped down to a vacuum of 5×10^{-6} mBar. When depositing contacts as the final layer of a device an evaporation rate between 0.5-2 Å/s was used. A precise rate was not required as the smoothness of the interface was controlled by the penultimate layer. Fast evaporation rates produced smoother films, hence for bottom gate contacts for TFTs or diodes, an evaporation rate of 3 Å/s was used. This is justified in Section 6.2.1 and ensured a smoother interface with subsequently deposited layers.

2.2 Optical Characterisation

2.2.1 UV-Vis Spectroscopy

UV-Vis spectroscopy is a technique that can be used to measure the transmission, reflection and absorption of light by a sample. Depending on the equipment set up, it can be used on thin films, powders and even liquids. The transmission measurement is the simplest to perform on transparent films, measuring the amount of light transmitted as a fraction of the incident light. Often plotted instead of transmittance is the partial misnomer “absorbance”. In simple UV-Vis spectroscopy where sample reflectance is minimal, the absorbance $A(\lambda) = 1 - T(\lambda)$ where T is the transmission of the sample.

Within this work, a Shimadzu 2600 spectrophotometer was used. The UV-Vis spectrometer contains both a halogen and deuterium light source that passes through a monochromator to emit a beam spread over a very short spectral range. The beam passes through the sample holder into an R-928 photomultiplier acting as a detector. An initial calibration scan is performed after the two light sources have heated up and stabilized in both frequency and power (which takes ~ 30 mins). The calibration is performed before the sample is placed into the holder. After calibration, the sample may be placed in the holder and a measurement taken of the transmission. The Shimadzu 2600 can measure frequencies between 220 nm and 900 nm, with the ability to measure up to 1400 nm using the accompanying integrating sphere attachment.

2.2.2 Electroluminescent Spectroscopy

Electroluminescent (EL) spectroscopy is the act of measuring the optical output of a device, specifically looking at the intensity as a function of wavelength. In this work EL spectroscopy was only used to measure the output of light emitting diodes (LEDs) used in an optoelectronic measurement setup. Since the emission spectra of an LED is a single sharp peak, even an uncalibrated detector can be used to determine the peak wavelength.

An Ocean Optics Optical Transmittance Spectrophotometer (with a range of 380 to 780 nm) was used to measure the output of three LEDs (red, green and blue) used in the optoelectronic measurement describe in Section 2.4.2. Each LED was placed over the photodetector in turn and covered to reduce external light. A current of 10 mA was applied to

the LED while the transmission software was run with the lamp used for transmission measurement left off. The resultant transmission spectra acts as an accurate EL spectrum for the LEDs as justified earlier.

2.3 Surface Characterisation

Within TFTs and diodes, the most important areas of the devices are always the interfaces. It is therefore vital to understand the formation of these interfaces and how they affect device performance.

2.3.1 Atomic Force Microscopy

Atomic force microscopy (AFM) is an imaging technique that uses the interaction between an ultra-sharp AFM tip and sample to provide a topological image of the sample surface. The setup consists of a sharp tip with a tip radius of the order of nanometres mounted on a cantilever. The cantilever can be moved in all three directions by providing fine control of the tip's position from the surface of the sample. A laser directed onto the rear of the tip is reflected into a sensor, which measures the deflection of the tip.

The simplest mode of operation for AFM is the contact mode. In this case, a piezo control attempts to maintain a constant distance from the sample surface as an X and Y raster scan is performed. This technique wears the tip out quickly and suffers from picking up material off the sample surface. A more accurate method is alternate current AFM (AC-AFM), also known as tapping mode AFM or intermittent contact mode. In AC-AFM, a small piezo oscillator in the cantilever holder induces an oscillation in the tip. This reduces the time spent in contact with the surface and decreases the likelihood of picking up material, slowing down the wearing of the tip. The AC-AFM technique is also better suited for soft materials such as polymers, due to the decreased force on the sample when compared to contact mode AFM.

In this work, an Agilent AFM 5500 was used along with an N9534B AC-AFM nose-cone. The system was mounted in a vibration dampening enclosure and operated in standard atmosphere. Image processing was then performed using the GNU General Public License software Gwyddion.

2.3.2 Transmission Electron Microscopy

Transmission electron microscopy (TEM) is an imaging method that uses a focused beam of electrons passing through a thin layer of sample to image its structure. The short De Broglie wavelength of the electrons involved allows for detailed images with atomic precision. The specimen being studied via TEM must be extremely thin, preferably $< 1 \mu\text{m}$, to allow for transmission of electrons and avoid full absorption of the beam. Full absorption of the beam will lead to image saturation. Therefore, preparation of the samples is a vital part of the experimental procedure.

The high-resolution TEM images shown in this work were produced at King Abdullah's University of Science and Technology (KAUST) by Dr. Kui Zhao and Prof. Aram Amassian. Samples were prepared using focused ion beam (a Helios 400s) with a nanomanipulator using a lift-out method. The images were subsequently taken with a Titan 80-300 Super Twin microscope operating at 300 kV with a US1000 charged couple device (CCD) as the camera.

2.3.3 Ellipsometry

Many methods exist for measuring the thickness of a thin film, but their applicability is dependent on the thickness and structure of the film. For thick films ($> 100 \text{ nm}$) where part of the layer has been physically removed, leaving a defined step between the film and substrate, a profilometer is sufficient to measure thickness. For films of less than 100 nm and below the vertical measurement resolution of a profilometer, then an AFM may be used. Both these techniques require selectively etching or depositing the film to produce a step between the film and substrate, although it is not always a simple process. For films that are highly resistant to etching, such as the dielectric layers reported within this work, a third technique of ellipsometry is ideal.

Ellipsometry measures the complex refractive index of multiple stacked layers of thin films as a function of wavelength and incident angle. It can also be used to ascertain various film parameters including: thickness, roughness, and complex refractive index of the component layers of a film. The setup consists of a beam of polarized light that is reflected off the surface of the sample into an analyser consisting of a second polarizer and a detector. The angle of incidence chosen for the measurement is close to the Brewster angle of the sample to maximize the difference between the reflected polarized light (p-polarized) and the light polarized at 90°

(s-polarized) to the original plane of polarization. The ellipsometer then measures the p-polarized and s-polarized light over a range of wavelengths, repeating the measurements at multiple angles.³⁶

Ellipsometry does not give a direct result for the optical constants of the materials involved, or for the thickness of the layers of each material. Instead, a model of the system must be produced, starting by inserting all known information about each layer. Next estimates for unknown parameters are entered as a starting point for the subsequent optimization. A large database of optical constants for different materials exist, along with simple models than can be used to approximate most materials. For each layer one of these must be selected and an appropriate thickness entered. After this initial model has been created the software will simulate the expected output for the previously performed experiment. The software then uses an iterative (normally a least-square minimization) procedure to maximize the fit between experimental results and simulation results, varying only the model parameters selected by the user. Within this work a Woolam VASE ellipsometer was used followed by modelling and analyses using Woolam's WVASE analysis software with the aid of Dr. Ivan Isakov.

2.4 Electrical Characterisation

2.4.1 Thin Film Transistor Measurements

Thin film transistors (TFTs) are three contact electrical devices in which a gate contact controls the flow of current between source/drain contacts. Although TFTs have three contacts, only two source measure units (SMUs) are required to characterise the device, since the source acts as a common ground for both gate and drain. Connecting the source to a ground or a virtual ground also provides stability to the measurements. The applied voltage and subsequent current between the source and drain are usually identified as the drain voltage (V_D) and drain current (I_D) respectively. Similarly, the voltage and total current between the source, channel, and drain and gate are the gate voltage (V_G) and gate (or gate leakage) current (I_G). An example experimental setup of a TFT has been included in **Figure 2.5**. In an ideal TFT the dielectric is assumed to be perfect. This would lead to a gate current of zero, but in reality this is not the case and non-zero values of I_G are found.

Two types of TFT measurement can be performed. The first is transfer characterisation, where V_D is held constant while V_G is swept across a range of voltages. V_G was varied using a linear double sweep from the off-state to the on-state and back for each TFT. This means V_G was initially increased in the positive direction for an N-type semiconductor and in the negative direction for a P-type semiconductor. The linear double sweep consists of equally spaced points using a linear scale from the initial to the final value of V_G , these values are then repeated in reverse order till the sweep returns to the initial V_G again. The speed of the sweep was controlled by the SMU which automatically chooses a scan rate dependent on the magnitude of current being measured. Through this the experimental noise could reach 10^{-11} A. Any difference between forward and reverse scans is an indication of one of multiple issues, but normally attributed to traps in the semiconductor or traps in the semiconductor-dielectric interface. The measurement is repeated at two drain voltages, one measuring the response in the linear regime of the device the second measuring response in the saturation regime (the two regimes are described in Section 3.1.1).

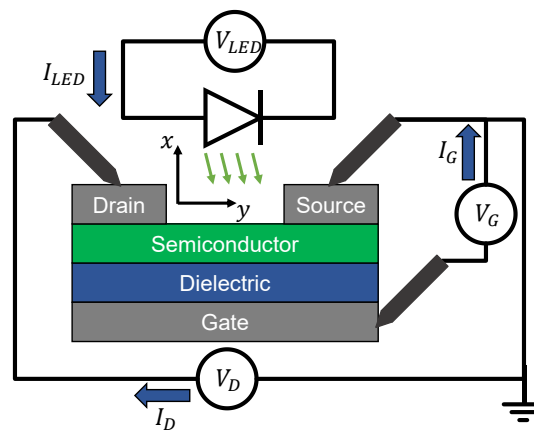


Figure 2.5: Experimental setup for measuring TFTs and phototransistors. Note that the LED is not used within standard TFT measurements, only during optoelectronic characterisation. Also included are the defined x and y directions used in calculations.

The second TFT measurement commonly performed is output characterisation. For this measurement, the gate voltage is held constant while a linear double sweep is performed on the drain voltage. The measurement is repeated for multiple gate voltages using a similar range for both the drain voltage and gate voltage used within transfer characterisation. From the output curves, it is possible to see at what drain voltage the transistor is in linear and saturation regimes, which aids in applying the correct mobility calculation equation to the transfer characteristics.

Within this work, samples were mounted on a PTFE chuck and micromanipulators were used to make contact between the TFTs and the tungsten needles used. TFT measurements were performed in nitrogen using an Agilent B2902A dual SMU at room temperature (unless stated otherwise). Output curves provided little extra visual information, so were omitted from the relevant sections. The high ratio of width to length (at least $W = 1000 \mu\text{m}$ to $L = 50 \mu\text{m}$) of the transistors reduced edge effects and possible parasitic currents. Gate leakage current was measured as part of the experimental setup to ensure correct assessment of the cause of each off-current and document parasitic leakage through the dielectric. Aluminium was used as the source/drain contacts, for devices produced with In_2O_3 as the semiconductor, as it is known to produce an ohmic contact.^{22,25} This ohmic contact is confirmed by the flat response in linear mobility extraction (the calculation is described in Section 3.1.2) at higher applied gate voltages for two In_2O_3 based devices on different dielectrics produced with aluminium source/drain contacts (as shown in **Figure 2.6**).

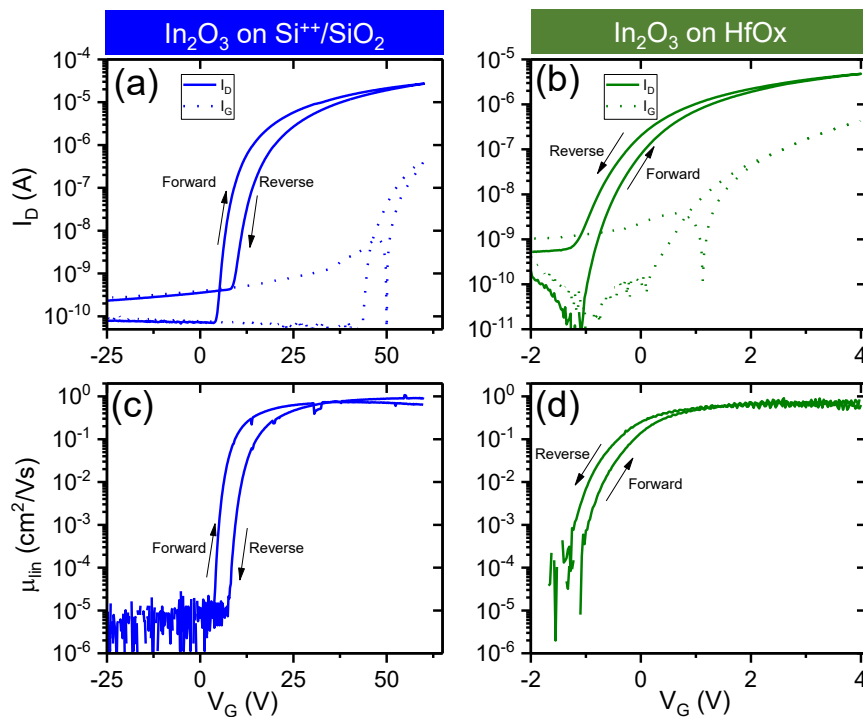


Figure 2.6: Example transfer characteristics (a),(b) and linear mobility (c),(d) against gate voltage plots for In_2O_3 transistors with aluminium source/drain contacts produced on a $\text{Si}^{++}/\text{SiO}_2$ wafer (a),(c) and a hafnium oxide solution processed dielectric (b),(d).

For the In_2O_3 dye-sensitized phototransistors of Chapter 5, HMDS patterning (as described in Section 2.1.3) was used to stop the In_2O_3 depositing over the edge of the SiO_2 dielectric and contacting the gate. This acted to reduce gate leakage within these devices. The

TFTs fabricated with solution processed dielectrics, as reported in Chapter 6, used patterned gate contacts which did not overlap with the pads used to connect to the source/drain contacts to reduce gate leakage.

2.4.2 Optoelectronic Measurements

Optoelectronic measurements are usually made on two terminal devices, such as solar cells or photodiodes. For these devices, there are three parameters: the applied voltage, illuminating light wavelength, and illuminating light intensity. In this thesis, only phototransistors were produced, which are three terminal devices. Phototransistors conceptually have most in common with a photoconductor with a gate contact used to modify its optoelectronic properties. The gate contact adds an extra parameter to control; therefore, a method of measuring the phototransistor using transfer characterisation from Section 2.4.1 was adopted.

To measure the optoelectronic properties of a phototransistor, the device was mounted on a probe station in a nitrogen environment at room temperature with the electrical setup shown in **Figure 2.5**. A set of three LEDs (red, green and blue) were fixed above the phototransistor and the setup was shrouded from external light sources. First, a transfer characteristic measurement was taken in darkness as outlined in Section 2.4.1, which is necessary to calculate both the responsivity and photosensitivity of the device. Next, a single LED was selected and a fixed current set through it using a Keithely 2400 source meter, causing the LED to emit light. The electrical response of the phototransistor was allowed to stabilize, and another transfer characteristic was then performed. The LED current was increased (resulting in higher light intensity), and the process repeated five more times. The same measurement was repeated till the response to all three LEDs was complete.

The EL spectrum of the three LEDs used was measured as outlined in Section 2.2.2 with peak wavelengths of 630 nm, 522 nm and 470 nm in turn for the red, green and blue LEDs. The light intensity of the LEDs was measured by fixing them above a Gentec-eo XLP12-3S-H2 calibrated thermopile.

3 Theory

Thin film transistors (TFTs) were described as a device created by the “evaporation of all components on to an insulating substrate”³⁷ in 1962. It would now be more accurate to describe it “as a transistor produced by the sequential deposition of the component layers”, especially when doped silicon is a highly popular gate contact and substrate (especially for research purposes). The first section of this chapter covers the square law model for TFTs along with possible modifications in response to non-ideal behaviour. The second section describes how to theoretically calculate the charge accumulation in a metal-insulator-semiconductor (MIS) capacitor. The third section compares three potential descriptions of charge transport: band transport, hopping transport and multiple trapping and release (MTR). While the final fourth section describes the effect of trap states within the bandgap on charge transport within a MTR model.

3.1 Square Law Model

The square law model is the simplest description of a TFT referenced to from 1964 by Paul K. Weimer³⁸ with earlier inaccessible references from the previous year³⁹. The model states that the current between the source and drain of a TFT (as shown in **Figure 2.5**) is controlled by the number of charge carriers induced into the channel by the gate voltage. Multiple approximations are required within this model which are listed below.

1. Drift is the predominant cause of current within the device and limited to movement in the y direction, where the y direction is defined as the direction between source and drain contacts. The assumption here is that diffusion and leakage currents are negligible.
2. The channel potential varies more slowly along the channel direction than across the channel; thus a two-dimensional problem is reduced to one-dimension.
3. There are no trap states within the material or at the interface.
4. The model is limited to work only when the gate voltage is greater than the threshold voltage and the drain voltage is less than the gate voltage. It can be applied to both the inversion and accumulation regimes, but not the depletion regime.

The number of charge carriers in the channel ($n(y)$) at the specific position y between the source and drain (where the source is positioned at $y = 0$ and the drain at $y = L$) is:

$$n(y) = \frac{C_{ins}}{q} (V_G - V_{Th} - V(y)) \quad (1)$$

where C_{ins} is the specific capacitance of the insulator in F/m² (leading to units of m⁻² for $n(y)$), and V_G, V_{Th} are the gate voltage, and threshold voltage in turn, finally $V(y)$ is the applied drain voltage at position y in the channel. Experimentally the threshold voltage is defined as the voltage that must be applied to the gate to remove all charge carriers, and this can be extracted experimentally, as will be detailed later. The drift current between the source and drain is:

$$I_D = -qWn(y)\mu_{SC} \frac{dV(y)}{dy} \quad (2)$$

where q is the elementary charge and μ_{SC} is the field effect mobility of the semiconductor. By inserting Equation (1) into Equation (2), separating variables of $V(y)$ and y , and integrating over both sides the following equation is produced:

$$I_D \int_0^L dy = -WC_{ins}\mu_{SC} \int_0^L (V_G - V_{Th} - V(y))dV(y) \quad (3)$$

which can be solved giving:

$$I_D L = WC_{ins}\mu_{SC} \left[(V_G - V_{Th})V(y) - \frac{1}{2}(V(y))^2 \right]_{V(0)}^{V(L)}. \quad (4)$$

Since this lateral voltage in the y direction is known at the points $V(L) = V_G - V_{Th} - V_D$ and $V(0) = V_G - V_{Th}$, this can be reinserted to produce:

$$I_D = \frac{WC_{ins}\mu_{SC}}{L} \left[(V_G - V_{Th})V_D - \frac{V_D^2}{2} \right]. \quad (5)$$

This is the square law equation for the drain current.

3.1.1 Linear and Saturation Regimes

TFT operation consists of two main regimes, most easily identified from the output characteristics. The first is the linear regime where $V_D \ll V_G - V_{Th}$. If this condition is met, then the term V_D^2 in Equation (5) is negligible, and hence Equation (5) can be approximated as:

$$I_{D,lin} = \frac{WC_{ins}\mu_{lin}}{L} (V_G - V_{Th})V_D \quad (6)$$

where μ_{lin} is the mobility of the device when measured in the linear regime.

As V_D is increased, the square-law model in Equation (5) will eventually reach a point at which the current starts to decrease with increasing V_D which is unphysical. This breakdown

occurs when $V_D = V_G - V_{Th}$, indicating when the channel voltage at the drain no longer accumulates charge. This leads to a pinch off of the channel at the drain that moves towards the source with increasing V_D . As long as the drain is not increased enough to cause an inversion region around it, the maximum potential difference across the channel is $V_G - V_{Th}$, hence one of limits of Equation (4) at the drain changes to $V(L) = 0$. This can also be described as saying that the drain voltage does not change the current after $V_D = V_G - V_{Th}$, such that V_D in Equation (5) can be replaced with the gate voltage minus the threshold voltage. Both descriptions simplify Equation (5) to:

$$I_{D,sat} = \frac{WC_{ins}\mu_{sat}}{2L} (V_G - V_{Th})^2 \quad (7)$$

where μ_{sat} is the mobility of the device in this saturation regime.

3.1.2 Field-Effect Transistor Mobility

The field-effect transistor (FET) mobility is a commonly used figure of merit for semiconducting materials. It is one of multiple ways⁴⁰ to calculate the mobility of charge carriers through a material along with time of flight measurements (TOF)⁴¹ and Hall effect measurements^{42,43}. As described in Section 3.1.2, there are two regimes of operation for a TFT, the linear and saturation regime. Each of these has a mobility related to it, often dealt with as two separate entities leading to two different experimental values of mobility.

To calculate mobility from an experimental transfer characteristics in the linear regime it would be ideal to remove the threshold voltage dependence of Equation (6). This can be achieved simply by differentiating the drain current with respect to gate voltage leaving:

$$\frac{dI_{D,lin}}{dV_G} = \frac{WC_{ins}\mu_{lin}}{L} V_D \quad (8)$$

which can be rearranged to give an expression to calculate the linear field-effect mobility:

$$\mu_{lin} = \frac{L}{WC_{ins}V_D} \frac{dI_{D,lin}}{dV_G}. \quad (9)$$

To calculate a value for charge mobility from a transfer characteristics in the saturation regime, we must also remove the threshold dependence of Equation (7). There are two specific methods for doing this. The first is to square root both sides of Equation (7) and then differentiate with respect to V_G to give:

$$\frac{d\sqrt{I_{D,sat}}}{dV_G} = \sqrt{\frac{WC_{ins}\mu_{sat}}{2L}} \quad (10)$$

which may then be rearranged to give:

$$\mu_{sat} = \frac{2L}{WC_{ins}} \left(\frac{d\sqrt{I_{D,sat}}}{dV_G} \right)^2 \quad (11)$$

The second technique is to take a double derivative of Equation (7) in terms of V_G such that:

$$\frac{d^2 I_{D,sat}}{dV_G^2} = \frac{WC_{ins}\mu_{sat}}{L} \quad (12)$$

and hence the saturation mobility can be calculated from:

$$\mu_{sat} = \frac{L}{WC_{ins}} \frac{d^2 I_{D,sat}}{dV_G^2} \quad (13)$$

The fact that the mobility measurements requires a derivative of drain current with respect to gate voltage means that they may only be performed on transfer characteristics data. At the same time the output characteristics is required to ensure that the transfer characteristics are within the correct regime for each applied drain voltage.

Within this thesis, mobilities for devices were extracted using a single MATLAB GUI. The GUI first calculates the linear and saturation mobilities as a function of the applied gate voltage using Equations (9) and (11) respectively. Next the top 20%, of the data points from each set were selected and averaged to calculate a final value of linear and saturation mobility. User input could increase this averaging fraction to better fit data with greater noise, or extraneous points.

3.1.3 Constant Contact Resistance

The square law model is the most basic available model, and hence many attempts to improve and expand on it have been made. Each of these attempts have often been motivated by issues specific to certain device structures, or material combinations. The first most common modification made to the model is to include a contact resistance between the source/drain contacts and the semiconductor. This is an especially common inclusion for mobility extraction from organic transistors where injection of holes into the very deep highest occupied molecular orbital (HOMO) can be hard to achieve.⁴⁴⁻⁴⁷

The simplest way to include contact resistance is to follow the procedure outlined by Braga and Horowitz²⁹. In it, they propose that the contact resistance R_C can be thought of as an

independent resistance in series with the channel. The voltage dropped across the channel is therefore reduced by $R_C I_D$, which is the voltage dropped over the total contact resistance. This means that V_D in Equation (6) should be replaced with $V_D - R_C I_D$ to give:

$$I_{D,lin} = \frac{WC_{ins}\mu_{lin}}{L} (V_G - V_{Th})(V_D - R_C I_{D,lin}) \quad (14)$$

which can be rearranged to:

$$I_{D,lin} = \frac{V_D}{R_C + \frac{L}{WC_{ins}\mu_{lin}(V_G - V_{Th})}}. \quad (15)$$

This function may then be fitted to experimental data to provide solutions for the mobility, threshold voltage and contact resistance.

This description is logically flawed though, as it assumes that the contact resistance exists only on the drain contact. It therefore assumes voltage is only dropped across the drain contact, and not across the drain and source. A further extension to this model can be found in the paper by M. M. Ibrahim et al.⁴⁸, in which they show how a more accurate mobility can be calculated assuming an equal potential drop across both the source and drain. This will result in a value for $V(0)$ in Equation (4) that isn't $V(0) = V_G - V_{Th}$, but instead includes the resistance of the source contact (R_S).

3.1.4 Gate Dependent Contact Resistance

The idea that the contact resistance of a device would be constant with gate voltage is arbitrary for all situations. Uemura et al.⁴⁹ highlighted this fact with devices based on the organic semiconductor C10DNTT. They defined a new value called the apparent mobility μ_{app} as the calculated result when extracting mobility using Equation (6) and an intrinsic mobility μ_0 (or μ_{int}) that is the true mobility of charge carriers through the semiconductor after confounding factors have been removed. Rearrangement of Equation (15) produces a relationship between the intrinsic and apparent mobility of:

$$\mu_{app} = \mu_0 \frac{1}{1 + \frac{R_C(V_G)WC_{ins}\mu_0(V_G - V_{Th})}{L}} \quad (16)$$

which shows that contact resistance should be more prevalent within short channel length devices. They measured μ_0 using the gated four-point-probe (gFPP) technique and μ_{app} using standard transconductance mobility extraction, and from this solved Equation (16) to get $R_C(V_G)$.

From this, they exhibited a gate dependence in the contact resistance for their specific devices, where the contact resistance decreases the apparent mobility compared to the intrinsic mobility.

Uemura et al.⁴⁹ also highlighted how there are cases where there are localised spikes where $\mu_{app}(V_G) > \mu_0$. This was unexpected as it was generally thought that contact resistance should only decrease the apparent mobility. Their explanation for this discusses the effect in terms of transconductance, and states that if the change of the contact resistance with gate voltage is large enough, the apparent mobility can become greater than the intrinsic mobility. The following calculations provide a secondary route to prove the validity of Uemura et al.'s argument.

First, for simplicity a value of $V'_G = V_G - V_{Th}$ is defined, this is equivalent to assuming that the threshold voltage of the device is at zero volts. By inserting this into Equation (14) we get:

$$I_D(V'_G) = \frac{WC_{ins}\mu_0}{L} V'_G (V_D - R_C(V'_G) I_D(V'_G)) \quad (17)$$

where it has been assumed that that contact resistance is an unknown function of gate voltage, but the intrinsic mobility is not. For the rest of this derivation the gate voltage dependence of $R_C(V'_G)$ and $I_D(V'_G)$ will not be explicitly shown, and the variables will be replaced with R_C and I_D respectively. By differentiating $I_D(V'_G)$ with respect to V_G , the following relation is produced:

$$\frac{dI_D}{dV'_G} = \frac{WC_{ins}\mu_0}{L} V_D - \frac{WC_{ins}\mu_0}{L} \left[R_C I_D + V'_G R_C \frac{dI_D}{dV'_G} + V'_G I_D \frac{dR_C}{dV'_G} \right] \quad (18)$$

which rearranges to:

$$\frac{1}{\mu_0} = \frac{WC_{ins}}{L} \left(\frac{dI_D}{dV'_G} \right)^{-1} V_D - \frac{WC_{ins}}{L} \left(\frac{dI_D}{dV'_G} \right)^{-1} \left[R_C I_D + V'_G R_C \frac{dI_D}{dV'_G} + V'_G I_D \frac{dR_C}{dV'_G} \right] \quad (19)$$

where the first term on the right hand side is equal to the inverse apparent mobility from Equation (9). Hence, it may be rewritten as:

$$\mu_{app} = \frac{\mu_0}{1 + \mu_0 A(V'_G)} \quad (20)$$

where:

$$A(V'_G) = \frac{WC_{ins}}{L} \left(\frac{dI_D}{dV'_G} \right)^{-1} \left[R_C I_D + V'_G R_C \frac{dI_D}{dV'_G} + V'_G I_D \frac{dR_C}{dV'_G} \right]. \quad (21)$$

From Equation (21) it is obvious that for $\mu_{app} \geq \mu_0$ we require that $\mu_0 A(V'_G) \leq 0$. There is also a secondary condition that $\mu_0 A(V'_G) > -1$ otherwise μ_{app} will become negative, but this in general can be ignored. From the condition that $\mu_0 A(V'_G) \leq 0$ the following may be calculated:

$$\frac{\mu_0 W C_{ins}}{L} \left(\frac{dI_D}{dV'_G} \right)^{-1} \left[R_C I_D + V'_G R_C \frac{dI_D}{dV'_G} + V'_G I_D \frac{dR_C}{dV'_G} \right] < 0 \quad (22)$$

which simplifies to:

$$\frac{1}{V'_G} + \frac{d \ln(I_D)}{dV'_G} + \frac{d \ln(R_C)}{dV'_G} < 0. \quad (23)$$

From Equation (23), we can examine the criteria for a localised spike in the apparent mobility. So far the calculations have assumed an N-type device, and in such a device the first two terms on the left-hand side of Equation (23) are always positive, so only $d \ln(R_D) / dV'_G$ can produce a negative value. If the decrease in contact resistance outmatches the increase in drain current and the inverse gate voltage, it is possible that there will be a spike in the apparent mobility above that of the intrinsic mobility. In a paper by Uemura et al.⁴⁹ discussing this issue, one device exhibited a negative change in contact resistance of 10^5 over a range of 15 volts. This massive change in contact resistance over a short voltage range could easily outmatch the change in the drain current. Looking at the supplementary information of the same work⁴⁹ it becomes obvious that the biggest spikes in the apparent mobility always occur when the differential of the drain current with respect to gate voltage decreases, further supporting this hypothesis.

The In_2O_3 semiconductor most commonly used in this work produces ohmic contacts with aluminium as discussed in Section 2.4.1. Hence this model, and the need to account for contact resistance was not required for the experimental work in this thesis. The inclusion of this discussion is due to observations of gate voltage localised peaks in mobility by collaborators and this highlights a possible cause with a firm theoretical backing.

3.1.5 Geometric Effects on Contact Resistance

A further expansion to contact resistance has been outlined by Marinkovic et al.⁵⁰, introducing the effect that contact geometry has on contact resistance. Using a resistive network model, they demonstrated that for a source/drain contact of width W and contact length L_C (not

to be confused with L defined as the length between source and drain), then the contact resistance is:

$$R_C = \frac{\sqrt{\rho_C R_{Sh}}}{W} \coth\left(\frac{L_C}{L_T}\right) \quad (24)$$

where ρ_C is the specific (per unit area) contact resistance, R_{Sh} is the sheet resistance of the semiconductor and L_T is the transfer length.

The transfer length is the critical area over which the majority of charge is injected, and defined by:

$$L_T = \sqrt{\frac{\rho_C}{R_{Sh}}}. \quad (25)$$

By assuming the electrode length is larger than the transfer length Equation (24) simplifies to:

$$R_C = \frac{\rho_C}{WL_T}. \quad (26)$$

Within the referenced paper, a thermionic emission of charge carrier model was cited as the main source of contact resistance.⁵⁰

3.1.6 Non-linear Mobility Extraction

The square law model, ignoring contact resistance, assumes a value of mobility independent of voltage. Multiple causes can create a non-linear relationship between the gate voltage and drain current including an exponential set of localised trap states below the conduction band.^{51,52} Because of this a new linear current has been proposed⁵³⁻⁵⁵ of the form:

$$I_{D,lin} = \frac{WC_{ins}\mu_{lin}}{L} (V_G - V_{Th})^\gamma V_D \quad (27)$$

where γ is an experimental constant that indicates the deviation from a linear response for the device. This is an empirically applied solution though, with no specified mathematical cause for the power law invoked.

From Equation (27) a relationship between the apparent mobility as a function of gate voltage ($\mu_{app}(V_G)$), and the maximum intrinsic mobility (μ_{int}) can be derived as:

$$\mu_{app}(V_G) = \mu_{int}(V_G - V_{Th})^{\gamma-1}. \quad (28)$$

where the values of μ_{int} & γ are found by fitting the curve to experimental data of $\mu_{app}(V_G)$ calculated from Equation (9). When applied to disordered semiconductors, the value of γ can

describe the relationship between the measurement temperature (T) and the equivalent energetic temperature (T_0) of the localised states within the semiconductor^{56,57}:

$$\gamma = \frac{2T_0}{T} - 1. \quad (29)$$

By converting T_0 into units of electron volts, it can be used to roughly approximate the average depth of trap states within a TFT.

3.1.7 Other Modifications to the Square Law Model

Multiple other modifications to the square law model have been studied. Some start by defining new figures of merit that highlight a specific form of mobility. One example of this is reported by R. Hoffman⁵⁸, in which he introduces an equation to calculate the mobility of just the induced charge into the channel due to an incremental increase of gate voltage. The last modification that shall be mentioned briefly was reported by Ryu et al.⁵⁹. In their report they described a method of directly measuring the capacitance of a TFT as a function of its applied gate voltage. Using this varied capacitance in mobility calculation will lead to more accurate results for devices whose capacitance has a large gate dependence on.^{60,61}

3.2 Charge Distribution in Semiconductors

Knowing the distribution of charge carriers within a semiconductor, especially within the metal insulator semiconductor (MIS) device, is key to understanding the operation of any TFT. This section shall outline the possible assumptions and solutions that may be used, and is adapted from the work of S. Skinner⁶². Appendix A contains full derivations for each part of this section. The directions x and y are visually shown in **Figure 2.5**, while z is logically deducible. The first key assumptions that must be made for all potential charge depth solutions are as follows.

1. The semiconducting material being examined is N-type, and hence only electron movement shall be considered.
2. There is uniformity and homogeneity in the metal, insulator and semiconductor in both the y and z directions.
3. The system is in equilibrium within the x direction, explicitly this means there is no current flow perpendicular to the interface plane.
4. There is no movement of charge through the insulator.

Along with this list of constant assumptions, there are two more optional assumptions that may be made and will be discussed in subsections below.

A. Thick Film Approximation (TFA)

Within this approximation, it is assumed that the thickness of the semiconductor is enough that the electrical field at the semiconductor surface tends to zero smoothly.

B. Voltage Drop Approximation (VDA)

Within this approximation, it is assumed that all the gate voltage is dropped across the insulator.

3.2.1 Drift and Diffusion Currents

In the semiconducting layer there are two main types of current, the drift current and diffusion current. The current density in the x direction can therefore be expressed as:

$$j(x) = q \left(\mu_n n(x) F(x) + D_n \frac{dn(x)}{dx} \right) \quad (30)$$

where $n(x)$ is the carrier density, q is the elementary charge, μ_n is the mobility of the electrons and D_n is the diffusion coefficient. One of the key assumptions made is that the system is in equilibrium in the x direction; hence, the total current in the x direction must also be zero across all space. Starting from Equation (30) and using the condition $j(x) = 0$, Gauss' law and Einstein's relation ($D_n/\mu_n = k_B T/q$), the following differential relation may be produced:

$$\frac{1}{2} \frac{dF^2(x)}{dx} = - \frac{k_B T}{q} \frac{d^2 F(x)}{dx^2} \quad (31)$$

where k_B is the Boltzmann constant, T is the temperature and q is the value of elementary charge.

By integrating both sides of Equation (31), an initial differential equation may be produced:

$$\frac{2k_B T}{q} \frac{dF(x)}{dx} + F^2(x) = - \left(\frac{2k_B T}{q} \right)^2 g^2 \quad (32)$$

where g is introduced as a constant of integration using the convention set by S. Skinner⁶². The value of g is determined by the boundary conditions imposed upon the system, and can be removed altogether by applying the thick film approximation.

3.2.2 Thick Film Approximation (TFA) and Solution

A common approximation made when solving Equation (32) is the thick film approximation (TFA). It states that the film is thick enough that the electric field will smoothly tend to zero at the surface of the semiconductor. Mathematically this means that both the electric field and the derivative of the electric field will be zero at the semiconductor surface. This can be inserted into Equation (32) to trivially prove that under these conditions $g = 0$.

If $g = 0$ the solution to Equation (32) is simply:

$$F(x) = \frac{2k_B T}{q} \frac{1}{x + \frac{2k_B T}{qF_0}} \quad (33)$$

where the electric field at the insulator semiconductor interface is $F(x = 0) = F_0$. It is important to note here that due to the TFA, $F(x)$ will only equal zero when $x = \infty$. Any simulation produced with this equation will lead to non-zero values of electric field at the semiconductor surface. It is also worth noting that the function of electric field is defined solely by the electric field at the insulator semiconductor interface (F_0).

3.2.3 General Solution

The general solution to Equation (32) is:

$$F(x) = \frac{2k_B T g}{q} \cot(g(x + x_0)) \quad (34)$$

where x_0 is the characteristic length of the spatial decay in charge and is calculable from boundary conditions. The boundary condition that will lead to a solution for g is simply that the electric field at the semiconductor surface is zero ($F(t_{SC}) = 0$). From this we find:

$$\cot(g(t_{SC} + x_0)) = 0 \quad (35)$$

where t_{SC} is the thickness of the semiconductor. Since $\cot(u)$ is a repeating function, the range can arbitrarily be limited to between $0 \rightarrow \pi$, such that $g(t_{SC} + x_0) = \pi/2$. Using the second boundary condition, that the electric field at the insulator semiconductor interface is F_0 , the following relationship can be produced:

$$\frac{qF_0}{2k_B T} \frac{1}{g} = \tan(gt_{SC}) \quad (36)$$

where gt_{SC} is also limited between 0 & $\pi/2$.

Equation (36) shows that the value of g is dependent on the value of F_0 and must be computed as there is no analytical solution. Once computed the value of g may be put into a form of Equation (34) that has had x_0 replaced as shown:

$$F(x) = \frac{2k_B T g}{q} \tan(g(t_{SC} - x)). \quad (37)$$

Because of the numerical calculation required to produce g it is unsurprising that the thick film approximation is a commonly made assumption.

3.2.4 Voltage Drop Approximation (VDA)

Whether or not the TFA is being implemented, the electric field at the semiconductor interface (F_0) is required to calculate the spatial function. The simplest way to calculate this electric field is using the voltage drop approximation (VDA). This approximation assumes that all the gate voltage is dropped across the insulator. Hence the electric field inside the insulator is $F_{ins} = V_G/t_{ins}$ where t_{ins} is the insulator thickness. From this the value of F_0 can be calculated using conservation of displacement fields:

$$F_0 = \frac{\epsilon_{ins} V_G}{\epsilon_{SC} t_{ins}} \quad (38)$$

where ϵ_{ins} and ϵ_{SC} are the permittivity of the insulator and semiconductor in turn. This gives an expression for F_0 that can be inserted into Equation (33) for the thick film solution (using the TFA) and Equation (36) for the non-thick film solution (the non-TFA solution).

In reality the voltage from the gate decreases both through the insulator and through the semiconductor. To calculate the electric field at the dielectric/semiconductor interface, the continuity across the interface must be considered. Continuity across the interface produces two conditions that must be fulfilled. Firstly, conservation of displacement field, and secondly conservation of voltage. Note that the differential of voltage does not need to be conserved across the interface. By applying these two conditions, the non-TFA solution for charge depth in a MIS structure can be modified to calculate g from Equation (36). This produces the following equation:

$$\ln|\cos(gt_{SC})| - \frac{\epsilon_{SC}}{C_{ins}} g \tan(gt_{SC}) + \frac{qV_G}{2k_B T} = 0 \quad (39)$$

where C_{ins} is the capacitance of the insulating layer. By solving Equation (39) to find g , the value of g can be reinserted into Equation (34) to produce the charge depth solution with neither the

VDA nor TFA. Finally, for the TFA (without the VDA), the same two conditions can be used to produce the following equation:

$$\ln \left| \frac{2k_B T}{q} + t_{sc} F_0 \right| - \frac{q \epsilon_{sc}}{2k_B T C_{ins}} F_0 + \frac{q V_G}{2k_B T} - \ln \left| \frac{2k_B T}{q} \right| = 0 \quad (40)$$

which allows for the numerical calculation of F_0 . This is reinserted into Equation (33) for the TFA solution without the VDA.

3.2.5 Summary of Charge Depth Equations

From the electric field for each of the two solutions, the voltage can be calculated by integrating the electric field from the semiconductor surface (where the voltage is zero) to any position in the semiconductor. Likewise, the carrier charge density can be calculated from Gauss's law. **Table 3.1** contains the solutions to these three physical entities as a function of the constant of integration g . Along with this, **Table 3.1** also contains solutions for g with and without the VDA. Similarly,

Table 3.2 contains the equations for electric field, voltage and carrier charge density for when the TFA is used. The physical entities are dependent on the surface potential F_0 and two methods for calculating this are provided both using, and avoiding the VDA.

Table 3.1: Summary of equations for the profile of electric field, voltage and carrier density in a MIS structure assuming the general solution. Includes the method of calculating the constant of integration g both with and without the voltage drop approximation (VDA).

	Equations for General Solution
Electric Field	$F(x) = \frac{2k_B T g}{q} \tan(g(t_{sc} - x))$
Voltage	$V_{sc}(x) = -\frac{2k_B T}{q} \ln \cos(g(t_{sc} - x)) $
Carrier Density	$n(x) = \frac{2k_B T \epsilon_{sc} g^2}{q^2} \sec^2(g(t_{sc} - x))$
	Definition of g with(out) Voltage Drop Approximation (VDA)
Without VDA	$\ln \cos(gt_{sc}) - \frac{\epsilon_{sc}}{C_{ins}} g \tan(gt_{sc}) + \frac{q V_G}{2k_B T} = 0$
With VDA	$\tan(gt_{sc}) - \frac{q V_G C_{ins}}{2k_B T \epsilon_{sc}} \frac{1}{g} = 0$

Table 3.2: Summary of equations for the profile of electric field, voltage and carrier density in a MIS structure using the thick film approximation solution. Includes the method for calculating the surface potential (F_0) both with and without the voltage drop approximation (VDA).

	Equations for Thick Film Solution
Electric Field	$F(x) = \frac{2k_B T}{q} \frac{1}{x + \frac{2k_B T}{qF_0}}$
Voltage	$V_{SC}(x) = \frac{2k_B T}{q} \ln \left \frac{x + \frac{2k_B T}{qF_0}}{t_{SC} + \frac{2k_B T}{qF_0}} \right $
Carrier Density	$n(x) = \frac{2k_B T \epsilon_{SC}}{q^2} \frac{1}{\left(x + \frac{2k_B T}{qF_0}\right)^2}$
	Solution F_0 for with(out) Voltage Drop Approximation (VDA)
Without VDA	$\ln \left \frac{2k_B T}{q} + t_{SC} F_0 \right - \frac{q \epsilon_{SC}}{2k_B T C_{ins}} F_0 + \frac{q V_G}{2k_B T} - \ln \left \frac{2k_B T}{q} \right = 0$
With VDA	$F_0 = \frac{V_G C_{ins}}{\epsilon_{SC}}$

3.3 Charge Transport within Semiconductors

There exist many different models describing charge transport in semiconductors. The main three of interest are band transport, hopping transport and multiple trapping and release (MTR). Band transport is defined as the movement of charge carriers as waves through a set of delocalised states (the conduction band for electrons, and valence band for holes). The mobility of these waves is controlled mainly by scattering with the lattice structure (otherwise called acoustic phonons) and ionic impurities (also known as charged impurities) within the semiconductor.⁶³ On the other hand, hopping transport describes the movement of charged polarons between adjacent localised states. This occurs by either thermal activation over the barrier separating the two states, or via less common tunnelling events.⁶⁴ The third option of multiple trapping and release falls somewhere in between the models of band transport and hopping transport. It describes a system with one set of states that allows band-like transport but a secondary set of localised trap states.⁶⁵

These three descriptions create starting points for multiple models that predict how conduction varies with carrier concentration, temperature, electric field and doping

concentration. However, it is important to note that within each model there are multiple different assumptions that may be made to produce largely different interpretations.

3.3.1 Band Transport Mobility

The mobility of an electron within band theory of transport is controlled by scattering events. Each possible scattering event will have a mobility related to it and using Matthiessen’s rule the inverse of each individual mobility may be summed to produce the inverse of the total mobility. For example:

$$\frac{1}{\mu_{tot}} = \frac{1}{\mu_{lattice}} + \frac{1}{\mu_{ionic}} + etc. \quad (41)$$

where μ_{tot} , $\mu_{lattice}$ and μ_{ionic} are the total scattering, lattice scattering and ionic scattering in turn.

The most commonly considered form of scattering is lattice scattering which has a mobility temperature dependence of $\mu \propto T^{-3/2}$, while ionic scattering is also quite common with a mobility temperature dependence of $\mu \propto T^{3/2}$.⁶³ The ratio of lattice to ionic scattering events controls the overall temperature dependence of the mobility within band transport. **Table 3.3** contains examples of experimental temperature dependences for electrons and holes within germanium, silicon and gallium arsenide. It is interesting to note that all exhibit an inverted temperature dependence, with some having exceeding the maximum expected value of $T^{-1.5}$.

Table 3.3: Examples of the temperature dependence of both electron and hole mobility for three classic semiconductors from “The Physics of Semiconductor Devices”⁶³.

Material	Electron	Holes
Germanium	$\mu \propto T^{-1.66}$	$\mu \propto T^{-2.33}$
Silicon	$\mu \propto T^{-2.5}$	$\mu \propto T^{-2.7}$
Gallium Arsenide	$\mu \propto T^{-1.0}$	$\mu \propto T^{-2.1}$

For every semiconductor within **Table 3.3** the mobility increases with decreasing temperature. This is normally assigned to a decrease in lattice scattering as the lattice is cooled less acoustic phonons will be produced. Because of this, an inverse temperature dependence with mobility is commonly cited as an indication of band or band-like transport.^{40,66}

3.3.2 Hopping Transport Mobility

The basic concept of hopping transport is that charge carriers move from one localised state to another. In a simple case, all localised states exist within an energy spread smaller than $k_B T$. With this assumption, charge hops to nearest neighbour states only, and the solution can be simplified to one of only percolation paths with no temperature dependence.⁶⁷ Considering that at room temperature the average kinetic energy is roughly 26 meV, this is obviously a highly erroneous assumption for most semiconductors.

One of the first temperature dependent models of hopping transport was based on the movement of charge through pre-breakdown insulators by N. Mott (1969)⁶⁸ known as variable range hopping (VRH). In this, he predicted a mobility temperature dependence of $\mu \propto T^{-1/4}$ for low temperatures. This was quickly shown to be valid for only extremely low temperatures via further theoretical work⁶⁹ and has had little application to disordered semiconductors.

Modern models of hopping transport focus on either Monte Carlo simulation results by H. Bässler⁷⁰ or a more generic empirically based Arrhenius model. The results of a Monte Carlo simulation of hopping between sites within a Gaussian energy distribution by Bässler demonstrated a mobility temperature dependence of:

$$\mu \propto e^{-\left(\frac{T_0}{T}\right)^2} \quad (42)$$

where T_0 is the characteristic temperature of the system. While the Arrhenius model:

$$\mu \propto e^{-\left(\frac{\Delta}{k_B T}\right)} \quad (43)$$

where Δ is the activation energy of the system, has mainly been used due to its simple form and empirical nature. It has been noted that fitting these models to the same set of data can lead to excellent fits to both models.⁶⁵ Studies have suggested that the temperature dependence shown in Equation (42) is indicative of a Gaussian density of states, while Equation (43) is indicative of an exponential density of states.⁶⁷ Though currently there is a lack of rigorous methods to distinguish or justify either.

3.3.3 Multiple Trapping and Release Mobility

Multiple trapping and release (MTR) can be described in two separate ways with identical results. Both descriptions are based on the idea that there are a set of conductive states above the conduction band edge with a fixed mobility, and a set of localised states below the conduction

band edge with very low or no mobility. The first description is a dynamic description in which charge is induced into the conduction band, where it is accelerated by the electric field until it is caught by localised trap states for a characteristic time before being thermally released back into the conduction band. The second description is that charge induced in the channel of a semiconductor fills up both immobile trap states below the conduction band edge and the mobile states within the conduction band. The relative occupation of these states can be described using Fermi-Dirac statistics. The MTR model does not describe the form of the trap states below the conduction band edge. Though to produce meaningful results, an assumption of the form of these trap states often has to be made.

The essence of this model goes back to the field of amorphous silicon physics from the 1970's and the work of Comber and Spear⁷¹. Shur, Hack et al.⁷²⁻⁷⁴ modified the model further by including a double exponential set of trap states to describe charge transport in amorphous silicon devices. Amorphous silicon bares many similarities to the metal oxide semiconductors^{75,76} to which a similar model has been applied. The MTR model also found application in the field of organic electronics in the work of Horowitz et al.⁷⁷ and since then has been used to describe multiple systems including small molecule TFTs^{78,79} and organic blends⁸⁰.

Describing the temperature dependence of mobility for MTR is complex as it is dependent on both the form of the trapping states and conduction band. It is made even more intricate by its dependence on Fermi level position within the semiconductor. In Section 3.1.6 the idea of an intrinsic and apparent mobility was introduced. This concept may be applied here, with the intrinsic mobility being the mobility of the conduction band alone assuming no trap states. While the apparent mobility is the measured field effect mobility due to the trap states using standard FET mobility extraction methods. The conduction band states can be considered to be band-like in transport, hence assuming the temperature dependence of band transport. The apparent mobility is a convolution of both the band transport of the conduction band (the intrinsic mobility) diminished by the fraction of induced charge in the conduction band states as opposed to trap states. This will similarly affect that temperature dependence of the mobility as well which will be discussed later in Section 3.4.

3.4 Bandgap Density of States

This section shall discuss the possible forms of bandgap states within an MTR and the expected behaviour. The description of the MTR model will be based on Fermi-Dirac statistics, and hence the characteristic trapping time for charge carriers is irrelevant. Description of the following density of states and MTR models will introduce the concept of mobility as a function of induced charge μ_{V_G} which is defined as:

$$\mu_{V_G}(Q_{tot}) = \frac{Q_{CB}\mu_{CB} + Q_{trap}\mu_{trap}}{Q_{tot}} \quad (44)$$

where Q_{tot} , Q_{CB} and Q_{trap} are the total charge, charge in the conduction band and charge in the trap states respectively. While μ_{CB} and μ_{trap} are the intrinsic mobilities of carriers in the conduction band and trap states. The term for the mobility will be μ_{V_G} in reference to the fact that charge, in the devices produced in this work, is induced by the applied gate voltage of a TFT. This notation will be used even if the gate voltage itself is not directly included.

For the standard situation where $Q_{CB}\mu_{CB} \gg Q_{trap}\mu_{trap}$, then Equation (44) simplifies to:

$$\mu_{V_G}(Q_{tot}) = \frac{Q_{CB}}{Q_{tot}} \mu_{CB}. \quad (45)$$

Within this thesis the terms bandgap states and trap states shall be used synonymously.

For each possible form of the bandgap states we will make the assumption that the conduction band $g_{CB}(E)$ is a rectangular set of states. This allows for them to be described as follows:

$$g_{CB}(E) = \begin{cases} 0, & E < E_{CB} \\ g_{CB_0}, & E \geq E_{CB} \end{cases} \quad (46)$$

where E_{CB} and g_{CB_0} are the conduction band edge energy and the density of states of the conduction band in turn.

A common result that is required by MTR models is the number of occupied conduction band states ($n_{CB}(E_F)$) when the Fermi level is at an energy E_F . This is given by:

$$n_{CB}(E_F) = \int_{E_{CB}}^{\infty} g_{CB_0} \times f(E - E_F) dE \quad (47)$$

where $f(E - E_F)$ is the Fermi function. Inserting the actual Fermi function into Equation (47) gives:

$$n_{CB}(E_F) = g_{CB_0} \int_{E_{CB}}^{\infty} \frac{1}{1 + e^{\beta(E-E_F)}} dE \quad (48)$$

where $\beta = 1/k_B T$. Finally the integral can be solved to give the following expression:

$$n_{CB}(E_F) = \frac{g_{CB_0}}{\beta} [\beta(E_F - E_{CB}) + \ln(1 + e^{\beta(E_{CB}-E_F)})]. \quad (49)$$

3.4.1 Monoenergetic Bandgap Density of States

The simplest form for the bandgap states is that of a monoenergetic delta function located at energy E_{mono} below the conduction band. The absolute position of the delta function is therefore $E_{trap} = E_{CB} - E_{mono}$. Mathematically a monoenergetic bandgap density of states is given by:

$$g_{mono}(E) = \begin{cases} 0, & E < E_{CB} - E_{mono} \\ g_{mono_0}, & E = E_{CB} - E_{mono} \\ 0, & E > E_{CB} - E_{mono} \end{cases} \quad (50)$$

where g_{mono_0} is the total number of states at the delta function. The number of charge carriers caught in the monoenergetic trap states ($n_{trap}(E_F)$) is:

$$n_{trap}(E_F) = g_{mono_0} \int_{-\infty}^{\infty} \delta(E_{CB} - E_{mono}) \times \frac{1}{1 + e^{\beta(E-E_F)}} dE \quad (51)$$

where $\delta(E_{CB} - E_{mono})$ is the Dirac delta function. By using the identity of the delta function the trapped charge is therefore:

$$n_{trap}(E_F) = \frac{g_{mono_0}}{1 + e^{\beta(E_{CB}-E_{mono}-E_F)}}. \quad (52)$$

Assuming that the trap states have no mobility, and that the conduction band mobility is constant with temperature, it is possible to calculate the mobility as a function of the Fermi level using Equation (45). The total charge (Q_{tot}) is given by the sum of Equations (49) and (52) while the conduction band charge (Q_{CB}) can be calculated from Equation (49). **Figure 3.1** shows an example of the temperature dependence of a model system with monoenergetic traps for different Fermi level energies.

At high temperatures, as the Fermi function broadens, the probability of occupation for the trap states and conduction band becomes independent of Fermi level position. This is seen in the convergence of all the Arrhenius lines within **Figure 3.1** when approaching $1000/T = 0$. At lower temperatures if the Fermi level is within the conduction band the mobility of the device is independent of temperature. When the Fermi level is lower than the conduction band, the low

temperature dependence of mobility becomes inversely exponential with a decreasing slope as the Fermi level reaches the trap states energy. When the Fermi level is far enough below the monoenergetic trap states, the temperature dependence becomes independent of Fermi level.

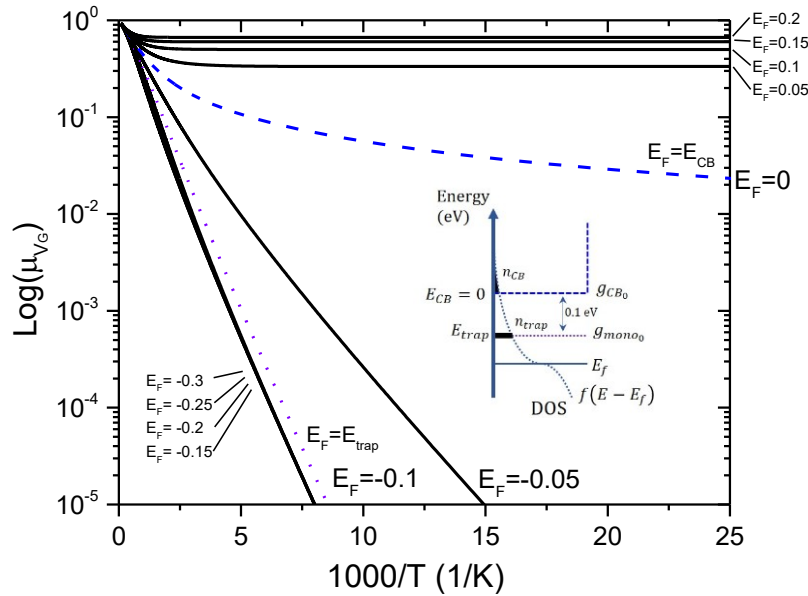


Figure 3.1: Arrhenius plot of apparent mobility with temperature for a system with a rectangular conduction band and monoenergetic trap states. All values of energy shown are in units of eV. The system assumes the following values: $E_{CB} = 0$ eV, $E_{trap} = -0.1$ eV, $g_{CB0} = 10^{20}$ eV⁻¹cm⁻³, $g_{mono} = 10^{19}$ cm⁻³, and $\mu_{CB} = 1$ cm²/Vs. Inset shows a schematic of the model used to generate the temperature dependence.

This description is very similar to the diagrams produced by Stallinga and Gomes⁸¹. The main differences lie in the use of the Fermi level as the third variable (instead of gate voltage) which allows the probing of solutions that the TFT applied model does not.

3.4.2 Exponential Density of States

Monoenergetic states provide the simplest example of trap states within a material and has a motivational basis in the addition of trapping dopants from classical semiconductor physics. Another way to describe the density of states in the bandgap is as one or two exponentials, an approach previously used and validated within the field of amorphous silicon physics.⁷²⁻⁷⁴ The first approach is to use a single exponential density of states that merges continuously with the conduction band. Only a single parameter is required to describe this exponential set of bandgap states which is the half-energy $E_{1/2}^{exp1}$ (the amount of energy required for the number of states to drop by half). The mathematical function for these states is $g_{exp1}(E)$ therefore:

$$g_{exp1}(E) = \begin{cases} g_{CB0} \exp\left(\frac{\ln(2)(E - E_{CB})}{E_{1/2}^{exp1}}\right), & E \leq E_{CB} \\ 0, & E > E_{CB} \end{cases} \quad (53)$$

By convoluting the exponential states with the fermi function an equation for the number of occupied trap states is found:

$$n_{exp1}(E_F) = \int_{-\infty}^{E_{CB}} \frac{g_{CB0} e^{(\ln(2)(E - E_{CB})/(E_{1/2}^{exp1}))}}{1 + e^{\beta(E - E_F)}} dE. \quad (54)$$

Equation (54) cannot be solved analytically; therefore, a computed quantized energy approach must be taken. The computed results, assuming a conduction band mobility independent of temperature, are shown in **Figure 3.2**. The results bear similarities to those of Section 3.1.4, though there is more differentiation in the temperature dependence at low Fermi levels for the exponential states.

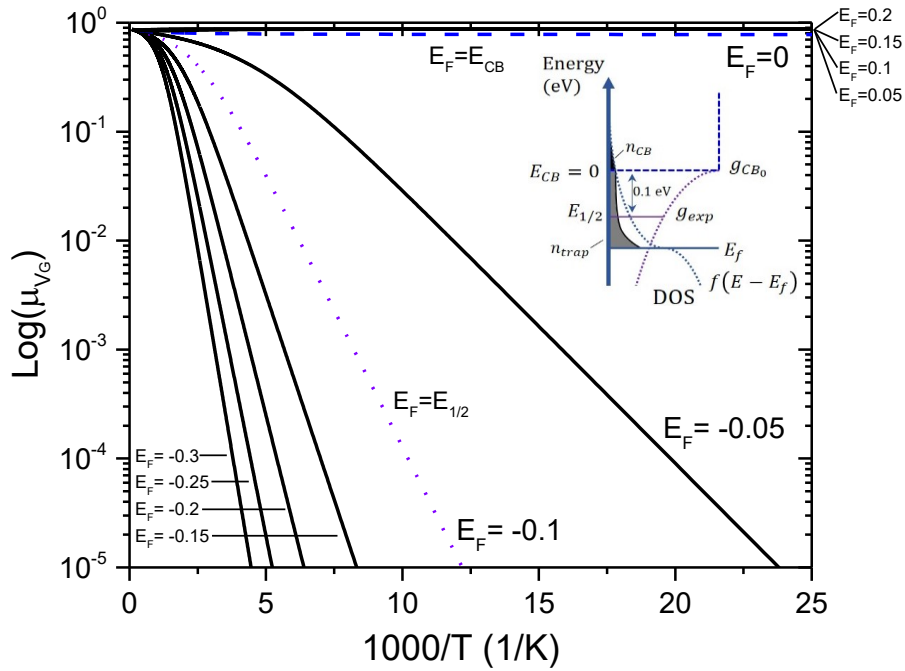


Figure 3.2: Arrhenius plot of apparent mobility with temperature for a system with a rectangular conduction band and a single exponential set of trap states that pairs smoothly with the conduction band. All values of energy shown are in eV. The system assumes the following values: $E_{CB} = 0$ eV, $E_{1/2} = -0.1$ eV, $g_{CB0} = 10^{20}$ eV⁻¹cm⁻³, and $\mu_{CB} = 1$ cm²/Vs. Inset shows a schematic of the model used to generate the temperature dependence.

In **Figure 3.2** there is also a large change that occurs in the temperature dependence as the Fermi level moves past the half-energy of the exponential trap states. As the Fermi level

moves towards the conduction band, the sensitivity of the measured mobility to temperature decreases until it becomes negligible when it reaches the conduction band.

The single exponential model of the bandgap density of states can be expanded to a double exponential by the addition of a second set of states ($g_{exp2}(E)$). Unlike the original set of states, which merges continuously with the conduction band, these second states have a maximum value of $g_{exp2_0}(E_{CB})$ and are described mathematically by:

$$g_{exp2}(E) = \begin{cases} g_{exp2_0} \exp\left(\frac{\ln(2)(E - E_{CB})}{E_{1/2}^{exp2}}\right), & E \leq E_{CB} \\ 0, & E > E_{CB} \end{cases} \quad (55)$$

Inserting this second set of trap states into the model from **Figure 3.2** produces the Arrhenius plot of **Figure 3.3**. The differences between the single and double exponential model are minimal, and mainly down to the increased number of states in total within the bandgap, leading to the conclusion that the higher density of states are more important within an MTR model.

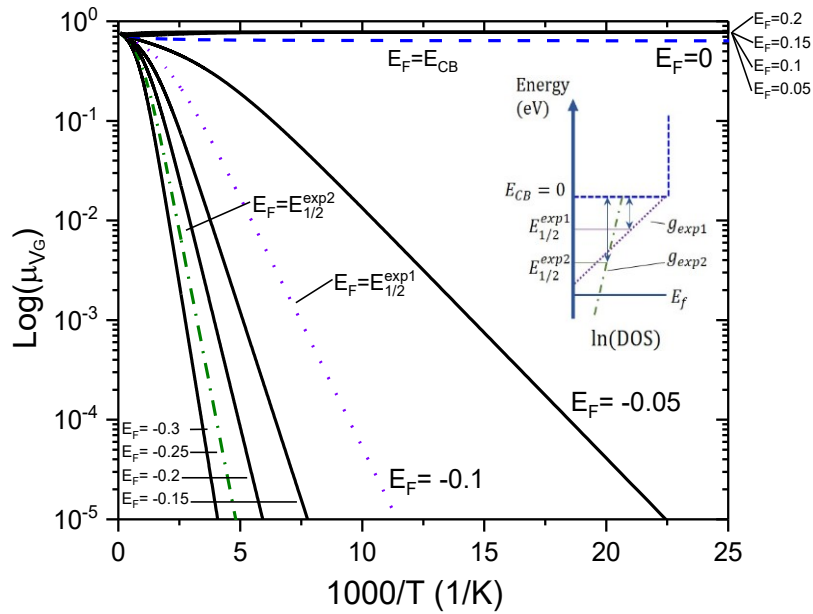


Figure 3.3: Arrhenius plot of apparent mobility with temperature for a system with a rectangular conduction band and two exponential sets of trap states that stop at the conduction band edge. The system conduction band assumes the following values: $E_{CB} = 0$ eV, $g_{CB_0} = 10^{20}$ eV⁻¹cm⁻³, and $\mu_{CB} = 1$ cm²/Vs. The first exponential set of trap states have a half energy of $E_{1/2}^{exp1} = 0.1$ eV. The second exponential set of trap states have the following values: $g_{exp2_0} = 5 \times 10^{19}$ eV⁻¹cm⁻³ and $E_{1/2}^{exp2} = 0.25$ eV. The inset shows a schematic of the model used to generate the temperature dependence.

3.4.3 Grain Boundary Models

Grain boundary models have gained popularity in both organic and inorganic polycrystalline semiconductors due to their prediction of gate dependent mobility. The grain boundary model was initially developed for polycrystalline silicon doped with boron.⁸² It describes how at grain boundaries there exist states that trap charge, consequently causing an accumulation of the opposite charge around it to screen it out. This accumulation of charge provides an energy barrier that must be overcome by carriers moving through the semiconductor. From this an equation for the apparent mobility (μ_{app}) as a function of intentional doping concentration was derived giving:

$$\mu_{app} = qL \left(\frac{1}{2\pi m^* k_B T} \right)^{1/2} e^{-\frac{E_B}{k_B T}} \quad (56)$$

where L is the distance between grain boundaries and E_B is the barrier energy at a grain boundary. This equation is often simplified to:

$$\mu_{app} = \mu_0 e^{-\frac{E_B}{k_B T}} \quad (57)$$

where μ_0 is the mobility prefactor, similar to the intrinsic mobility of the device. This is problematic as it leads to an identical relationship as described by the Arrhenius hopping model in Section 3.3.2.

The energy barrier height is given by:

$$E_B = \begin{cases} qL^2 N / 8\epsilon_{SC}, & LN < Q_t \\ qQ_t^2 / 8\epsilon_{SC} N, & LN > Q_t \end{cases} \quad (58)$$

where N is the doping concentration, ϵ_{SC} is the permittivity of the semiconductor and Q_t is the density of trap states in the grain boundary. Baccarani et al.⁸³ expanded on this model by demonstrating the differences expected between grain boundary models assuming different energy distributions of the trap states at the grain boundary.

Another interesting adaption to this model was reported in 2000 by Horowitz et al.⁷⁷. They applied and adapted the grain boundary model further for polycrystalline oligothiophene semiconductors measured at low temperatures where thermionic emission decreases rapidly. In their report they argue that a new regime is reached, in which tunnelling current becomes the dominant mechanism for charge transport across the boundary.

3.4.4 Unbound Models

MTR models do not always require the bandgap density of states to be known a priori. Instead MTR theory can be used as the basis for calculating the shape of states within the bandgap. One of the first such methods was developed by Spear and Comber and published in 1972⁸⁴, where they demonstrated a calculation for localised states (another term for bandgap or trap states) within amorphous silicon. Using the ratio of mobile to trapped charge, from Equation (45), and assuming a parabolic Schottky barrier at the dielectric-semiconductor interface, they produced a routine for calculating the bandgap states within a material from field effect measurements applying a stepwise approach. This method's advantage as well as downfall exists in its simplicity. It makes the assumption that when increasing the gate voltage, all of the induced charge is in localised states, and that free carriers may be ignored. Still, for its time it was an appropriate approximation, as it allowed for simple calculation by hand of the density of states.

It is inevitable when trying to calculate bandgap states that approximations must be made. Some are justified by proving the approximation close enough to reality to be an irrelevant complication to the model. Others are made out of necessity to render the unsolvable solvable. The majority of theoretical work and analysis within this thesis focuses on the second scheme to calculate the density of states in the bandgap following the approach published in 1980 by Grünewald et al.⁸⁵. A full description and derivation of the Grünewald method is to follow in Section 4.2. Other methods exist for calculating these bandgap states, and an excellent review of such schemes has been performed by Kalb et al.⁸⁶

4 Simulation and Analysis Models

Within this thesis, the Grünewald method, as outlined in the 1980 paper by Grünewald et al.⁸⁵, was used to extract the bandgap states of the semiconducting layer of a TFT. This analysis takes experimental data from a single transfer characteristics (as described in Section 2.4.1) and, using this, calculates the density of states (DOS) in the bandgap of the semiconductor. Two important assumptions are made by the Grünewald method of analysis. The first is that the films are thick enough to use the thick film approximation described mathematically in Section 3.2.2. The second is that the voltage drop inside the semiconductor is insignificant compared to the voltage dropped across the dielectric (described mathematically in Section 3.2.4).

To probe the validity of these assumptions, simulations were performed using a finite element model based upon the same mathematical root as the Grünewald analysis method. This model and the simulations performed with it shall form the basis of Section 4.1 of this chapter.

4.1 Finite Element Model Simulation

A finite element model takes a description of a physical system and breaks it down into a chosen number of small sections. It is often used when solutions to equations, describing physical situations, are unable to be solved analytically and hence must be calculated numerically instead. Finite element modelling is a commonly used technique and forms the basis of multiple commercial software including the multiphysics modelling tool COMSOL.

Within this research, the current through a semiconducting material due to the accumulation of charge in a metal-insulator-semiconductor (MIS) capacitor was calculated. The accumulated charge is therefore a function of both position and energy. Four possible calculations for the accumulation of charge in a MIS structure are given in Section 3.2.5, only one of which may be analytically solved. It is because of this that a finite element model is required. The finite model contains two sets of elements: the first is in the x -direction (defined as perpendicular to the dielectric/semiconductor interface), and the second is the energetic position away from the Fermi level of the material. A more accurate model would consider also the drain voltage perpendicular to the x -direction, and how this voltage would alter the applied voltage of the gate contact in a TFT. This inclusion of a y -direction for modelling the applied drain voltage is deemed

unnecessary when the gate voltage range is much greater than the drain voltage. Such as when a TFT is operating in the linear regime, as with the data used within this thesis.

4.1.1 Model Parameters

A schematic of the setup of the quantization of spatial and energetic functions is shown in **Figure 4.1**. For the spatial quantization, the thickness of the semiconductor (t_{SC}), as illustrated in inset (c) of **Figure 4.1**, was separated into N_x points with a distance between points of $\Delta x = t_{SC}/(N_x - 1)$. Similarly, for the energetic quantization, a maximum (E_{max}) and minimum (E_{min}) energy for the model was defined and then separated into N_E points with a spacing of $\Delta E = (E_{max} - E_{min})/(N_E - 1)$.

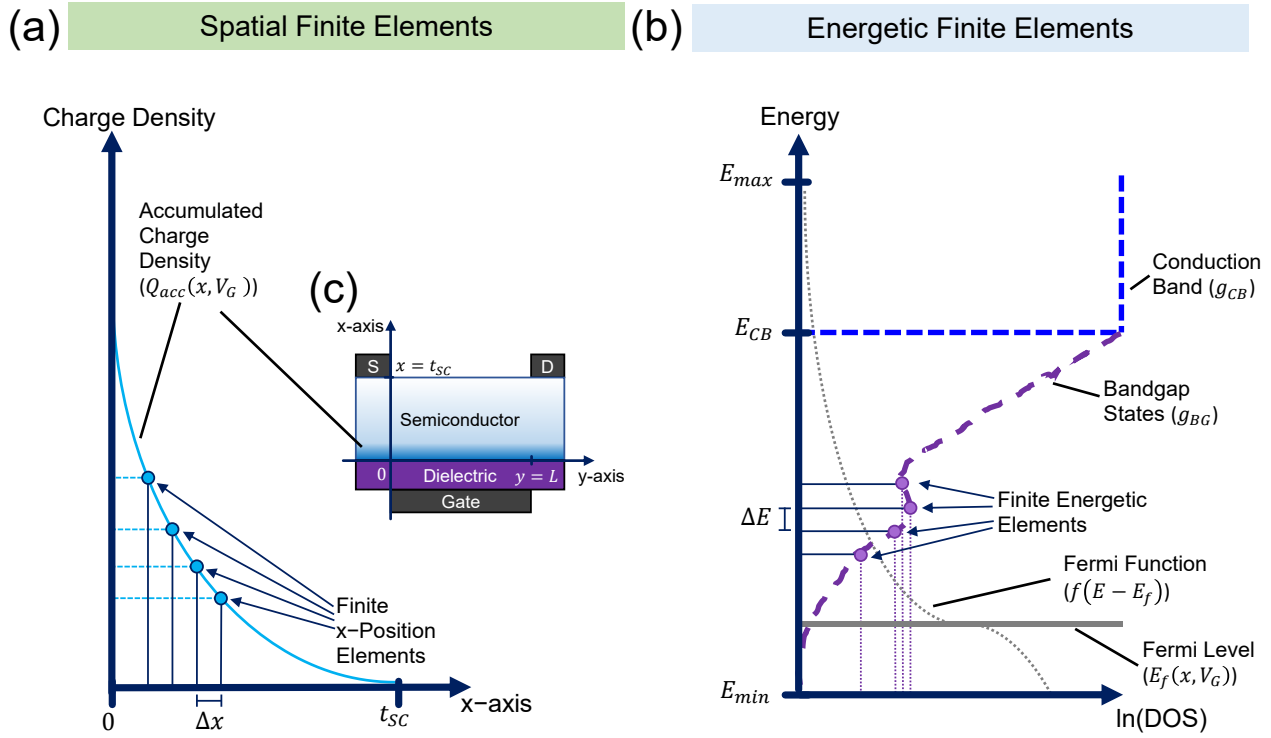


Figure 4.1: Schematics of (a) the spatial finite element aspect and (b) the energetic finite element aspect of the simulation used to produce linear transfer characteristics for device structures shown in the inset (c). Within the description Δx and ΔE are the spacing between position and energetic elements respectively. All other parameters are defined in **Table 4.1**.

The parameters required to first describe the energy structure of a semiconductor and then simulate a TFT using that semiconductor are provided in **Table 4.1**. The required parameters have been separated into energetic properties of the DOS, semiconductor properties unrelated to the energetics, and general TFT properties.

Table 4.1: Parameters required to simulate the linear transfer characteristics of a TFT

Symbol	Units	Parameter
Energetic Properties		
E_{CB}	eV	Conduction band edge energy
g_{CB_0}	$eV^{-1} cm^{-3}$	Conduction band DOS
E_{BG_0}	eV	Bandgap state peak energy (refer to Table 4.2)
g_{BG_0}	$eV^{-1} cm^{-3}$	Bandgap state peak DOS (refer to Table 4.2)
$E_{BG_{1/2}}$	eV	Characteristic energy of bandgap states (refer to Table 4.2)
E_{max}	eV	Maximum energy of the finite element model
E_{min}	eV	Minimum energy of the finite element model
N_E		Number of energy points to split the energy finite element model into
Semiconductor Properties		
t_{SC}	nm	Thickness of the semiconductor
N_x		Number of points in the x direction to split the semiconductor finite element model into
T	°K	Temperature of the semiconductor
μ_{CB}	$cm^2 V^{-1} s^{-1}$	Mobility of the conduction band of the semiconductor
ϵ_{SCr}		Relative permittivity of the semiconductor
TFT Properties		
V_G	V	The maximum gate voltage of the TFT
N_{V_G}		Number of voltage points corresponding to voltage points in the transfer characteristics
V_D	V	Drain voltage applied to the TFT
W, L	μm	TFT width and length
C_{ins}	nF/cm ²	Specific capacitance of the insulator
I_{off}	A	Minimum value of current that is able to be measured

The values used to describe the bandgap states in **Table 4.1** are generic so that they may be applied to one of three possible DOS forms; rectangular, Gaussian or exponential. The simulation, as described in the flow diagram in **Figure 4.2**, allows for three unique bandgap DOS (g_{BG_1} , g_{BG_2} , and g_{BG_3}), that are summed to produce a total density of bandgap states (g_{BG}). The bandgap DOS

and the rectangular conduction band as described by parameters in **Table 4.1** and illustrated in **Figure 4.1** are then quantized in energy. Next the Fermi level (E_F) is set to equal each quantized energy point and for each value of the Fermi level the total charge (Q_{tot}) and mobile charge in the conduction band (Q_{CB}) are calculated. This produces a function of mobile charge to accumulated charge from the energy finite element model that can be interpolated later.

Table 4.2: The three possible forms for individual bandgap states. The total density of bandgap states consisted of the sum of these three states. Variables within the equations are defined in **Table 4.1**.

Trap State Form	Equation
Rectangle	$g_{BG_x}(E) = \begin{cases} 0, & E - E_{BG_0} > \frac{E_{BG_{1/2}}}{2} \\ g_{BG_0}, & E - E_{BG_0} \leq \frac{E_{BG_{1/2}}}{2} \end{cases}$
Gaussian	$g_{BG_x}(E) = g_{BG_0} \exp\left(-4 \ln(2) \left(\frac{E - E_{BG_0}}{E_{BG_{1/2}}}\right)^2\right)$
Exponential	$g_{BG_x}(E) = \begin{cases} 0, & E > E_{BG_0} \\ g_{BG_0} \exp\left(-\frac{E - E_{BG_0}}{\ln(2) E_{BG_{1/2}}}\right), & E \leq E_{BG_0} \end{cases}$

The next step within the simulation is to calculate for each respective gate voltage (V_G) the accumulated charge for each x element. This produces a two-dimensional matrix with axes of gate voltage and x -position, whose values are the accumulated charge. By interpolating the relationship between total charge and mobile charge calculated from the energetic model, the values of accumulated charge in the two-dimensional matrix can be converted to mobile charge. By summation over all x elements for each gate voltage, the drain current can be calculated using the linear drain current in Equation (6), modified to only include mobile charge.

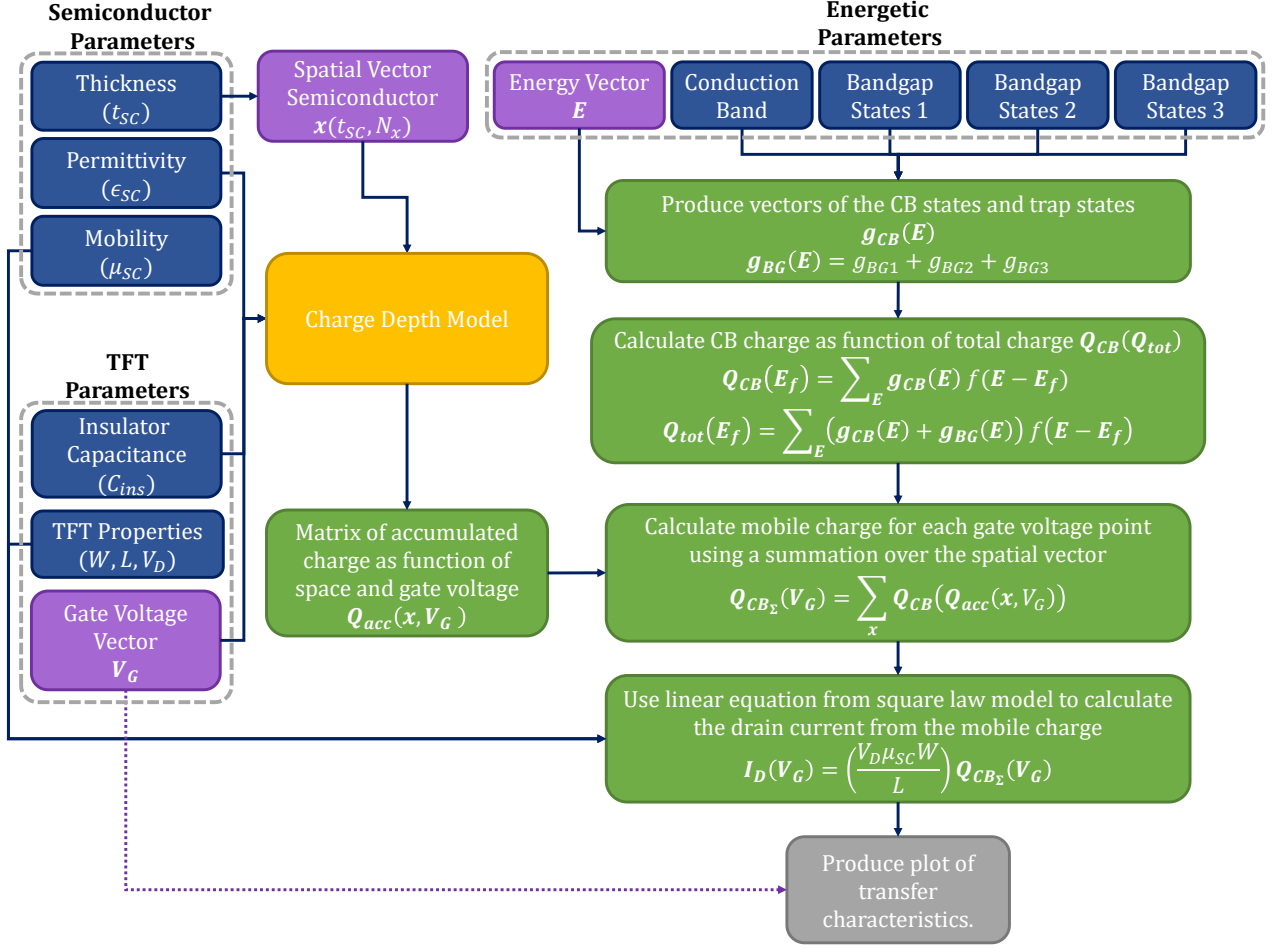


Figure 4.2: Flow diagram of finite element model used to simulate the linear transfer characteristics of a TFT. The simulation produces a finite element vector for both the spatial x -position and the energy of the DOS. It then performs the calculations in green for each applied gate voltage in the gate voltage vector to simulate a drain current for each gate voltage point. The charge depth calculations used to model the charge depth (in orange) are described in Section 3.2.

4.1.2 Approximation Simulations

Before simulating TFT characteristics using the thick film approximation (TFA) and voltage drop approximation (VDA), the voltage, electric field and charge carrier were modelled. **Table 3.1** and **Table 3.2** were used to calculate these three values for a MIS capacitor with semiconductor and dielectric thickness of 100 nm, a dielectric capacitance of 34.4 nF/cm². The semiconductor's relative permittivity was set to 8.9 and the MIS structure was under a bias of 1 V. The simulation result is shown in **Figure 4.3** and represents a 100 nm thick layer of In₂O₃ produced on 100 nm of thermally grown SiO₂. The keen of eye may note that the internal potential for the VDA

solution is not zero within the semiconductor. The explanation for this is that the electric field within the semiconductor is calculated using the VDA. The internal potential is then calculated from integrating the electric field from t_{SC} to the position x . Hence why there is finite voltage in the semiconductor even with the VDA. Also, to maintain visual continuity the values for internal potential in the dielectric were calculated by linearly fitting between the applied voltage (1 V) at the gate contact and the internal potential calculated at the interface. Similarly the electric field in the dielectric was calculated by linearly matching from zero field at the gate contact, to the interface field at the dielectric/semiconductor interface.

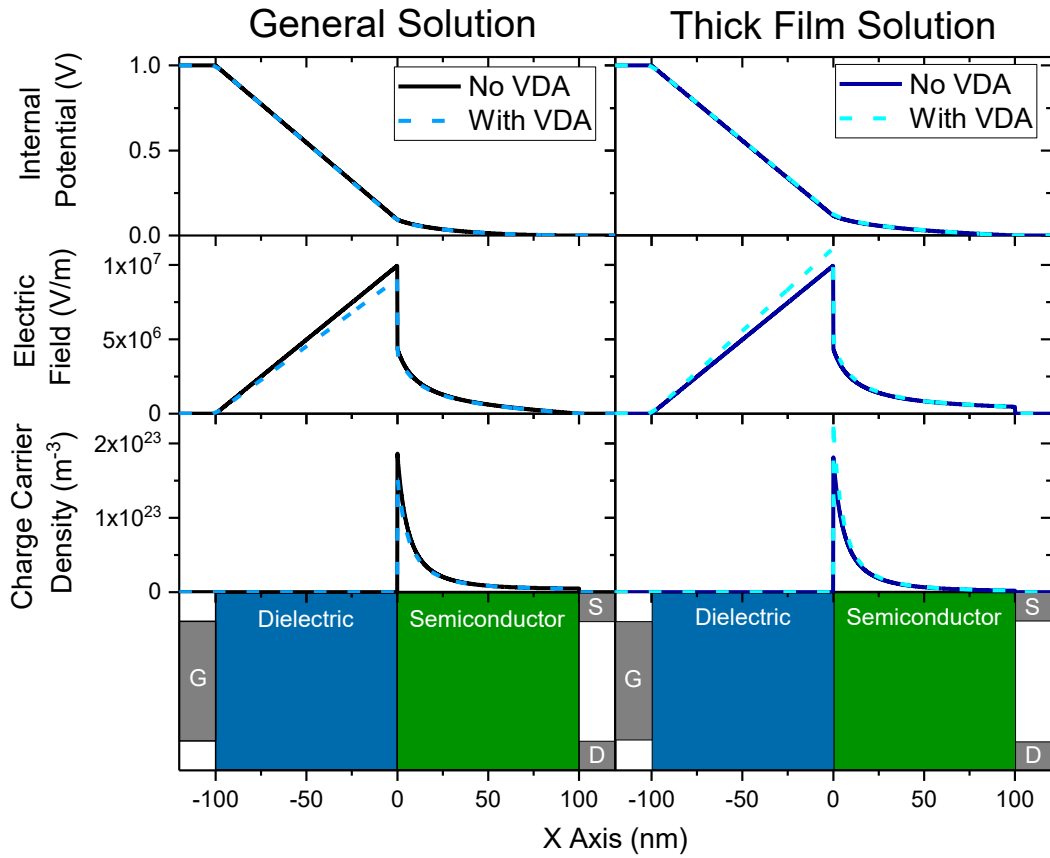


Figure 4.3: The internal potential, electric field and charge carrier density as calculated using the four different charge depth equations. The results were calculated using the following parameters: $t_{SC} = 100$ nm, $V_G = 1$ V, $\epsilon_{SC} = 8.9$, $t_{ins} = 100$ nm and $C_{ins} = 34.4$ nF/cm².

The results of the simulation in **Figure 4.3** highlight that there is very little difference using the general or thick film solution, with or without the VDA for thick films, and even at voltages as low as 1 V. Although not shown here, other simulations exhibited even less of a difference between results for higher applied gate voltages than 1 V.

The next step in assessing the impact of the CDA and VDA is to examine the effect of reduced film thickness on the calculated charge density for each of the approximation combinations. To do this the same system as modelled in **Figure 4.3** was used, varying the semiconductor thickness, and with an increased gate voltage of 10 V. The simulation results for the charge carrier density calculated for a semiconductor of thickness 1, 10 and 100 nm are shown in **Figure 4.4**.

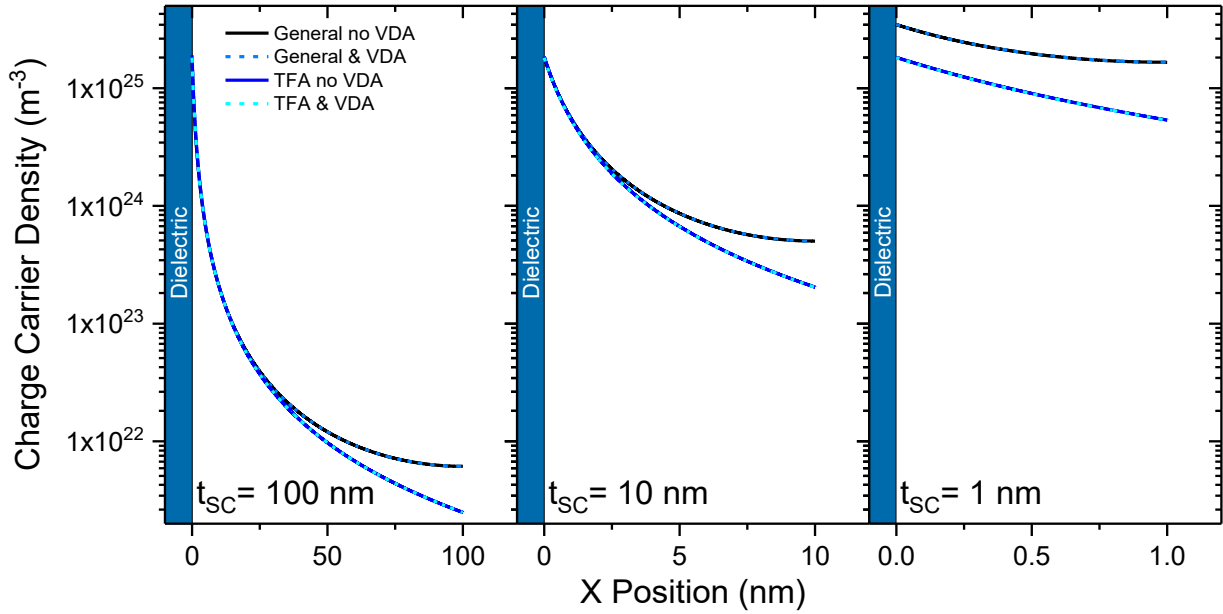


Figure 4.4: A comparison of the charge carrier density for semiconductors of thickness 100, 10 & 1 nm using four different charge depth equations. The results were calculated using the following parameters: $V_G = 10 \text{ V}$, $\epsilon_{SC} = 8.9$, $t_{ins} = 100 \text{ nm}$ and $C_{ins} = 34.4 \text{ nF/cm}^2$.

As stated earlier, **Figure 4.4** demonstrates that for higher gate voltages the difference in charge density calculated with or without the VDA becomes negligible. Hence the VDA is a reasonable approximation to use in the Grünwald analysis model. Also observable in **Figure 4.4** is the similarity in all solutions for the 10 nm and 100 nm simulations near the dielectric/semiconductor interface. Although for the 10 nm and 100 nm simulations the general and TFA solutions diverge towards the semiconductor surface, the log scale makes this difference almost negligible. It should be noted that we are assuming that the general solution without VDA is the physically realistic solution. The TFA solution underestimates the charge density at all thicknesses, but especially for the 1 nm semiconductor layer simulation. The conclusion from this is that the thick film approximation is applicable down to thicknesses of

even 10 nm, and maybe lower. On the other hand, for 1 nm thick thin films or less, the thick film approximation is completely inappropriate.

The final stage of these simulations involved creating a hypothetical set of bandgap states and calculating the drain current for a set of gate voltages, hence simulating a transfer characteristic measurement. The bandgap DOS consists of a double exponential with a Gaussian as illustrated in **Figure 4.5** (a) while the MIS capacitor is the same as that described in **Figure 4.4** but with varying gate voltages. Full details of all the parameters used in this simulation are available in Appendix C.

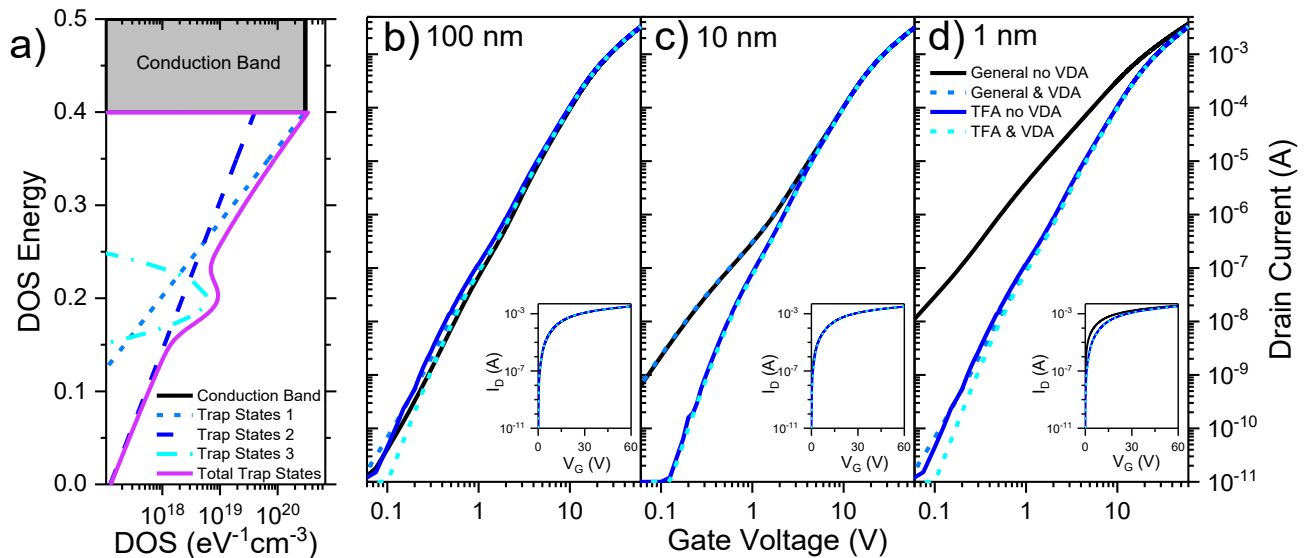


Figure 4.5: a) Energetics of bandgap states used to model TFTs of semiconductor thickness b) 100 nm, c) 10 nm and d) 1 nm. TFT calculations were performed using each of the four different charge depth equations. Insets within b), c) and d) show the same data as the corresponding subfigure but on the standard semilog axis (log(y) and lin(x)) used to express transfer characteristic data. Full simulation parameters used to produce these plots are available in **Table 7.1**.

The results of TFT simulations on 1, 10 and 100 nm layers of semiconductor in a MIS transistor (or TFT) are shown in **Figure 4.5**. The black line in **Figure 4.5** (b)-(d) is the solution without the use of approximation, and for the 100 nm semiconductor film, all the possible approximation combinations produce extremely similar results to the non-approximated solution. As the semiconductor thickness decreases to 10 nm, the thick film approximated results start to deviate at low gate voltages. Note, to see this deviation the simulation results had to be plotted on a double logarithmic axis. The inset in **Figure 4.5** (c) shows the same data on a semilog axis normally used for transfer characteristic measurements. In the semilog axis the

deviation between the general solution and the TFA solution is unobservable as it exist only below 1 V.

Finally, for the 1 nm semiconductor film simulation shown in **Figure 4.5** (d), all the approximated solutions fall far from the general non-VDA solution. The difference is so significant that, unlike for the 10 nm film, it is observable on a semilog plot (as seen in the inset of **Figure 4.5** (d)). The outcome from these simulations continues on from the charge carrier depth results of **Figure 4.4**. The charge depth results made it seem as if just the thick film approximation broke down for films somewhere between 10 nm and 1 nm. But from **Figure 4.5** it is obvious that both the thick film approximation and the voltage drop approximation breakdown in this region.

4.2 Grünewald Bandgap Analysis

The Grünewald model is the second of the two models that form the basis of the theoretical work within this thesis. In 1980 Grünewald et al. described a scheme for calculating the density of states in a semiconductor based off a single transfer characteristic.⁸⁵ The model compares the amount of charge injected into the channel with the amount of mobile charge carriers measured via the drain current. The difference between these values is attributed to the localised states below the bandgap and, from this, the bandgap states are calculated.

The Grünewald model is usually applied to intrinsic semiconductors, where there exist only intrinsic impurities in the bandgap to trap charge. These intrinsic impurities are assumed to be charge neutral until occupied and hence do not dope in the same manner as a conventional and intentionally added dopant. The addition of an intentional dopant to produce an extrinsic semiconductor could be assumed to cause a breakdown of this model. But as far as the author is aware, this assumption is incorrect. The Grünewald model does not care what the charge is of a bandgap state before or after it is occupied, only that states exist in the bandgap to be occupied. The addition of an intentional or unintentional dopant will only change the charge balance within a material leading to a shift in the thermal equilibrium Fermi level as discussed in great detail in Chapter 16.3 of William Shockley's "Electrons and Holes in Semiconductors with Applications to Transistor Electronics"⁸⁷. It is important to note that if an extrinsic semiconductor is used, the channel must still remain homogenous, though the dopant need not be homogenous outside of the channel.

4.2.1 Model Derivation

A detailed derivation of this analysis scheme can be found in Appendix B, but a more concise description will be outlined here. The parameters used within the derivation are all outlined within **Table 4.3**.

Table 4.3: Parameters used within the Grünewald model derivation.

Symbol	Units	Parameter
Energetic Parameters		
E	eV	Energy
E_{CB}	eV	Conduction band edge energy
E_F	eV	Fermi level position
E_{FB}	eV	Flat-band energy
g_{CB_0}	$\text{eV}^{-1} \text{cm}^{-3}$	Conduction band DOS
$g_{BG}(E)$	$\text{eV}^{-1} \text{cm}^{-3}$	Unbound form bandgap density of states
$n_{CB}(\phi)$	cm^{-3}	Charge carrier density in the conduction band as a function of the internal potential
$n_{BG}(\phi)$	cm^{-3}	Charge carrier density in bandgap states as a function of the internal potential
$n(\phi)$	cm^{-3}	Total charge carrier density in the semiconductor
ϕ	eV	The internal potential within the semiconductor
Semiconductor Parameters		
t_{SC}	nm	Thickness of the semiconductor
T	$^{\circ}\text{K}$	Temperature of the semiconductor
μ_{CB}	$\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$	Mobility of the conduction band of the semiconductor
ϵ_{SC}	F m^{-1}	Permittivity of the semiconductor
TFT Parameters		
V_G	V	The maximum gate voltage of the TFT
V_D	V	Drain voltage applied to the TFT
W, L	μm	TFT width and length
C_{ins}	nF cm^{-2}	Specific capacitance of the insulator
I_{off}	A	Minimum value of current measurable

The derivation starts from Gauss' Law:

$$\frac{d}{dx}(\phi'(x)) = \frac{qn(\phi(x))}{\epsilon_{SC}} \quad (59)$$

where $n(\phi(x))$ is the density of additional charge carriers, which can be rearranged and then both sides integrated over x to give:

$$(\phi'(x))^2 - (\phi'(t_{SC}))^2 = \frac{2q}{\epsilon_{SC}} \int_0^{\phi(x)} n(\phi(x)) d\phi. \quad (60)$$

To aid in further calculation a function $T(\phi(x))$ is defined as:

$$T(\phi(x)) = \int_0^{\phi(x)} n(\phi(x)) d\phi \quad (61)$$

which means Equation (60) can be rewritten as:

$$\phi'(x) = -\sqrt{\frac{2q}{\epsilon_{SC}} T(\phi(x)) + (\phi'(t_{SC}))^2}. \quad (62)$$

By resolving Equation (62) at the semiconductor-dielectric interface $\phi(x = 0) = \phi_0$, the electric field in the semiconductor at the interface (F_{SC_0}) can be calculated as:

$$F_{SC_0}(V_G) = \sqrt{\frac{2q}{\epsilon_{SC}} T(\phi_0(V_G)) + (\phi'(t_{SC}))^2}. \quad (63)$$

Next, conservation of displacement fields across the semiconductor-dielectric interface produces a relationship between the electric field in the semiconductor and the applied gate voltage using voltage drop approximation:

$$F_{SC_0} = \frac{C_{ins} V_G}{\epsilon_{SC}}. \quad (64)$$

From this the explicit function between $T(\phi_0(V_G))$ and V_G is:

$$V_G = \sqrt{1 + \delta} \sqrt{\frac{2q\epsilon_{SC}}{C_{ins}^2} T(\phi_0(V_G))} \quad (65)$$

where δ is given by:

$$\delta = \frac{C_{ins}^2 (\phi'(t_{SC}))^2}{2q\epsilon_{SC} T(\phi_0(V_G))}. \quad (66)$$

Making the approximation $\delta \ll 1$ simplifies Equation (65) to:

$$V_G = \sqrt{\frac{2q\epsilon_{SC}}{C_{ins}^2}} \sqrt{T(\phi_0(V_G))}. \quad (67)$$

By differentiating the gate voltage with respect to the interface potential we produce:

$$\frac{dV_G}{d\phi_0} = \sqrt{\frac{q\epsilon_{SC}}{2C_{ins}^2}} \frac{n_0(V_G)}{\sqrt{T(\phi_0(V_G))}}. \quad (68)$$

Combining Equations (67) and (68) to remove the function $T(\phi_0(V_G))$ gives:

$$\frac{dV_G}{d\phi_0} = \frac{q\epsilon_{SC}}{C_{ins}^2} \frac{n_0(V_G)}{V_G}. \quad (69)$$

These results will become useful after considering the drain current flowing through the TFT as a function of internal potential.

The drain current in the TFT is given by:

$$I_D(V_G) = \frac{V_D \mu_{CB} W}{L} \int_0^{t_{SC}} n_{CB}(\phi(V_G, x)) dx. \quad (70)$$

Here the assumption that the conduction band is a Heaviside function that is zero below the conduction band edge and single valued above the same edge is applied. Assuming the Fermi level is always below the conduction band energy, we can change this integral to:

$$I_D(V_G) = \frac{V_D \mu_{CB} W}{L} g_{CB_0} \beta e^{\beta(E_{CB} - E_{FB})} \int_0^{t_{SC}} e^{\beta\phi(V_G, x)} dx. \quad (71)$$

The term in front of the integral on the right hand side of Equation (71) can be redefined in terms of a single value of off current:

$$I_D(V_G) = \frac{I_{off}}{t_{SC}} \int_0^{t_{SC}} e^{\beta\phi(V_G, x)} dx. \quad (72)$$

The next two steps involve first subtracting 1 from either side of Equation (72) to avoid an artificial singularity caused by the thick film approximation. Then the integral over space is transformed to one over internal potential to give:

$$\frac{I_D(V_G)}{I_{off}} - 1 = \frac{1}{t_{SC}} \int_{\phi(0)}^{\phi(t_{SC})} \frac{(e^{\beta\phi(V_G, x)} - 1)}{\phi'(V_G, x)} d\phi. \quad (73)$$

By differentiating each side by ϕ , then resolving at the interface ($x = 0$) and utilizing Equation (62) this becomes:

$$\frac{1}{I_{off}} \frac{dI_D(V_G)}{d\phi_0(V_G)} = \sqrt{\frac{\epsilon_{SC}}{2qt_{SC}^2} \frac{(e^{\beta\phi_0(V_G)} - 1)}{\sqrt{T(\phi_0(V_G))}}} \quad (74)$$

where the differential can be split with respect to the gate voltage:

$$\frac{dI_D(V_G)}{dV_G} \frac{dV_G}{d\phi_0(V_G)} = I_{off} \sqrt{\frac{\epsilon_{SC}}{2qt_{SC}^2} \frac{(e^{\beta\phi_0(V_G)} - 1)}{\sqrt{T(\phi_0(V_G))}}} \quad (75)$$

Inserting Equation (68) into Equation (75) gives one of the three final required Equations for calculating the density of states from the transfer characteristics:

$$n_0(\phi_0(V_G)) = \frac{I_{off} C_{ins}}{qt_{SC}} \left(\frac{dI_D(V_G)}{dV_G} \right)^{-1} (e^{\beta\phi_0(V_G)} - 1). \quad (76)$$

Equation (76) gives the density of charge carriers at the interface as a function of the internal potential and the differential of drain current with respect to gate voltage. To use this, a relationship between the gate voltage and interface potential is required. This can be achieved using Equation (69) to replace the variable $n_0(\phi_0(V_G))$ in Equation (76). This leads to the integrals:

$$\frac{C_{inst_{SC}}}{I_{off}\epsilon_{SC}} \int_0^{V_G} V_G \frac{dI_D(V_G)}{dV_G} dV_G = \int_{\phi_0(0)}^{\phi_0(V_G)} (e^{\beta\phi_0(V_G)} - 1) d\phi_0 \quad (77)$$

which when solved gives:

$$\frac{C_{inst_{SC}}}{I_{off}\epsilon_{SC}k_B T} \left[V_G I_D(V_G) - \int_0^{V_G} I_D(V_G) dV_G \right] = e^{\phi_0(V_G)\beta} - \beta\phi_0(V_G) - 1 \quad (78)$$

where the left hand side consists of solely experimentally available data from a transfer characteristics which we can refer to as $W(V_G)$:

$$W(V_G) = e^{\phi_0(V_G)\beta} - \beta\phi_0(V_G) - 1. \quad (79)$$

The right hand side of Equation (78) cannot be solved numerically, but can be solved analytically. Therefore, by finding the value of ϕ_0 for each gate voltage point, ϕ_0 can be inserted back into Equation (76) to find $n_0(\phi_0(V_G))$.

Finally we can use the fact that the total number of occupied states is related to the density of states by a convolution to get:

$$n_{tot_0}(\phi_0(V_G)) = \int_{-\infty}^{\infty} g_{BG}(E) f(E - \phi_0(V_G)) dE \quad (80)$$

where $f(E - \phi_0(V_G))$ is the Fermi function. Equation (76) gives us the total number of filled accumulated states within the semiconductor, which is given by:

$$n_0(\phi_0(V_G)) = \int_{-\infty}^{\infty} g_{BG}(E)[f(E - \phi_0(V_G)) - f(E)] dE. \quad (81)$$

The difference between Equations (80) and (81) is that the accumulated charge defined by n from the beginning of this derivation only considers the built up charge, while n_{tot_0} considers all present charge carriers within the semiconductor. So to solve for $g_{BG}(E)$ we must deconvolute the number of carriers in bandgap states with the Fermi function.

4.2.2 Grünewald Analysis Scheme

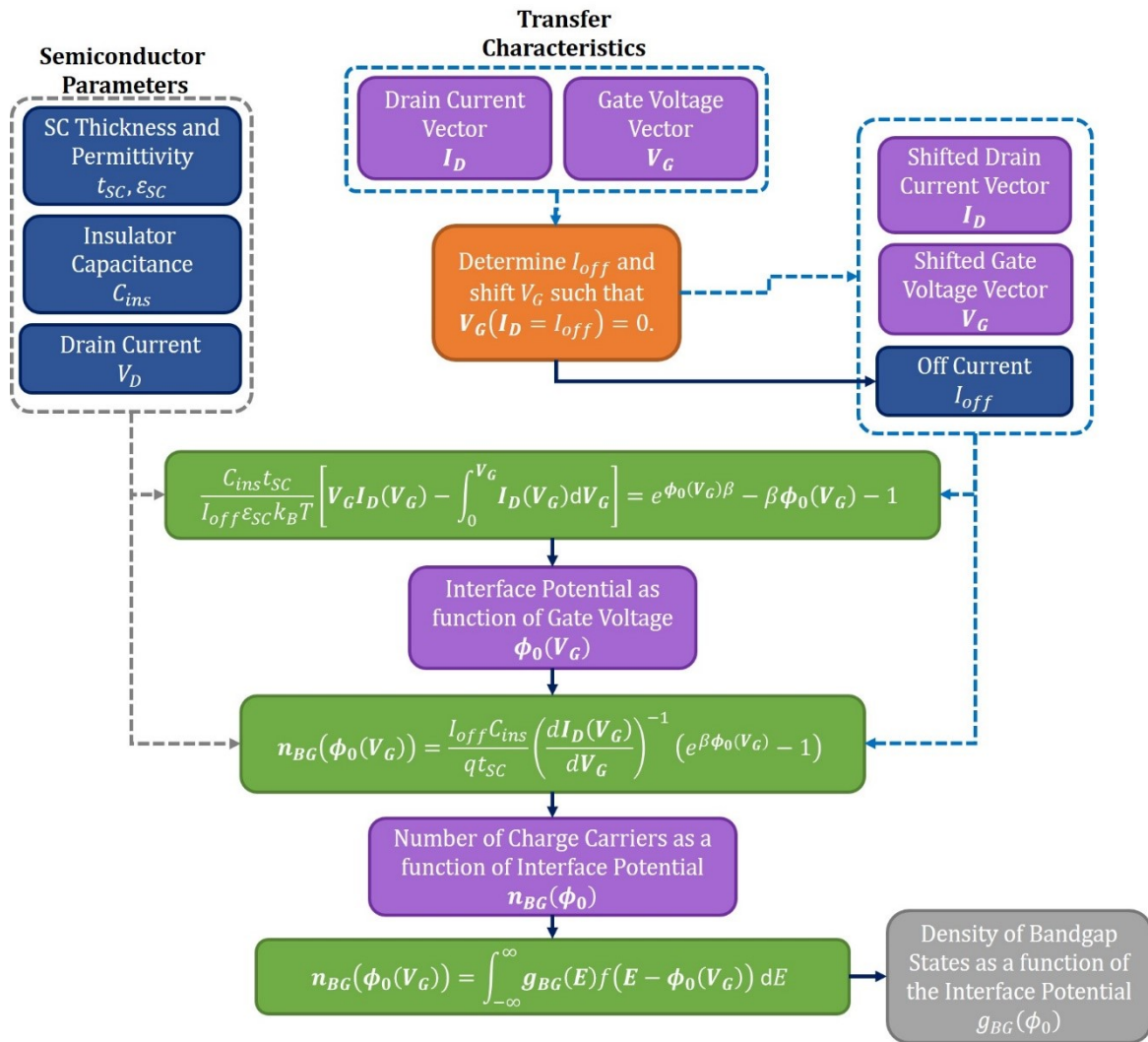


Figure 4.6: Evaluation scheme to calculate the density of bandgap states from experimental transfer characteristics and semiconductor parameters.

The first step to calculate the density of states using the Grünwald evaluation scheme is to shift the experimental data for gate voltage and drain current. The point of this is to shift the data such that the off current occurs when there is no applied gate voltage. Next, for each gate voltage point a corresponding surface potential needs to be calculated using Equation (78). From the surface potential, the total number of charge carriers for a specific surface potential can be calculated using Equation (76). The final step is to deconvolute the number of charge carriers for a specific surface potential with the Fermi function to produce the density of states. This whole process is illustrated within the flow diagram of **Figure 4.6**.

4.2.3 Deconvolution of the Density of States

The process of attaining the density of states from the number of charge carriers in those states requires a deconvolution of the data. Only numerical methods exist for performing a deconvolution, hence a scheme for deconvolution must be chosen.⁸⁸ This thesis shall report on the simplest and most commonly applied method.

The method starts with the assumption that the Fermi function is a Heaviside function centred at ϕ_0 . This assumption requires the approximation that in the Fermi function $k_B T \ll E - \phi_0$. From this the integral in Equation (80) can be rewritten as:

$$n_0(\phi_0(V_G)) = \int_0^{\phi_0} g_{BG}(E) dE \quad (82)$$

and by differentiating this with respect to the interface potential we get:

$$\frac{dn_0}{d\phi_0} = g_{BG}(\phi_0). \quad (83)$$

Hence, by simply differentiating the function of accumulated filled states by the surface potential, a solution for the density of states can be calculated. This deconvolution scheme breaks down at two points: firstly for values of g_{BG} where ϕ_0 is close to or less than $k_B T$, and secondly when ϕ_0 is within $k_B T$ of the conduction band. Also, it is poor at resolving fine features within the density of states. Studying further methods of deconvolution provides great scope for improving this analysis technique, especially with the modern computing power of even standalone pcs.

4.3 Applications of Grünewald Analysis

The Grünewald method for analysing bandgaps, or just bandgap analysis, requires multiple calculations on carefully input experimental data. To assist in this process, and as part of my work within my PhD, I developed a graphical user interface (GUI) using MATLAB to quickly take experimental data files from transistor probe stations and analyse the bandgap structure of the semiconductor. The GUI aided in auto-calculation of the off current and turn on voltage, required to prepare the gate voltage and drain current for analysis. It then allowed users to visually confirm correct alignment of these values, and to manually alter the data before analysis (if required).

The development of this code led to four collaborations during this PhD. This section shall outline the results gained from each analysis and describe how the results were interpreted. It shall contain only summaries of the work, focusing on the value added by analysing the bandgap of each structure. Although the code used to calculate the bandgap states was produced by the author as part of this thesis, the experimental results within this section were provided by colleagues within the Advanced Materials and Devices Group at Imperial College London and I was not involved with the experimental work. The discussions produced from these analyses are attributed equally to the author and collaborators.

4.3.1 CuSCN Bandgap Analysis

As part of the collaboration, the code developed as part of this PhD was applied to results gathered from solution processed copper thiocyanate (CuSCN) TFTs. The experimental work was performed by Dr. Pattanasattayavong et al. and was published in a 2015 report⁸⁹ (of which I am the second author). The results from this report pertaining to the bandgap analysis will be covered within this section.

CuSCN films were solution processed onto glass substrates with gold source/drain contacts. Either the commercial polymer dielectric CYTOP or the ferroelectric polymer poly(vinylidene fluoride-trifluoroethylene-chlorofluoroethylene) (P(VDF-TrFE-CFE)) was used as a dielectric layer. TFTs were then finished with a top gate of thermally evaporated aluminium. The inset (c) in **Figure 4.7** shows a simple schematic for the TFT structure. The TFTs produced were characterised at temperatures from 78 K to 300 K to study the temperature dependent charge transport through the CuSCN films.

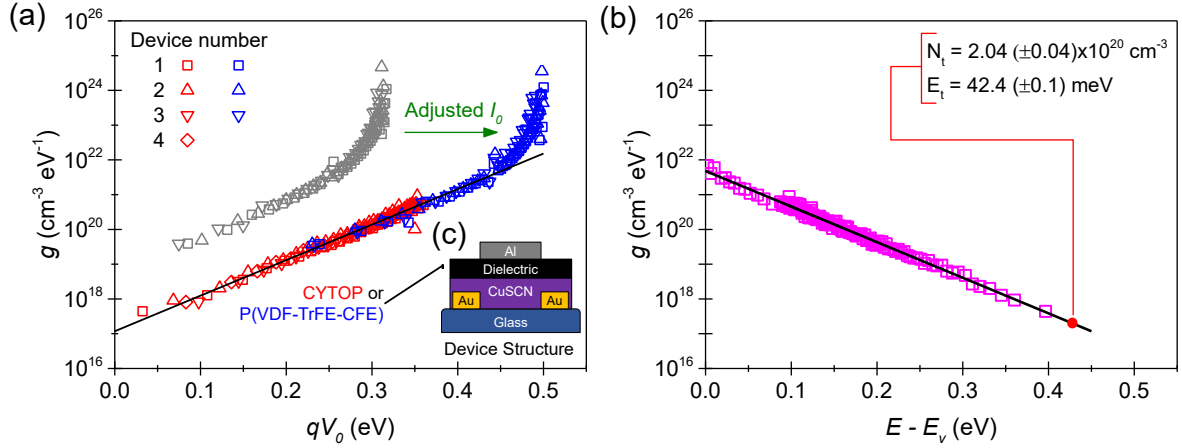


Figure 4.7: Density of bandgap states analysis of seven CuSCN films produced with the two dielectrics of CYTOP and P(VDF-TrFE-CFE) at room temperature. (a) Original results of the bandgap analysis of both CYTOP (in red) and original results of P(VDF-TrFE-CFE) (in grey). The P(VDF-TrFE-CFE) results are also shown when shifted (in blue) using the off-current of CYTOP devices to align with the CYTOP results. (b) The combined density of states replotted with respect to the valence band, and the characteristic energy and total DOS are shown. The inset (c) shows the device structure of the TFTs measured for this analysis. (Adapted and reprinted with permission from Pattanasattayavong et al.⁸⁹. Copyright 2015, Wiley-VCH.)

Initially a bandgap analysis was performed on the room temperature results of CuSCN TFTs produced with both CYTOP and P(VDF-TrFE-CFE). The resultant DOS are shown in (a) and (b) of **Figure 4.7**. This initial analysis produced two sets of states, one set for the four devices produced with CYTOP, and one for the 3 devices produced with P(VDF-TrFE-CFE). The difference in states was attributed to the fact that the bandgap analysis is highly sensitive to the off current (I_{off}) of the device. For the analysis to correctly calculate the absolute energy with respect to the Fermi level at equilibrium, the off current must be controlled by the lowest value of conduction. Often this value is masked by experimental effects such as the noise limit of the SMU or gate leakage through the dielectric. The thickness of the CYTOP layer was 900 nm with an $I_{off} = 10^{-12}$ A, while the thickness of the P(VDF-TrFE-CFE) was only around 220 nm with an $I_{off} = 10^{-9}$ A. This explains the shift in energy, visually seen as a greater number of states, for the P(VDF-TrFE-CFE) in **Figure 4.7** (a) in grey.

To counteract the gate leakage of the thinner P(VDF-TrFE-CFE) dielectric, an artificial off current was taken from the CYTOP layer and applied to the P(VDF-TrFE-CFE) linear characteristics. The newly calculated bandgap states were then plotted again and are shown in **Figure 4.7** (a) in blue. With this new value of off current the DOS for the P(VDF-TrFE-CFE) align

with those for CYTOP, extending to higher energies and densities. It is logical that the P(VDF-TrFE-CFE) DOS extends further towards and into the valence band. This is because the higher capacitance of the P(VDF-TrFE-CFE) dielectric will accumulate more charge, and therefore move the quasi Fermi level deeper into the valence band.

Within the continuous CYTOP and shifted P(VDF-TrFE-CFE) DOS (red and blue) results in **Figure 4.7** (a), a greater than exponential region can be seen starting at 0.45 eV. The values for the density of trap states at this point become unrealistic. We argue that this is due to the breakdown of the Grünwald model as the energy reaches the valence band. Though another possible cause is an increasing contact resistance at higher charge carrier densities. Assuming that the former is true, the data can be used to calculate the DOS as a function of energy from the valence band as shown in **Figure 4.7** (b). The points in **Figure 4.7** (b) follow a single exponential decay that can be fitted to the general expression:

$$g(E) = \frac{N_t}{E_t} \exp\left(-\frac{E}{E_t}\right) \quad (84)$$

where E_t is the characteristics energy of the trap states and N_t is the characteristic density of states. The ambiguity of the position of the valence band induces error into the value of N_t , but since E_t is calculated from the slope it is unaffected by an incorrectly positioned valence band edge.

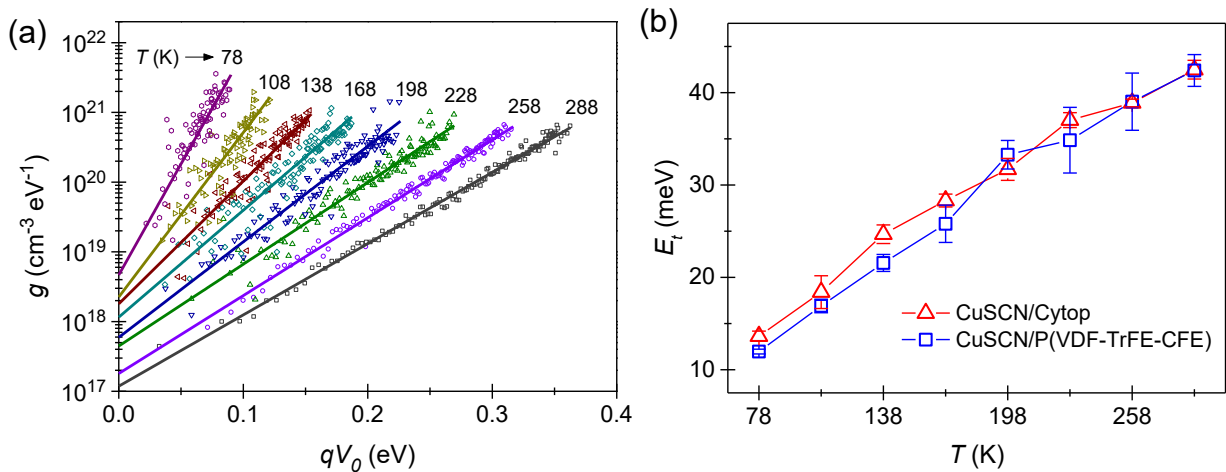


Figure 4.8: (a) The density of bandgap states at multiple temperatures calculated from CuSCN films produced with the dielectric CYTOP. Solid lines show the exponential fits to the DOS from which the characteristic energies of the trap states E_t were calculated. (b) The calculated E_t plotted for both CYTOP and P(VDF-TrFE-CFE) based devices. (Adapted and reprinted with permission from Pattanasattayavong et al.⁸⁹. Copyright 2015, Wiley-VCH.)

The characteristic energy of a system is an indicator of how quickly trap states decay from the valence band edge. A common assumption, used by temperature dependent data methods to calculate the bandgap states within a material,^{64,90-92} is that the bandgap states are temperature independent. This assumption is often unjustified, with reports explicitly showing the temperature dependence of bandgap states within certain materials^{93,94}. Therefore, to study the temperature dependence of the bandgap states within CuSCN, both CYTOP and P(VDF-TrFE-CFE) TFTs were measured at temperatures from 288 K to 78 K in decreasing steps of 30 K. The bandgap DOS were then calculated, with the results for the CYTOP devices shown in **Figure 4.8 (a)**.

The temperature independent assumption is shown to be faulty in **Figure 4.8 (a)**. This is evident in the sharper fall off in states and a higher maximum DOS for the same device measured at lower temperatures. This is indicative of thermal energetic broadening of localised states upon heating, a phenomenon also observed in the Urbach tails of hydrogenated a-Si⁹³. Exponential fits were made to both the data for the CuSCN/CYTOP device shown in **Figure 4.8 (a)** and identical temperature dependent data from CuSCN/ P(VDF-TrFE-CFE) devices (not shown here). From this the characteristic energy was extracted and plotted in **Figure 4.8 (b)**. The near identical characteristic energy as a function of temperature, shown in **Figure 4.8 (b)**, for CuSCN produced with two separate dielectrics leads us to believe that this is an intrinsic property of bandgap states within CuSCN. The linear nature of the temperature dependence of the characteristic trap energy, past a specific critical energy, is consistent with previous work on a-Si by G. Cody et al.⁹³. In it they conclude that this relationship is due to the high temperature approximation of the average thermal displacement of atoms from their equilibrium position.

4.3.2 Organic Blend Temperature Bandgap Analysis

This second collaboration consisted of the application of the code developed for bandgap analysis to a small molecule/polymer blend. The experimental work was performed by Dr Hunter et al. and culminated in the publication of a report in 2016⁹⁵ (of which I am the second author). Within this section, the key analysis from the report shall be summarized.

The report⁹⁵ studied blends of the small molecule 2,8-difluoro-5,11-bis(triethylsilylethynyl) anthradithiophene (diF-TES ADT) and the polymer poly(triarylamine) (PTAA). **Figure 4.9 (a)** contains the chemical structure of both blend components, along with a

schematic of the device structure used to produce TFTs. The blend composition is often referred to as one of the controlled parameters within the study, and is reported as the weight percentage (wt. %) of small molecule compared to polymer in the solution prior to deposition. Fabrication involved the spin casting of the blend onto glass substrates with thermally evaporated gold source drain contacts. Next, CYTOP was applied to act as a dielectric layer for TFT measurements, followed by a thermally evaporated aluminium gate contact. A full description of the fabrication of these devices can be found in the report by Hunter et al.⁹⁵.

First a 50 wt. % blend of small molecule to polymer TFT was measured at temperatures from 90 K – 320 K, and the linear transfer characteristics were used to calculate the bandgap DOS as shown in **Figure 4.9** (b). The results show the general trend of a decreasing decay rate at higher temperatures as seen within the work performed with Pattanasattayavong et al.⁸⁹ in Section 4.3.1. **Figure 4.9** (b) also contains two highlighted regions, the first in green is a greater than exponential region, where a single exponential fit would no longer provide an acceptable fit. The second region, highlighted in pink, demarcates where a rapid increase in the calculated density of states occurs. This, as with the similar feature at 0.45 eV within **Figure 4.7** (a), is assumed to be the breakdown of the analysis model as the quasi Fermi level approaches the valence band. Using the energy at the intersection of each temperature DOS with the pink box as the valence band mobility edge, the data was realigned and plotted as a function of distance from the valence band edge in **Figure 4.9** (c).

The same measurement performed on the 50 wt. % blend was also repeated for 30, 40, 60, and 70 wt. % blends, along with pristine diF-TES ADT and pristine PTAA TFTs. Using the fitting technique outlined in Section 4.3.1 by Pattanasattayavong et al.⁸⁹, a decay constant (E_0) was extracted from each blend composition at each measured temperature. The decay constant E_0 is identical to the characteristics trap energy E_t described by Pattanasattayavong et al.⁸⁹. The results for the temperature dependent decay constants for each blend composition are shown in **Figure 4.9** (d). As with the CuSCN devices in Section 4.3.1, the decay constant increases from low temperatures up to 250 K at which point it plateaus for all blend compositions. After 250 K, the activation energy is a function of blend composition with the decay constant increasing with increasing small molecule percentage.

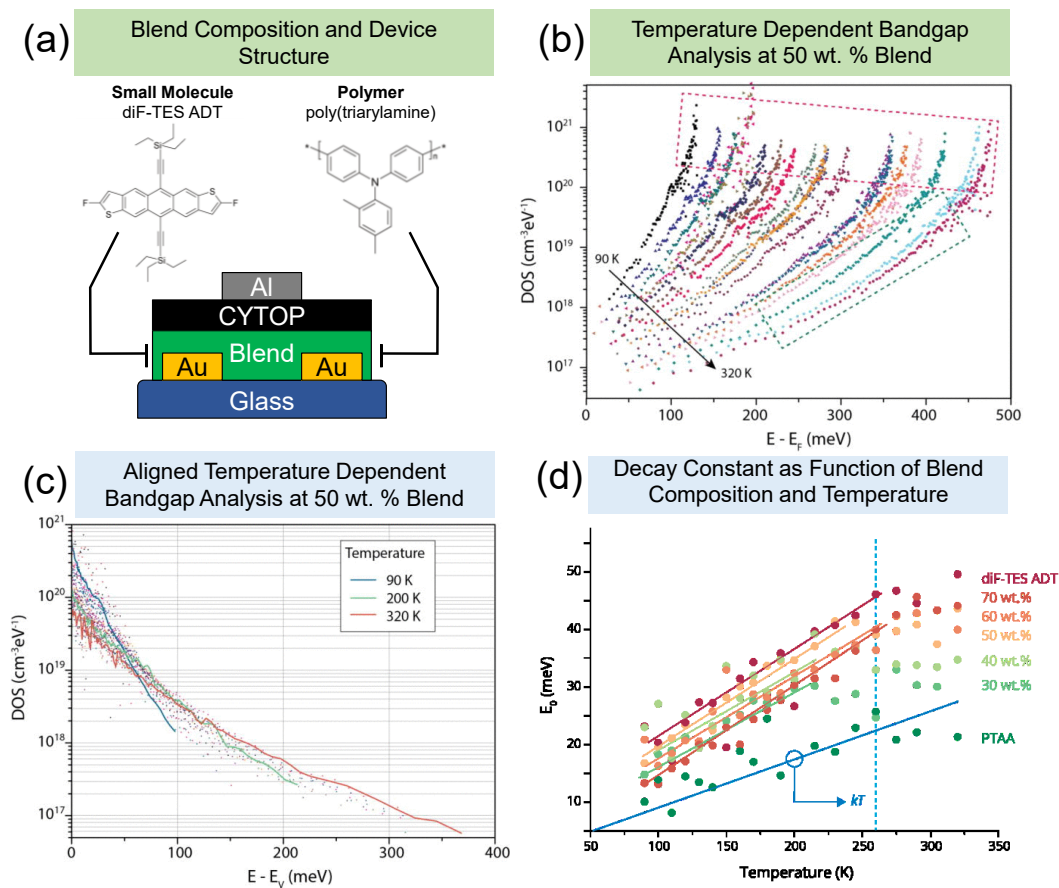


Figure 4.9: (a) The two components of the organic blend and the device structure used for transfer characteristic measurements. (b) Results of bandgap DOS analysis from a 50 wt. % blend TFT measured at temperatures from 90 – 320 K. The pink box highlights the region in which the analysis technique appears to breakdown, and the green box indicates where the DOS decay is greater than exponential. (c) The results from the 50 wt. % device aligned around the breakdown of the model, assumed to be the position of the valence band. (d) The decay constant as a function of temperature for multiple blend compositions between 90 – 320 K. (Adapted and reprinted with permission from Hunter et al.⁸⁹. Copyright 2016, AIP Publishing LLC.)

It has previously been reported that the highest mobility TFTs were produced by the 50 wt. % composition⁸⁰. Work by Smith et al.⁹⁶ shows that, as expected, the small molecule component has a much higher mobility than the polymer within a blend system. This leads to the expectation that a pure small molecule film will produce higher mobilities than any blend. An explanation for the peak mobility at a 50 wt. % blend is provided by previous work from Hunter et al.⁸⁰. In it they describe how the increased control in phase separation of the two components produces an entirely crystalline layer within the TFT channel at 50 wt. % without the cratering at higher concentrations of small molecule. Cratering will lead to a poor interface with the dielectric material, reducing the measured mobility of the semiconductor films. This

new bandgap analysis shows that the small molecule weight percentage controls the activation energy, with a roughly sigmoidal relationship (more detail of which can be found in the report). This mirrors the relationship between composition and effective mobility seen within previous studies⁸⁰.

In conclusion, TFTs produced from small molecule and polymer blends exhibit complex behaviour. The performance can be separated into two key figures of merit, the maximum mobility and the subthreshold slope. The maximum mobility is controlled by the intrinsic mobility of the small molecule component, but can be affected by morphological properties of the blend such as percolation pathways or cratering. The subthreshold slope is controlled by the bandgap trap states within the material, and this is what has been studied using the code produced as part of this thesis. Through analysis and discussion, we have concluded that the polymer exhibits a lower decay constant than the small molecule, with a roughly sigmoidal relationship between decay constant and blend wt. %.

4.3.3 Organic Blend Doping Analysis

This section shall report upon a collaboration with Dr. Paterson based on analysis of further organic small molecule/polymer blends and their subsequent p-type doping. Details on the fabrication and current characterisation of this system can be found in the 2016 report by Paterson et al.⁹⁷. The following analysis shall be part of a follow up report (of which I will be a co-author) on the same materials, providing further in-depth analysis of the electronic properties of the blend system.

Devices were fabricated by preparing a 25 to 75 wt. % solution of the small molecule 2,7-dioctyl[1]-benzothieno[3,2-b][1]benzothiophene (C₈-BTBT) with the polymer indacenodithiophene-benzothiadiazole (C₁₆IDT-BT) in 50:50 vol. solution of tetralin and chlorobenzene at 10 mg/ml. A mixed solvent is used due to the improved mobility as previously reported by Paterson et al.⁹⁷. To dope the blend the fluorinated fullerene derivative C₆₀F₄₈ was added in wt. % of 0, 0.05, 0.1, 0.5 and 1. Devices were produced on glass substrates with gold source/drain contacts using an inverted architecture. The dielectric poly[4,5-difluoro-2,2-bis(trifluoromethyl)-1,3-dioxole-co-tetrafluoroethylene] (PTFE AF 2400) was applied as an insulating layer, and an aluminium top contact was thermally evaporated as a gate contact. The overall structure is shown in the inset of **Figure 4.10** (c).

Linear transfer characteristics as shown in **Figure 4.10** (a) were measured for each of the 4 doped devices and the pristine control device. The 1 wt. % doped TFT exhibited an order of magnitude increase in drain current compared to the control TFT at -30 V onwards. There was also an increase in the off current for the two highest doping percentages. For the 0, 0.05 and 0.1 wt. % doped devices the off current was limited by the experimental noise floor of the measurement setup, hence leading to identical values of I_{off} .

It has already been noted in Section 4.3.1 how important the off current is in ensuring comparable bandgap DOS results between different linear characteristic measurements. The 0.5 and 1 wt. % doped blend TFTs definitely have an off current controlled by the minimum value of conductance available in the material. It is reasonable to expect that the relative energetic position of the bandgap density of states calculated from these linear transfer characteristics will be accurate (with respect to each other). The same cannot be assumed for the other three bandgaps calculated from the 0, 0.05 and 0.1 wt. % doped devices.

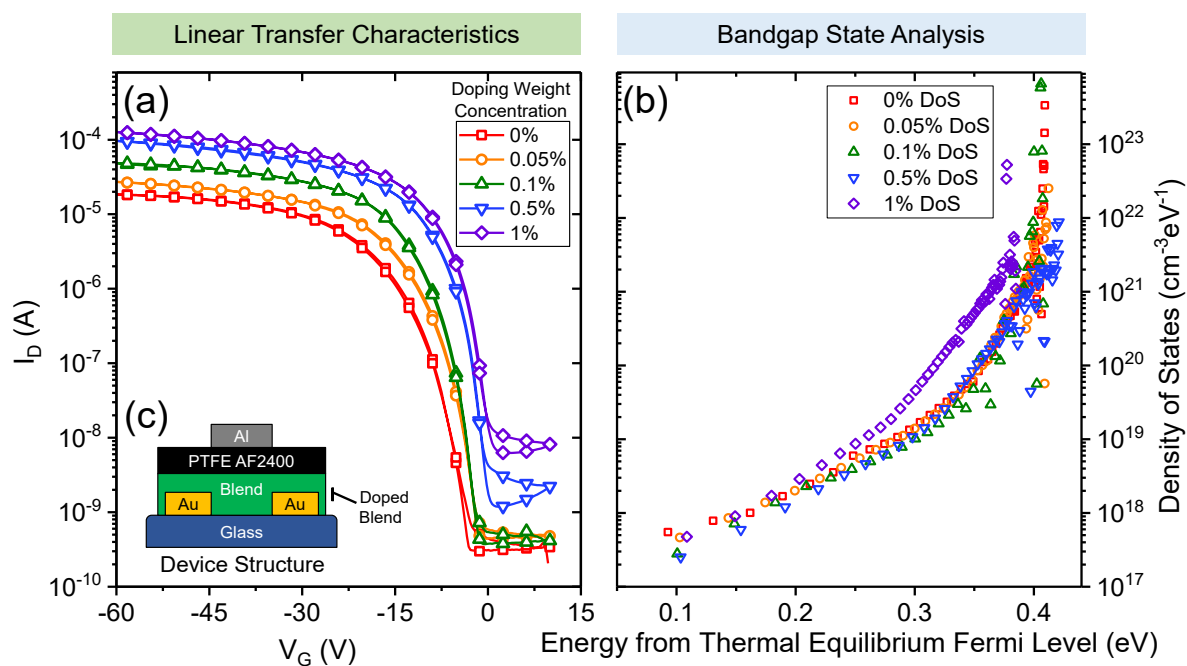


Figure 4.10: (a) Linear transfer characteristics of blend device at 5 doping concentrations from 0–1 wt. %. (b) Corresponding bandgap density of states calculated from the linear transfer characteristics of the 5 doping concentrations. Inset (c) shows the device structure of the TFTs measured.

The bandgap analyses of the linear characteristics are shown in **Figure 4.10** (b). The results for all doping densities overlap, except for the 1 wt. % doped blend. The 1 wt. % doped blend is shifted energetically and with a small additional increase in the number of states when

compared to the other calculated bandgap DOS. Without the 0.5 wt. % doped blend, it would be hard to conclude if the absolute energetic positions of the 0, 0.01 and 0.05 wt. % were accurate. As previously explained, the 0.5 wt. % doped blend definitely has an I_{off} controlled by bulk conduction in the channel, as it is above both gate leakage currents and the experimental noise floor. Since the 0.5 wt. % doped blend is aligned with all lower doping percentages, this indicates that any difference between 0.5 wt % and the lower percentages is too small to measure.

Though not shown, as the work was neither performed nor analysed as part of this thesis, the values of linear and saturation mobility exhibited a general increase in mobility upon doping. Average mobilities from 10 devices increased from $\sim 1 \text{ cm}^2/\text{Vs}$ for undoped device to $\sim 8 \text{ cm}^2/\text{Vs}$ for the 1 wt. % doped device. It was also noted that the shape of the linear mobility as a function of gate voltage was not indicative of fully ohmic contacts, though not dramatically so. This potential increase in contact resistance at more negative gate voltages could lead to the sharp increase in states seen closer towards the valence band in **Figure 4.10** (b). The increasing on-current upon addition of the dopant can be directly linked to a doping effect. This is because the effective mobility measured would be higher due to the ratio of mobile to immobile charge carriers.

In conclusion, one of three situations could be occurring for the 0.5 wt. % and lower blends. The first hypothesis is that doping is occurring and moving the Fermi level closer to the valence band, but it is too small to be calculated through this analysis. The second hypothesis is that for small doping concentrations the shift in the Fermi level is negligible, but the mobility is being enhanced leading to the higher drain currents. The final, third, hypothesis is that there is both doping and an enhancement to mobility being produced by low level doping percentages. For the third hypothesis, like the first hypothesis, the shift due to doping would have be too small to measure. Finally, the 1 wt. % doping ratio exhibited a combination of a Fermi shift, indicative of p-type doping, and also an increase in the density of states. The Fermi shift is concluded due to the large displacement between the 1 wt. % ratio and all other results. Why the extra states only become apparent at the 1 wt. % doping concentration is unclear though, and hard to calculate, as the total number of states present is the integral of the DOS over all energy.

4.3.4 In₂O₃ Thickness Bandgap Analysis

The final application of a bandgap analysis was produced as a collaboration with Dr. Isakov. A paper containing this analysis is currently in progress which will report on the origins of thickness dependent mobility in ultra-thin spray-coated indium oxide (In₂O₃) (for which I will be a co-author). The work focuses specifically on In₂O₃ films produced via spray coating, at thicknesses of 15 nm and less. Previous work focused on optimizing the fabrication techniques used for this continued work can be found in the 2015 study by Faber et al.²².

Devices were fabricated from 30 mg/ml solutions of indium nitrate hydrate in deionized water. The solution was spray coated onto SiO₂/Si⁺⁺ substrates (with a SiO₂ thickness of 100 nm) heated to 250 °C. Four devices were produced using 16, 32, 48 and 64 spray passes, and the thicknesses of the In₂O₃ films produced was obtained via ellipsometry. Finally, devices were completed with evaporated aluminium source/drain contacts to produce the structure shown in inset (c) of **Figure 4.11**.

The linear transfer characteristics of the four In₂O₃ TFTs of varying semiconductor thickness is shown in **Figure 4.11** (a). It should be noted that although the device widths for these transistors were identical, the device lengths did vary. Although not included, as the work was not performed as part of this thesis or directly relevant to the analysis, the AFM topography images of the 2.7 nm films were extremely rough and formed incomplete films. Likely due to the rough and uneven coverage, the 2.7 nm In₂O₃ film did not produce standard functioning TFTs, with occasional negative differentials in the drain current. This instable result is expected to produce negative values and large oscillations within the DOS calculated by bandgap state analysis.

Next a comparison should be drawn between the off-currents of the 7 nm In₂O₃ film and those of the 11 and 15 nm films. The off-current for each of the three devices is set by a combination of the conductivity and the gate leakage of the 100 nm SiO₂ layer. The reason why it cannot be attributed to one or the other is because the more conductive the semiconductor film, the easier for charge to be laterally transported across the film, and hence the larger the area available for gate leakage to occur through. This interplay between the conductance of the semiconductor and the gate leakage current will complicate interpretation of any potential energy shift that may be seen in the bandgap DOS upon calculation. Mobility extraction from the transfer characteristics exhibited a trend of increasing mobility with device thickness,

levelling off at < 10 nm. For sub 3 nm thick films the mobility was less than unity, varying from $\sim 0.001 - 0.5 \text{ cm}^2/\text{Vs}$. This increased to $\sim 40 \text{ cm}^2/\text{Vs}$ for 10 nm thick films of In_2O_3 , after which the mobility became independent of thickness.

Next the bandgap analysis was performed on the linear transfer characteristics shown in **Figure 4.11** (a), and DOS were plotted in **Figure 4.11** (b). The results for the 2.7 nm thick In_2O_3 film (red squares in **Figure 4.11** (b)) are as expected, with a larger than usual number of negative points (not shown due to the logarithmic axis), and large oscillations. This is a result of both the poor-quality data being used for the analysis and the fact that such a thin film breaks the thick film approximation used by the Grünewald analysis as described in Section 4.1.2.

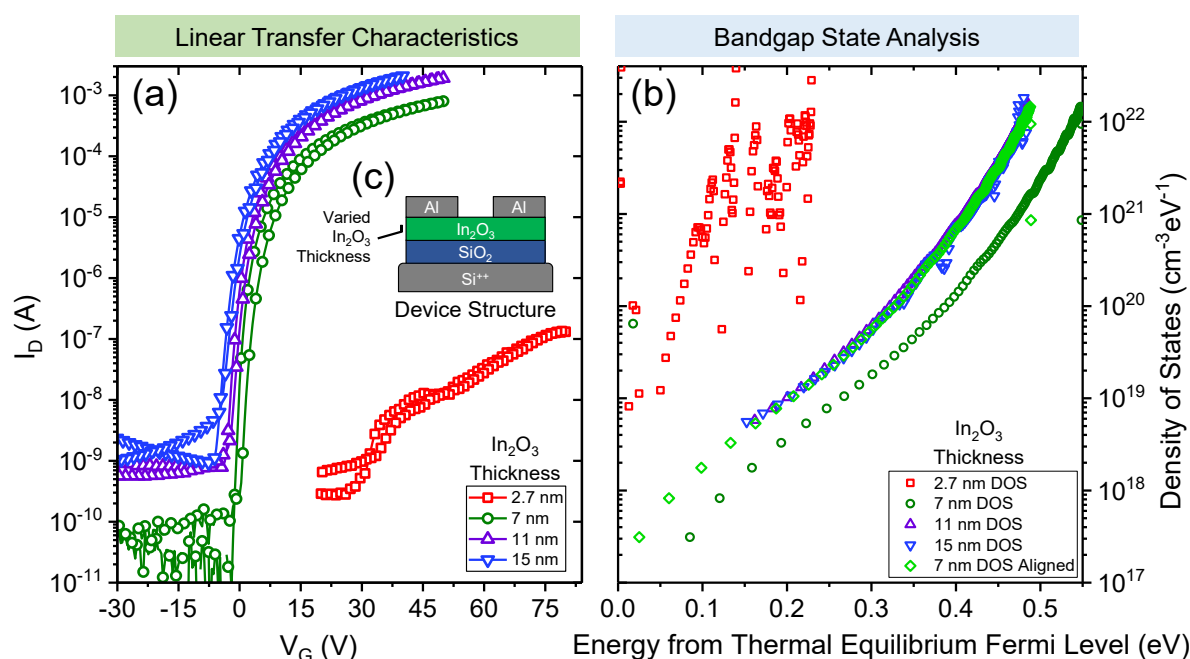


Figure 4.11: (a) Linear transfer characteristics ($V_D = 5 \text{ V}$) of In_2O_3 layers of thickness 2.7 nm to 15 nm. TFT width was $1000 \mu\text{m}$ for all thicknesses, but lengths were $30 \mu\text{m}$, $100 \mu\text{m}$, $80 \mu\text{m}$ and $80 \mu\text{m}$ for the 2.7 nm, 7 nm, 11 nm and 15 nm film respectively. (b) The corresponding bandgap density of states for each semiconductor thickness. The inset (c) shows the device structure used for these measurements and subsequent analysis.

The 7 nm thick In_2O_3 film has been plotted twice, first using the original values of energy above the equilibrium Fermi level (dark green circles **Figure 4.11** (b)). The second plotting of the 7 nm results was performed after the data had been shifted (light green diamonds **Figure 4.11** (b)) to align with the 11 and 15 nm thick In_2O_3 films DOS. Upon alignment, the similarity between the 7, 11, and 15 nm thick In_2O_3 films DOS becomes obvious. The only deviation in results are small regions of noise in the 15 nm DOS results (blue downward facing triangles

Figure 4.11 (b)) which are attributed the SMU automatically switching between different current ranges during the measurement causing small jumps in the drain current.

To summarize, the bandgap analysis model has shown that the density of trap states within In_2O_3 films is independent of the layer thickness. This allows an important conclusion to be drawn about the semiconductor thickness dependence of mobility. The analysis allows us to rule out trap states increasing at lower film thicknesses as a cause of decreased mobility and hence focus on other possible mechanisms such as surface roughness scattering.

4.3.5 Application of the Bandgap Analysis Summary

A few fundamental precautions have been necessary when applying this analysis code and evaluating the data produced. Also, from the data it has been applied to, a few key results can be concluded. These precautions and results are listed below.

1) **Complimentary Technique**

The bandgap analysis is a complimentary technique and produces little useful information from a single device. It is best applied to a series of similar devices with a single changing variable (temperature, dielectric, doping conc.), which removes the importance of absolute values. Using this technique should focus on finding trends cross-referenced with other experimental results.

2) **Off-Current Sensitive**

The absolute value of energy of the density of states is calculated from the Fermi level at equilibrium. This is the work function of the semiconductor if there is no band bending, a value which is extremely hard to experimentally measure. The bandgap states analysis extrapolates this value from the off current and the turn on voltage. Hence the absolute value of energy can be unreliable if the off current is not controlled by the minimum value of conduction achievable in the semiconductor.

3) **Dielectric Independent**

Identical devices made with only a change in dielectric should have similar bandgap density of states as long as the dielectric does not create a large amount of interfacial trap states and does not affect the growth of the semiconductor. This result is seen both in CuSCN within Section 4.3.1 and later in this thesis with In_2O_3 films produced on various metal oxide dielectrics in Section 6.4.5. But, differences in leakage current

and dielectric dipoles present in the dielectric, can lead to shifts in the calculated energy positions of the dielectric density of states as discussed in the previous conclusion point.

4) **Thickness Independent**

The bandgap analysis calculates the DOS for the semiconductor under the assumption that it is a bulk property. From the results of Section 4.3.4 we can see that, after removing shifts likely due to mismatched off currents, the calculated number of bandgap states is independent of thickness as expected.

5) **Temperature Dependent**

Many other models used to calculate bandgap density of states from temperature dependent TFT measurements require the assumption the DOS is temperature independent. Within this work we have shown that for two separate material systems (CuSCN, and a small molecule/polymer blend) this assumption is false. In both cases, a shallower fall off in the bandgap DOS is seen at higher temperatures, implying that disorder is spreading the localised states to produce a broader tail at increased temperatures.

To conclude, the bandgap state analysis is a powerful tool for gaining greater information on the electronic structure of a material system able to form TFTs. Its strength lies in the simplicity with which large amounts of experimental data can be analysed. Yet its use must be treated with caution, as the absolute values of energy and DOS can be subject to error due to experimental conditions. Instead, it should be used to identify larger trends that other methods may not be able to such as the temperature dependence of bandgap states.

5 Dye-Sensitized In₂O₃ Phototransistors

Motivation for further research into photodetectors comes directly from their practical use. Recent advances in materials and fabrication techniques have led to complex and multifunctional devices including touch screens integrated with photodetectors⁹⁸, photosensitive screens⁹⁹ and RGB stacked pixel sensors¹⁰⁰. New photodetectors are therefore advancing in two orthogonal directions: the first striving to improve performance, and the second trying to expand the versatility and functionality of devices.

When considering the first direction of performance, the relevant metrics depend heavily on the application. Common requirements are high responsivity, high photosensitivity, stable performance and low noise levels. The relative importance of frequency response, absolute accuracy and power consumption is then specific to each practical application.

The second direction of increased versatility and functionality is where the field of solution processed semiconductors' strengths come forth. The second improvement direction can be split into the two categories of fabrication techniques, and unique device properties. Fabrication methods using additive techniques, low-temperature processes and solution deposition have the potential advantage of scalable low-cost manufacturing. While unique properties that could prove useful within future technologies are colour selectivity, device transparency and integrated gain mechanisms.

Considering this, an ideal new photodetector should have high-performance, flexibility in fabrication and unique characteristics. This chapter reports upon dye-sensitized In₂O₃ phototransistors exhibiting high levels of photosensitivity (10^6) and responsivity (2000 A/W) as published by Mottram et al.¹⁰¹ (for which I was the first author). In addition to high performance, the devices were fabricated at low temperatures (≤ 200 °C) using solution processing. Dye-sensitization of the In₂O₃ was shown to produce a preferential colour response to green light (~ 500 nm), while the In₂O₃/D102 bilayers produced remained highly transparent with > 92 % transmission in the wavelength range of 400–700 nm.

5.1 Introduction to Phototransistors

There exist multiple possible structures for a photodetector. The simplest photodetector is the photoconductor which uses a single material, sandwiched between two contacts, whose

conductivity is altered directly upon illumination. The photoconductor differs from a photodiode as the photodiode bilayer's mismatch in energy levels produces an electric potential upon illumination that is not present in a photoconductor. Therefore, the photoconductor relies solely on an externally applied voltage, and consequently external power, to make a measurement. On the other hand, the in-built potential produced by a photodiode upon illumination allows it to power itself dependent on the mode of operation.

A phototransistor's operation is highly dependent on the transistor structure, but for phototransistors based on TFTs, a comparison can easily be drawn with the photoconductor. In this scheme the incoming photons create charge carrier pairs within the semiconductor that separate under the applied source-drain voltage. The photogenerated carriers will continue to partake in charge transport increasing the TFT channel current until they recombine. Separate to this, the gate voltage can be used to control built up charge due to the field effect, modulating the current as in a standard TFT. From this simple description, it is reasonable to expect that the effect of increasing illumination on transfer characteristics of a TFT would lead to an increase of the off current. This is because the photoinduced charge will only be evident when it is equal to or greater than the field effect induced charge.

Currently this description has ignored the potential localization of one of the photoinduced charge pairs, assuming both may move freely for a limited amount of time. If instead, a charge carrier pair is produced where one of the charges is spatially fixed, illumination could induce photodoping, leading to a shift in the whole transfer characteristics.

5.1.1 Figures of Merit

There are multiple figures of merit to compare the performance of photodetectors, the two most important of these are the photosensitivity (PS) and responsivity (R). The photosensitivity is defined as the ratio of the increase in device current to the current under dark conditions. Therefore, the photosensitivity is given by:

$$PS = \frac{I_{illum} - I_{dark}}{I_{dark}} \quad (85)$$

where I_{illum} and I_{dark} are the drain currents under illumination and in dark conditions, respectively.

The photosensitivity gives a good measure of how a sensor will function in an active device, with external circuitry to provide gain. Where it fails is its lack of normalization to the incoming light intensity, reducing its use for comparing two devices with different applied illumination power. This is where the responsivity becomes of use, defined as the change in current upon illumination normalized to the incident light power:

$$R = \frac{I_{illum} - I_{dark}}{P_{illum}} \quad (86)$$

where P_{illum} is the illuminating power. The responsivity is defined by the incident light power as opposed to the irradiance; the latter being defined as the incident light power per unit area. Because of this, responsivity is often favourable to devices with small active areas, where the lower illuminating power will produce a larger responsivity for an equal change in current.

Both the responsivity and photosensitivity of a phototransistor are expected to be a function of both the applied gate voltage as well as the wavelength of incident light. If the optoelectronic response of a device is linear to incident light power a single value of responsivity will correspond to all illuminating intensities. This is not to be expected by any device that uses inbuilt gain mechanisms to amplify the signal such as a phototransistor.

5.1.2 State-of-the-Art Phototransistors

In order to understand quantitatively the current state of the field of phototransistors, a review was undertaken of modern devices for which values of photosensitivity and responsivity were published (or calculable from published data). The result of this review can be seen in **Table 5.1**. The devices have been categorized by the technology that they are based upon, being either: conventional e.g. Si or Ge; organic e.g. small molecule or polymer; low-dimensional (Low Dim) e.g. nanowires or flake based; quantum dots (QD); or dye-sensitized films as reported in this thesis. It is important to note that the photosensitivity and responsivity for these devices may be reported for different operating conditions, for example extracted at two separate gate voltages. Graphically the results of **Table 5.1** are shown within **Figure 5.1** with the number next to each point corresponding to the labelling number in the table.

There are a few stand out points within **Figure 5.1**. First, as mentioned in Section 5.1.1, low-dimensional devices dominate the high responsivity regime. This is due to the extremely small active areas of the devices inflating the value of responsivity even when only small currents

are being measured. Also of importance is device 21, which was developed by Pattanasattayavong et al.³³ using a ZnO transistor dyed with the small organic molecule D102. This device had both an ultra-high photosensitivity and responsivity and acted as a foundation for the work reported here.

Table 5.1: List of state-of-the-art photodetectors based on phototransistor structures and their maximum values of photosensitivity and responsivity. “Low Dim” is used to refer to low-dimensional devices (such as graphene or nanowires) and “QD” is used to indicate quantum dots.

#	Device Type	Publication Year	Photo-sensitivity	Responsivity (A/W)	Experimental Wavelength	Ref.
1	Conventional	1984	1×10^6	300	Green 550 nm	102
2	Conventional	2008	12.6 [†]	2	IR 1550 nm	103
3	Conventional	2011	$\sim 7^*$	35	Red 630 nm	104
4	Organic	2005	2.05×10^5	82	UV 340 nm	105
5	Organic	2005	50	1.3×10^5	UV 365 nm	106
6	Organic	2008	4×10^3	4300	NUV 436 nm	107
7	Organic	2009	800	1000	White Light	108
8	Organic	2012	7.3×10^4	0.761	Unstated	109
9	Organic	2013	$\sim 50 \times 10^6^*$	5×10^5	NIR 800 nm	110
10	Organic, QD	2012	2×10^4	2×10^4	NIR 895 nm	111
11	Low Dim	2012	1×10^3	0.12 [*]	Red 630 nm	112
12	Low Dim	2013	$\sim 30^*$	800	Green 561 nm	113
13	Low Dim	2013	0.17 [*]	5×10^8	Red 635 nm	114
14	Low Dim	2014	$\sim 1 \times 10^{3^*}$	97.1	Green 532 nm	115
15	Low Dim	2014	600	0.27	Red 630 nm	116
16	Low Dim	2014	$\sim 4 \times 10^6^*$	1.06×10^7	Red 633 nm	117
17	Low Dim	2014	0.06 [*]	10	Red 632.8 nm	118
18	Low Dim	2014	10	157	Red 633 nm	119
19	Low Dim, QD	2012	$\sim 0.3^*$	2×10^4	NIR 895 nm	120
20	Low Dim, QD	2013	$\sim 0.04^*$	4×10^7	IR 1040 nm	121
21	Dye-sensitized	2012	1×10^6	1×10^4	Green 522 nm	33
22	Dye-sensitized	2016	1×10^6	3.9×10^3	Green 500 nm	101

*Value taken from figure within the publication

†Value calculated from other data within the publication

One advantage of the phototransistors demonstrated by Pattanasattayavong et al.³³ is the modularity of their design. The ZnO transistor could be replaced with any semiconductor as long as the surface is compatible with the selected dye. This means, instead of using sprayed ZnO processed at temperatures of up to 300 °C, a lower temperature semiconductor can be substituted.

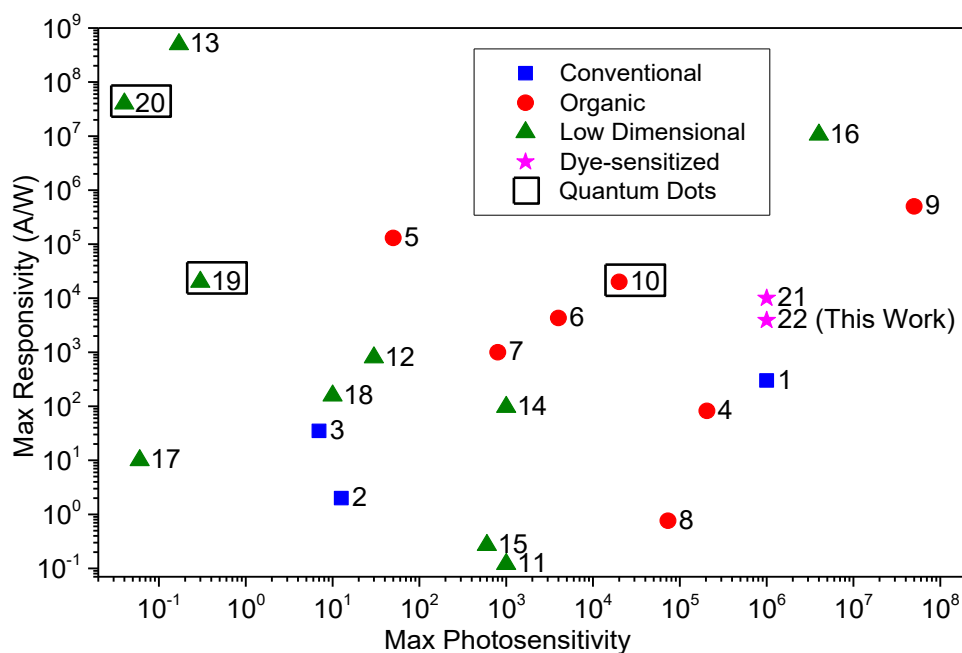


Figure 5.1: Values of maximum photosensitivity and responsivity reported to date for multiple transistor-based photodetectors from **Table 5.1**. References for each device are within **Table 5.1**. (Adapted with permission from Mottram et al.¹⁰¹. Copyright 2016 American Chemical Society.)

5.2 Device Structures

Within this work four device structures were produced as shown **Figure 5.2**. The first two structures in **Figure 5.2** were In₂O₃ films and bilayers of D102 dye-sensitized In₂O₃, respectively produced on quartz substrates for UV-Vis spectroscopy measurements. The second set of structures in **Figure 5.2** were control In₂O₃ TFTs and D102 dye-sensitized In₂O₃ TFTs, used in all other measurements. These were produced on 400 nm thick silicon dioxide (SiO₂) with a geometric capacitance of 8.6 nF/cm², thermally grown on highly doped silicon wafers. These acted as the TFT dielectric and gate contact in turn. All device fabrication and characterisation in this Chapter was performed by the author.

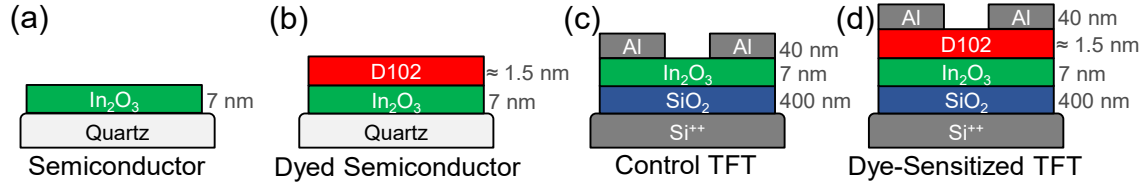


Figure 5.2: Device structures of (a) the In_2O_3 sample and (b) the dyed In_2O_3 samples used for UV-Vis spectroscopy. Next (c) the transistor structure used as a control and (d) the phototransistor structure tested for optoelectronic properties.

5.2.1 Device Fabrication

Before use, all substrates were cleaned in deionized water, acetone and IPA using an ultrasonic bath for 10 mins each. This was followed by a UV-ozone treatment of 20 mins to improve wettability of the surface. Next the substrates were treated with HMDS around the edges as described in Section 2.1.3 to reduce parasitic gate leakage over the edge of the dielectric.

To fabricate the In_2O_3 layers, a solution was produced by dissolving anhydrous indium nitrate [$\text{In}(\text{NO}_3)_3$] in deionized water at a concentration of 40 mg/ml. The semiconductor solution was then left to stir at room temperature for 1 h before use. Finally the solution was deposited via spin-casting onto the relevant substrates (quartz or $\text{SiO}_2/\text{Si}^{++}$) at 4000 rpm for 30 s, followed by a 2 h thermal anneal at 200 °C to produce the In_2O_3 layers.

Dye-sensitization of In_2O_3 films was achieved by immersing substrates, with freshly applied In_2O_3 films, for 1 min in a solution of D102 in a 50:50 vol. % mix of acetonitrile and tert-butanol at a concentration of 0.8 mM. Excess dye was then rinsed off using deionized water and afterwards the samples were dried with a nitrogen gun. The single layer devices of pristine In_2O_3 on quartz and the control TFT were left untreated during the dying process.

Finally, to produce the In_2O_3 and $\text{In}_2\text{O}_3/\text{D102}$ bilayer phototransistors, aluminium source-drain contacts were thermally evaporated. The aluminium was evaporated at a rate of 1 Å/s through shadow masks to produce TFTs of length and width 50 μm and 1000 μm , respectively.

5.3 Film Characterisation and Functionalization

Initially the surfaces and cross-sections of the pristine In_2O_3 and $\text{In}_2\text{O}_3/\text{D102}$ bilayers were studied with different techniques. This was done firstly to confirm the presence of the dye upon

functionalization and then to investigate the potential change in the topography of the In_2O_3 surface after functionalization.

5.3.1 Cross-Sectional TEM

Samples of the pristine In_2O_3 films on $\text{SiO}_2/\text{Si}^{++}$ were studied using high-resolution cross-sectional TEM performed by Dr. Kui Zhao and Prof. Aram Amassian at King Abdullah's University of Science and Technology (KAUST) and described in Section 2.3.2. The results are provided in **Figure 5.3** and demonstrate the highly polycrystalline nature of the fabricated In_2O_3 films. Furthermore, the films are ultra-thin with an average thickness of 7 nm, and a uniform distribution. The ultra-thin nature of these films is extremely promising, as the dyed surface of the bilayer will be extremely close to the active channel of the TFT.

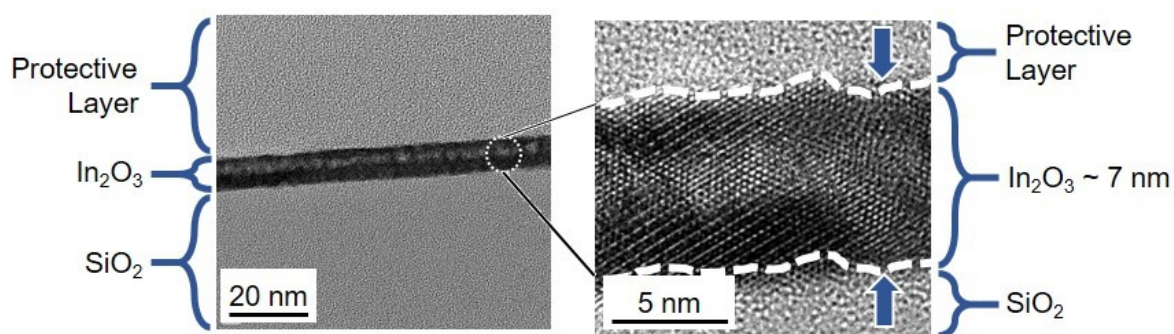


Figure 5.3: High-resolution cross-sectional TEM images of In_2O_3 films produced on silicon dioxide with a protective top layer for imaging. (Adapted with permission from Mottram et al.¹⁰¹. Copyright 2016 American Chemical Society.)

5.3.2 UV-Vis Spectroscopy

The prepared pristine In_2O_3 samples and $\text{In}_2\text{O}_3/\text{D102}$ bilayer samples produced on quartz were measured using UV-Vis spectroscopy. Details of the spectrometer are in Section 2.2.1. First a cleaned quartz substrate was measured to establish an absorption baseline. Next the pristine In_2O_3 and $\text{In}_2\text{O}_3/\text{D102}$ bilayer samples were measured. The quartz baseline was removed and the resulting absorbance for pristine In_2O_3 (black) and $\text{In}_2\text{O}_3/\text{D102}$ bilayer (red) samples can be seen in **Figure 5.4**. These two samples have been normalized to the maximum value of both measurements, hence maintaining relative amplitude between the two sets of results. Also within **Figure 5.4** is the effect of dye-sensitization (blue), calculated from the difference between pristine In_2O_3 and $\text{In}_2\text{O}_3/\text{D102}$ bilayer results, and normalized for illustration.

The results of **Figure 5.4** show that upon dye-sensitization a new peak of absorbance can be seen at ~ 500 nm. This corresponds well with the expected absorption peak of the dye D102³² indicating the successful deposition of the D102. Accompanying this peak is a general increase in the sub 400 nm absorbance, which is attributed to increased interband absorption. An important feature not shown is the overall transmission of the bilayer film, which is very high at $> 92\%$ across all visible wavelengths. This means the active layer of these devices are highly transparent, absorbing only a fraction of incident light.

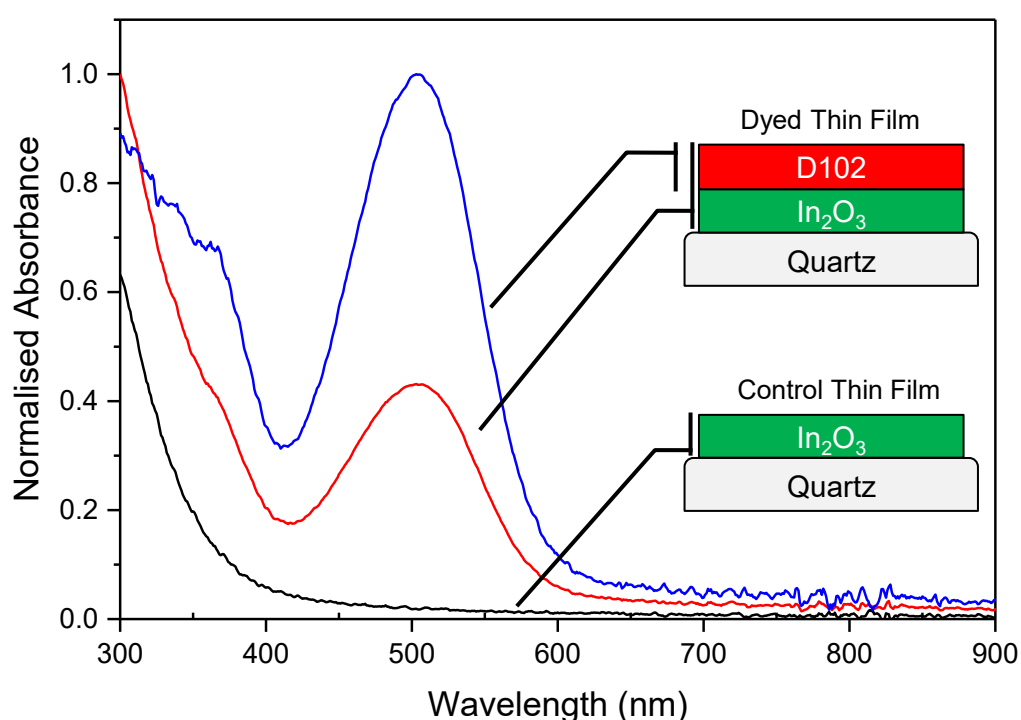


Figure 5.4: UV-vis spectroscopy results for an In₂O₃ film on quartz (black), along with a D102 dyed In₂O₃ film on quartz (red) and the difference between undyed and dyed films (blue). The In₂O₃ film (black), and D102 dyed In₂O₃ film (red) have been normalized together so that the relative values of absorbance are maintained. (Adapted with permission from Mottram et al.¹⁰¹. Copyright 2016 American Chemical Society.)

On quartz substrates, the completeness of the dye coverage of the In₂O₃ is apparent visibly across the whole of the substrate. In addition, the absorbance of the bilayer was independent of immersion time during the dyeing process. These two observations lead us to believe that we have complete coverage of the D102 dye on the In₂O₃ films, both produced on quartz and on SiO₂/Si⁺⁺.

5.3.3 Surface Topography

In order to identify possible conglomeration of the D102 dye on the In_2O_3 surface AC-AFM topography imaging, as described in Section 2.3.1, was performed. The resulting ($0.5 \mu\text{m} \times 0.5 \mu\text{m}$) topography images, height distributions and chemical structure of the D102 dye are shown in **Figure 5.5**. Visually the topography image of pristine In_2O_3 and the bilayer film are extremely similar. This is confirmed quantitatively by both the similar height distribution plots of the pristine and bilayer devices and the comparable surface root-mean-squared (RMS) roughness of both devices at $\sim 0.2 \text{ nm}$. Due to these observations there is strong evidence that the D102 produces a molecularly thin layer on the In_2O_3 surface without any apparent conglomeration.

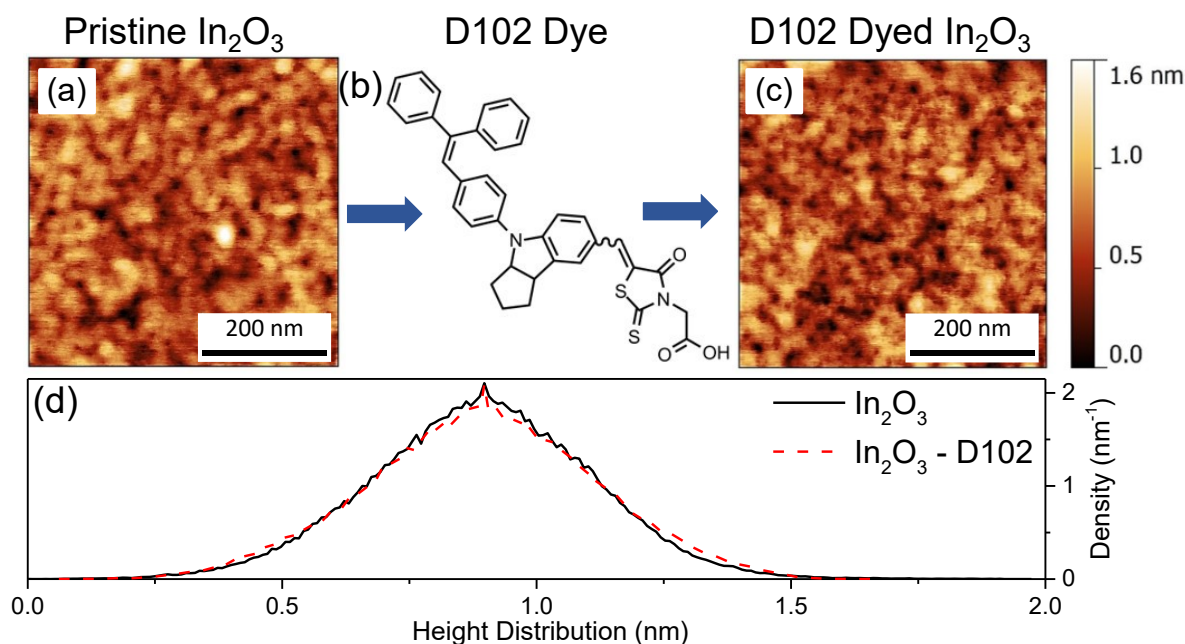


Figure 5.5: Surface topography of (a) pristine In_2O_3 before being functionalized and (c) after functionalization with (b) the small molecule dye D102. The graph (d) shows the similarities in height distribution for both (a) the undyed surface and (c) the dyed surface. (Adapted with permission from Mottram et al.¹⁰¹. Copyright 2016 American Chemical Society.)

5.4 Optoelectronic Characterisation

The primary methodology for testing the optoelectronic properties of the control and dye-sensitized phototransistors is outlined in Section 2.4.2. The results of which are included in **Figure 5.6**, which shows the transfer characteristics response of the control TFT (schematically illustrated **Figure 5.6** (a)) and dyed TFT (schematically illustrated **Figure 5.6** (b)) to three

separate LEDs. The method can be summarized as six transfer characteristic measurements performed in dark (the black lines in **Figure 5.6** (c)-(h)) and with the following currents, 1 mA, 5 mA, 10 mA, 50 mA and 100 mA, flowing through the selected LED. V_G was swept from negative to positive voltages, and back, though for clarity only the forward sweep is shown since hysteresis was minimal. The process was repeated on both the control and dye-sensitized phototransistors for each of the three LEDs (red, green and blue), the spectra of which can be found in **Figure 5.6** (i). The illumination intensity of each LED colour for each current can be seen in the legend of **Figure 5.7**. The LEDs are positioned such that the whole substrate, containing multiple TFT source/drain contacts, is fully and homogeneously illuminated. This does lead to an increase in parasitic edge effects as well as bulk conductance. It is well known that there are large variations in the operating characteristics of transistors, specifically the turn-on voltages (V_{on}) and threshold voltages (V_{Th}).^{122,123} These variations are often attributed to ambient conditions, such as humidity and the oxygen content of air, hence measurements were all undertaken in an inert atmosphere of nitrogen.¹²⁴

The results of the optoelectronic transfer measurements are displayed in **Figure 5.6** (c)-(h). The first conclusion from **Figure 5.6** (c)-(h) is that functionalizing the In_2O_3 surface with D102 does not cause any key change in the operation of the transistors. This is seen in the dark transfer characteristics of the control and D102 dyed-devices where the change after dyeing is less than the device-to-device variation for each structure. All devices also exhibited very similar electron mobilities of $\sim 1 \text{ cm}^2/\text{Vs}$.

The control TFT shows no response to red light (**Figure 5.6c**), a comparatively small response to green light (**Figure 5.6e**) and the biggest response to blue light (**Figure 5.6g**). The relative shifts in the transfer characteristics of the control TFTs to the different wavelength LEDs closely resembles the convolution of the LEDs EL spectra (**Figure 5.6i**) with the absorbance spectra of the In_2O_3 film (**Figure 5.4**). The photoresponse for the control TFT can be separated into two components: (i) an increase in the transistors off current (I_{off}) and (ii) a negative shift in the turn on voltage (V_{on}) of the transistors. The increase in the off current is more noticeable in response to blue light. It should be noted that for the two lowest level intensities of blue light the off currents are lower than the device under dark conditions. This was due to changes in the integration time (the time taken to measure current, especially needed to measure low currents) used during characterisation. For all other measurements, the lowest possible value of I_{off} was

controlled by the sensitivity of the semiconductor parameter analyzer used ($\sim 10^{-11}$ A). Therefore, an increase in I_{off} could only be observed if an illumination intensity caused the devices I_{off} to become greater than the noise floor of the semiconductor parameter analyser.

In comparison to the control TFT, the dye-sensitized transistor responded moderately to red light (**Figure 5.6 (d)**), with a large response to both green (**Figure 5.6 (f)**) and blue (**Figure 5.6 (h)**) light. As with the control TFT, the dye-sensitized transistor response consists of the two components of a negative shift in the V_{on} and an increase in I_{off} .

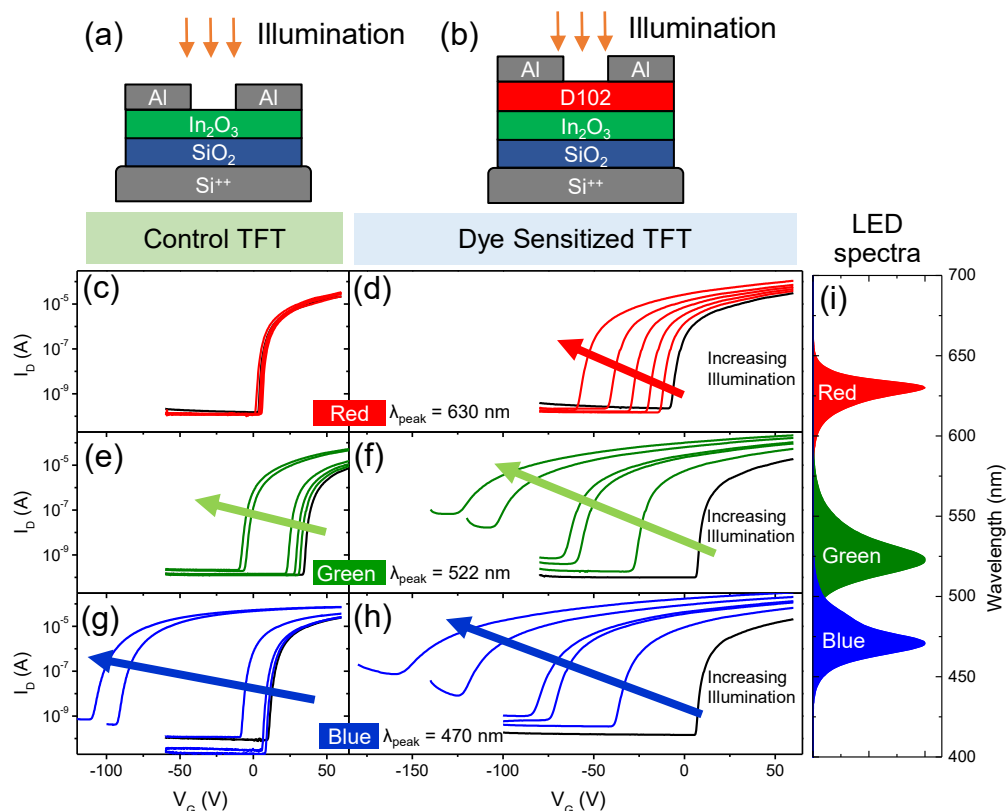


Figure 5.6: Optoelectronic response of (a) the control TFT and (b) the dye-sensitized TFT under illumination from three LEDs whose spectra are shown in (i). The black line in (c)-(h) indicates the response of the device in dark, while the following lines are the transfer characteristics with the LED set to currents of 1, 5, 10, 50 and 100 mA. The left column shows the control TFTs response to (c) red, (e) green and (g) blue illumination. The right column shows the dye-sensitized TFTs response to (d) red, (f) green and (h) blue illumination. (Adapted with permission from Mottram et al.¹⁰¹. Copyright 2016 American Chemical Society.)

There are three mechanisms responsible for the effects observed during transistor characterisation: photoconduction, photodoping, and dye assisted photoconduction and photodoping. The first discussed mechanism will be photoconduction. As briefly mentioned in Section 5.1, photoconduction can be summarized as the creation of electron hole pairs due to

absorption of incident photons by impurity states and the bandgap. The photoinduced transient charge carriers will have a short life time, temporarily increasing the channel conductance by increasing the background charge carrier density.¹²⁵ The rate of absorption of light is approximately proportional to the number of states with an energy separation equal to that of the incoming light. A commonly made assumption within amorphous and polycrystalline semiconductor physics is that the trap states within the bandgap can be approximated as an exponential function decaying away from the conduction band edge.^{54,74} The result of exponential decaying tails of localised states in the bandgap is a sharp decrease in the absorption of short wavelength light, and hence lower photocurrents.

Photoconduction normally produces only very small currents. If the photoconduction induced charge is less than the field induced charge then the photoconduction will be unobservable, therefore photoconduction is normally seen as an increase in I_{off} . Another caveat required to observe photoconduction within experimental measurements is that the photocurrent produced must exceed the sensitivity of the source measure unit. The effect of photoconduction is most obvious within the control TFTs response to blue light (**Figure 5.6g**). Photoconduction in the control TFT under red light (**Figure 5.6c**) and green light (**Figure 5.6e**) is not apparent, as any effect is smaller than the experimental sensitivity. Photoconduction within the In_2O_3 successfully describes the increase in I_{off} within the control TFT under illumination, but cannot account for the negative shift in V_{on} observed under both green and blue illumination. Therefore, we must assume that there is another mechanism relating to the In_2O_3 layer producing this response.

To explain the negative shift in V_{on} for the control TFT it is useful to recognize that the shift in the transfer curves is typical of a doping like response, increasing with light intensity. This shift could be explained by charging of the semiconductor/dielectric interface shifting the threshold voltage, but such an explanation does not fit the transient measurement response, or light sensitivity as discussed later in this Section. This photodoping response upon illumination has been previously reported in various metal oxide materials. As a result of that, a theory of photodoping of metal oxides has been developed by Verbakel et al. in order to explain increases in the conductivity of ZnO nanoparticle TFTs and diodes.¹²⁶ This theory has been similarly applied by Lakhwani et al. to explain the creation of a Moss-Burstein shift in ZnO nanoparticles films when exposed to UV light.¹²⁷

This second mechanism, photodoping, works as follows. Oxygen bound to the surface of the In_2O_3 film acts as electron traps, locally depleting the semiconductor. Holes introduced by photogenerated charge pairs due to interband absorption allow for desorption of this surface bound oxygen, consequently increasing the electron concentration within the channel. It is highly unlikely for holes to be injected directly from the Al S-D electrodes due to the deep level of the In_2O_3 valence band at -7.85 eV ¹²⁸, allowing this to be a solely photon induced event. If the bound oxygen is released in a controlled nitrogen environment, such as during optoelectronic characterisation, the oxygen will be removed from the surface. Due to a lack of oxygen in the measurement atmosphere, it is then unable to reabsorb. This will lead to a semi-permanent deficiency of oxygen, increasing the number of charge carriers within the TFT channel. It has previously been argued by Kim et al.¹²⁹ that this oxygen deficiency will create a back channel that increases the overall conduction within the device. Due to the ultra-thin nature of the In_2O_3 used within this work it is hard to isolate effects of a back channel from the active channel of the TFT. It is therefore likely that the photodoping will directly affect the TFT channel, which is observed in the large negative shift in the transfer characteristics of the control TFT under blue illumination (**Figure 5.6g**). Just like photoconduction, photodoping is dependent on the number of charge carriers produced, explaining the pattern of increasing doping with decreasing wavelength in the control device.

A final mechanism is required to create a complete description of the optoelectronic response of both control and dye-sensitized TFTs. It must explain the difference in response between these two sets of devices. From **Figure 5.6** it is obvious that the D102 dye has both the effect of increasing apparent photodoping, and larger increase in I_{off} upon illumination when compared to the control TFT. Both previous processes of photoconduction and photodoping are dependent on the number of photons absorbed, and hence the extra electron-hole pairs produced. From **Figure 5.4** it is obvious that the addition of D102 increases the absorption of light in the red region of the spectra by a small amount, and it greatly increases the absorption of light at green wavelengths. The D102 dye has a lowest unoccupied molecular orbital (LUMO) at -2.59 eV , while the conduction band (CB) of In_2O_3 is at -3.98 eV .^{128,130,131} This means it is energetically favourable for the electrons produced by light absorbed in the D102 to transfer to the CB of In_2O_3 , thus increasing the electron concentration in the ultrathin TFT channel. This explains why the increase in I_{off} to green and blue illumination on the dye-sensitized device

(**Figure 5.6** (f) and (h)) is much greater than that of the control device (**Figure 5.6** (e) and (g)). There is no observed increase in I_{off} for the dye-sensitized device with red illumination. It is assumed that this is because any change is less than the experimental sensitivity of the SMUs.

The addition of D102 has been shown to amplify the photoconduction within the dye-sensitized TFT. Similarly, there is an observable increase in negative shift of the transfer curves for the dye-sensitized TFT. This indicates that the absorption of light by the D102 is facilitating the photodoping process. It is proposed that the holes, produced when D102 absorbs a photon, assist in desorption of surface oxygen in proximity. This explains the doping effect seen by the dye-sensitized TFT under red illumination (**Figure 5.6** (d)), and the increase in doping between the control and dye-sensitized TFTs to green and blue illumination (**Figure 5.6** (f) and (h)).

These three mechanism of photoconduction, photodoping, and dye-assisted photoconduction and photodoping provide a complete description that fully explains the experimental results. Two other phenomena, observed during measurements, which support this conclusion are the long term nature of the change in transfer characteristic and the ability to “reset” devices by exposing them to air. When illuminated, the transfer characteristics would change as previously described, but after the device was returned to dark, it would maintain most of the features of the illuminated response. This effect could be undone by removing the devices from the testing atmosphere of nitrogen, and exposing them to ambient air. After being exposed, they were returned to the nitrogen atmosphere for remeasuring, upon which they were found to have electrical characteristics similar to its original state.

5.4.1 Gate Dependent Figures of Merit

The transfer characteristics in **Figure 5.6** (c)-(h) show that there is an obvious gate voltage dependency to the photoresponse. Hence the figures of merit that define performance as a phototransistor will also be gate voltage dependent. To assess the function of control and dye-sensitized TFTs as phototransistors the photosensitivity (**Figure 5.7**) and the responsivity (**Figure 5.8**) were calculated as a function of gate voltage.

From **Figure 5.7**, three specific regions can be seen in the photosensitivity, though not all regions are visible for each device and LED combination. The first region (i) starts from negative voltages and can be seen as a plateau in the photosensitivity increasing with light intensity, and most clearly visible in the control TFT response to green light (**Figure 5.7** (b)). The region (i) is

characterised by its flat nature and low values for photosensitivity and created by photoconduction increasing the off current of the TFT. The next region (ii) is characterised by a rapid increase in the photosensitivity which plateaus as it approaches V_{on} of the TFT in dark. Here, due to photodoping, the TFT is exhibiting a negative shift in its transfer characteristics. For a given gate voltage, the device under illumination is effectively switched from being turned off into the subthreshold regime, where there is a massive increase in current of multiple orders of magnitude. This rapid increase in current in region (ii) ultimately gives rise to the highest values of photosensitivity. The final region (iii) shows a quickly decaying photosensitivity from V_{on} of the device in dark to positive voltages. This is due to the increase of the TFT dark current at higher gate voltages decreasing the photosensitivity.

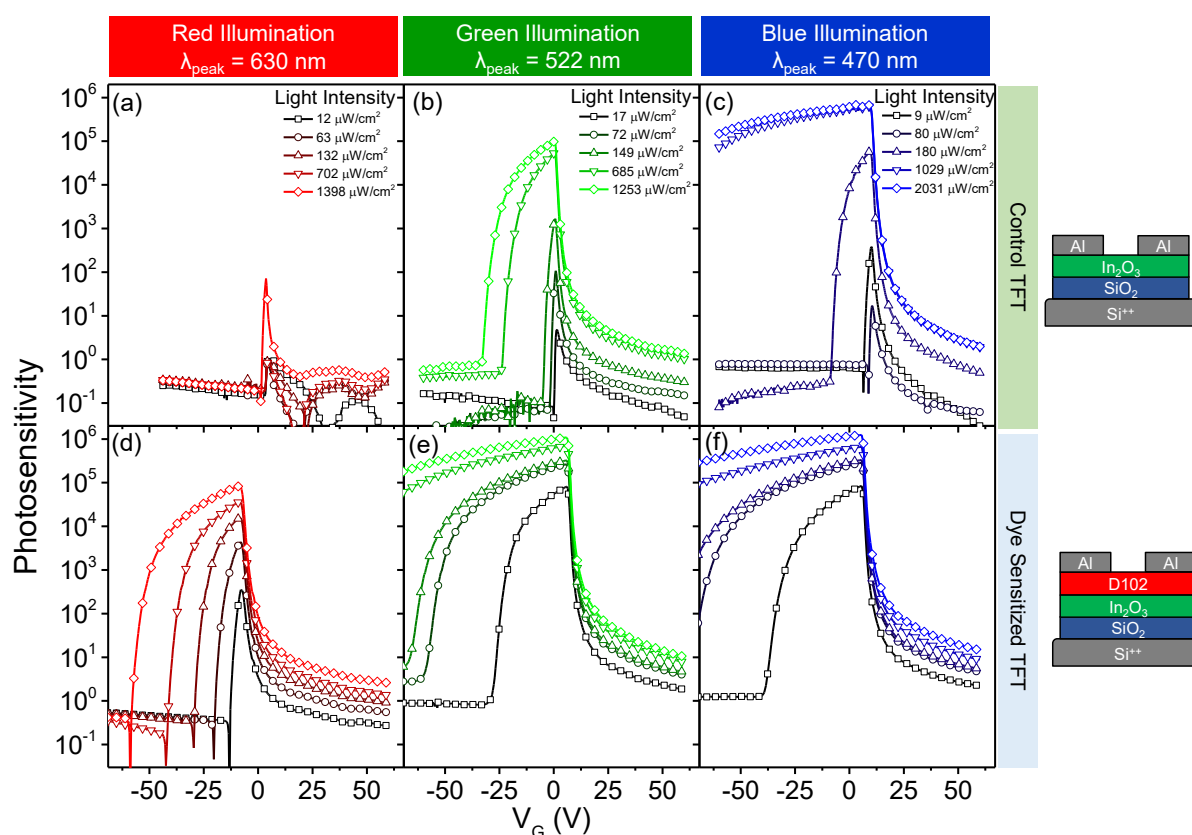


Figure 5.7: Photosensitivity of (a)–(c) the control TFT and (d)–(f) the dye-sensitized TFT to: (a),(d) red illumination, (b),(e) green illumination and (c),(f) blue illumination. Light intensities were identical for both control and dye-sensitized devices.

The photosensitivity of the control TFT to red light is nearly non-existent, while its response to green light shows increasing I_{off} that is creating the region (i) behaviour. The control TFTs response to blue light obviously produces region (ii) and (iii) like behaviour, but

region (i) behaviour is not observable due to the changes in integration time causing a drop in the noise floor. For the dye-sensitized device exposed to red light, the region (i) behaviour is unobservable as any change in I_{off} due to photoconduction is masked by the sensitivity of the SMU. Region (i) behaviour is also hard to see for the dye-sensitized TFTs response to green and blue light, this is due to that region being at more negative voltages than those plotted. The regions of (ii) and (iii) are apparent in the response of the dye-sensitized TFT to all wavelengths of light.

The maximum photosensitivity for each device occurs around V_{on} (usually lying between ± 10 V for all devices). For control devices the maximum photosensitivity increases with decreasing wavelength (red to blue); this is also true for the dye-sensitized devices. It is notable though that the difference between maximum sensitivity to blue and green LEDs for the dye-sensitized device is minimal unlike the order of magnitude difference seen for the control device. Dye-sensitization increased the photosensitivity of the phototransistor significantly to red and green illumination, with only a modest increase in response to blue illumination.

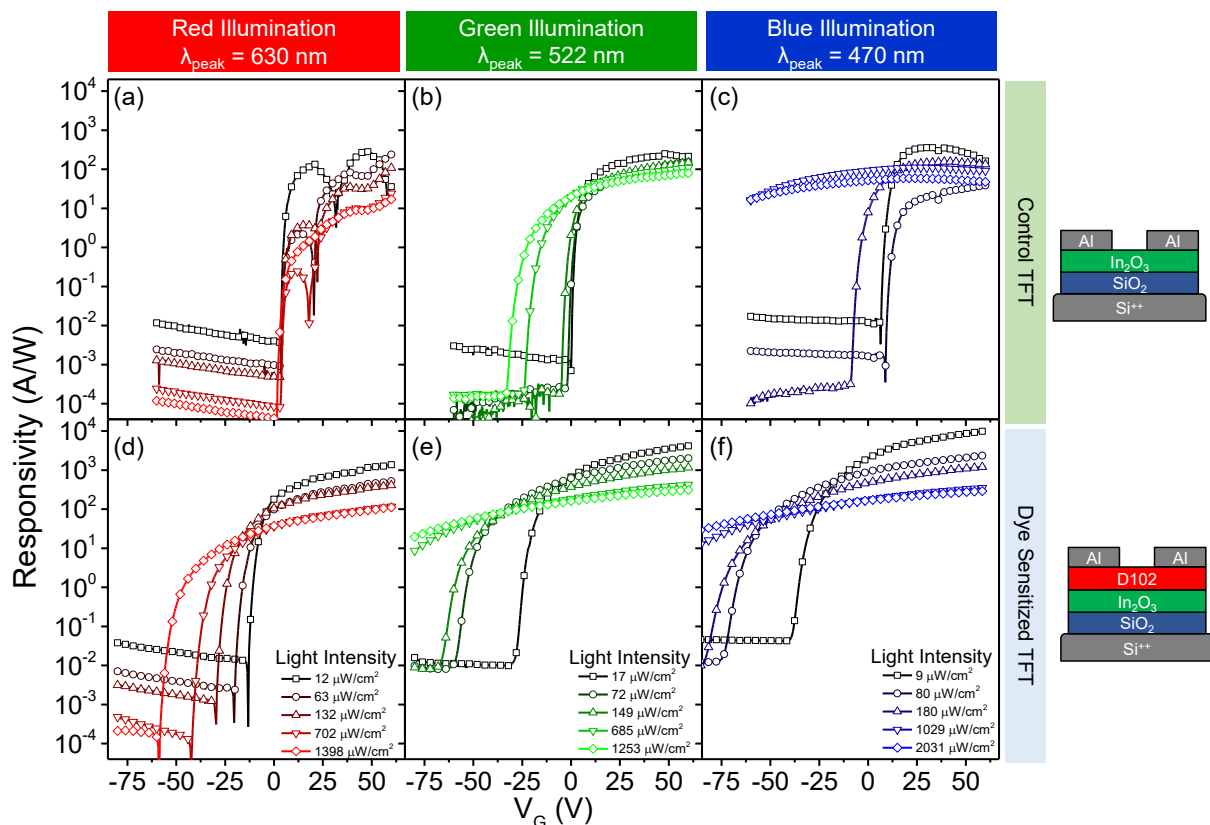


Figure 5.8: Responsivity of (a)–(c) the control TFT and (d)–(f) the dye-sensitized TFT to: (a),(d) red illumination, (b),(e) green illumination and (c),(f) blue illumination. Light intensities were identical for both control and dye-sensitized devices.

The responsivity of control and dye-sensitized TFTs is shown in **Figure 5.8** and all follow a general trend of increasing responsivity with increasing gate voltage. This is because the responsivity is not normalized with respect to the dark current at the set gate voltage. This highlights why the responsivity alone provides a poor figure of merit, unless paired with the photosensitivity. The dye-sensitized device shows an increased responsivity to every illuminating wavelength, with the maximum value (of 1.2×10^6) given by the dye-sensitized device when exposed to blue light. Also of note is the fact that for all results the responsivity decreases with increasing light intensity. This effect is attributed to the response being cumulative over time until the system reaches equilibrium. As the light intensity is increased step by step during the course of the experiment, the oxygen available for desorption incrementally decreases, ultimately limiting the possible photodoping effects.

5.4.2 Illumination Dependent Figures of Merit

When applied as a practical photodetector a phototransistor is unlikely to be operated using transfer measurements to calculate the incident light intensity. Instead, the gate voltage should be fixed, at a value to optimize both responsivity and photosensitivity, and the drain current will be measured. Using the combined results of **Figure 5.7** and **Figure 5.8** an optimal value of photosensitivity and responsivity occurs at $\sim V_G = 0$ V for all devices at all wavelengths. Therefore, the photosensitivity and responsivity were calculated at $V_G = 0$ V as a function of light intensity (**Figure 5.9**).

The results of **Figure 5.9** show that in all cases the photosensitivity and responsivity increase upon dye-sensitization of the In_2O_3 layer. The photosensitivity increases due to the D102's assisted photodoping process that causes an exponential increase in current upon illumination. This behaviour is characteristic of a system with a high signal amplification, but leads to nonlinear behaviour in its response to incident light power. The non-linear, or to be more specific sub-linear, behaviour of the photosensitivity leads to corresponding responsivities that decrease with illumination power. This has already been attributed to the increased scarcity of surface oxygen at higher light intensities, decreasing the ability to be released to cause photodoping.

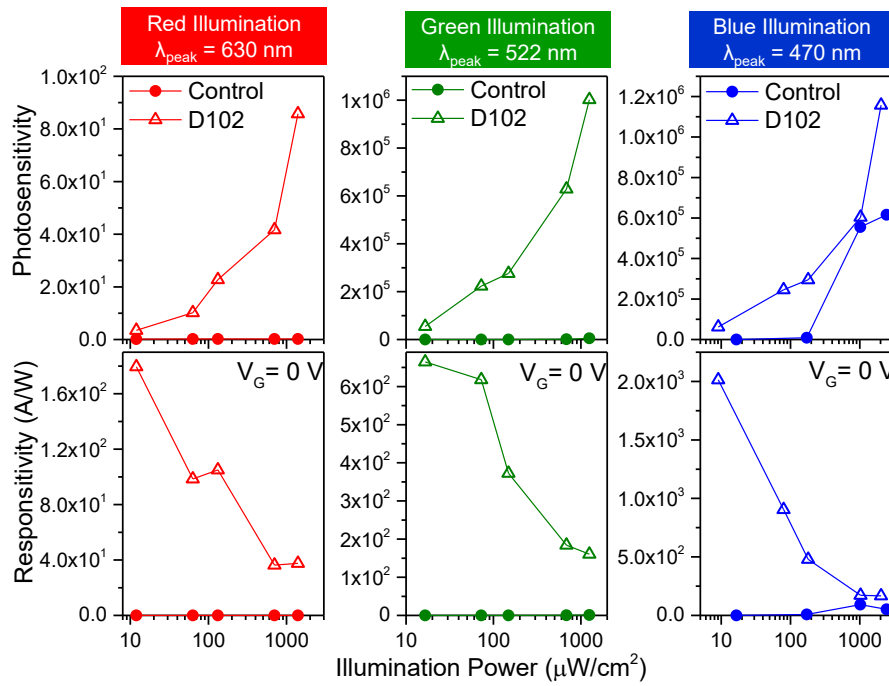


Figure 5.9: Photosensitivity (top row) and responsivity (bottom row) of control and D102 dyed devices as a function of illumination power. The results are for (left column) red, (middle column) green and (right column) blue illumination. (Reprinted with permission from Mottram et al.¹⁰¹. Copyright 2016 American Chemical Society.)

The maximum values for photosensitivity and responsivity (with $V_G = 0$ V) for the In_2O_3 bilayer device was measured under blue illumination as 1.16×10^6 and 2000 A/W respectively. However, it is the response to green light that was most improved upon addition of D102 with a photosensitivity and responsivity (with $V_G = 0$ V) of 1.00×10^6 and 660 A/W respectively. The maximum value of responsivity of 2000 A/W for the dyed phototransistor is achieved at $V_G \approx 25$ V. These values compare very favourable to the current state-of-the-art devices, as can be seen by the position of this work (point 22) in **Figure 5.1**. This demonstrates that the D102 has been electronically coupled to the TFT via an extremely simple method.

5.5 Photodoping and Bandgap Analysis

Bandgap states are a key factor within the performance of all transistors as thoroughly covered within Section 3.4. The density and energy of these bandgap states dominate the form of the subthreshold slope via the trapping of field-induced charge, retarding progress of the quasi Fermi level⁸⁷ towards the conduction band when the gate voltage is increased. Previous discussion within this chapter has proposed that the negative shifts in the transfer

characteristics and V_{on} is due to photoinduced n-type doping of the In_2O_3 . The energetic result of such a mechanism will be the shifting of the Fermi energy level (E_F) towards the conduction band upon increasing illumination intensities. In this study the Gr̈unewald bandgap analysis technique⁸⁵, described in detail within Section 4.2, provides a systematic method for calculating the bandgap states of a TFTs semiconductor from a single transfer characteristics.

Upon illumination it should be expected that the photodoping process outlined within Section 5.4 will increase the number of charge carriers in the TFTs semiconductor at flat band voltage. The flat band voltage of a semiconductor manifests as V_{on} within most TFTs, and so as doping increases, the position of E_F (free from external effects, including band bending) should move towards the conduction band. Although photodoping could produce extra states, there already exist a substantial number of bandgap states within oxide materials,^{132,133} hence it is not expected to cause a significant change in the total number. Any large increase in the number of bandgap states is unlikely without a physical change in crystal structure, as expected when introducing extrinsic dopants.

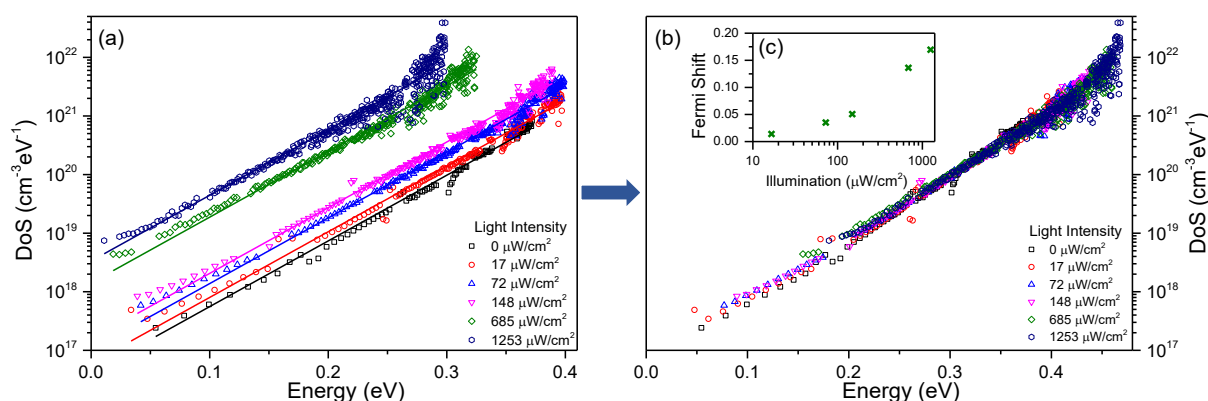


Figure 5.10: Density of states in the bandgap for the dye-sensitized device as a function of green illumination intensity. (a) The results from a Gr̈unewald analysis of the transfer characteristics where zero energy is set as the energy of the Fermi level when the transistor is at flat band voltage. Lines indicate linear fits to the data. (b) The results from (a) after they have been aligned to the zero light intensity result by subtracting the offset in energy from the linear fits within (a). (c) Shows the required subtraction from the linear fit used to align the data in (b). (Adapted with permission from Mottram et al.¹⁰¹. Copyright 2016 American Chemical Society.)

Using the bandgap analysis the density of states (DOS) as a function of energy away from the Fermi level were calculated as shown in **Figure 5.10** (a). The results within **Figure 5.10** are for the dye-sensitized TFT when exposed to green light. The similarities between different intensities is immediately apparent, supporting the theory that this is the measurement of the

same set of states, starting at different E_F . To align the data and measure the shift in E_F , linear fits were produced for each light intensity, with the fit lines demonstrated in **Figure 5.10** (a). The results for each illuminated DOS were then aligned with the DOS of the phototransistor in darkness (**Figure 5.10** (b)). **Figure 5.10** (c) shows the required energy shift in E_F used to align the data and enables a simple and quantifiable measurement of the degree of photodoping.

The findings of **Figure 5.10** support the hypothesis that photodoping is the predominant mechanism causing the shift in the TFTs transfer characteristics towards more negative values of gate voltage. This in turn has produced the ultra-high values of photosensitivity and responsivity as a photodetector. Within **Figure 5.10** (b) there are fluctuations in the DOS for intensities at higher energies (> 0.44 eV) and this can be explained by the breakdown of the Grünewald model as it approaches the conduction band of the In_2O_3 . Another possible explanation for these fluctuations is the increased error in the deconvolution as less data is available to produce the result for higher energies.

5.6 Summary of Dye-Sensitized In_2O_3 Phototransistors

To summarize Chapter 5, dye-sensitized In_2O_3 phototransistors with the small molecule D102 were fabricated and studied. Except for the use of evaporation to create source/drain contacts, the devices were produced from solution at temperatures ≤ 200 °C using facile upscalable processes. This produced a high performance phototransistor with maximum values of photosensitivity and responsivity of $\sim 10^6$ and ~ 2000 A/W respectively to green illumination. The high performance is attributed to the ultra-thin nature of the semiconducting layer allowing for strong optoelectronic coupling of the D102 dye with the channel. Also, the addition of gating the device provided access to energetic regimes inaccessible to two-terminal photodetectors.

It has been proposed that the mechanism responsible for the large responsivity and photosensitivity is one of photodoping. Surface adsorbed oxygen may be desorbed with the aid of adjacent holes, produced either by absorption of light by the D102 dye or the semiconductor. The irreversible response of the phototransistor within a nitrogen atmosphere and the subsequent bandgap analysis provide support for this assertion. Additional support towards this hypothesis comes from the correlation between the overlap of UV-Vis absorption and experimentally observed negative shift in the transfer characteristics. Due to the irreversible

nature of this mechanism within a nitrogen atmosphere further development into regeneration of the sensor would prove beneficial.

6 High-k Metal Oxide Dielectrics

Dielectrics form an important part of multiple electronic devices, from barrier layers in resonant tunnelling diodes¹³⁴⁻¹³⁶ to the insulator within a thin film transistor (TFT)¹¹. Within this work, a focus on their application within TFTs shall be maintained. As with the rest of this thesis, the study will use solution processable, low-temperature fabrication techniques.

The quantifiable figures of merit for a dielectric as the insulating layer within a TFT are the specific capacitance, leakage current and breakdown field. The specific capacitance (capacitance per unit area, synonymous with areal capacitance) controls the operating voltage required to efficiently induce charge within the channel of the TFT to turn on the device. The specific capacitance of a dielectric is given by:

$$C_{ins} = \frac{\epsilon_{ins}\epsilon_0}{t_{ins}} \quad (87)$$

where ϵ_{ins} , ϵ_0 and t_{ins} are the relative permittivity, the permittivity of free space and thickness of the insulator, respectively. Obviously, the capacitance of an insulator can be increased by decreasing the thickness of that layer or by choosing a material with a higher permittivity. But decreasing the dielectric thickness too much will impact TFT leakage current and breakdown voltages. To produce a set geometric capacitance, a high permittivity material will require a thicker film than a lower permittivity material. This in turn reduces gate leakage, hence a high permittivity material, allows for reduced gate leakage without compromising capacitance.

So far within this work, the dielectric silicon dioxide (SiO_2) has been used. This is due to availability of high quality thermally grown $\text{SiO}_2/\text{Si}^{++}$ substrates, with a range of thicknesses. The Si^{++} acts as an excellent gate contact, and the SiO_2 at 100 nm and 400 nm provides a capacitance of 34.4 nF/cm² and 8.6 nF/cm² respectively. This is quite low due to the relative permittivity of SiO_2 being only 3.9. Also, the thermal requirements of growing the SiO_2 layer is energy intensive and requires expensive substrates to produce. Hence an alternative solution would be preferable.

6.1 Comparable Dielectrics

As can be seen in **Figure 6.1**, SiO_2 has one of the lowest relative permittivities compared to the other available metal oxide dielectrics. Its popularity as a dielectric is based on how easy it is to

produce on silicon and its large bandgap providing low leakage current. The general trend seen within **Figure 6.1** is one of decreased bandgap with increased dielectric constant. On a side note this leads to the interesting case of titanium dioxide: considered a dielectric, but often used as a semiconducting transport layer within DSSCs.¹³⁷

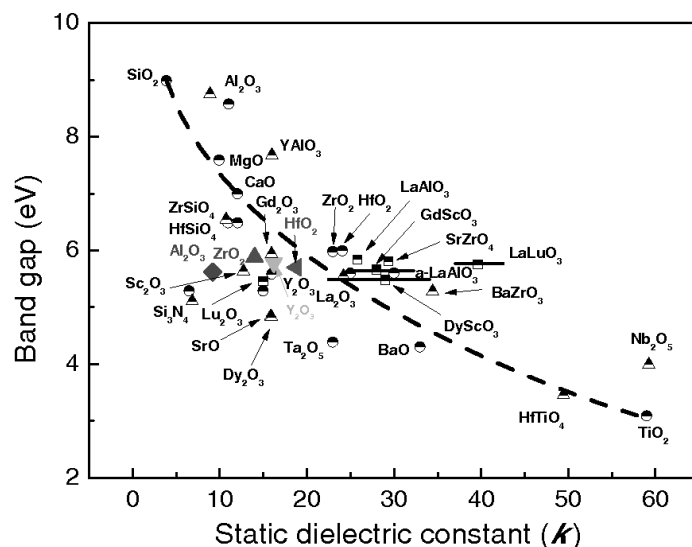


Figure 6.1: Static dielectric constants (relative permittivities) vs band gap for various gate dielectric metal oxides grown via a range of deposition techniques as reported by Esro et al.¹³⁸. Solid filled data points correspond to spray coated dielectrics. (Reprinted with permission from Esro et al.¹³⁸. Copyright 2014, Wiley-VCH.)

Development of silicon dioxide deposited from solution has been attempted from precursors such as tetraethyl orthosilicate (TEOS)¹³⁹ and perhydropolysilazane (PHPS)^{140,141}. Though successful, the resulting capacitances of these layers were still extremely low compared to other solution dielectrics as demonstrated in **Table 6.1** and illustrated in **Figure 6.2**. **Table 6.1** shows a selection of recently reported solution processed dielectrics as compiled by Sungjun Park et al.¹⁴², with extra SiO₂ based devices included. Since processing temperature is one of the key factors of this thesis the figures of merit of capacitance, breakdown field and on/off current ratio have been plotted as a function of temperature in **Figure 6.2**.

It may be expected that increasing processing temperature would improve all figures of merit, but this is not observed. Instead there seems to be little correlation between processing temperature and any of the three figures of merit plotted in **Figure 6.2**. It is important to note that leakage current is not included as a figure of merit due to the inconsistent reporting methods. Also, there are many confounding factors that affect the performance of a dielectric

past the processing temperature. These include: solvent use, processing method, layer thickness and the selected semiconductor (for the on/off ratio).

Table 6.1: Comparative list of dielectric materials produced via solution processing compiled from Sungjun Park’s review paper on metal oxide dielectrics.¹⁴² Extra papers using solution processed SiO₂ dielectrics have been added and all data has been sorted by processing temperature. Note that “d” refers to dielectric thickness, “C” is the dielectric capacitance, “k” is the relative permittivity, “BD F” is the breakdown field and “SC” is the semiconductor it was paired with to make TFTs. (Adapted and reprinted from Sungjun Park et al.¹⁴², with permission from Elsevier.)

Dielectric	Process Temp °C	d nm	C nF/cm ²	k	BD F MV/cm	SC	Max Mob cm ² /Vs	On Off Ratio	Pub Year	Ref
SiO ₂	150*	205	32	7.4	>5	IZO	49.1	~10 ⁵	2016	141
ZrOx	150*	5	~830	8.79	~18	ZnO	0.45	~10 ⁵	2012	143
AlOx	150	20	250	-	~8	InO	8.3	~10 ⁷	2015	20
AlOx	150	59	104	7.04	~8	ZnO	1.37	~10 ⁶	2014	144
SiO ₂	180†	200	-	-	>1	ZnO	3	~10 ⁷	2015	140
AlOx	200	40	160	-	-	IGZO	11	~10 ⁴	2015	145
AlOx	250	38	~188	-	-	InO	40	~10 ⁷	2011	146
GaOx	250	52	172	10.1	>2.5	InO	4.1	~10 ⁵	2015	147
ZrOx	250	20	502	13	>5	IZO	75	~10 ⁴	2015	148
ZrOx:B	250	100	-	12.1	~3.94	InO	39.3	~10 ⁷	2013	149
AlOx	300	55.4	167	10.4	>42	InO	21.7	~10 ⁴	2014	150
AlOx	300	52	194	11.4	-	IZO	10.1	~10 ⁵	2015	151
AlOx	300	70	~80	~6.3	~4	ZTO	33	~10 ⁸	2011	152
HfOx	300	65	~190	~14	-	ZTO	1.05	~10 ⁵	2012	153
YOx	300	59.2	380	25.4	>2	IZO	0.1	~10 ²	2014	150
YOx	300	20	360	14.8	4	IZO	25.9	~10 ⁶	2015	154
ZrOx	300	54.2	369	22.6	>2	InO	1.6	~10 ⁴	2014	150
ZrOx	300	149	-	10	-	CdS	~48	~10 ⁵	2009	155
ZrOx	300	35	~240	24.5	-	ZTO	4	~10 ⁵	2012	156
ZrOx	300	-	426	12.5	7.2	InO	23	~10 ⁷	2014	157
AlPOx	350	~180	-	5.2	~5	IGZO	4.5	~10 ⁹	2011	158
AlOx	350	242	143.7	-	~4	ZnO:Li	46.9	~10 ⁵	2013	159
AlOx	350	10	625	7.1	-	GZTO	1.3	~10 ⁴	2014	160
AlOx	350	150	46.3	-	4.9	IGZO	84.4	~10 ⁵	2014	161
AlOx	350	15	350	-	-	IGZO	1.32	~10 ⁶	2015	162
AlOx	350	85	70	7.07	8.2	IGZO	19.8	~10 ⁵	2016	163

AlPO _x	350	148 ~185	-	4.8	~5	ZnO	~3.5	~10 ⁶	2007	164
SiO ₂	350	143	21	3.5	7	InO	28	~10 ⁸	2015	139
YO _x	350	17	448	16.5	>5	InO	15.9	~10 ⁶	2015	165
ZrO _x	350	45	255	-	-	IZO	93.4	~10 ⁵	2015	145
ZrO _x	350	25	370	14.3	9.5	IGZO	28.5	~10 ⁵	2016	163
ZrO _x	350	210	-	14.8	~2.8	IZO	7.21	~10 ⁶	2013	166
AlO _x	385	16	380	7.9	>4	IGZO	6	~10 ⁵	2015	167
HfO _x	385	16	409	11	-	-	-	-	2015	167
AlO _x	400	-	~50	~9.2	~1.8	ZnO	7	~10 ⁵	2011	168
GdO _x	400	100	-	10~12	~3.5	ZTO	~2.53	~10 ⁵	2013	169
HfO _x	400	~120	-	~13	~5.5	IGZO	13.1	~10 ⁷	2011	170
YO _x	400	22.7	345.7	8.85	3.5	IZO	20.9	~10 ⁶	2015	171
YO _x	400	-	134.1	16.2	~1.8	ZnO	34	~10 ⁴	2011	168
ZrO _x	400	100	-	-	-	SnO	~100	~10 ⁵	2013	172
HfO _x	450	100	155	18.5	>2.5	ZnO	42	~10 ⁵	2015	138
ZrO _x	450	~98	126	~14	~1.6	ZnO:Li	~85	~10 ⁶	2011	173
ZrO _x	450	<100	108.7	19.1	3.2	ITZO/ IGZO	40	~10 ⁶	2014	174
AlO _x [†]	500	80	~200	9.2	~2	ZTO	19.6	~10 ⁴	2013	175
GdO _x	500	100	146	9~14	~3.5	ITZO	~1.9	~10 ³	2013	176
ZrO _x	500	~60	-	22	4	SnO	11	~10 ⁶	2015	177
ZrO _x	500	90	~240	-	-	ZTO	~10	~10 ⁹	2013	178
AlO _x	550	32.7	335.7	-	-	ITZO	23.7	~10 ⁶	2015	179
AlO _x	600	30	~56	~10	~2	ZnGaO	4.7	~10 ³	2010	180
AlO _x :Na	600	75	~2000	170	~5.3	ZTO	28	~10 ⁴	2009	181
AlO _x :Na	830	80	100	170	-	ZTO	18	~10 ⁴	2011	182

*Process assisted by UV exposure

†Process assisted with plasma treatment

‡AlO_x imbedded with atoms of Li, Na or K

The most important information that can be extracted from **Table 6.1** and **Figure 6.2** is that it is possible to produce high quality solution processed dielectrics at low temperatures. Four of the most commonly studied dielectrics within the literature are aluminium oxide (AlO_x), hafnium oxide (HfO_x), yttrium oxide (YO_x) and zirconium oxide (ZrO_x). AlO_x has previously been produced from aluminium nitrate hydrate in the solvents ethanol¹⁵¹ and 2-methoxyethanol^{20,180,183} with positive results. HfO_x films have been reportedly fabricated using the precursor of hafnium chloride (HfCl₄) dissolved and processed with the following solvents: mixed methanol and ethanol¹³⁸, ethylene glycol and acetonitrile¹⁵³ and deionized water¹⁸⁴. For

YOx the use of the precursor of yttrium(III) nitrate hexahydrate has been reported in two ways. Firstly by dissolving it in deionized water, producing a slurry, followed by centrifugation, precipitation, and redissolving it in acetic and nitric acid.¹⁸⁵ Secondly, by the much simpler method of spin casting after dissolving the precursor in deionized water.¹⁶⁵ Finally, ZrOx has been produced from a nitrate precursor of zirconium oxynitrate in the deionized water as part of a bilayer AlOx and ZrOx dielectric¹⁴⁴. Due to the established work on these four materials, they were chosen as the four precursors for this study.

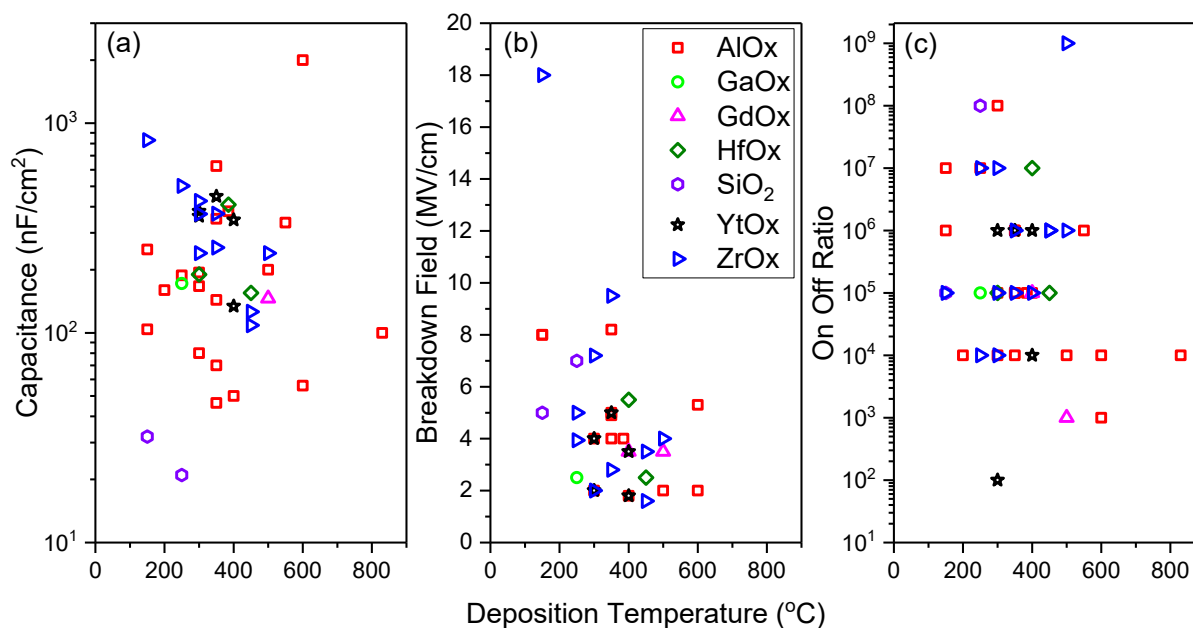


Figure 6.2: Plots of (a) the capacitance, (b) the breakdown field and (c) the on off ratio against the deposition temperature of devices from **Table 6.1**. For papers where a maximum breakdown voltage was not reported, the maximum shown breakdown voltage exhibited in the paper was used instead. Original results were collated by Sungjun Park et al.¹⁴²

6.1.1 Fabrication Constraints

The work in this chapter was approached as a comparative study of four dielectric precursors under identical processing conditions. The processing conditions were decided by following a set of fabrication constraints, as set out below.

- 1) **Solution processed** – the dielectric and semiconducting layers of these devices must be solution processed
- 2) **Low-temperature** – the maximum processing temperature allowed in processing is 200 °C so that the dielectrics could be compatible with plastic substrates in future work

- 3) **Air-processed** – the dielectric and semiconductor should be able to be processed in air, avoiding need for specialized atmospheres or dust prevention
- 4) **Facile upscalable techniques** – simple techniques with up-scalability should be chosen over lab specific methods
- 5) **Inexpensive substrates** – avoid expensive substrates such as doped silicon in favour of cheaper glass substrates

By following these five guidelines we hoped to identify the best potential candidate. This candidate may then be optimized further and commercialized.

6.2 Device Structure

From Section 6.1, four precursors were identified for producing the dielectrics layers. These are shown in **Figure 6.3** as aluminium nitrate nonahydrate to produce AlO_x , hafnium chloride for HfO_x , yttrium nitrate hexahydrate for YO_x and zirconium oxynitrate hydrate for ZrO_x . Although the most common solvent used to spin cast all of the named precursors was deionized water, preliminary research found that this led to wetting issues in connection with the glass substrates. Therefore, the solvent 2-methoxyethanol (2-MeOH) was used instead due to its excellent wettability on glass. The precursors of aluminium nitrate nonahydrate dissolved easily within this solvent, while hafnium chloride and zirconium oxynitrate required extra time (up to 24 h) to fully prepare the solution.

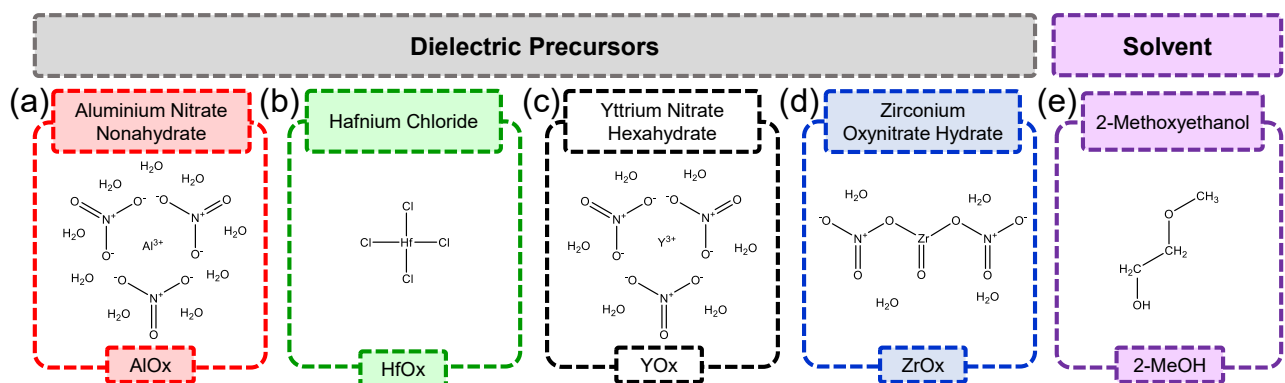


Figure 6.3: Materials used to process dielectric layers from solution including the four precursors used in attempt to produce (a) aluminium oxide, (b) hafnium oxide, (c) yttrium oxide and (d) zirconium oxide. Also included is (e) 2-methoxyethanol, the common solvent used for all dielectric layers.

Two device types were produced for each dielectric to fully characterise these four materials, namely capacitors and TFTs. The first device type, shown as (a) in **Figure 6.4**, is a

capacitor structure that is used to measure break down voltage, leakage current and capacitance. The capacitor structures were also used to measure the topography of the dielectric surface when produced upon aluminium contacts. In this way, the dielectric surface topography is not only indicative of the dielectric film quality but also represents a way to characterise the interface roughness with a subsequently deposited semiconductor layer. Such a dielectric/semiconductor interface is present in the second device structure investigated in this work, the TFT as shown in **Figure 6.4** (b). TFTs were used for transfer characteristic measurements, FET mobility calculations and bandgap analysis.

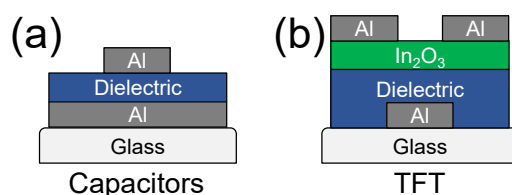


Figure 6.4: Device structures of (a) the capacitors and (b) TFTs, both produced on glass substrates.

All experimental work within this Chapter was performed by the author with two noted exceptions. Collaboration with two colleagues helped with producing data on the roughness of aluminium rates, and performing ellipsometry measurements.

6.2.1 Aluminium Evaporation Rate and Interface Roughness

Before producing any devices, the aluminium bottom contact was studied in conjunction with Gwen Wyatt-Moon, who provided some of the experimental data. The dependence of surface roughness on the evaporation rate has been reported for both electron beam evaporation^{186,187} and also for thermal evaporation³⁵. Since the bottom contact is the foundation of all the subsequent layers a short study was performed to provide a smooth foundation for the solution processed depositions.

Aluminium films were evaporated at rates of 0.5, 1, 2, 3 and 5 Å/s onto cleaned glass substrates to produce 40 nm thick films using the process and equipment outlined in Section 2.1.5. The surface topography was then measured using AC-AFM as described in Section 2.3.1, the results of which are shown in (a)-(e) of **Figure 6.5**. Contra to e-beam evaporation techniques, the roughness of the 40 nm films seems to decrease with evaporation rate, confirmed by both the RMS roughness and the height distribution plots, as seen in (f) and (g) of **Figure 6.5**

respectively. The RMS roughness seems to plateau at a minimum value as the evaporation rate reaches 3 Å/s. The conclusion from this short study is that for the bottom contact an evaporation rate of greater than 3 Å/s is vital for producing a smooth foundation for subsequent layers. On the other hand, top contacts, such as the source/drain contacts for the TFT, can be evaporated at lower rates. This is because the interface roughness for the source/drain contacts will be controlled by the previously deposited layer.

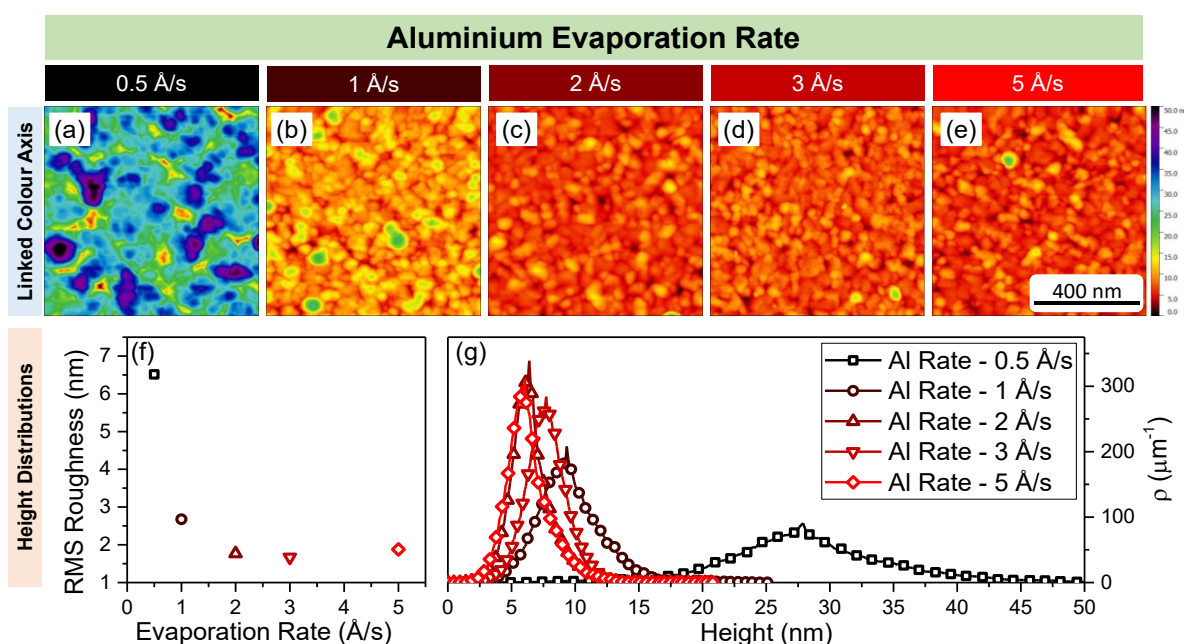


Figure 6.5: Effect of evaporation rate on the roughness of aluminium. Within (a)–(e) are shown $0.8 \mu\text{m} \times 0.8 \mu\text{m}$ topography scans of 40 nm thick aluminium films evaporated at rates of 0.5, 1, 2, 3 and 5 Å/s. Also included are (f) the root mean squared roughness of the topography scans and (g) height distribution plots for the five evaporation rates tested for the same scan size.

6.2.2 Solution Preparation

Four kinds of dielectric solutions were produced for use within this work. Solutions of 0.2 M concentration, for each of the precursor solutes listed in **Table 6.2**, were made with the solvent 2-MeOH. The solutions were then left to stir for 12 h at 80 °C. The semiconductor precursor solution was prepared by dissolving 40 mg/ml of indium nitrate hydrate in 2-MeOH, and leaving it to stir for 12 h before use.

Table 6.2: Solution strengths of solute within the solvent 2-methoxyethanol required to produce 0.2 M solutions of each dielectric precursors.

Solute	Atomic Weight	Concentration
Aluminium nitrate nonahydrate	375.13	75 mg/ml
Hafnium chloride	320.30	64 mg/ml
Yttrium(III) nitrate hexahydrate	383.01	77 mg/ml
Zirconium(IV) oxynitrate hydrate	231.23	46 mg/ml

6.2.3 Device Fabrication

Glass substrates were cleaned in deionized water, acetone and IPA for 10 mins in turn. This was followed by 10 mins UV-Ozone treatment to clean the surface further. Rectangular bottom contacts of width 0.8 mm and length 18 mm were then deposited onto the cleaned glass substrates at a rate of 3 Å/s. Following this the aluminium contacts were exposed to UV-light from a low-pressure mercury lamp for 12 hours to induce a surface layer of AlO_x.

Immediately before spin casting, samples were rinsed in IPA and dried with a nitrogen gun and given a 30 mins UV-Ozone treatment to improve wettability. The first layer of dielectric was spin cast at 4000 rpm for 30 s, followed by a 1 hour annealing step at 200 °C. For double layer dielectric devices, another 10 minute UV-Ozone treatment was performed followed by a repeated identical spin casting and annealing step.

To finalize the capacitors, a second set of identical rectangular contacts to the bottom contacts were evaporated at 0.5-1 Å/s onto the dielectric film at 90 ° to the initial contacts. This produced capacitor structures with an area of 0.64 mm². To instead create the TFTs, the single and double dielectric layers were UV-Ozone treated for 10 mins prior to spin casting. The indium nitrate hydrate solution was then spin cast at 6000 rpm followed by a 1 h annealing step at 200 °C. The TFTs were finished by evaporating 40 nm aluminium source/drain contacts at a rate of 0.5-1 Å/s. The TFTs produced were of length 1000 μm and widths 30 μm to 100 μm.

6.3 Material Characterisation

6.3.1 Substrate Topography

The quality of a dielectric film is judged by the quality of both its interfaces, and its ability to block charge transport. A smooth surface on the preceding layer to the dielectric film will reduce pin holes, responsible for increased gate leakage within TFTs. Therefore, both the smoothness of the gate-dielectric interface and the dielectric-semiconductor interface are key parameters in reducing gate leakage.

There are two possible architectures that may be used to produce TFTs. The choice of architectures will affect both the formation of the gate-dielectric interface and the dielectric-semiconductor interface. The first standard architecture, used within this work is the sequential deposition of gate contact, dielectric and then semiconductor. The second option is the inverted architecture, which inverts the deposition sequence to: semiconductor, dielectric and finally gate contact. The source/drain contacts have been ignored in this description as the deposition position of the source/drain contacts controls whether the TFT will be staggered or coplanar.

The deposition of thin film from solution often leads to planarization, and reduced roughness of the surface of the deposited layer. It would therefore seem preferential to choose an inverted architecture so that the semiconducting film will planarize the roughness of the aluminium source/drain contacts (discussed in Section 6.2.1). In addition, an inverted architecture is preferred for the production of certain organic materials where phase separation or other mechanisms produce increased conductivity at the surface of the deposited semiconductor¹⁸⁸. They are often used in conjunction with a polymer based dielectrics such as CYTOP^{80,189} or ferroelectrics such as poly(vinylidene fluoride-trifluoroethylene-chlorofluoroethylene)⁸⁹. To reiterate, there exist two key advantages of the inverted structure. Firstly, it may improve the mobility of charge within the channel by selecting the top surface of the semiconductor, particularly important for organic blend TFTs^{97,188}. Secondly, the dielectric layer can planarize any roughness within the semiconductor that may cause pin holes within the dielectric.

It is sensible to ask as to why an inverted structure was not used within this work to decrease the comparatively rough aluminium gate contacts. The answer to this is three-fold. To start with, the planarizing effect of the semiconductor, in an inverted device, is only efficient

when the semiconductor thickness is of the order, or greater than, the thickness of the source drain contacts being used. Due to the ultra-thin (~ 7 nm) nature of the In_2O_3 film produced, such a planarizing effect would not be expected. This is because 7 nm is not enough to fully cover the 40 nm thick source/drain contacts in an inverted structures. In addition, unless carefully controlled, the aluminium used for source/drain contacts will form an aluminium oxide barrier on the surface providing a small but measurable decrease in injection. Finally, due to the ultra-thin nature of the semiconductor the devices produced will be coplanar as opposed to staggered. Coplanar contacts have been shown to produce inferior device performance as they limit injection as described by Kim et al.¹⁹⁰. Therefore, standard bottom gate contact with staggered source/drain contacts were used as a device structures.

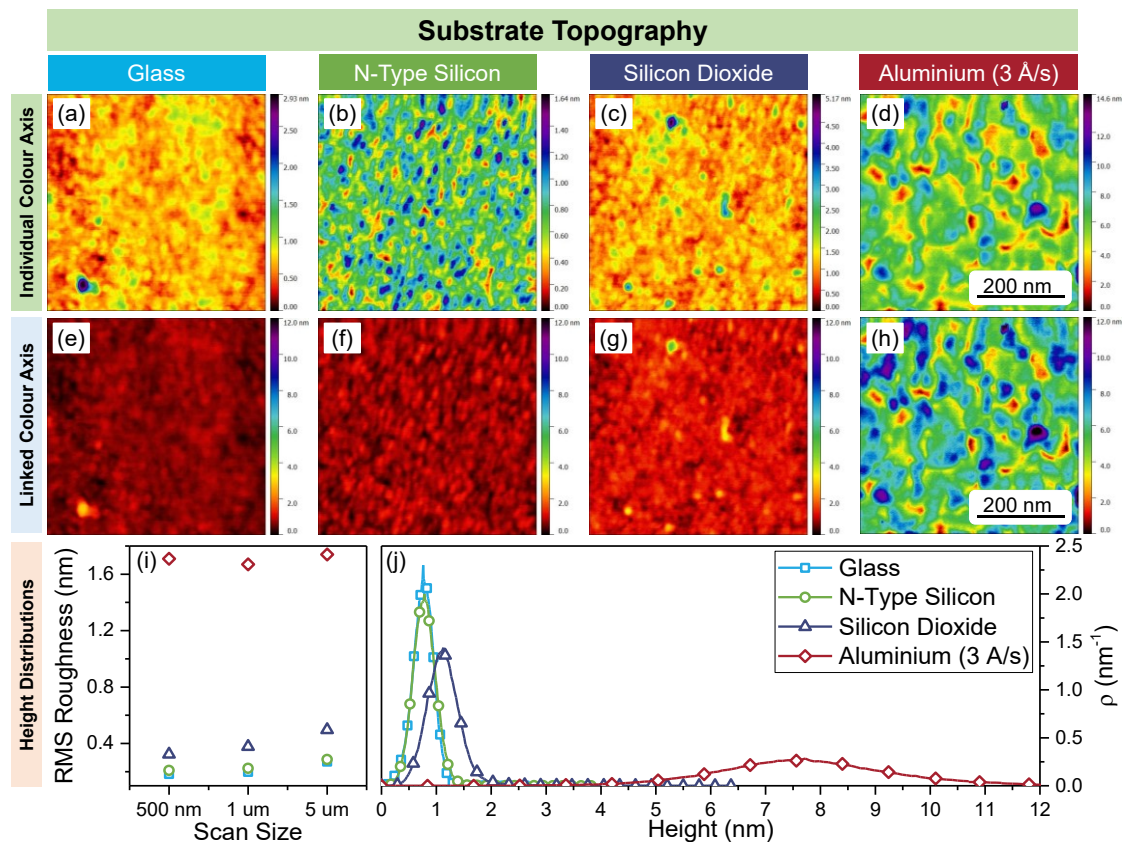


Figure 6.6: Examples of surface roughness for four separate substrates surface: (a),(e) borosilicate glass substrates; (b),(f) heavily doped N-type silicon substrates, (c),(g) 100 nm of silicon dioxide on silicon substrates and (d),(h) thermally evaporated aluminium at a rate of 3 Å/s on glass substrates. The first row of topography images (a)-(d) have individual z colour axes, while the topography images (e)-(h) share the same z colour axis with a maximum value of 12 nm. Also shown is (i) the root mean squared roughness for scan sizes of 500 nm, 1 μm and 5 μm and (j) height distributions for the substrates at the 500 nm scan.

The substrate type chosen for this work, due to its low pricing and mass availability, was glass. To compare the roughness of aluminium contacts produced on glass to other popular substrates, an AFM study on glass, N-type silicon, SiO₂ and the aluminium contacts was performed.

Figure 6.6 demonstrates the surface topography, RMS roughness and height distributions for these four commonly used substrates. From the height distributions in **Figure 6.6** it is obvious that the roughness of glass and N-type silicon are comparable. On the other hand, the previously optimized aluminium deposited at 3 Å/s is over 5 times rougher than either the glass, N-type silicon or SiO₂. The fact that doped silicon is so smooth and can act as a gate contact for TFTs explains why it is the preferred substrate for testing dielectric films.¹⁹¹⁻¹⁹³ Starting with glass substrates necessitates the use of an evaporated contact, in this case aluminium, which then creates a rougher surface for the gate dielectric interface. This places the devices within this work at a disadvantage when compared to devices produced on doped silicon, with a RMS roughness of 1.7 nm on aluminium compared to 0.2 nm on doped silicon. But it strictly follows the fabrication constraints set in Section 6.1.1.

6.3.2 Dielectric Thickness

To measure the thickness of the single and double layer dielectric films, single and double layers of each solution were spin cast onto 100 nm of SiO₂ on highly doped p-type silicon (Si⁺⁺). The fabrication steps were identical to those for spin casting onto the aluminium gate contact on glass substrates. Si⁺⁺/SiO₂ substrates were used due to their well-known optical properties and reflective nature making them ideal for ellipsometry measurements and subsequent modelling. Ellipsometry measurements were performed using a Woolam VASE ellipsometer as outlined in Section 2.3.3 and with the aid of Dr. Ivan Isakov.

Results of fitting to the ellipsometry data are shown in **Figure 6.7**. The thinnest dielectric films were those of AlO_x and ZrO_x at 20 nm and 40 nm for single and double layers respectively. HfO_x films were slightly thicker at 30 nm and 47 nm for single and double layers respectively. The YO_x layer was the thickest at 48 nm and 66 nm for single and double layers. Both HfO_x and YO_x experienced diminishing returns upon addition of a second layer of the precursor solution. For HfO_x the large error bars in thickness, due to roughness over the measurement area, could account for this. Though another possible explanation for both HfO_x and YO_x films is that the

solvent in the second layer of spin casting removed a small amount of the previously deposited film. So far, all layers seem to produce films thick enough to create an effective insulator.

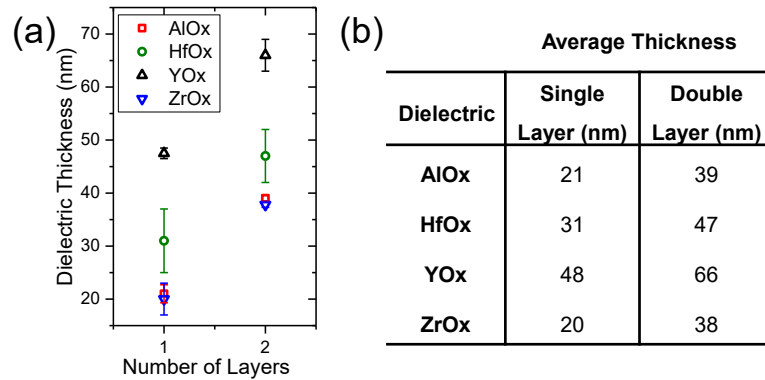


Figure 6.7: Thickness of single and double layers of each of the four dielectrics as measured by ellipsometry, (a) shows the values graphically with experimental error and (b) is a table of the average values.

6.3.3 Interface Topography

To determine the interface roughness between the dielectric and semiconductor AC-AFM was performed, as outlined in Section 2.3.1, on the single and double layers of each dielectric. These layers were produced on aluminium gate contacts on glass substrates. Scans were performed over areas of $500 \text{ nm} \times 500 \text{ nm}$, $1 \text{ }\mu\text{m} \times 1 \text{ }\mu\text{m}$ and $5 \text{ }\mu\text{m} \times 5 \text{ }\mu\text{m}$. The results of these measurements are shown in **Figure 6.8**. The overall trend shows a decreasing roughness upon a secondary spin casting for each film, due to the planarizing effect of the additional spin casting.

The film roughness was lowest for HfOx (double layer RMS 0.30 nm) and YOx (double layer RMS 0.46 nm), with greater values for the ZrOx film (double layer RMS 0.39 nm), and the highest being AlOx (double layer RMS 0.80 nm). The AlOx was particularly rough at larger scan sizes due to peaks in the thermally evaporated aluminium being exacerbated by the extra growth of AlOx. Finally, small crystalline boundaries are observable within the ZrOx, with fainter grain boundaries also observable in the HfOx sample.

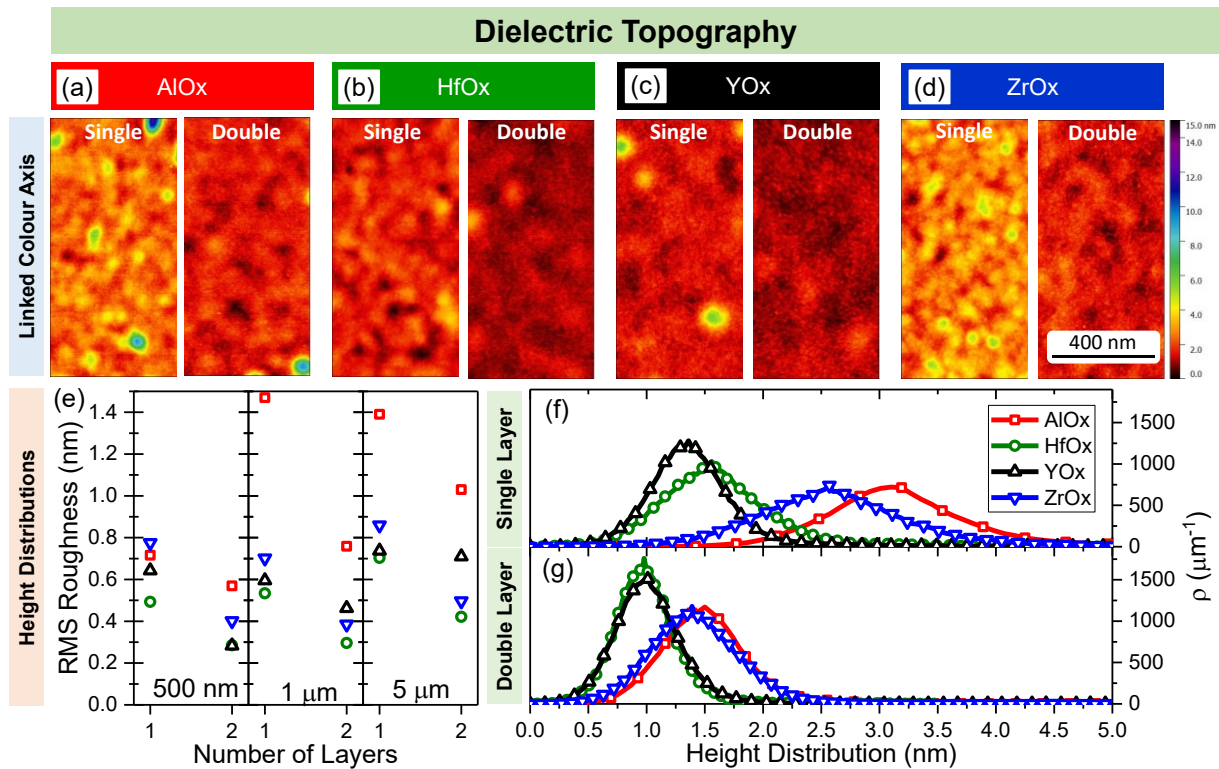


Figure 6.8: Dielectric/semiconductor interface topography and roughness. Top images show the topography of single and double layers of (a) AlOx, (b) HfOx, (c) YOx and (d) ZrOx using a linked z colour axis with a maximum value of 15 nm. (e) RMS roughness for topography scans of single and double layer films at scan sizes of 500 nm, 1 μm and 5 μm. Also included are height distribution plots for (f) single layer and (g) double layer dielectrics at a scan size of 500 nm.

6.4 Electronic Characterisation

6.4.1 Dielectric Impedance Measurements

Capacitance measurements of capacitors with an area 0.64 mm² were performed using a Solartron SI 2160 Impedance/Gain-Phase Analyzer. Three devices for each dielectric were measured in ambient conditions, the results of which are shown in **Figure 6.9**. The capacitance of AlOx and ZrOx films increased with decreasing frequency, likely due to ionic movement within the dielectric. The rapid decrease in capacitance at high frequencies for single layer dielectrics is due to the low pass filter nature of the capacitor and in series resistance of the measurement setup. On the other hand the peaks in capacitance for double layer dielectrics is indicative of a parallel inductance from the coaxial cable. Values for the single and double layer specific capacitances are shown in **Table 6.3**, and were calculated as an average of three devices as measured at 100 Hz in **Figure 6.9**. 100 Hz was chosen as it is comparable with the scan rate of

the TFT measurements. The maximum value of capacitance was for a single ZrOx layer at 567 nF/cm², and a minimum value for a double layer of 125 nF/cm². Even the lowest value of capacitance is nearly an order of magnitude greater than 100 nm of SiO₂ (34.4 nF/cm²). The double layer dielectric always exhibited a decrease in capacitance compared to the single layer dielectric, most of which can be attributed to the increased thickness of the film. Though, the differences in permittivity between double and single layers in **Table 6.3** indicate that the change in capacitance is not just dependent on dielectric film thickness.

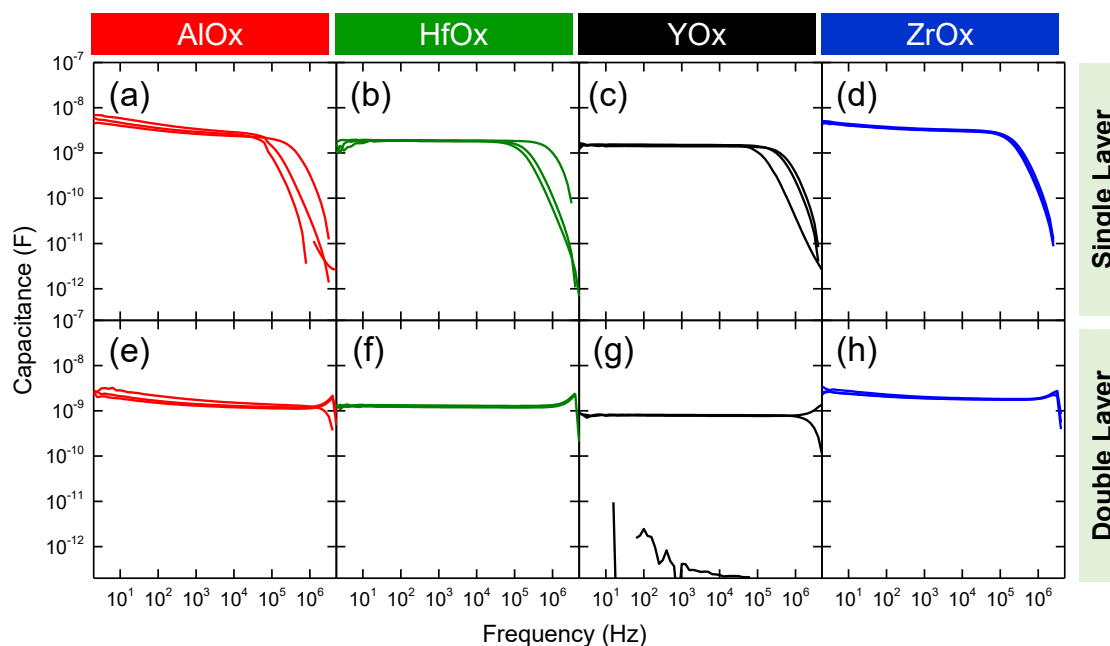


Figure 6.9: Capacitance measurements of diodes made from (a)-(d) single layers and (e)-(h) double layers of: (a),(e) AlOx; (b),(f) HfOx; (c),(g) YOx; and (d),(h) ZrOx. All dielectrics were deposited between two orthogonal strips of aluminium of width 0.8 mm leading to an active area for each device of 0.64 mm².

Table 6.3: Capacitance and permittivities of single and double layers of the four dielectric materials. Values were calculated by averaging the results of three capacitors measured at 100 Hz.

	AlOx		HfOx		YOx		ZrOx	
Parameter	Single	Double	Single	Double	Single	Double	Single	Double
Capacitance (nF/cm ²)	575	275	297	201	235	125	567	336
Thickness (nm)	21	39	31	47	47.5	66	20	38
Relative Permittivity	13.6	12.1	10.4	10.7	12.5	9.4	12.8	14.4

The impedance analyser calculates the real impedance and capacitance from the real and imaginary parts of the complex impedance. It makes the assumption that the capacitor consists of a resistor and capacitor in parallel, and uses this equivalent circuit model to calculate the resistance and capacitor. The results of the real impedance for the single and double layer dielectrics are included in **Figure 6.10**. The impedance of the non-functioning YOx double layer device has a unique form when compared to all other devices.

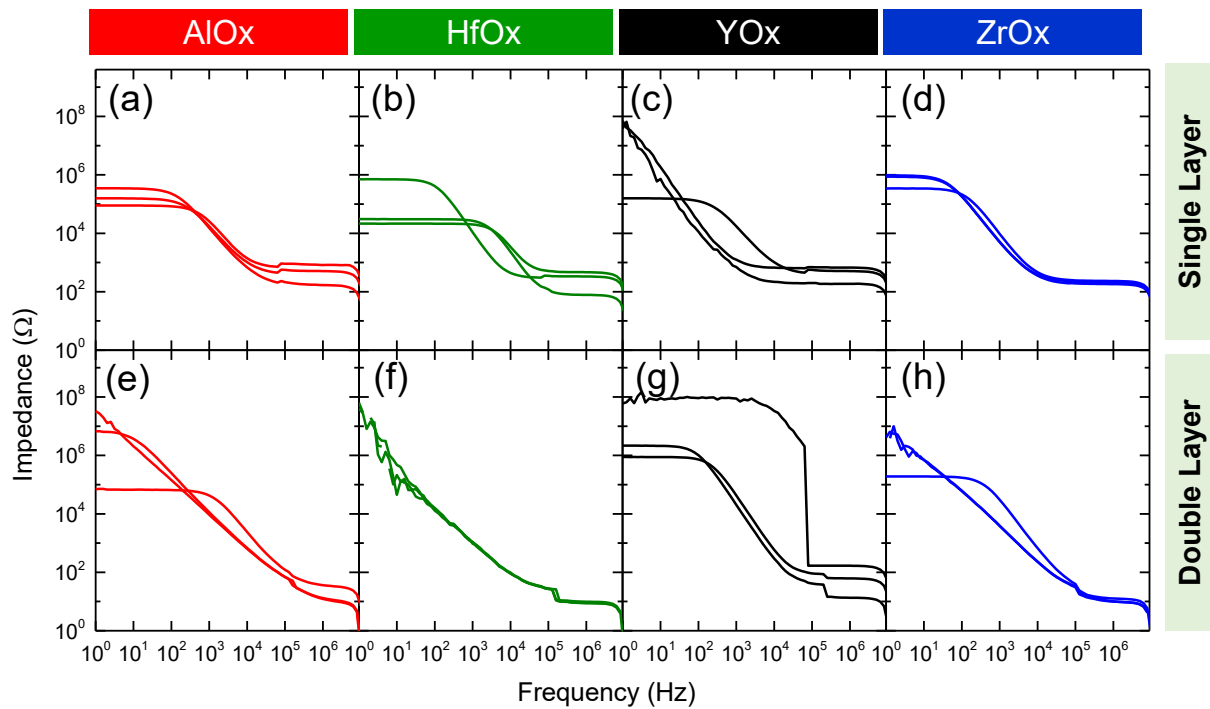


Figure 6.10: Real impedance measurements of capacitors made from (a)–(d) single layers and (e)–(h) double layers of: (a),(e) AlOx; (b),(f) HfOx; (c),(g) YOx; and (d),(h) ZrOx. All dielectrics were deposited between two orthogonal strips of aluminium of width 0.8 mm leading to an active area for each device of 0.64 mm².

6.4.2 Dielectric Breakdown

The equivalent circuits used to calculate the capacitance and impedance of the diodes do not consider a bypass resistance to the capacitor. A bypass resistance models the leakage current through the imperfect insulating layer. To study this leakage current and the dielectric breakdown, two separate additional experiments were performed. Ten capacitors for each dielectric film studied were placed within a nitrogen atmosphere, and then a bias sweep was from 0- 10 V was applied. The breakdown voltage was manually identified by selecting the point at which the current no longer followed a consistent diode like behaviour. The results of the ten

breakdown voltage (V_B) sweeps are visible in **Figure 6.11**(b)-(i), from this the breakdown field (E_B) was calculated using $E_B = V_B/t_{ins}$, where t_{ins} is the dielectric thickness from Section 6.3.2.

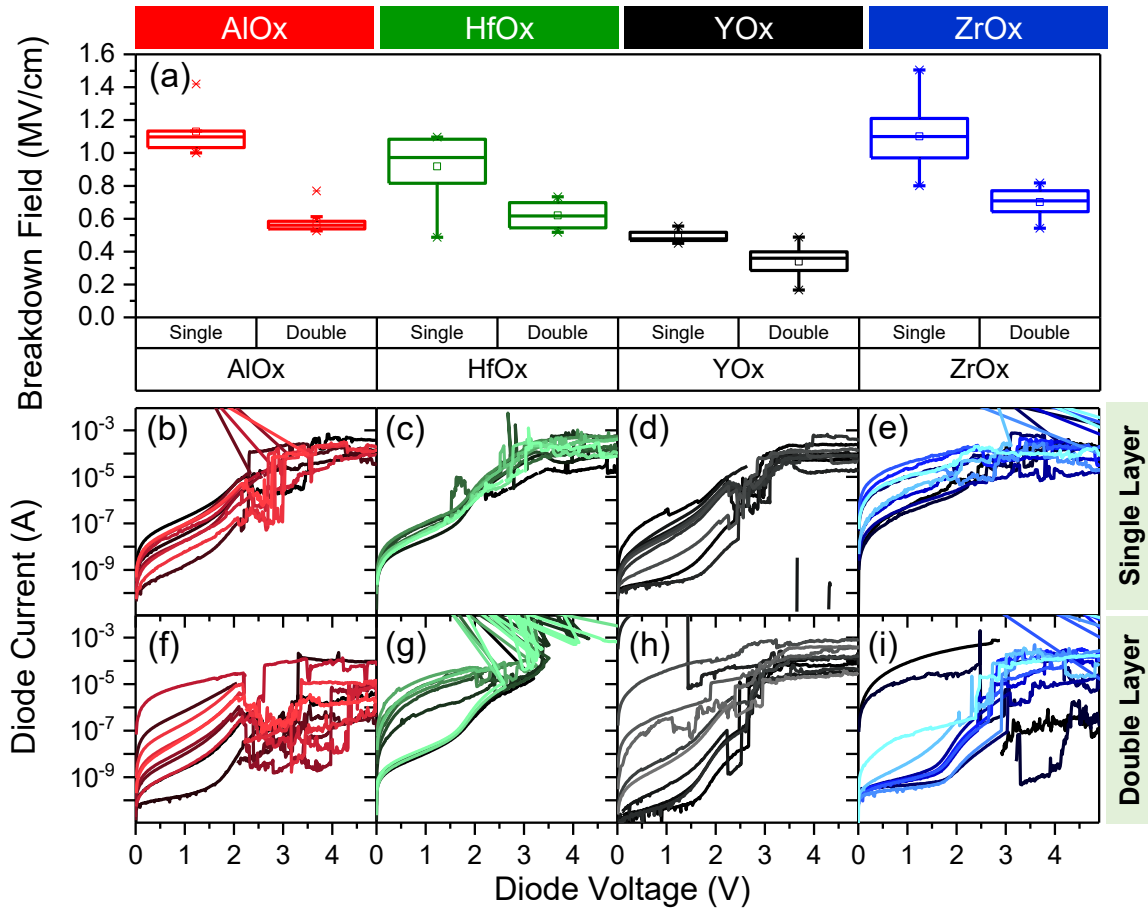


Figure 6.11: Breakdown results for capacitor made of single and double layers of each dielectric and exhibited as (a) box plots. Also included are the ten individual diode tests for each (b)-(e) single layer and (f)-(i) double layer.

For all devices the breakdown voltage increased with the addition of a second layer. But the breakdown field shown in **Figure 6.11** (a), makes it apparent that the breakdown field decreases with the number of layers for each dielectric. This also corresponds to an increased spread of leakage current around 1 V seen in the diode current measurements. The implication of this is that the breakdown field of the dielectric films is based upon the inherent material properties of the film, and is not solely determined by the thickness of the film produced. The ZrOx single layer devices had the highest breakdown field, though the leakage current of the ZrOx single layer was much greater than that of the HfOx single layer, when compared at 1 V. Finally, the YOx had extremely poor breakdown voltages at 0.5 MV/cm for a single layer and less for the double layer.

6.4.3 Transistor Characterisation

Testing of each dielectric layer's performance in the TFT structures consisted of measuring the transfer characteristics as outlined in Section 2.4.1 within a nitrogen atmosphere. Multiple devices of varying channel lengths on multiple substrates were tested to create a random sample of results. Devices were repeatedly tested under increasing voltages until driven to breakdown. This led to measurements for some devices, specifically the HfO_x double layer, reaching much higher gate voltages than other devices.

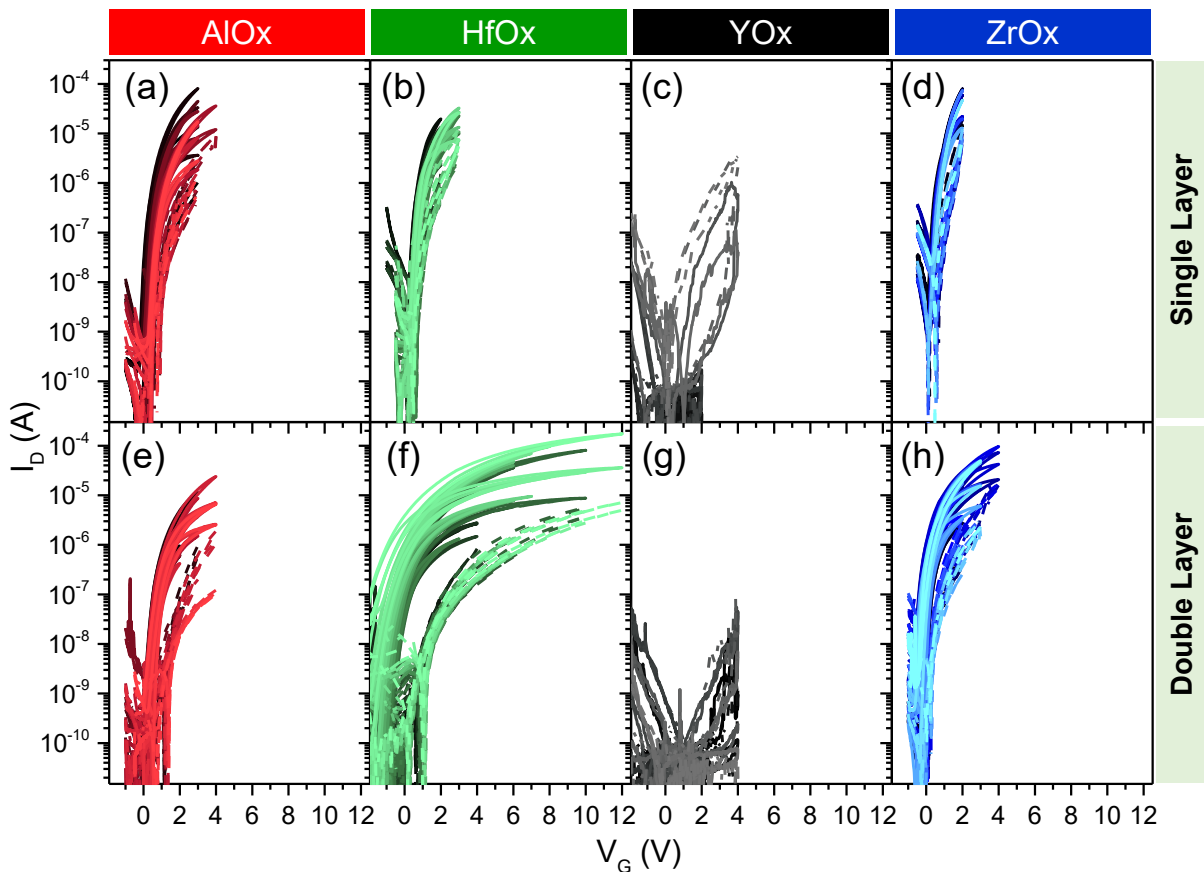


Figure 6.12: Various transfer characteristics of In₂O₃ TFTs produced on single and double layer dielectric devices with set width of 1000 μm and various lengths from 30-50 μm . Drain voltages vary from 0.2-12 V. Solid lines represent measurements performed in the saturation regime, while dashed lines indicate linear regime results. The response of YO_x devices was a result of gate leakage, and not of field effect built up charge.

The results of these mixed transfer characteristics are shown in **Figure 6.12**, and were used as the basis of a statistical analysis of FET mobility in Section 6.4.4. YO_x failed to produce any successful TFTs, unlike the other three successful dielectrics. In general, even though the

breakdown field for double layers was less than that of a single layer, the double layer devices for HfOx and ZrOx were able to be driven to higher gate voltages.

To draw a direct comparison, a single TFT transfer characteristic under identical conditions was selected and plotted in **Figure 6.13**. In this the AlOx and HfOx double layers are observed to have a reduced gate leakage when compared to single layer. In addition, the increase in drain current with gate voltage for all three dielectrics was less for the double layer. This is due to decreased capacitance from the thicker double layer impeding the rate at which charge is accumulated in the channel. For ZrOx, the second spin casting has a lesser effect on the gate leakage when compared to the AlOx and HfOx devices.

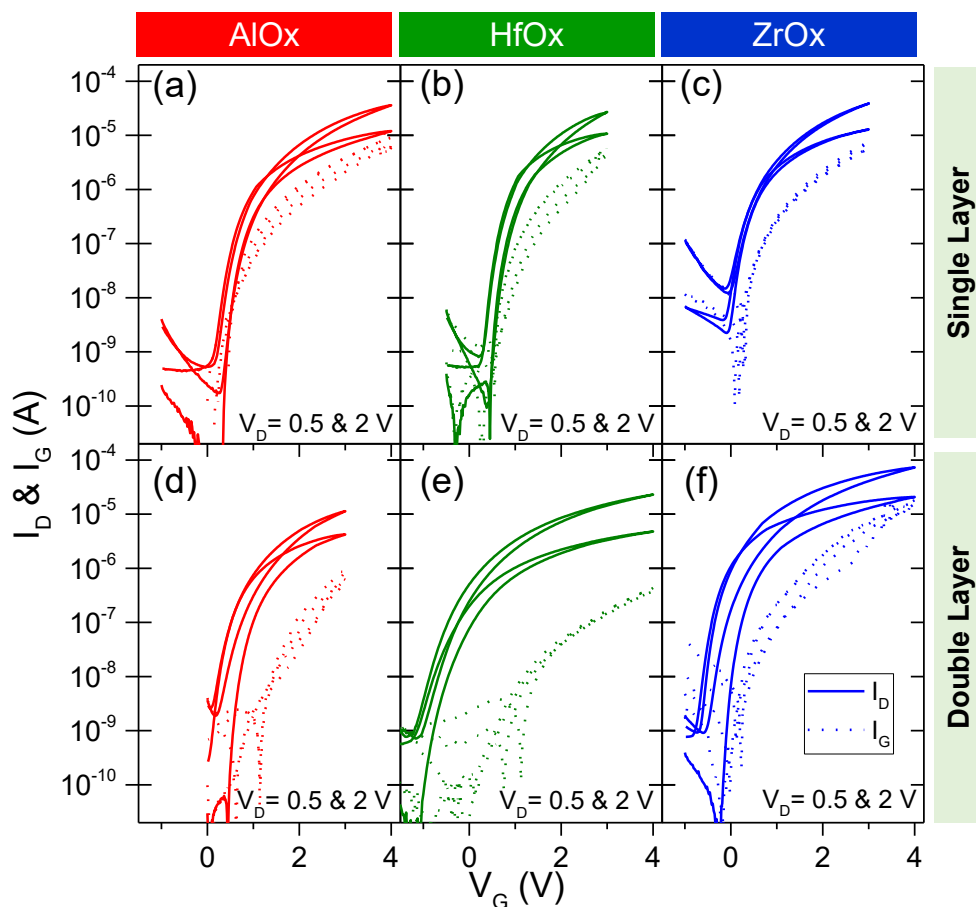


Figure 6.13: Linear ($V_D = 0.5$ V) and saturation ($V_D = 2$ V) transfer characteristics of In_2O_3 transistors produced using the three functioning dielectric materials with (a)-(c) single and (d)-(f) double layer dielectric devices of width $1000 \mu\text{m}$ and length $50 \mu\text{m}$. Solid lines indicate drain current while dashed lines indicate the gate leakage.

The best performing TFT from those tested was that of a double layer of HfOx. This is considered the best device for two reasons. First, it has the lowest gate leakage. Second, the

stability of the dielectric layer under high voltages allowed it to consistently be driven to higher gate voltages than any other TFT.

6.4.4 Field-Effect Transistor Mobility

The Field Effect Transistor (FET) mobility was extracted from the data in **Figure 6.12**, using both linear and saturation mobility calculations for the lower and higher drain voltages respectively as described in Section 3.1.2..

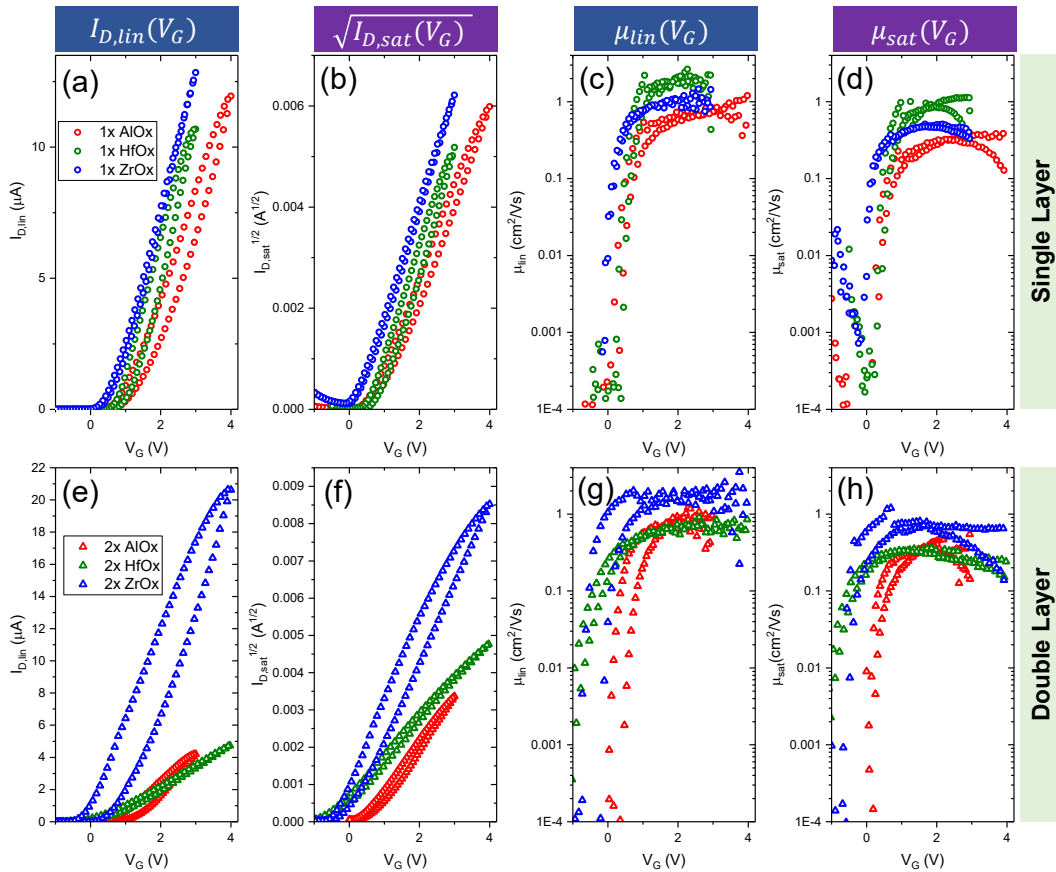


Figure 6.14: Example analysis of In_2O_3 TFTs (from **Figure 6.13**) produced on single (a)-(d) and double (e)-(h) layers of the functioning dielectrics. Included is the linear drain current against gate voltage (a),(e), a square root of the saturated drain current against gate voltage (b),(f), the linear mobility as a function of gate voltage (c),(g), and the saturation mobility as a function of gate voltage (d),(h).

Example analysis of the In_2O_3 TFTs from **Figure 6.13** is provided in **Figure 6.14**. From the linear plots of **Figure 6.14**(a), the ohmic nature of the aluminium contact with the In_2O_3 film is apparent for the devices produced on a single layer of dielectric. The linear plots deviate slightly for the double layer devices in **Figure 6.14**(e), though since the In_2O_3 is identical to that

used for the single device, this is likely an effect of the dielectric and not due to non-ohmic source/drain contacts. The single layer devices have a strong linear correlation between the square root of the saturation current and gate voltage (**Figure 6.14(b)**), which is weaker in the double layer devices (**Figure 6.14(f)**). Differences between the forward and reverse runs in the drain currents for linear and saturation regime measurements is indicative of charging of the TFT. This leads to the variation between forward and reverse mobility calculations seen in **Figure 6.14(c),(d),(g),(h)**. The method used to calculate mobility within this work was by averaging the top values from the mobility against V_G plots.

The resulting values of mobility are shown in the box plots within **Figure 6.15**. In it, the double layer devices have increased mobilities over their single layer counterparts. The explanation for this can be reasoned by the smoother surface of the double layer reducing scattering along the dielectric/semiconductor interface.

Before discussing the dielectric dependence of mobility further, it is worth considering how an inaccurate measurement of the dielectric film capacitance will affect the FET mobility measurement. It is impossible to ensure that the dielectric films used for capacitance measurements are identical to those used for TFT measurements. Variation in the thickness of the dielectric film has already been observed via ellipsometry (**Figure 6.7**), and slight unintentional changes in processing would be expected to increase this further. But since the scatter in mobility (as seen in **Figure 6.15**) is much bigger than any possible error in capacitance, it is possible to state with confidence that the dielectric/semiconductor interface significantly alters the mobility of charge within the channel.

Within **Figure 6.15**, the average mobilities of In_2O_3 on the three double layer dielectrics of AlO_x , HfO_x and ZrO_x were $2 \text{ cm}^2/\text{Vs}$, $6.4 \text{ cm}^2/\text{Vs}$, and $18.7 \text{ cm}^2/\text{Vs}$ respectively. The tuning of semiconductor mobility based on the dielectric interface has been previously reported in ZnO^{23} and quasi-superlattice structures¹²⁸. In both cases a ZrO_x dielectric interface with the semiconductor enhanced the channel mobility when compared to identical SiO_2 based devices. Furthermore, the effect has also been seen with AlO_x films¹⁴⁶, with an increase in channel mobility of an order of magnitude when compared to identical devices fabricated upon SiO_2 . There exist two main arguments to explain how the dielectric material affects the channel mobility. The first is that the metal oxide dielectrics being used can affect the microstructure of the semiconducting layer, with possible epitaxial-like growth on top of the more polycrystalline

dielectric.¹²⁸ The second is that the dielectric helps control the number of interfacial trap states with the semiconductor.¹⁴⁶

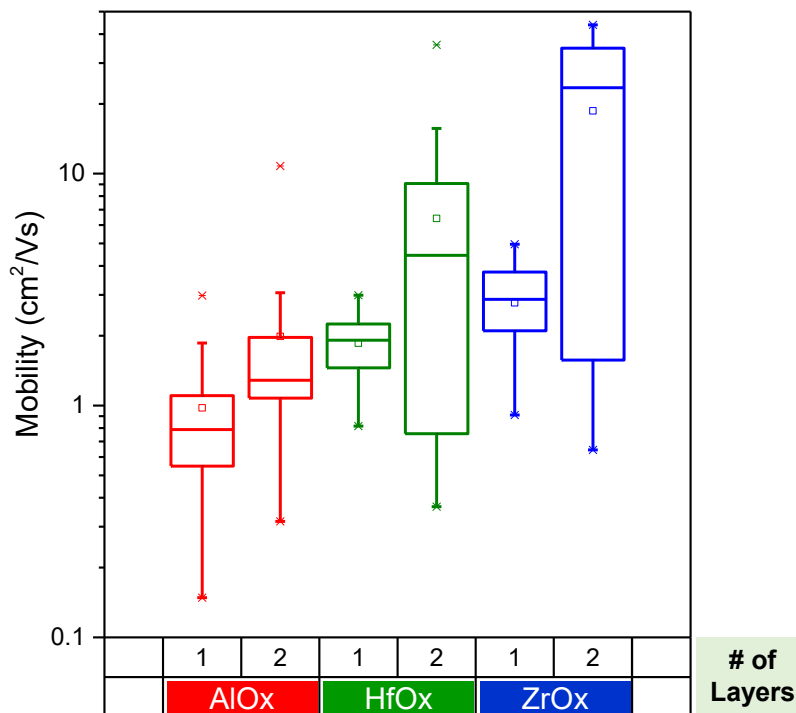


Figure 6.15: Statistical analysis of Field Effect Transistor (FET) mobility for single and double layers of AlOx, HfOx and ZrOx. The transfer characteristics related to these results are displayed in **Figure 6.12**. The boxes contain 50 % of results, excluding outliers, while the whiskers contain all results excluding outliers. The crosses represent the furthest outliers, while the small squares represent the average mobility including outlying points.

The idea that an increased polycrystalline nature in the dielectric can improve growth of the semiconducting layer is consistent with the limited data from within this study. From the AFM topography images in **Figure 6.7**, the ZrOx has obvious grain boundaries in the single layer film, and the HfOx has less pronounced but still present crystalline boundaries. On the other hand, the AlOx exhibits no visible boundaries in the topography images. All of which fits the hypothesis that the dielectric can be used to template improved growth and enhance mobility within the semiconducting channel. Specifically that crystallinity in the dielectric may induce crystallinity within the semiconductor that then increases the channel mobility. This explains why the perceived amorphous AlOx produces the lowest mobility TFTs. This is obviously inconclusive though, and provides an excellent opportunity for further study.

6.4.5 Bandgap Analysis of Dielectrics

To examine the trap states within the semiconductor and search for a possible increase in interfacial trap states as mentioned by Kim et al.¹⁴⁶, a bandgap analysis was performed. Details of the bandgap analysis can be found in Section 4.2. The results of this analysis are shown within **Figure 6.16**, including both the results from the original analysis, and the same results aligned around higher values of the density of states.

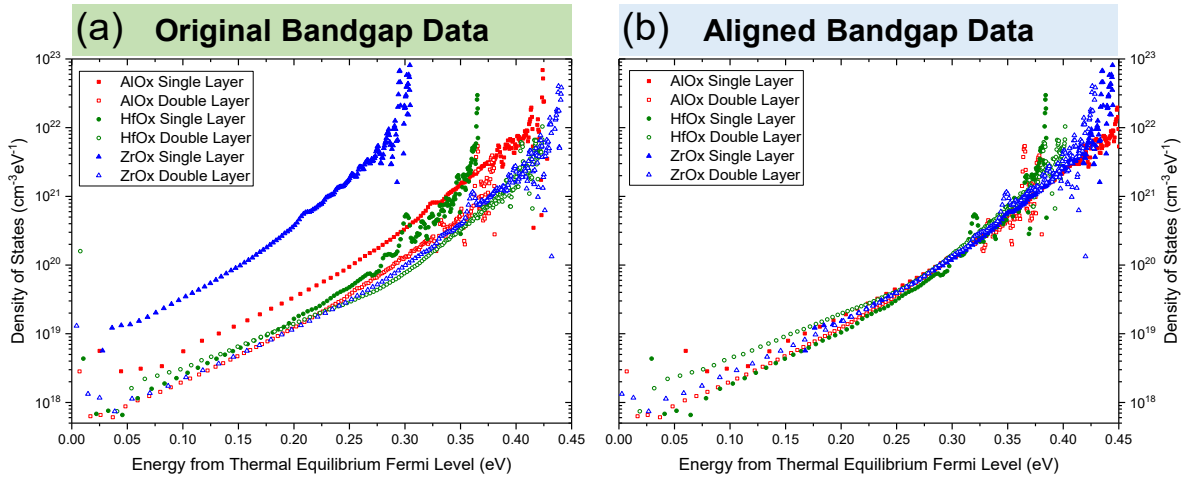


Figure 6.16: Bandgap analysis of the AlO_x, HfO_x and ZrO_x, single and double layers as calculated from the linear transfer characteristics in **Figure 6.13**. (a) The original results from the analysis before alignment and (b) the same results aligned around high values of energy and DOS.

Part of the motivation to perform a bandgap analysis on the three dielectrics producing functional TFTs is to probe the effect of interfacial trap states on the semiconductor. But, the Grünewald analysis as part of its requirements states that the trap states must be uniformly spatially distributed throughout the semiconductor. It is expected that the contribution of any spatially localised trap states will be spread across the whole of the semiconductor by the analysis process. It is also expected that spatially localised trap states will be spread energetically from their original energy. The further into the channel these states are, the more sensitive the calculation of bandgap states will be to them. Therefore, we postulate that a large amount of interfacial trap states between the dielectric and semiconductor will lead to equally significant increases in the measured number of trap states.

The original results of **Figure 6.16** (a) show near identical bandgap density of states for all semiconductors produced on double layer dielectrics. The bandgap states for semiconducting films produced on single layer dielectrics seem to vary greatly, with the AlO_x producing slightly

higher values, and the ZrO_x producing even higher values for the density of states. The explanation for this can be seen in **Figure 6.13**, due to the increased gate leakage causing a high off current in the ZrO_x device, and also increasing the off current in the AlO_x device. As previously mentioned in Section 4.3.5, the bandgap analysis will only produce accurate results on absolute values of energy if the off-current is controlled by the conductance in the semiconductor. Due to the large leakage current for the single layer of ZrO_x, and other dielectric films, this is not the case. Therefore, conclusions should not be drawn on the absolute position of the energetic position of the bandgap states as shown in **Figure 6.16 (a)**.

All six density of states within in **Figure 6.16 (a)** exhibited a similar structure of two exponentials of varying slopes. This is often attributed to tail and deep trap states within the material⁷⁴, but could equally be due to the insensitivity of the bandgap analysis to low densities in the DOS at lower energies. To compare the DOS produced for each result, a least squares fit was performed on the steeper sloped, and higher valued section of the DOS for each dielectric. These were then aligned to produce **Figure 6.16 (b)**. From the aligned data, we see that there is very little difference between the semiconductors' density of states. Noise from the transfer characterisation measurement can be seen in the semiconductor produced on a single layer of HfO_x, but otherwise there is an excellent fit between all semiconducting films.

From these results, it is concluded that the dielectric has not changed the interfacial trap density except for a small amount in the deep trap states. The change in deep trap states could be due to interface roughness with the dielectric, though the trend is not strong enough to draw a definitive conclusion. From these results the bandgap states within the material are unaffected by the selection of the dielectric. This promotes the theory that, for this specific situation, trap states within the semiconductor are intrinsic to the semiconductor, and enhanced microstructure leads to the improved mobility of charge through the TFT channel.

6.5 Summary of High-k Metal Oxide Dielectric

In conclusion we have successfully demonstrated capacitors and TFTs made with the three high-k materials: AlO_x, HfO_x and ZrO_x. Both single and double layers of these three dielectrics were tested using identical fabrication methods, along with single and double layers of YO_x which failed to produce functioning TFTs. The TFTs were produced upon inexpensive glass substrates

and fully solution processed at low-temperatures (≤ 200 °C) with the exception of the thermally evaporated aluminium contacts.

Table 6.4: Comparative results of single and double layers of identically processed AlO_x, HfO_x and ZrO_x.

Parameter	AlO _x		HfO _x		ZrO _x	
	Single	Double	Single	Double	Single	Double
Capacitance (nF/cm ²)	575	275	297	201	567	336
Thickness (nm)	21	39	31	47	20	38
Relative Permittivity	13.6	12.1	10.4	10.7	12.8	14.4
Average Breakdown Field (MV/cm)	1.1	0.6	0.9	0.6	1.1	0.7
Typical On/Off Ratio	10 ⁵	10 ⁵	10 ⁴	10 ⁵	10 ³	10 ⁴
Typical Threshold Voltage (V)	1	0.8	1	-0.3	0.3	0.1
Average FET Mobility (cm ² /Vs)	1.0	2.0	1.9	6.4	2.8	18.7

The functioning dielectric layers exhibited values of capacitance from 201-575 nF/cm², with thicknesses ranging from 20-47 nm. The calculated permittivity for all the dielectrics measured within this work exceeded a relative value of 10, a significant improvement over that of SiO₂ at 3.9. These high values of permittivity and capacitance produced very low voltage TFTs which operated at ≤ 3 V, with on/off ratios of up to 10⁵. A significant increase in mobility was observed within double layer dielectric devices compared to single layer devices. This is attributed to smoother dielectric/semiconductor interfaces due to the planarizing effect of additional spin castings of dielectric. Also, it was observed that the dielectric/semiconductor interface is able to enhance the mobility of charge within the channel of the TFT, the highest value being for In₂O₃ produced on ZrO_x at 18.7 cm²/Vs. The results of experimental characterisation of all three functioning dielectric materials can be found in **Table 6.4**.

Finally, the aim of this study was to identify the best potential precursor candidate for further development in low-temperature plastic substrate based TFTs. Although the mobility enhancing properties of the ZrO_x film makes it a strong competitor, it is the HfO_x double layer film that provides the best overall properties. The HfO_x films exhibited lower gate leakage and greater electrical durability when compared to the ZrO_x films, making it a more reliable and

reproducible dielectric layer. Another possible route for further research would be into bilayer dielectrics. It is hoped that by combining a bottom layer of HfO_x with a secondary layer of ZrO_x it could be possible to harness the mobility enhancement of the ZrO_x with In₂O₃ without compromising the gate leakage.

7 Conclusion

The work within this thesis is split into three topics. Topic one covered the description of the Grünewald bandgap analysis and how to apply it to experimental data. Topic two gave examples of the application of the bandgap analysis to various material systems, both organic and inorganic. Topic three described the fabrication and reporting of experimental devices based on thin film transistor architectures. This Conclusion Chapter shall cover the experimental devices produced and the results from the application of the bandgap analysis. From this, we will extrapolate a set of rules to aid in future design of low-temperature solution processed TFTs.

The first experimental report demonstrated low-temperature (≤ 200 °C), solution-processed D102 dyed films of In_2O_3 in phototransistor structures. Both the responsivity of 2000 A/W and photosensitivity of $\sim 10^6$ is extremely high and comparable to other state-of-the-art phototransistors. This excellent performance was attributed to photodoping and the ultra-thin nature of the In_2O_3 film sensitizing the channel to surface effects. The employed modular phototransistor structure allows for the simple replacement of the small molecule dye with any other dye with a compatible anchoring group. Also, the gating of the phototransistor can be used to tune the optoelectronics for optimal gain and response.

Next the In_2O_3 semiconductor studied further in conjunction with four potential metal oxide dielectrics produced from single and double layers of AlO_x , HfO_x , YO_x and ZrO_x . An identical low-temperature (≤ 200 °C) solution-processed method for all four dielectric precursors involved was carried out to identify the best candidate for optimization and further development. The AlO_x , HfO_x and ZrO_x films all produced functioning TFTs operating at low voltages (≤ 5 V) with the best performing devices exhibiting on/off ratios of 10^5 . The TFTs produced on single and double layers of YO_x were non-functioning. The In_2O_3 mobility is dependent on the dielectric layer, with double layers of AlO_x , HfO_x and YO_x exhibiting average mobilities of $2 \text{ cm}^2/\text{Vs}$, $6 \text{ cm}^2/\text{Vs}$ and $18 \text{ cm}^2/\text{Vs}$ respectively. Although ZrO_x produced the highest mobilities, HfO_x produced from HfCl_4 in 2-methoxyethanol, was nevertheless identified as the optimal candidate due to its low leakage currents and stability.

The bandgap analysis was applied to both the In_2O_3 of the phototransistors and the In_2O_3 of the TFTs produced with metal oxide dielectrics. In the case of the phototransistors, previous reports had described how desorption of molecular oxygen and other surfactants from the

surface of a metal oxide semiconductor can lead to localised doping of the semiconductor. The bandgap analysis of these phototransistors combined with the ultra-thin nature of the In_2O_3 supports this hypothesis. This also provides a possible mechanism for doping undyed ultra-thin In_2O_3 films to control its on-current and turn-on voltage within a TFT.

Additionally, the transfer characteristics of the In_2O_3 TFTs produced on single and double layers of AlO_x , HfO_x and ZrO_x were analysed. After appropriate energetic realignment of the calculated DOS, it was found that the choice of dielectric and the number of layers used had little effect on the density of bandgap states, A0 result also seen within CuSCN devices in Section 4.3.1. The varying leakage current of the different dielectrics was isolated as the main cause of energy shift in the DOS, especially for In_2O_3 semiconductor produced on a single layer of ZrO_x .

Although all the summaries so far are specific to the material system that they have been drawn from, a few guidelines can be extrapolated to aid with the design of future solution-processed TFTs. These guidelines are most applicable to metal oxide devices, but may also be applied to particular small molecule semiconductors with similar multiple trapping and release type transport. The guidelines are as follows:

1) **Controlled and Excessive Doping**

Doping a semiconductor can lead to an increase in the on-current, but it is equally as likely to lead to an increase in the off-current as well (see Sections 4.3.3 and 5.4). Doping itself should not lead to an increase in mobility, but the addition of a dopant may incidentally produce such an effect. Excessive doping can produce extremely high on-currents but will also result in the extremely negative and undesirable turn on voltages. Hence when designing a TFT, where there is a controlled method of doping, it should be used to tune the turn on voltage to 0 V, and no further.

2) **Dielectric Enhancement of Mobility**

In this work, we have demonstrated In_2O_3 devices produced on three metal oxide dielectrics. It was observed that the mobility was dependent not only on the dielectric, but also the number of layers of dielectric deposited. The layer dependence of mobility is explained by the smoother surface of a double layer dielectric. For the material dependence of mobility, two possible mechanisms have been implicated. The first is that increased interfacial trap states decrease the mobility in the semiconductor for certain dielectric/semiconductor combinations. This is not

supported by the applied bandgap analysis reported here. Instead it is assigned to improved microstructure in the semiconductor, templated by the polycrystallinity of the ZrO_x and partial polycrystallinity of HfO_x when compared to AlO_x. When designing TFTs with metal oxide semiconductors it is advisable to select a polycrystalline material for the dielectric layer in an attempt to induce improved microstructure, and enhance mobility. Also, attention must be paid to the roughness of the dielectric/semiconductor interface, so that it is not limiting charge transport laterally across in the channel.

3) **HfO_x Dielectric**

Low-voltage TFTs are preferable due to their ability to run logical operations in complimentary structures at lower power. Within this thesis we have demonstrated the effectiveness of double layer HfO_x films in TFTs. Similar uses of HfCl₄ to produce dielectric films with other solvents has previously been reported. But, the fabrication method described in this work proves effective even with a processing temperature limit of 200 °C. It is therefore highly recommended for further development and should be considered for use in future low-voltage solution-processed TFTs, especially where processing temperature limitations apply.

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Appendix A Charge Density in a MIS Structure

A.1 Electric Field Differential Equation

The charge density in a metal insulator semiconductor (MIS) structure can be calculated by first forming a differential equation in terms of the electric field $F(x)$. The electric field is defined in the x direction between three specific points, namely, $x = -t_{ins}$, the position of the metal/insulator interface, $x = 0$, the position of the insulator/semiconductor interface, and $x = t_{SC}$ is the surface of the semiconductor. In this work the thickness of the insulator t_{ins} and the thickness of the semiconductor t_{SC} are defined as positive.

The process of creating a differential equation in terms of electric field, starts by considering the current density $j(x)$ in the x direction. The first assumption made is that electrons are the majority carrier and that holes do not contribute at all, from this $j(x)$ is given by the sum of drift and diffusion currents:

$$j(x) = q \left(\mu_n n(x) F(x) + D_n \frac{dn(x)}{dx} \right) \quad (88)$$

where $n(x)$ is the carrier density, q is the elementary charge, μ_n is the mobility of the electrons and D_n is the diffusion coefficient.

In equilibrium the current flow is zero at all points such that:

$$\mu_n n(x) F(x) = -D_n \frac{dn(x)}{dx} \quad (89)$$

which can be modified, using Gauss' law:

$$\frac{dF(x)}{dx} = -\frac{qn(x)}{\epsilon_{SC}} \quad (90)$$

where ϵ_{SC} is the permittivity of the semiconductor. Therefore Equation (89) becomes:

$$\mu_n F(x) \frac{dF(x)}{dx} = -D_n \frac{d^2 F(x)}{dx^2} \quad (91)$$

which can be simplified further using Einstein's relation $D_n/\mu_n = k_B T/q$:

$$F(x) \frac{dF(x)}{dx} = -\frac{k_B T}{q} \frac{d^2 F(x)}{dx^2}. \quad (92)$$

The left-hand side of Equation (92) can be packaged all into a single differential using the chain rule:

$$\frac{1}{2} \frac{dF^2(x)}{dx} = -\frac{k_B T}{q} \frac{d^2 F(x)}{dx^2} \quad (93)$$

and by integrating over both sides and rearranging it leads to the generalized differential equation for the electric field in a thin film:

$$\frac{2k_B T}{q} \frac{dF(x)}{dx} + F^2(x) = -\left(\frac{2k_B T}{q}\right)^2 g^2 \quad (94)$$

where g^2 is a constant of integration. The term $((2k_B T)/q)^2$ in front of the g^2 is allowed to be added as it merely modifies the constant of integration and helps make it simpler to solve for $F(x)$.

A.2 General Film Solution

The general solution to Equation (94) is:

$$F(x) = \frac{2k_B T g}{q} \cot(g(x + x_0)) \quad (95)$$

where x_0 is a constant of integration that is calculable from boundary conditions. The voltage within the semiconductor $V_{SC}(x)$ is related to the electric field via:

$$F(x) = -\frac{dV_{SC}(x)}{dx} \quad (96)$$

which means the voltage within the semiconductor is given by:

$$V_{SC}(x) = -\frac{2k_B T}{q} \left[\ln |\sin(g(x + x_0))| \right] + k \quad (97)$$

where k is a constant of integration. Using the boundary condition that is true both for thick and thin semiconductor films, that $V_{SC}(t_{SC}) = 0$, then:

$$V_{SC}(x) = -\frac{2k_B T}{q} \left[\ln \left| \frac{\sin(g(x + x_0))}{\sin(g(t_{SC} + x_0))} \right| \right]. \quad (98)$$

The value of x_0 which is the characteristic length of decay within the semiconductor can be calculated using the boundary condition that the electric field at the semiconductor edge must be zero $F(t_{SC}) = 0$. Since $\cot(u)$ repeats every π with a singularity at $n\pi$ where n covers each all integers, we can define a range for u : $0 \rightarrow \pi$. Therefore $\cot(u) = 0$ when $u = \pi/2$ hence,

$$\frac{\pi}{2} = g(t_{SC} + x_0) \quad (99)$$

which transforms Equations (95) & (98) into:

$$F(x) = \frac{2k_B T g}{q} \tan(g(t_{SC} - x)) \quad (100)$$

and

$$V_{SC}(x) = -\frac{2k_B T}{q} \ln|\cos(g(t_{SC} - x))|. \quad (101)$$

The second boundary condition that defines the electric field at the insulator semiconductor interface $F(x = 0) = F_0$. This allows for the numerical calculation of the value of g :

$$\frac{qF_0}{2k_B T} \frac{1}{g} = \tan(gt_{SC}) \quad (102)$$

where the value of gt_{SC} is also limited between 0 & $\pi/2$.

A.2.1 Avoiding the Voltage Drop Approximation

Equation (102) can be used to calculate g numerically, but requires the field at the insulator/semiconductor interface, which is not experimentally known. Often this value will be approximated using the ‘‘Voltage Drop’’ approximation (VDA), where it is argued that the majority of the voltage will be dropped over the insulator. This allows the user to calculate the electric field in the insulator as $F_{ins} = V_G/t_{ins}$, where V_G is the gate voltage and t_{ins} is the thickness of the dielectric layer. Combining this with conservation of displacement field at the semiconductor/insulator interface i.e. at $x = 0$ gives $F_0 = \epsilon_{ins}V_G/\epsilon_{SC}t_{ins}$ where ϵ_{ins} and ϵ_{SC} are the permittivity of the insulator and semiconductor respectively.

This approximation can be avoided using the fact that voltage is continuous across the interface, even if the first derivative is not continuous. Since all the voltage must be dropped over the whole of the device the gate voltage V_G is:

$$V_G = V_{SC}(0) + F_{ins}t_{ins} \quad (103)$$

and when combined with Equation (101) gives the electric field at the insulator semiconductor interface as:

$$F_{ins} = \frac{2k_B T}{qt_{ins}} \ln|\cos(gt_{SC})| + \frac{V_G}{t_{ins}}. \quad (104)$$

From this, conservation of displacement field can be used again to calculate the value of F_0 to give:

$$F_0 = \frac{V_G \epsilon_{ins}}{t_{ins} \epsilon_{SC}} + \frac{2k_B T \epsilon_{ins}}{qt_{ins} \epsilon_{SC}} \ln|\cos(gt_{SC})|. \quad (105)$$

Equation (105) shows that the electric field at the interface is equal to the electric field expected using the VDA minus a compensation (since $\cos(u) \leq 1$ then $\ln(\cos(u)) \leq 0$). The compensation is dependant on the materials, and thickness of the materials used and becomes more prominent with decreasing insulator thickness.

Equation (105) also states that the electric field at the interface is dependent on the value of g as well, which is unsurprising. By inserting Equation (105) into Equation (102) a new expression to obtain the value of g is produced that no longer includes the electric field at the interface:

$$\ln|\cos(gt_{SC})| - \frac{t_{ins}\epsilon_{SC}}{\epsilon_{ins}} g \tan(gt_{SC}) + \frac{qV_G}{2k_B T} = 0. \quad (106)$$

One further simplification can be made to Equation (106) by using the definition of specific capacitance $C_{ins} = \epsilon_{ins}/t_{ins}$ to give:

$$\ln|\cos(gt_{SC})| - \frac{\epsilon_{SC}}{C_{ins}} g \tan(gt_{SC}) + \frac{qV_G}{2k_B T} = 0. \quad (107)$$

A.2.2 Using the Voltage Approximation Drop

When using the voltage drop approximation the field at the insulator semiconductor interface is given by just:

$$F_0 = \frac{V_G \epsilon_{ins}}{t_{ins} \epsilon_{SC}} \quad (108)$$

which can be reinserted into Equation (102). By doing this a new numerical function for calculating g is found:

$$\tan(gt_{SC}) - \frac{qV_G C_{ins}}{2k_B T \epsilon_{SC}} \frac{1}{g} = 0 \quad (109)$$

which replaces Equation (107).

A.2.3 Summary of General Film Solution Equations

In summary, numerical methods may be used to calculate the value of g either by using the equation:

$$\ln|\cos(gt_{SC})| - \frac{\epsilon_{SC}}{C_{ins}} g \tan(gt_{SC}) + \frac{qV_G}{2k_B T} = 0 \quad (110)$$

which is the full solution and may be used even at low voltages. For larger voltages VDA may be made, stating that all the voltage is dropped across the insulator, in which case g can be calculated from the equation:

$$\tan(gt_{SC}) - \frac{qV_G C_{ins}}{2k_B T \epsilon_{SC}} \frac{1}{g} = 0. \quad (111)$$

The value of g may then be used to calculate the electric field ($F_{SC}(x)$), voltage ($V_{SC}(x)$), and carrier density ($n_{SC}(x)$). For these equations, the subscripts SC have been used to avoid confusion with the electric field and voltage within the insulator. The following equations recap those calculated early in this section, and calculate the carrier density using Gauss's law:

$$F_{SC}(x) = \frac{2k_B T g}{q} \tan(g(t_{SC} - x)) \quad (112)$$

$$V_{SC}(x) = -\frac{2k_B T}{q} \ln|\cos(g(t_{SC} - x))| \quad (113)$$

$$n_{SC}(x) = \frac{2k_B T \epsilon_{SC} g^2}{q^2} \sec^2(g(t_{SC} - x)). \quad (114)$$

A.3 Thick Film Approximation Solution

The thick film approximation provides a simpler if less accurate solution to Equation (94). It states that in a thick film both the electric field will tend to zero smoothly towards the semiconductor surface and hence both the electrical field, and the differential of the electrical field at the surface are zero, ($F(t_{SC}) = 0$ & $dF(t_{SC})/dx = 0$). From this the value of g in Equation (94) must be zero, so Equation (94) becomes:

$$\frac{2k_B T}{q} \frac{dF(x)}{dx} + F^2(x) = 0 \quad (115)$$

which leads to the simple solution that:

$$F(x) = \frac{2k_B T}{q} \frac{1}{(x + x_0)} \quad (116)$$

where x_0 is a constant to be calculated from boundary conditions.

By using the boundary condition that $F(x = 0) = F_0$ then $x_0 = +2k_B T/qF_0$, hence Equation (116) is:

$$F(x) = \frac{2k_B T}{q} \frac{1}{x + \frac{2k_B T}{qF_0}} \quad (117)$$

from which the voltage in the semiconductor can be calculated as:

$$V_{SC}(x) = \frac{2k_B T}{q} \ln \left| x + \frac{2k_B T}{qF_0} \right| + k \quad (118)$$

where k is a constant of integration. To solve for k , we require another boundary condition, namely $V(x = t_{SC}) = 0$ to give:

$$V_{SC}(x) = \frac{2k_B T}{q} \ln \left| \frac{x + \frac{2k_B T}{qF_0}}{t_{SC} + \frac{2k_B T}{qF_0}} \right|. \quad (119)$$

A.3.1 Avoiding the Voltage Drop Approximation

To calculate the voltage drop over the insulator and semiconductor in turn, Equation (119) must be inserted into Equation (103) at $x = 0$, leading to the equation:

$$V_G = \frac{2k_B T}{q} \ln \left| \frac{\frac{2k_B T}{qF_0}}{t_{SC} + \frac{2k_B T}{qF_0}} \right| + F_{ins} t_{ins}. \quad (120)$$

Using conservation of displacement field to replace F_{ins} in Equation (120) gives:

$$\ln \left| \frac{2k_B T}{q} + t_{SC} F_0 \right| - \frac{q \epsilon_{SC}}{2k_B T C_{ins}} F_0 + \frac{q V_G}{2k_B T} - \ln \left| \frac{2k_B T}{q} \right| = 0 \quad (121)$$

which can be solved by numerical methods to calculate F_0 .

A.3.2 Summary of Thick Film Solution

For the thick film solution there is no value of g unlike the general solution. Instead the electric field at the insulator semiconductor interface (F_0) is the controlling factor to calculate the voltage, electric field and charge carrier density within the material. When using the charge drop approximation the value of F_0 is simply:

$$F_0 = \frac{V_G C_{ins}}{\epsilon_{SC}} \quad (122)$$

but to take into account the voltage dropped in the semiconductor the equation:

$$\ln \left| \frac{2k_B T}{q} + t_{SC} F_0 \right| - \frac{q \epsilon_{SC}}{2k_B T C_{ins}} F_0 + \frac{q V_G}{2k_B T} - \ln \left| \frac{2k_B T}{q} \right| = 0 \quad (123)$$

must be solved for F_0 instead.

Once a value for F_0 has been gained, the electric field, voltage, and charge carrier density can be calculated from the following equations:

$$F_{SC}(x) = \frac{2k_B T}{q} \frac{1}{x + \frac{2k_B T}{qF_0}} \quad (124)$$

$$V_{SC}(x) = \frac{2k_B T}{q} \ln \left| \frac{x + \frac{2k_B T}{qF_0}}{t_{SC} + \frac{2k_B T}{qF_0}} \right| \quad (125)$$

$$n_{SC}(x) = \frac{2k_B T \epsilon_{SC}}{q^2} \frac{1}{\left(x + \frac{2k_B T}{qF_0}\right)^2}. \quad (126)$$

Appendix B Grünewald Analysis Derivation

During previous derivations $V(x)$ has been used to describe the internal potential within the semiconductor. In the derivation below, the internal potential will be symbolized by $\phi(x)$.

B.1 Density of Bandgap States

The aim of the Grünewald analysis is to calculate the bandgap density of states from the transfer characteristics of a TFT. It uses the sweeping gate voltage of the TFT to fill, incrementally, the density of states within the device. This will in turn fill the conduction band with mobile charge carriers. Not all accumulated charge is injected into the conduction band, as first bandgap states below the conduction band must be filled in accordance to Fermi-Dirac statistics.

The number of charge carriers within the bandgap states is given by:

$$n_{BG}(E_F) = \int_{-\infty}^{\infty} g_{BG}(E) f(E - E_F) dE \quad (127)$$

where $f(E - E_F)$ is the Fermi function, $n_{BG}(E_F)$ is the number of filled bandgap states at specific Fermi level position E_F and $g_{BG}(E)$ is the density of bandgap states within the material. Within this convolution, the Fermi function is well known and the density of states is what we would like to calculate. Any derivation must therefore calculate the number of filled states over a range of energies to deconvolute the right hand side of Equation (127).

When calculating the electronic structure within TFTs band bending is often used to describe how the conduction band is pulled below the non-varying Fermi level to increase the occupation of states within the conduction band. This description is identical to saying that the Fermi level is increased and driven into the non-varying conduction band to cause the same effect. In this work, we shall use the latter description as it is more robust. The Fermi level in a material is defined as the point at which the fractional occupancy of states is exactly $\frac{1}{2}$, and this will be a function dependent on applied gate voltage and position within the semiconductor ($E_F(x, V_G)$).

It is useful to define the term thermal equilibrium Fermi level, or flat-band Fermi level (E_{FB}). This is the Fermi level within the semiconductor in a vacuum with no other interfaces to other materials and at thermal equilibrium (i.e. no external applied voltages or injected charge). This is also the Fermi level within the semiconductor when there is zero band bending which is

also called flat-band voltage. A common assumption made within device physics is that the flat-band voltage of the device occurs at the turn on voltage (V_{on}). This is useful as it allows us to say that $E_F = E_{FB}$ when $V_G = V_{on}$.

The usefulness of E_{FB} is the fact that it is independent of position, and so can be combined with an internal potential $\phi(x)$ that is spatially varied. Therefore, the Fermi level E_F is given by:

$$E_F(x, V_G) = E_{FB} + \phi(x, V_G). \quad (128)$$

From this we also know that $E_{FB} = E_{FB} + \phi(x, V_G = V_{on})$, so $\phi(x, V_G = V_{on}) = 0$. This is often simplified by defining a new shifted gate voltage $V_G' = V_G - V_{on}$ so that $\phi(x, V_G = 0) = 0$. In this work, we will assume that this shift in the gate voltage has already been made within the experimental data and therefore not use V_G' . If E_{FB} is set to equal zero, the number of charge carriers in bandgap states can be rewritten as:

$$n_{BG}(\phi(x, V_G)) = \int_{-\infty}^{\infty} g_{BG}(E) f(E - \phi(x, V_G)) dE. \quad (129)$$

This may seem like a minor change from Equation (127) but means we require a function of n_{BG} in terms of internal potential as opposed to Fermi level.

Since the internal potential is a function of both space and the applied gate voltage, an arbitrary spatial position to place this function must be chosen. The most convenient position to use would be $x = 0$ at the semiconductor/dielectric interface as it allows for an easy relationship to be formed between ϕ_0 and V_G . Therefore, the function that we will need to calculate via other means to perform the deconvolution is therefore $n_{BG}(\phi_0(V_G))$ where $\phi_0 = \phi(x = 0, V_G)$.

B.2 Conduction Band and Drain Current

The drain current $I_D(V_G)$ as a function of gate voltage within a transistor can be described mathematically as:

$$I_D(V_G) = \frac{qV_D\mu_{CB}W}{L} \int_0^{t_{SC}} n_{CB}(\phi(V_G, x)) dx \quad (130)$$

where W and L are the width and length of the TFT, V_D is the drain voltage, μ_{CB} is the mobility of charge carriers within the conduction band and t_{SC} is the thickness of the semiconductor. Finally $n_{CB}(\phi(V_G, x))$ is the density of charge carriers in the conduction band, which is a function of both distance x from the semiconductor/dielectric interface and the applied gate voltage both of which are expressed through the internal potential ϕ .

To calculate the number of charge carriers within the conduction band and how that value changes with the internal potential, an assumption about the conduction band shape must be made. This model assumes that the conduction band is a Heaviside function:

$$g_{CB}(E) = \begin{cases} 0, & E < E_{CB} \\ g_{CB_0}, & E \geq E_{CB} \end{cases} \quad (131)$$

where g_{CB} is the density of states and g_{CB_0} is the value of the density of states above the conduction band edge E_{CB} . The density of charge in the conduction band is therefore:

$$n_{CB}(\phi) = \int_{-\infty}^{\infty} g_{CB}(E) f(E - E_{FB} - \phi(V_G, x)) dE \quad (132)$$

where $f(E - E_{FB} - \phi(V_G, x))$ is the Fermi function and E_{FB} is the position of the Fermi level at flat band voltage. This integral can be simplified to:

$$n_{CB}(\phi) = g_{CB_0} \int_{E_{CB}}^{\infty} f(E - E_{FB} - \phi(V_G, x)) dE \quad (133)$$

and by explicitly including the Fermi function:

$$n_{CB}(\phi) = g_{CB_0} \int_{E_{CB}}^{\infty} \frac{1}{1 + \exp(\beta(E - E_{FB} - \phi(V_G, x)))} dE \quad (134)$$

where $\beta = 1/k_B T$; k_B and T being the Boltzmann constant and temperature in turn.

This integral can be simplified heavily if $\exp(\beta(E - E_{FB} - \phi(V_G, x))) \gg 1$ for all values of E . Since the minimum value of $E = E_{CB}$ we gain the condition that $\beta(E_{CB} - E_{FB} - \phi(V_G, x)) \gg 0$. Since the Fermi level at a point x in semiconductor is given by the $E_F = E_{FB} + \phi(V_G, x)$, this condition essentially requires that the Fermi level not go near or enter the conduction band. From this Equation (134) simplifies to:

$$n_{CB}(\phi) = g_{CB_0} \int_{E_{CB}}^{\infty} \exp(-\beta(E - E_{FB} - \phi(V_G, x))) dE \quad (135)$$

and when integrated gives to:

$$n_{CB}(\phi) = \frac{g_{CB_0}}{\beta} e^{-\beta(E_{CB} - E_{FB} - \phi(V_G, x))}. \quad (136)$$

By combining Equations (130) & (135) the drain current is given by:

$$I_D(V_G) = \frac{V_D \mu_{CB} W}{L} \frac{g_{CB_0}}{\beta} e^{-\beta(E_{CB} - E_{FB})} \int_0^{t_{SC}} e^{\beta \phi(V_G, x)} dx \quad (137)$$

where the terms in front of the spatial integral may be combined into a simple single term of I_{off}/t_{SC} :

$$I_D(V_G) = \frac{I_{off}}{t_{SC}} \int_0^{t_{SC}} e^{\beta \phi(V_G, x)} dx. \quad (138)$$

The next manipulation of Equation (138) will seem enigmatic for the time being. Its use will be to avoid an artificial singularity in the integral due to an approximation later in the

derivation. Hence we divide through by the off current and then subtract 1 from either side of Equation (138) to leave:

$$\frac{I_D(V_G)}{I_{off}} - 1 = \frac{1}{t_{SC}} \int_0^{t_{SC}} (e^{\beta\phi(V_G,x)} - 1) dx. \quad (139)$$

This is a spatial integral where an explicit spatial function of ϕ would be required to solve it. One method of circumnavigating the spatial integral is by changing it to one over ϕ instead as follows:

$$\frac{I_D(V_G)}{I_{off}} - 1 = \frac{1}{t_{SC}} \int_0^{t_{SC}} (e^{\beta\phi(V_G,x)} - 1) \frac{dx}{d\phi} \frac{d\phi}{dx} dx \quad (140)$$

which can then be simplified further to:

$$\frac{I_D(V_G)}{I_{off}} - 1 = \frac{1}{t_{SC}} \int_{\phi(0)}^{\phi(t_{SC})} \frac{(e^{\beta\phi(V_G,x)} - 1)}{\phi'(V_G,x)} d\phi \quad (141)$$

where $\phi' = d\phi/dx$, $\phi(t_{SC})$ is the potential at the semiconductor surface, and $\phi(0)$ is the potential at the semiconductor/dielectric interface. To solve Equation (141) we have to replace ϕ' with an equivalent function in terms of just ϕ . Which is exactly the sort of relationship produced when solving Gauss' Law.

B.3 Internal Potential from Gauss' Law

To calculate a relationship between ϕ' and ϕ we start with Gauss' law:

$$\frac{d}{dx}(\phi'(x)) = \frac{qn(\phi(x))}{\epsilon_{SC}} \quad (142)$$

where ϵ_{SC} is the permittivity of the semiconductor and $n(\phi(x))$ is the total number of charge carriers (both in the conduction band and bandgap states). Note that a somewhat flexible usage of permittivity has been adopted; in this case it is referring to the absolute permittivity. Next we multiply both sides of Equation (142) by $\phi'(x)$, the purpose of which will become apparent soon:

$$\phi'(x) \frac{d}{dx}(\phi'(x)) = \frac{qn(\phi(x))}{\epsilon_{SC}} \phi'(x). \quad (143)$$

A small rearrangement maybe performed on the left-hand side to produce:

$$\frac{1}{2} \frac{d}{dx}((\phi'(x))^2) = \frac{qn(\phi(x))}{\epsilon_{SC}} \phi'(x). \quad (144)$$

The differential on the left-hand side can now be removed by integrating both sides between two spatial points:

$$\left[(\phi'(x))^2 \right]_{x_a}^{x_b} = \int_{x_a}^{x_b} \frac{2qn(\phi(x))}{\epsilon_{SC}} \frac{d\phi}{dx} dx \quad (145)$$

at which point the $\phi'(x)$ on the right-hand side allows the integral to be changed to one over the internal potential at the specific points x_a and x_b :

$$(\phi'(x_b))^2 - (\phi'(x_a))^2 = \frac{2q}{\epsilon_{SC}} \int_{\phi(x_a)}^{\phi(x_b)} n(\phi(x)) d\phi. \quad (146)$$

Careful selection of spatial points of $x_a = x$ as generalized position of x and $x_b = t_{SC}$ at the semiconductors surface produces:

$$(\phi'(x))^2 - (\phi'(t_{SC}))^2 = \frac{2q}{\epsilon_{SC}} \int_{\phi(t_{SC})}^{\phi(x)} n(\phi(x)) d\phi \quad (147)$$

where $\phi(t_{SC}) = 0$ from the boundary condition that there is no internal potential at the semiconductor surface:

$$(\phi'(x))^2 - (\phi'(t_{SC}))^2 = \frac{2q}{\epsilon_{SC}} \int_0^{\phi(x)} n(\phi(x)) d\phi. \quad (148)$$

By creating a new function $T(\phi(x))$ defined as:

$$T(\phi(x)) = \int_0^{\phi(x)} n(\phi(x)) d\phi \quad (149)$$

we can rearrange Equation (148) to give:

$$\phi'(x) = -\sqrt{\frac{2q}{\epsilon_{SC}} T(\phi(x)) + (\phi'(t_{SC}))^2} \quad (150)$$

where the negative sign is chosen as it is expected that the internal potential decreases from the semiconductor-dielectric interface to the semiconductor surface. This has produced $\phi'(x)$ as a function of the newly defined function $T(\phi(x))$ and the differential of the internal potential at the semiconductor surface. Note that although the boundary condition that $\phi(t_{SC}) = 0$, we do not assume that $\phi'(t_{SC}) = 0$. This is the same as the thick film approximation where, since the electric field $F(t_{SC}) = -d\phi(t_{SC})/dx$, the electric field is non-zero at the semiconductor surface (visually shown in **Figure 4.3**).

B.4 Interface Potential and Gate Voltage

So far our relationships between ϕ' and ϕ are functions of space, but as discussed in Appendix B.1 we need to choose an arbitrary position to solve these functions. The obvious value of x to solve it is at $x = 0$. From this Equation (150) becomes:

$$\phi'_0(V_G) = -\sqrt{\frac{2q}{\epsilon_{SC}} T(\phi_0(V_G)) + (\phi'(t_{SC}))^2} \quad (151)$$

where $\phi'_0(V_G) = \phi'(V_G, x = 0)$ and $\phi_0(V_G) = \phi(V_G, x = 0)$. Since the electric field in the semiconductor F_{SC} (as opposed to the dielectric) is $F_{SC}(x) = -d\phi/dx$, then:

$$F_{SC_0}(V_G) = \sqrt{\frac{2q}{\epsilon_{SC}} T(\phi_0(V_G)) + (\phi'(t_{SC}))^2} \quad (152)$$

where $F_{SC_0} = F_{SC}(x = 0)$. If F_{ins} is the electric field in the dielectric of thickness t_{ins} , then $F_{ins} = V_G/t_{ins}$. This requires the assumption that all the gate voltage is dropped across the dielectric (more detail of which is discussed in Appendix A).

The electric field across the semiconductor/dielectric interface is not conserved, but the displacement field is, therefore $\epsilon_{ins}F_{ins}(x = 0) = \epsilon_{SC}F_{SC}(x = 0)$ which means:

$$F_{SC_0} = \frac{\epsilon_{ins}V_G}{\epsilon_{SC}t_{ins}} \quad (153)$$

where ϵ_{ins} is the permittivity of the dielectric. Another way of writing this is:

$$F_{SC_0} = \frac{C_{ins}V_G}{\epsilon_{SC}} \quad (154)$$

where $C_{ins} = \epsilon_{ins}/t_{ins}$ and is the specific capacity of the dielectric (in units of F/m²). Using this Equation (152) becomes:

$$V_G = \sqrt{\frac{2q\epsilon_{SC}}{C_{ins}^2} T(\phi_0(V_G)) + (\phi'(t_{SC}))^2} \quad (155)$$

which can be rewritten as:

$$V_G = \sqrt{1 + \delta} \sqrt{\frac{2q\epsilon_{SC}}{C_{ins}^2} T(\phi_0(V_G))} \quad (156)$$

where δ is given by:

$$\delta = \frac{C_{ins}^2 (\phi'(t_{SC}))^2}{2q\epsilon_{SC}T(\phi_0(V_G))}. \quad (157)$$

Grünewald's 1980 paper ⁸⁵ goes into depth as to why the approximation $\delta \ll 1$ may be made, and using said approximation means Equation (156) can be simplified to:

$$V_G = \sqrt{\frac{2q\epsilon_{SC}}{C_{ins}^2}} \sqrt{T(\phi_0(V_G))}. \quad (158)$$

Starting again from Equation (155) the differential $dV_G/d\phi_0$ can be calculated as:

$$\frac{dV_G}{d\phi_0} = \frac{1}{2} \frac{\frac{2q\epsilon_{SC}}{C_{ins}^2} \frac{dT(\phi_0(V_G))}{d\phi_0}}{\sqrt{\frac{2q\epsilon_{SC}}{C_{ins}^2} T(\phi_0(V_G)) + (\phi'(t_{SC}))^2}} \quad (159)$$

which simplifies to:

$$\frac{dV_G}{d\phi_0} = \frac{\sqrt{\frac{q\epsilon_{SC}}{2C_{ins}^2}} n_0(V_G)}{\sqrt{1 + \delta} \sqrt{T(\phi_0(V_G))}} \quad (160)$$

where δ is the same as previously defined in Equation (157). Using the approximation that $\delta \ll 1$ it becomes:

$$\frac{dV_G}{d\phi_0} = \sqrt{\frac{q\epsilon_{SC}}{2C_{ins}^2}} \frac{n_0(V_G)}{\sqrt{T(\phi_0(V_G))}}. \quad (161)$$

By combining this differential with Equation (158) repeated below:

$$V_G = \sqrt{\frac{2q\epsilon_{SC}}{C_{ins}^2}} \sqrt{T(\phi_0(V_G))} \quad (162)$$

we can produce an equation for the differential of the gate voltage with respect to the interface potential without the function $T(\phi_0)$:

$$\frac{dV_G}{d\phi_0} = \frac{q\epsilon_{SC}}{C_{ins}^2} \frac{n_0(V_G)}{V_G}. \quad (163)$$

B.5 Combining Results

By combining Equations (141) and (150) we reach:

$$\frac{I_D(V_G)}{I_{off}} - 1 = \frac{1}{t_{sc}} \int_0^{\phi(0)} \frac{(e^{\beta\phi(V_G,x)} - 1)}{\sqrt{\frac{2q}{\epsilon_{sc}} T(\phi(x)) + (\phi'(t_{sc}))^2}} d\phi \quad (164)$$

and using the approximation that $\frac{2q}{\epsilon_{sc}} T(\phi(x)) \gg (\phi'(t_{sc}))^2$ it simplifies to:

$$\frac{I_D(V_G)}{I_{off}} - 1 = \frac{1}{t_{sc}} \sqrt{\frac{\epsilon_{sc}}{2q}} \int_0^{\phi(0)} \frac{(e^{\beta\phi(V_G,x)} - 1)}{\sqrt{T(\phi(x))}} d\phi. \quad (165)$$

Differentiating this with respect to the internal potential and resolving it at $x = 0$ gives:

$$\frac{1}{I_{off}} \frac{dI_D(V_G)}{d\phi_0(V_G)} = \sqrt{\frac{\epsilon_{sc}}{2qt_{sc}^2}} \frac{(e^{\beta\phi_0(V_G)} - 1)}{\sqrt{T(\phi_0(V_G))}} \quad (166)$$

where the differential of current with respect to surface potential can be split into two separate differentials:

$$\frac{dI_D(V_G)}{dV_G} \frac{dV_G}{d\phi_0(V_G)} = I_{off} \sqrt{\frac{\epsilon_{sc}}{2qt_{sc}^2}} \frac{(e^{\beta\phi_0(V_G)} - 1)}{\sqrt{T(\phi_0(V_G))}}. \quad (167)$$

Using Equation (160) it becomes:

$$\frac{dI_D(V_G)}{dV_G} \sqrt{\frac{q\epsilon_{sc}}{2C_{ins}^2}} \frac{n_0(V_G)}{\sqrt{T(\phi_0(V_G))}} = I_{off} \sqrt{\frac{\epsilon_{sc}}{2qt_{sc}^2}} \frac{(e^{\beta\phi_0(V_G)} - 1)}{\sqrt{T(\phi_0(V_G))}} \quad (168)$$

which rearranges to give:

$$n_0(\phi_0(V_G)) = \frac{I_{off} C_{ins}}{qt_{sc}} \left(\frac{dI_D(V_G)}{dV_G} \right)^{-1} (e^{\beta\phi_0(V_G)} - 1) \quad (169)$$

which is the relationship between the number of filled states required for the deconvolution of Equation (129).

Although Equation (169) provides a relationship between n_0 and ϕ_0 , it has a dependence on I_D and V_G still. To use Equation (169) we must first calculate ϕ_0 as a function of V_G . The first step is to replace n_0 in Equation (169) using Equation (163) to give:

$$\frac{C_{ins} t_{sc}}{I_{off} \epsilon_{sc}} V_G \frac{dI_D(V_G)}{dV_G} \frac{dV_G}{d\phi_0} = (e^{\beta\phi_0(V_G)} - 1) \quad (170)$$

and since the variables of V_G and ϕ_0 are separated each side may be separately integrated to remove one of the differentials:

$$\frac{C_{ins}t_{SC}}{I_{off}\epsilon_{SC}} \int_0^{V_G} V_G \frac{dI_D(V_G)}{dV_G} dV_G = \int_{\phi_0(0)}^{\phi_0(V_G)} (e^{\beta\phi_0(V_G)} - 1) d\phi_0. \quad (171)$$

Solving either side of Equation (171) gives:

$$\frac{C_{ins}t_{SC}}{I_{off}\epsilon_{SC}} \left[V_G I_D(V_G) - \int_0^{V_G} I_D(V_G) dV_G \right] = \frac{1}{\beta} [e^{\phi_0(V_G)\beta} - \beta\phi_0(V_G) - 1] \quad (172)$$

which is finally simplified to:

$$\frac{C_{ins}t_{SC}}{I_{off}\epsilon_{SC}k_B T} \left[V_G I_D(V_G) - \int_0^{V_G} I_D(V_G) dV_G \right] = e^{\phi_0(V_G)\beta} - \beta\phi_0(V_G) - 1. \quad (173)$$

The left hand side of Equation (173) consists completely of experimentally obtainable values. The right hand side can be numerically, but not analytically, solved for each individual value of ϕ_0 for each experimental gate voltage point.

B.6 Analysis Scheme

The three final equation used to go from experimental TFT data to a set of bandgap density of states are as follows:

$$\frac{C_{ins}t_{SC}}{I_{off}\epsilon_{SC}k_B T} \left[V_G I_D(V_G) - \int_0^{V_G} I_D(V_G) dV_G \right] = e^{\phi_0(V_G)\beta} - \beta\phi_0(V_G) - 1 \quad (174)$$

$$n_0(\phi_0(V_G)) = \frac{I_{off}C_{ins}}{qt_{SC}} \left(\frac{dI_D(V_G)}{dV_G} \right)^{-1} (e^{\beta\phi_0(V_G)} - 1) \quad (175)$$

$$n_0(\phi_0(V_G)) = \int_{-\infty}^{\infty} g_{BG}(E) [f(E - \phi_0(V_G)) - f(E)] dE. \quad (176)$$

To calculate the bandgap density of states, first a vector of points of surface potential must be calculated for each gate voltage ($\phi(V_G)$) point from Equation (174). The differential of the drain current with gate voltage and previously calculated $\phi(V_G)$ can then be evaluated within Equation (175) to give $n_0(\phi_0)$. This can then be deconvoluted using one of multiple techniques to give the actual density of states of the bandgap states.

Appendix C Simulation Settings

Table 7.1: Table of simulation settings used to produce **Figure 4.5**.

Variable	Value	Variable	Value
CB Form	Rectangle	Max Energy (eV)	4
CB Bandedge (eV)	0.4	Min Energy (eV)	-4
CB Band DOS (eV ⁻¹ cm ⁻³)	3×10 ²⁰	# Energy Points	16001
TS1 Form	Exponential	TFT Width (μm)	1000
TS1 max DOS (eV ⁻¹ cm ⁻³)	3×10 ²⁰	TFT Length (μm)	50
TS1 Peak Energy (eV)	0.4	Max Gate Voltage (V)	60
TS1 FWHM (eV)	0.05	# Gate Voltage Points	2401
TS2 Form	Exponential	TFT Capacitance (nF/cm ²)	34.4
TS2 max DOS (eV ⁻¹ cm ⁻³)	4×10 ¹⁹	Drain Voltage (V)	10
TS2 Peak Energy (eV)	0.4	# Charge Depth Points	1001
TS2 FWHM (eV)	0.1	Temperature (K)	300
TS3 Form	Gaussian	SC Thickness (nm)	100/10/1
TS3 max DOS (eV ⁻¹ cm ⁻³)	6×10 ¹⁸	SC Mobility (cm ² /Vs)	10
TS3 Peak Energy (eV)	0.2	SC Permittivity	8.9
TS3 FWHM (eV)	0.04	Off Current (A)	13×10 ⁻¹¹
Charge Depth Solution	All		

Appendix D List of Publications

- [1] Pichaya Pattanasattayavong, **Alexander D. Mottram**, Feng Yan, and Thomas D. Anthopoulos, "Study of the Hole Transport Processes in Solution-Processed Layers of the Wide Bandgap Semiconductor Copper(I) Thiocyanate (CuSCN)," *Advance Functional Materials*, vol. 25, no. 43, pp. 6802–6813, Nov. 2015.
- [2] **Alexander D. Mottram**, Yen-Hung Lin, Pichaya Pattanasattayavong, Kui Zhao, Aram Amassian, and Thomas D. Anthopoulos, "Quasi Two-Dimensional Dye-Sensitized In 2 O 3 Phototransistors for Ultrahigh Responsivity and Photosensitivity Photodetector Applications," *ACS Applied Materials and Interfaces*, vol. 8, no. 7, pp. 4894–4902, Feb. 2016.
- [3] Simon Hunter, **Alexander D. Mottram**, and Thomas D. Anthopoulos, "Temperature and composition-dependent density of states in organic small-molecule/polymer blend transistors," *Journal of Applied Physics*, vol. 120, no. 2, p. 25502, Jul. 2016.

D.1 List of Publications in Preparation

- [1] **Alexander D. Mottram**, Ivan Isakov, Gwen Wyatt-Moon, Yen-Hung Lin, Kornelius Tetzner, Hendrik Faber and Thomas D. Anthopoulos, "Comparison of High-K Dielectrics Using Facile Solution Processing Techniques"
- [2] Ivan Isakov, Hendrik Faber, **Alexander D. Mottram**, Satyajit Das, Max Grell, Anna Regoutz, Becky Kilmurray, Martyn McLachlan, David Payne and Thomas D. Anthopoulos, "Elucidating the mobility variation in low dimensional metal oxide semiconductor systems"

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Date: Nov 1, 2013
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Alexander D. Mottram, Yen-Hung Lin, Pichaya Pattanasattayavong, et al

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