A 0.016 mm$^2$ 12 b $\Delta \Sigma$ SAR With 14 fJ/conv. for Ultra Low Power Biosensor Arrays

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Abstract—The instrumentation systems for implantable brain-machine interfaces represent one of the most demanding applications for ultra low-power analogue-to-digital-converters (ADC) to date. To address this challenge, this paper proposes a $\Delta \Sigma$ SAR topology for very large sensor arrays that allows an exceptional reduction in silicon footprint by using a continuous time 0-2MASH topology. This configuration uses a specialized FIR window to decimate the $\Delta \Sigma$ modulator output and reject mismatch errors from the SAR quantizer, which mitigates the overhead from dynamic element matching techniques commonly used to achieve high precision. A fully differential prototype was fabricated using 0.18 μm CMOS to demonstrate 10.8 ENOB precision with a 0.016 mm$^2$ silicon footprint. Moreover, a 14 fJ/conv figure-of-merit can be achieved, while resolving signals with the maximum input amplitude of ±1.2 Vpp sampled at 200 kS/s. The ADC topology exhibits a number of promising characteristics for both high speed and ultra-low power systems due to the reduced complexity, switching noise, sampling load, and oversampling ratio, which are critical parameters for many sensor applications.

Index Terms—A/D conversion, bio-sensors arrays, oversampling, incremental delta-sigma, FIR decimation, low power analogue, ADC calibration.

I. INTRODUCTION

THE emergent market for wearable electronics and implantable devices for personalized health care has resulted in a growing demand for miniaturized battery powered systems that wirelessly connect a network of sensors [1]. These systems rely extensively on high precision analogue to digital conversion to leverage digital processing techniques and accommodate stringent diagnostic requirements [2]. As a result the ADC power, area, and precision can have a profound impact on a system’s overall capabilities. For this reason oversampling techniques using $\Delta \Sigma$ ADCs have already been used extensively to accommodate the niche characteristics of biomedical devices and acquire low frequency bio-signals [3].

More recent developments allow these techniques to be more applicable to large sensor arrays using an incremental analogue to digital converter (IADC) topology [4]. This is in contrast to the conventional use where a single oversampling ADC continuously converts the signal from a single sensing unit with exceptional efficiency. IADC designs are unique in the sense that they periodically reset the loop filter which enables a single ADC to process multiple analogue inputs with reduced latency. This periodic reset associates a particular conversion time for each result and enables pipelined [4], two-step [5], or multi-step operation [6]. The resulting modulator can exhibit reduced mismatch sensitivity and require a smaller oversampling ratio while achieving equivalent performance to that of higher order modulators [7]. This is crucial for larger sensor arrays because reduced circuit complexity leads to more compact designs and faster signal conversion. These earlier publications realize an IADC structure that explicitly transfers the quantization residue from one quantizer to the next using a sample and hold mechanism which is not necessarily required. For instance the zoom technique used in [8] reuses the capacitive DAC during conversion thereby reducing complexity and power consumption. The resulting system achieves exceptional precision by combining a SAR with a second order switched capacitor (SC) $\Delta \Sigma$ modulator. A common problem however is that the SAR INL/DNL errors are not shaped by the loop filter and end up limiting the overall precision unless dynamic element matching techniques (DEM) are used. This can lead to exhaustive digital overhead for DEM control and necessitate additional redundancy in the capacitive digital to analogue converter (DAC) to remove the SAR nonlinearity [9].

The system proposed by this paper is illustrated in Fig. 1 which uses a SAR and CT-$\Delta \Sigma$ together to convert the signal from four analogue inputs. This configuration is then tiled 16 times in parallel to record from 64 channels simultaneously for neural recording applications. The topology is introduced as a $\Delta \Sigma$SAR because it emerged from introducing higher order CT-$\Delta \Sigma$ type noise shaping to the SAR by processing the residue charge left after the SAR conversion. Using SC techniques with a similar motivation also lead to the noise shaping SAR (NSSAR) topology from [10] which has been used extensively to achieve very high resolution SARs [11] and optimum precision.
and higher order modulators with reduced active filter structures [12]. In fact the fully-passive NSSAR technique can increase the SAR precision by several bits while immune to PVT variation [13]. The distinction here is that the NSSAR will shape the quantization noise over multiple samples by introducing 1 to 3 extra cycles per sample where as the \( \Delta \Sigma \) SAR will allow one-shot conversions but introduce considerably more cycles corresponding to the oversampling ratio of the modulator. The later is characteristic of IADC operation. Additionally the CT approach leads to an inherent reduction in size because the loop filter is not subject to extra sources of sampling noise typical in CS circuits. The IADC 0-2 multi-stage noise shaping (MASH) quantization scheme used by the \( \Delta \Sigma \) SAR can be interpreted as first resolving the sampled input using a conventional SAR and then applying a \( \Delta \Sigma \) feedback loop to resolve the remaining quantization residue left on the capacitor array equivalent to the zoom technique. The resulting bit stream from the comparator output consists of both SAR and oversampled quantization results. The advantage this topology presents is that it can be configured without the need for DEM or analogue dithering techniques because SAR INL/DNL errors can instead be cancelled by calibrating the FIR filter that processes this bit stream in the digital domain. This minimises capacitive switching during signal conversion and reduces overall complexity. Moreover by virtue of resolving a small SAR residue, the CT loop filter can maximize its noise efficiency without much concern for distortion or modulator nonlinearity.

This paper presents an analytic design method for evaluating which condition allows the zoom type IADCs to exhibit high performance and which two-step configuration will lead to the best efficiency or size. Preliminary efforts to realize the system in Fig. 1 are presented in [14] and the circuits proposed here are improved to achieve better power efficiency as part of a larger reconfigurable neural recording system [15]. This system uses an array of miniaturised ADCs that distributes the digital processing over many parallel segments leading to lower clock frequencies and better efficiency opposed to demanding a single high frequency ADC and digital core. To present the design characteristics of the \( \Delta \Sigma \) SAR, this paper is organized as follows. Section II introduces the principle design relations of this ADC structure with regard to system efficiency and size. This is followed by the proposed mismatch compensation method in Section III. The circuit level implementation is proposed in Section IV with design considerations for the loop filter, capacitive DAC and FIR filter. Finally measured results are presented in Section V which are used to draw conclusions in Section VI.

II. \( \Delta \Sigma \) SAR Architecture

The \( \Delta \Sigma \) SAR topology closely resembles the SAR with an additional loop filter that can switch between amplifying \( A(s) \) and integrating \( H(s) \) behaviour following the last SAR conversion. This similarity is shown in Fig. 2 which represents a single ended equivalent of the fully differential implementation described here. The input signal is sampled on the bottom plate of the capacitive array such that conventional SAR feedback can be applied while the loop filter is initially providing wideband amplification of 10x. Once the first \( N \) bits are resolved the comparator output is connected directly to a unit element in the capacitive array for the \( \Delta \Sigma \) quantization phase. Simultaneously the loop filter is switched to introduce second order noise shaping and resolves another \( M \) bits using DC extra oversampling cycles. In theory this will result in \( M + N \) bits of precision but in practice the SAR conversion will need to evaluate \( N + 1 \) bits with 1 bit of redundancy. This redundancy implies that the residue will always be half of the modulator input range to prevent overloading the \( \Delta \Sigma \) ADC [16]. If 1 cycle is used for sampling the ADC will need to be clocked at \( (N + DC + 2f_{imp}) \) for a sampling frequency \( f_{imp} \) with a modulator bandwidth \( f_{bw} \) at half this clock frequency. A typical conversion is illustrated by the timing diagram in Fig. 3 which shows the FSM using 1 cycle for sampling, \( N + 1 \) cycles for SAR, and DC cycles for \( \Delta \Sigma \) modulation. Meanwhile the comparator results will infer if the corresponding FIR coefficient provided by a shared controller is added or subtracted from a local accumulator thereby resolving the input signal. To provide insight to the design considerations we will first discuss the noise requirements needed for achieving a \( N + M \) ADC precision. This will reveal the dominant power requirements due to the filter and capacitive DAC and also give some indication about the size of each capacitor in Fig. 2 which can then be used to estimate area. Note however that the defining characteristic of this quantization process is that the SAR residue is bound to a well defined voltage range of \( \pm V_R/2^N+1 \) where \( V_R \) is the ADC reference voltage. The reduced input range implies that feedback may not be needed to linearise the Gm-C loop filter used during \( \Delta \Sigma \) conversion but it also indicates the filter coefficients have to be carefully adjusted to achieve second order noise shaping.
A. Topology Optimization

The efficient operation of low speed ADCs primarily relies on the careful consideration of various noise sources to avoid dissipating excess power. However the two modes of operation have characteristically different requirements. Concisely stated the ΔΣ modulator will focus on achieving a specific noise floor because out of band noise is removed after decimation while the SAR operation is sensitive to integrated noise over the entire circuit bandwidth. To illustrate the design relations quantitatively the following discussion will reiterate on several expressions from well established ΔΣ theory [17]. This will allow us to determine system constraints particularly with respect to the analogue filter that provides second order noise shaping and in this case consumes most of the power.

1) Filter Noise Constraints: First recall that the oversampling ratio for a second order modulator is dictated by Eq. 1 in terms of resolving $M$ bits. This will later be used in association with the expression in Eq. 2 to evaluate acceptable quantization noise power $S_n^2$ for a $N+M$ precision ADC.

$$DC \geq \frac{\sqrt{2\pi^4}}{15 \cdot 2^{-2(M+1)}} \quad (1)$$

$$S_n^2 = \frac{1}{12} \left( \frac{VR}{2^{N+M+1}} \right)^2 \quad (2)$$

Now in order to capture the subjective performance of the circuit level implementation and its impact, this analysis uses the Noise Efficiency Factor (NEF). The expression for NEF in Eq. 3 normalizes the input referred noise $e_{in}^2$ of a particular implementation to that of a bipolar transistor with a biasing current equivalent to that used by the filter $I_{filt}$. As a result we can abstractly consider noise-power relations without considering a specific filter topology that will exhibit some particular NEF.

$$NEF^2 \equiv \frac{2I_{filt}e_{in}^2}{\pi UT 4kT f_{bw}} \quad (3)$$

In fact by combining this with the ADC noise requirement in Eq. 2, $I_{filt}$ can be predicted as a function of circuit topology and its equivalent NEF. This is detailed in Eq. 4 under the condition that $e_{in}^2 = S_n^2$ where the relevant circuit noise bandwidth is reduced $f_{bw}/DC$ due to oversampling.

$$I_{filt} = \pi UT 24kT \left( \frac{f_{bw}}{DC} \right) \left( \frac{2^{N+M+1} \cdot NEF^2}{VR} \right)^2 \quad (4)$$

Similarly $I_{filt}$ can be evaluated for just the SAR operation as a special case: $I_{SAR} \equiv I_{filt}(DC = 1, M = 0)$. In the case that $I_{SAR}$ is larger than the estimate in Eq. 4 we should adopt that value instead. This result is mainly relevant for SAR converters where an analogue amplifier is used to precede the comparator and thereby dominating the noise requirements [18]. Here it will also be used to indicate the preliminary performance with respect to $N & M$ with a fixed clock speed and the associated conversion time of $N + DC + 2$ cycles. The resulting conversion efficiency is proportional to $2^{N+M} / P_A (N + DC + 2)$ as conversion per Watt where total analogue power is estimated as $P_A \approx VR I_{filt}$. In this case the filter supply voltage is simply equal to the reference voltage. Normalization allows the relative efficiency to be visualized in Fig. 4 which provides some evidence that the filter alone tends to be more efficient as $M$ becomes larger than $N$. However $N$ can not be arbitrarily small if the residue need to be kept in the linear range of the modulator. This implies a direct relationship between the ADC reference voltage and the minimum SAR resolution. The details of this requirement is strongly dependent on the full ADC precision and its sensitivity towards transistor nonlinearity. However as a priori the minimum SAR resolution $N$ can be approximated by considering that the linear input range for sub-threshold differential input pair is related to the thermal voltage $\pm UT$ [19] which suggests that $N \geq \log_2(V_R/UT)$ to keep the residue inside the linear range.

2) Estimating System Power: The previous result is relatively optimistic in the sense that it does not consider the decimation filter or DAC power dissipation. To warrant an accurate estimation of the ADC’s efficiency and resource requirements the Digital $P_D$, and capacitive switching $P_C$ losses should also be estimated.

$$P_C = C_U f_{sam} V_R^2 \left( \frac{DC}{2} + \sum_{i=1}^{N} (2^i - 1)2^{N-2i-2} \right) \quad (5)$$

Eq. 5 includes the SAR energy dissipation in terms of the capacitive switching using the analysis from [20]. The $V_{cm}$ based switching method employed here retains a stable common mode $V_{DAC}$ with good conversion efficiency. This will help to preserve the linearity of the modulator. Variation in common mode voltage changes the offset of the loop filter as well as the impact of top plate parasitics [20]. Both will introduce nonlinearity that is convoluted by the SAR quantization process and can be challenging to compensate accurately. $P_C$ is evaluated for $N+1$ SAR cycles where the unit capacitor $C_U$ size introduces some degree of freedom. Strictly the total capacitance is bounded such that the $kT/C$ noise is smaller than noise requirement of Eq. 2. For instance we could let the sampling noise contribute half the allowable noise power which leads to a minimum capacitance according to Eq. 6 give a $2^{N+1}$ unit binary DAC.

$$C_U = \frac{12kT}{V_R^2} 2^{N+2M+1} \quad (6)$$

Fig. 4. Power efficiency as $2^{N+M}/P_A (N + DC + 2)$ in terms of conversions per Watt where $N+M$ is the target precision of the analogue filter for different values of $N & M$ normalised by the best case where $M = 8 & N = 1$. [Graph]
This unit element should be noticeably larger than what may be expected from SAR configurations due to the small number of elements in the capacitor array resulting in reduced matching and interconnect complexity. Generally such a configuration will favour high density vertical metal-insulator-metal (MIM) capacitors that have large minimum size requirements and can be placed over active circuitry to reduce silicon footprint. In fact by using a split capacitor configuration the size of \( C_U \) can be even larger with less elements in the array for the same sampling capacitance leading to very efficient utilization of MIM capacitor area [21]. It may still be the case that \( C_U \) is smaller than the minimum capacitance \( C_{min} \) for intermediate precision of 6-10 bits. In such a case this model will simply adopt \( C_{min} \). This will also apply to the load capacitance \( C_{L1} \) when it is calculated with respect to the modulator bandwidth as \( f_{bw} = gm_1/CL_1 \). However this should carefully consider the reduced input swing of \( VR_{filt} \) which means the transconductance for a conventional fully-differential input in sub-threshold operation would be \( gm_1 = VR_{filt}/(\eta \mu_f 2^N) \) where \( \eta \) is the transistor slope factor.

In order to estimate the digital losses this model extrapolates the energy dissipation per clock cycle extracted from a 1 bit accumulator taken as \( E_{reg} \). The associated register depth \( R_D = N + M + \log_2(DC) \) bits is derived by considering the accumulated rounding errors from DC additions during FIR decimation. This leads to Eq. 7 which is expected to be insignificant at higher resolutions because decimation filter has reduced requirements when compared to the full precision of the integrator.

\[
P_D = R_D E_{reg} f_{smpl} (DC + N + 2) \text{ Cycles/Sample} \tag{7}
\]

3) FOM Dependence: The above relations should provide a good indication for the power requirements even though some system components such as the comparator and auxiliary circuits have been ignored. The Walden FOM \( W \) and Schreier FOM \( S \) are presented in Eq. 8 & 9. These performance metrics are plotted in Fig. 5 by assuming typical values from the 0.18 \( \mu m \) CMOS process. \( VR \) is adjusted to 0.6/1.2/2.4 V which keeps the linear input range of the \( \Delta \Sigma \) modulator consistent while resolving different SAR resolutions for fair comparison. Other constants are assumed as follows; \( \eta = 1.2, \ NEF = 1.4, E_{reg} = 1 \Omega, C_{min} = 100 \Omega, f_{smpl} = 10^5 \) Hz, \( f_{bw} = 10^5 (N + DC + 2)/2 \) Hz. The general trend presented here is that the topology operates at maximal performance when the most of the power is dissipated by the oversampling loop and the lowest energy per conversion is dissipated when the capacitive switching and modulator power become comparable. It is not surprising that reducing the supply voltage makes it more difficult to achieve a good FOM because the absolute noise performance becomes more difficult to achieve. For reference a conventional \( \Delta \Sigma \) modulator [22] is designed with the same target specifications and using the same analysis method to configure the OPAMP integrators and resistive input network. Such a configuration achieves 167 dB FOM\( S \) irrespective of target resolution when we consider just the filter power dissipation. In fact this figure is commonly achieved by state of the art [8]. This highlights how the \( \Delta \Sigma \SAR \) configuration can theoretically achieve more than 2X better performance for resolutions above 12 bits even when operating at lower supply voltages.

\[
FOM_W = \frac{P_C + P_D + P_A}{f_{smpl} 2^{N+M}} \tag{8}
\]

\[
FOM_S = 6.02 (N + M) + 10 \log_{10} \left( \frac{f_{smpl}/2}{P_C + P_D + P_A} \right) \tag{9}
\]

\[
EA = \left( 2 CL_1 + CU \right) 2^{N+2} / C_{dens} \tag{10}
\]

The required area for this configuration is estimated by Eq. 10 which uses the MIM capacitor density \( C_{dens} \) of 2fF/\( \mu \)m\(^2\). As shown in Fig. 6 high resolution configurations will tend towards noise limited requirements that are closely related to the integration and sampling capacitors. Lower resolutions are largely dependent on technology and how the SAR DAC is configured to address mismatch. Fig. 7 shows the impact of \( M \) on overall ADC efficiency in combination with the area requirement. This is characterised using the density of performance \( DOP = FOM_S - 10\log_{10}(EA) \) which peaks for an ENOB of 11.4 bits with \( M \) being 5.8 bits. The overall quantitative results show exceptional figures of merit with highly compact configurations for 10-16 bit designs from first principles. The design described above only focuses on achieving an optimal noise performance because it dominates the low frequency FOM metrics. Naturally a number of extra considerations need to be made for achieving the desired ENOB. Finding the requirements for open loop gain, parasitics, nonlinearity, and digital filtering is done by using numerical optimization on simplified models guided by analytic results from prior work [22], [24]. However we can observe some agreement with this simplified model and the performance achieved in other works.

III. FOREGROUND CALIBRATION FOR THE \( \Delta \Sigma \SAR \)

The foregoing analysis suggests that the resources dedicated to SAR operation should be kept small in order to achieve the peak performance of the oversampling modulator. As a result the DAC linearity may be much worse than the
target precision. Ideally before instrumentation the system should perform a calibration procedure that determines the actual capacitor weights $W_{DAC}$ and recovers any lost accuracy due to mismatch in the digital domain [25], [26]. Digital calibration techniques are extensively used for SAR converters because they enable more aggressive capacitor sizing without introducing extra analogue complexity that does not benefit from technology scaling [27]. A simplified model of the quantization process is shown in Fig. 8 where the SAR result is fed back according to the 7 capacitor weights $W_{DAC}$ to produce a residue that is oversampled by the modulator and decimated by the FIR filter. The mismatch errors arise when the coefficients $W_{SAR}$ do not correctly calculate the exact charge offset by the capacitors (i.e. $W_{DAC} \neq W_{SAR}$). The structural advantage here is that all mismatch induced errors are accurately evaluated by the oversampling loop which can operate with extra noise shaping during calibration without needing a more precise reference ADC. First note that the DNL errors due to DAC mismatch are only observed upon changes in the SAR codes. Secondly the single bit $\Delta \Sigma$ modulator can present significantly better linearity without calibration if SAR codes remain unchanged. Moreover if the weights are correctly estimated we should expect no discontinuities in the DNL characteristic for slowly varying inputs. The proposed calibration method takes advantage of these observations by correlating the first order difference of the ADC output and the SAR codes to find the correct coefficients for $W_{SAR}$. In addition by using a triangular test signal to perform calibration this procedure does not need full precision multipliers. This is because the triangular waveform distributes the occurrences of each SAR code evenly when at least one sample is taken per SAR code. Therefore the number of toggles on each SAR bit is exactly distributed as powers of two. Now if each SAR coefficient is adjusted when the respective SAR bit toggles then the rate of adjustment for each capacitor weight will be uniform if the adjustments are proportionally scaled by powers of two.

$$W_{SAR}[n + 1] = W_{SAR}[n] + \alpha \cdot sign(Q_{out}[n]) \cdot Q_{SAR}[n]$$ \tag{11}

Eq. 11 introduces the proposed method for iteratively updating $W_{SAR}$ for the $n$th sample using $\alpha$ as fixed adjustment factor. $Q_{out}$ is the first order difference of the quantized output which is a function of the SAR $Q_{SAR}$ and modulator $Q_{\Delta \Sigma}$ outputs. The exact relation is expressed in Eq. 12. No multiplication is required here because whether a SAR bit has toggled is strictly Boolean and represented by $Q_{SAR}[n]$. This leads to a ternary result with respect to the adjustment rule for incrementing or decrementing the estimated weights that can be implemented using 7 up/down counters of varying depth. In this case the MSB counter has a logical depth of 16 bits while the LSB uses 22 bits.

$$Q_{out}[n] = Q_{SAR}[n] \cdot W_{SAR}[n] + 2^{-N} Q_{\Delta \Sigma} \cdot W_{FIR}$$ \tag{12}

If we presume our $\Delta \Sigma$ converter has ideal performance then $2^{-N} Q_{\Delta \Sigma} \cdot W_{FIR} = V_{IN}[n] - W_{DAC}[n]$ which leads to $Q_{out}$ as:

$$Q_{out}[n] = V_{IN}[n] + W_{SAR}[n] - W_{DAC}[n]$$ \tag{13}

Eq. 13 reveals that during calibration the output will consist of two components. The first is due to the input as the ramp’s rate of change $V_{IN}$ that is either increasing or decreasing. The second term results from an incorrect weight estimate on whichever SAR bit changed. In fact depending on the sign of this error we know if the estimated weight needs to be larger or smaller. In essence Eq. 11 uniformly averages over all DNL errors to approach the correct weights.

IV. CIRCUIT IMPLEMENTATION

Using the foregoing results, the presented implementation targets a 12 bit resolution using $N = 6$ & $M = 6$ which should
lie just on the inflection point of estimated area requirement curve. In particular we will present the configuration for a fully differential sensor array using analogue and digital supplies at 1.2 V and a commercially available 6-Metal 0.18 μm CMOS technology (AMS/IBM C18A6/7SF).

A. Loop Filter

The loop filter topology used here is a second order feed forward architecture that is used extensively in CT modulators due to its reduced complexity and low distortion [28], [29]. This particular structure reduces the number of summation nodes and digital feedback elements to minimise power consumption. The signal and noise transfer functions due the loop filter \( H(s) = 2^N \left( s^2 + 2 \omega_{bw} s + \omega_{bw}^2 \right) \) and the feedback factor \( f \approx 2^{-N} \) are summarised in Eq. 14 & 15 where \( \omega_{bw} \) is the filter bandwidth in radians. The feedback \( f \) is determined by evaluating the capacitive coupling from \( C_{\Delta \Sigma} \) onto \( V_{DAC} \). Since \( f \) is quite small there is an apparent gain in the STF but not in the NTF. This gain is provided by increasing the bandwidth of the first stage by \( 2^N \) which substantially diminishes the input referred noise from the second integrator and comparator. Then using the requirements from Sec. II-A.1 will allow the capacitors to be specified for this implementation as \( f_{\text{mp}} (N + DC + 2)/2 = 4 VR I_{R1}/(\eta UT^2 \mu C_L1) = 2 VR I_{R2}/(\eta UT C_{L2}) \).

\[
NTF(s) = \frac{s^2}{s^2 + 2 \omega_{bw} s + \omega_{bw}^2} \quad (14)
\]

\[
STF(s) = 2^N \frac{2 \omega_{bw} s + \omega_{bw}^2}{s^2 + 2 \omega_{bw} s + \omega_{bw}^2} \quad (15)
\]

The transistor level implementation is shown in Fig. 9 where the switches \( S_{\Delta \Sigma} \) allow the filter to change its operation. The first stage uses a fully differential complementary or inverter-based transconductor that can tolerate small variations in input common mode fluctuation by ±100 mV and this specific configuration exhibits an \( NEF \approx 1.6 \). The sizing of this complementary pair requires some attention regarding the capacitive loading on \( V_{DAC} \) due to the gate to drain capacitance of the transistors. In fact \( C_u \) needs to be considerably larger than this parasitic such that the open loop gain of the first integrator is not reduced and thereby diminishing filter performance. The circuit is segmented into three sections; two analogue integrators and one summation stage. The first integrator will switch between resistive and capacitive loads. This stage will have the most demanding bandwidth requirement when providing pre-amplification during SAR quantization. Both integration capacitors are reset outside of the \( \Delta \Sigma \) phase and the last two stages should achieve -40 dB HDs for a ±100 mV input signal which is derived from simulations [24]. The common mode feedback on the two integrators uses linear mode devices that reference \( V_{DD}/2 \). These transistors can be quite large and introduce considerable parasitics because of the large current dissipated in the first stage. To avoid a reduction in bandwidth, a sub-set of these gates are connected to the loading capacitor \( C_{L1} \) that is switched out during SAR conversion which retains the steady state common mode voltage. The 1-bit quantization is realized using a dynamic latch where offset associated concerns should follow conventional wisdom for accurate SAR conversion. The diode connected load in the summing stage places the input common mode of the comparator close to \( V_{DD} \). This improves both the bandwidth and noise performance of the latch [30].

B. Capacitive DAC

A 7-bit fully differential binary weighted capacitive DAC is used to perform the SAR quantization. The single ended structure is shown in Fig. 10. The voltage scaling on the last conversion cycle reduces the number of capacitors needed and takes advantage of the reduced reference sensitivity for the last SAR conversion. Because calibration is performed with respect to \( C_{\Delta \Sigma} \) that references \( V_R \) the mismatch in the last SAR coefficient will also accommodate the mismatch in voltage reference. The array is realized by precision top metal-on-metal capacitor devices which utilize M5-M6. A M4 \( V_{CM} \) shield is introduced to isolate this array from active analogue and digital circuitry placed below. While bottom plate sampling diminishes the effect of parasitics on \( V_{DAC} \), the split capacitor needs tuning according to the extracted parasitics on the LSB section particularly with respect to the shielding layer. The unit capacitor is 71 fF with \( 6 \times 6 \mu m^2 \) dimensions yielding 0.2% deviation of capacitor mismatch for a 3σ confidence interval. This should allow a precision of 9 ENOB without calibration [31] and will utilise all the top metal area needed for the sub-blocks placed below.

During sampling each input will be loaded by a total of 768 fF for an equivalent 52 μVrms sampling noise. This should indicate that the upper bound of maximum signal to
noise and distortion ratio (SNDR) for this DAC is 78 dB. Also note that the INL characteristic of the SAR and comparator noise will inevitably lead to additional sources of quantization error which implies the $\Delta \Sigma$ input range will correspondingly increase from its expected value. Moreover resolving a sampled input with a $\Delta \Sigma$ modulator can lead to increased distortion due to idle tones. This is why the modulator should be designed such that signals that are $-3$ dB of the maximum $\Delta \Sigma$ input range can still be adequately resolved. Fortunately comparing single bit modulators reveals second order feed-forward structures are substantially more capable of processing signals close to the full range input due to improved stability dynamics [16]. This means the DAC mismatch requirements are less stringent and will not need a sub-binary weighting or additional calibration capacitors to minimize the sources of excess residue. The simpler binary weighted structure will allow good baseline matching for the unit capacitors with the minimum number of elements in the DAC. Moreover introducing the split capacitor in addition to the $V_{cm}$ switching method dramatically reduces the total switching energy to the extent that it is dominated by the oversampling phase. Particularly when multiple data converters are operated in parallel the excessive capacitive switching raises a concern for high frequency supply noise of the reference voltage that is outside the LDO bandwidth. The anti-aliasing provided by the loop filter will partly reject this component as a result of opting for a CT implementation. The $\Delta \Sigma$ feedback will dissipate at most 77 fC every cycle which needs to be partly absorbed by decoupling capacitors local to the ADC. High density MOS capacitors are therefore introduced to load the reference voltage by 20 pF per ADC. The reduced switching noise should represent a clear advantage over switched capacitor modulators. An improvement over the conventional SAR may only be expected when calibration overhead is unavoidable because the sampling noise constraint makes energy dissipation in SAR switching mostly indifferent to its resolution.

C. FIR Filtering

Decimation of the $\Delta \Sigma$ bit stream of incremental topologies finds the application of FIR filters particularly suitable. This is in part because resetting the integrators for each sample and discards residual components from the previous conversion and the corresponding group delay requirement can limit the IIR filter design. Moreover sharing FIR filter coefficients with multiple ADCs reduces the hardware requirements to a shared lookup table with individual accumulators for each modulator. Using an $OSR$ of 24 implies $N + DC + 1 = 31$ additions are needed per sample where a second order CIC filter would need at least $N + 2DC + 3 = 57$ additions per sample for a full evaluation and four times the number of registers [32]. From Sec. II-A we know that the register depth $R_D$ should be 16 bits while the FIR coefficient precision needs to be 8 bits. The application of a symmetric FIR window also assists with a number of circuit considerations for rejecting noisy aggressors near $f_{bw}$ [8]. Supply noise is a typical culprit but it may be less obvious that the FIR also reduces the sensitivity due to the second integrator’s offset when the quantization mode switched. Hanning or raised cosine FIR windows are known to provide exceptional aliasing particularly when applied to sample limited $\Delta \Sigma$ decimation [33]. Using a general family of raised cosine windows [34] a configuration is proposed here that matches the noise shaping of the loop filter order ($L$) with that of the FIR side-lobe roll-off by defining its coefficients as:

$$FIR[n] = \cos^K\left(\frac{\pi n}{OSR + 1} - \frac{\pi}{2}\right)$$  \hspace{1cm} (16)

The factor $K$ in Eq. 16 determines the spectral characteristics of the filter similar to that of the Kaiser windows. The rapid side-lobe roll-off is related to $K$ as $30K$ dB/Dec with the first zero location at $\pi (1 + K/2) f_{smp}$. Because the quantization noise is shaped in relation to $L$ at $20L$ dB/Dec [5], $K$ can be defined as $K = 2/L$. This leads to a near uniform quantization noise profile with a reduced transition band from better pole placement. The $K$-factor dependent frequency characteristics are shown in Fig. 11 for an $OSR = 16$ applied to the output of a second order modulator. Note that when $K = 2$ the FIR is equivalent to that of a Hanning window. The overall system transfer function $S_{sys}(z)$ can be analysed in the z-domain using a bilinear transform of the loop filter $H(s)$ and convolving it with that of the FIR response. To see how well decimation is achieved we compare the decimation performance to that of an ideal filter.

$$S_Q^2 = \frac{2\pi L}{3(2L+1)(OSR)^{2L+1}}$$  \hspace{1cm} (17)

Eq. 17 introduces the expected in-band quantization noise power $S_Q^2$ from analytic relations [35] which assume an ideal brick-wall filter with a cut off frequency at $f_{smp}/2$ that is not
Fig. 12. Quantization noise suppression based on numerical simulations and Eq. 17 and the respective precision loss for varying OSR.

Fig. 13. Microphotograph of the 64 channel neural recording system showing two 32 channel macros used in parallel with integrated power management and digital processing.

limited in any way. Similarly integrating over the resulting power densities in $\text{Sys}(z)$ will indicate the expected quantization noise from the proposed configuration. Comparing these two results will indicate how effectively the quantization noise is rejected by the FIR filter. The noise excess is shown in Fig. 12 as a function of OSR and filter order. This shows that using the proposed window results in loss smaller than 0.5 bits. Also notice that we do not pay special attention to how the $\Delta \Sigma$ quantization noise folds onto the signal band. After the signal is convolved by the SAR quantization process the residue no longer shares the same structure as the input signal and therefore better in band decimation performance will not lead to better in band SNR.

V. MEASURED RESULTS

A chip micrograph is shown in Fig. 13 depicting the 64 channel instrumentation system with die size of 6.2 mm$^2$. This configuration uses two macros each of which integrates eight ADCs together with the DSP in a tiled fashion to post-process the recordings from 32 instrumentation amplifiers. In fact the architecture may be scaled to accommodate more channels by virtue of the pipelined architecture that distributes the processing capacity. The measured results presented here are taken from an isolated test structure that allows detailed characterization without overhead from the whole system. The physical implementation of the $\Delta \Sigma$SAR sub-block is shown in Fig. 14 which is $96\mu m \times 164\mu m$ in size. Because the DSP is assisted by a specialized execution unit that also performs neural signal decomposition only the digital accumulator is included in this figure. The active components inside the modulator contribute to a small portion to the overall system. Instead the most demanding layout consideration is with regard to the switches driving the capacitive DAC. Even though the capacitance is not too large, the switch resistance in $\Delta \Sigma$ mode can introduce a pole leading to excess loop delay that could result in performance degradation [36].

Initial ADC characterization used a low-frequency 180 Hz tone at half to the full input range where the comparator bit stream was directly acquired off-chip for post-processing. This allowed the proposed calibration mechanism to be compared with more robust methods. In fact when using more elaborate numerical optimization methods to adjust $W_{\text{SAR}}$ the THD only showed 2 dB improvement although convergence is typically much faster. Both testing and calibration waveforms were generated off-chip using an Agilent 33120a with additional bandpass filtering. The measured INL characteristics
LEENE AND CONSTANTINOU: 0.016 mm² 12 b ΔΣ SAR WITH 14 fJ/conv. FOR ULTRA LOW POWER BIOSENSOR ARRAYS

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Fig. 16. Convergence of DNL rms and peak to peak values during calibration subject to a 90 Hz triangular waveform.

Fig. 17. Measured ADC performance showing the spectral characteristics of a) SAR residue at the output of the ΔΣ and b) the full precision output which has a SNDR of 66.8 dB. This recording was taken using a 2.35 Vpp 95 kHz input tone sampled at 200 kHz.

are shown in Fig. 15. The calibration method decreases the SAR nonlinearity by a factor of 10. As shown in Fig. 16 the main drawback of this method is that in order to reject noisy perturbations the α rate must be small amounting to slow convergence on the order of 10⁶ quantization cycles or around 10 seconds. The DAC used for generating the ramp signal will need to be more accurate than the ADC precision to allow correct calibration. On the other hand instead of using a more powerful centralized DSP unit to perform tuning, this system allows all channels to calibrate simultaneously resulting in a speed up for multichannel systems that can share a single high resolution DAC. The discontinuities visible in this trend result from the fitting method used to calculate DNL as a function of time which is not very consistent.

Fig. 17 shows the spectral characteristics of the ADC after the capacitor weights have been estimated with 16 bit precision together with the SAR residue that can be obtained by only taking the decimated modulator output. This illustrates that SAR residue has its spectral power distributed over the entire bandwidth at multiple tones. This wideband quantization ‘noise’ will in effect present dithering on modulator’s nonlinearity before appearing at the output. Fig. 18 shows the signal resolved by the modulator as a function of time. Interestingly the polarity in residue will directly correspond to the polarity of the sampled input signal because swapping the reference voltage on the capacitive DAC will imply a successive approximation while maintaining correspondingly positive or negative residues. Then by performing a Fourier transform on the measured modulator output for each conversion separately we can evaluate the noise shaping characteristic of the loop filter. This result is shown in Fig. 19 which follows closely to the expected second order noise shaping.

In Table I the performance is summarized and state-of-the-art noise shaping ADC structures are compared. This work achieves exceptional compactness for the 12 bit target resolution particularly in relation to the conversion efficiency [37]. The measured power dissipation is about 5 μW which simulations indicate 40% is dissipated in the loop filter and 23% in capacitive switching. Note that power dissipation from the look up table is not included in this figure. Fig. 20 presents the measured SNDR and $FOM_W$ for varying oversampling ratios. During calibration the OSR was doubled to gain 3 dB in precision while the typical operation uses an OSR of 24. The total conversion uses an additional 11 cycles for SAR and sampling phases to give the resulting 200 kS/s speed for a 7 MHz system clock. We also show the measured SNDR for varying input frequencies in Fig. 21. This shows that maximum
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### TABLE I

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>[18]</th>
<th>[23]</th>
<th>[7]</th>
<th>[13]</th>
<th>[38]</th>
<th>[39]</th>
<th>[40]</th>
<th>[41]</th>
<th>This Work</th>
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<tr>
<td>Tech.</td>
<td>[nm]</td>
<td>180</td>
<td>65</td>
<td>180</td>
<td>65</td>
<td>110</td>
<td>65</td>
<td>180</td>
<td>180</td>
<td>180</td>
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<tr>
<td>Topology</td>
<td></td>
<td>SAR</td>
<td>NSSAR</td>
<td>IADC</td>
<td>NSSAR</td>
<td>SAR</td>
<td>SAR</td>
<td>IADC</td>
<td>NSSAR</td>
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<tr>
<td>Supply-V</td>
<td>[V]</td>
<td>1</td>
<td>0.8</td>
<td>1.8</td>
<td>0.8</td>
<td>0.9</td>
<td>0.4</td>
<td>1.8</td>
<td>1.2</td>
<td>1.2</td>
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<tr>
<td>Supply-I</td>
<td>[$\mu$A]</td>
<td>25</td>
<td>1.7</td>
<td>19</td>
<td>151</td>
<td>27</td>
<td>1.8</td>
<td>16.4</td>
<td>13.1</td>
<td>23</td>
</tr>
<tr>
<td>Speed</td>
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<td>100k</td>
<td>32k</td>
<td>8k</td>
<td>6.25M</td>
<td>1M</td>
<td>1k</td>
<td>313k</td>
<td>4k</td>
<td>2k</td>
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<tr>
<td>ENOB</td>
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<td>12.4</td>
<td>12.3</td>
<td>9.35</td>
<td>11.0</td>
<td>7.81</td>
<td>9.3</td>
<td>15.7</td>
<td>16.1</td>
</tr>
<tr>
<td>SNDR</td>
<td>[dB]</td>
<td>65</td>
<td>76</td>
<td>57</td>
<td>58</td>
<td>67</td>
<td>49</td>
<td>57</td>
<td>96</td>
<td>76</td>
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<tr>
<td>Area</td>
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<td>0.18</td>
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<td>0.012</td>
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<td>0.013</td>
<td>0.002</td>
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<td>0.5</td>
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<td>FOMW</td>
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<td>165</td>
<td>8</td>
<td>862</td>
<td>14.8</td>
<td>11.7</td>
<td>3.19</td>
<td>151</td>
<td>73.8</td>
<td>320</td>
</tr>
<tr>
<td>FOMS</td>
<td>[dB]</td>
<td>156</td>
<td>177</td>
<td>159</td>
<td>163</td>
<td>170</td>
<td>137</td>
<td>154</td>
<td>180</td>
<td>175</td>
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</tbody>
</table>

![Fig. 21. Measured SNDR dependency for varying input frequency for a 2.35 Vpp input tone.](image)

precision is maintained for signals below 20 kHz but also shows some degradation at frequencies near the maximum input bandwidth. The main experimental difficulty resulting from the proposed configuration is that the filter characteristics are closely tied to the reference voltage in a practical setting. On occasion it is useful to give additional voltage overhead for aggressive digital and analogue systems to accommodate process voltage and temperature variance. However in this case the biasing circuit will need extra tuning parameters to keep the modulator’s linearity consistent while adjusting the reference voltage. Multi channel systems can generally accommodate complex tuning for all ADCs to eliminate wafer/process level variations without substantial overhead since this functionality is already needed by instrumentation circuits to perform precise filtering. The power management block in Fig. 13 provides 12 bit digital trimming on the ADC reference voltages and bias currents such that most of the offset can be accommodated although this is performed externally on the test structure.

### VI. CONCLUSION

A novel 12-bit analogue-to-digital data converter has been proposed that uses SAR & $\Sigma\Delta$ quantization schemes to realize a compact and ultra low power data converter for a 64 channel neural sensor system. Using an efficient Gm-C filter, compact 7 bit binary DAC, and optimized FIR decimation this work aims to eliminate the circuit complexity from DEM and increase power efficiency which is highly desirable for biomedical sensors. A prototype fabricated in 0.18 $\mu$m CMOS demonstrates 10.8 ENOB precision at the nyquist frequency with a state-of-the-art 0.016 mm$^2$ silicon footprint and is capable of resolving full scale signals at 200 kS/s. The proposed techniques are appropriate for a variety of sampling frequencies making this configuration applicable to numerous other applications that require aggressive ADC miniaturization. In addition a calibration technique suitable for large sensor arrays is presented that takes advantage of the two step quantization scheme to calibrate multiple ADCs simultaneously.

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### REFERENCES


