A Charge-Based Ultra-Low Power Continuous-Time ADC for Data Driven Neural Spike Processing

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***Abstract*—The paper presents a novel topology of a continuous-time analogue-to-digital converter (CT-ADC) featuring ultra-low static power consumption, activity-dependent dynamic consumption, and a compact footprint. This is achieved by utilising a novel charge-packet based threshold generation method, that alleviates the requirement for a conventional feedback DAC. The circuit has a static power consumption of 3.75 μW, with dynamic energy of 1.39 pJ/conversion level. This type of converter is thus particularly well-suited for biosignals that are generally sparse in nature. The circuit has been optimised for neural spike recording by capturing a 3 kHz bandwidth with 8-bit resolution. For a typical extracellular neural recording the average power consumption is in the order of $\sim$4 μW. The circuit has been implemented in a commercially available 0.35 μm CMOS technology with core occupying a footprint of 0.12 mm^2.**

I. Introduction

Never before has there been such a drive to develop innovative neurotechnologies for studying the human brain. The current trend is to aggressively scale the number of recording channels towards 10s to 100s of thousands. With this ambition there also lies significant challenge as the development of more complex implantable technologies is constrained by a limit for dissipated heat of the order of 80 mW/cm^2 [1]. As virtually all neural implants require the input analogue signals to be digitised prior to any processing (e.g. spike sorting) or communication, there is need for a highly energy-efficient analogue-to-digital-conversion (ADC).

Since neural signals typically exhibit long "quiet" periods followed by sporadic spike activity it is usually very inefficient to use uniform sampling. Conventional systems typically address this by using a threshold comparison to detect the presence of a spike and then transmit only the spike snippets [2]. A promising alternative, Continuous Time (CT) sampling, records the time when the signal crosses into the next quantisation level [3] adapting its momentary sampling rate to the instantaneous spectral content of the signal, similarly to [4], reducing the amount of taken samples during the quiet periods leading to a reduction of used energy. Moreover, since the taken samples are exactly at the edge of a quantisation level the quantisation error is reduced by approximately 10-20 dB [3]. Furthermore, there has recently been interest in implementation of entirely clock-less spike-sorting [5] paving a way to activity-dependent neural implants entirely relying on CT sampling techniques.

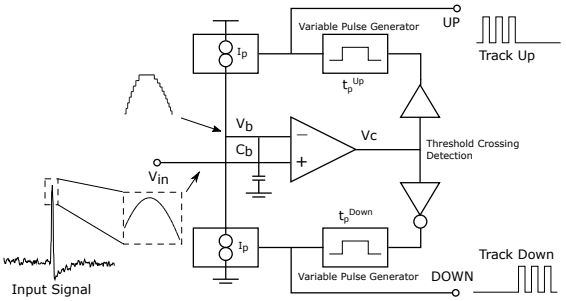

Fig. 1. System concept for the proposed charge-based CT-ADC.

This leads to an interest in a recently emerging class of ADC circuits called Continuous-Time Analogue-to-Digital-Converters (CT-ADC) sometimes also referred to as event-based or level-crossing ADCs [3]. Over recent years several different implementations have been presented most commonly using a set of two comparators comparing the input signal to the two closest quantisation levels [6]–[9]. A significant challenge of this approach is however precise generation of the quantisation threshold potentials used as a reference. One approach is to use a complete N-bit DAC [6], [9] to generate the potential of the last sample and subtract it from the input signal giving rise to an error signal in the range of one Least Significant Bit (LSB) which is then compared to a fixed reference. An alternative approach is injecting an offset to the input signal using a capacitor bank and comparing the signal to a fixed reference [7], [8].

As an alternative we present here a novel topology of a CT-ADC (shown in Fig.1) that operates on the principle of balancing a comparator input voltage V_{in} by its quantised version V_b recreated by applying charging and discharging charge packets to a capacitance C_b of the comparator's inverting input. Unlike previous topologies, the proposed method in theory only requires a single differential amplifier acting both as a comparator as well as an input amplifier leading to the possibility of achieving ultra-low power consumption and efficient area utilisation.

This paper is organised as follows: Section II presents the principle of operation; Section III provides a theoretical analysis; Section IV describes our implementation; Section V presents measured results; and Section VI concludes this work, comparing it to the state-of-the-art.

II. Principle of Operation

The underlying concept of the proposed topology is illustrated in Fig. 1. This consists of a comparator acting both as an input amplifier and a device calculating the error between the last taken sample and the input. The comparator output is then passed through a threshold crossing detector implementing quantisation levels V_{tH} and V_{tL}. Their difference ΔV_t is chosen such that a sufficient hysteresis is achieved thus preventing excessive switching in the presence of noise.

Using a cascade of inverter-based amplifiers the signal is then amplified to a logic level indicating when one of the thresholds has been crossed and the error of the input exceeds one LSB at which time a new sample has to be taken. When this occurs a pulse generator is triggered leading to a generation of a pulse of length t_p acting as an output of the system in addition to controlling a current source of current I_p adding or removing a charge packet $Q_b = I_p t_p$ from capacitance C_b of the inverting input of the comparator. If I_p and t_p are chosen such that $|Q_b| = C_b \times V_{LSB}$ where V_{LSB} is the voltage representing one LSB the potential V_b is now going to be equal to the new sample different by one LSB from the previous one. On start-up or when the potential at C_b is significantly different from the input signal a train of pulses is generated synchronising the system with the input.

III. System Analysis

The key design parameters are the required pulse length t_p, current I_p and comparator specifications. Rather than being limited by the input bandwidth the proposed ADC is limited by the maximal input slope it can follow. Assuming we are designing a comparator limited to a bandwidth B having an input of maximum input peak-to-peak voltage V_{pp} the worst case input signal would be a sinewave $s(t)$ of frequency B and amplitude $V_{pp}/2$ having a maximal slope of:

$$\frac{ds}{dt}|_{max} = V_{pp}\pi B \tag{1}$$

Assuming the tracker has a resolution of N bits and each pulse is followed by a minimal idle time of t_d the maximal slope the converter can follow is:

$$\frac{\Delta V_b}{\Delta t} = \frac{V_{LSB}}{t_d + t_p} = \frac{V_{pp}}{2^N \times (t_d + t_p)} \tag{2}$$

Comparing Eqns. (1) and (2) gives rise to a first design condition:

$$t_p + t_d < \frac{1}{\pi \times B \times 2^N} \tag{3}$$

Once a suitable value of t_p is chosen the required pulse current I_p is then calculated as $I_p = V_{LSB} C_b / t_p$

A. Comparator Requirements

When the quantised voltage V_b changes, the resulting step has to propagate through the comparator faster than a new pulse can be triggered. This takes: $T = t_p + t_d < 1/(V_{pp}\pi B)$. Assuming that the comparator output settles within three time constants of the amplifier $\tau = 1/2\pi B_{comp}$ where B_{comp} is the comparator's open-loop bandwidth we can then obtain an expression for the minimal B_{comp}:

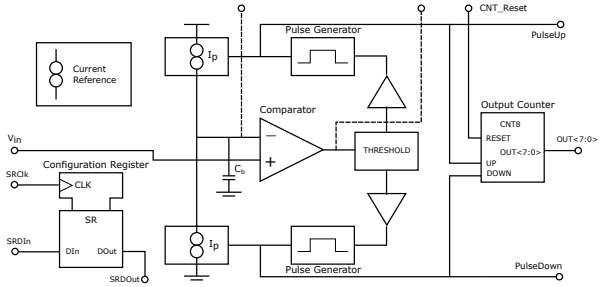

Fig. 2. Simplified circuit schematic for the proposed charge-based CT-ADC.

$$B_{comp} > 3 \times B \times 2^{N-1} \tag{4}$$

Furthermore, there is a relationship between the comparator's gain A_{comp} and the threshold difference ΔV_t. If we denote the input referred hysteresis V_{hys} this expression can than be given as:

$$\Delta V_t = A_{comp} \times (V_{LSB} + V_{hys}) \tag{5}$$

This shows that a smaller LSB can be achieved either by increasing A_{comp} or decreasing any of ΔV_t or V_{hys} followed by updating t_p or I_p.

IV. Circuit Implementation

The circuit has been implemented in a 0.35 μm CMOS technology provided by AMS (H35B4S1 process). Key challenges include: ensuring that the charge packets added and removed from capacitance C_b when a quantisation step up and down respectively is applied are equal; (2) ensuring that the input comparator has a sufficient bandwidth greater than the minimum found in Eq. (4) while making sure that the power consumption is kept to a minimum.

Since it is challenging to precisely match a current source onto a current sink, the charging and discharging charge packet Q_{up} and Q_{down} can be externally tuned to match by using different configurable pulses of lengths t_p^{up} and t_p^{down}.

The target specification has been set to an 8-bit, 3 kHz ADC, operating from a 1.5 V supply. The proposed system shown in Fig. 2 implements the basic topology and adds a shift register holding the configuration of all circuits, a counter providing an 8-bit output and an on-chip current reference. The balancing capacitor C_p was chosen to be C_p = 3 pF as a compromise between distortion due to unwanted charge injection, occupied area and power consumption.

A. Comparator

This is based on a simple single stage fully-balanced Operational Transconductance Amplifier (OTA) biased at a current of 1.25 μA generating a gain of 39.94 dB and open-loop bandwidth of 917.3 kHz which is close to worst-case theoretical requirement of 1.15 MHz. As the comparator is operated in an open-loop configuration, the achieved gain is expected to depend on temperature and process variations

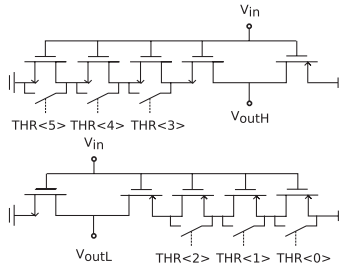

Fig. 3. Configurable threshold crossing detector circuit. All devices are minimum size (W/L = 0.4/0.35).

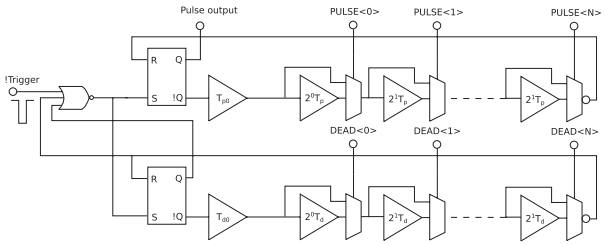

Fig. 4. Programmable pulse generator with 8-bit pulse and 2-bit idle time resolution.

resulting in an LSB size change. This can be rectified using calibration during signal reconstruction.

B. Threshold Crossing Detector

To add flexibility to the circuit we have decided to use a configurable threshold crossing detector composed of two inverters with electronically programmable length as shown in Fig. 3. This gives rise to three different settings of both thresholds V_{tH} and V_{tL}.

C. Comparator Buffer

After adding the threshold crossing detector it was found that the open loop bandwidth of the comparator is greatly compromised due to relatively large input capacitance of the inverters amplified by the Miller effect. To address this issue we have included a voltage follower composed of single stage OTA biased by a current of 0.5 μA between the threshold detector and the comparator.

D. Pulse Generator

This consists of a monostable circuit formed by an SR latch followed by a configurable delay line. To add a controllable idle (dead) time t_d a second monostable circuit is used inhibiting the main pulse generator as seen in Fig. 4.

The pulse length t_p has a basic length of $T_0 \approx 42.7$ ns which can be extended by changing the 8-bit `PULSE` register by additional ≈ 0.5 – 58 ns. To ensure that there are no large gaps between achievable delays due to process variations the bits of `PULSE` have weightings which are a power of 1.7 rather than a power of 2. This possibly leads to a non-monotonic characteristic of t_p with respect to the setting of `PULSE`. Similarly the inhibitor circuit has a basic setting of $T_0 \approx$ 163 ns onto which an additional delay of 163 ns and 316 ns can be added by altering the setting of a 2-bit `DEAD` register.

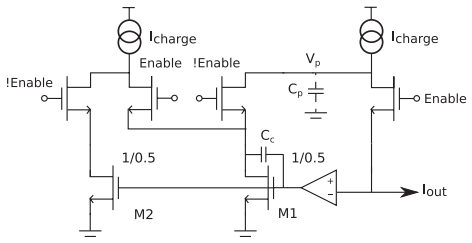

Fig. 5. Schematic of the used charge injection circuit. All devices have W/L = 0.8/0.35 unless shown otherwise.

E. Charge Injection Circuit

It is generally quite challenging to inject a precise amount of charge to the balancing capacitor C_b due to extra charge injected from the used current switch. The circuit shown in Fig. 5 addresses this issue by applying negative feedback to bootstrap node V_p so the parasitic capacitance C_p of the switch at the same potential as the balancing voltage V_b. A dual current source is used to ensure there is uninterrupted current flow through transistor `M1` of Fig. 5 leading to its stable drain-source voltage. The circuit is replicated with opposite polarities to create a discharging circuit.

F. Current Reference

The design uses an internal self-biasing current reference of 50 nA described by H. Oguey and D. Aebischer [10] to provide bias current to all amplifiers and pulse current I_p. I_p is configurable in the region of 4 – 32 nA in steps of 4 nA and is fed to the switch using Wilson current mirrors for increased output resistance.

V. Measured Results

The proposed circuit was implemented using full-custom layout in a commercially available 0.35 μm CMOS technology with circuit core occupying an area of $\approx 320\,\mu\text{m} \times 360\,\mu\text{m}$ seen in Fig. 6.

With no input applied the static consumption is $\approx$3.75 μW from a 1.5 V supply. The circuit was configured for I_p = 16 nA, the maximal ΔV_t and the shortest possible t_p. A sinewave of a 450 mV DC bias and a peak-to-peak voltage of 250 mV was then applied to the input and frequency varied from 45 Hz to 6 kHz. The output signal was reconstructed using zero-order hold and automatic mismatch calibration employed in the reconstruction algorithm with power consumption and SNDR plotted in Fig. 7. The demonstrated activity dependent power consumption and an increase in SNDR for fast varying inputs shows the circuit's particular suitability for conversion of neural spikes.

To find the output power spectral density (PSD) and noise performance a 1 kHz sinusoidal signal was applied to the input and the configuration left unchanged leading to the output passing through 212 quantisation levels (7.73 bits). The resulting PSD plotted in Fig. 8 demonstrates an SNDR of 51.50 dB and ENOB of 8.26 bits.

A sample amplified neural signal of a 450 mV offset and a peak-to-peak voltage of 250 mV was then applied to the input

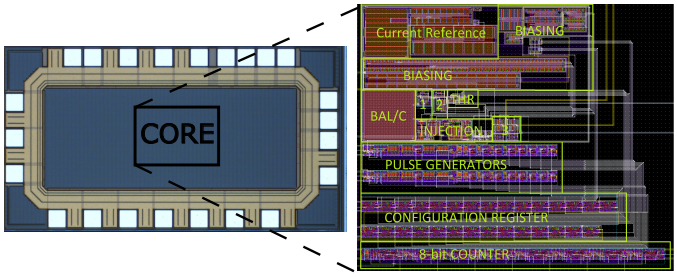

Fig. 6. A microphotograph of the fabricated circuit and a close-up of annotated layout exported from Cadence. 1 - Input Comparator, 2 - Unity Gain Buffer, 3 - Debugging Circuits

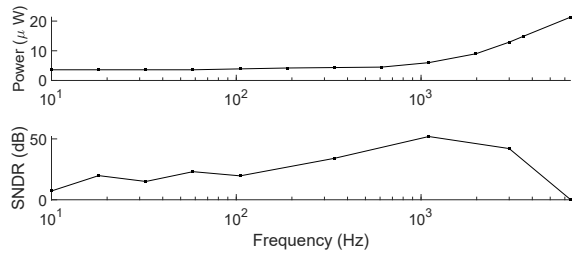

Fig. 7. Power consumption and SNDR obtained after converting a sinusoidal input.

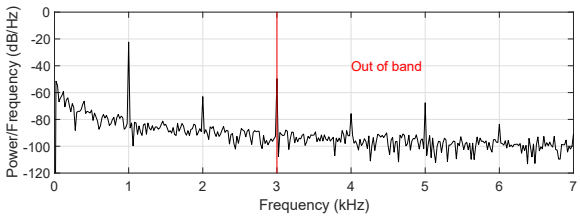

Fig. 8. Power spectral density of reconstructed output for a 250 mV, 1 kHz sine input. SNDR = 51.50 dB, ENOB = 8.26 bits

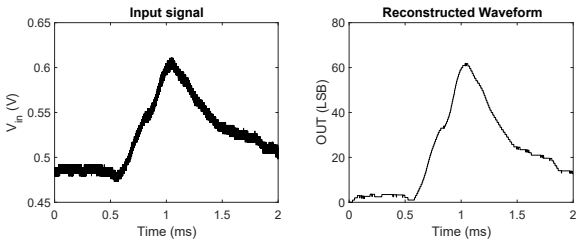

Fig. 9. An example of a neural spike reconstructed using zero-order hold and automatic mismatch removal.

and the output was reconstructed using the same procedure. The output waveform seen in Fig. 9 shows a sample neural spike crossing 62 quantisation levels (5.95 bits) giving rise to SNDR of 41.67 dB calculated as $SNDR = P(in)/P(in - out)$. The average power consumption in this case rose to ≈4.2 μW.

VI. Conclusion

A novel topology of a CT-ADC has been introduced and a proof-of-concept implementation described and validated by manufacturing and testing a full-custom integrated circuit. Selected work representing the state-of-the-art is compared in Table I with the Figure of Merit (FOM) calculated as $P/(2^N \times BW)$ where P, N and BW are the power consumption, resolution and bandwidth respectively.

It can be seen that the designed circuit is comparable with alternative CT-ADCs despite a higher absolute reported power consumption. It should be noted that the measured power consumption is inflated by ≈1.5 μW due to use of debugging voltage followers that would not be used in a final design. It is fully expected the power consumption will scale with supply voltage and process technology and as such the presented system represents the best energy efficiency of such a circuit implemented in a 0.35 μm process. This circuit validates the proposed topology with more improvements in terms of power consumption reduction possible in the future such as by employing a more advanced amplifier topology.

TABLE I
Summary of current CT sampling implementations

	[6]	[9]	[7]	[8]	This work
N (bits)	8	5	8	8	8
BW (kHz)	20	≥ 0.35	5	0.11-10.5	3
Tech (μm)	0.13	0.13	0.18	0.09	0.35
Area (mm^2)	1.69	0.357	0.045	N/A	0.115
Supply (V)	0.8	0.3	0.8	0.5 & 0.7	1.5
Power (μW)	3-9	0.22	0.31-0.58	0.54-0.73	≈ 3.75-12.9
FOM (pJ)	0.59-1.76	19.64	0.24-0.46	0.20-25.85	4.9-16.8

Acknowledgment

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