A 6-bit, Two-step, Successive Approximation Logarithmic ADC for Biomedical Applications

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***Abstract*— This paper presents the design and realization of a novel low-power 6-bit successive approximation logarithmic ADC for biomedical applications. A two-step successive approximation method is proposed to obtain a piecewise-linear approximation of the desired logarithmic transfer function. The proposed ADC has been designed and simulated using process parameters from a standard 0.35 µm 2P4M CMOS technology with a single 1.8 V power supply voltage. Simulation results show that, at a sampling rate of 25 kS/s, the proposed ADC consumes 4.36 µW to 14.6 µW (proportional to input amplitudes). The proposed ADC achieves 18.6 pJ/conversion-step, maximum INL of 0.45 LSB, an ENOB of 4.97-bits, and SNDR of 31.7 dB with 1 V full-scale input range.**

Keywords—logarithmic ADC; successive approximation ADC; biomedical applications; analog-to-digital converter; two-step ADC; non-linear ADC

I. INTRODUCTION

For several biomedical applications, such as cochlear implants [1], hearing aids [2], neural recording and stimulation [3-6], a nonlinear analog-to-digital converter (ADC) can offer key advantages to a signal processing system in contrast to a linear ADC. Benefits of a nonlinear ADC include the ability to handle large input signal dynamic range [1-5], reduction of noise and data bit-rate [6] and compensation of nonlinear sensor characteristics [7]. Specifically, a logarithmic ADC (LogADC) performs analog-to-digital conversions with non-uniform quantization. In a logADC, small analog input amplitudes are quantized with fine resolution, while large analog input amplitudes are quantized with coarse resolution.

A logADC can be realized either by using a nonlinear device with a linear ADC [1] or by performing the required signal operations in the logarithmic domain with conventional ADC architectures such as pipeline [3-5], cyclic [7], or lookup table [8]. This paper describes the design and realization of a logADC using the successive approximation register (SAR) architecture, which owns advantages in terms of low power consumption, low complexity and suitability for CMOS implementation. The desired logarithmic relationship is realized by using a piecewise-linear approximation and the ADC circuit is implemented by using a two-step successive approximation structure. This paper is organized as follows: Section II presents the characteristics of the logarithmic ADC; Section III describes the structure and circuit implementation of the proposed logarithmic SAR ADC; Post-layout simulation results and conclusion are given in Section IV and V, respectively.

II. LOGARITHMIC ADC

An N-bit logarithmic ADC converts an analog input voltage (V_{in}) to an N-bit digital output code (D_{out}) according to a logarithmic mapping described by (1), where N is the number of bits, b is the base of the logarithmic function, C is defined as the code efficiency factor [2], and V_{FS} is the full-scale analog input voltage range. In contrast to an N-bit linear ADC which has a constant LSB (least significant bit) size of $V_{FS}/2^N$, the LSB size of an N-bit logarithmic ADC varies with the input amplitudes. For small input amplitudes, the LSB size is small and has the minimum value of (2) when D_{out} changes from 0 to 1. For large input amplitudes, the LSB size is larger and has the maximum value of (3) when D_{out} changes from 2^N-2 to 2^N-1. Note that the logarithm of the LSB size is constant for a logarithmic ADC. The dynamic range (DR) of an ADC is defined by the ratio of the maximum input amplitude to the minimum resolvable input amplitude. Thus, in theory, the DR in decibels of an N-bit linear ADC is equal to $20\log_{10}(2^N)$, while the DR of an N-bit logarithmic ADC is given by (4).

$$D_{out} = \frac{2^N}{C} \cdot log_b \left(\frac{V_{in}}{V_{FS}} \cdot b^C\right) \quad (1)$$

$$LSB_{min} = V_{FS} \cdot b^{-C} \cdot \left(b^{C/2^N} - 1\right) \quad (2)$$

$$LSB_{max} = V_{FS}\left(1 - b^{-C/2^N}\right) \quad (3)$$

$$DR = 20\, log_{10} \left(\frac{V_{FS}}{LSB_{min}}\right) = 20\, log_{10} \left(\frac{b^C}{b^{C/2^N}-1}\right) \quad (4)$$

The ADC's logarithmic mapping relationship in (1) can be adjusted by the values of C and b. Fig. 1 shows examples of characteristics of an ideal 3-bit logarithmic ADC with V_{FS}=1 V and assorted values of C and b, while the threshold voltage levels, LSB_{min} and DR are summarized in Table 1. It can be deduced that larger values of C and b will result in a more non-linear logarithmic mapping, which emphasizes on the conversion of small input amplitudes and yields a larger DR. Note that Fig. 1 and Table. I also includes the characteristics of a 3-bit ADC for comparison. It is shown that, with identical N-bits, the logarithmic ADC can achieve a much larger DR than the linear counterpart.

III. PROPOSED LOGARITHMIC SAR ADC

This research work presents the design and implementation of a 6-bit SAR logADC. A straightforward method to realize a

TABLE I THRESHOLD VOLTAGE LEVELS, LSB_{MIN} AND DR OF 3-BIT LOGARITHMIC ADC WITH ASSORTED VALUES OF *b* AND *C*

$V_{in,th}$ (V)	b=10,C=2	b=10,C=3	b=10,C=4	b=2,C=7	b=2,C=8	b=2,C=9	Linear ADC
$V_{in,th}@D_{out}=7$	0.562341325	0.421696503	0.316227766	0.545253866	0.5	0.458502022	0.875
$V_{in,th}@D_{out}=6$	0.316227766	0.177827941	0.1	0.297301779	0.25	0.210224104	0.75
$V_{in,th}@D_{out}=5$	0.177827941	0.074989421	0.031622777	0.162104944	0.125	0.096388177	0.625
$V_{in,th}@D_{out}=4$	0.1	0.031622777	0.01	0.088388348	0.0625	0.044194174	0.5
$V_{in,th}@D_{out}=3$	0.056234133	0.013335214	0.003162278	0.048194088	0.03125	0.020263118	0.375
$V_{in,th}@D_{out}=2$	0.031622777	0.005623413	0.001	0.026278013	0.015625	0.009290681	0.25
$V_{in,th}@D_{out}=1$	0.017782794	0.002371374	0.000316228	0.014328188	0.0078125	0.004259796	0.125
$V_{in,th}@D_{out}=0$	0.01	0.001	0.0001	0.0078125	0.00390625	0.001953125	0
LSB_{min} (mV)	7.783	1.371	0.216	6.516	3.906	2.307	0.125
DR (dB)	42.18	57.26	73.30	43.72	48.16	52.74	18.06

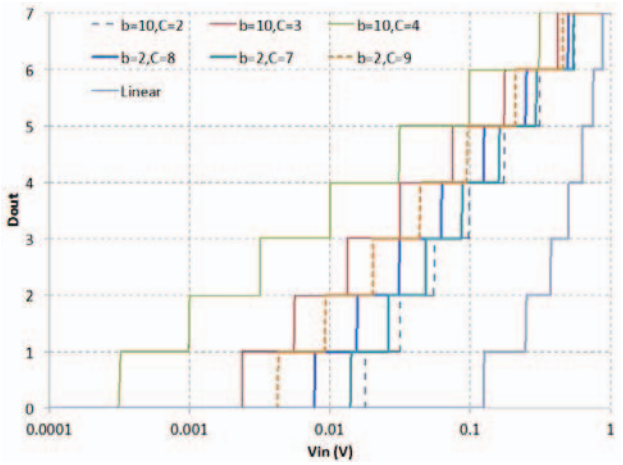

Fig. 1 Characteristic of an ideal 3-bit logADC with assorted values of *b* and *C*

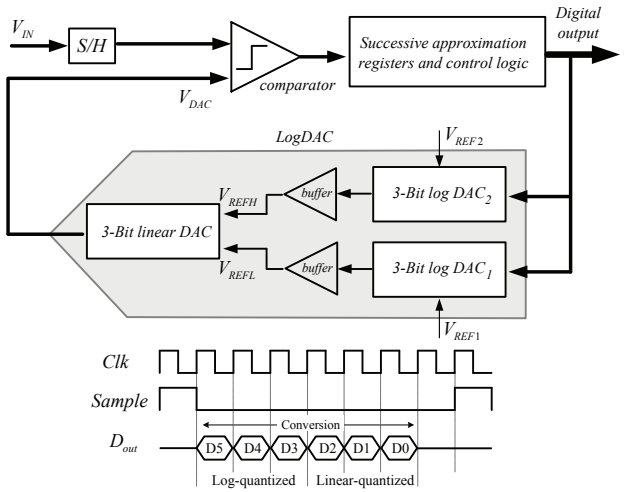

Fig. 2 Simplified block and timing diagram of the proposed SAR logADC.

SAR logADC is to employ the conventional linear SAR ADC structure and substitute the linear charge-redistribution digital-to-analog converter (DAC) with a logarithmic counterpart, as shown in Fig. 2.

The operation of the SAR logADC is identical to its linear counterpart. The comparator compares the analog input voltage with the threshold voltage levels from the logarithmic DAC (logDAC) to resolve the digital output successively from the MSB (most significant bit) to the LSB. In this work, we chose to design the logADC with *b=2* and *C=8* because the threshold voltage values (see Table 1) are in form of powers of 2, which allows an easy and practical realization of the logarithmic charge-redistribution DAC. However, using (2), the 6-bit logADC with *b=2* and *C=8* will have LSB_{min} = 0.354 mV (i.e. equivalent to LSB of an 11.5-bit linear ADC) which is very difficult to achieve practically due to noise, linearity and matching constraints.

To alleviate this practical difficulty, a two-step charge-redistribution DAC is proposed. The first conversion step performs a 3-bit logarithmic coarse conversion and the second step performs a 3-bit linear fine conversion. This is equivalent to a piecewise linear approximation of the logarithmic function, as depicted in Fig. 3. The first conversion step employs two 3-bit logDACs to perform a coarse conversion and determine the segment of the piecewise linear approximation. The analog output voltages of the logarithmic DACs will be used as the high and low reference voltages (V_{REFH} and V_{REFL}) for the linear DAC. This can be obtained by setting $V_{REF2}=2V_{REF1}$, where V_{REF1} and V_{REF2} are the reference voltages of the $logDAC_1$ and $logDAC_2$, respectively. Thus, given the same digital input code, the analog output voltage of $logDAC_2$ is twice that of $logDAC_1$ (i.e. $V_{REFH} = 2V_{REFL}$).

A. Logarithmic DAC and linear DAC

The logDACs and linear DAC are realized by using the conventional passive charge-redistributed capacitor arrays, as depicted in Fig. 4(a). Note that the choice of *b=2* and *C=8* allows an easy and practical implementation of the logDACs' capacitor arrays since all capacitance values are in the form of an integer multiple of a unit-size capacitance (C_{unit}). The total capacitance for each logDAC is $128C_{unit}$ thus LSB_{min} is equal to $(1/128)V_{REF1}$. Considering the thermal noise (kT/C) and matching accuracy, C_{unit} of the logDACs and linear DAC are set to 50 fF and 800 fF, respectively. Thus, the total capacitance used in the logDACs and linear DAC are 12.8 pF and 6.4 pF, respectively. To minimize the effects of charge injection, the bottom-plate sampling is employed and all switches are realized by CMOS transmission gates. Fig. 4(b) shows the layout floorplan of the capacitor arrays, which employs symmetrical common-centroid and dummy layout techniques, to minimize errors from mismatches, parasitics and process variation.

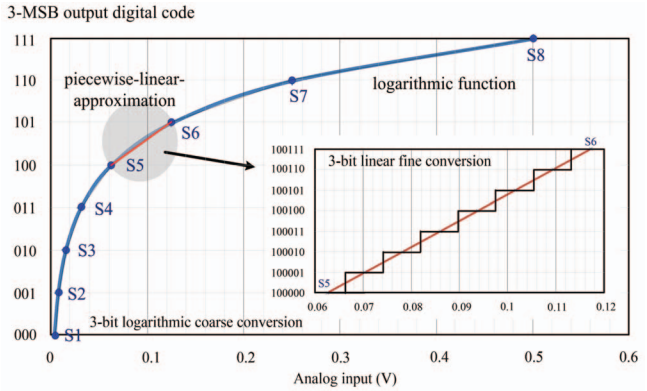

Fig. 3 Piecewise-linear approximation of the proposed 6-bit SAR logADC

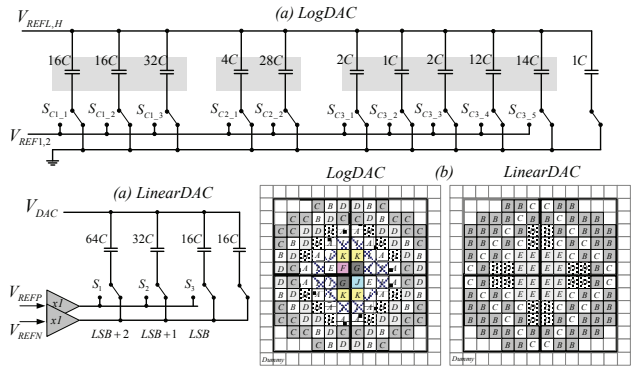

Fig. 4 (a) The conventional passive charge-redistributed capacitor arrays of logDAC and linearDAC (b) common-centroid and symmetrical layout

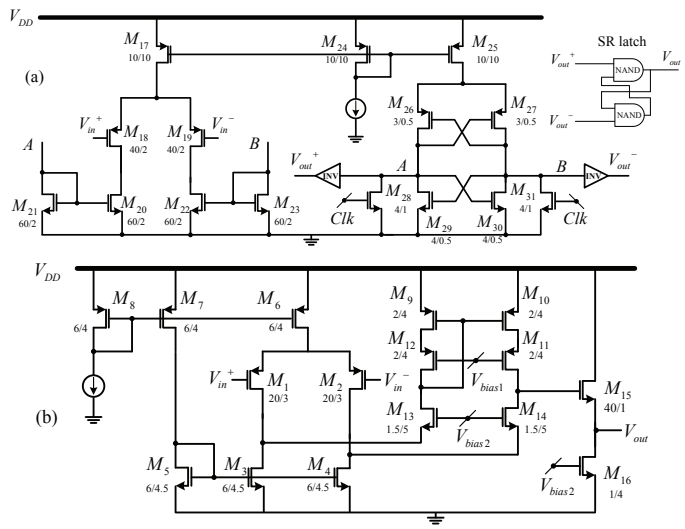

Fig. 5 Schematic diagram (a) comparator (b) unity-gain voltage buffer

B. *Comparator and voltage buffer*

The proposed 6-bit logADC has the minimum LSB size of 488.28 µV, which is equivalent to the LSB of a 11-bit linear ADC. The input offset voltages of the comparator and buffer should be smaller than 0.5 LSB. Fig. 5(a) shows the circuit schematic of the comparator, which is based on the two-stage latch topology in [9]. Fig. 5(b) shows the circuit schematic of the two-stage folded-cascode operational amplifier that is used as the voltage buffer.

C. *Sucessive approximation register and control logic*

The SAR and control logic are realized based on the circuit in [10]. Eight clock cycles are used for each conversion. The control logic is required to control switches S_{cN} and S_N of the logDAC and the linear DAC, as shown in Fig. 4, to produce logarithmic characteristic.

IV. Post-Layout Simulation Results

The proposed SAR logADC was designed and simulated with process parameters from a standard 0.35 µm CMOS technology under 1.8 V single power supply voltage. The overall ADC occupies a total area of 0.164 mm^2 (400 µm x 410 µm), as shown in Fig 6. Layouts of the capacitor arrays were carefully drawn and common-centroid, dummy, and symmetrical techniques were used to minimize the effects of device mismatch and process variation. The hold capacitance of the sample-and-hold circuit is 7.8 pF. The ADC's full-scale input range is set to 1 V. The reference voltages of $logDAC_1$ and $logDAC_2$ were set to 0.5 V and 1 V, respectively. The sampling frequency is 25 kHz. All results presented in this section are obtained from post-layout simulations including extracted parasitics. The dynamic power consumption of the ADC is dependent on the input signal amplitudes and varies from 4.36 µW to 14.6 µW.

Fig. 7 plots the ideal and simulated input-output characteristics of the proposed logADC. Fig. 8 shows the calculated differential nonlinearity (DNL) and integral nonlinearity (INL), which are in the range of +0.26/-0.32 LSB and +0.19/-0.45 LSB, respectively.

The dynamic performance of the ADC is evaluated by performing transient simulations with time-varying input voltage signals. In a linear ADC, a pure sinusoidal input signal is used and the output digital codes are converted to waveform to calculate the effective number of bit (ENOB) and the signal-to-noise-and-distortion ratio (SNDR). However, for a logarithmic ADC, an exponential function of a sinusoidal waveform is more suitable because it produces a sinusoidal waveform of the digital output codes [5]. In this work, a simple common-source amplifier with a weak-inversion input PMOS and a resistor load is used to generated the desired exponential input waveform. Fig. 9 shows the waveforms of the exponential input voltage and the reconstructed output of the ADC when a 100 mV, 100 Hz sinusoidal signal is applied to the common-source amplifier. The ADC input signal has a voltage swing between 3 mV to 850 mV and the reconstructed ADC output has a voltage swing between 0.2 V to 0.7 V. A 4096-point Fast Fourier transform (FFT) was used to calculate the spectral component of the reconstructed ADC output. The signal-to-noise-distortion ratio (SNDR) is 31.7 dB, which is equivalent to an effective number of bits (ENOB) of 4.97. The proposed ADC achieves the maximum resolution of 11-bit when the input amplitude is below 7.81 mV and achieves the minimum resolution of 4-bit when the input amplitude is more than 0.5 V. Therefore, the dynamic range is 66 dB. Note that the dynamic range is 30 dB higher than that of a 6-bit linear ADC.

$$FoM = \frac{P}{2^{ENOB} \times f_s} \quad (5)$$

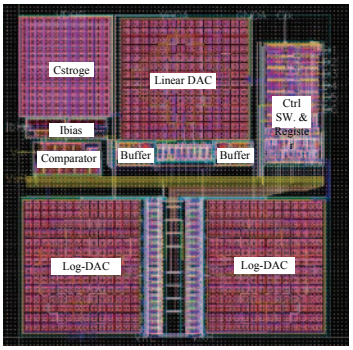

Fig.6. Layout of the proposed logADC with the size of 400 µm x 410 µm

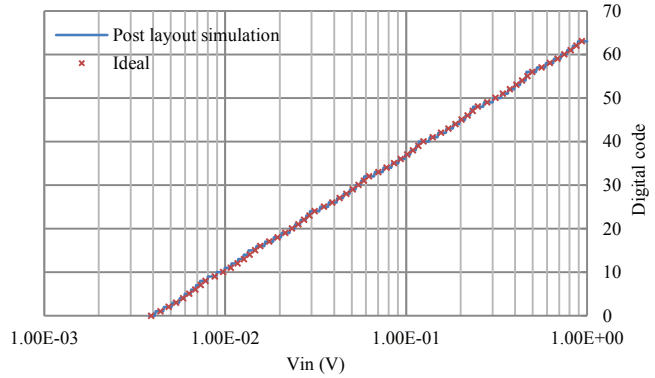

Fig. 7 Input-output characteristic of the proposed 6-bit logADC

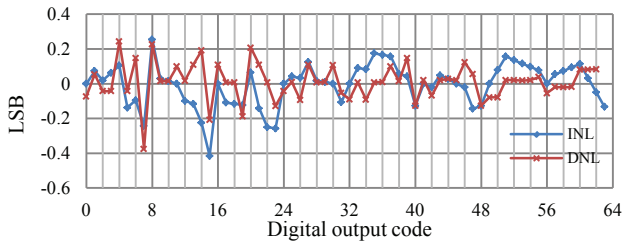

Fig. 8 Simulated INL and DNL

Table II summarizes the simulated performance of the proposed logADC in comparison with other non-linear ADCs. The well-known figure of merit (FoM) of ADC, shown in (5), is used for comparison. The proposed ADC achieves the FoM of 18.6 pJ/conversion-step.

V. Conclusion

This paper described the design and realization of 6-bit low-power logarithmic ADC for biomedical applications in a 0.35 µm CMOS technology. The proposed logarithmic ADC was realized by using the successive approximation topology with two-step DACs. Post-layout simulation results showed that the proposed ADC achieved the energy efficiency of 18.6 pJ/conversion-step at 25 kS/s sampling rate.

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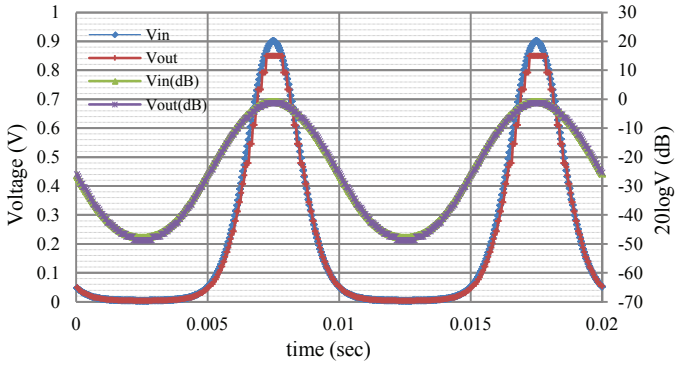

Fig. 9 Waveforms of the ADC input and the reconstructed output voltages

TABLE II. Performance Summary and Comparisons

Parameter type	This work	[1]	[2]	[5]	[7]
Type	Log	Log	Log	Log	Exp.
Topology	SAR	Dual-slope	Pipeline	Cyclic	SAR
Supply	1.8	3	1.62	1	1.8
Power	4.36-14.6 µW	3 µW	2.54 mW	0.33 µW	40 µW
Sampling rate	25 kS/s	300 S/s	22 MS/s	1 kS/s	25 kS/s
Number of bits	6	8	8	6	8
ENOB (bit)	4.97	7.85	5.62	5.95	N/A
Full scale range	1 V	350 nA	1 V	100 nA	1 V
Max. INL	+0.19/-0.45	0.5	0.77	0.88	+4.3/-2.1
Max. DNL	+0.26/-0.32	1	0.32	0.8	+0.8/-0.9
SNDR (dB)	31.7	49	35.6	37.6	N/A
DR	66	60.1	80	40	64.1
FoM (pJ/conv-step)	18.6	41.7	2.38	5.33	N/A
Area (mm^2)	0.164	4.84*	0.56	N/A	0.036
Process (µm)	0.35	1.5	0.18	0.18	0.18

* with PAD and testing circuit area

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