A 32-Ch. Bidirectional Neural/EMG Interface with on-Chip Spike Detection for Sensorimotor Feedback

Ian Williams[†⋆], Adrien Rapeaux[†⋆], Yan Liu[†⋆], Song Luan[†⋆] and Timothy G. Constandinou[†⋆]

†Department of Electrical and Electronic Engineering, Imperial College London, SW7 2BT, UK

⋆Centre for Bio-Inspired Technology, Institute of Biomedical Eng., Imperial College London, SW7 2AZ, UK

Email: {i.williams10, adrien.rapeaux13, yan.liu06, s.luan, t.constandinou}@imperial.ac.uk

Abstract—This paper presents a novel 32-channel bidirectional neural interface, capable of high voltage stimulation and low-power, low-noise neural recording. Current-controlled biphasic pulses are output with a voltage compliance of 9.25 V, user-configurable amplitude (max. 315 μA) & phase duration (max. 2 ms). The low-voltage recording amplifiers consume 23 μW per channel with programmable gain between 225 - 4725. Signals are 10-bit sampled at 16 kHz. Data rates are reduced by granular control of active recording channels, spike detection and event-driven communication, and repeatable multi-pulse stimulation configurations.

I. INTRODUCTION

Bidirectional neural interfaces not only provide exciting opportunities for novel neuroscience experiments, but could lead to major benefits in the field of responsive therapeutic neural devices (e.g. for epilepsy [1] and Parkinson disease [2]) where neuromodulation is a function of detectable changes in brain dynamics. However, previous work has generally focused on Deep Brain Stimulation (DBS) implants, while devices designed for the Peripheral Nervous System (PNS) [3] are either not implantable or not integrated, restricting their experimental utility.

The SenseBack project[1] aims to develop technologies to provide prosthetic limb users with sensory feedback from their prosthesis (in particular mimicking natural tactile and proprioceptive neural patterns) ultimately to enhance the control, effectiveness and acceptability of the artificial limb to the user [4]. Developed technology will be integrated into a platform for chronic implantation in the PNS of a rat as depicted in Fig. 1.

The core of the implant is a neural interface capable of neural stimulation and recording (as well as EMG recording by adjusting channel gain settings) on any of its 32 channels. A flexible bidirectional interface such as this maximises the utility of each implanted electrode and provides a number of benefits including: performing a broader range of experiments (e.g. closed-loop experiments), the ability to more closely mimic neural signals which are contingent on system state and wider neural activity (e.g. proprioceptive muscle spindle signals which are dependent on muscle state and fusimotor activity), and can help identify neuron types and stimulation requirements from recorded information.

Developing an implantable bidirectional interface suitable for use with an inductive transcutaneous link presents significant size, power and data rate challenges. This paper describes a novel highly-integrated neural interface IC (controlled using
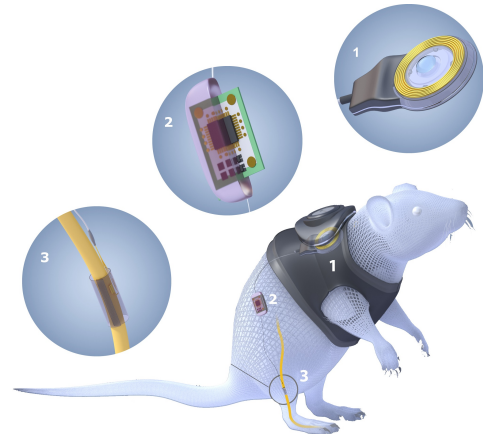

Fig. 1. Senseback implant platform. (1) inductive, transcutaneous link between a backpack and implantable biotelemetry; (2) bidirectional neural interface implant (the subject of this paper); and (3) flexible, biocompatible penetrating microelectrode array implanted on a peripheral nerve.

an SPI link) using low-power neural recording and High-Voltage (HV) charge-balanced stimulation. In comparison to previous bidirectional ICs, here power and data rates are reduced by usage of spike detection (enabling low data rate & power event driven data transmission), on chip storage of stimulation profiles (enabling a single SPI word to trigger up to 256 stimulations) and an onboard Phase Locked Loop (PLL) (enabling use of a low power 32kHz external oscillator). The stimulation system is capable of incrementally decreasing or increasing interpulse times in order to efficiently achieve stimulation frequency modulation, as well as symmetric and asymmetric biphasic pulses. Additionally, an electrode voltage monitoring circuit is included to provide information on electrode health and impedance.

This paper is organised as follows: Section II introduces the top level system architecture; Section III describes the circuit implementation; Section IV presents simulated performance measures and noise measurements; and finally Section V summarises the system design and performance.

II. SYSTEM ARCHITECTURE

The system (Fig. 2) is broadly composed of 6 main parts:

1) Neural recorder – 32 analogue amplification channels multiplexed into 8 ADCs (providing a gain of 225-4725 and outputting second-order high & low pass filtered 10-bit digital samples). Each recording channel can be independently enabled/disabled and configured. Protection of the recording subsystem during stimulation is discussed in Section III-G;
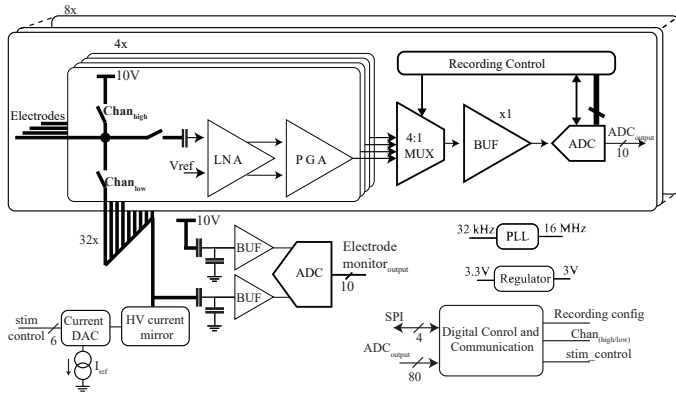
Fig. 2. System architecture: 32 parallel recording channels with blocks of 4 channels sharing an ADC; a single current control block combined with a 32-channel H-bridge; digital communication & control; and ancillary support (LDO and PLL). Each electrode (cuff or intraneural) can be used for stimulation or recording. Thick lines indicate HV.

2) Stimulation control – a 6-bit programmable current sink (with additional high gain setting) controls the stimulation current to provide current-controlled biphasic stimulation pulses with user-defined amplitude and phase/interphase duration. This block uses predominantly low-voltage components, but has HV thin oxide protection transistors at the output.

3) H-bridge – a 32-branch HV H-bridge steers the stimulation current through any pair of the 32 electrodes.

4) Electrode monitor – HV potential dividers combined with low voltage buffers and a differential ADC, scale and digitise the voltage measured across the pair of stimulating electrodes during stimulation.

5) Digital control and communications – an SPI interface with the IC to enable system configuration, recorded signal readout, stimulation profile creation and enabling of stimulation and recording blocks.

6) Auxiliary circuits – a Low Drop Out (LDO) regulator creating a clean 3 V signal from the 3.3 V supply; and a PLL generating 16 MHz from a low power external 32 kHz oscillator.

III. CIRCUIT IMPLEMENTATION

The system was implemented in the $0.35\,\mu m$ HV CMOS AMS process (see Fig. 3). The system requires 3 power supplies at: 3.3 V for all the low voltage circuitry; 10 V for stimulation; and 20 V for ESD purposes (as the H-bridge acts as a charge pump) and to drive HV digital logic. As a result of these power domains the system has 2 pad rings; a HV ring with 36 pads and a LV ring with 18 pads.

A. Stimulation

A standard beta-multiplier current reference (500 nA) is used and combined with a 6-bit binary weighted cascode current-mirror DAC scaling the current from 0 to $6.3\mu A$ in 100 nA steps. The 6-bit DAC has cascoded outputs to improve mirroring and linearity at all current levels.

The output stage consists of two sets of regulated cascode current mirrors with a thin oxide HV transistor (max. 3.3 V V_{GS}, but 20 V V_{DS}) cascoding a LV transistor (see Fig. 4). The mirrors amplify the DAC current by 5 and 45 (high gain
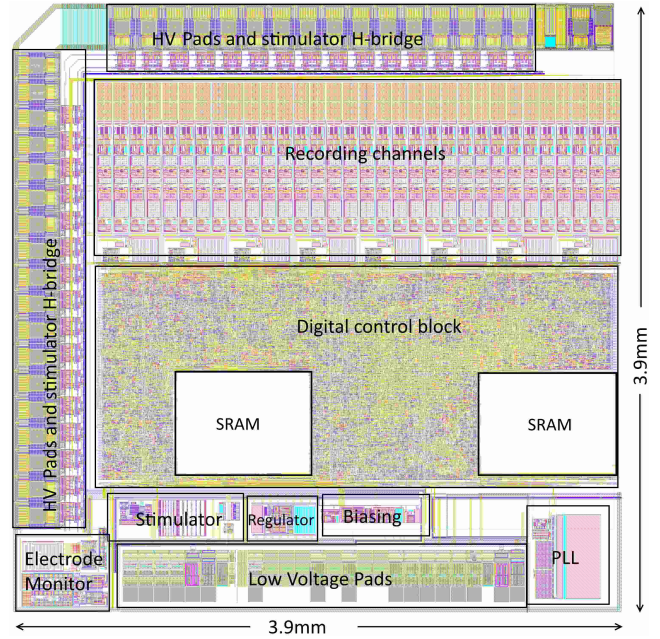

Fig. 3. The SenseBack die layout in $0.35\mu m$ HV CMOS.

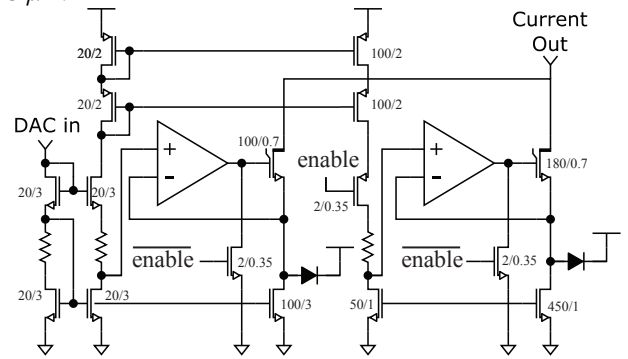option) respectively giving a maximum stimulation current of $315\,\mu A$.

Fig. 4. HV output stage. Shut-off signals allow independent operation of low and high output branches. All resistors values are $32\,k\Omega$.

B. H-bridge

The H-bridge is designed to connect one of two buses running along the periphery of the chip to any pair of electrode bondpads. The buses are connected to the current output buffer of the stimulator and 10 V supply line respectively. To avoid complicated routing each electrode bondpad is connected to a half-H-bridge, designed as a pair of HV symmetrical thick oxide transistor switches driven by HV level shifters.

C. Recording

Each analogue recording channel (shown in Fig. 5) consists of 4 stages of amplifiers, the first two have a combined gain of $\times 225$ and a tunable 1st order high pass filter, the third stage is unity gain, while the fourth stage has a 4 level programmable gain of between 1 and 21. This results in a total gain of between 225 and 4725 and combines to give a 2nd order low pass filter. The output of 4 channels of amplification are time multiplexed into a single 10-bit Successive Approximation Register (SAR) ADC sampling at 64 kHz (16 kHz per channel). More detail is available in [5].
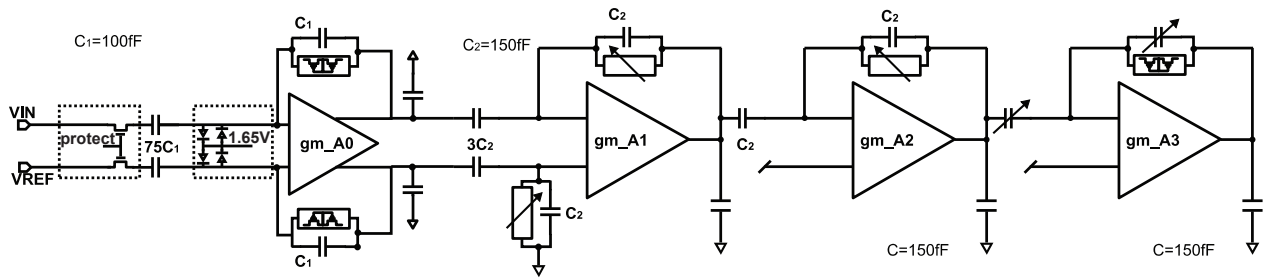
Fig. 5.   Recording amplifier chain (adapted from [5]). Dashed boxes represent the HV protection measures described in Section III-G.
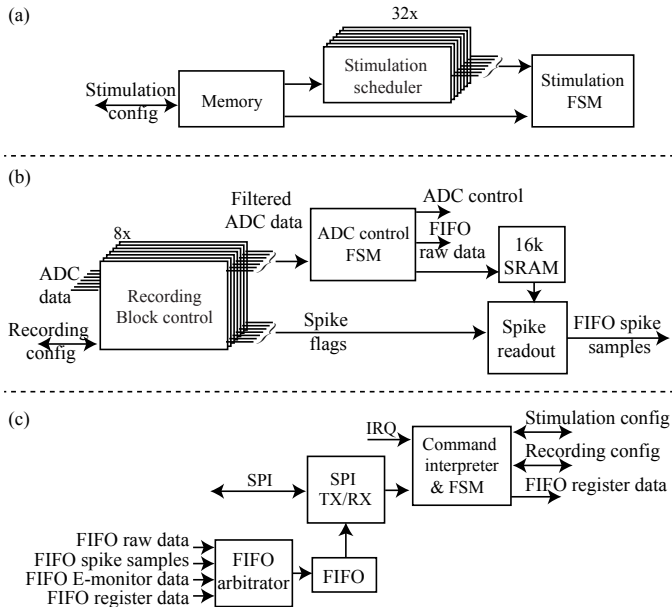

Fig. 6.   The digital communication and control system, main data flows: (a) for triggering stimulation, (b) for recorded data processing, and (c) for streaming out the recorded data.

D. Electrode monitor

The electrode monitor consists of 2 capacitive potential dividers (gain of $1/8$, total capacitance $1.6\,\mathrm{pF}$), one connected to each of the buses that form the upper and lower rails of the H-bridge (see Fig. 2). These potential dividers are used to scale the HV stimulation signals down to low voltage before they are buffered and digitised using another 10-bit SAR ADC. Voltages are recorded at 256kHz before, during and after the stimulation cycle, enabling real time telemetry of electrode & tissue resistance and reactance.

E. Digital control and communication

Digital control can be considered in 3 distinct parts: stimulation control, recording control, and communications (as shown in Fig. 6).

Stimulation is controlled by the user by first writing (over SPI) stimulation configuration(s) (see Table I) to memory. Each configuration can initiate up to 256 stimulations and 32 configurations can be stored. Following configuration setting, a single SPI word is used to select a configuration to be activated. This causes the configuration to be loaded into 1 of 20 schedulers (or queued if no schedulers are available). The stimulation scheduler waits for the indicated interpulse delay and then flags for a stimulation to occur, once the

stimulation has been carried out by the stimulation Finite State Machine (FSM) then the scheduler changes the interpulse delay (according to the loaded interpulse ramp setting) and decrements the repetition number. This setup enables a single spi word to trigger up to 255 stimulations with varying stimulation frequency. The stimulation FSM is constantly checking for stimulation flags and when one is raised it performs the stimulation by setting/clearing appropriately timed signals (8-bit control of stimulation phase and interphase duration) to the H-bridge, current control block and blanking signal to the recording blocks. Asymmetric pulses (with reduced charge balance performance) are possible by setting a 2-bit 'asymmetry ratio', this setting bit-shifts the anodic phase duration and anodic amplitude thereby stretching the duration while also decreasing the amplitude.

TABLE I.   STIMULATION CONFIGURATION STRUCTURE

Word	Bit							
	7	6	5	4	3	2	1	0
0	High I*	–	Stimulation amplitude					
1	Phase duration							
2	Asym-ratio†	–	Stimulation channel A					
3	–	Stimulation channel B						
4	Interphase duration							
5	Interpulse duration							
6	Interpulse ramp change							
7	Number of stimulation repetitions							

* Activate the high current branch of the stimulation output.
† Control the asymmetry between cathodic and anodic phases.

Recording control is achieved using a separate small controller for each recording block. Each controller enables/disables individual channels, sets the channel configuration and also contains a digital IIR filter and spike detection circuitry that is used to process each ADC sample as it comes in. Spike detection involves detecting when the absolute value of an ADC sample exceeds a user-defined channel-specific threshold for 3 consecutive samples, the block controller then waits a further 9 samples and then flags that a spike has been detected and stores a timestamp which acts as a pointer to the spike location in memory. The spike readout block waits for a channel to flag a spike and then reads out the appropriate 16 samples from memory (4 before and 11 after the initial threshold crossing). A global ADC controller provides the necessary timing for all the recording ADCs and also manages the writing of samples to memory (in spike detection mode) or the FIFO (in streaming mode).

Communication with the IC is over a 16 MHz SPI link with the IC as SPI master, but if data needs to be sent to the master, then communication can be requested by a slave IC by setting

the IRQ line high.

F. Other components

A PMOS pass LDO provides 3 V clean supply from the 3.3 V to the recording, while a PLL translates a low power 32 kHz reference clock input up to 16 MHz.

G. HV protection

To protect sensitive LV recording gates, HV DC blocking capacitors are placed at the input to the recording front end. Two further forms of protection are assessed (see Fig. 5) on the IC: the first is the use of a HV transistor pass transistor which is disabled during stimulation, the second is the use of back-back parasitic diodes clamping both differential inputs to within a diode drop of 1.65 V.

IV. RESULTS

Figs. 7 and 8 illustrate the simulated system performance. Fig. 7 shows the charge balance performance for a maximum amplitude stimulation delivering 5nC into a simplified model (series RC) of a cuff electrode, indicating <0.02% charge error. Fig. 8 shows the recording performance and the blanking interaction between the recording and stimulation during a stimulation cycle.

Table II shows comparison figures with other state of the art bidirectional ICs.
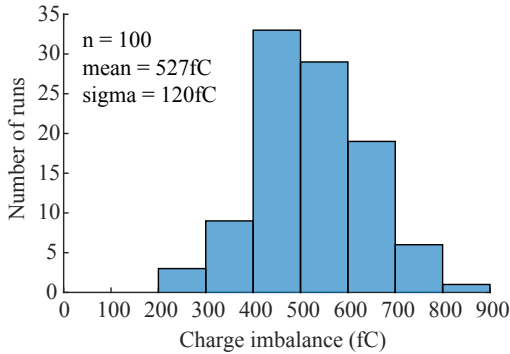

Fig. 7. Stimulation charge balancing over 100 Monte Carlo runs for a symmetrical biphasic pulse. Anodic and cathodic pulse duration and amplitude are 16 μs and 315 μA respectively.

TABLE II. PERFORMANCE COMPARISON

	[6]	[7]	[8]	This work
Technology	0.18 μm	0.18 μm HV	0.5 μm	0.35 μm HV
No. of channels	8	4	8	32
ENOB	6.5	N/A	7.5	9.1
Voltage compliance	4.5	16.4	1.8	9.25
Input-referred noise	1.16 μV[†]	>2.8 μV[†]	6.4 μV[†]	3.8 μV[†]

* Voltage controlled stimulator – off chip control.
† 3 kHz, 10 kHz, 10 kHz and 10 kHz bandwidth respectively

V. CONCLUSION

This paper presented a highly integrated 32-channel bidirectional neural interface IC targeted at implantation in a rat with:

- current controlled HV stimulation and low noise, low power neural recording through the same electrodes;
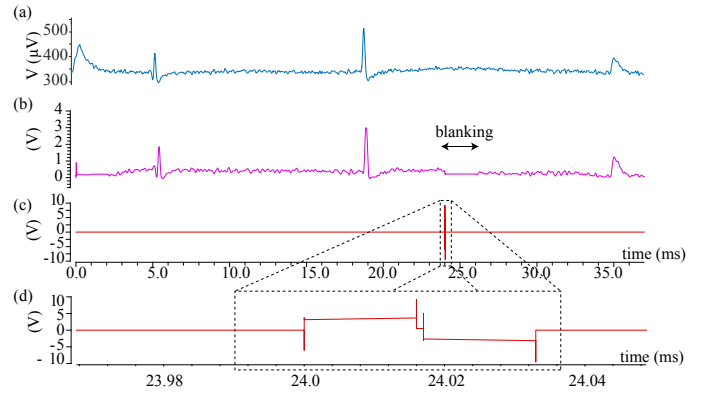

Fig. 8. Recording and stimulation waveforms. (a) The waveform at the electrode; (b) the output of the analogue neural amplifier chain with blanking during a stimulation; (c) the stimulation waveform (voltage across two electrodes); and (d) zoom in on the stimulation waveform.

- data rate reduction using spike detection, individual control of channel enabling, and flexible multi-pulse stimulation initiation;

- Front-end recording protection;

- HV electrode monitoring during stimulation.

Ultimately these features deliver a flexible platform suitable for chronic implantation, that can interface with intra/extra-neural electrodes to stimulate & record neural signals in the PNS or brain, enabling novel closed loop experiments as well as providing the ability to monitor electrode impedance and health in real time.

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