ALGORITHMS FOR THE STATISTICAL DESIGN OF ELECTRICAL CIRCUITS

A THESIS SUBMITTED FOR THE DEGREE OF DOCTOR OF PHILOSOPHY IN THE FACULTY OF ENGINEERING, THE UNIVERSITY OF LONDON.

BY

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ABSTRACT

The research reported in this thesis is concerned with algorithms for designing for statistical variations in the performance of manufactured circuits. The variation in performance is a consequence of variations in component parameter values which in turn result from uncertainties in the process of manufacture of these components or to their dependence on environmental effects such as temperature.

The research contribution can be seen to comprise three distinct elements: (a) A review of the general field of statistical design (chapter 1) and an assessment of existing techniques and algorithms, including a clear problem formulation and classification (chapter 2). (b) A practical investigation of some of the techniques reviewed and the proposal, implementation and general investigation of new algorithms to extend the range of problems addressed (chapter 3,4 and 5) and (c) the identification of areas of further research (chapters 2 and 6).

The thesis commences with an overview of the general field of statistical design, followed by a critical review of existing algorithms and techniques addressed to some particular statistical design problems (namely tolerance assignment and design centering). The next three chapters present contributions of new algorithms and techniques. In chapter three we discuss branch and bound methods of discrete optimization, applied to the tolerance assignment and design centering problems. A geometrically based feasibility testing procedure, INDENTATION, is described and demonstrated for a particular circuit example. In chapter four iterative Monte Carlo based design centering methods are described and demonstrated for circuit examples involving up to 43 variable components. Special sampling schemes for reducing overall computational effort are discussed and compared. In chapter five, iterative Monte Carlo based tolerance assignment methods are considered. Results of a practical investigation of an existing method, TOLERATE, are presented and its shortcomings are demonstrated. A new method, PERTOL, which overcomes some of these shortcomings is proposed and demonstrated for practical circuit examples. Finally, in chapter six an assessment of existing techniques (including those reported in this thesis) is made and areas of further research identified.

To my Mother and Father

ਪੜਿ ਪੜਿ ਗਡੀ ਲਦੀਅਹਿ। ਪੜਿ ਪੜਿ ਭਰੀਅਹਿ ਸਾਥ।
ਪੜਿ ਪੜਿ ਬੇੜੀ ਪਾਈਐ। ਪੜਿ ਪੜਿ ਗਡੀਅਹਿ ਖਾਤ।
ਪੜੀਅਹਿ ਜੇਤੇ ਬਰਸ ਬਰਸ। ਪੜੀਅਹਿ ਜੇਤੇ ਮਾਸ।
ਪੜੀਅਹਿ ਜੇਤੇ ਆਰਜਾ। ਪੜਿਅਹਿ ਜੇਤੇ ਸਾਸ।
ਨਾਨਕ ਲੇਖੈ ਇਕ ਗਲ। ਹੋਰੁ ਹਉਮੈ ਝਖਣਾ ਝਾਖ।

A man may load carts with books; he may load men with books to take with him;

Books may be put on boats; pits may be filled with them.

A man may read books for months; he may read them for years;

He may read them for life; he may read them while he hath breath -

Nanak, only one word, God's name, would be of account; all else would be the senseless discussion of pride.

Guru Nanak

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STATEMENT OF ORIGINALITY

As far as the author is aware, the opinions and techniques presented in this thesis are his own unless otherwise acknowledged by making specific reference. The main contributions are deemed to be the following:

1. The proposal and implementation of an iterative, small sample, Monte Carlo based, statistical method (called MYOSE) for design centering, and its verification for practical circuit examples (chapter 4). This includes the proposal of specific criteria for choosing a direction of search and step size (to move the design centre to improve yield) based on results obtained in Monte Carlo analysis.

In addition, in the case where only certain discrete values for the design centers may be available, the demonstration of the efficacy of a procedure for rounding of the optimum continuous solution to the nearest discrete solutions.

2. The proposal and incorporation in MYOSE (chapter 4) of a special sampling scheme (called the common points scheme) to reduce computational cost by re-employing both for design centering and yield estimation, at current iterations, circuit analyses performed at previous iterations. In addition the demonstration of the added efficiency of this sampling scheme for purposes of ranking yield estimates when their confidence intervals overlap, and a practical comparison of the common points scheme with a standard sampling scheme, called correlated sampling /1/.

3. A practical assessment of an existing Monte Carlo based, statistical method of tolerance assignment, TOLERATE /2/ (chapter 5). The proposal and implementation of a more effective technique, called PERTOL. This includes the proposal of specific criteria for choosing nominals and tolerances on the basis of results obtained in Monte Carlo analysis. In addition a practical comparison of the two methods when applied to particular circuit examples.

4. The proposal and implementation of a geometrical technique (called INDENTATION) for testing the worst case feasibility (i.e. 100% yield) of tolerance solutions; as part of a general branch and bound method /4/ for tolerance assignment and design centering for the situations where only discrete values of tolerances and nominals may be available (chapter 3). This includes a demonstration of the applicability of the method for a particular circuit example.

5. A critical review and classification of existing methods for tolerance assignment and design centering. (chapter 2).

6. A review of specific problems and techniques in the general field of statistical circuit design. (chapter 1).

7. An identification of the outstanding problems in the field of statistical design of electrical circuits, and proposals for future research in this area in the light of the contributions in this thesis. (chapter 6).

CHAPTER 1 - STATISTICAL CIRCUIT DESIGN - THE SCENARIO

1.1 Introduction.

1.2 Notation and terminology.

1.3 Statistical analysis.

- 1.3.1 Monte Carlo analysis.
- 1.3.2 The method of moments.

1.4 Parameter value distributions.

- 1.4.1 Discrete components.
- 1.4.2 Integrated circuits components.

1.5 Statistical circuit design - some scenarios.

- 1.5.1 Tolerance assignment and design centering.
- 1.5.2 Choice of performance specifications.
  - (a) Specification sensitivity.
  - (b) System specification.
- 1.5.3 Specification of manufacturing tests.
  - (a) Go-no Go testing.
  - (b) Accounting for environmantal effects in factory testing.
  - (c) Selection of testing accuracy.

1.6 Summary.

CHAPTER 1

STATISTICAL CIRCUIT DESIGN - THE SCENARIO

1.1 INTRODUCTION

The increasing degree of reliance placed on computer aids by circuit and systems designers may be traced to two broad trends. Firstly, the availability in increasing volume of progressively cheaper and more powerful computing facilities. Concomitant with this trend has been the discovery and development of numerous algorithms and programs /5/[α] addressed to the solution of various problems in the design and manufacture of electrical circuits and systems. Secondly, there has been a proliferation in the range and complexity of available devices and circuits, such as integrated circuits. For these, some of the traditional methods of approximate modelling and laboratory simulation and experimentation (e.g. breadboarding) are inadequate.

Three broad areas of engineering activity for which computer aids are available may be discerned. Firstly, in circuit design, where the principal aids are circuit simulators. These comprise facilities for describing to the computer program, the topology of the circuit, the component types and their parameter values. The program employs appropriate mathematical models of the electrical behaviour of the relevant components, and facilitates numerical simulation to study and change the circuit

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[α] An extensive review of available circuit analysis packages is reported by Bowers and Zobriest et al /6/.

to improve its performance. Secondly, computer aids are essential in the area of component layout, the routing of interconnections, the drafting of artwork for photo-lithographic processes etc, in the manufacture of many types of electrical circuits, especially integrated circuits /7/. Thirdly, with the increased complexity of performance of circuits and systems, and for greater cost effectiveness, computer aids are increasingly being brought to the factory floor to aid activities such as testing, verifying performance and detecting faults in manufactured circuits and systems /8/.

Therefore in some specific areas of application, computers help perform traditional design tasks more efficiently, and in others design activities are introduced which could only be performed crudely and with a large degree of approximation if at all by non computer aided methods. One such area of application in the field of circuit design, is statistical design. The most common application of computers in circuit design is in performing analyses of circuit behaviour to compute various responses such as voltages, currents, power gains, time delays, sensitivities etc. This information is then used either manually by the designer, or automatically by the computer program, to make adjustments to the proposed circuit, to improve its performance with respect to appropriate criteria. Here the designer is experimenting with the nominal circuit. However, when a circuit is to be manufactured in large numbers,the designer must analyse and design for statistical spreads in the performance of nominally identical circuits, arising from statistical

spreads encountered in values of the parameters of their constituent components. This latter design activity is called statistical design.

For illustration consider the representation of figure 1.1. For a particular set of stimuli $S = S_1 \ldots\ldots S_r$, the circuit responses $f_1 f_2 \ldots\ldots f_m$ are functions of the component parameters $P = p_1 p_2 \ldots\ldots p_k$, i.e. $f_j = f_j(p_1 \ldots\ldots p_k)$; $j=1 \ldots\ldots m$. For example, for a frequency selective circuit, the parameters may be values of the resistances, capacitances and inductances, while the f_j (.) may be responses such as insertion loss, group delay etc, at a number of frequencies. Uncertainty is associated with the values of the component parameters and thus the values of the response functions, in the following sense. If a number of nominally identical circuits are to be manufactured (assembled or fabricated) from their constituent components, then variations in the processes of manufacture of the components cause the values of their parameters to be statistically distributed. Consequently, the response values of the manufactured circuits also display variation from one circuit sample to another. In addition the response of a particular circuit whose component parameters have particular values $p_1{}^* p_2{}^* \ldots\ldots p_k{}^*$ at the time of manufacture, will experience a non-deterministic drift in response, as a result of drift in the values of these component parameters due to factors such as fluctuations in the environmental conditions of service (e.g. temperature or humidity) or component ageing.

The spread in performance may be such that some of the manufactured circuits fail to meet the required limits on response values specified by the customer. Therefore, yield[α,β] will be less than 1 (100%). The failing circuits need then be discarded or repaired, hence incurring additional cost. The extent of spread of response may be reduced and hence the yield increased by employing more precise (i.e. subject to a smaller extent of spread) components. However, precise components are more expensive. Therefore, the circuit designer may seek a compromise between yield and precision (generally called tolerance) of component parameters to minimize overall cost. This particular design problem is called tolerance assignment. On the other hand yield may be increased by re-assigning the nominal values of the component parameters, while their tolerances remain fixed. This latter procedure is called design centering. In the general case a combined procedure for reassigning both tolerances and nominals will lead to the design of the most cost effective circuits.

Numerous algorithms have been proposed for various formulations of the design centering and tolerance assignment problems. The work reported in this thesis is addressed to a critical

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[α]Yield is that proportion of manufactured circuits whose response meets the limits specified by the customer. Yield will be formally defined in section 1.2.

[β]From the point of view of yield, we shall only consider circuits which are assumed to be free from gross errors, such as wiring faults, mask misalignment, crystal defects etc.

survey of the nature and limitations of existing methods, and the proposal and investigation of new and improved methods. In chapter two several formulations of these design problems are presented, together with a classification and critical review of proposed solution techniques. The next three chapters then report the proposal, implementation and general investigation of a number of new algorithms. Finally, in chapter six, we outline areas of future research in this field.

The aims of this chapter are two fold. Firstly, we introduce a consistent terminology and notation to be then used throughout this thesis. In addition the expected parameter distributions and methods of statistical analysis are briefly reviewed. Secondly, we note that tolerance assignment and design centering are particular instances of statistical design problems. Therefore the latter half of this chapter discusses various scenarios to illustrate the wider scope of statistical design.

1.2 NOTATION AND TERMINOLOGY

Let $p \triangleq p_1 p_2 \ldots p_K$ be a general set of values for the component parameters of the circuit in question. P can be thought of as a point in a K-dimensional space (called the input space). The variability of P can be represented by a K-dimensional probability density function (p.d.f.), denoted by $\emptyset(P)$. Therefore the following equation holds:

$$\int_{-\infty}^{\infty} \cdots \int_{-\infty}^{\infty} \emptyset(P)\, dp_1 \ldots dp_K = 1 \qquad 1.1$$

In practice the range of variation of the individual parameters

will be truncated i.e.

$$\emptyset(P) = 0 \text{ for } \underline{p}_j \leq p_j \leq \overline{p}_j \quad j=1 \text{ .... } K \tag{1.2}$$

Where $\underline{p}_j$ and $\overline{p}_j$ are constants, respectively termed the lower limit and the upper limit of variation of the jth parameter. Also consider the vector of tolerances

$T \triangleq t_1 t_2 \text{ .... } t_K$ where $t_i = (\overline{p}_i - \underline{p}_i)/2 \quad i=1 \text{ ..... } K$

and the vector of nominal values:

$P^o \triangleq p_1^o \text{ ..... } p_K^o$ where, $p_i^o = (\overline{p}_i + \underline{p}_i)/2$

Equation 1.1 may then be rewritten as

$$\int_{p_K^o - t_K}^{p_K^o + t_K} \text{..........} \int_{p_i^o - t_1}^{p_i^o + t_1} \emptyset(P)\, dp_1\, dp_2 \quad dp_K \simeq 1 \tag{1.3}$$

Relation (1.2) defines a region in the input space, called the tolerance region, and denoted R_T, such that

$$P \in R_T \text{ if } \emptyset(P) > 0 \tag{1.4}$$

Clearly R_T is a hyper rectangle, with center P^o and sides of length $2t_i$, i=1 ..... K. A geometrical representation is given in figure 1.2. Also we denote by $f_i(P)$, i=1 .... m the response functions of the circuit. The variability of these responses may be modelled in terms of another joint probability density function, which is denoted as $\Omega(f_1 f_2 \text{ .... } f_m)$. In addition we denote by $\Omega_i(f_i)$ the particular p.d.f. of the ith performance function. The

problems of statistical analysis involve computation of various parameters of the function $\Omega(.)$. For example the customer for whom the circuit is manufactured may require its response to be constrained such that

$$\underline{f}_i \leq f_i\ (P) \leq \overline{f}_i \qquad i=1\ \ldots\ldots\ m \qquad 1.5$$

where $\underline{f}_i$ and $\overline{f}_i$ are constants. The proportion of manufactured circuits which meet condition 1.5 is termed the production yield, and may be written as the multi-dimensional integral

$$\text{Yield} = \int_{\underline{f}_m}^{\overline{f}_m} \cdots \int_{\underline{f}_1}^{\overline{f}_1} \Omega(f_1\ \ldots\ldots\ f_m)\ df_1\ \ldots\ df_m \qquad 1.6$$

Alternately we may define a testing function g(P) reflecting the acceptance or rejection of a circuit, such that

$g(P) = 1$ if $\underline{f}_i \leq f_i\ (P) \leq \overline{f}_i \quad i = 1\ \ldots\ldots\ m$ 1.7

and $= 0$ otherwise.

Yield is then the following expectation.

$$\text{Yield} = \langle g(P) \rangle = \int_{p_K^o - t_K}^{p_K^o + t_K} \ldots\ldots \int_{p_1^o - t_1}^{p_1^o + t_1} g(P)\emptyset(P)\ dp_1\ \ldots\ldots\ dp_K \qquad 1.8$$

Relation (1.7) allows definition of another region in the input space, the region of acceptability, R_A, such that

$$P \in R_A \quad \text{if} \quad g(P) = 1 \qquad 1.9$$

Clearly R_A represents all those combinations of component values which result in acceptable circuits. With the definition of the tolerance region R_T and the region of

acceptability R_A it is useful to consider a geometrical interpretation of yield, as represented in figure 1.2. Here we consider a 2 dimensional example (K=2), with nominal $P^o = p_1^o, p_2^o$ and tolerances $T = t_1, t_2$. Initially we assume that the p.d.f. $\emptyset(P)$ is bivariate uniform and the parameters are statistically independent /9, chapter 5/, i.e. $\emptyset(P) = \emptyset_1(p_1).\emptyset_2(p_2)$

and

$$\emptyset_1(p_1) \begin{cases} = \frac{1}{2t_1} & \text{for } (p_1^o - t_1) \leq p_1 \leq (p_1^o + t_1) \\ = 0 & \text{otherwise} \end{cases} \qquad 1.10$$

and

$$\emptyset_2(p_2) \begin{cases} = \frac{1}{2t_2} & \text{for } (p_2^o - t_2) \leq p_2 \leq (p_2^o + t_2) \\ = 0 & \text{otherwise} \end{cases}$$

Then, yield is the ratio of the areas (in the general case volumes) of the regions $(R_T \cap R_A)$ and R_T. That is;

$$\text{Yield} = V(R_T \cap R_A)/V(R_T). \qquad 1.11$$

Where V(.) indicates volume. For the more general case the parameter values may be statistically dependent (correlated) and the individual probability density functions may be other than uniform. In that case the function $\emptyset(.)$ may be taken to represent a weighting of the points of R_T. Hence the volumes in expression 1.11 should now be interpreted as weighted volumes.

1.3 STATISTICAL ANALYSIS

Statistical analysis involves computation of various parameters of the output probability density function $\Omega(.)$.

For example, for a particular set of nominal values, tolerances and input p.d.f., it is very important to estimate the expected production yield. For the present discussion, it is assumed; (i) that for a set of values P* for the K parameters of the circuit in question, it is possible to evaluate the m response functions, and (ii) the form of the input probability density function is known. In practice the first assumption is true for most circuits of interest, although evaluation of circuit responses may involve considerable computational expense. However, the statistical distribution of component parameters is not generally known. In some situations, namely discrete components, a simple choice (such as Uniform or Gaussian p.d.f.) may suffice. However, for integrated circuits, the function $\emptyset(.)$ may be very complex. The question of suitable choice for $\emptyset(.)$ is discussed later.

A thorough review of different methods of statistical analysis is reported by Tahim /10/. We shall re-iterate the main features of two methods, namely, Monte Carlo analysis and the method of moments. These are emphasised here because of their importance as integral parts of certain statistical design methods, to be discussed in this thesis. Monte Carlo analysis is a direct and general method, applicable to all circuit problems. However, it is computationally very expensive and may be prohibitively so in many cases. On the other hand the method of moments, although computationally cheaper, involves considerable approximation. However, the approximations may not hold in all situations. Nevertheless, the method of moments is useful in several statistical design methods.

1.3.1 MONTE CARLO ANALYSIS

In this method, illustrated in figure 1.3, a number N: P_1 P_2 ..... P_N, of sets of sample circuit values are generated. These values are obtained by suitably transforming pseudo random numbers, so that they are distributed according to the relevant p.d.f. $\emptyset(.)$. This is illustrated for a two dimensional example in figure 1.4. The sample circuits are analysed and a representation of the performance distribution is obtained. To illustrate its salient features, the use of the method for estimating yield is discussed here.

The Monte Carlo method simulates the process which takes place in a circuit production run. Circuits are assembled using components randomly picked from particular bins[α]. In the equivalent computer exercise, random numbers are generated with a uniform distribution, in the interval 0 to 1 and are then transformed (this is illustrated for one component in figure 1.5) to satisfy the required p.d.f. Each set of component parameter values, representing a manufactured circuit, is analysed and the corresponding values of the performance functions are obtained. Each analysed circuit is assigned to one of two mutually exclusive classes namely acceptable and reject. An acceptable circuit is one which meets all performance requirements such as relation 1.5. A reject circuit is one which fails at least one requirement. The process is repeated a number of times and yield is estimated as follows.

[α]Although for integrated circuits, individual components may not be handled, the analogy still holds.

If, of N analysed circuits NA are found to be acceptable then $\tilde{Y} = NA/N$ is an unbiased estimate[α] of the true yield Y. $\tilde{Y}$ is a random variable, since if the experiment were to be repeated with a different set of N sample circuits, a different value would be obtained for $\tilde{Y}$. It is appropriate to consider the accuracy of the estimate $\tilde{Y}$, and its dependence on the number of circuits analysed. Specifically, it is required to construct confidence intervals, so that we can make statements like

$$(\tilde{Y}-C) < Y < (\tilde{Y}+C) \tag{1.12}$$

with a particular degree of confidence. Here, C denotes some constant called the confidence interval.

Each circuit analysis and test for compliance with performance requirements may be taken to be a Bernoulli[β] trial. If the probability that a circuit with randomly selected component values is acceptable, is Y, then the probability of exactly NA acceptable circuits in N trials is

$$F(NA) = \frac{N!}{(N-NA)!\ NA!} \quad Y^{NA}\ (1-Y)^{N-NA} \tag{1.13}$$

The function F(NA) is a Binomial probability density function (p.d.f.) with mean and variance given by:

$$\mu = NY \tag{1.14}$$

[α] In statistics an unbiased estimator is a random variable, whose expected value is the parameter being estimated. An unbiased estimate is an estimate provided by such an estimator. /9, chapter 7, page 230).

[β] A Bernoulli trial is a random experiment which can only have one of two outcomes, e.g. the tossing of a coin.

and $$\sigma^2 = NY(1-Y) \qquad 1.15$$

When N is reasonably large, the Binomial distribution may be approximated by a Gaussian distribution. Therefore, the p.d.f. of the random variable $\tilde{Y}$ may be written as

$$F(\tilde{Y}) = \frac{1}{\sigma_{\tilde{Y}}\sqrt{2\pi}} \exp - \tfrac{1}{2} \frac{(\tilde{Y}-\mu_Y)^2}{\sigma_{\tilde{Y}}} \qquad 1.16$$

where the mean μ_Y and variance σ_Y^2 are given by:

$$\mu_Y = Y \qquad 1.17$$

and

$$\sigma_{\tilde{Y}}^2 = \frac{\tilde{Y}(1-\tilde{Y})}{N} \qquad 1.18$$

Thence the confidence interval for the Yield estimate Y can be constructed as follows. The probability of $\tilde{Y}$ falling in the interval $(\tilde{Y}-\varepsilon\sigma_Y)$ to $(\tilde{Y}+\varepsilon\sigma_Y)$ is the integral

$$\int_{\tilde{Y}-\varepsilon\sigma_{\tilde{Y}}}^{\tilde{Y}+\varepsilon\sigma_{\tilde{Y}}} F(\tilde{Y})\,dY \qquad 1.19$$

$$= \frac{1}{\sqrt{2\pi}} \int_{-\varepsilon}^{\varepsilon} \exp \frac{-x^2}{2}\, dx \qquad 1.20$$

where $x = \dfrac{\tilde{Y}-Y}{\sigma_{\tilde{Y}}}$ and ε is a constant.

The function F(.) is now Gaussian. The most commonly used value for ε is 2, leading to a probability of 0.95 that the true value of yield is between the limits $(\tilde{Y}-2\sigma_{\tilde{Y}})$ and $(\tilde{Y}+2\sigma_{\tilde{Y}})$.

Clearly Monte Carlo analysis is a very general procedure and can accomodate any type of circuit (linear, non-linear etc) and any number and type of circuit response. However, the

repetitive analysis of sample circuits is computationally expensive. The total cost of a Monte Carlo analysis is roughly proportional to N, the number of sample circuits analysed. However, as embodied in equation 1.18 the accuracy of the resulting estimates is proportional to the inverse of the square root (i.e. $1/\sqrt{N}$) of the number of analyses. Therefore to double the accuracy, N has to be increased four fold. For different values of yield, the dependence of the confidence interval on the sample size, is depicted in figure 1.6. The corresponding confidence level is 95% i.e. the probability of bracketing the true yield, in the appropriate confidence intervals is 0.95.

1.3.2 THE METHOD OF MOMENTS

Whereas in the Monte Carlo method an empirical characterization of the output p.d.f. $\Omega(.)$ is constructed, here we consider approximation to $\Omega(.)$ constructed from a knowledge of the moments of the input p.d.f. $\emptyset(.)$ and an approximation of the performance function in terms of the input parameters.

Each of the performance functions $f_i(p_i)$; i=1 .... m, may be expanded in Taylor series /11, Sec.4.10 / to give analytic expressions for these functions in the vicinity of the nominal point P^o. i.e.

$$f_i(p_1 \dots p_K) = f_i(P^o) + \sum_{r=1}^{K} \frac{\partial f_i}{\partial p_r} \Delta p_r + \frac{1}{2} \sum_{r=1}^{K} \sum_{s=1}^{K} \Delta p_r \frac{\partial^2 f_i}{\partial p_r \partial p_s} \Delta p_s + \dots \quad 1.21$$

where the Δp_i are deviations from the nominal values, i.e. $\Delta p_i = p_i - p_i^o$.

Neglecting second and higher order terms in 1.21, we get 1.22

$$f_i(p_1 \dots p_K) = f_i(p^o) + \sum_{r=1}^{K} \frac{\partial f_i}{\partial p_r} \Delta p_r \qquad 1.22$$

We may then easily obtain the following expression relating the variances $\sigma^2_{p_i}$; i=1 ... K, of the input parameters to the variances $\sigma^2_{f_j}$; j=1 ... m of the performance functions,as:

$$\sigma^2_{f_j} = \sum_{i=1}^{K} \frac{\partial f_j}{\partial p_i} \sigma^2_{p_i} + 2 \sum_{r=1}^{K} \sum_{s=1}^{K} \frac{\partial f_j}{\partial p_r} \frac{\partial f_j}{\partial p_s} \text{COV}(p_r, p_s) \dots\dots \quad 1.23$$

Where $\text{COV}(p_r,p_s)$ is the covariance between parameters p_r and p_s. Further the mean value of f_i, will clearly be $f_i(p^o)$. Expressions equivalent to 1.23 may be obtained for all m performance function /3, chapter 3/.

According to the central limit theorem /9, chapter 5/, the joint probability density function of the performance functions will be approximately m-variate Gaussian if several conditions are met /13, chapter 2-3/. These are;
(a) the number of component parameters are large, (b) the variances of a few parameters are not much greater than those of all the others, (c) the individual parameter p.d.f.'s are symmetrical about the nominal values. The diagonal elements of the variance-covariance[α] matrix of $\Omega(.)$ are given by expressions such as 1.20. Similar expressions may

[α] For an m dimensional random variable, the variance-covariance matrix is an (m by m) symmetrical matrix. The elements s_{ij} - i = 1 .... m, j = 1 .... m; are the covariances between component i and j of the random variable.

be obtained relating the covariances of different performance functions to the variances and covariances of the input p.d.fs. These form the non-diagonal elements of the variance covariance matrix of $\Omega(.)$

Even such an approximation to $\Omega(.)$ as a multivariate Gaussian p.d.f., presents formidable computational problems for obtaining yield, since it involves the evaluation of an m dimensional integral, where m may be large.

However, the Normal (Gaussian) approximation can effectively be used to derive bounds on the true value of yield. We first consider the notion of "partial yield". In all there will be m partial yields, Y_i; $i=1 \ldots m$, where Y_i is the probability that a correctly manufactured circuit will meet the ith, performance requirement, i.e.

$$Y_i = \text{Probability } (\underline{f}_i < f_i(P) < \overline{f}_i)$$

or the integral :

$$Y_i = \int_{\underline{f}_i}^{\overline{f}_i} \Omega_i(f_i)df_i \qquad 1.24$$

If all the performance functions were independent, i.e. $\Omega(.)$ was the product

$$\Omega = \prod_{i=1}^{m} \Omega_i \qquad 1.25$$

then the overall yield Y, would be the product

$$Y = \prod_{i=1}^{m} Y_i \qquad 1.26$$

In practice 1.25 does not often hold, and 1.26 is replaced by the inequality 1.27.

$$Y > \prod_{i=1}^{m} Y_i \qquad 1.27$$

Hence, 1.27 provides a lower bound on the yield.

Evaluation of the Y_i, involves single dimensional integrations (expression 1.24). These may be easily performed, since the Ω_i are assumed Gaussian with means and variances calculated from expressions such as 1.23. Tighter bounds on yield may be obtained as follows. Now the probability of occurrence of a reject circuit is the joint probability of occurrence of failure to meet at least one of the m performance requirements. Consider the following additional notation: Let x_j denote the condition that the jth performance requirements is met, i.e.

$$\underline{f}_j \leq f_j(P) \leq \overline{f}_j \qquad 1.28$$

and $\overline{x}_j$ that the condition is not met. Then clearly $Y_i = Pr(x_i)$, where $P_r(.)$ denotes probability.

Therefore we may write:

$$(1-Y) = P_r(\overline{x}_1 + \overline{x}_2 + \ldots\ldots \overline{x}_m) \qquad 1.29$$

From elementary probability theory /9, chapter 2/, 1.29 may be rewritten as:

$$(1-Y) = \{P_r(\overline{x}_1) + P_r(\overline{x}_2) + \ldots\ldots P_r(\overline{x}_m)\} +$$

$$\{Pr(\overline{x}_1\overline{x}_2) + Pr(\overline{x}_1\overline{x}_3) + \ldots\ldots \underset{i \neq j}{Pr(\overline{x}_i\overline{x}_j)} + Pr(\overline{x}_{m-1}, \overline{x}_m)\} + \ldots\ldots$$

$$+ (-1) \; Pr(\overline{x}_1\overline{x}_2 \ldots\ldots \overline{x}_m) \qquad 1.30$$

If we replace $Pr(\bar{x}_i)$, $Pr(\bar{x}_{ij})$ etc as follows.

$$W_j = Pr(\bar{x}_j)$$

$$W_{ij} = Pr(\bar{x}_i\bar{x}_j)$$

and

$$W_{ijk} = Pr(\bar{x}_i\bar{x}_j\bar{x}_k)$$

Then (1.30) may be rewritten as

$$(1-Y) = \sum_{j=1}^{m} W_j + \sum_{j=1}^{m-1} \sum_{k=j+1}^{m} W_{jk} - \sum_{j=1}^{m-2} \sum_{k=j+1}^{m-1} \sum_{\ell=k+1}^{m} W_{jk\ell} + \ldots \qquad 1.31$$

Returning to equation 1.30, we note that the right hand side is the sum of (2^m-1) bracketed addends of non increasing numerical value with alternating signs. According to the Benferoni inequality procedure /3, chapter 3/, if we truncate the right hand side of 1.30, and use only the first K bracketed addends, then the value of the left hand side will be bounded by the first (K-1) and the first K addends. We may use this to obtain closer bounds on yield than 1.27. Equation 1.31 shows three addends. Thus the following bound on yield is obtained:

$$1 - \sum_{j=1}^{m} W_j + \sum_{j=1}^{m-1} \sum_{k=j+1}^{m} W_{jk} - \sum_{j=1}^{m-2} \sum_{k=j+1}^{m-1} \sum_{\ell=k+1}^{m} W_{jk\ell} \le Y \le$$

$$1 - \sum_{j=1}^{m} W_j + \sum_{j=1}^{m-1} \sum_{k=j+1}^{m} W_{jk} \qquad 1.32$$

Clearly, $Y_i = 1-W_i$ etc.

Hence evaluation of the W_i, the W_{ij} and the W_{ijk}, involve the integration of univariate, multivariate and trivariate

Gaussian probability density functions respectively e.g.

$$W_{ijk} = \int_{f_i}^{f_i} \int_{f_j}^{f_j} \int_{f_k}^{f_k} \Omega_i \; \Omega_j \; \Omega_k \quad df_i \; df_j \; df_k \qquad \text{etc.}$$

The procedure for obtaining yield bounds, outlined above is computationally cheaper than Monte Carlo analysis. However, it relies on several series of approximations and assumptions and is therefore less general and less reliable.

1.4 PARAMETER VALUE DISTRIBUTIONS

To perform effective statistical analysis, it is necessary to have knowledge of the statistical distributions of the component parameter values. Distinct differences exist in the distributions encountered in the parameters of components in discrete circuits and those in integrated circuits.

1.4.1 DISCRETE COMPONENTS

For discrete passive elements, i.e. resistors, capacitors, and inductors, it is adequate to determine the nominal values and form of the individual parameter p.d.f. The parameters of the various components in a circuit will be statistically independent. Therefore, the K dimensional joint p.d.f. $\emptyset(.)$, may be written as the product of the individual parameter p.d.fs. i.e.

$$\emptyset(P) = \prod_{i=1}^{K} \emptyset_i(p_i) \qquad 1.33$$

The component manufacturer may impose tolerance limits on a batch of components by removing out of tolerance components. It is therefore convenient to write 1.33 as

$$\emptyset(P,P^o,T) = \prod_{i=1}^{K} \emptyset_i(p_i^o,t_i,p) \qquad 1.34$$

where as before P^o and T are respectively, the nominal value and tolerance vectors. Further we expect

$$\phi_i(p_i,p_i^o,t_i) = 0 \quad \text{for} \quad (p_i^o-t_i) > p_i \qquad 1.35$$

$$\text{or} \quad (p_i^o+t_i) < p_i$$

The form of the p.d.f. for most manufactured components is found to be Gaussian (figure 1.7a), when they leave the production line /12, chapter 6/. This is especially the case if a manufacturer mixes nominally identical components from batches produced at different times. Manufacturers often select components from the middle of the distribution to sell as precision components. Therefore for particulr nominals and tolerances, the distributions encountered by the component purchaser may be of the form shown in figure 1.7b, and 1.7c. For some types of components, e.g. thin film resistors, the probability density function is often found to be markedly skewed, as shown in figure 1.8.

For purposes of circuit analysis discrete active circuits are represented by equivalent circuits. For example, the hybrid Π model, which is applicable when the transistor is used in linear a.c. applications. The different parameters of the equivalent circuit will then be inter-related and their statistical distributions correlated. The interrelations and correlations may be characterized from a knowledge of the physics of the device or more commonly from measurements made on a representative number of sample components.

1.4.2 INTEGRATED CIRCUIT COMPONENTS

The values of the parameters of the components of an integrated circuit are determined by the physical properties (e.g. material properties such as mobility, doping levels, diffusion constants etc) of the material of which the component is made and the geometrical dimensions of its layers. In general parameter tolerances in integrated circuits are larger than those encountered in discrete components, and there are distinct differences in the forms of the distributions encountered. For example, the values of the resistances depend upon sheet resistivity. Uncertainty in the manufacturing processes results in a tolerance of a few percent, on the value of the sheet resistivity from slice to slice. However, the variation of resistivity in circuits on one slice will be very small. Further this variation will be very gradual over the slice. Therefore although large tolerances may be associated with individual resistors, the statistical distribution of values of resistors in close proximity on single chips, will be correlated, thus reducing the overall tolerance effect. Therefore the designer of integrated circuits may exploit this fact by designing circuits whose performance depends upon ratios of resistances. Similarly the parameters of other components, such as the β values of transistors, will be correlated, especially when they are in close proximity. Such correlations must be characterized and taken into account when performing statistical analysis of integrated circuits.

Tolerances in the lateral dimensions of integrated components also cause considerable variation in parameter values. Inaccuracies may result from errors in layout or cutting of master drawings and in the photographic reduction processes. Further, inaccuracies may occur in positioning masks with respect to previous patterns. In general, such surface dimension tolerances will tend to increase towards the edge of a circuit. The uncertainty in the definition of the edges may be reduced by making the sizes of the components larger.

Generally the p.d.fs encountered in integrated circuits will be continuous and for many parameters will approach a Gaussian form. However, for several important situations, the distributions will be skewed. For example a major source of error in a resistor will be its path width, and the chance of it being too narrow would be about twice the chance of it being too wide. Also the value of resistance for a particular length and depth is inversely proportional to the width. Therefore a $\pm$ 50% tolerance in width would result in a tolerance on resistance values from +100% to -33% with a marked skew towards the higher resistance values.

To summarize this discussion, typical tolerances of integrated circuit components are given in table 1.1 /12, chapter 6/.

1.5 STATISTICAL DESIGN - SOME SCENARIOS

Although in this thesis we are largely concerned with algorithms for tolerance assignment and design centering, many

other instances of statistical design problems may be identified. Therefore in this section we briefly examine some design scenarios. We commence however, with some comments on our specific problem (i.e. tolerance assignment) and introduce geometrical interpretations which will be useful for further exposition.

1.5.1 TOLERANCE ASSIGNMENT AND DESIGN CENTERING

For discrete components, the parameter p.d.fs will be centered about the nominal value and be truncated at the tolerance limits. The region of variation in the input space may then be represented by a rectangle centered[α] about the nominal value (design center) with sides of length $2t_i$, where the t_i are the relevant tolerances. We illustrate this for a 2-dimensional case (K=2) in figure 1.9. Also shown are the two p.d.fs which in this case are taken to be, truncated Gaussian and uniform, for parameters p_1 and p_2 respectively. The region of acceptability, (defined in equation 1.9) is a mapping in the input space of the performance specifications defined in the output space. Consider figure 1.10(a) where both the tolerance region R_T and the region of acceptability R_A are represented. Initially, assume both parameters to be uniformly distributed. Then yield will be the ratio of the volume (area for K=2) of region $(R_T \cap R_A)$ to the volume of region R_T. In the illustration of figure 1.10(a) this ratio is less than unity.

[α] In the case of skewed p.d.f., the nominal value may by definition be taken to be the mid point between the tolerance limits.

To increase the yield the designer may keep the size of the tolerance region fixed and increase the overlap between the two regions. This may be achieved by choosing the nominal values such that the tolerance region is more centrally placed inside the region of acceptability as illustrated in figure 1.10(b). Hence, this process is called design centering. Alternately the designer may accept the nominal value and decrease tolerances, and therefore reduce the size of the tolerance region. This latter procedure is called tolerance assignment. Figures 1.10(b) and 1.10(c) illustrate application of these two alternatives to the situation of figure 1.10(a). Tighter tolerances imply better grade and therefore more expensive components. Therefore, the designer may invoke a combination of both procedures to obtain a suitable trade-off between component costs and the cost of discarding or repairing failed circuits.

For the situation where all the parameters are not independent and uniformly distributed, the relevant p.d.f. $\phi(P)$ will define a weighting of every point in R_T. The yield will then be a ratio of weighted volumes. A similar geometrical interpretation of tolerance assignment and design centering may also be considered in this situation.

In the manufacture of integrated circuits, individual components cannot be sorted and therefore tolerances cannot be placed upon individual parameters. For many parameters, tolerances determined by the manufacturing process have to be accepted and the designer may then attempt to maximize yield by re-assigning nominal values. However, for other components,

for example resistors, tolerances on parameter values are determined by the chip area occupied by the component. The larger the area, the smaller the tolerance. However, larger component sizes increase the overall area occupied by the circuit. This increases the cost of processing the circuit and may result in a greater incidence of catastrophic faults. Here again a higher cost is associated with tighter tolerances. Therefore both tolerance assignment and design centering procedures are of relevance to integrated circuits.

1.5.2 CHOICE OF PERFORMANCE SPECIFICATIONS

(a) Specification Sensitivity

In the discussion so far it has been assumed that the specifications on performance (expression 1.7) are invariant and the engineer has to design for component value statistical spreads with respect to these specifications. However, the designer may find response spreads are such that even after tolerance assignment and design centering, the resulting circuits are still too expensive to manufacture. The designer may then explore the effect on yield of altering various specifications to consider possible trade-offs between different specifications. It may be possible to offer to the customer, circuits which are appreciably cheaper, but have specifications more commensurate with performance spreads achievable with available component spreads. The performance requirements are often somewhat arbitrary and there is usually the possibility of suitable trade-off of different specifications.

The sensitivity of yield to different performance specifications may be explored using Monte Carlo analysis. Associated with each of the N sample circuits is a number m of values for the performance functions. Overall yield is estimated as the proportion of the N analysed circuits which simultaneously meet all performance specifications. Similarly the partial yields (introduced in section 1.3.2) for each performance may be estimated as the fraction which meets that particular performance specification. The effect of relaxing or tightening specifications may then be explored by changing performance specifications and re-calculating overall and partial yields.

(b) System Specification

The discussion so far has been concerned with the problems of designing circuits in the presence of uncertainty in component parameter values. However, the concepts and methods (specifically Monte Carlo analysis) may be extended to certain aspects of system[α] specification. System specification consists firstly of a functional specification, i.e. a specification of the functions to be performed by each of the subsystems, and the nominal values expected of their response.

Secondly, it involves a specification of the allowed range of variation of response in each subsystem. The specification of allowed variations in subsystem response calls for a

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[α]Although a circuit may always be considered a system, here we take system to be, entities such as F.D.M. communication systems, digital transmission systems etc.

knowledge of the effects on the overall system performance of deviation from nominal of each of the subsystem performances. Computing the effects on the overall system performance deviations, taking the system responses one at a time would not be valid in the presence of non-linearities. Monte Carlo analysis can be very effective in studying overall system behaviour when the performance of the subsystems deviates from nominal. An initial study would assume a hypothetical p.d.f., for example multivariate uniform, to represent variation of subsystem response. Monte Carlo analysis could then be performed as summarized in the block diagram in figure 1.3, where the block labelled circuit simulator may now be replaced by a system simulator.

Such a study would provide the designer with information as to how subsystem performances combine and what maximum and minimum system degradation may be expected from subsystem degradation. The designer would be interested in specifying the largest allowable subsystem degradation such that overall system performance were still acceptable. More generally, a trade-off between different subsystem performance specifications may be considered. An example of such a study for a waveguide transmission system is reported in reference /14/, where the subsystems may comprise equalizers, detectors, regenerators etc. The system designer would be required to specify allowable deviations such as delay, amplitude distortion, error rate etc, in the subsystems.

1.5.3. SPECIFICATION OF MANUFACTURING TESTS

The engineer may study a wide variety of circuit properties for evaluation and improvement during the design stage. However, it is desirable for economic reasons, to keep the number of tests performed on manufactured circuits to a minimum. In addition certain test may be substantially more expensive than others. For example, for linear integrated circuits, testing for d.c. properties is much cheaper than a.c. testing /15/. Therefore the specification of manufacturing tests is an important part of design. The methods of statistical analysis are very useful to study circuit behaviour from the point of view of specifying a suitable testing strategy while minimizing cost. In this section we describe a number of scenarios from this area.

(a) Go-No Go Testing

This represents the simplest case where statistical analysis may be employed to specify testing procedures. Consider the situation where the manufactured circuit is required to meet a certain number of performance specifications. Every manufactured circuit is to be tested sequentially for compliance with each performance specification. A circuit failing any one test is to be discarded or repaired. A Monte Carlo analysis performed with the expected input p.d.f.s would then give an indication of the performance functions where circuits are most likely to fail and of the likely correlations between failures at different specifications. An order of testing could then be estabilished to minimize overall cost of testing.

(b) Accounting For Environmental Effects In Factory Testing

Manufactured circuits have to function in environmental conditions (e.g. temperature, humidity etc) subject to uncertainty. These factors, in addition to component ageing, cause input parameters to drift from their values at the time of manufacture. Further, this drift is reflected in circuit performance while in service. Generally it is not feasible to physically simulate these effects upon manufactured circuits while testing in the factory. Therefore, to allow for degradation of behaviour while in service, circuits have to be tested to specifications more stringent than required for acceptability. A Monte Carlo analysis may easily be modified to simulate such environmental effects. This would require knowledge of the dependence of component parameter values upon environmental parameters. The additional performance degradation due to environmental effects could be estimated and the factory test limits set accordingly.

(c) Selection Of Testing Accuracy

In most situations testing procedures with greater attendant accuracy will incur a greater cost. A Monte Carlo analysis may be employed to select test accuracy and strategy to reduce overall testing costs. For illustration consider the hypothetical example of figure 1.11. A Monte Carlo analysis is employed to obtain a histogram (not depicted in the diagram) of the expected distribution of a particular performance function f_i. The accuracy of a particular test may be represented by an interval of uncertainty and a hypothetical distribution of errors. We may consider a

strategy where two test procedures are to be employed. This may comprise a crude test for performance values in the middle of the allowed range, and a more precise test for values near the limits of the allowed range. For particular choices of accuracy of the two tests, the results of the Monte Carlo analysis may be employed to estimate the proportion of manufactured circuits for which either test will be required. Hence, overall testing costs may be estimated. Indeed the results of the Monte Carlo analysis may be used to specify the accuracy of the two tests, such that overall testing costs are minimized.

1.6 SUMMARY

This chapter is a general review of the field of statistical design. Some useful notation and terminology is introduced and explained. The two most widely used methods of statistical analysis, viz. Monte Carlo analysis and the Method of Moments are briefly described. Brief comments on the type of distributions encountered in discrete and integrated circuit components are given.

In addition to tolerance assignment and design centering some other problems in the field of statistical design are described. These include the specification of performance constraints in manufactured circuits; the specification of sub-system performance constraints in system design; and various problems related to the specification of performance tests on manufactured circuits. The possible use of Monte Carlo analysis for such problems is emphasised.

Element	Symbol	Typical value	Tolerance normal/ narrow linewidth		Temperature Coefficient
General					
Sheet resistance of base diffusion	R_s	150Ω/	±10%		+0.2% /°C
Sheet resistance of emitter diffusion	R_s	2.5Ω/	±30%		+0.01%/°C
Sheet resistance of epitaxial layer	R_s	200Ω/	±15%		+0.2% /°C
Sheet resistance of deposited resistance layer	R	50-1000 Ω/	±5%		0.01%/°C
Transistors					
Current amplification factor	β	50	+50% -30%		+0.5%/°C
Matching of β between identical transistors in close proximity	Δβ	-	±10%		±0.0005% /°C
Resistors					
Resistance of diffused resistors	R	-	±25%	+100% - 50%	+0.2% /°C
Resistance of deposited resistors	R	-	±8%	+30% -20%	+0.01%/°C
Matching between identical resistors in close proximity	ΔR	-	±3%	±8%	±0.0005%/°C
Capacitors					
Capacitance of diffused capacitors	C	-	±25%	+100% -50%	-
Capacitance of deposited capacitors	C	-	±20%	+80% 40%	-
Matching of identical capacitors in close proximity	ΔC	-	±3%	±8%	-
Junction FET					
Transconductance	g_m	-	±50%		-0.2%/°C
Pinch-off voltage	V_p	-	±30%		-0.5%/°C
IGFET					
Transconductance	g_m	-	±50%		±0.1%/°C
Threshold voltage	V_T	-	±50%		-

Table 1.1 Typical Tolerances And Temperature Coefficients Of Component Parameters In Integrated Circuits.

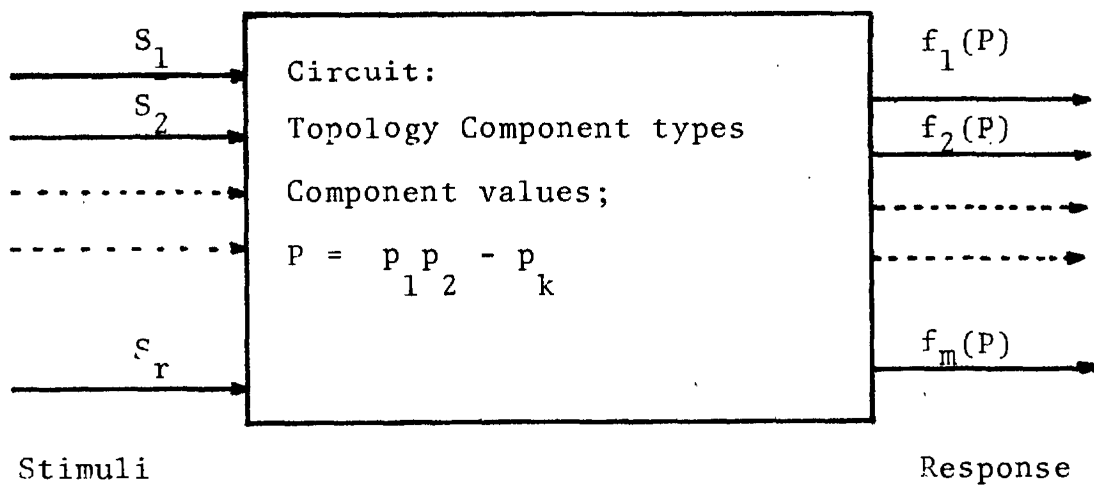


Figure 1.1 A General Circuit Representation

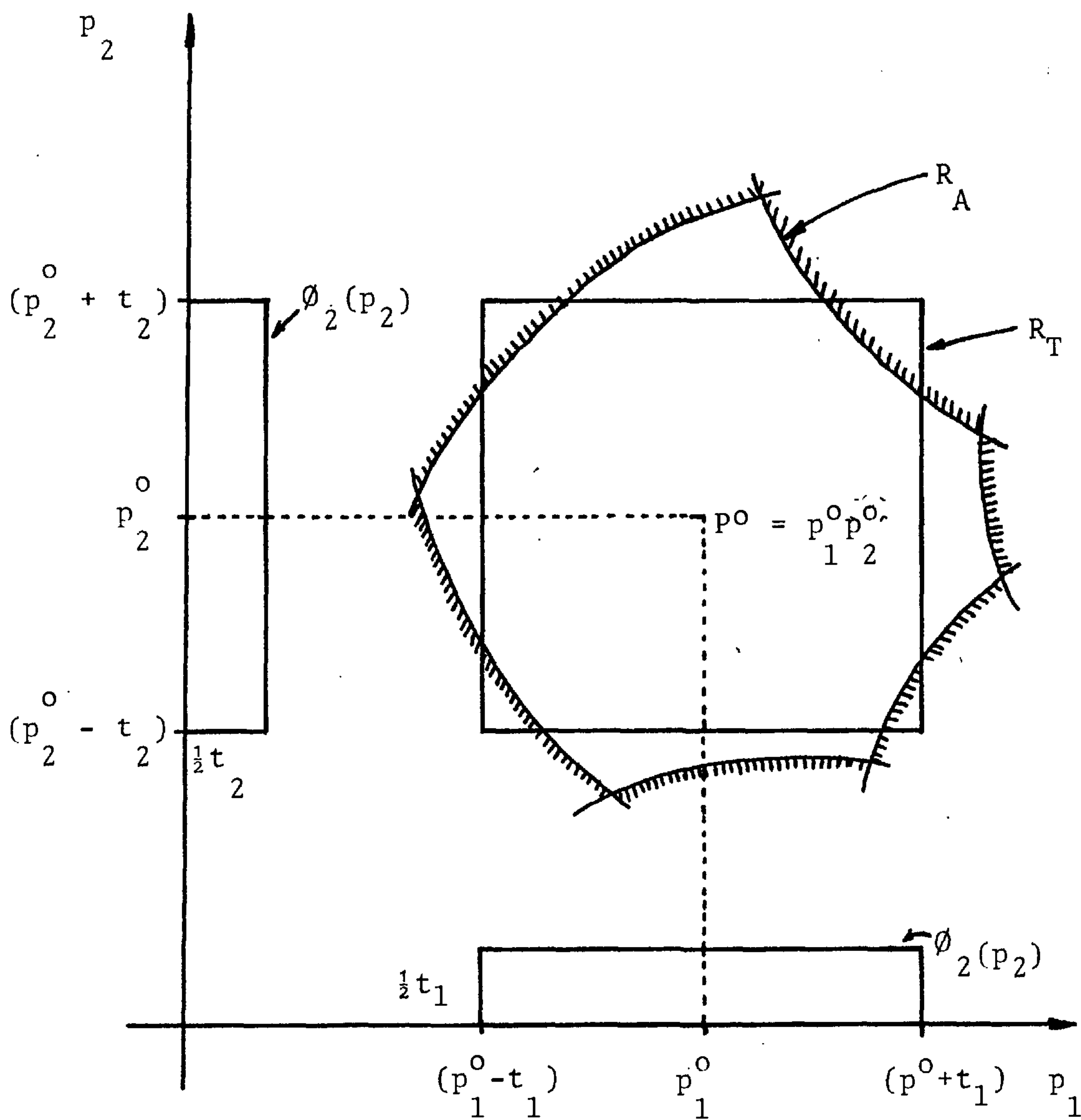


Figure 1.2 An illustration of some notation

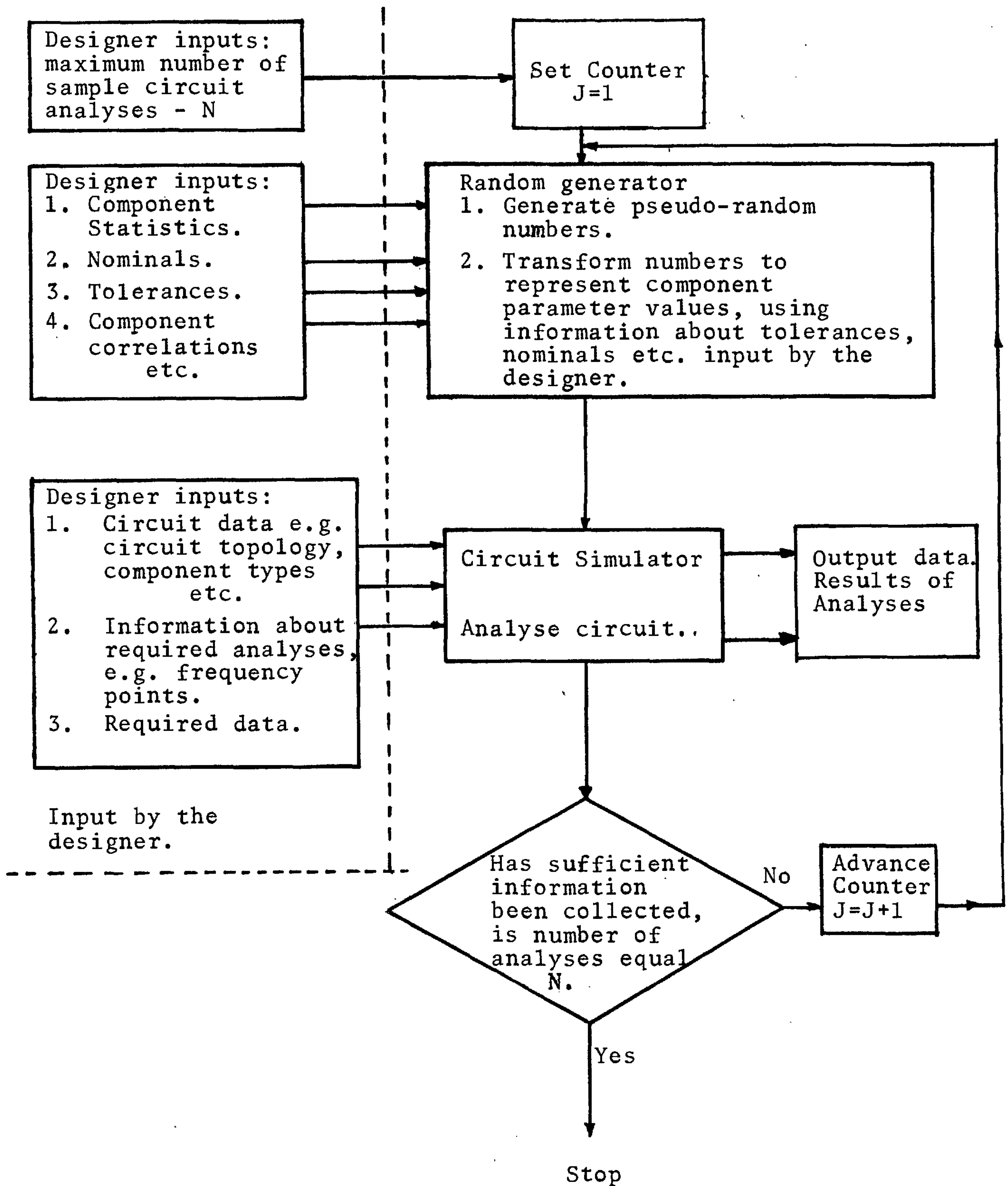


Figure 1.3 : Monte Carlo Analysis - A General Flow Chart.

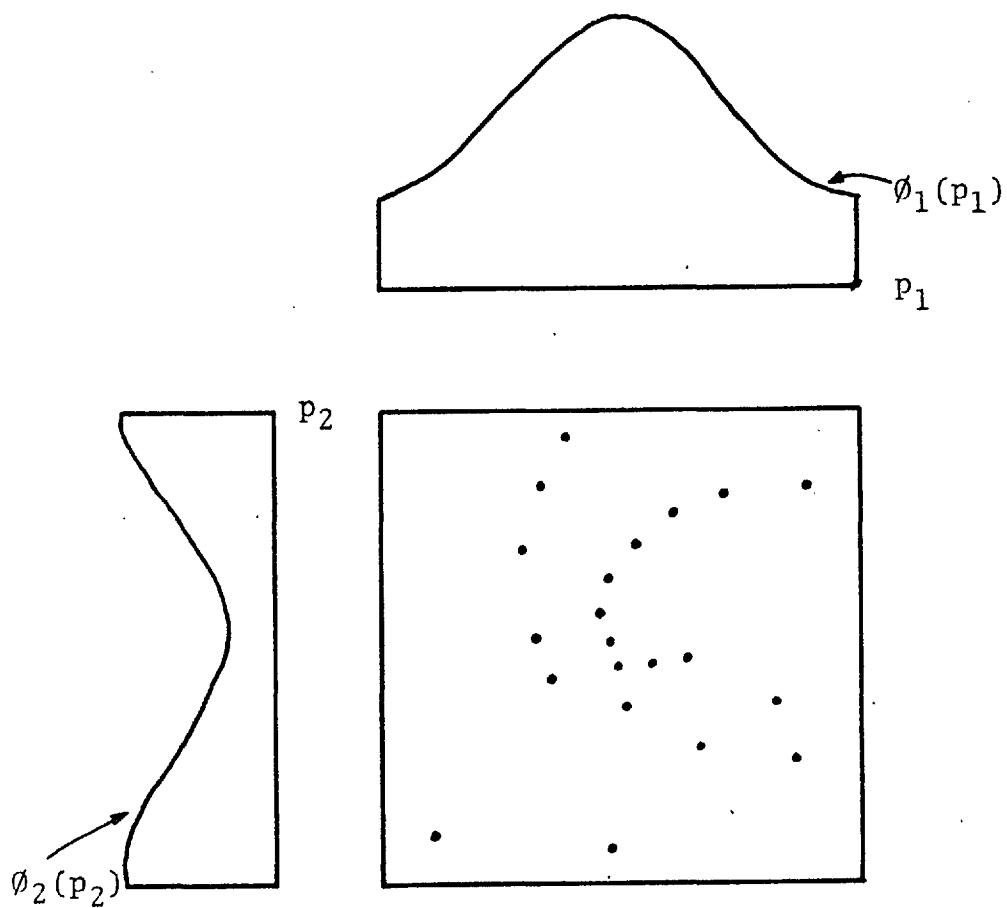


Figure 1.4 Typical set of Monte Carlo samples (points) generated by a pseudo random process.

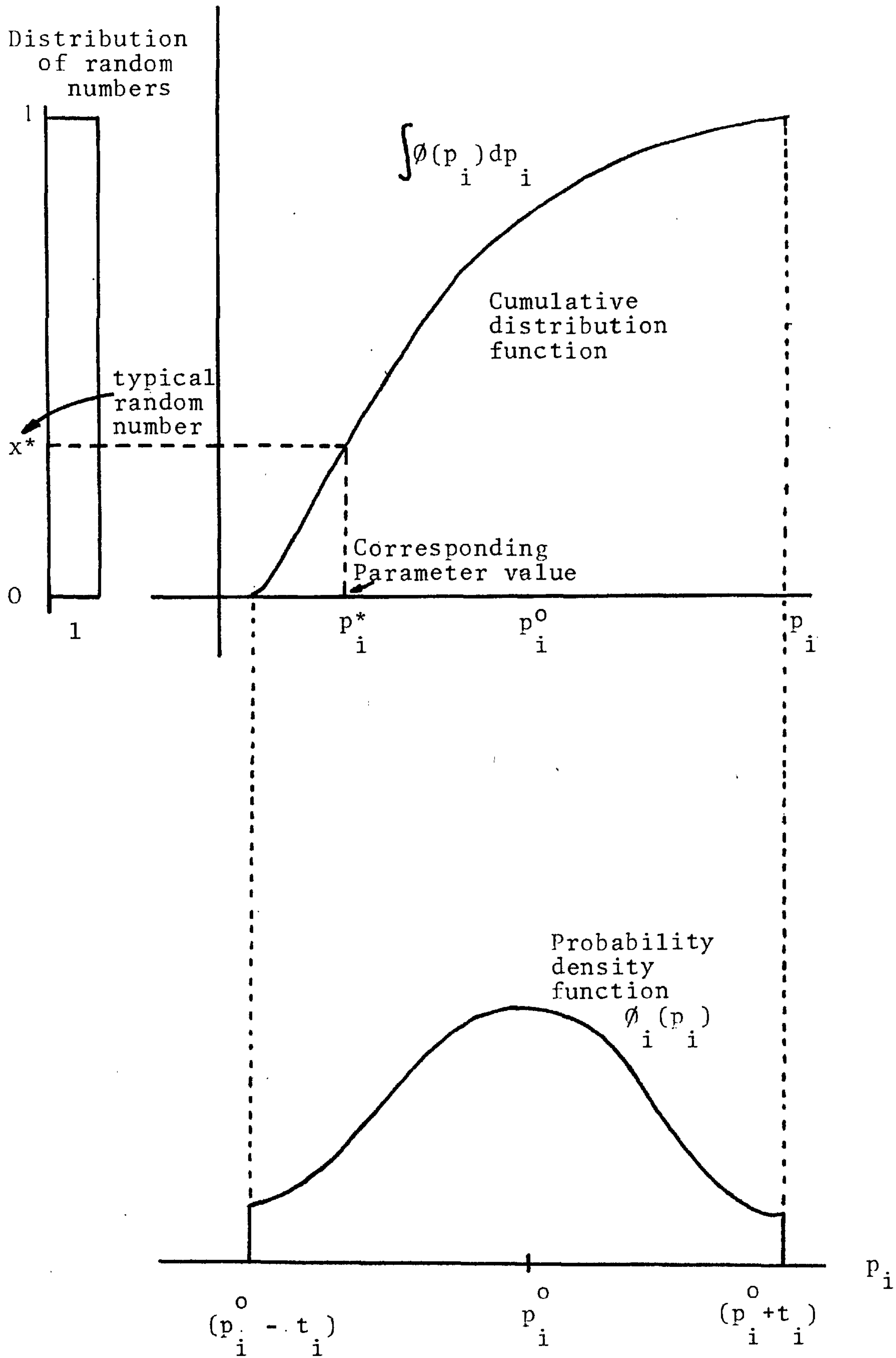
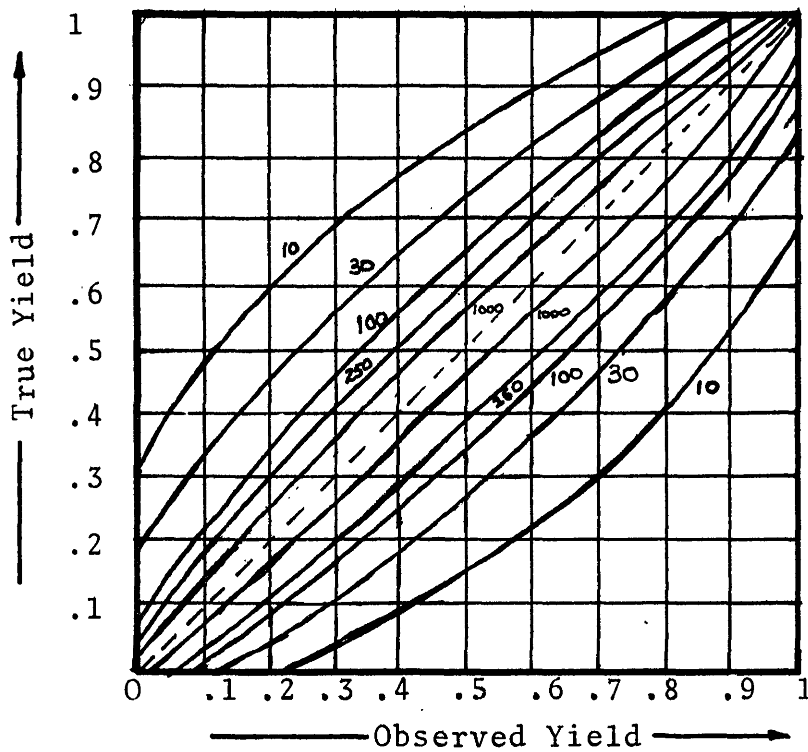


Figure 1.5 Illustrating A Method For Generating Component Parameter Values From random numbers Distributed In The Interval 0 to 1.



Note : These Curves Correspond To The Case When ε=2 And The Confidence Level Is 95%. For Example, The 95% Confidence Interval For An Observed Yield Of 60%, Based On A Sample Size Of 100, Is ~ 50% To 70%./12, Chapter 5 ,Page 131/

Figure 1.6 : The Relationship Between The Number Of Samples And The Accuracy Of The Yield Estimate , In Monte Carlo Analysis

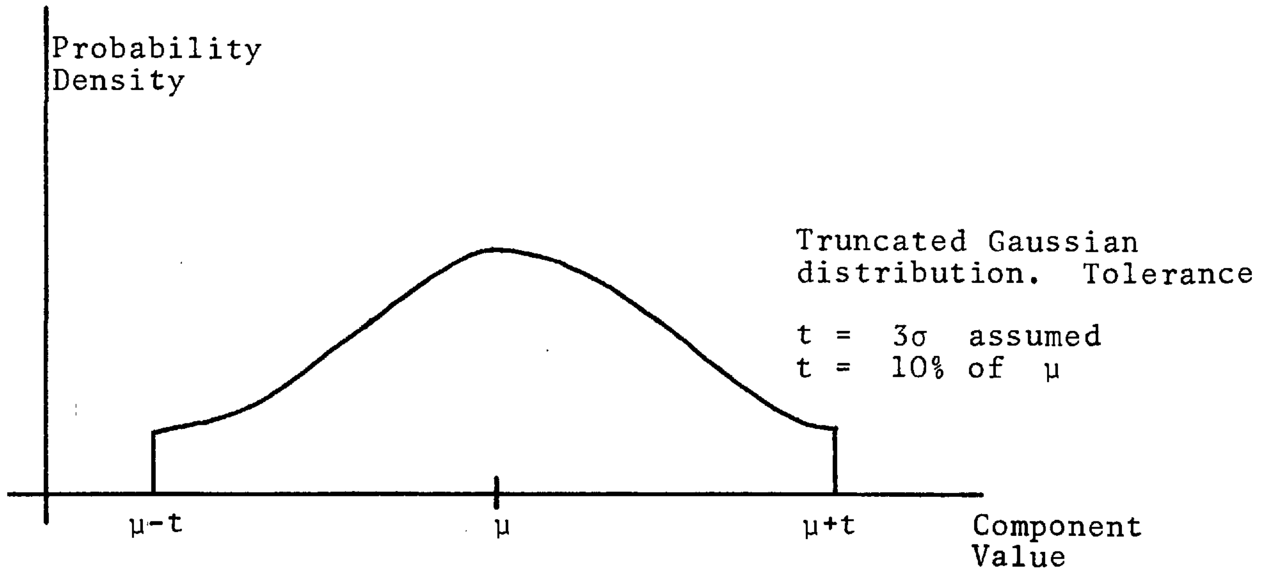


Figure 1.7(a)

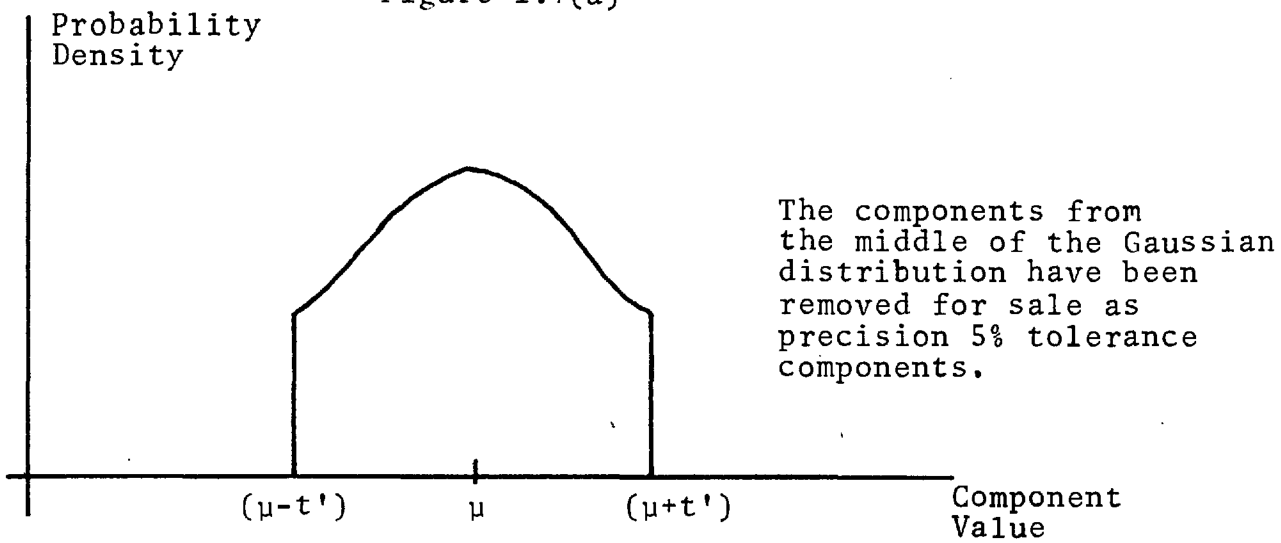


Figure 1.7(b)

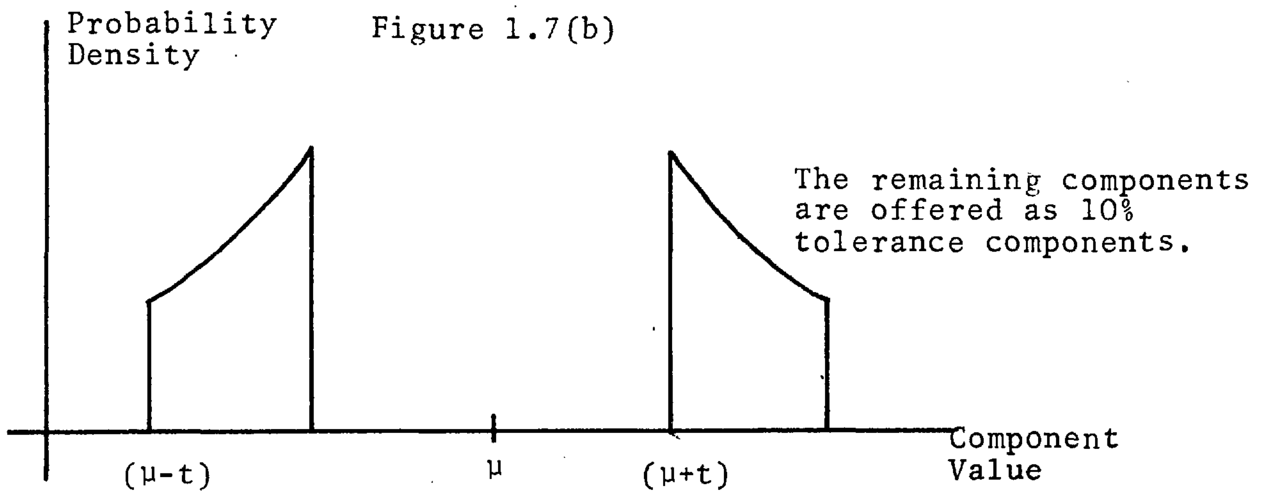


Figure 1.7(c)

Figure 1.7 Typical Probability Density Functions Encountered with discrete components.

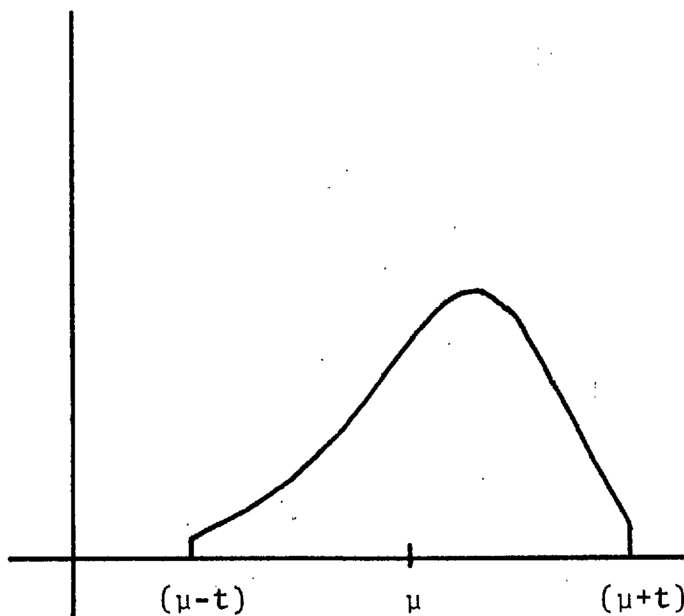


Figure 1.8 A Skewed Component p.d.f.

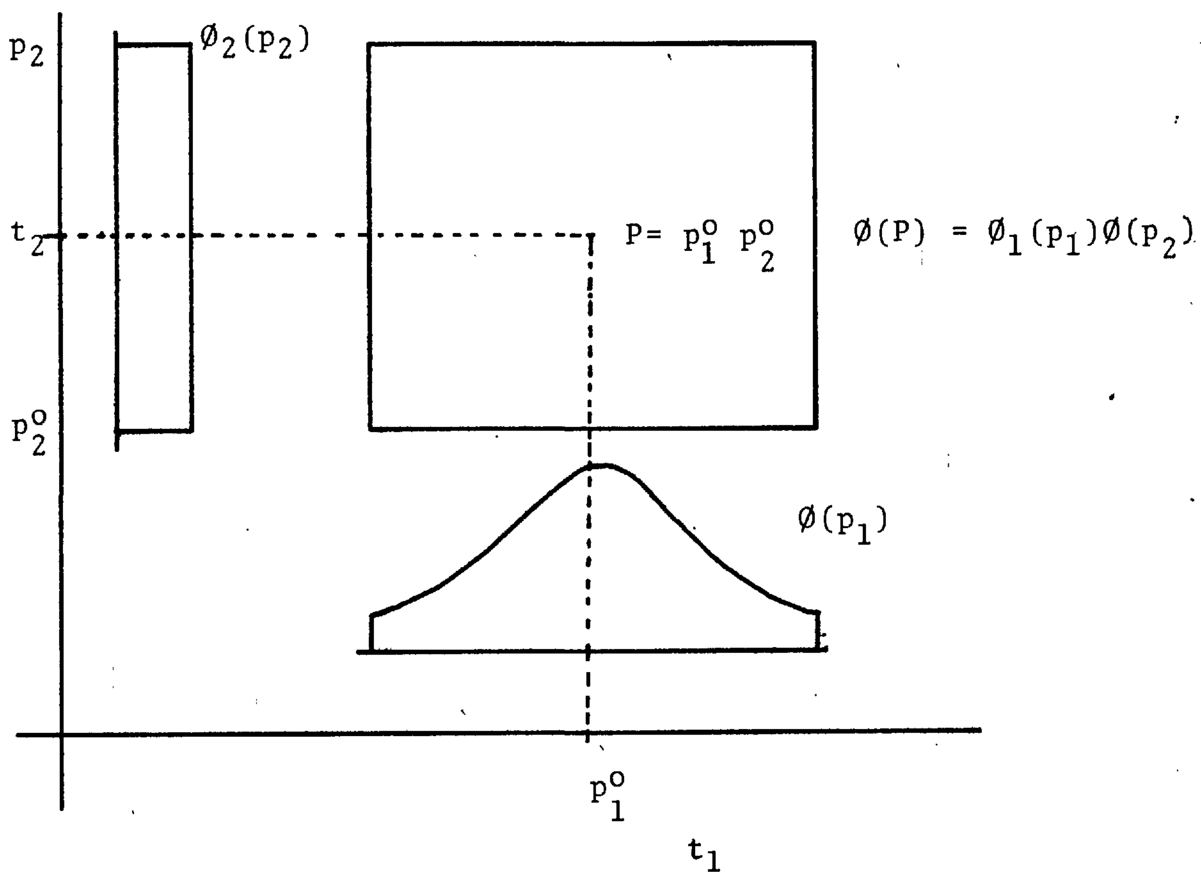


Figure 1.9 Illustration Of The Terms Design Center And Tolerance.

Figure 1.10(a)
Illustration
Of Accept-
ability and
tolerance.

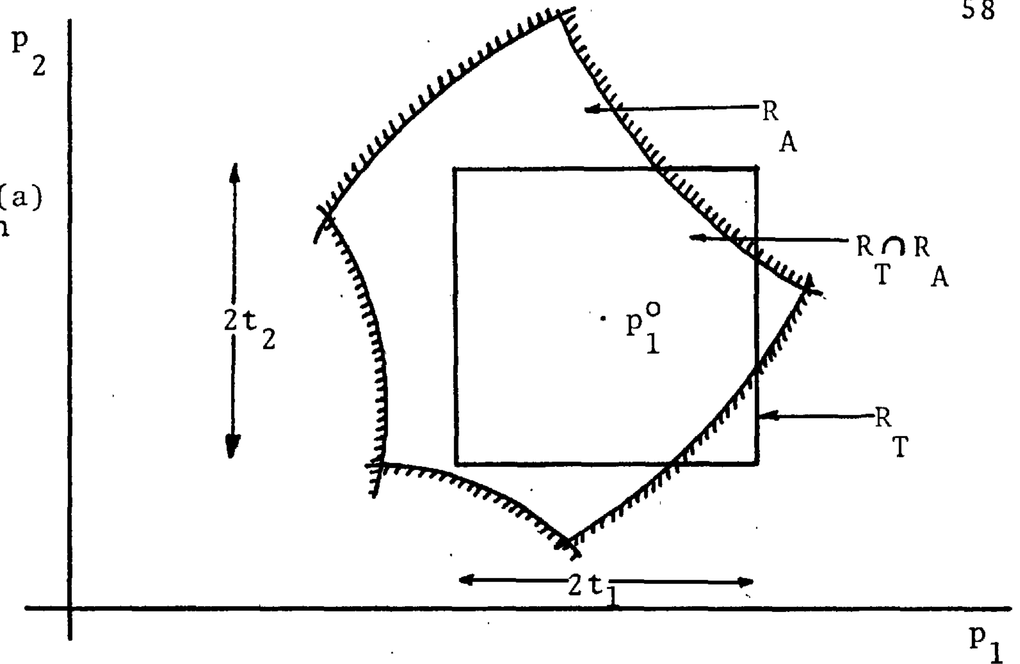


Figure 1.10(b)
Design
Centering
Original
Tolerances, new
Nominal Point.

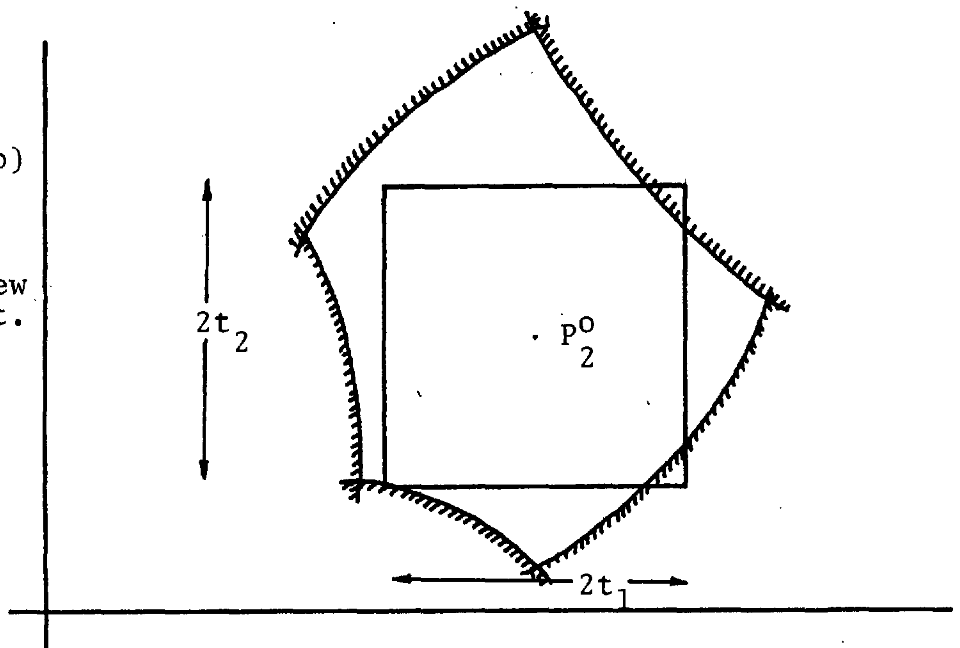


Figure 1.10(c)
Tolerance
Assignment
Original
Nominal Point,
New Tolerances.

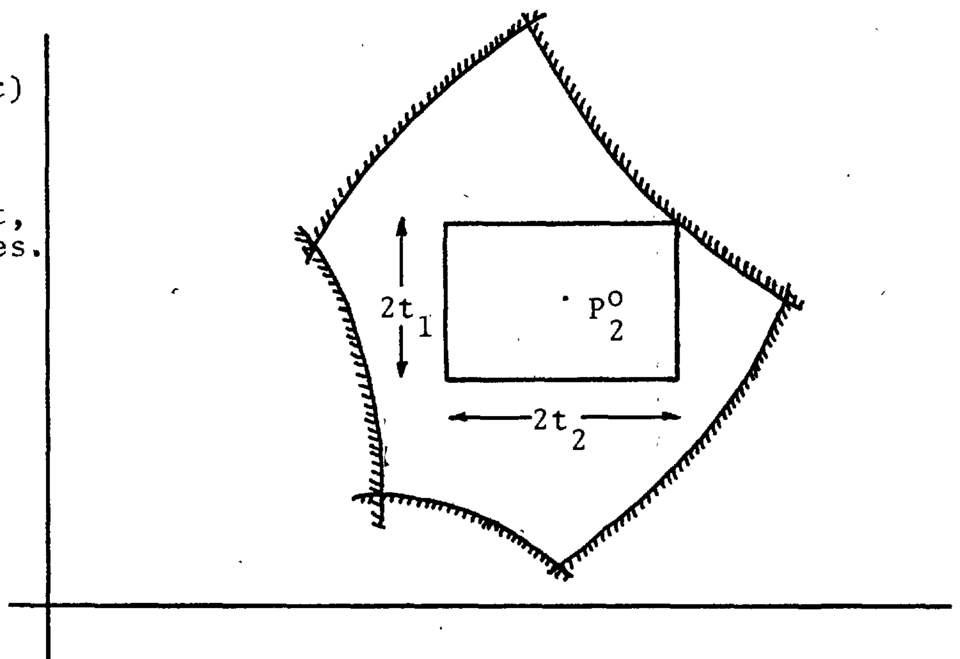


Figure 1.10 Geometrical Interpretation of Design Centering And Tolerance Assignment.

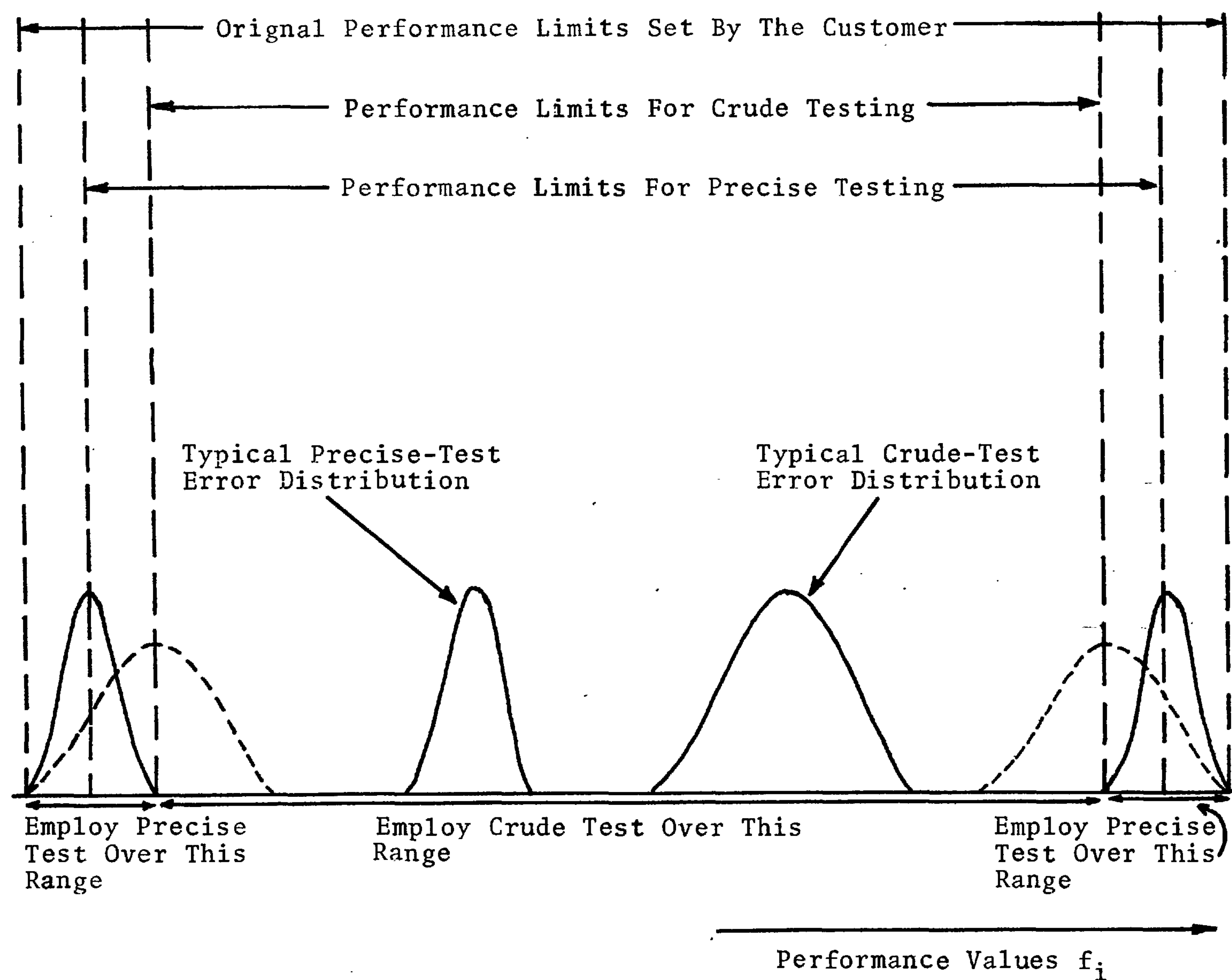


Figure 1.11: Illustrating The Application Of Statistical Design To The Problem Of Selecting Testing Accuracy.

CHAPTER 2 - ALGORITHMS FOR TOLERANCE ASSIGNMENT AND DESIGN CENTERING - A CRITICAL REVIEW

2.1 Introduction.

2.2 Cost models.

2.2.1 Component cost functions.

2.2.2 The unit cost function.

2.3 Problem formulations.

2.3.1 Problem P1: Composite tolerance assignment and design centering.

2.3.2 Problem P2: Worst case tolerance assignment and design centering.

2.3.3 Problem P3: Worst case tolerance assignment.

2.3.4 Problem P4: Statistical tolerance assignment and design centering.

2.3.5 Problem P5: Statistical tolerance assignment.

2.3.6 Problem P6: Design Centering (Yield Maximization)

2.3.7 Problem P7: Tolerance assignement, design centering, and tuning.

2.4 The Review.

2.4.1 Methods based on geometrical characterization.

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(a) Worst case formulation.

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2.4.3 Methods based on Monte Carlo analysis.

2.4.4 Discrete methods.

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CHAPTER 2

ALOGRITHMS FOR TOLERANCE ASSIGNMENT AND DESIGN CENTERING - A CRITICAL REVIEW

2.1 INTRODUCTION

As discussed in the previous chapter, statistical distribution of component parameter values may cause some of the manufactured circuits to fail to meet performance requirements at the time of manufacture. That is, the manufacturing yield may be less than 100%. Clearly there is an inter-dependence between component tolerances and manufacturing yield. In general tightening tolerances will lead to higher yields. However, tighter tolerance components are more expensive and increase the overall cost of producing the circuit. On the other hand for yield less than 100% failed circuits have to be discarded or repaired, and this too leads to increased costs. Hence a compromise between tighter tolerance and higher yield may be sought. A procedure for effecting such a compromise is termed tolerance assignment.

In the manufacture of some types of circuits, expecially integrated circuits, it may not be possible to impose tolerances on the component parameters. This is unlike the case for discrete circuits, where a stipulated tolerance may be imposed on a particular batch of a component. To do this, the component manufacturer simply removes from the batch those components whose value falls outside the

tolerance limits he wishes to choose. For integrated circuits, the designer usually has to accept parameter tolerances determined by the physical process employed to fabricate the components, and to try and increase yield by changing the nominal values of the component parameters. This latter procedure is called design centering, and a particular set of nominal parameter values is called a design center. In the case of discrete circuits, design centering and tolerance assignment procedures may be combined to give even more cost effective circuit solutions.

In both design centering and tolerance assignment, the designer seeks to minimize those circuit costs which depend upon component tolerances and circuit yield. We therefore commence this chapter with a discussion of appropriate cost models. This is then followed by various problem formulations which may be appropriate in different circuit applications. In the latter part of this chapter, various proposed solution techniques are reviewed. This review is by intention not exhaustive; nevertheless, different general strategies are identified and their attributes illustrated by a discussion of one or two representative alogrithms. Thus the advantages and shortcomings of each category of solution technique are highlighted. Finally, conclusions are drawn as to the best area for the development of more effective methods.

2.2 COST MODELS

The total cost of manufacturing an electrical circuit will depend upon a large variety of factors. Of concern to the engineer are costs of purchase of components, the cost of circuit assembly or fabrication and of testing, repairing or tuning. The cost models discussed here will be derived by considering (a) tolerance dependent component costs and (b) the cost of repairing or discarding correctly assembled or fabricated circuits, whose performance fails to meet requirements as a result of variation of parameter values within allowed tolerances.

2.2.1 COMPONENT COST FUNCTIONS

These relate specifically to circuits employing discrete components. Let $C_i(t_i)$ denote the cost function of the ith component whose fractional tolerance is t_i. Then if C_C represents the total component cost of the circuit, we may write:

$$C_C = \sum_{i=1}^{K} C_i(t_i) \qquad 2.1$$

In every case the function $C_i(\cdot)$ will be a monotonically decreasing function of tolerance t_i. The individual $C_i(\cdot)$ may take on various forms, typically:

$$C_i(t_i) = a_i + b_i/t_i^{\ell_i} \qquad 2.2$$

and

$$C_i(t_i) = f_i + d_i \log t_i \qquad 2.3$$

The constants a_i and f_i represent the fixed costs i.e. the basic material and labour cost of making the component.

The constants b_i and d_i reflect the weighting, relative to other components in the circuit, of that component. The constant ℓ_i in 2.2 is a measure of the rate at which the cost approaches a minimum (typically ℓ_i is unity) /17/. A typical cost versus tolerance curve is depicted in figure 2.1.

2.2.2 THE UNIT COST FUNCTION

The unit cost function expresses the average cost of producing one acceptable circuit. Two functions will be derived. Firstly, we will assume a strategy where correctly assembled circuits which fail to meet performance requirements are discarded, and secondly a strategy where failing circuits are repaired by replacement of all the components. Obviously, the latter strategy can only be applied to the manufacture of discrete component circuits.

Assuming that a total number N of circuits is to be manufactured then a yield Y implies that NY of the N circuits will on average be acceptable. Therefore, the total cost of producing N circuits is

$$C_T = N(C_A + \sum_{i=1}^{K} C_i(t_i)) \qquad 2.4$$

C_A embodies the fixed, tolerance independant costs of producing each circuit. For example the cost of printed circuit boards, labour cost, costs of testing, etc. Now if failing circuits are to be discarded, then the average cost per acceptable circuit is:

$$C_U = \frac{C_T}{NY} = \frac{C_A + \sum_{i=1}^{K} C_i(t_i)}{Y} \qquad 2.5$$

In an alternative strategy each of the failing circuits is repaired by replacing all the components with a different set, selected at random as before. Let us assume that this is continued until practically all the circuits have been made to meet the performance requirements. If we let C_R represent the cost of repairing each failing circuit, then the total cost of ensuring that practically all the circuits are acceptable will be the following sum

$$\begin{aligned} C_T &= N(C_A+C_C)+N(1-Y)C_R+N(1-Y)^2C_R+\ldots\ldots\ldots \\ &= N\{C_A + C_C+C_R(\sum_{i=1}^{K}(1-Y)^i)\} \\ &= N\{C_A+C_C+C_R(\frac{1-Y}{Y})\} \end{aligned} \qquad 2.6$$

As before C_A is the fixed cost and C_C the sum of the tolerance dependent component costs. Therefore, the cost per acceptable circuit for this second strategy will be:

$$C_{UR} = C_A+C_C + C_R(\frac{1-Y}{Y}) \qquad 2.7$$

The relative merits of the two strategies may now be compared. Clearly, the throwaway strategy is less expensive if:

$$C_A+C_C<C_R \qquad 2.8$$

That is to say it is cheaper to discard failing circuits if the cost of repairing a circuit, exceeds the sum of the fixed and component costs.

2.3 PROBLEM FORMULATIONS

This section presents various problem formulations of design centering and tolerance assignment, based on the cost functions discussed previously. Only the throw away strategy will be considered, although similar formulations may be obtained for the repair strategy.

2.3.1. PROBLEM P1: COMPOSITE TOLERANCE ASSIGNMENT AND DESIGN CENTERING

P1: Minimize

$$C = \frac{C_A + \sum_{i=1}^{K} C_i(t_i)}{Y(P^o, T)} \qquad 2.9$$

by appropriate choice of P^o and T. Reiterating, $P^o = p_1^o \ldots\ldots p_K^o$ is the vector of nominal component values and $T = t_1 \ldots\ldots t_K$ the vector of relative tolerances. The yield $Y(\cdot)$ depends upon the joint probability density function $\emptyset(\cdot)$ of the component parameters. In practice a particular form of p.d.f. is assumed for $\emptyset(\cdot)$ and the parameter P^o and T regarded as indices for $\emptyset(\cdot)$. For example $\emptyset(.)$ may be multi-variate Gaussian, truncated at the 3σ points. So that p_i^o would be the mean of the ith component and t_i, its tolerance would be related to the standard deviation as $t_i = 3\sigma_i$. Therefore in this notation yield may be written as a function of P^o and T for stipulated form of p.d.f.

P1 as stated in 2.9 is an unconstrained optimization problem. This formulation will only be relevant to discrete component circuits. However, in such circumstances, the designer may only be allowed tolerance values

from a discrete set, i.e.

$$t_i \varepsilon t_{i1}\ t_{i2}\ \ldots\ldots\ldots\ t_{ij}\ ,\ j=1\ \ldots \ell_i;\ i=1\ \ldots\ldots\ K \qquad 2.10$$

Where ℓ_i is the number of available discrete tolerance values for the ith component. In addition the parameter nominals may also only be allowed a discrete set of values. For example the jth component may be a resistor whose nominal value would have to be from a preferred range, i.e.

$$p^o_j \varepsilon\ p^o_{i1}\ p^o_{i2}\ \ldots\ldots\ldots\ p^o_{ij}\ ;\ j=1\ \ldots n_i\ ;\ i=1\ \ldots\ K \qquad 2.11$$

Further the denominator in 2.9, the yield, is a multi-dimensional integral. Therefore, it is impractical to analytically compute either the cost function (2.9), or its gradients with respect to the design parameters P^o and T. Hence, standard methods of non-linear programming cannot easily be applied to (2.9). To make the problem more tractable, various authors have considered alternative formulation by modifying the cost function as follows.

2.3.2 PROBLEM P2: WORST CASE TOLERANCE ASSIGNMENT AND DESIGN CENTERING.

P2. Minimize

$$C = C_A + \sum_{i=1}^{K} C_i(t_i) \qquad 2.12$$

by appropriate choice of p^o_i, t_i; i=1 .... K

Under the constraint that yield is unity i.e.

$$Y(P^o,T) = 1 \qquad 2.13$$

The geometrical interpretation of 2.12 and 2.13 is given in figure 2.2. Basically, the tolerance rectangle $R_T(P^o,T)$ is to be placed inside the region of acceptability R_A

by choosing P^o and T, such that $R_T(P^o,T)$ is wholly contained in R_A; i.e. $R_T(P^o,T) \subseteq R_A$ and cost is minimized.

2.3.3 PROBLEM P3: WORST CASE TOLERANCE ASSIGNMENT

P3: Minimize $$C = C_A + \sum_{i=1}^{K} C_i(t_i) \qquad 2.14$$

by appropriate choice of t_i; i=1 .... K, for design center P^o_* and subject to the constraint that yield is unity. This formulation is more restrictive than P2, as it assumes a fixed nominal point. Geometrically it may be interpreted as: with tolerance rectangle centered about P^o_*, discover the largest tolerances t_i, for which the cost function (2.14) is minimized and the tolerance rectangle is wholly contained in R_A (see figure 2.2)

2.3.4 PROBLEM P4: STATISTICAL TOLERANCE ASSIGNMENT AND DESIGN CENTERING

In the formulations P4 and P5, we relax the constraint on yield, which is now required to be greater than a certain value Y_L.

P4: Minimize $$C_A + \sum_{i=1}^{K} C_i(t_i) \qquad 2.15$$

by appropriate choice of P^o and T, subject to the constraint that $$Y(P^o,T) > Y_L \qquad 2.16$$

The constant Y_L is a lower bound on the yield. This problem formulation is of importance, because in a particular class of solution technique the constraint on yield is first transformed to constraints on the design parameters P^o and T;

standard methods are then used to solve the resulting constrained non-linear programming problem.

2.3.5. PROBLEM P5: STATISTICAL TOLERANCE ASSIGNMENT

This may be defined as a variant of P4 when the design center is assumed fixed.

P5: Minimize $$C = C_A + \sum_{i=1}^{K} C_i(t_i) \qquad 2.17$$

by appropriate choice of t_i, i=1 ... K, for a fixed design center P^o_* subject to the constraint that:

$$Y(T) > Y_L \qquad 2.18$$

2.3.6. PROBLEM 6: DESIGN CENTERING (YIELD MAXIMIZATION)

P6: Maximize $Y(\emptyset(P^o))$ 2.19

by appropriate choice of design center P^o.
This particular formulation is of especial interest in the design of integrated circuits. Here, the designer has to accept tolerances determined by the uncertainties of the manufacturing process and to try and maximize yield by changing nominal component values. The procedure is also useful as a prelude to tolerance assignment for discrete circuits. For fixed tolerances, cost is a monotonically decreasing function of yield, therefore no cost function need be formulated explicitly in terms of the yield.

2.3.7 PROBLEM P7: TOLERANCE ASSIGNMENT, DESIGN CENTERING AND TUNING

In many circuits of high complexity, it may not be possible to obtain satisfactory performance of manufactured circuits, using components with available tolerances. It may then

be necessary to tune (adjust) some of the component parameters after circuit manufacture, until performance requirements are met. Two examples of tuning are the adjustment of a slug in a pot core inductor and the laser triming of thin film resistors. In general we require a procedure for selecting a subset (of size K' say) of the K relevant component parameters, such that by adjustment of components from this subset, the deviation of performance beyond specified limits may be compensated for in some or all of the manufactured circuits. It may not be possible to formulate a suitable cost function which satisfactorily reflects the costs of making adjustments and the added costs of tunable components. We may however, consider simpler problem formulations, such as the worst-case design centering, tolerance assignment and tuning problem. The circuit is designed such that performance deviation in the manufactured circuits can always be compensated by adjusting the tunable components. The problem then reduces to ;

P7: Minimize $$C = C_A + \sum_{i=1}^{(K-K')} C_i(t_i) \qquad 2.20$$

by appropriate choice of nominals and tolerances for the (K-K') non tunable components; subject to the constraint that yield is unity, after adjustment of the K' tunable components. The formulation is investigated by Bandler et al /17/. The additional problem of selecting the most effective component parameters as candidates for tuning is investigated by Glesner /18/ and will not be treated in this thesis.

2.4 THE REVIEW

The numerous proposed schemes addressed to the design centering and tolerance assigment problems may be classified according to various criteria. For the purpose of this review, the classification employed is based on the type of solution technique used. Four classes are identified, viz. geometrical characterization, standard non-linear programming, iterative Monte Carlo and discrete methods.

Algorithms are often divided into worst case, i.e. those that require yield to be constrained to unity, and statistical i.e. those that allow yield to take on a value less than unity. This latter classification relates to the problem formulation and not the solution technique. For instance standard non linear programming techniques have been reported /19,20/ for both worst case and statistical formulations.

2.4.1. METHODS BASED ON GEOMETRICAL CHARACTERIZATION

Geometrical interpretations may be associated with the various problem formulations. However, it is prohibitively expensive to compute the boundary ∂R_A of the region of acceptability R_A for circuit examples involving more than a few variables.

Director and Hachtel /21/ have demonstrated a scheme, where ∂R_A is approximated by a simplex /22, chapter 6/ of bounding hyper planes. For a K-dimensional example, the process commences with (K+1) hyper-planes, each of dimension (K-1). The planes are constructed by forming the convex hull of a number $M \geq K+1$ of points on ∂R_A. These initial points are

obtained by performing a series of unidimensional line searches parallel to the co-ordinate axes, emanating from the initial nominal point (design center). The simplicial approximation is improved iteratively. A new point on ∂R_A is obtained by searching along the outward normal from the center of the largest bounding hyper-plane of the current approximating simplex. The approximation is then improved by forming the convex hull of all previous points and the newly discovered boundary point. The process is illustrated for a two dimensional example in figure 2.3.

Such a characterization of ∂R_A considerably simplifies the design centering and tolerance assignment problems. For example, in one version of this method, the design centre is computed as the centre of the largest inscribable hypersphere (of dimension K) in the simplicial approximation. The computational effort is largely made up of circuit evaluations to determine points on the boundary ∂R_A. The procedures for determining the largest hyper-planes, for inscribing hyperspheres etc. may be formulated as standard problem in linear programming. However, the process can only work well for problems of small dimension, as the number of faces (bounding hyperplanes) required for a good approximation of R_A becomes very large with increasing dimensionality /53/. The procedure is largely addressed to the design centering problem (P7) applicable in the design of integrated circuits, where the design variables are process parameters such as sheet resistivities and specific capacitances. These parameters are normally fewer in number (typically less than 10) than the design variables

(resistances capacitances and inductances etc.) encountered in practical discrete component circuits.

Some of the dimensional dependence of the above method of simplicial approximation is reduced in the point basis approach /23/ where the approximating simplex is characterized in terms of the co-ordinates of a number $N > K+1$ points on ∂R_A. For a particular dimensionality, the point basis method, illustrated in figure 2.4 is reported to require a smaller number of circuit analyses than the face based method. Nevertheless, the effectiveness of such schemes has only been demonstrated for circuit examples involving a maximum of four toleranced components /24/.

An additional difficulty arises, since the approximating simplex will only be interior to R_A if R_A is convex. This assumption may not hold in general and hence can cause difficulty.

2.4.2 METHODS BASED ON NON-LINEAR PROGRAMMING

The methods considered in this section minimize cost functions which depend explicitly on component tolerances. Whereas both the design center and associated tolerances may be taken as design variables, yield is only introduced implicitly. Constraints are placed on yield, which are then transformed to constraints on the tolerances. Both worst case and statistical formulations are considered.

(a) WORST CASE FORMULATION

The problem formulation is as in P2 or P3. Re-iterating P3: Minimize

$$\sum_{i=1}^{K} C_i(t_i, p_i^o) \qquad 2.21$$

by appropriate choice of p_i^o and t_i; i=1 ... K, subject to the constraint

$$\text{Yield} = \text{Unity} \qquad 2.22$$

This formulation has been treated by Pinel and Roberts /25/, Sud and Spence /26/ and more extensively by Bandler et al /19,27/.

A yield of unity requires that the tolerance hyper-rectangle $R_T(P^o, T)$, (centered about P^o and of sides of length $2t_i$, $T = t_1 \ldots t_K$) be wholly contained in R_A; i.e.

$$R_T(P^o, T) \subseteq R_A \qquad 2.23$$

The condition 2.23 is given geometrical interpretation in figure 2.2. This condition entails an infinite number of constraints, since the infinity of points comprising R_T is required to belong to R_A. The problem is made more tractable by adopting either of two approaches.

(i) It is assumed that the worst value of a performance function occurs at one of the vertices of R_T rather than at a point interior to it. The unity yield condition then requires that all 2^K vertices of R_T belong to R_A i.e.

$$S_v \in R_A \text{ implies } R_T \subseteq R_A \qquad 2.24$$

Where S_v is the set of the 2^K vertices of R_T. The number of constraints can be reduced further by performing sensitivity analyses at the centre of R_T and for each performance function, identifying the worst vertex from the signs of the first order sensitivities of that performance with respect to the component parameters /28/. This reduces the number of constraints from 2^K, to m, where m is the number of requirements on the performance of a circuit for it to be deemed acceptable.

(ii) In an alternative strategy, it is assumed that the region of acceptability R_A is one dimensionally convex / 27/, as illustrated in figure 2.5. A closed region R is one dimensionally convex, if for any two points in R, which are the end points of a line parallel to any one of the co-ordinate axes all the points on the line also belong to R. Now we recall that each side of the tolerance rectangle R_T is parallel to one of the co-ordinate axes. Therefore for a one-dimensionally convex R_A, if the vertices of R_T are contained in R_A, then so is the entire region R_T (condition 2.24). However, unlike the first approach above, with the one-dimensional convexity assumption, the worst value of the performance functions need not occur at the vertices of R_T, for 2.24 to hold.

This second approach is treated by Bandler et al /17,19,27/. For each performance constraint, a combination of sensitivity analyses and tests for monotonicity of the performance functions are employed to identify the critical vertices. For a particular

tolerance region, a vertex will be designated critical if it touches the boundary of the region of acceptability. Thus the number of constraints to be considered is usually much less than 2^K.

For either approach, the minimization is performed by standard non-linear programming methods, for example, the sequential unconstrained optimization technique of Fiacco and McCormick /29/. For the discrete tolerance problem (2.10 and 2.11) a continuous solution is first obtained and is followed by a tree search method to discretize the continuous solution /19,30/.

In many practical examples, these methods and the assumptions upon which they are based are found to be acceptable. However, the worst case formulation leads to excessively narrow tolerances. It is often the case that tolerances can be relaxed appreciably for a very small dimunition in yield in the vicinity of 100%. This is illustrated in figure 2.6. The worst case methods do not provide information about, or exploit such yield tolerance trade-offs. Further, the methods are inapplicable where a unity yield is not achievable with available tolerances, such as in the design of integrated circuits.

(b) STATISTICAL FORMULATION

A general statistical formulation such as problem P1, comprising an unconstrained minimization and incorporating yield in the objective function, poses problems due to

the difficulty of computing yield. Methods addressed to problem P1 and which employ Monte Carlo analysis to estimate yield are discussed in the next section. Here we consider methods addressed to formulations P4 and P5. The cost functions depend explicitly upon tolerances, whereas yield is introduced implicitly via constraints. Unlike the worst case formulation, yield is required to be greater than a certain minimum value Y_L, say, where Y_L is less than unity.

Seth and Roe /31/ and later Thorbjorensen and Director /20/ have reported alogrithms based on the method of moments approximation, discussed in section 1.3. Essentially, the moments of the performance p.d.f. are written in terms of the moments of the component parameter p.d.f. by invoking Taylor series representations of the response functions. If the performance p.d.f. is assumed multivariate Gaussian, then bounds on the yield may be obtained via the Bonferoni inequality procedure. Alternately if no assumption is made about the form of the performance p.d.f., then a generalization of the Chebychev inequalities[α] will allow suitable estimates of the yield to be made. In either approach, constraints on the response moments may be obtained from constraints on the yield. The relationship

---

α The Chebychev inequality allows statements of the spread of a p.d.f. in terms of its variance, and mean. For example for a univariate p.d.f. P(x), with mean μ and variance σ^2:

$\{P(\mu - K\sigma < x < \mu + K\sigma)\} > 1/K^2$, where K is a constant.

between the response moments and the component parameter moments may then be used to derive constraints on the tolerances. Thence the tolerance dependent cost function can be minimized subject to these constraints. The whole process may be iterated to explore the yield tolerance trade off. The series of steps is symbolically expressed in figure 2.7. The main shortcomings of this approach arise from the fact that the inherent approximations and assumptions do not hold in practical cases. Pinel and Singhal /32/ report that the output p.d.f. cannot be assumed to be multivariate Gaussian in practical examples. In addition the low order Taylor series upon which the Transmission of variances equation is based may poorly approximate the response functions over the tolerance intervals considered.

Bandler et al /33/ employ a modified worst case method. A worst case solution is first obtained. The tolerance rectangle is then expanded and yield estimated by calculating the volume of the "infeasible region", i.e. $R_T \cap \bar{R}_A$, as shown in figure 2.8. The boundaries of the region where individual performance constraints are violated, are approximated as planes. The planes are obtained by linearizing quadratic approximations to the performance constraint boundaries. Among the main limitations of this approach are that it is only suitable where each reject circuit is expected to fail only one performance constraint. Further, the general validity of the quadratic approximation still remains unresolved.

2.4.3. METHODS BASED ON MONTE CARLO ANALYSIS

Elias /2/ has introduced a method (called TOLERATE) for tolerance assignment and design centering, where the yield versus tolerance trade-off is explored. The method is summarized in flow chart in figure 2.9. For a particular set of nominals and tolerances and for particular forms of input parameter p.d.fs Monte Carlo analysis is performed and yield is estimated. Information about the distribution in the input space, of passing and failing sample circuits, obtained from the Monte Carlo analysis is then used to re-assign nominals and tolerances. The process is iterated and the yield tolerance trade-off is explored. The method commences with wide tolerances and low corresponding yields, and progressively tightens tolerances to increase yield.

A method employing a similar approach has been introduced by Becker and Jensen /12 , chapter 9 /. For particular input parameter p.d.fs and fixed absolute tolerances, a standard direct search optimization method, pattern search /34/, is used to choose suitable nominal values. The objective function to be maximized, the yield, is estimated via Monte Carlo analysis.

The main shortcomings of these methods arise from the computational expense of performing Monte Carlo analyses iteratively. However, the number of sample circuits required to be analysed is independent of the number of toleranced components. Therefore, these methods can

deal with larger circuit examples than other techniques. In chapter 4, we describe a novel Monte Carlo based design centering method and illustrate its effectiveness for circuit examples involving up to 43 toleranced components. Unlike the pattern search method, the new technique uses information about the position in the tolerance region of pass and fail sample circuits to choose a design center to improve yield. The computational expense is moderated by efficient sampling schemes which re-use sample circuits between iterations. Further, practical shortcomings of the TOLERATE method are discussed in chapter 5. A more effective tolerance assignment method, PERTOL is introduced and a comparison with TOLERATE is presented.

In contrast to the above methods, which use standard Monte Carlo analysis, Tahim/10, chapter 5/ has introduced a radial exploration method for design centering. Essentially, an indicator approximating the yield is computed as detailed on figure 2.10. The value of the indicator is used to control the design centering process. The design centering procedure itself is based upon achieving a reduction in the assymetry of the feasibility region, i.e. $R_T \cap R_A$, as shown in figure 2.11. The radial exploration employs a particular large change sensitivity algorithm /35/ to reduce computational effort. However, this sensitivity algorithm is only applicable to linear circuits and over a restricted tolerance range.

2.4.4 DISCRETE METHODS

In many practical situations values for nominals and tolerances must be chosen from discrete sets of allowable values. For example for discrete capacitors the designer may only be allowed choices from the E24 series /36/. Although there may be greater freedom of choice of nominal values (within an achievable range) for integrated circuit components, the finite resolution of the mask making process and other processes will ensure that the choices are ultimately quantized. Therefore all proposed algorithms have eventually to consider methods for arriving at choices of nominals and tolerances from allowable discrete sets.

Two distinct approaches for the discretization problem have been reported. In the first approach a continuous solution is first sought. A discrete solution is then obtained by rounding off to the nearest discrete values, or by invoking a standard tree search method, e.g. Dakin's tree search technique /30/. In an alternative approach continuous solutions are not sought and the methods work with discrete solutions throughout. An algorithm from the class of techniques called the branch and bound methods is generally employed.

Karafin /3/ has described branch and bound methods addressed to both worst case and statistical tolerance assignment problems. In the worst case algorithm the main computational cost accrues from the process of testing

particular tolerance solution for the 100% yield condition. In chapter three, we describe the general structure of the algorithm together with a discussion of some worst case testing methods. In addition we report a cheap and efficient worst case testing method based on a regionalization/ 37/ of the input parameter space. However, as with other worst case methods, the branch and bound method offers tolerance solutions which are too pessimistic.

In contrast the branch and bound algorithm for the statistical formulation employs the method of moments to estimate yield. The assumptions and approximations involved in the method of moments, render the statistical branch and bound algorithm unreliable for many circuit applications. Nevertheless, the use of Monte Carlo analysis in place of the method of moments is not to be recommended as the number of yield estimations required would incur a prohibitive computational cost.

2.5 SUMMARY AND CONCLUSIONS

This chapter comprises a critical assessment of reported methods of tolerance assignment and design centering. Initially we discuss relevant cost functions and various problem formulations which fall under the general headings of tolerance assignment and design centering. The methods reviewed are considered under four categories. These are Geometrical characterization, Standard non-linear programming iterative Monte Carlo based methods and Discrete methods.

Of the Geometrical methods, simplicial approximation is briefly described. Geometrical methods in general become prohibitively expensive as the number of toleranced components increases beyond about ten /53/. To date simplicial approximation has been reported for a largest circuit example involving only four toleranced components.

The methods based on standard non-linear programming are further subdivided into worst case and statistical. Both groups avoid the evaluation of yield. The worst case methods constrain yield to be equal to 100%. On the other hand the statistical methods require yield to be greater than a certain minimum value Y_L, where Y_L is less than 100%. The worst case methods require procedures for testing the 100% yield condition, while the statistical methods approximate yield via procedures based on the method of moments.

The main shortcoming of the worst case methods is that of over-design. In general it is possible to trade-off yield against tolerances. The worst case methods do not explore this trade-off and hence provide expensive tolerance solutions. Additionally the worst case methods are inapplicable for situations where 100% yield is not achievable with available tolerance such as in the manufacture of integrated circuits.

In contrast the statistical non-linear programming based methods allow yield to be less than 100%, and do not produce as tight tolerances as the worst case methods. Nevertheless, statistical non-linear programming methods maximizes tolerances for a particular choice of yield and do not explore the yield tolerance trade-off. To explore this trade-off the optimization

could be repeated for different choices of yield. However, the inherent unreliability of a yield estimation procedure based on the method of moments makes this approach unattractive.

The methods based on Monte Carlo analysis have important advantages over both the geometrical and non-linear programming based methods. Firstly, in estimating yield the number of circuit analyses required in Monte Carlo analysis is independent of the number of toleranced components. Therefore such methods may be considered for large circuits. Secondly, the Monte Carlo yield estimation procedure is more general and more reliable than the method of moments. The main contributions of new techniques in this thesis falls in the area of Monte Carlo based methods. These are fully discussed in chapters four and five and only brief mention is made in this chapter.

The three categories discussed above provide continuous solutions. In practice however, only discrete choices may be available for tolerances and nominal values. The expedient of rounding off the best continuous solution to the nearest allowable discrete solution does not always provide the best available discrete solution. On the other hand Discrete methods work in terms of the discrete choices without first seeking continuous solutions. The main shortcomings of such an approach arise from the fact that the number of available discrete solutions becomes very large for the size of most circuit examples of interest. Therefore, the computational effort is often prohibitive.

The applicability of the main contributions in the field of tolerance assignment and design centering , appearing in the recent literature is summarised in table 2.1.

	Less than 100% yield	100% yield	
	P5: Seth and Roe /31/ Karafin /3, chapter 3/	P3: Pinel and Roberts /25/ Sud and Spence /26/ Karafin /38; 3, chapter 3/	Variable tolerances
Variable nominals	P1 ; P4 Elias /2/ Thorbjorensen and Director /20/ Li, Hammond and Su /39/ Bandler et al /33/ Soin /This thesis, chapter 5/	P2 Bandler et al /27/	Variable tolerances
Variable nominals	P6 Director and Hachtel /21,23/ Becker and Jensen /12, chapter 6/ Tahim and Spence /40/ Soin and Spence /41,42/ Soin /this thesis chapter 4/	May not be possible with available tolerances	

Table 2.1: A summary of the main contributions in the field of tolerance assignment and design centering (P1, P2 etc. refer to the problem formulations of section 2.3)

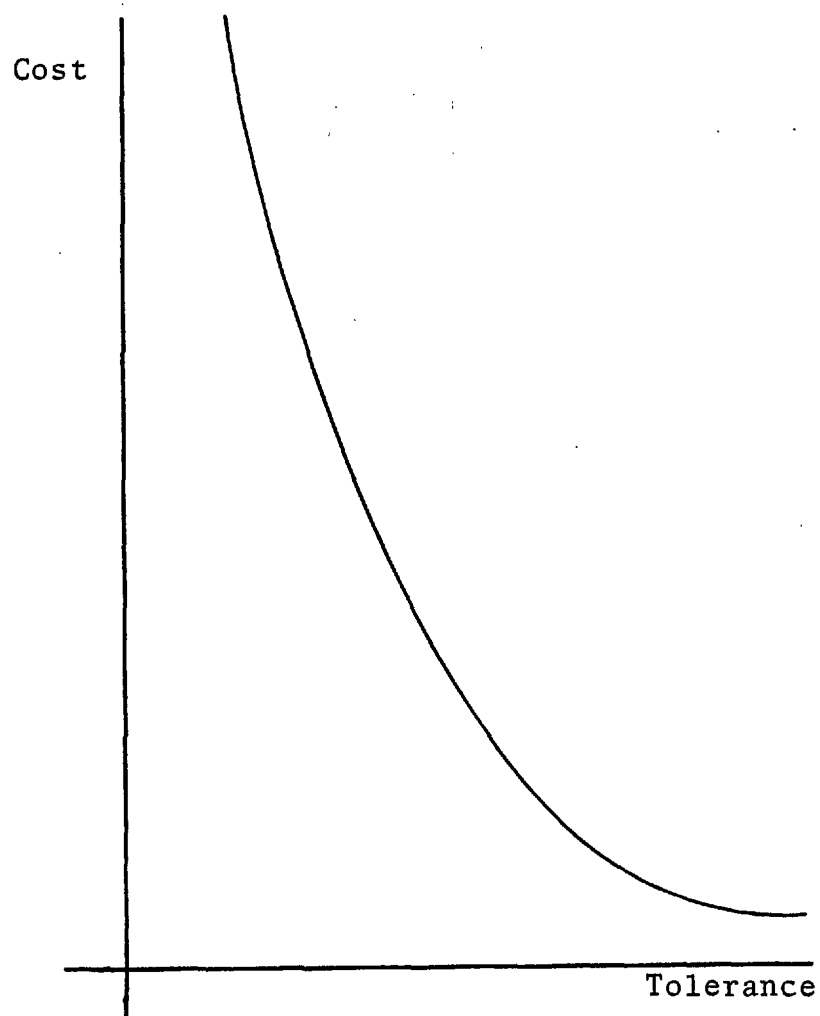


Figure 2.1 : A Typical Cost-Versus-Tolerance Relationship For A Single Component.

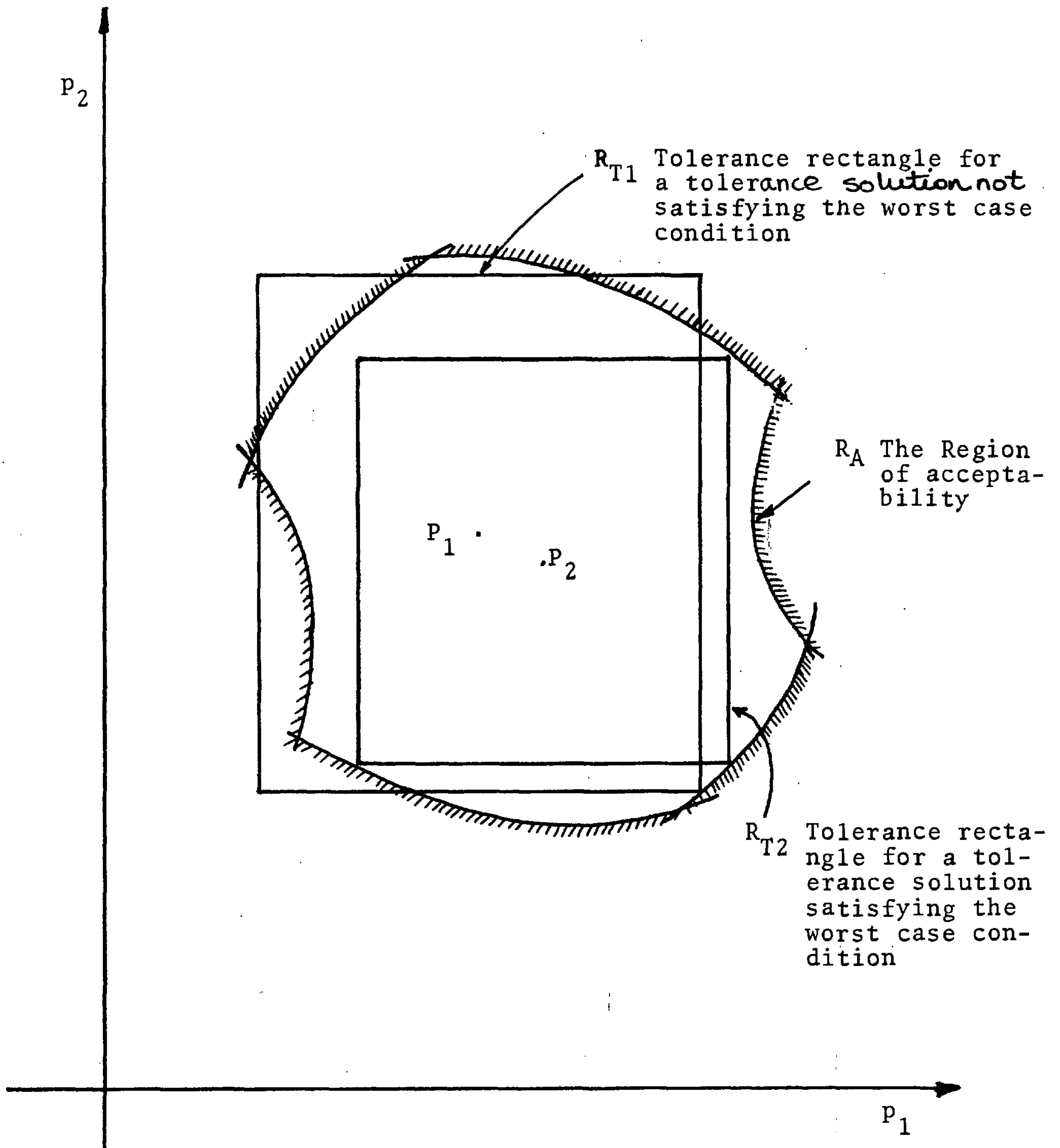
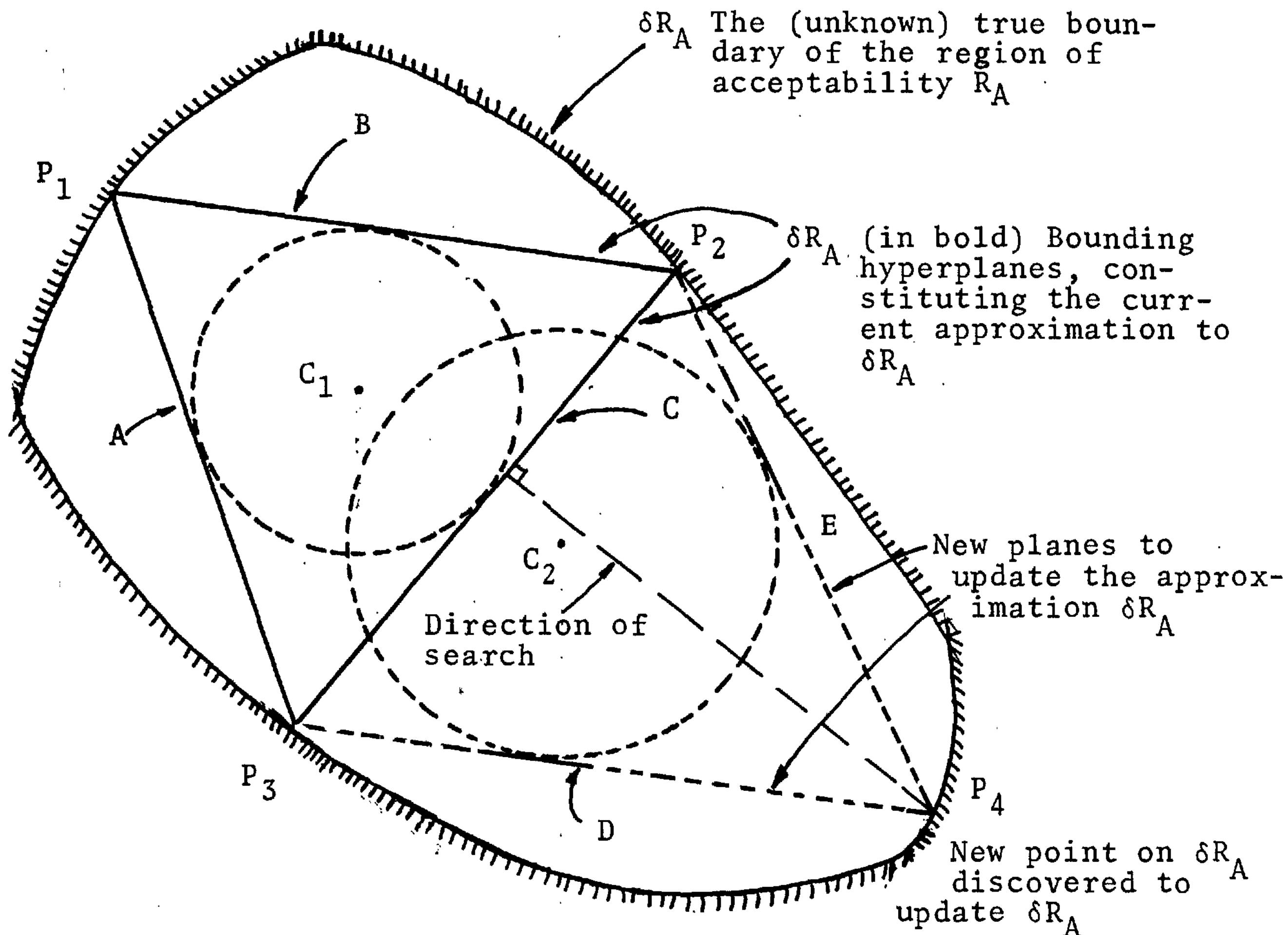


Figure 2.2 : An Illustrating Of The Geometrical Interpretation Of The Worst Case Constraint.



Note : Points P_1 P_2 P_3 are used for the current simplicial approximation , which is constituted by the lines (planes in higher dimensions) A,B, and C, indicated in bold line. Point P_4 is discovered by searching along the outward normal from the center of the largest plane (i.e C) to the boundary δR_A. The Simplicial Approximation is updated by eliminating plane C and including the new planes D and E. The center of the largest inscribable circle (hyper-sphere) in the approximation is taken to be the best design center.

Figure 2.3 : An Illustration Of The(Face Based) Simplicial Approximation Method Of Design Centering.

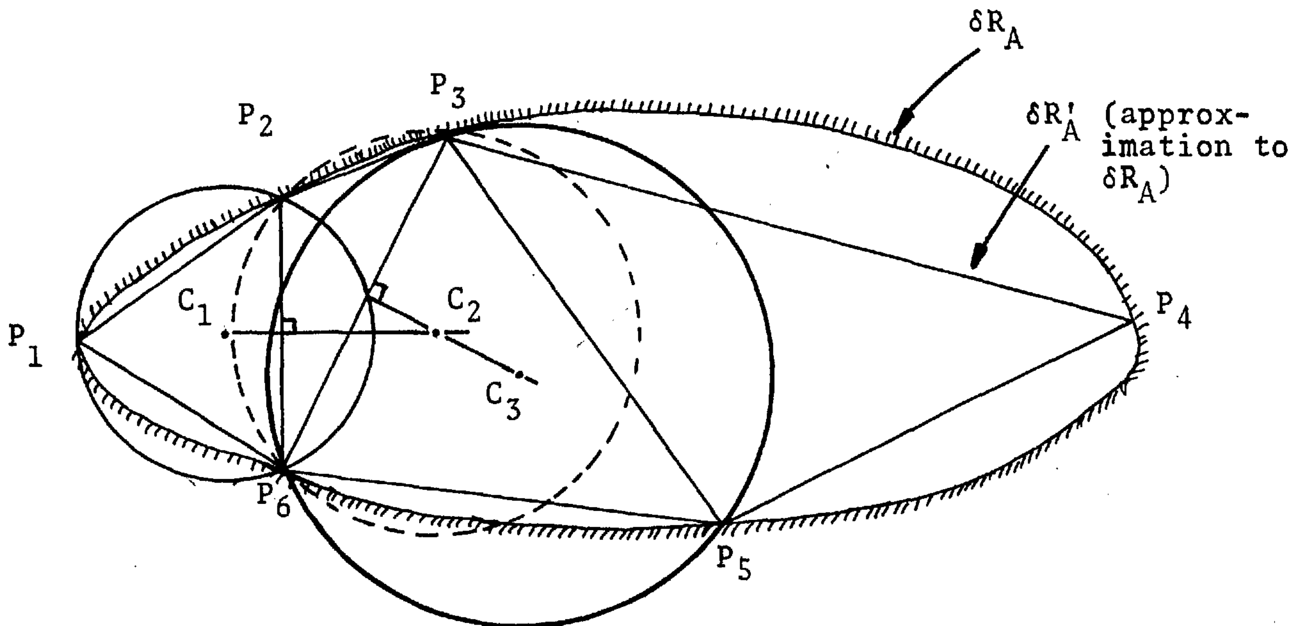


Figure 2.4(a)

Note : The point basis simplicial approximation method of design centering is described with the aid of figures 2.4(a),(b), (c),(d), and (e). Points P_1 P_2 P_3 P_4 P_5 P_6 are predetermined points on the boundary δR_A of R_A the region of acceptability. Initially the center C_1 of the circle circumscribing points P_1 P_2 P_6 is determined. The three lines (faces)of triangle P_1 P_2 P_6 are tested one by one to see if a larger circle can be found which circumscribes two points from the set P_1 P_2 P_6 and another point on the boundary δR_A. The search consists of examining trial centers which lie on the line from C_1, normal to the line of the triangle, being tested. Such a center is is discovered as C_2 which lies on the line from C_1 normal to the line P_2 P_6. The circle centered about C_2 now circumscribes points P_2 P_3 P_6. The lines of triangle P_2 P_3 P_6 are now tested as were the lines of triangle P_1 P_2 P_6. A new center C_3 is now discovered for a circle circumscribing points P_6 P_3 P_5.The procedure is terminated at C_3 because a larger circle cannot be found which will circumscribe two points from the set P_3 P_6 P_5 and P_4. The next step in the overall procedure is to discover new points on the boundary δR_A.The procedure for finding design centers can then be repeated as described above.The three stages of design centering for this example are illustrated in sequence in figures 2.4(b),(c) and (d). For clarity δR_A is not shown . Figure 2.4(e) shows the procedure for determining new points on δR_A.(Further notes are provided in the next two pages).

Figure 2.4 : The Point Basis Method Of Design Centering

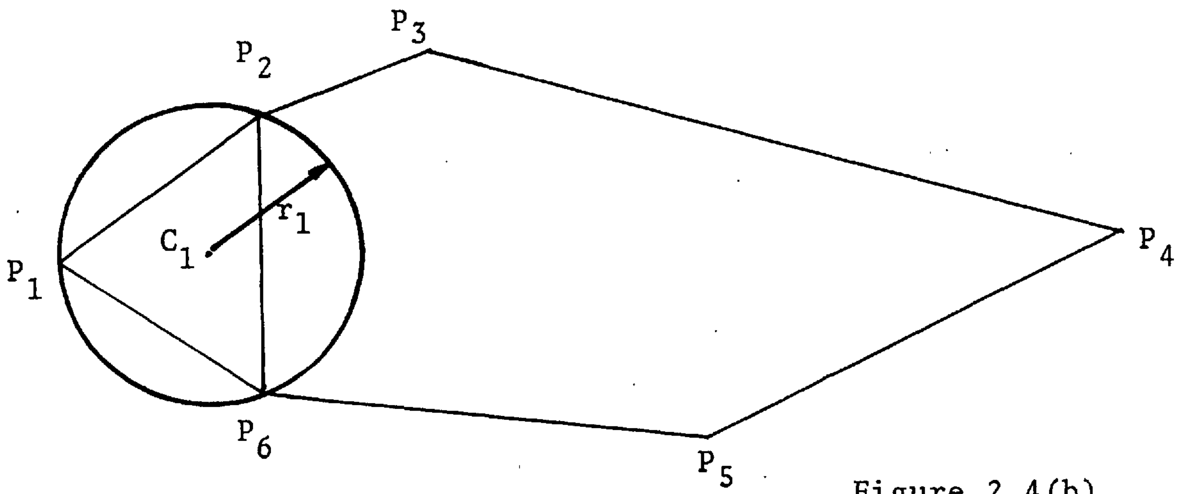


Figure 2.4(b)

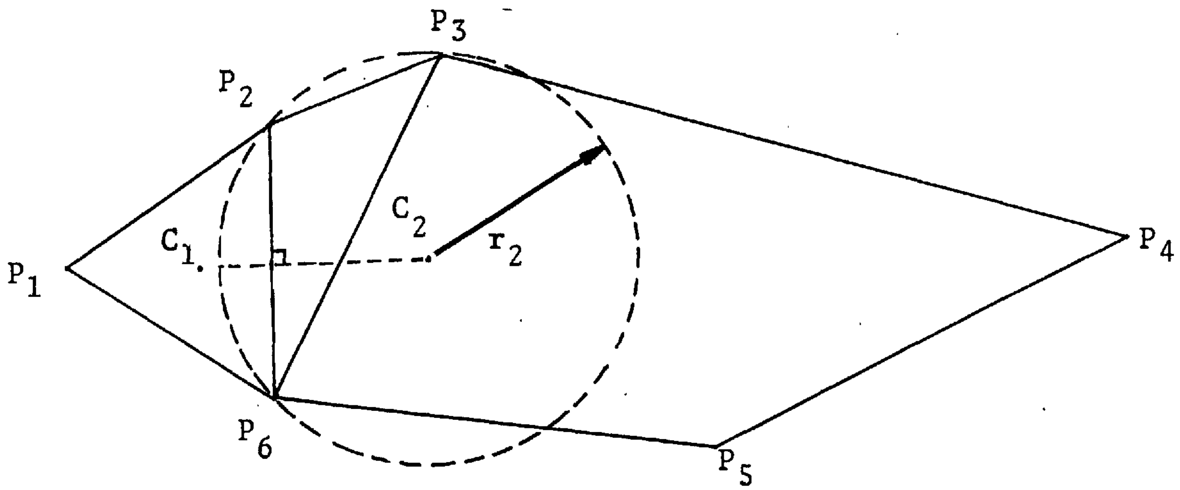


Figure 2.4(c)

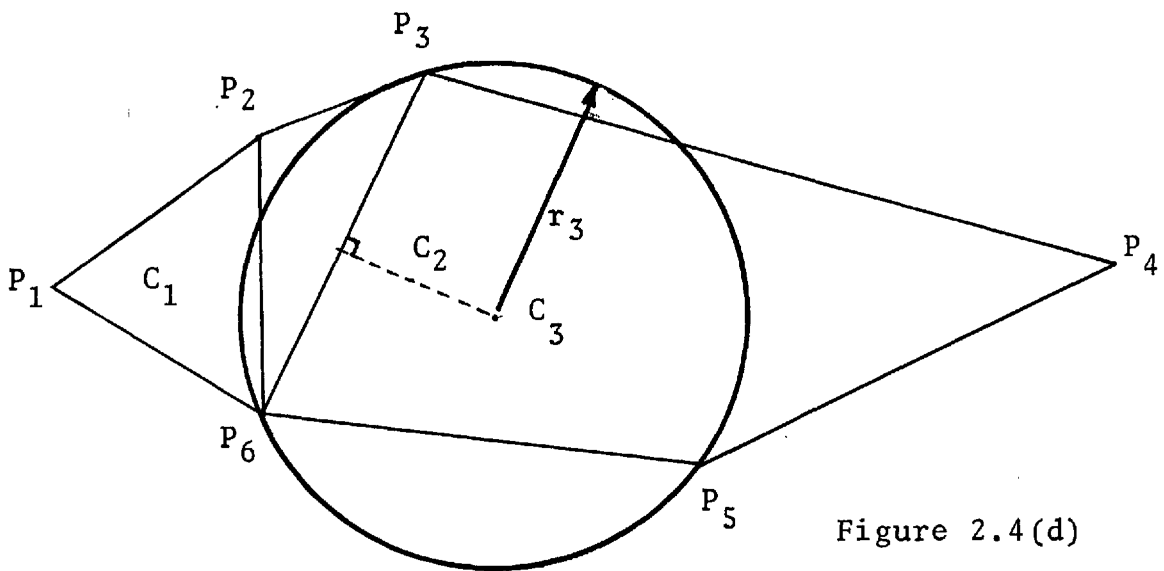


Figure 2.4(d)

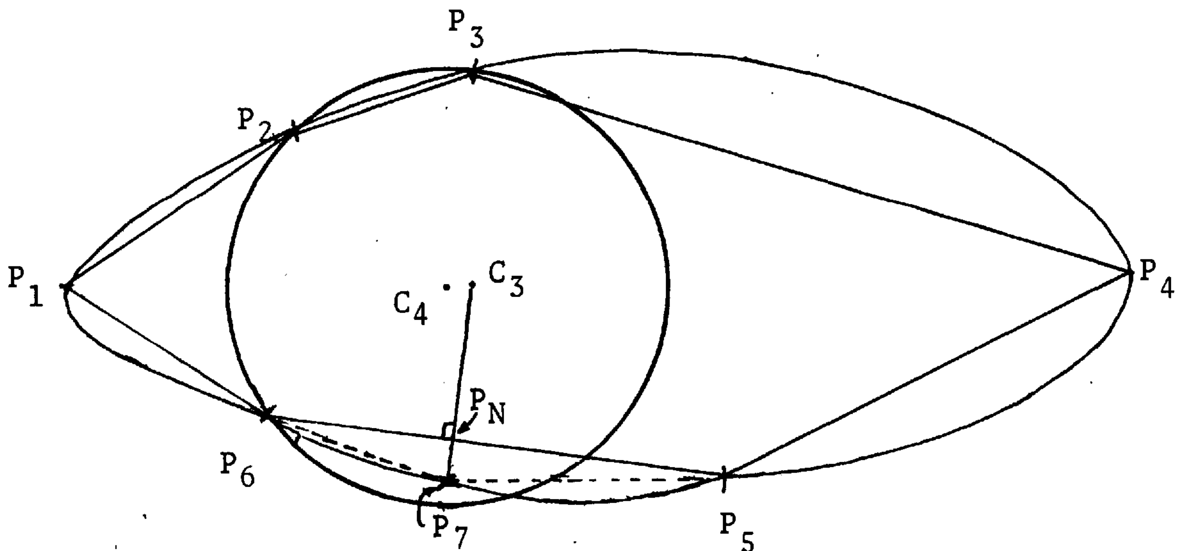


Figure 2.4(e)

Note : In figure 2.4(e) we show how new points on δR_A are located in this procedure. The point P_N on the approximating plane nearest the current design center C_3, is located. The line joining this point to the design center is searched until a new point (P_7) on δR_A is located. The procedure described in figure 2.4(a) is then repeated to obtain the best design center. For this example this is shown as C_4. The corresponding circle now circumscribes points P_2 P_3 P_7.

The point basis method has been described with reference to a two dimensional parameter space. In the general case of an n dimensional space we must consider n dimensional spheres circumscribing n+1 points on δR_A. A rigorous description is given in /23/.

The point basis method has the advantage over the face based methods that all the planes constituting the simplicial approximation do not have to be stored. Since the number of planes is much greater than the number of points this results in a considerable saving in computational effort. In addition the point basis method is not as prone to failure as the face based method when the region of acceptability is not convex.

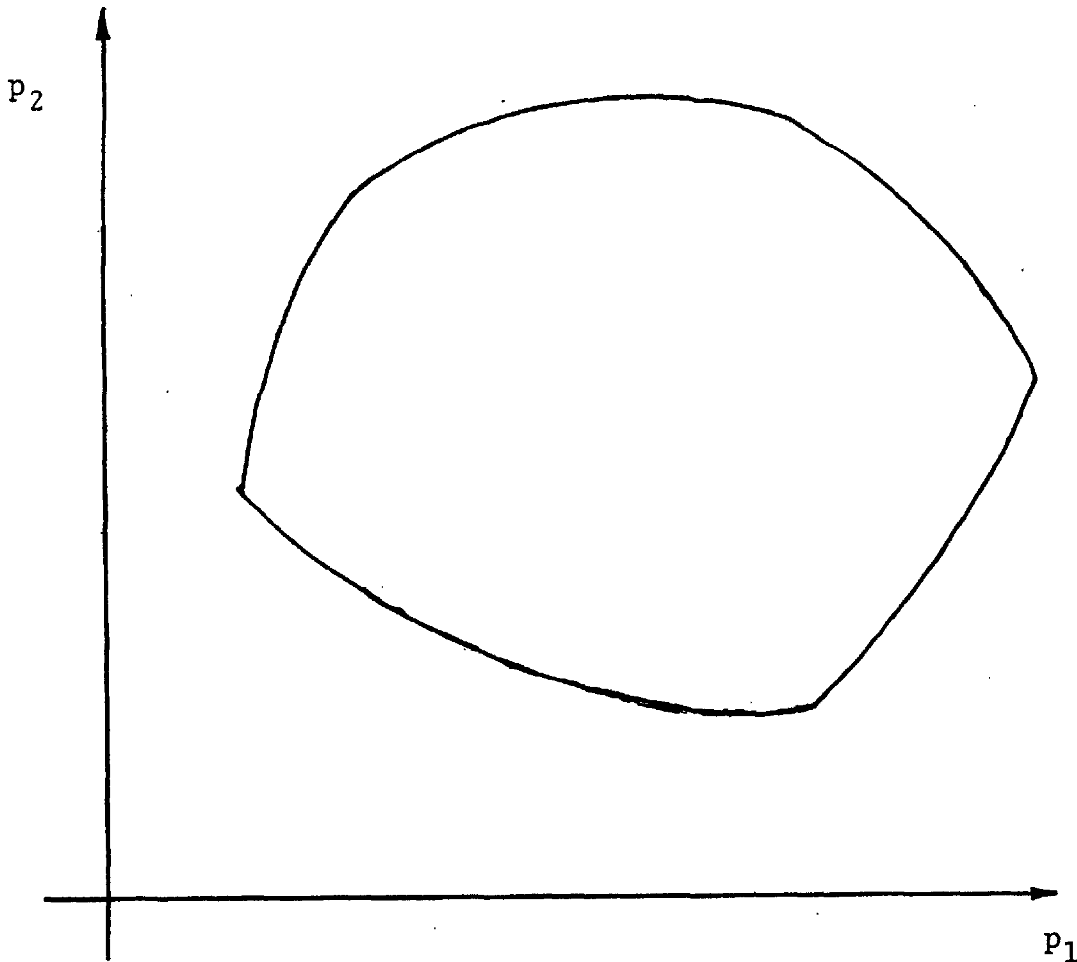


Figure 2.5(a) : A Convex region in two dimensions

Note : In figures 2.5(a) and 2.5(b) we give a simple geometrical illustration of the terms convexity and one dimensional convexity. Figure 2.5(a) illustrates a convex region in two dimensions and figure 2.5(b) a one dimensionaly convex region in two dimensions. A region is said to be convex if for any two points belonging to the region all the points on the line joining the two points also belong to the region. On the other hand a region is said to be one dimensionally convex if for any two points which are the end points of a line parrallel to any one of the co-ordinate axes,and belonging to the region, all the points on the line joining the two points also belong to the region.
Clearly if the vertices of a rectangle (hyper-rectangle) belong to a convex or one dimensionally convex region then the entire rectangle will be contained inside the region.

Symbolically a two dimensional region R is convex if

For $A=a_1,a_2$ $B=b_1,b_2$ and $A\varepsilon R$; $B\varepsilon R$ implies $P\varepsilon R$, where

$$P = A + \lambda(B - A) \qquad 0\leq\lambda\leq 1$$

Figure 2.5 : An Illustration Of One dimensional Convexity

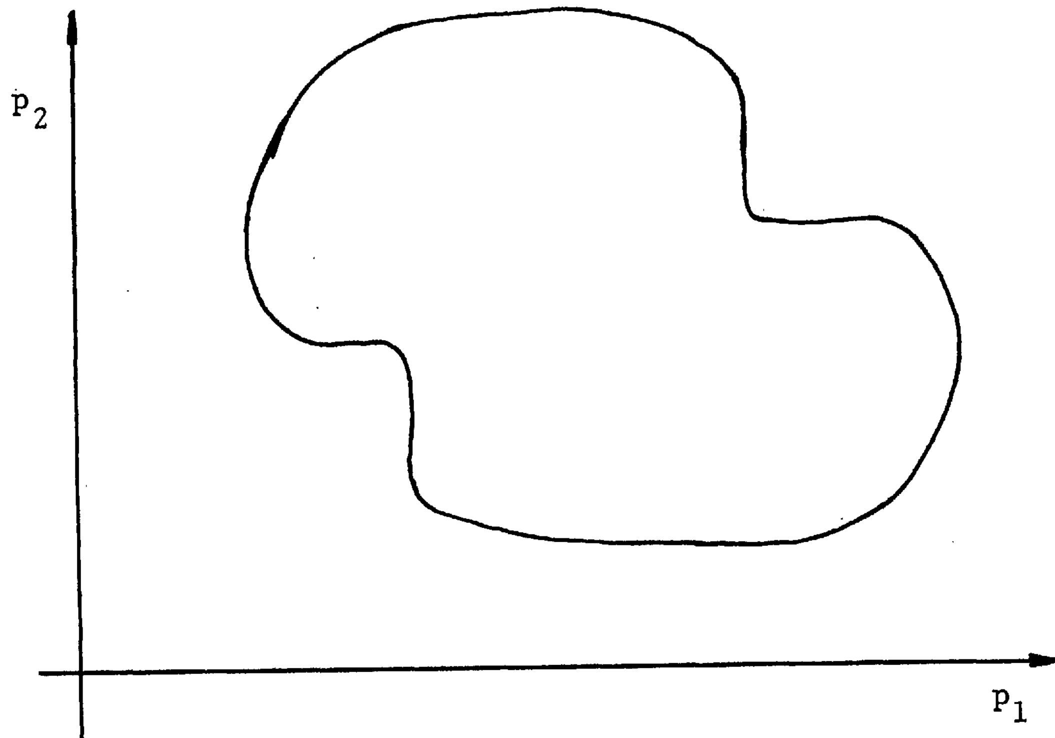
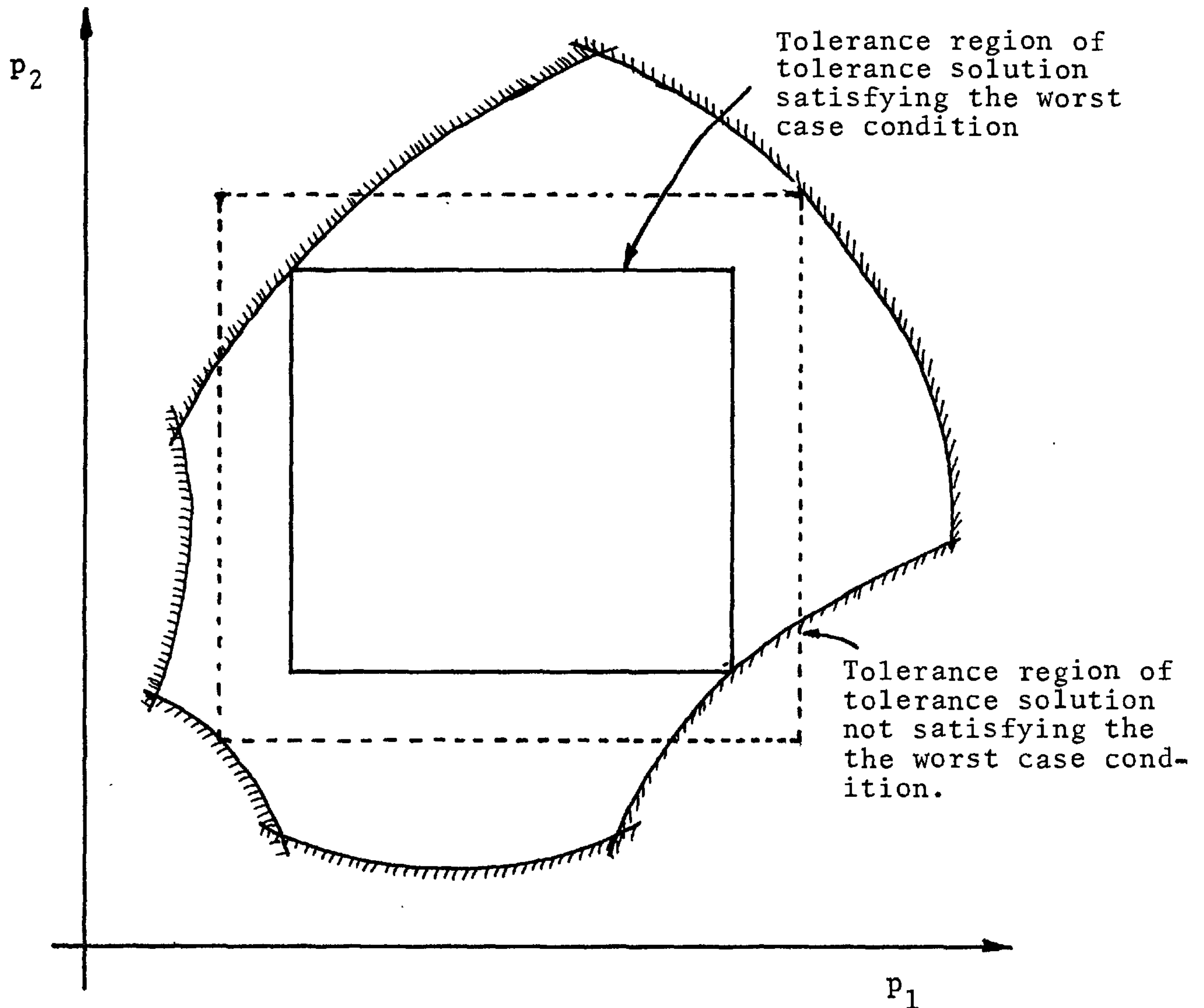


Figure 2.5(b) : Illustrating A One Dimensionally Convex Region In Two Dimensions.

Symbolically, a region R is one dimensionally convex if:

For $A=a_1,a_2$ and $B=b_1,b_2$ and $A\epsilon R$ and $B\epsilon R$ and

$b_1=a_1$ and $P = a_1,\lambda(a_2-b_2)$ $0\leq\lambda\leq 1$ implies $P\epsilon R$



Note : The diagram shows that a small diminution of yield (less than 100%) allows an appreciable relaxation of tolerances.

Figure 2.6 : Illustrating The Overdesign Inherent In The Worst Case Tolerance Solution.

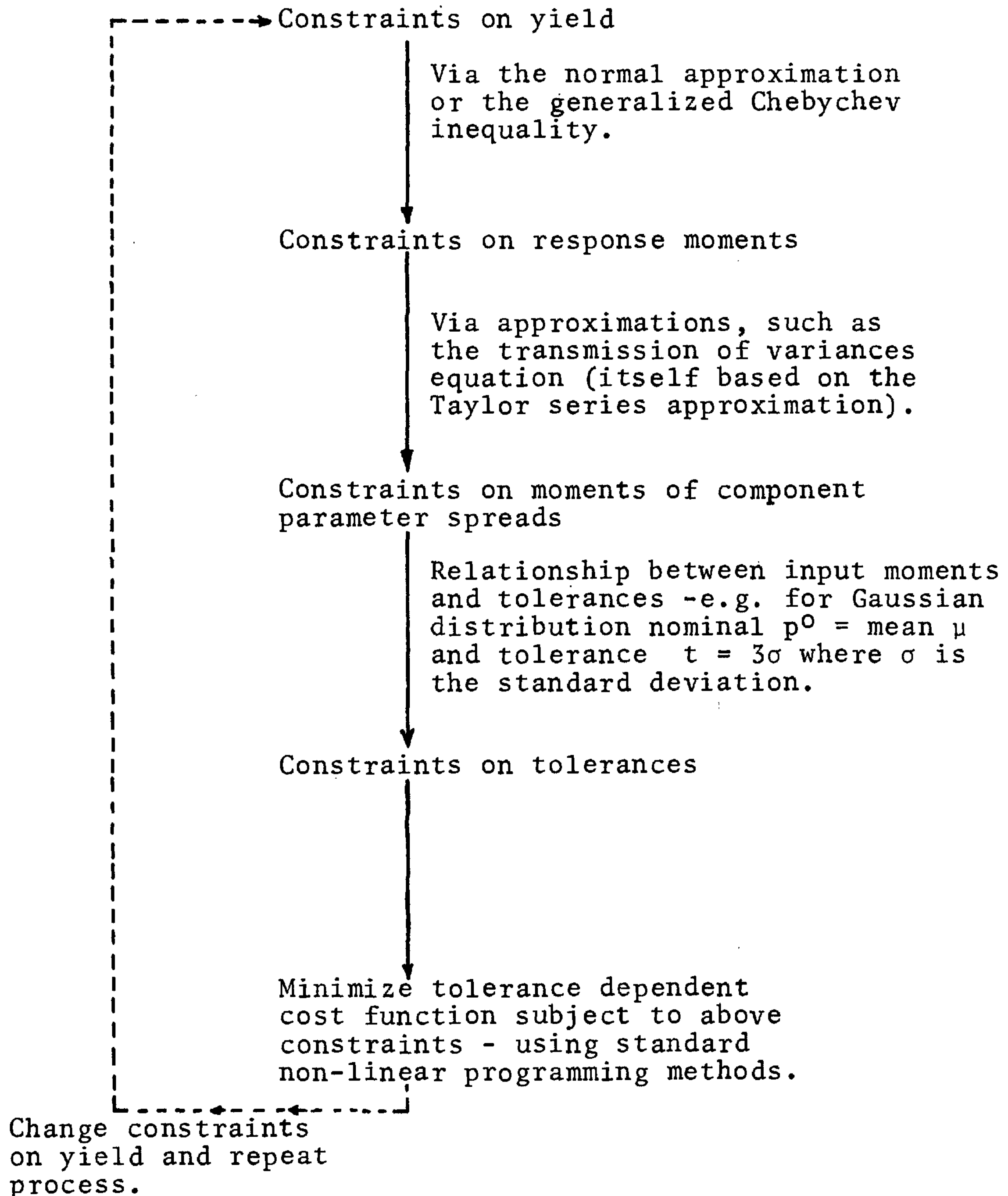
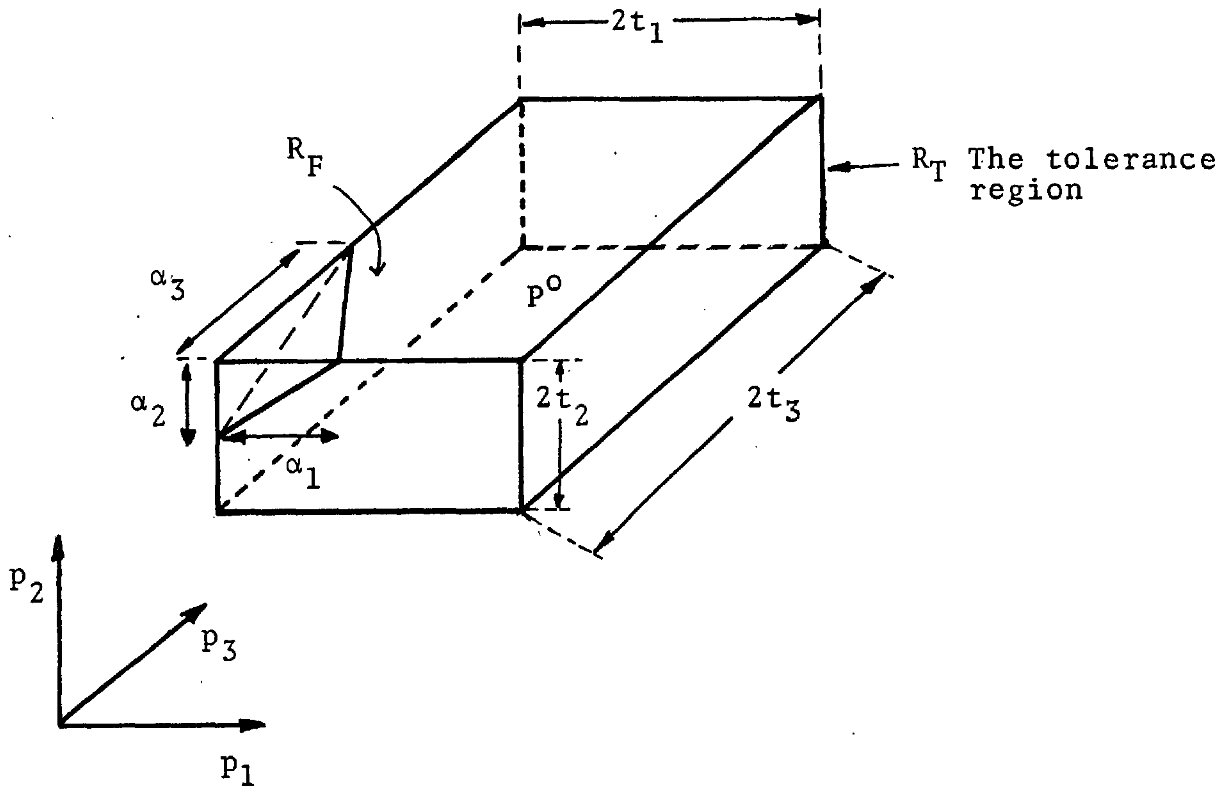


Figure 2.7 An illustration of the structure of statistical non-linear programming based methods for tolerance assignment.



Note : Here we give a simple illustration of the deterministic yield estimation method by Bandler et al. Essentially the method consists of locating points such as α_1, α_2, and α_3 which are the intersection of the region of acceptability and the tolerance region. For a three dimensional region such as the one illustrated above the three points $\alpha_1\alpha_2\alpha_3$ define a plane, which is used as a linear approximation to the intersection of the tolerance region and the boundary of the region of acceptability.
With the additional notation : $R_F = R_A \cap R_T$, where R_F is called the feasible region ,
then yield is the ratio of the volume of the feasible region to the volume of the tolerance region.
For this example the volume of the infeasible region $\bar{R}_F$ is:

$$V_F = \frac{1}{3!} (\alpha_1 \; \alpha_2 \; \alpha_3)$$

Such analytic formulae allow us to estimate yield and since the $\alpha_1 \; \alpha_2 \; \alpha_3$ are functions of the coordinates of $p_1^o \; p_2^o$ of the design center P^o we can also obtain formulae for the gradients of the yield with respect to p_1^o and p_2^o. Therefore design centering (yield maximization) may be performed using standard gradient based methods of optimization. We envisage the main difficulty with such a method will be that the approximations will be poor for more complicated regions of acceptability and when the dimensionality is high.

Figure 2.8 : A Yield Estimation Procedure Based On Linear approximation Of The boundary Of The intersection Of The Regions R_A And R_T

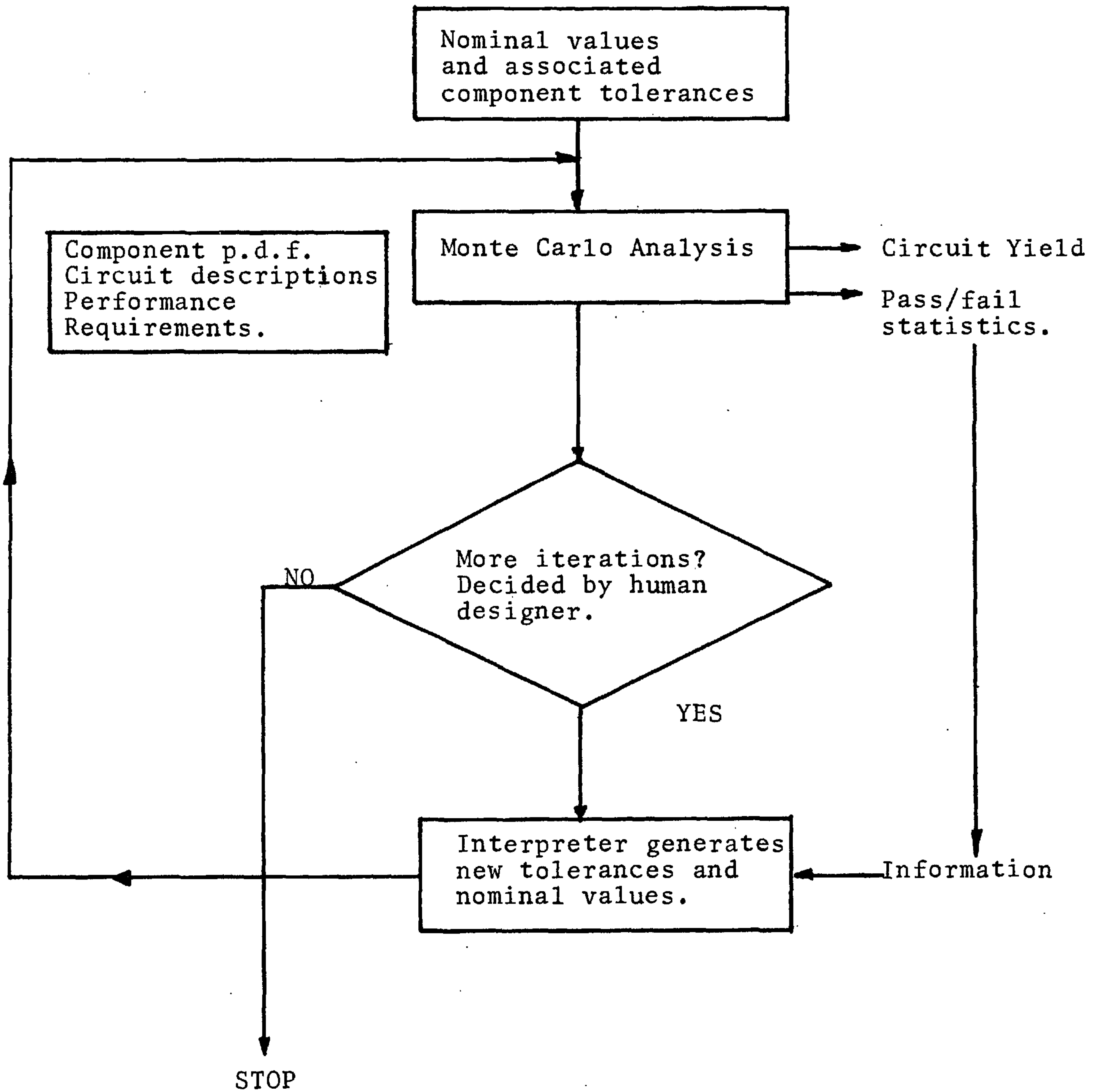
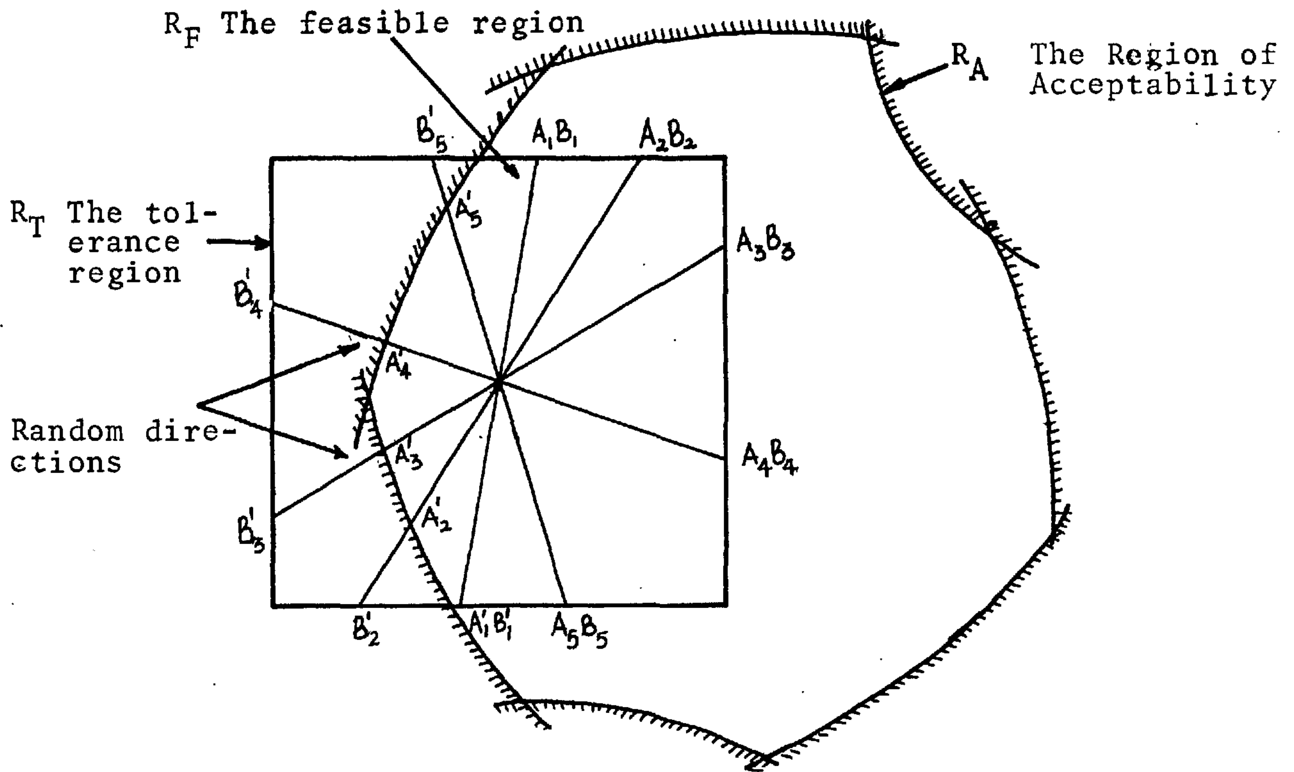


Figure 2.9 : The TOLERATE Method Of Tolerance Assignment.



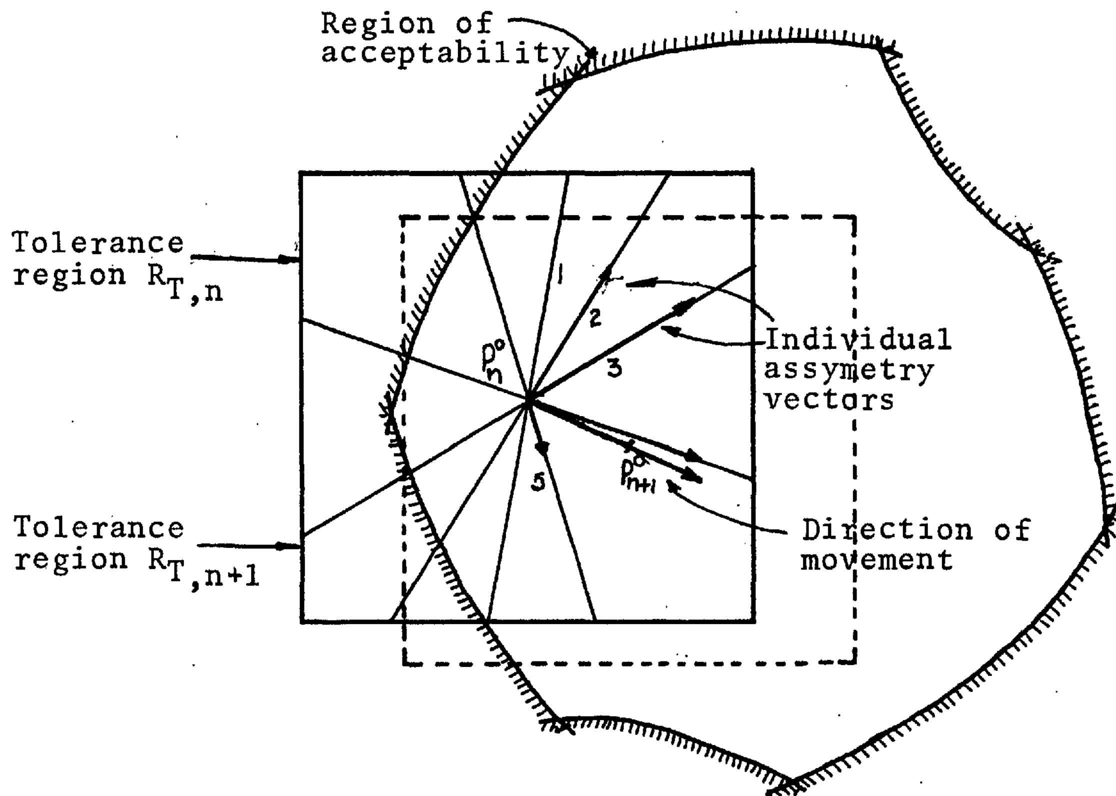
Note : A number of lines are generated at randomly chosen angles , emanating from the design center. For each line the ratios $r^+ = \frac{OA}{OB}$ and $r^- = \frac{OA'}{OB'}$ are computed. OB and OB' are the distances to the boundary of the tolerance region and OA and OA' are are distances to the boundary of the feasible region (The feasible region R_F is the intersection of the region of acceptability, and the tolerance region i.e $R_F = R_A \cap R_T$)

An indication of yield is obtained as :

$$1/N \sum_{j=1}^{N} r^+_{oj} + r^-_{oj}$$

Where N is the number of lines.

Figure 2.10 : The Radial Exploration Method Of Obtaining An Indication Of Yield



Note : P_n^o corresponds to the current design center. P_{n+1}^o corresponds to the new design center.

An indication of yield is first obtained as summarised in figure 2.10. For design centering , the assymetry vector for each line is computed. The assymetry vector of the jth. line, is a line parallel to the jth. line, and of length $r_{oj}^{+} - r_o^{-}$. The assymetry vectors are vectorially summed and a direction of movement for the design center is obtained.

Figure 2.11 : The Radial Exploration Method Of Design Centering.

CHAPTER 3 - DISCRETE OPTIMIZATION METHODS FOR WORST CASE TOLERANCE ASSIGNMENT AND DESIGN CENTERING.

3.1 Introduction.

3.2 Notation.

3.3 Branch and bound methods.

3.3.1 General structure.

3.3.2 Procedures for selecting tolerance solutions for feasibility testing.

3.3.3 Considerations for eliminating non-feasible and non-optimal solutions.

3.3.4 Feasibility testing procedure.

(a) Monte Carlo analysis.

(b) Vertex analysis.

(c) Pairwise constraints.

(d) Indentation.

3.4 Circuit example and results.

3.5 Summary.

CHAPTER 3

DISCRETE OPTIMIZATION METHODS FOR WORST CASE TOLERANCE ASSIGNMENT AND DESIGN CENTERING

3.1 INTRODUCTION

This chapter deals with the problem of tolerance assignment and design centering for the special case in which nominals and tolerances are to be selected from discrete sets of allowable values. A number of alogrithms have been developed /20,25/ where nominals and tolerances are first chosen from continuous ranges and the discrete solutions are then obtained by rounding off to the nearest allowable discrete values. However, in general rounding off the continuous solution will not produce the best available discrete solution. This is illustrated for a hypothetical case in figure 3.1. In this chapter attention is confined to an alternative class of methods, where the optimization is performed with discrete values without first seeking continuous solutions. Such methods fall in the realm of discrete optimization methods (sometimes called integer programming). Specifically, we address the discrete worst case tolerance assignment and design centering problem.

Karafin / 3/ has investigated the application of a branch and bound strategy, which comprises a tree search algorithm and various worst case testing techniques. We make brief comments on the general structure of this type of strategy, together with a review of some worst case testing

methods. The main orignal contribution reported in this chapter is a geometrically based technique, called "Indentation".[α] Indentation was developed as a complement to the regionalization method /37/ of statistical analysis. For application to linear circuits, the efficiency of regionalization and therefore indentation is enhanced by application of the systematic exploration method /44/ of large change sensitivity computation.

3.2 NOTATION

Initially consider the case where nominal component values are fixed as some constants; $P^o_* = p^*_1\ p^*_2\ \ldots.\ p^*_K$. For each component a number of tolerance values are available. Let t_{ij}, $j=1 \ldots. n_i$ represent the n_i available tolerances for the ith component. Tolerances need to be selected for each of the K component parameters. We denote by $T = t_1 t_2 \ldots. t_K$ (tolerance vector) any such choice of tolerances and by S_T the set of all possible tolerance vectors. Then the total number of elements of S_T is the product.

$$N_T = \prod_{i=1}^{K} n_i \qquad 3.1$$

Associated with each tolerance vector T is a cost denoted by C(T). C(T) is the sum of the tolerance dependent

[α] A similar approach to Indentation, called the method of orthogonal silhouettes was suggested by Leung / 43 , chapter 7/.

cost of each of the components i.e.

$$C(T) = \sum_{i=1}^{K} C_i(t_i) \qquad 3.2$$

Also associated with any tolerance vector T is a tolerance region R_T. R_T is a K-dimensional hyper-rectangle centered about the nominal point P^o and of sides of length $2t_i$; i=1 .... K. Of the set S_T of all possible tolerance vectors, we are interested in a subset S_W of vectors which result in 100% yield. Therefore the tolerance region associated with any tolerance vector belonging to S_W will be wholly contained in the region of acceptability R_A. That is $T \varepsilon S_W$ implies $R_T \subseteq R_A$. The optimization problem is then stated as:

$$\text{Minimize} \quad C(T) = \sum_{i=1}^{K} C_i(t_i) \qquad 3.3$$

by choice of $T = t_i t_2 \ldots\ldots t_K$ from the discrete set S_T, subject to the constraint that $T \varepsilon S_W$.

Task 3.3 is therefore a discrete constrained optimization problem. For most circuits of interest, the total number of possible tolerance solutions will be very large. For example, for a circuit with eight toleranced components with each component allowed five values of tolerance, the total number of possible tolerance vectors will be 8^5. Therefore, an exhaustive procedure which checked the feasibility (i.e. membership of S_W) of all possible tolerance solutions and amongst the feasible solutions identified the one with the smallest associated cost, would incur a prohibitive computational cost.

Consider now the case where nominal values are also variable. We denote by p_{ij}, $j=1 \ldots \ell_i$, the choices for the ith component and hence by

$$N_N = \sum_{j=1}^{K} \ell_j \qquad 3.4$$

the total number of possible choices. The optimization problem 3.3 can be extended to include the nominal values as design variables. The total number of possible solutions is now the product

$$N = N_N \times N_T \qquad 3.5$$

For suitable choices of nominal values it will generally be possible to select larger values of tolerance which still satisfy the worst case constraint.

3.3 BRANCH AND BOUND METHODS

Branch and bound / 4 / is a generic name for a family of discrete optimization methods. For example for the discrete worst case tolerance assignment problem the strategy entails selecting test solutions from the current set of possible solutions. The set of possible solutions initially comprises all N_T available solutions (equation 3.1). If the test solution meets the feasibility condition then its associated cost forms a lower bound. All solutions with a higher cost are eliminated. Thus the size of the current set of possible solutions is reduced. On the other hand if the test solution is infeasible then all solutions with larger tolerances will be guaranteed to be infeasible and can therefore be eliminated. The process of selecting test solutions, testing for feasibility and eliminating more expensive or infeasible solutions is continued until the cheapest feasible tolerance solution is obtained. So that although the total number of possible solutions is very large,

only a small number are tested. The vast majority of infeasible and non-optimal solutions are systematically eliminated.

3.3.1 GENERAL STRUCTURE

Figure 3.2 summarizes the essential features of one method / 3/ which is a variant of the general strategy outlined above. The two main computational tasks are a tree search for selecting tolerance solutions (box B) and procedures for testing their feasibility (boxes A, C and E). Preliminary feasibility tests are first performed (box A). The results of these computations help eliminate a large number of tolerance solutions from the total number of possible solutions. The amended set of tolerance vectors is referred to as the "current set of possible solutions".

A tree search alogrithm (box B) is then invoked to determine the optimum solution from the current set of possible solutions. The optimum solution so obtained is checked for feasibility (box C) through an initial, computationally cheap feasibility test. If it fails this feasibility test then the current set of possible solutions is amended (box D) by eliminating a number of possibilities and the tree search procedure is repeated. On the other hand, if the solution passes the initial feasibility test, it is subjected to a second more stringent and computationally more expensive feasibilty test (box E). Again failure to meet the feasibility test results in the current set of possible solutions being amended and the tree search being re-entered. Otherwise the solution is accepted as the optimum feasible solution.

3.3.2 PROCEDURES FOR SELECTING TOLERANCE SOLUTIONS FOR FEASIBILITY TESTING

Various tree search methods can be used to obtain the solution with the least associated cost from the current set of possible solutions. We note that the current set of possible solutions contains both feasible and infeasible tolerance vectors. A full description of one particular tree search alogrithm is given in reference /3, chapter 2/. However, this technique is too complex to be briefly summarized in this chapter.

Nevertheless the general ideas will become apparent from the following description of a very simple tree search alogrithm called the bisectional search. This method has been incorporated in a general optimization strategy, (see section 3.4), which differs a little from the structure shown in figure 3.2.

Consider an example involving three toleranced components. Let the number of allowed tolerance values for each component be five, and let these be 1% 2% ..... 5%. Therefore there are initially a total of 125 possible tolerance solutions. Firstly, the cost associated with each solution is computed and the tolerance vectors are ordered in descending order of cost. A typical ordering will be the following.

Solution No.	% TOLERANCES Component 1	Component 2	Component 3
1	5	5	5
2	5	4	5 ⌉ equal cost
3	4	5	5 ⌋
63	3	3	3
125	1	1	1

Now the current set of possible solutions contains 125 elements. To choose a candidate for feasibility testing the ordered set is bisected. That is the tolerance solution half way between the most and least expensive is selected. In the first case this will be solution number 63, which will correspond to tolerances of 3% on each component.

Now if this solution passes the feasibility tests then the solutions numbered 64 to 125 are eliminated from consideration, since they are more expensive than 63. Alternately, if the test solution is infeasible, then among solutions 1 to 62, the tolerance vectors with corresponding tolerances equal to or larger than those of the test solution are eliminated. For example if the test vector 3 3 3 is found to be infeasible, then 3 4 3, 3 3 4, 4 4 4 etc. will also be infeasible. This will be further clarified in the next section.

The remaining solutions are now re-numbered. The next trial solution is then chosen as before by bisecting the current set of possible solutions. The process is continued as before, until only one tolerance vector remains and all the others have been eliminated as described above. The remaining tolerance solution will then be the optimum feasible solution.

3.3.3. CONSIDERATIONS FOR ELIMINATING NON-FEASIBLE AND NON-OPTIMAL SOLUTIONS

If a particular tolerance solution is found to be feasible, then all other tolerance solutions with greater associated cost are eliminated from consideration. On the other hand if the tolerance solution is found to be infeasible, then all other solutions with tolerances equal to or larger than this trial solution will also be infeasible. These in turn can be eliminated from consideration. The basis for this is explained below.

Now the cost associated with a particular tolerance vector is the sum of the costs of the individual component tolerances: i.e. equation 3.3

$$C(T) = \sum_{i=1}^{K} C_i(t_i)$$

The individual cost functions $C_i(.)$ are discontinuous functions defined for discrete values of t_i (see figure 3.3). Typically:

$$C_i(t_i) = \frac{a_i}{t_i} \qquad 3.6$$

for $t_i = t_{i1}\ t_{i2}\ \ldots .\ t_{ij}\ \ldots .\qquad j=1\ \ldots\ldots\ n_i$

The $C_i(t_i)$ are monotonically decreasing functions. That is, they have the following property.

$$C_i(t_i^*) < C_i(t_i^{**}) \quad \text{for} \quad t_i^* > t_i^{**} \qquad 3.7$$

We consider two tolerance vectors $T' = t_1' \; t_2' \; \ldots . \; t_K'$ and $T'' = t_1'' \; t_2'' \; \ldots \; t_K''$, such that

$$t_i'' \leq t_i' \quad \text{for all } t_i,\ i=1 \ldots K \qquad 3.8$$

Then for overall costs $C(T') = \sum_{i=1}^{K} C_i(t_i')$ and $C(T'') = \sum_{i=1}^{K} C_i(t_i'')$, we may say:

$$C(T'') \geq C(T') \qquad 3.9$$

In other words the cost of a particular tolerance solution T' is less than or equal to the cost of any other tolerance solution T'', if the elements of T' are greater than or equal to corresponding elements of T''.

Secondly, if a vector T' is found to be infeasible, then any other vector T'' will also be infeasible if T' and T'' satisfy condition (3.8). This is so, because if T' and T'' obey condition (3.8), then the dimensions of the sides of the tolerance rectangle R_T' will be greater than the dimensions of the corresponding sides of tolerance rectangle R_T''. Therefore, if R_T' cannot be wholly contained in R_A then neither can R_T''. Symbolically if T' and T'' obey

condition (3.8), then

$$R'_T \nsubseteq R_A \quad \text{implies} \quad R''_T \nsubseteq R_A \qquad 3.10$$

This is shown in figure 3.4.

3.3.4 FEASIBILITY TESTING PROCEDURES

In general no computational procedure will allow us to say with absolute certainty that a particular tolerance solution is feasible. Nevertheless, in the method outlined in figure 3.2, the feasibility tests are used to detect infeasible tolerance solutions. Now the passing of a feasibility test by a tolerance solution does not guarantee its feasibility. However, failure to do so does guarantee infeasibility. That is, in addition to passing all feasible solutions, the tests will also pass some infeasible solutions. The tendency of a test to pass infeasible solution is referred to as its stringency. The greater the stringency of a test, the less likely it is to pass infeasible solutions. Also in practice it is found that the more stringent feasibility tests tend to be computationally more expensive. Therefore, in the discrete optimization strategy, the tests are used in ascending order of computational cost (hence stringency). In the next section we examine the cost and efficiency of different feasibility tests.

(a) MONTE CARLO ANALYSIS

For the general case, Monte Carlo analysis provides the most stringent feasibility test. However, it is also computationally the slowest and most expensive method. Therefore

in a discrete optimization scheme such as the one outlined in figure 3.2, Monte Carlo analysis is only employed after a tolerance solution has passed the computationally cheaper and less stringent tests.

In this procedure a random sample circuit is generated in the tolerance region and is analysed and tested against performance requirements. If the circuit fails to meet any one of the performance requirements, the tolerance solution under test is deemed to be infeasible and the test is terminated. Otherwise a new random sample circuit is generated and the analysis is repeated. The procedure is continued for several hundred sample circuits (typically 300) and if all circuits are found to meet performance requirements then the tolerance vector is accepted. This will still not guarantee feasibility because the Monte Carlo analysis does not exhaustively explore the entire tolerance region.

With the expectation that worse values of performance occur at the periphery of the tolerance region, the random component values are often generated to have a bimodal distribution (figure 3.5). However, with such distributions the random circuits always tend to be adjacent to the vertices. The regions adjacent to the sides of the tolerance rectangle tend not to be tested. Therefore, it is considered preferable / 3/ to employ p.d.f's of the form shown in figure 3.6. These distributions ensure that points not adjacent to the vertices are also tested. Although a bias towards the periphery of the tolerance region is maintained, some points from the middle are also tested. This makes the feasibility test more stringent.

(b) VERTEX ANALYSIS

For a tolerance solution T to be feasible, the associated tolerance region R_T has to satisfy the condition.

$$R_T \subseteq R_A \qquad 3.11$$

If it is assumed that the extreme values of each performance function occurs at one of the vertices of R_T then a suitable feasibility test consists of circuit analyses at all vertices of R_T. However, R_T has 2^K vertices (where as before K is the number of toleranced components). Therefore such a procedure is prohibitively expensive for most circuit examples. The problem becomes more tractable if certain sensitivity analyses are employed to give an indication of the worst vertex for each performance constraint. This reduces the number of vertices to be tested to be less than or equal to m, where m is the number of performance constraints. A fuller discussion of this method is provided in chapter 2, Section 2.4.2 and in references /16,19,28/. Failure of a tolerance solution to satisfy such a vertex test guarantees infeasibility; however, success does not ensure feasibility. This is so because it cannot be ensured that the assumptions of worst behaviour at vertices, and the method of identifying the worst vertices are always valid. Nevertheless, in practice this method has been found to give satisfactory results for a large number of circuit examples.

(c) PAIRWISE CONSTRAINTS

The feasibility testing procedures discussed above check feasibility of one particular tolerance vector at a time. In contrast the pairwise constraint method provides information on combinations of individual component tolerances which will result in feasible and infeasible tolerance solutions. The technique is invoked prior to commencing with the tree search routine (figure 3.1). This routine uses the pairwise information to eliminate infeasible solutions from consideration while searching for an optimal feasible solution.

The pairwise constraint method is essentially a geometrical technique. Component parameters are selected two at a time. Thus for K parameters $\binom{K}{2}$ selections are made. Consider the ith and jth parameters p_i and p_j respectively. The values of the other (K-2) parameters are held at their nominal values and the two dimensional space of variation of p_i and p_j is explored. That is, circuit analyses are performed for various pairs of parameter values chosen by some search alogrithm, and an approximation to the boundary of the region of acceptability R_{Aij} in this space is obtained.

Now let the allowable tolerances of the parameters p_i and p_j be:

$$t_{ir}, \quad r=1 \,.....\, n_i \tag{3.12}$$

and

$$t_{js}, \quad s=1 \,.....\, n_j$$

Then pairs of tolerance values, with each pair comprising a member from t_{ir} and a member from t_{js} are tested

for feasibility inside R_{Aij}, as shown in figure 3.7. The set S_{ij} of pairs of tolerances of components i and j which meet the feasibility condition is identified. The process is repeated for all possible combinations of components taken two at a time.

To test the feasibility of a particular tolerance solution $T^* = t_1^* \; t_2^* \; \ldots\ldots \; t_K^*$, these specific tolerance values are taken two at a time and checked for membership of the appropriate set S_{ij}. If any one of the pairs of tolerance values does not belong to the relevant set, then the entire tolerance solution is guaranteed to be infeasible. However, the converse does not hold. Compliance with pair-wise constraints does not guarantee feasibility. This is further explained in reference / 3/.

Most of the computational cost associated with this method is incurred in performing circuit analyses to obtain approximations to the 2-dimensional regions of acceptability R_{Aij}. This cost can be reduced by use of a large change sensitivity alogrithm, such as systematic exploration /43/. Nevertheless, the computational cost of this method is much greater than other feasibility tests. In addition it is found to pass too many infeasible solutions and hence is not to be generally recommended.

(d) INDENTATION

Indentation is a geometrically based feasibility test which is applicable when the component parameter space is regionalized /37/. Regionalization is demonstrated for a two dimensional example in figure 3.8. An initial tolerance region, the region of exploration R_E is divided into a number of sub-regions by partitioning along each of the component parameter directions. The circuit is analysed at the center point of each sub region. Accordingly the point and corresponding region are identified as pass or fail. In this way a discrete representation R'_A of the region of acceptability R_A is obtained (see figure 3.9).

Initially assume that both nominals and tolerances are variable. Then the set of points to be analysed is determined by the available choices of nominal values. On the other hand the available choices of tolerance values determine the lateral dimensions of the sub regions. For a particular tolerance solution T^* and tolerance hyper-rectangle R^*_T, the procedure to be described checks whether one of the analysed points can be chosen as the center of R_{T^*}, such that R_{T^*} is wholly contained in $R_{A'}$. That is, indentation tests whether

$$R_{T^*} \subseteq R_A \qquad (3.13)$$

The indentation procedure also identifies the points (if any) about which R_{T^*} may be centered for 3.13 to hold.

The basis of the method is illustrated in fig. 3.10. R_E and $R_{A'}$ are the regions of exploration and acceptability as before.

The computational procedure identifies "indented regions" such as $R_T^{1,1}$ and $R_T^{2,3}$. Region $R_T^{2,3}$ for example is the region containing all those points about which a tolerance rectangle of lateral dimensions $4\Delta p_1$ and $6\Delta p_2$ may be centered and yet be wholly contained in R'_A. Similarly, $R_T^{1,1}$ corresponds to the centers of a tolerance rectangle of dimensions $2\Delta p_1$ and $2\Delta p_2$. For this two dimensional example, these regions can be obtained by a very simple geometrical procedure involving an indentation of the boundary of the region R'_A.

The computational procedure for the general case is described with reference to figures 3.11 and 3.12 and 3.13. The region of exploration R_E is represented as an array of logical elements as shown in figure 3.11. A logical 1 implies membership of R_A for the corresponding sub-region and logical 0 implies membership of $\bar{R}_A$. For the components p_1 and p_2, let the number of quantized intervals be n_1 and n_2 respectively. Any allowable choice for tolerances t_1 and t_2 will be some multiple of the respective lateral dimensions Δp_1 and Δp_2 of the sub regions. Let us further assume that the feasibility of the solution $t_1 = 2\Delta p_1$ and $t_2 = 3\Delta p_2$ is to be tested. Then for a two dimensional example a maximum of four sets of logical operations called "partial indentations" will need to be performed.

Figures 3.12 (a) to 3.12 (d) represent the partial indentations. Matrix A is the original R_E matrix. Matrices B,C,D and E are obtained by indenting matrix A by appropriate amounts. For example B is obtained from A by offsetting the elements by +2 and +3 along dimensions one and two respectively.

Symbolically the elements b_{ij}: $i=1 \ldots n_1$, $j=1 \ldots n_2$ of B are related to the elements a_{ij}; $i=1 \ldots n_1$, $j=1 \ldots n_2$ of A as:

$$b_{ij} = a_{i+2,j+3} \qquad \begin{array}{l} i=1 \ldots\ldots (n_1-2) \\ j=1 \ldots\ldots (n_2-3) \end{array} \qquad 3.14$$

$$= 0 \quad \text{otherwise.}$$

Similarly, the elements of C are obtained by offsetting the elements of A by +3 and -2 along dimension one and two respectively. So that

$$C_{ij} = a_{i-2,j+3} \qquad \begin{array}{l} i=3,4 \ldots\ldots n_1 \\ j=4,2 \ldots\ldots (n_2-3) \end{array}$$

and so on for matrices D and E.

To complete the process logical AND operations are performed on corresponding elements of B,C,D and E. That is, we get matrix F as: $F = B.C.D.E$

or

$$f_{ij} = b_{ij} \cdot c_{ij} \cdot d_{ij} \cdot e_{ij} \qquad \begin{array}{l} i= 1 \ldots n_1 \\ j= 1 \ldots n_2 \end{array} \qquad 3.15$$

where b_{ij}, c_{ij}, d_{ij}, e_{ij}, f_{ij} are elements of matrices B,C,D,E and F respectively. For this example (figure 3.11 and 3.12) the matrix F is shown in figure 3.12 (e). Every element of F with a value of 1, represents a point about which a tolerance rectangle of size 6 by 4 can be centered and be wholly contained in R'_A.

In practice it is inadvisable to perform all the partial indentations before performing the AND operations, i.e. 3.15. For a K dimensional example 2^K partial indentations would be required. Now the storage requirements for 2^K matrices would be prohibitive for most examples. Therefore

the AND operations are performed after each partial indentation. So that for the two dimensional example above, after obtaining matrix C we would obtain matrix F as:

$$F = B.C \qquad 3.19$$

Matrices B and C would no longer be required and hence would be discarded. Matrix D would be obtained from matrix A as described before. This would be followed by matrix F being updated as

$$F = F.D \qquad 3.20$$

Then after obtaining matrix E by the appropriate partial indentation, we would get the final F matrix as:

$$F = F.E \qquad 3.21$$

In general the process need not always be performed for all 2^K partial indentations. We recall that if every element of the final F matrix, i.e. 3.21 is a logical 0 then the tolerance solution under test in infeasible. Clearly, this will also be the case if all the elements of the F matrix after an intermediate stage (i.e. 3.19 and 3.20 etc) are zero. Therefore, in a practical implementation of this method the matrix F is checked for non-zero elements after each partial indentation and logical AND operation. If at any stage the elements of F are all zero, then the test is terminated and the tolerance solution declared infeasible. Otherwise, at the end of 2^K partial indentations, the tolerance solution is taken to have passed the feasibility test. The component values corresponding to logical 1's are then identified as suitable design centers for the tolerance solution under test.

In the situation where the nominal point is to remain fixed, the procedure is modified slightly. After each partial indentation and logical AND operation, the resulting F matrix is checked to see if the particular element corresponding to the fixed nominal point is a logical 1. The test is terminated and the tolerance solution declared infeasible if this element is a logical 0.

In the next section the effectiveness of the indentation procedure will be demonstrated by application to a particular circuit example involving three toleranced components. We note that in common with other geometrically based methods, the computational cost increases very sharply with dimensionality. The greater proportion of the computational cost will be incurred in performing circuit analyses following regionalization. For example, for a circuit with K toleranced components and with q intervals for each component, a total of q^K circuit analyses will be required. On the other hand the computational cost of each partial indentation will largely be incurred in performing q^K logical AND operations. In addition the maximum number of partial indentation required (2^K) will double with dimensionality. Again the computational effort incurred in the circuit analyses may be considerably moderated by employing the large change sensitivity method called systematic exploration /43/. However, this method is only applicable to the frequency domain behaviour of linear circuits.

3.4 CIRCUIT EXAMPLE AND RESULTS

The indentation procedure was incorporated in a discrete optimization strategy comprising the bisectional search described in section 3.3.2. Tolerance assignment and design centering were performed on the circuit shown in figure 3.13. The circuit was subject to the performance requirements detailed in figure 3.14. The three components marked with arrows were taken to be toleranced. For performing the regionalization, the nominal component values shown in figure 3.14 (i.e. p_1^o, p_2^o, p_3^o) were used. For each component a range of ±10% of this nominal value was divided into 10 intervals. The resulting 11^3 points[α] were then analysed and tested for compliance with the performance requirements. The logical matrix so obtained is illustrated in figure 3.15. $R_{E'}$ is a three dimensional logical array of size 11 x 11 x 11. To represent $R_{E'}$ in two dimensions, eleven 11 x 11 matrices are shown. Each matrix corresponds to one of the eleven allowable values of component X_1. The 11 x 11 points of each matrix correspond to the eleven choices for each of the other two components.

In total four tolerance solutions were tested for feasibility. The final solution comprised tolerances of 4, 6 and 6 percent respectively of p_1^o, p_2^o and p_3^o (see figure 3.13) for components X_1, X_2 and X_3. The corresponding design center

[α]These points could have been analysed cheaply with the systematic exploration technique. However, in the absence of an implementation of this method, 11^3 analyses were performed.

is indicated in figure 3.15. Finally, for these tolerances and nominals a 500 sample Monte Carlo analysis was performed using uniform distributions for each component. No failures were encountered.

3.5 SUMMARY

In this chapter discrete optimization methods for the worst case tolerance assignment and design centering problems have been considered. The general branch and bound strategy has been outlined. The main computational aspects of this strategy have been identified firstly as a discrete search method for selecting suitable tolerance solutions and secondly various methods for testing tolerance solutions for their compliance with the worst case condition. A simple search strategy called the bisectional search and various worst case testing methods have been described. In particular a novel geometrically based worst case testing method called indentation has been presented. The effectiveness of this method has been demonstrated by application to a circuit involving three toleranced components.

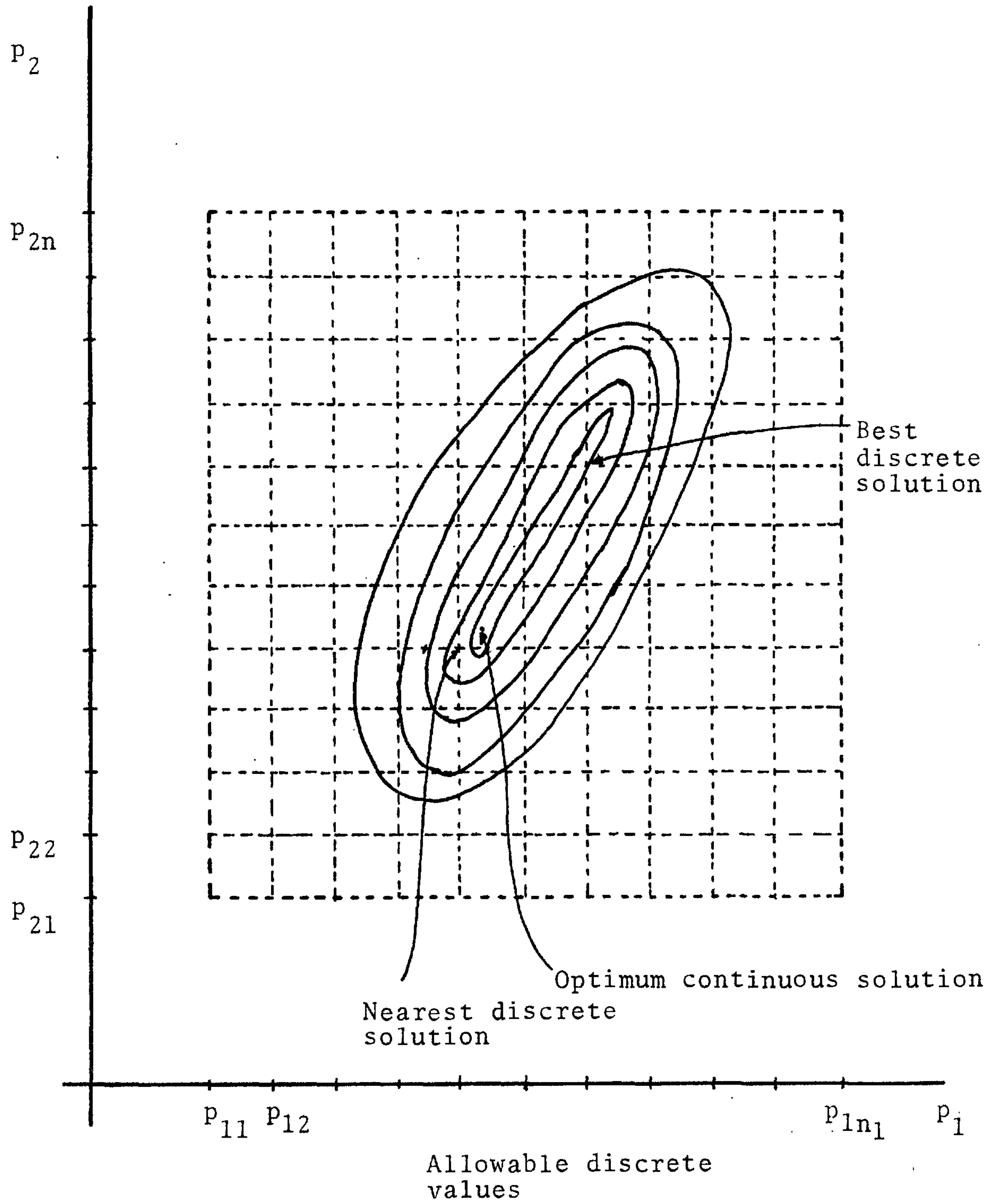


Figure 3.1 Contours For A Hypothetical Objective Function Showing That In General The Discrete Solution Nearest To The Continuous Optimum Solutions Is Not Necessarily The Best Available Discrete Solution.

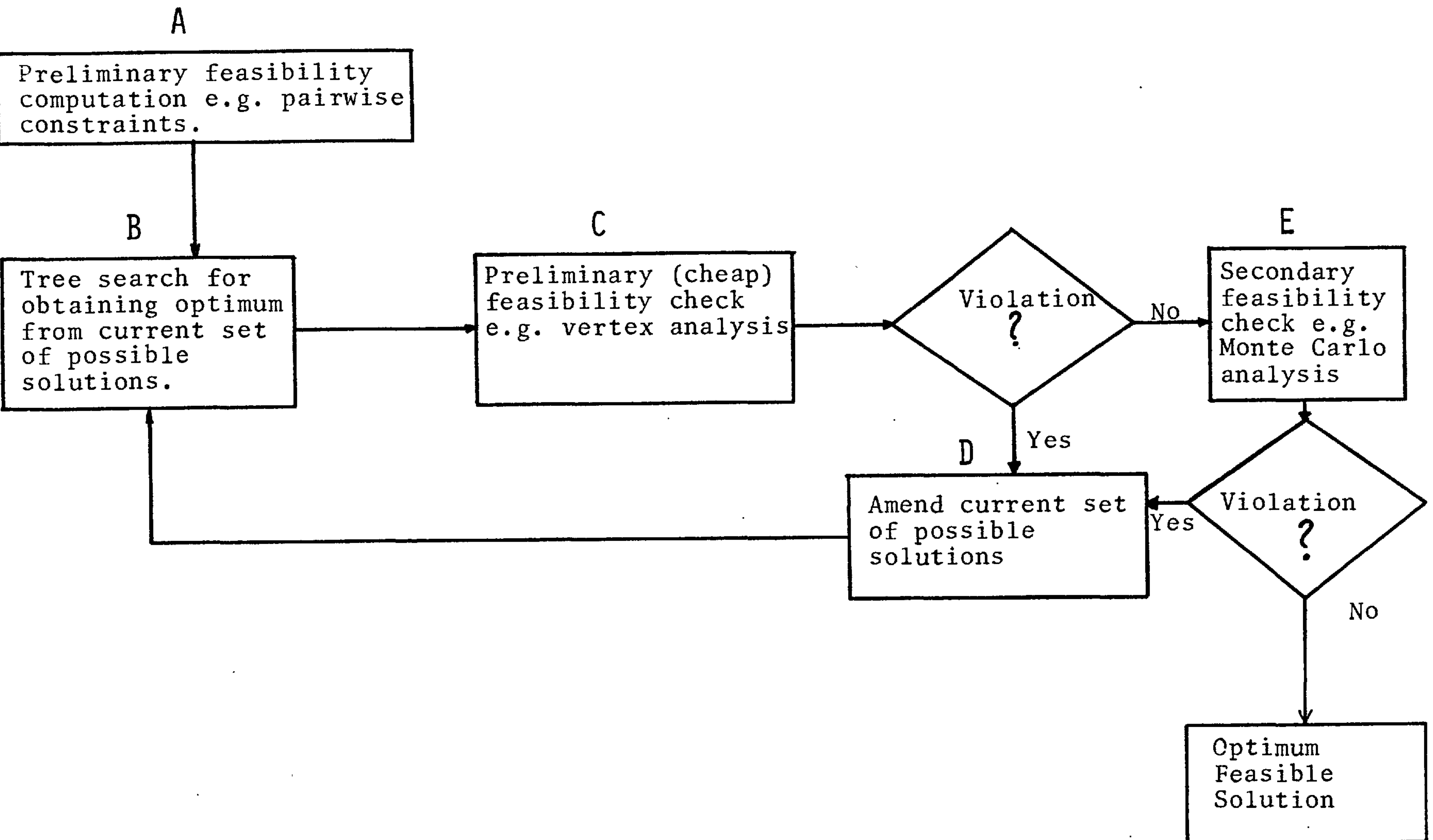


Figure 3.2: General Structure Of A Branch and Bound Method For Discrete Worst Case Tolerance Assignment

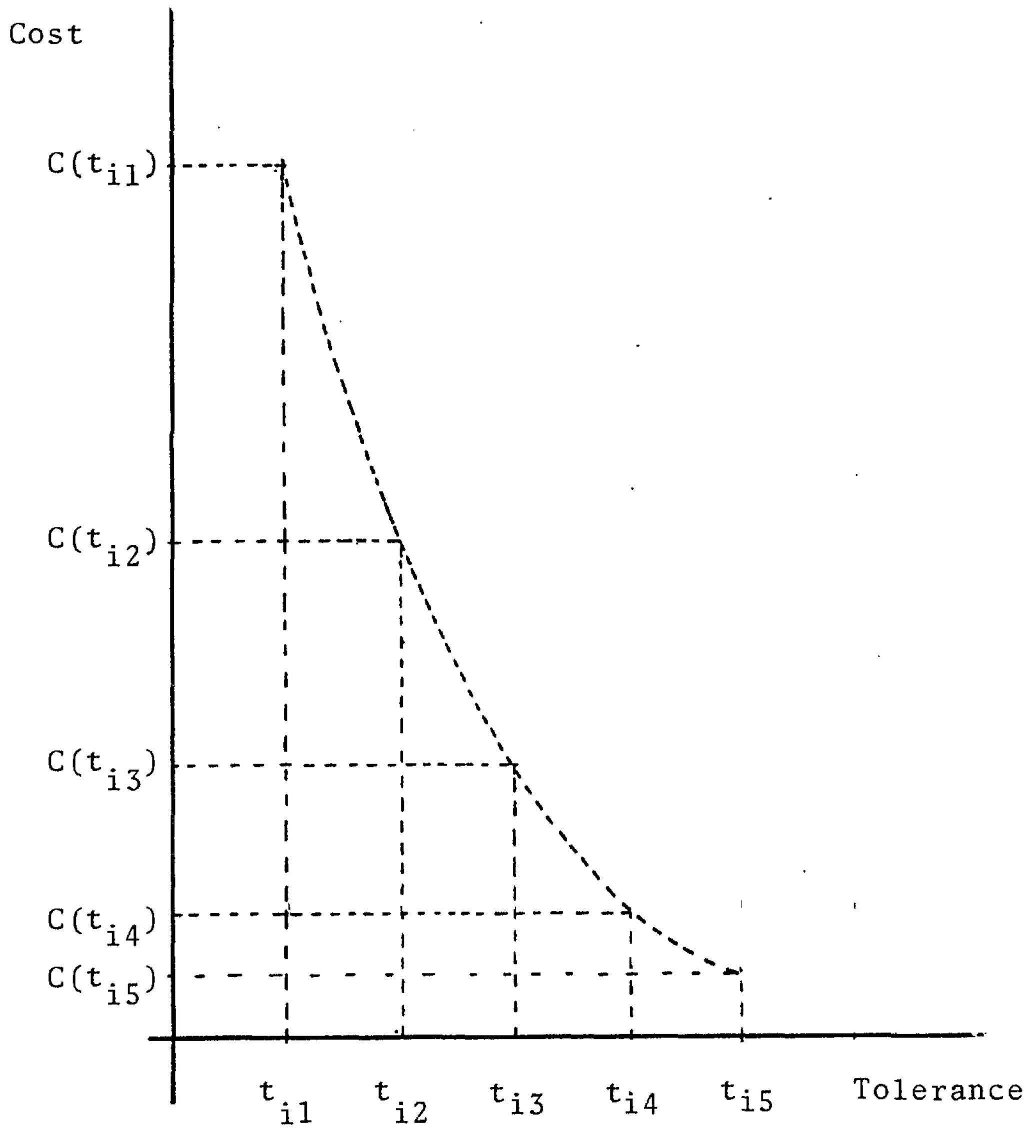
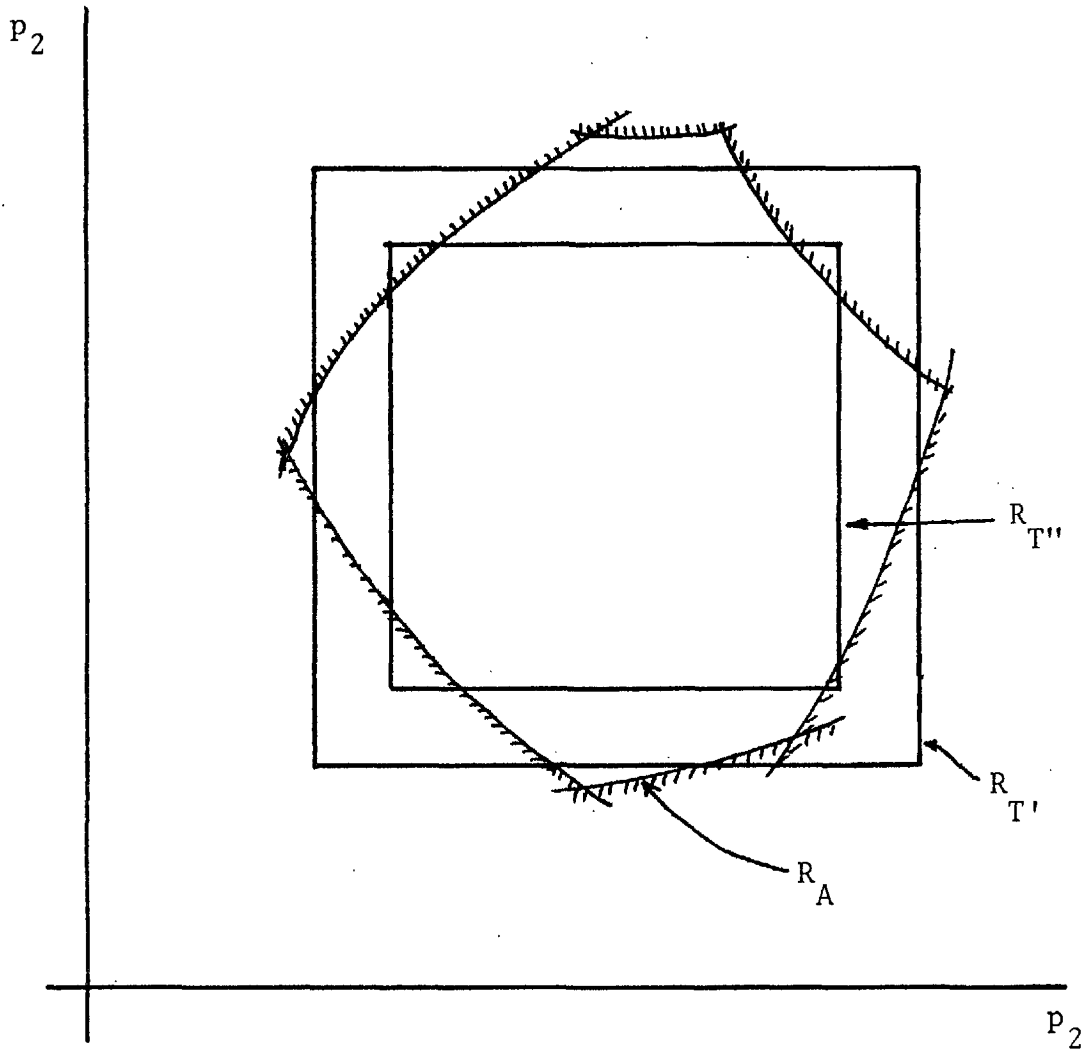


Figure 3.3 Typical Discrete Cost Versus Tolerance Relationship



Clearly $R_{T'} \not\subseteq R_A$ implies $R_{T''} \not\subseteq R_A$

Figure 3.4 Illustrating The Basis For Eliminating Certain Non Feasible Solutions In The Branch And Bound Methods For Worst Case Tolerance Assignment.

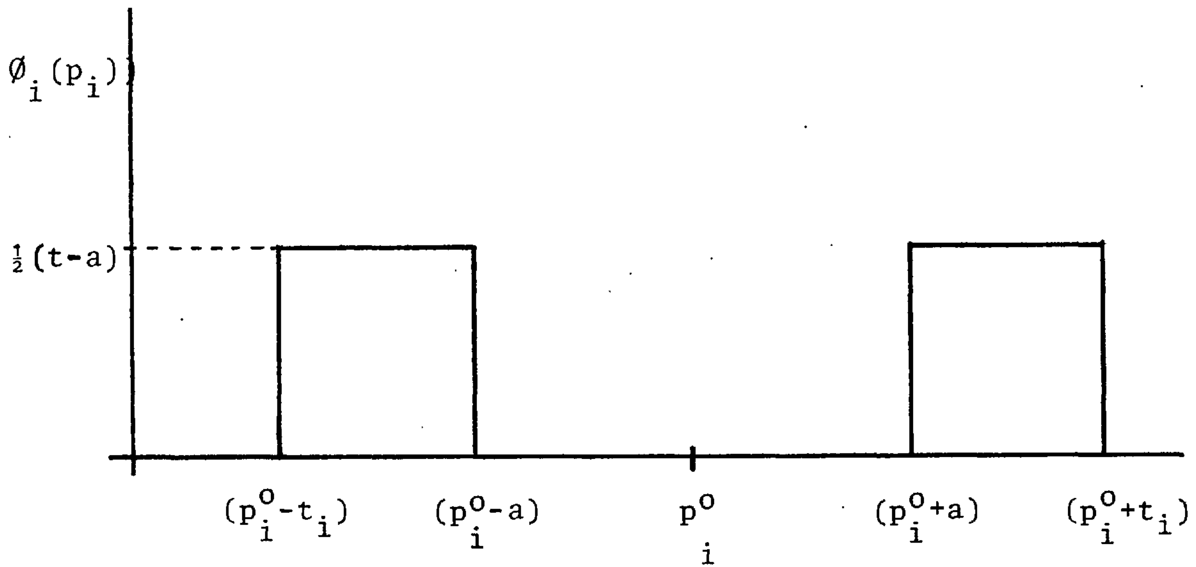


Figure 3.5 Bimodal Distribution Used In Monte Carlo Feasibility Testing.

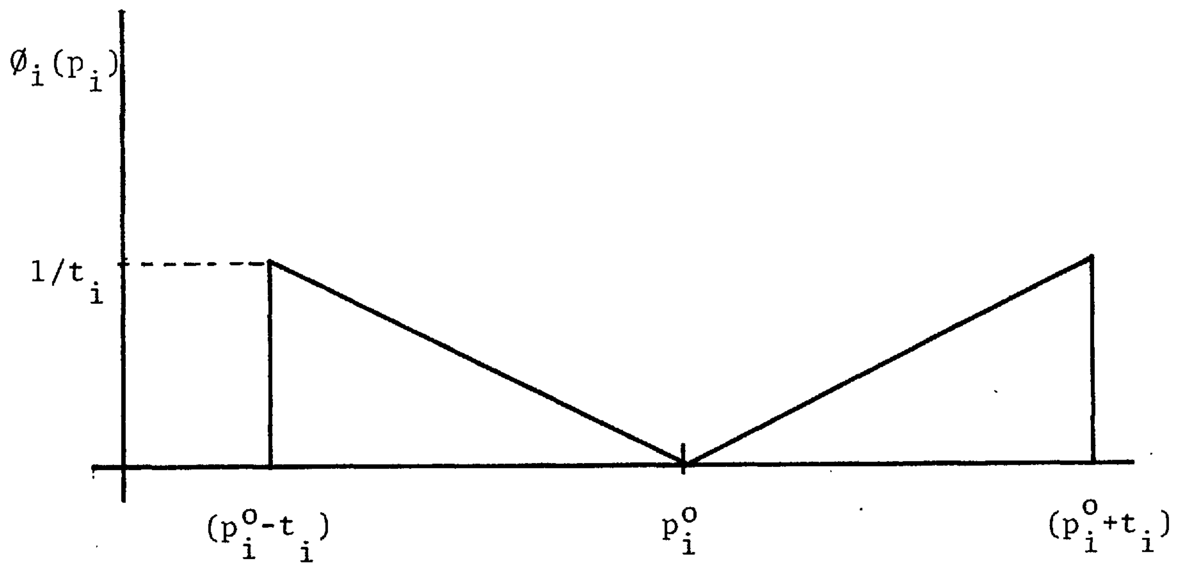
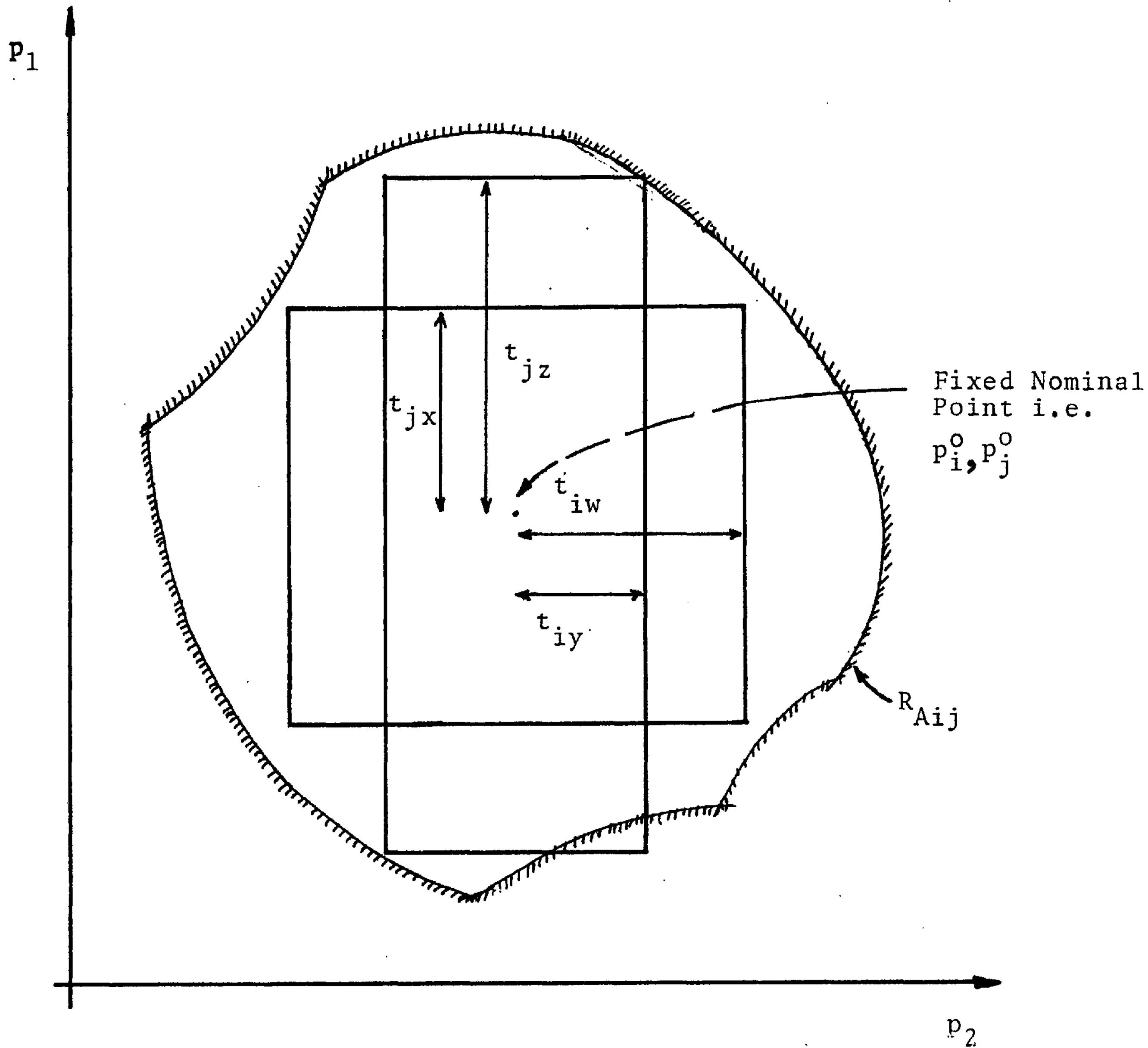


Figure 3.6 Double Triangular Distribution Used In Monte Carlo Feasibility Testing.



Two pairs of tolerances t_{iw}, t_{jx} and t_{iy}, t_{jz} are considered. Clearly t_{iw}, t_{jx} is feasible while t_{iy}, t_{jz} is infeasible.

R_{Aij} is the region of acceptability computed after setting the other (K-2) parameters at their i.e. $p_r = p_r^o$ for $r \neq i$, $r \neq j$.

Figure 3.7: An illustration of pairwise feasibility

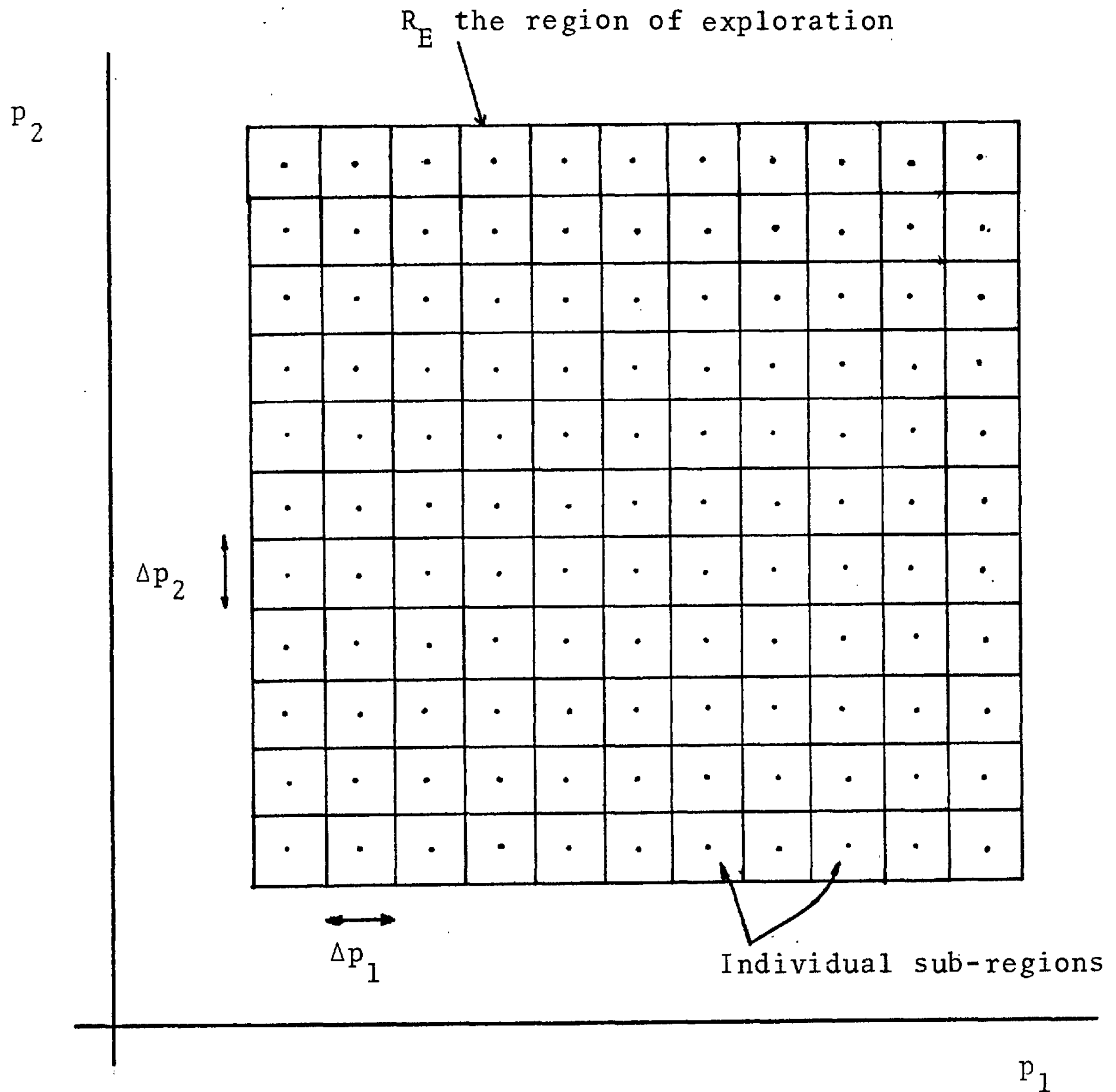
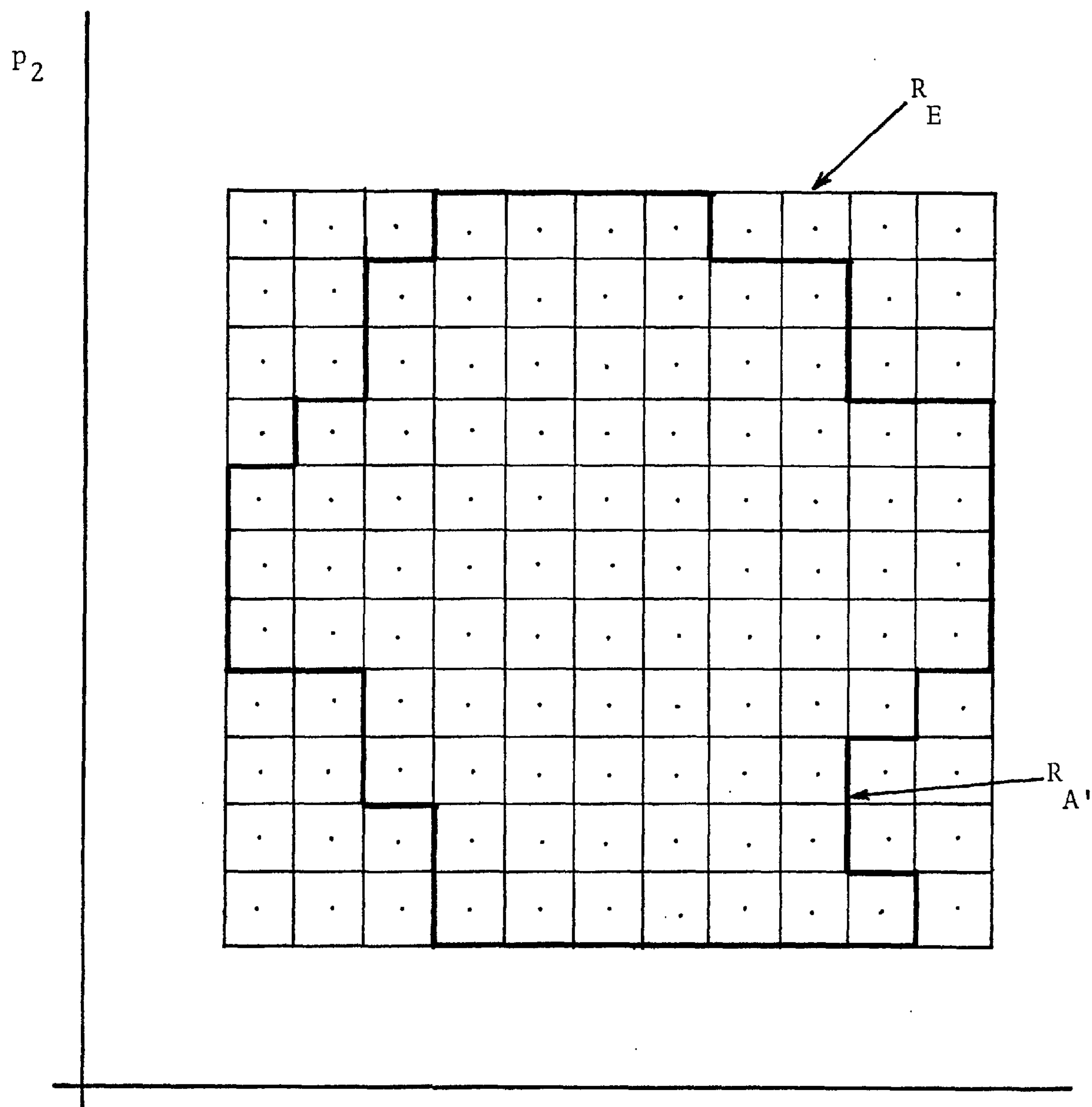


Figure 3.8 Illustrating Regionalization For A Two-dimensional Example.



Points Inside Thick Lines Pass Performance Requirements

Figure 3.9 A Discrete Representation Of The Region Of Acceptability

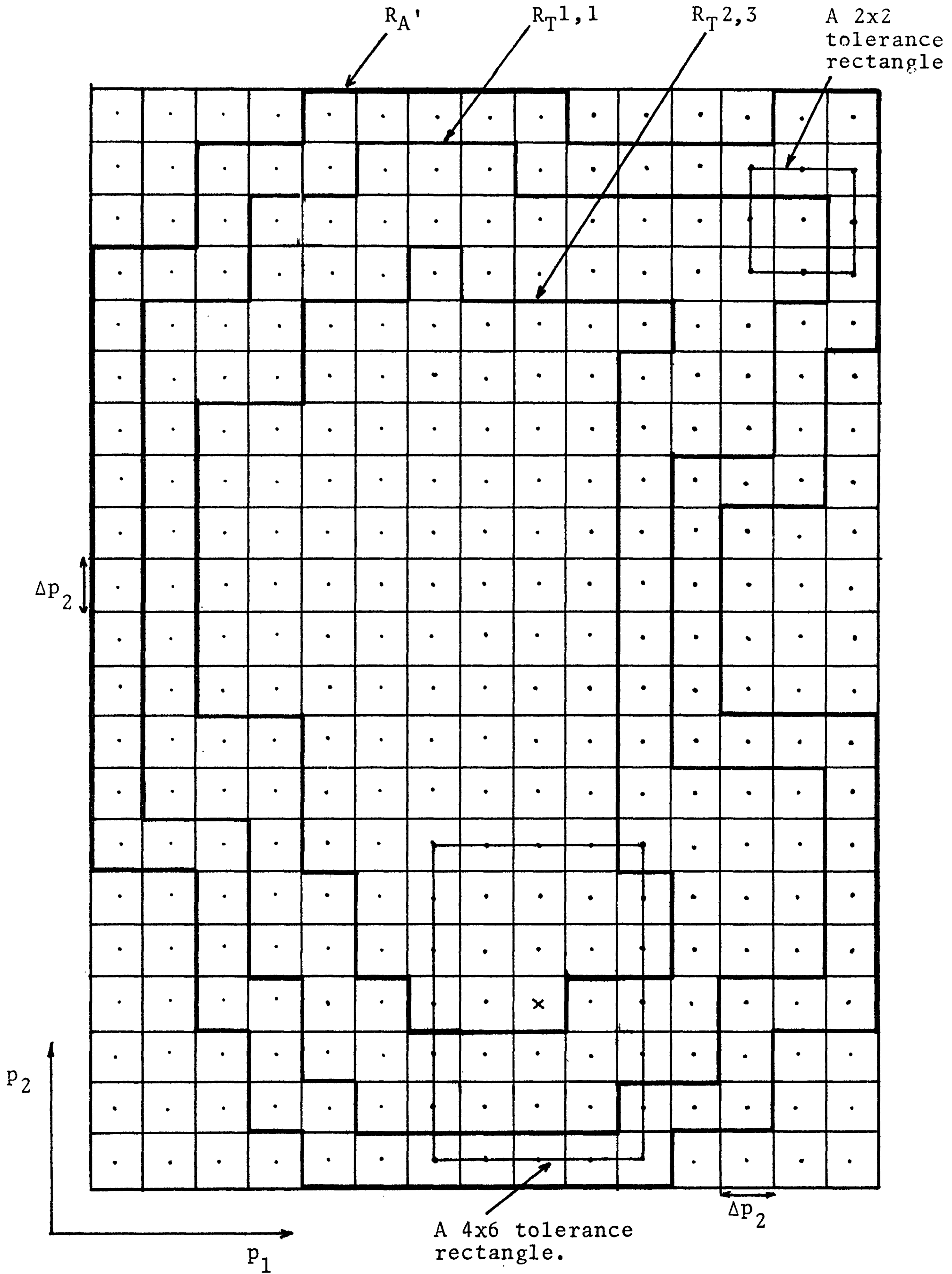


Figure 3.10 Illustrating The Basis of The Indentation Method.

```
0 0 0 0 1 1 1 1 1 0 0 0 0
0 0 1 1 1 1 1 1 1 0 0 0 0
0 1 1 1 1 1 1 1 1 1 1 0 0
1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 0
0 1 1 1 1 1 1 1 1 1 1 1 0
0 0 1 1 1 1 1 1 1 1 1 0 0
0 0 1 1 1 1 1 1 1 1 1 0 0
```

Figure 3.11 Representing The Region Of Exploration As A Matrix Of Logical Elements.

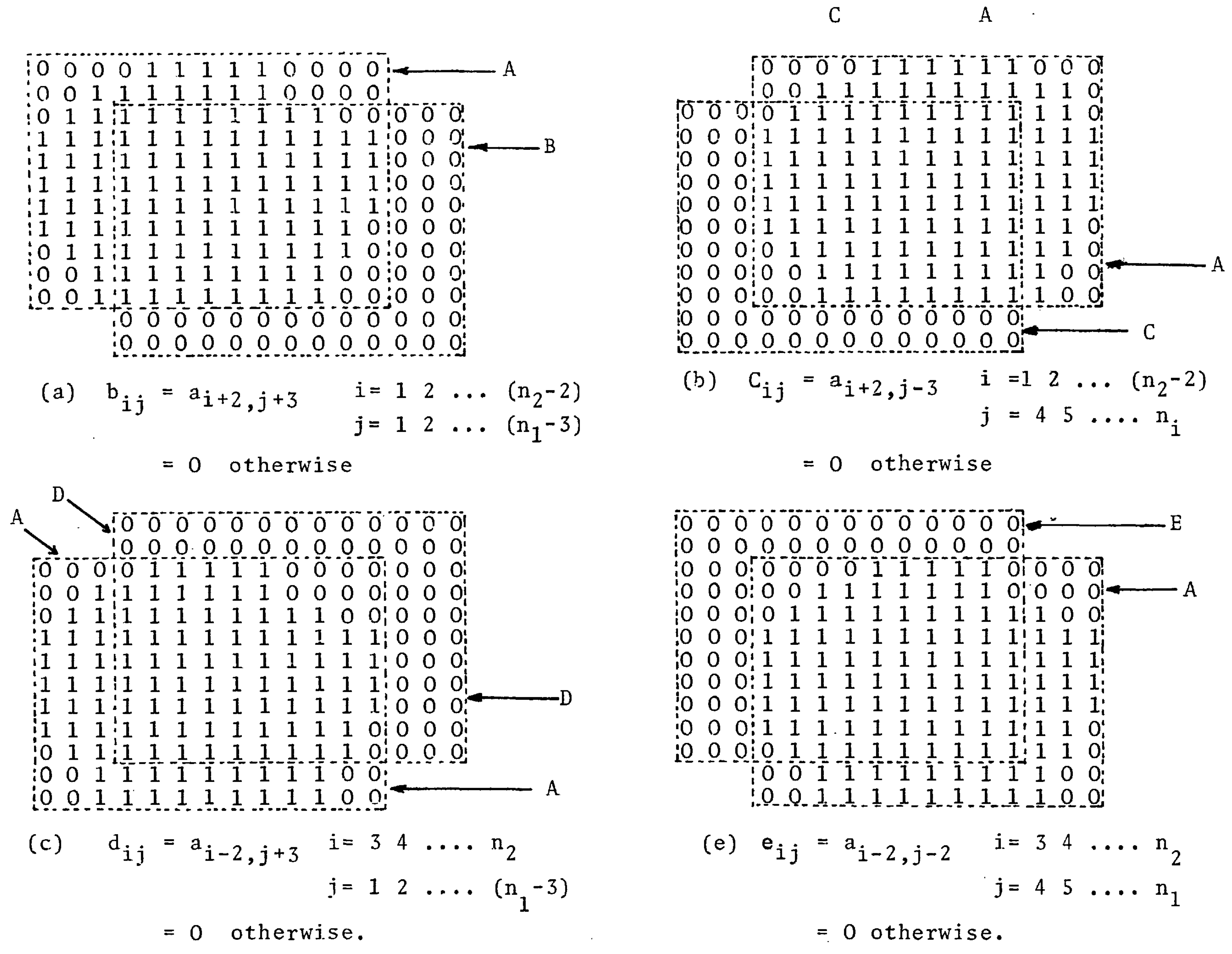
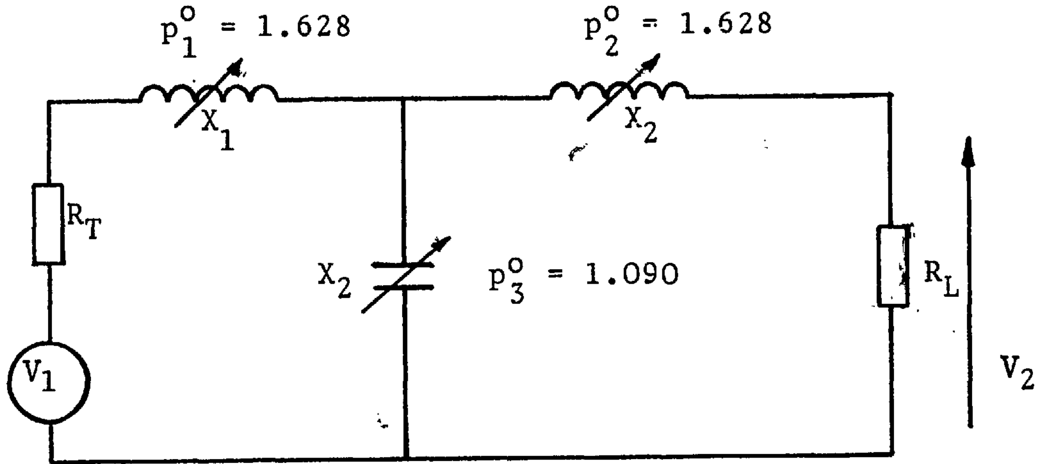


Figure 3.12 Illustrating Partial Indentation

```
0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 1 1 0 0 0 0 0 0
0 0 0 1 1 1 1 1 1 1 0 0 0
0 0 0 1 1 1 1 1 1 0 0 0 0
0 0 0 0 1 1 1 1 1 0 0 0 0
0 0 0 0 0 1 1 1 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0
```

Figure 3.12 (e)



Note: Insertion Loss is: 20 $\text{Log}|V_2(j\omega)/V_1(j\omega)|$

Figure 3.13: A Low Pass Filter Example

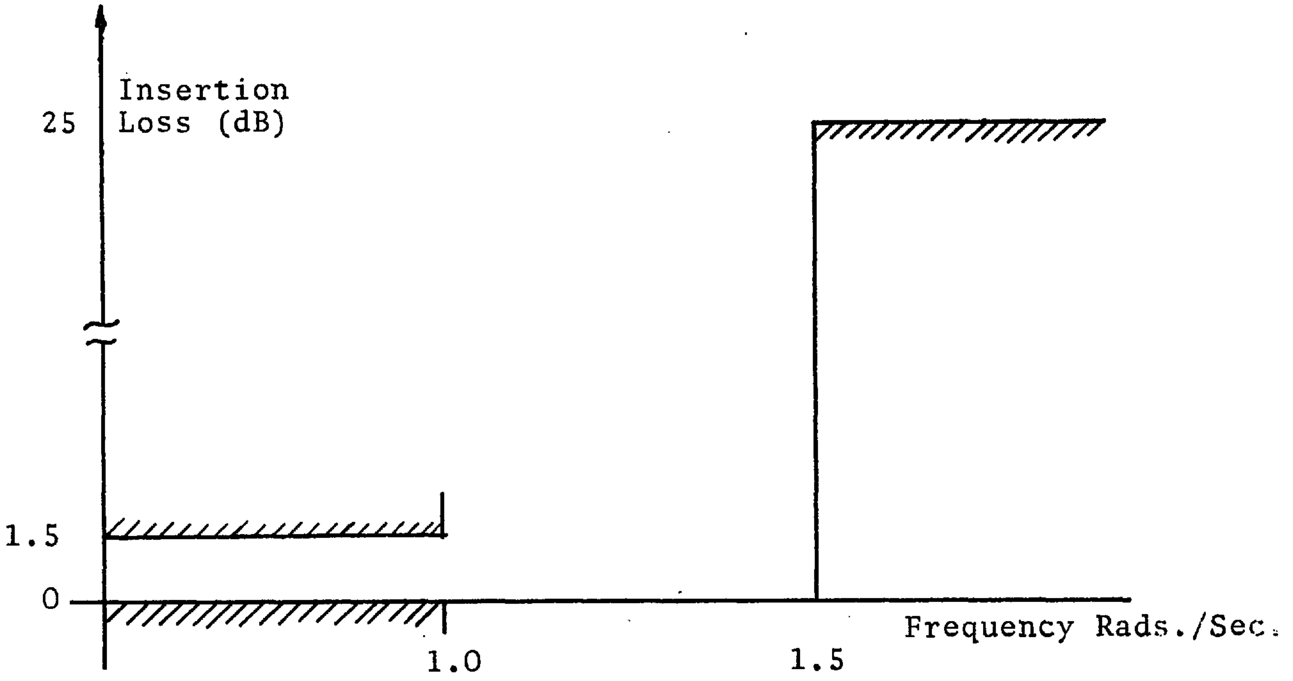


Figure 3.14: Performance Requirements For The Low Pass Filter Example.

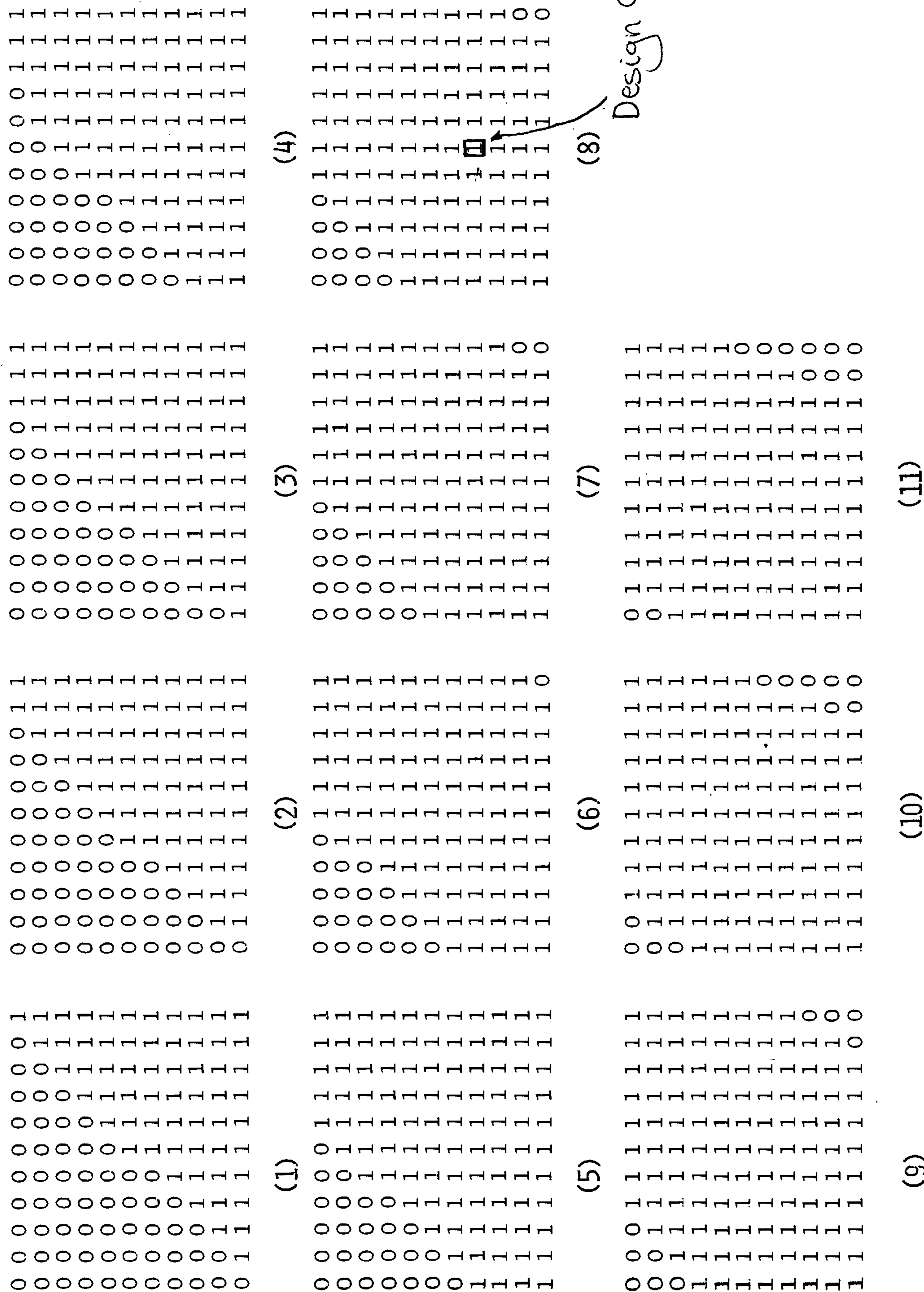


Figure 3.15 The region of acceptability of the low pass filter represented as a 3-dimensional matrix of logical element.

CHAPTER 4 - ITERATIVE MONTE CARLO BASED METHODS FOR DESIGN CENTERING.

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4.5 Summary and conclusions.

CHAPTER 4

ITERATIVE MONTE CARLO BASED METHODS FOR DESIGN CENTERING

4.1 INTRODUCTION

In chapters four and five we consider techniques where an objective function involving yield is optimized by methods based on Monte Carlo analysis. Specifically, we discuss design centering (yield maximization) in chapter four while tolerance assignment is considered in chapter five.

As discussed in chapters one and two, Monte Carlo analysis is a general procedure which can deal with any number of component parameters and performance requirements. Unlike the method of moments, the Monte Carlo method is not based on approximations of the circuit response or on assumptions of Normality (Gaussian) about the response probability density functions. In addition the number of sample circuits required to be analysed is independent of the dimensionality (number of component parameters) of the circuit. This is unlike the situation with deterministic methods such as simplicial approximation (see chapter 2), where the number of sample circuits required to be analysed increases rapidly with dimensionality.

Therefore, design methods based on Monte Carlo analysis are preferred over other methods, especially for application to circuit examples involving a large number of toleranced components.

Gradient based optimization methods /45/ are inappropriate for the design centering problem since the Monte Carlo yield estimation procedure does not evaluate the gradients of yield with respect to the nominal parameter values (design center). Therefore, attention is confined to direct search methods /45/ which do not require gradient information. However, in addition to an estimate of yield the Monte Carlo method does provide information about the distribution of passing and failing circuits in the input space. Therefore in addition to investigating the applicability of conventional direct search methods, we propose novel schemes which make use of the spatial information obtained from the Monte Carlo procedure.

4.2 PROBLEM FORMULATION AND GEOMETRICAL INTERPRETATION

The problem addressed is that of maximizing yield for fixed absolute tolerances and a particular form of component parameter p.d.f. Notationally the following unconstrained optimization problem is considered:

$$\text{Maximize} \quad Y(\emptyset\,(P^o,T)\,) \qquad 4.1$$

by appropriate choice of design center $P^o = p_1^o\, p_2^o \ldots\ldots p_K^o$, for constant tolerances $T = t_1 t_2 \ldots\ldots t_K$.

The vectors P^o and T are considered to be parameters of the component probability density function $\emptyset(.)$. For example if the component parameters are statistically independent with Gaussian distributions, then $\emptyset\,(.)$ is

the product;

$$\emptyset(.) = \prod_{i=1}^{K} \emptyset(p_i, p_i^o, \sigma_i) \qquad 4.2$$

p_i^o and σ_i are respectively the mean and standard deviation of the ith probability density function $\emptyset_i(.)$. For all practical purposes we may take $\emptyset(.)$ to be zero for $|p_i - p_i^o| > 3\sigma_i$. Therefore we can say that $t_i = 3\sigma$; i=1 ... K. Similar relationships can be defined for other forms of p.d.f.

The geometrical interpretation of design centering briefly discussed in chapter one is now expanded. Initially we reconsider certain definitions. For example the vectors P^o and T define a region in the input space, the tolerance region $R_T(P^o,T)$, such that for

$$P = p_1 p_2 \ldots\ldots p_K$$

$$P \varepsilon R_T \text{ if } (p_i^o - t_i) < p_i < (p_i^o + t_i) \qquad i=1 \ldots\ldots K \qquad 4.3$$

The function $\emptyset(P,P^o,T)$ is defined over the tolerance region and is zero otherwise. Further since $\emptyset(.)$ is a p.d.f., we have

$$\int_{p_K^o - t_K}^{p_K^o + t_K} \cdots \int_{p_1^o - t_1}^{p_1^o + t_1} \emptyset(P,P^o,T)\, dp_1 dp_2 \ldots\ldots dp_K = 1 \qquad 4.4$$

We re-iterate the definitions of yield and region of acceptability.

$$\text{Yield} \triangleq \int_{p_K^o - t_K}^{p_K^o + t_K} \cdots \int_{p_1^o - t_1}^{p_1^o + t_1} g(P)\emptyset(P,P^o,T)\, dp_1\, dp_2 \ldots dp_K \qquad 4.5$$

As before g(P) denotes a testing function whose value is unity if the circuit with component values P satisfies all performance requirements, and is zero otherwise. The region of acceptability R_A is then defined as:

$$R_A \triangleq \{P | g(P) = 1\} \qquad 4.6$$

It is profitable to reconsider the geometrical interpretation of yield. Figure 4.1 illustrates the definitions for the case where the dimensionality K, is two. Initially, we take $\emptyset(P,P^o,T)$ to be a multivariate uniform p.d.f: i.e.

$$\emptyset(P,P^o,T) = \prod_{i=1}^{K} \frac{1}{2t_i} \quad \text{for } P \varepsilon R_T \qquad 4.7$$

$$= 0 \text{ otherwise.}$$

Then with notation $V\{R_x\}$ meaning volume of region R_x, yield is the following ratio of volumes:

$$Y(\emptyset(.)) = \frac{V\{R_T(P^o) \cap R_A\}}{V\{R_T(P^o)\}} \qquad 4.8$$

For the situation where the p.d.f. $\emptyset(.)$ is other than uniform, the function $\emptyset(P,P^o,T)$ may be taken to define a weighting of every point in R_T. Therefore notation $V\{R_x\}$ in equation 4.8 should now be taken to mean the volume of region R_x weighted according to the function $\emptyset(.)$. As a consequence of definition 4.3 and equation 4.4, the value of the denominator in equation 4.8 will have a constant value irrespective of the design center P^o. Therefore a geometrical interpretation of design centering is to find a center P^o_* for the tolerance region R_T, such that the volume $V\{R_T(p^o_*) \cap R_A\}$ is maximized.

In practice design centering can be treated as an unconstrained optimization problem. The most commonly occurring constraints on parameter values will be box constraints /46/. One example of a box constraint is the non-negativity condition, $p_i^o > 0$; i=1 .... K. Other common examples are the constraints imposed by the limits of the technological processes used to make the components. For example it may be required that the resistors in planar integrated circuits be less than a certain maximum value (typically 20KΩ). Nevertheless, in almost all practical problems these constraints are never encountered in the search for an optimal design center.

4.3 OPTIMIZATION METHODS FOR YIELD MAXIMIZATION - SOME GENERAL COMMENTS

Yield as defined in equation 4.5 is a multidimensional integral, where the dimensionality is equal to the number of component parameters subject to variation. For circuits of realistic size and complexity, the integral cannot be computed by a deterministic numerical method such as quadrature. This difficulty is unresolved with a geometrical approach, as the computational effort required to characterize the regions R_A or $R_T \cap R_A$ is prohibitive for most circuit examples.

In chapter one we have described a computationally cheap statistical method, namely the method of moments. However, we re-iterate that the approximations inherent in this method make it unsuitable for most applications.

In practice Monte Carlo analysis has to be employed to estimate yield. However, Monte Carlo analysis is computationally expensive and it is therefore unattractive to use it prodigiously in any adaptation of conventional iterative optimization methods. Nevertheless, Monte Carlo analysis can deal with circuit examples comprising any number of components and performance requirements. Further, it does not require simplifying approximations and assumptions. Therefore, we consider methods which make prudent use of all the information generated in the Monte Carlo analysis and which moderate the computational effort by employing efficient sampling schemes.

A confidence interval is associated with each Monte Carlo estimate of yield. The true yield is expected to occur inside this interval with a certain degree of confidence. When the Monte Carlo method is used iteratively, the confidence interval associated with the yield estimates at different iterates may overlap. Therefore a situation could arise where the estimated yield for a particular iterate was greater than that of another iterate, when the true yield was not so. Therefore it is important to consider the confidence of correctly ranking iterates. That is, the degree of confidence in asserting that the true yield associated with one iterate is greater than that associated with the other.

The extent of the confidence intervals associated with the yield estimates and the confidence of correctly ranking iterates depend upon the number of sample circuits analysed in the Monte Carlo analyses. In general it requires a smaller number of samples to have a high confidence of correct

ranking than to attain small confidence intervals. Also, in the intermediate stages of the optimization, it is sufficient to correctly rank iterates, whereas the accuracy of the yield estimate becomes important for the final iterate.

Later in this chapter the basis for computing the confidence of correct ranking will be discussed. We shall also consider special sampling schemes, which while giving sufficient confidence of correct ranking, reduce considerably the sample sizes below those required for a direct iterative application of Monte Carlo analysis.

In considering the applicability of standard optimization methods to the maximization of yield, it is noted that Monte Carlo analysis does not provide gradients of the yield with respect to the design variables, i.e. p_1^o p_2^o .... p_K^o. Further, no tractable numerical methods are available for the computation or estimation of such gradients. Hence gradient based methods are inappropriate. Therefore we consider direct search methods, which in contrast do not require gradient information.

4.4 DIRECT SEARCH METHODS

All numerical optimization methods involve iterative procedures where the objective function is evaluated at difference points (trial solutions) in the input space, until a maximum (or minimum) is obtained. Direct search methods are a class of optimization method where a trial solution is determined by a strategy which considers the

position of a number of previous trial solutions and the values of the objective function at these points. The gradients of the objective function with respect to the design variables are not required to determine the next trial solution.

Two specific direct search methods are considered for the problem of maximizing yield. Firstly, we discuss a standard method, namely Pattern search /34/. Secondly, we propose a novel technique called "statistical exploration". In choosing trial solutions, the latter method uses information about the position of pass and fail circuits generated by Monte Carlo analysis.

The optimization process involves a number M of trial solutions, P_1^o, P_2^o .... P_M^o, with associated tolerance regions R_{T1}, R_{T2} .... R_{TM}. As before, region R_{Tj} is a hyper-rectangle centered about the point P_j^o. The sides of R_{Tj} are of lengths $2t_i$, i=1 .... K. In addition we let $\tilde{Y}_j$ denote an estimate of the true yield Y_j associated with the design center P_j^o. The estimate $\tilde{Y}_j$ is obtained via a Monte Carlo analysis with a sample size of N_j.

In the initial discussion, it is assumed that the sample sizes provide adequate confidence of correct ranking. The question of sample size is relevant to all Monte Carlo based methods and is taken up in section 4.4.2.

4.4.1 THE PATTERN SEARCH METHOD

Becker and Jensen /12/ report the application of the pattern search method to the yield maximization problem. The method

takes the form of alternative application of "exploratory" and "pattern" moves as summarized in figure 4.2.

Let $P_1^o = p_{11}^o\ p_{12}^o\ \ldots\ldots\ p_{1K}^o$ be the starting point with associated yield estimate Y_1. We refer to P_1^o as the first base point and additionally denote it as P_{B1}. To commence the procedure, the value p_{11}^o is incremented by a specific amount Δp_1 and yield is re-estimated. If the yield increases then $p_{11}^o + \Delta p_1$ is accepted as the new value of p_1^o; otherwise p_{11}^o is decremented by Δp_1 and yield is re-estimated. If yield is now found to increase, then $p_{11}^o - \Delta p_1$ is accepted as the new value of p_1^o. If neither perturbation results in an increase of yield over Y_1, then the value of p_1^o is left unchanged.

Let us assume that an increment of the value of p_1^o resulted in an increase in yield. Then in our notation, we have $P_2^o = (p_{11}^o + \Delta p_1)\ p_{12}\ p_{13}\ \ldots\ p_{1K}$. We now begin to explore the effect on yield of changes to the value of the second component p_2^o. We increment the value p_{12}^o by Δp_2 and re-estimate yield , so that we are now estimating yield for design center $P_3 = (p_{11}^o + \Delta p_1)(p_{12} + \Delta p_2)p_{13}^o\ \ldots\ldots\ p_{1K}^o$. The yield Y_3 is now compared with yield Y_2. If no increase in yield is obtained then the value of P_2^o is decremented and yield is re-evaluated. If neither perturbation results in an increase in yield, then the value of p_2^o is left unchanged at p_{12}^o. These perturbations and yield estimations are carried out for each parameter in turn, and constitute the exploratory moves. At the end of the exploratory moves we get a new point P_{B2}, i.e. the second base point.

The line joining the new base point P_{B2} with the initial base point P_{B1} forms the direction of movement. A pattern move is made by extending this line from the first base point to the second base point by doubling its length. The end of this line forms the third base point from which the exploratory moves are restarted.

If the exploratory moves do not produce an increase in yield, then the sizes of the perturbations Δp_i, i=1 ... K, are reduced and the process is restarted from the previous base.

The procedure involving alternative application of exploratory moves and pattern moves is continued until no further increase in yield are obtained.

A hypothetical trajectory for a two dimensional example is illustrated in figure 4.3. The trial solutions are numbered 1 to 27. The thin lines depict exploratory moves, while the thick lines indicate pattern moves. Among the thin lines, the broken ones indicate exploratory moves which did not lead to an increase in yield. The exploratory moves around base point P_{B7} do not lead to an increase in yield. Therefore the procedure reverts to the previous base point and re-commences the exploratory moves, but with smaller perturbations.

Application of the pattern search method has been reported for the three transistor amplifier circuit shown in figure 4.4. The design variables are the nominal values of the resistors R_2 to R_7. Each resistance has an associated tolerance of 10% of the initial values. The probability density function for each parameter is taken to be unform. The circuit performance

constraints are shown in table 4.1. Table 4.2 shows the results obtained for one of the yield maximization runs. This example is reproduced here for comparison with the results of the statistical exploration method described below.

4.4.2 THE STATISTICAL EXPLORATION METHOD

This method takes advantage of the exploratory spatial information generated by the Monte Carlo yield estimation procedure. To appreciate this, we recall the geometrical interpretation of design centering as maximizing the volume of the region of intersection $R_T \cap R_A$.

In the Monte Carlo estimation of yield, circuits (points in R_T) are randomly generated, analysed, and tested against performance requirements. For each analysed circuit, we know its position in the tolerance region, and whether or not it belongs to the region of acceptability. Therefore, Monte Carlo analysis identifies points generated in regions $R_T \cap R_A$ and $R_T \cap \bar{R}_A$. This information can be used efficiently for design centering.

A general flow chart of the method is shown in figure 4.5. The procedure is iterative. From a particular trial solution P_j^o with associated yield estimate $\tilde{Y}_j$, a new trial solution P_{j+1}^o is sought such that

$$V(R_{T,j+1} \cap R_A) > V(R_{T,j} \cap R_A) \qquad 4.10$$

The new trial solution P_{j+1}^o may be written as:

$$P_{j+1}^o = P_j^o + \lambda_j \Delta P_j \qquad 4.11$$

Clearly every point in R_{T_j} is moved in a direction parallel to ΔP_j by an amount $\lambda_j |\Delta P_j|$ to form $R_{T,j+1}$. This is illustrated in figure 4.6.

(a) Choice Of Search Direction

From geometrical considerations, e.g. figure 4.6, we surmise that an effective search direction will be the direction parallel to the line joining the centers of gravity of the acceptable and reject regions. That is, the search direction ΔP_j given by:

$$\Delta P_j = G_{Aj} - G_{Rj} \qquad 4.12$$

More precisely, G_{Aj} and G_{Rj} are the centers of gravity of regions $(R_{Tj} \cap R_A)$ and $(R_{Tj} \cap \overline{R}_A)$ which have been weighted according to the relevant p.d.f. $\emptyset(.)$.

After performing Monte Carlo analysis, the centers of gravity are estimated as follows.

Let N be the total number of sample circuits analysed. Let N_A be the number which pass all performance requirements. Then yield is estimated as $\tilde{Y} = \frac{N_A}{N}$. Clearly the number of circuits which fail at least one performance requirement will be $(N-N_A)$. Further, let $P = p_1^\ell \; p_2^\ell \; .... \; p_K^\ell$ represent the component values of the ℓth analysed circuit. In addition let the N_A acceptable circuits be numbered from 1 to N_A and the $(N-N_A)$ reject circuits from (N_A+1) to N. Then the co-ordinates g_{Aj}^i and g_{Rj}^i ; i=1 .... K, of G_{Aj} and G_{Rj}, are estimated as:

$$g_{Aj}^i = \frac{1}{N_A} \sum_{\ell=1}^{N_A} p_i^\ell \qquad i=1 \; .... \; K \qquad 4.13$$

and

$$g^i_{RJ} = \frac{1}{(N-N_A)} \sum_{N_A+1}^{N} p^\ell_i \quad i=1 \;....\; K \qquad 4.14$$

For the sake of rigour, definitions of the centers of gravity G_{Aj} and G_{Rj} are given in equations 4.15 and 4.16.

$$g^i_{Aj} = \frac{\int_{R_{Tj} \cap R_A} p_i \emptyset(P^o_j)\, dp_1 \;.....\; dp_K}{\int_{R_{Tj} \cap R_A} \emptyset(P^o_j)\, dp_1 \;.....\; dp_K} \qquad 4.15$$

And

$$g_{Rj} = \frac{\int_{R_{Tj} \cap \bar{R}_A} p_i \emptyset_i(P^o_j)\, dp_1 \;.....\; dp_K}{\int_{R_{Tj} \cap \bar{R}_A} \emptyset(P^o_j)\, dp^o_1 \;.....\; dp_K} \qquad 4.16$$

Clearly the quantities defined in 4.13 and 4.14 are estimates of the quantities defined in 4.15 and 4.16.

(b) Choice Of Step Size

In view of the computational cost of Monte Carlo analysis, it is inadvisable to perform a unidirectional search for maximum yield along the search direction ΔP_j. We are content with any value of λ_j (and hence P^o_{j+1} through equation 4.11) such that the resulting yield Y_{j+1} is greater than the current yield Y_j.

Since little is known about the shape of typical regions of acceptability, very precise rules for the choice of λ cannot be obtained. However, prudent constraints on the choice of λ may be derived from the following qualitative development. Consider figure 4.6 depicting the tolerance

regions for successive design centers P^o_j and P^o_{j+1}. The following additional notation is introduced.

Region A	$\triangleq R_T(P^o_j) \cap \overline{R}_T(P^o_{j+1})$	That part of R_{Tj} not overlapped by $R_{T,j+1}$
Region B	$\triangleq R_T(P^o_j) \cap R_T(P^o_{j+1})$	The overlap region.
Region C	$\triangleq \overline{R}_T(P^o_j) \cap R_T(P^o_{j+1})$	That part of $R_{T,j+1}$ not overlapped by R_{Tj}

For convenience, this notation is illustrated in figure 4.7.

Initially, all the component parameters are assumed to be independent and uniformly distributed. Notation V_X denotes the volume of region X. Then the two yields of interest may be written as:

$$Y_j = \frac{V_{(A\cup B)\cap R_A}}{V_{R_T}} \tag{4.18}$$

and

$$Y_{j+1} = \frac{V_{(B\cup C)\cap R_A}}{V_{R_T}} \tag{4.19}$$

Also let ΔY_j denote the difference between yields Y_{j+1}. That is,

$$\Delta Y_j = Y_{j+1} - Y_j$$

$$= \frac{V_{(B\cup C)\cap R_A} - V_{(A\cup B)\cap R_A}}{V_{R_T}}$$

$$= \frac{V_{C\cap R_A} - V_{A\cap R_A}}{V_{R_T}} \tag{4.20}$$

Consider now a limit case in which (a) 100% yield can be achieved with the given tolerances and (b) one step in the iteration causes 100% yield to be obtained. These conditions imply that $Y_{j+1} = 1$ and hence $V_{C \cap R_A} = V_C$ and $\Delta Y_j = 1 - Y_j$. Equation 4.20 may be re-written as

$$\frac{V_C - V_{A \cap R_A}}{V_{R_T}} = 1 - Y_j \qquad 4.21$$

However, $V_C = V_A = V_{R_T} - V_B$ and hence (4.21) may be replaced by:

$$\frac{(V_{R_T} - V_B) - V_{A \cap R_A}}{V_{R_T}} = 1 - Y_j \qquad 4.22$$

In practice the maximum obtainable yield is often less than 100% and cannot be achieved in one iteration. Therefore the equality in 4.22 is replaced by an inequality. Further, for any particular V_B, the left hand side of 4.22 is maximized if $V_{A \cap R_A} = 0$. Therefore we obtain:

$$\frac{V_{R_T} - V_B}{V_{R_T}} < 1 - Y_j \qquad 4.23$$

Also $V_B = \prod_{i=1}^{K} (2t_i - \lambda_j \Delta p_i)$, where Δp_i is the ith co-ordinate of ΔP, and $V_{R_T} = \prod_{i=1}^{K} 2t_i$. Therefore substituting for V_{RT} and V_B in 4.23, we get:

$$\frac{\prod_{i=1}^{K} 2t_i - \prod_{i=1}^{K} (2t_i - \lambda_j \Delta p_i)}{\prod_{i=1}^{K} 2t_i} < (1 - Y_j) \qquad 4.24$$

Alternately, this may be written as:

$$\frac{\prod_{i=1}^{K} (2t_i - \lambda_j \Delta p_i)}{\prod_{i=1}^{K} 2t_i} > Y_j \qquad 4.25$$

The tolerances t_i are given constants and the Δp_i are co-ordinates of ΔP_j, the search direction. Therefore inequality (4.25) constitutes a constraint on the value of λ_j. Although λ_j cannot be explicitly written in terms of the other quantities, relationship (4.25) is essentially an upper bound on the value of λ_j. This is so because the value of the expression on the left hand side of 4.25 monotonically decreases with increasing value of λ_j.

Inequality 4.25 is also of importance in the common points sampling scheme to be discussed later. We note that region B is the region common to successive tolerance regions. Moreover the left hand side of 4.25 is simply the ratio of the volume of the common region to the volume of the entire tolerance region, i.e. V_B/V_T. Therefore, the above qualitative argument has shown that for a particular choice of search direction ΔP, the step size λ should be chosen such that the common volume ratio is greater than the yield for the current iterate.

So far the arguments for choice of step size have assumed uniform distributions. A parallel development is not provided for non-uniform distributions. However, in practice and especially for the choice of Gaussian distributions, choices of λ based on 4.25 have been found to be very effective for design centering.

The statistical exploration algorithm has been implemented as a part of an interactive statistical design facility, where the choice of step size is made by the human designer. Further discussion of criteria for choice of step size will be presented in the respective sections dealing with algorithm implementation and with specific circuit examples.

(c) Choice of Sample Size

Computational cost is largely dependent on the total number of sample circuits tested in the Monte Carlo analyses. The sample sizes also determine the extent of the confidence intervals associated with individual yield estimates and the confidence of correctly ranking iterates. In the intermediate stages of the optimization, the correct ranking of iterates is of greater importance while the accuracy of the yield estimate becomes significant for the final design center. We first discuss the dependence on sample size both of correctly ranking estimates and of the extent of the confidence intervals. Then two sampling schemes are introduced, which for a particular sample size increase the confidence of correct ranking.

From chapter one, we recall that for an N sample Monte Carlo analysis, where NA circuits are found to be acceptable, yield is estimated as $\tilde{Y} = NA/N$. The sampling distribution of $\tilde{Y}$ is Binomial, which for reasonably large N can be approximated by a Gaussian distribution with mean $\mu = \tilde{Y}$ and variance $\sigma^2 = \tilde{Y}(1-\tilde{Y})/N$. The sampling distribution is sketched in figure 4.8. Confidence statements may then be made about Y. For example 95% of the total area under

the Gaussian curve is within $\mu \pm 2\sigma$, which is hence the 95% confidence interval.

Now consider yield estimates $\tilde{Y}_j$ and $\tilde{Y}_{j+1}$ for successive iterates P_j^o and P_{j+1}^o respectively. As before ΔY_j denotes the difference between the two yields, i.e. $\Delta Y_j = Y_{j+1} - Y_j$. Having performed two Monte Carlo analyses, we can estimate $\Delta\tilde{Y}_j$ as the difference between the two yield estimates, i.e.

$$\Delta\tilde{Y}_j = \tilde{Y}_{j+1} - \tilde{Y}_j \qquad 4.26$$

The sampling distribution of $\Delta\tilde{Y}_j$ is also Gaussian because $\Delta\tilde{Y}_j$ is the difference between two Gaussian distributed random variables. In addition, the variance $\sigma^2_{\Delta Y_j}$ of the sampling distribution of $\Delta\tilde{Y}_j$ is related to the variances $\sigma^2_{Y_j}$ and $\sigma^2_{Y_{j+1}}$ of estimates $\tilde{Y}_j$ and $\tilde{Y}_{j+1}$ according to 4.27.

$$\sigma^2_{\Delta Y_j} = \sigma^2_{Y_j} + \sigma^2_{Y_{j+1}} - 2\ \mathrm{COV}\ (\tilde{Y}_j, \tilde{Y}_{j+1}) \qquad 4.27$$

$\mathrm{COV}\ (\tilde{Y}_j, \tilde{Y}_{j+1})$ is the covariance between the two yield estimates $\tilde{Y}_j$ and $\tilde{Y}_{j+1}$.

The sampling distribution of $\Delta\tilde{Y}_j$ is sketched in figure 4.9(a), where the estimated yield difference is assumed positive. The degree of confidence in the assertion that the true yield difference ΔY_j is positive when the estimated yield difference $\Delta\tilde{Y}_j$ is positive, is the area under the curve to the right of the abscissa, i.e. the shaded area. This area is equal to $\frac{1}{2} + \mathrm{erf}\ (\Delta\tilde{Y}/\sigma_{\Delta Y})$,

where erf(.) is the error function defined below.

$$\operatorname{erf}(x) = \frac{1}{\sqrt{2\pi}} \int_0^x \exp - t^2/2 \; dt.$$

The value of the error function and hence that of the confidence of correct ranking increases monotonically with the value of the argument $\Delta\tilde{Y}/\sigma_{\Delta Y}$. Therefore the confidence of correct ranking is increased either if $\Delta\tilde{Y}$ is large or if $\sigma^2_{\Delta Y}$ is small. Qualitatively, the shaded area (in figure 4.9a) will be increased either if the curve is squeezed inwards, i.e. there is a smaller variance, or if the whole curve is shifted to the right, i.e. there is a greater difference in yield. The two situations are described in figure 4.9(b) and 4.9(c) respectively.

We now describe two sampling schemes which, for a particular sample size, increase confidence by attempting each of the above two alternatives. One, correlated sampling, decreases $\sigma_{\Delta Y}$; the other, the common points scheme, increases $\Delta\tilde{Y}$.

(d) The Correlated Sampling Scheme

A sample circuit in Monte Carlo analysis comprises values for each of the K variable component parameters. The component values are obtained by suitably transforming sets of values, called raw random numbers. The raw random numbers are pseudo-randomly generated to lie in the interval 0 to 1. If in the estimation of $\tilde{Y}_j$ and $\tilde{Y}_{j+1}$, the raw random numbers were unrelated, the covariance term in equation 4.27 would tend to zero. For future reference this situation is termed "independent sampling".

It is however more satisfactory to employ the same stream of raw random numbers for the jth and (j+1)th yield estimation. This can easily be done since the raw random numbers are obtained from a deterministic equation /28, chapter 6/ and hence may be repeated. This later strategy is termed "correlated sampling", /1,12,13, chapter 4/.

In contrast to independent sampling, correlated sampling introduces a positive covariance between estimates $\tilde{Y}_j$ and $\tilde{Y}_{j+1}$ and hence reduces the variance $\sigma^2_{\Delta Y}$ (see equation 4.27) of the estimated yield difference $\Delta\tilde{Y}_j$.

The cause of the positive covariance will be examined presently. Firstly, we note that $\tilde{Y}_j$ and $\tilde{Y}_{j+1}$ will be unbiased estimates of the true yields Y_j and Y_{j+1} respectively. This is so, since although the same stream of raw random numbers is employed for both estimations, the raw random numbers are transformed according to different p.d.f.'s i.e. $\emptyset(P^o_j)$ and $\emptyset(P^o_{j+1})$. Therefore for either iteration representative sets of sample circuits corresponding to design centers P^o_j and P^o_{j+1} are generated and analysed.

Secondly, it is noted that the difference between two unbiased estimates is an unbiased estimate of the difference. In the correlated sampling scheme the precision of the estimate of the yield difference is enhanced because the dependence between the two individual yield estimates is such that when one result is overestimated (or underestimated) by sampling variations, then so is the other one by roughly the same amount /13, page 48/.

A detailed comparison of independent and correlated sampling is made by Jensen /1/. Here we briefly develop the formula for computing the sampling variance defined in equation 4.27.

Let the number of sample circuits tested in each Monte Carlo analysis be N. Also let $P_j^1\ P_j^2\ \ldots.\ P_j^N$ and $P_{j+1}^1\ P_{j+1}^2\ \ldots.\ P_{j+1}^N$ denote the sample circuits of two successive iterations. The result of each circuit analysis and test can be represented as 1 or 0, reflecting the sample circuit's conformity or otherwise with the performance requirements. The vector of outcomes (results) of a Monte Carlo analysis is termed its yield trace. We let $X_j = x_j^1\ x_j^2\ \ldots.\ x_j^N$ and $X_{j+1} = x_{j+1}^1\ x_{j+1}^2\ \ldots.\ x_{j+1}^N$ denote the yield traces of the jth and (j+1)th Monte Carlo analysis. The dependence in the two yield traces introduced by the use of the same raw random numbers is seen in the outcomes of corresponding circuits, i.e. x_j^i and x_{j+1}^i etc. Also let n_{11} be the number of times x_j^i and x_{j+1}^i are both 1, n_{00} the number of times both x_j^i and x_{j+1}^i are zero, n_{10} the number of times x_j^i is 1 while x_{j+1}^i is 0 and so on for n_{01}.

Clearly
$$\tilde{Y}_j = (n_{11} + n_{10})/N$$
and
$$\tilde{Y}_{j+1} = (n_{11} + n_{01})/N$$

It is shown in /1/ that

$$\mathrm{COV}(\tilde{Y}_j, \tilde{Y}_{j+1}) = \frac{1}{N}\ \mathrm{COV}\ (x_j^i, x_{j+1}^i)$$

and further that

$$COV(x_j^i, x_{j+1}^i) = (n_{11} n_{00} - n_{01} n_{10})/N^2$$

leading to

$$COV(\tilde{Y}_j, \tilde{Y}_{j+1}) = (n_{11} n_{00} - n_{01} n_{10})/N^3 \qquad 4.28$$

The cause of this positive covariance may be appreciated by reconsidering the geometrical interpretation. In figure 4.10 a two dimensional example is considered. The parameters p_1 and p_2 are subject to a uniform and a Gaussian p.d.f. respectively. The diagram illustrates the relationship between the joint p.d.fs of successive iterates.

Figure 4.11 shows successive tolerance regions $R_{T,j}$ and $R_{T,j+1}$ associated with design centers P_j^o and P_{j+1}^o respectively. Now we recall that P_{j+1}^o and P_j^o are related as

$$P_{j+1}^o = P_j^o + \lambda_j \Delta P_j$$

The difference between the two design centers and therefore between the two joint p.d.f.'s $\emptyset(p_j^o)$ and $\emptyset(P_{j+1}^o)$ is simply one of translation by $\lambda_j \Delta P_j$. Similarly since the same raw random numbers are employed for both iterations, the difference between corresponding sample points is also $\lambda_j \Delta P_j$. Therefore we may write

$$p_{j+1}^i = P_j^i + \lambda_j \Delta P_j \qquad 4.29$$

$$\text{for} \qquad i = 1 \ldots\ldots N$$

As before P_j^i and P_{j+1}^i represent the ith samples of the jth and (j+1)th iterations respectively.

Figure 4.11 shows the two design centers and two pairs of typical points; p_j^r, p_{j+1}^r and p_i^s, p_{j+1}^s, say. In practice $\lambda_j|\Delta P_j|$ will be small. Therefore, corresponding points will be in close proximity in the input parameter space. Hence, there will be a small difference in performance between corresponding circuits. So that if the outcome of a particular sample circuit in iteration j is a pass, then the corresponding sample circuit in iteration j+1 is also likely to be so and, similarly for a fail.

(e) The Common Points Scheme

When iteratively performing Monte Carlo analysis, the common points scheme makes computational savings by re-employing, for current iterations, circuit analyses performed at previous iterations. However, unlike correlated sampling, the common points scheme is only applicable when the component parameter p.d.f. $\emptyset(.)$ is multivariate uniform. For practical circuit examples, the common points scheme uses smaller sample sizes and is found to give levels of confidence of correct ranking which are comparable to or greater than those obtained with correlated sampling. Later in this section we shall present a typical set of results demonstrating this. Initially, we develop the basic ideas behind the common points scheme.

Again consider figure 4.7, and the definitions of regions A, B and C. Let the relevant component parameter p.d.f. be K-variate uniform. Let us say that a straightforward Monte Carlo analysis is performed for design center P_j^o and tolerance region R_{T_j}. If the analysis comprises N sample circuits randomly distributed with a uniform distribution and if NA circuits are found to be acceptable, then yield can be

estimated as:

$$\tilde{Y}_j = NA/N \qquad 4.30$$

In view of the distribution of sample circuits according to a uniform p.d.f., on average a number

$$N' = N \times (V_A/V_T)$$

will fall in region A and

$$N'' = (N-N') = N \times (V_B/V_T)$$

will fall in region B. As before V_A, V_B and V_T denote the volumes of regions A, B and R_T respectively.

The yields Y_A and Y_B in regions A and B are referred to as partial yields, and can be estimated as:

$$\tilde{Y}_A = NA'/N' \qquad 4.31$$

and

$$\tilde{Y}_B = NA''/N''$$

NA' and NA" are the numbers of acceptable circuits in regions A and B respectively (see figure 4.12). An alternative estimate of the overall yield will then be the following:

$$\tilde{Y}_j = (V_A/V_T)\tilde{Y}_A + (V_B/V_T)\,\tilde{Y}_B \qquad 4.32$$

Both expressions 4.30 and 4.32 are unbiased estimates of the true yield Y_j. If N' is exactly equal to (V_A/V_T) then the two estimates are identical. The estimation of yield based on 4.32 is an instance of a variance reduction technique known as stratified sampling. Specifically, it is an instance of

"stratification after sampling". The general ideas involved in stratified sampling are discussed by Kleijnen /47,chapter 3, pp. 110-132/. At the end of this section we shall quote the relevant expressions for estimating the variance associated with a yield estimate based on stratified sampling, (i.e. estimate 4.32) and compare it with the variance of the conventional Monte Carlo estimate, i.e. expression 4.30. In practice the difference is too small to merit a fuller exposition.

Now for iteration j+1, the new design center P^{o}_{j+1} can be chosen as described earlier. We now need to estimate the new yield Y_{j+1}. This can be written as:

$$\tilde{Y}_{j+1} = \tilde{Y}_B(V_B/V_T)+\tilde{Y}_C(V_C/V_T) \qquad 4.33$$

However, an estimate of the partial yield Y_B is available from the previous iteration, and hence this estimation need not be repeated. Partial yield Y_C can then be estimated by randomly generating and analysing a number of sample circuits distributed in the region C. In one practical algorithm to be described later, the number of new circuits generated in region C is chosen to be N', i.e. equal to the number of circuits in region A. Therefore, the estimate $\tilde{Y}_{j+1}$ (expression 4.33) is also based on a sample size of N; whereas only N' new circuit analyses are performed, and N" circuit analyses from the previous iteration are re-employed.

Now we consider the implications on confidence of correctly ranking yield estimates, arising out of this scheme. Subtracting

equation 4.32 from 4.31, the difference between the two yields Y_{j+1} and Y_j can be written as

$$\Delta Y_j = (V_C/V_T)Y_C-(V_A/V_T)Y_A \qquad 4.34$$

However, $V_A = V_C$. Therefore (4.34) becomes:

$$\Delta Y_j = (V_A/V_T)\ (Y_C - Y_A) \qquad 4.35$$

Denoting $(Y_C - Y_A)$ as $\Delta Y'_j$, expression (4.35) may be re-written as:

$$\Delta Y_j = (V_A/V_T)\Delta Y'_j \qquad 4.36$$

In other words the difference ΔY_j between the yields Y_{j+1} and Y_j is (V_A/V_T) times the difference $\Delta Y'_j$ between the partial yields Y_C and Y_A. However, $(V_C/V_T) < 1$, therefore

$$\Delta Y'_j > Y_j \qquad 4.37$$

To estimate $\Delta Y'_j$, we subtract estimate $\tilde{Y}_A$ from $\tilde{Y}_C$ (see expression 4.31). The difference $\Delta\tilde{Y}_j$ in the overall yields can then be obtained from expression 4.36.

The sampling distribution of $\Delta\tilde{Y}'$ will be Gaussian with mean $\mu = \Delta\tilde{Y}'_j$ and variance $\sigma^2_{\Delta Y'}$ given by expression 4.38 below:

$$\sigma^2_{\Delta Y'} = \sigma^2_{Y_C} + \sigma^2_{Y_A} \qquad 4.38$$

The individual variances $\sigma^2_{Y_C}$ and $\sigma^2_{Y_A}$ will be given by the following expressions:

$$\sigma^2_{Y_A} = \frac{\tilde{Y}_A(1-\tilde{Y}_A)}{N'} \qquad 4.39$$

and

$$\sigma^2_{Y_C} = \frac{\tilde{Y}_C(1-\tilde{Y}_C)}{N'} \qquad 4.40$$

In comparing expression 4.38 with expression 4.27, we find that the covariance term has been omitted. In practice we expect the covariance to be approximately zero. This is so since the raw random numbers employed in the Monte Carlo estimation of the partial yields Y_A and Y_C are independent.

To rank overall yields Y_{j+1} and Y_j, we only need to rank yields Y_A and Y_C. That is because

$$Y_C > Y_A \text{ implies } Y_{j+1} > Y_j$$

or

$$\Delta Y_j' > 0 \text{ implies } \Delta Y_j > 0 \qquad 4.41$$

The confidence of correct ranking is now $\frac{1}{2} + \text{erf}(\Delta Y_j'/\sigma_{\Delta Y})$ where erf(.) is the error function defined previously. This compares with a confidence of $\frac{1}{2} + \text{erf}(\Delta Y_j \ /\sigma_{\Delta Y})$ for independent sampling. The confidence of correct ranking increases monotonically with the value of the argument of the error function. In practice we have always found that due to relationship 4.37,

$$\frac{\Delta Y_j'}{\sigma_{\Delta Y_j}} > \frac{\Delta Y_j}{\sigma_{\Delta Y_j}} \qquad 4.42$$

Unfortunately, no simple relationship connecting the variances $\sigma_{\Delta Y_j'}$ and $\sigma_{\Delta Y}$ can be obtained. However, in practice we have found that the larger magnitude of $\Delta Y_j'$ over ΔY_j

ensures that 4.42 holds. Therefore the confidence of correct ranking is enhanced in the common points scheme. The effect is illustrated in figure 4.9 (c) and can be contrasted with the effect achieved by using correlated sampling as illustrated in figure 4.9 (b).

The correlated sampling scheme described earlier is applicable for both non-uniform and uniform component p.d.f.'s, whereas the common points scheme is only applicable for uniform distributions. However, in the latter case the common points scheme is found to be more efficient. We demonstrate this with a typical set of results.

Figure 4.13 shows the yield trajectory (i.e. curve of yield against iteration) obtained by application of the statistical exploration design centering algorithm to a particular circuit example[α]. The applicable p.d.f. is assumed to be uniform and the common points scheme is used. The number of new circuit analyses performed at each iteration is indicated. The algorithm maintains a constant number of circuit samples (in this case 100) throughout the optimization. So that for iteration two for example, 29 new circuit analyses were performed, hence 71 analyses from the previous iteration were re-employed.

The results are further summarized in Table 4.3 and a comparison with correlated sampling is made. Column two of table 4.3,

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[α] The circuit in question is a seven component high pass filter which will be more fully discussed in the next section.

shows the number of new circuit analyses performed at each iteration while column three shows the overall estimate of yield. Columns four and five show the partial yields Y_A and Y_C, while column six indicates the difference in the partial yields. Column seven on the other hand is the difference in the overall yields. For example the entry in row two, column seven is the overall difference in yields between iterations one and two.

The confidence of correct ranking for the common points and correlated sampling schemes is compared in columns eight, nine and ten. We recall that the confidence of correct ranking is a monotonically increasing function of the co-efficient $\Delta Y/\sigma_{\Delta Y}$. Column eight shows the value of this co-efficient at different iterations, for the common points scheme. Columns nine and ten show the value of the same argument if the correlated sampling scheme had been employed. To appreciate the significance of this, we re-iterate the equation (4.27) for the variance $\sigma^2_{\Delta Y}$ in correlated sampling as:

$$\sigma^2_{\Delta Y_j} = \sigma^2_{Y_j} + \sigma^2_{Y_{j+1}} - 2\ \mathrm{COV}\ (Y_j, Y_{j+1}) \qquad 4.27$$

However, we can replace the covariance term as:

$$\mathrm{COV}\ (Y_j, Y_{j+1}) = \rho\sigma_{Yj} . \sigma_{Y_{j+1}} \qquad 4.43$$

Here ρ is the correlation co-efficient. Therefore we may re-write 4.27 as:

$$\sigma^2_{\Delta Y} = \sigma^2_{Y_J} + \sigma^2_{Y_{j+1}} - 2\rho\ \sigma_{Y_j} \sigma_{Y_{j+1}} \qquad 4.44$$

Further from elementary probability theory /9, chapter 5/, we recall that $-1 \leq \rho \leq 1$. In column nine and ten we have assumed particular positive values (0.5 and 0.8) for the correlation co-efficient and computed the variance $\sigma_{\Delta Y}$ using equation 4.44.

In every case it can be seen that the value of the co-efficient in column eight (common points scheme) is larger than that in columns nine or ten (correlated sampling). These results are typical of those obtained with other practical circuit examples.

Finally to conclude this section we reconsider expressions for the variance associated with an overall estimate of yield based on equation 4.32, i.e stratified sampling. We re-iterate equation 4.32, (also consider figure 4.12).

$$Y_{j+1} = (V_A/V_T)Y_A + (V_B/V_T)Y_B \qquad 4.32$$

The variance associated with this estimate is derived by Kleijnen /47/ as:

$$\sigma^2_{Y_j} = \left(\frac{V_A}{V_T}\right)^2 \sigma^2_{Y_A} + \left(\frac{V_B}{V_T}\right)^2 \sigma^2_{Y_B} \qquad (4.45)$$

The individual variances $\sigma^2_{Y_A}$ and $\sigma^2_{Y_B}$ can be estimated as indicated by expressions 4.39 and 4.40 i.e.

$$\sigma^2_{Y_A} = \frac{Y_A(1-Y_A)}{N'} \qquad 4.39$$

and

$$\sigma^2_{Y_B} = \frac{Y_B(1-Y_B)}{N'} \qquad 4.40$$

This compares with the conventional yield estimate as

$$\tilde{Y} = NA/N \qquad (4.30)$$

and an associated variance

$$\sigma_{Y_j}^2 = \frac{\tilde{Y}_j(1-\tilde{Y}_j)}{N} \qquad (4.46)$$

In general the variance (4.45) obtained with stratified sampling is smaller than that (4.46) obtained with conventional sampling. However, in our example, the region of interest R_T has been divided into two strata, i.e. regions A and B. It is shown in reference /47/, that the reduction in variance obtained by stratified sampling depends upon the number of strata and is very small for only two strata. In practice for yield estimation, we have found negligible differences in the variances calculated from the two expressions.

(f) Some Algorithms

Design centering algorithms based on the statistical exploration approach discussed above are summarized in figure 4.14 and 4.15.

(i) Algorithm 4.1 - Correlated Sampling Scheme

The following notes are provided in addition to figure 4.14.

1. The raw random numbers are a pseudo random sequence of values, uniformly distributed in the interval 0 to 1. The sequence of values is obtained by a deterministic equation and can be repeated exactly if the process commences from a particular value. This value is called the

random seed. Since we are employing the correlated sampling scheme, we are interested in repeating the sequence of raw random numbers. Therefore the initial random link is stored. After each iteration the value of the random link is re-set to this initial value.

2. Monte Carlo analysis is described in chapter one.

3. The design center for the next iteration is selected as described in section (b) and (c), i.e.

$$P^o_{j+1} = P^o_j + \lambda(G_A - G_R)$$

The centers of gravity G_A and G_R can be computed as described in section (a). In section (b), we have developed constraints on the value of the step size λ. In this practical algorithm, the constraint on the value of λ was of the form:

$$\frac{\prod_{i=1}^{K} \{2t_i - \lambda_j(g_{A_i} - g_{R_i})\}}{\prod_{i=1}^{K} 2t_i} < Y_j \qquad 4.25$$

Here t_i are the absolute tolerances of the K components, g_{Ai} and g_{Ri} are the co-ordinates of the centers of gravity G_A and G_R respectively and Y_j is the yield for the current iteration. Also we note that 4.25 is an implicit constraint on λ, i.e. λ cannot be written explicitly in terms of the other quantities. Therefore in practice the left hand side of 4.25 is evaluated for several discrete values of λ. Typically fifteen values are considered from 0.1 to 1.5 in steps of 0.1. In the initial stages of the optimization, the largest value of λ

which satisfies inequality 4.25 is chosen. However, as the optimization progresses and smaller yield increases per iteration are encountered, even smaller values of λ are selected. Typical selections of value of λ will be indicated for several practical examples in the next section.

4. Before every iteration the random link is reset to the initial value. This ensures that the same set of raw random numbers are used.

5. The confidence of correct ranking is computed as indicated in the formulae developed in section (d) above.

6. This is a decision made by the designer. If the confidence of correct ranking is small, say less than about 90%, then the designer may decide to perform more circuit analyses. The designer may then re-assess the difference in yield and the confidence of correct ranking. He may continue performing more analyses until the confidence is sufficiently high.

7. After each iteration the designer decides whether the process is to be continued to another iteration. As is indicated in the diagram, the designer normally terminates the optimization if a decrease in yield occurs over that for the previous iteration.

(ii) Algorithm 4.2 - Common Points Scheme

The following notes are provided in addition to figure 4.15.

1. The designer initially selects an "available sample size",

typically 100. This means that the method maintains 100 samples for each iteration. For example at a particular iteration 60 samples from the previous iteration may be found to be relevant to the current iteration. Then the 60 relevant samples are re-used and the other 40 circuit samples are discarded. Forty new sample circuits relevant to the current iteration are then generated and analysed. This is further explained in notes 4 and 5.

2. A conventional Monte Carlo analysis is performed as outlined in chapter one.

3. The design center is determined as explained in sections (a) and (b). The step size λ_j is selected as outlined in note 3, of algorithm 4.1 above.

4&5 The definitions of regions A, B and C are given in figure 4.6 and section (e). N is the available sample size. The method checks the position of each sample point. All sample circuits incident in the region A are discarded. The sample circuits incident in region B are re-employed. If N_j' is the number of sample circuits incident in region A, then N_j' new samples are generated in region C. Therefore in total N samples are available for the next iteration. The N_j' samples for region C are generated by a rejection technique. Basically, samples are generated with a uniform distribution over the entire tolerance region $R_{T_{j+1}}$, (i.e. region $B \cap C$). If a sample belongs to region B it is discarded, while if it belongs to region C, the sample is analysed. This

is continued until N_j' circuit samples have accrued in region C.

6. The overall yield for the new tolerance region and the confidence of correct ranking are computed as described in section (e).

7. This represents one of the decisions made by the human designer. If the confidence of correct ranking is low, say less than about 90%, then the designer may decide to perform more circuit analyses in regions A and C and re-compute the confidence.

8. Circuits can be generated to fall in regions A and C, by a method similar to the rejection technique mentioned in notes 4 and 5.

9. After each iteration the designer may decide to terminate the optimization. Usually, this is done if the yield is found to have decreased over that for the previous iteration.

(g) Circuit Examples And Results

The algorithms have been extensively tested for several circuit examples. In this section the results pertaining to three particular circuit examples are presented and discussed.

(i) Passive High Pass Filter /25/

The relevant circuit diagram is shown in figure 4.16. The specifications on the insertion loss, together with a sketch of the typical shape of the response curve are shown in figure 4.17. The circuit comprises seven

toleranced components and a total of eleven frequency points are tested.

In figures 4.18 and 4.19, we show typical yield-trajectories obtained by the application of the design centering algorithm. Uniform distributions are assumed and tolerances are taken as 5% and 15% respectively of the nominal component values of iteration No. 1. The common points sampling scheme is employed, and the number of fresh circuit samples analysed per iterate is indicated. For example, for the 5% tolerance case (figure 4.18), a total of 195 circuit analyses were performed over six iterations, for each of which the "available sample size" was 100. That is, the yield estimate for each iteration was based on 100 samples, although the number of circuit analyses performed was smaller. For example for iteration No. 3, 29 new sample circuits were analysed, whereas 71 samples from the previous iterations were re-employed.

For both examples, substantial increases in yield were obtained over five or six iterations. The confidence of correctly ranking successive iterates, also indicated in the diagrams, was high. In both cases, a confirmatory 500 sample Monte Carlo estimation was made at the initial and final iterations. The results of these analyses are also indicated in the diagrams.

The values of the step size λ are shown in the diagrams. These values were chosen by the experimenter by the method outlined in note 3 on algorithm 4.1, in Section (f).

In figure 4.20, we present the results of the application of the method when the component probability density functions are Gaussian. Two curves are shown. Curve A is the yield trajectory obtained when sample values were generated assuming Gaussian distributions. The correlated sampling scheme (described earlier) was employed. The sample size for each iteration was 100. Again substantial increases in yield were obtained and the confidence of correct ranking was high.

Curve B shows the yield trajectory when uniform distributions were assumed. As for curve A, tolerances were 10% of the nominals at iteration No. 1. Identical values were assumed for the design centers corresponding to iteration No. 1, for both yield trajectories.

For strategy B, the common points scheme was employed. The total number of circuit analyses performed over five iterations was 217. Strategy A on the other hand employed correlated sampling, which required a total of 500 samples. We note however, that strategy A used Gaussian distributions, for which the common points scheme was inapplicable.

At the termination of the design centering (strategy B), a 500 sample Monte Carlo analysis was performed for nominal values (design center) corresponding to iteration No. 5 of strategy B, but with the sample values generated assuming a Gaussian distribution. The resulting yield estimate was within 5% of the yield estimate for iteration No. 5 of strategy A. Now since strategy B is substantially

cheaper, these results suggested an overall strategy where uniform distributions and the common points scheme are employed for several iterations until further increases in yield appear unlikely. A switch is then made to the Gaussian distribution and the correlated sampling scheme. In the example shown here, no further increases in yield were obtained when a switch to a Gaussian distribution was made after iteration No. 5 of strategy B.

So far the results of the design centering experiments have been summarized in the form of graphs (yield trajectories). To give the reader an impression of the typical changes in component values, the component values for the various iterations represented in figures 4.18, 4.19 and 4.20 are presented in tables 4.4, 4.5 and 4.6 respectively.

As discussed in chapters two and three, the circuit designer may be constrained to select nominal values from a discrete set. A common method of dealing with such a constraint is to round off the continuous solution to the nearest allowable discrete solution. Although such a strategy can be shown to be non-optimal (see figure 3.1, chapter 3), the other alternative commonly used, i.e. a branch and bound method, would incur a prohibitive computational cost due to the need to perform a large number of yield estimations.

In figures 4.21 we present the results of a design centering strategy, where the continuous solutions are rounded off

to the nearest discrete solution. The results relate to the high pass filter example (figures 4.16 and 4.17). Tolerances were taken to be 5% of the nominal values for iteration No. 1. That is if the design center for the first iteration is $P_1^o = p_{11}^o\ p_{12}^o \ldots\ p_{1K}^o$, then the tolerances are $T = t_1\ t_2 \ldots\ t_k$, where $t_i = p_{1i} \times 0.05$; for $i=1 \ldots K$.

Eleven discrete choices of nominal values were assumed available for each component parameter. These allowable values were equally spaced in the intervals:

$$(p_{1i}^o - t_i) < p_i^o < (p_{1i} + t_i) \; ; \quad i=1 \ldots K$$

Symbolically the allowable values for the ith component would be:

$$(p_{1i}^o - t_i),\ (p_{1i}^o - 0.8t_i),\ (p_{1i}^o - 0.6t_i) \ldots\ p_{1i}^o,$$
$$(p_{1i}^o + 0.2t_i) \ldots (p_{1i}^o + 0.8t_i)\ (p_{1i}^o + t_i) \qquad (4.45)$$

The exact numerical values for this example are presented in table 4.7.

In results shown in figure 4.21, continuous values were first assumed available for iterations one to six. The continuous values for iteration six were rounded off to the nearest available discrete values for each of the toleranced components. A Monte Carlo analysis was then performed for the discrete design center, i.e. iteration No. 7.

On the other hand in figure 4.22, we illustrate a modified method where the continuous solution at each iteration was rounded off to the nearest allowable values before performing the Monte Carlo analysis. The same tolerances, allowable values and initial design center as for the example in figure 4.21 were assumed. After four iterations, a result identical to the one obtained with the previous strategy was obtained. That is, iterates four of figure 4.22 and seven of figure 4.23 were identical.

Similar results were obtained when considering tolerances of 10% of the initial nominal values. As before eleven discrete allowable values distributed as indicated in expression 4.45 were assumed.

A sufficient number of circuits were not tested to come to definite conclusions as to which of the above two variations of the rounding off strategy was to be preferred. Nevertheless, the results confirmed the effectiveness of the rounding off procedure employed in conjunction with the statistical exploration method of design centering.

Finally we note that commercially available components /36/ are not usually available in preferred values which are equally spaced over an interval, as is assumed above. Nevertheless, in principle the methods discussed above could deal with arbitrary distributions of discrete values.

We acknowledge that a more thorough practical investigation of the discrete value design centering problem still remains to be made.

(ii) A High Frequency Amplifier

Design centering was performed for the high frequency amplifier circuit shown in figures 4.23 and 4.24 /48/. Figure 4.23 shows the full circuit diagram including the resistors employed to bias the transistors. On the other hand in figure 4.24 (a) we consider only that part of the circuit which affects its a.c. behaviour. Figure 4.24(b) shows the a.c. small signal model employed for the transistors. The nominal values of the parameters of each of the transistors is also indicated.

The effectiveness of the statistical design centering method can be demonstrated with the a.c. equivalent circuit. In principle there is no limitation in considering the d.c. behaviour as well. However, in the absence of an implementation of a suitable d.c. analysis facility, the d.c. behaviour was not considered. Our purpose in including this example is to demonstrate the application of the design centering method to different types of circuits and to illustrate its independence of dimensionality.

The nominal values of the adjustable component parameters at the start of the optimization are shown in figure 4.24 (a) and in table 4.8(b). The absolute tolerances of the component are also shown. Uniform p.d.fs are assumed for each component parameter. This example involves nineteen

toleranced components. The circuit is required to meet a power gain specification at eleven frequencies as is indicated in table 4.8.

The results of the design centering are shown in figure 4.25. Substantial increases in yield are obtained over four iterations. The common points scheme was employed and the confidence of correctly ranking successive iterates was high.

(iii) A Transversal Filter

Here we demonstrate the application of the statistical exploration method to a circuit example consisting of 43 toleranced components. The circuit belongs to a family of transversal filters /49/ to be manufactured using charge-coupled devices. The basic structure of a transversal filter is shown in figure 4.26. The circuit operates on sampled values of an analogue signal. The input signal is passed through a cascade of delay elements. The output of each delay element is multiplied by a particular co-efficient and the multiplied outputs are summed to form the overall output of the filter. The mode of operation of the circuit for both frequency and time domains can be summarized as:

Time domain: $$U_2(t) = \sum_{\nu=0}^{K-1} \alpha_\nu U_1(t-\nu T)$$

Frequency Domain: $$V_2(j\omega) = \sum_{\nu=0}^{K-1} \alpha_\nu V_1 \, e^{-j\nu\omega T}$$

Or The Transfer Function: $$\frac{V_2}{V_1} = \sum_{\nu=0}^{K-1} \alpha_\nu \; e^{-j\nu\omega T}$$

T is the time interval between samples, and is related to the sampling frequency f_s as:

$$T = 1/f_s$$

$U_1(t)$ is the stream of input pulses and U_2 the output pulses. The α_i, i=0 ..... K-1, the filter co-efficients are the parameters subject to variation. The values of the α_i are determined by a capacitance which in turn is proportional to the area of an electrode in the integrated circuit. This is further explained in reference /49/. Due to the uncertainties of the manufacturing process, the values of these co-efficients are subject to statistical variation.

Design centering was performed on a filter involving 43 variable co-efficients. The applicable frequency domain specifications are shown in figure 4.27. The nominal values of the co-efficients were in the range -1 to 1, and the largest value encountered was 1. For design centering, tolerances were taken to be $\pm$ 0.01 (i.e. 1% of the largest co-efficient) for all the co-efficients. The applicable p.d.f. s were assumed to be uniform and independent. In the absence of accurate information about the statistical distributions of co-efficient values, the choice of uniform distributions was considered prudent for an initial attempt at improving the design /50/.

The results obtained are shown in figure 4.28. As for the examples discussed before, substantial increases in yield were obtained. These results lend support to the assertion that statistical Monte Carlo based methods are relatively independent of dimensionality, since in most cases a substantial fraction of the achieved yield increase is obtained in six or seven iterations.

4.5 SUMMARY AND CONCLUSIONS

In this chapter we have investigated the application of direct search optimization methods to the problem of maximizing production yield for fixed absolute component tolerances. We commenced the chapter with a brief description of a standard method, Pattern search, together with results for a particular circuit example.

The main contribution of this chapter is the introduction and development of a novel technique called Statistical Exploration. Both Pattern Search and Statistical Exploration employ Monte Carlo analysis to estimate yield. However, in contrast to Pattern Search, Statistical Exploration makes use of the spatial information generated by Monte Carlo analysis, to choose suitable design centers. A direct comparison between the two methods has not been made. Pattern search has been reported for a 5 variable circuit, where the initial yield was 80%. Yield increases of 9% to 10% were reported. On the other hand Statistical Exploration has been reported for various circuit examples ranging from 7 to 43 toleranced components. In addition while commencing with yields smaller than 80%, large overall increases in yield have been achieved.

It was concluded in the review in chapter two that statistical methods which are independent of dimensionality (number of toleranced components) were preferred over deterministic methods. We note that both Pattern search and Statistical Exploration employ Monte Carlo analysis, for which the number of circuit analyses required is independent of dimensionality. However, Monte Carlo analysis is computationally very expensive. Therefore we are interested in minimizing the number of iterations performed. In the examples tested with Statistical Exploration, the number of iterations performed to arrive at yield maxima ranges from 4 to about 8, and is found to be independent of dimensionality. This is summarised in table 4.9 , for the circuit examples reported here and in references /51,52/. These results contrast with those expected for the Pattern Search strategy, which is inherently dependent upon dimensionality. For example, the minimum number of iterations required for one set of exploratory moves will be K (the number of toleranced components), while the maximum number will be $2K$. In addition the number of base points has been reported to be proportional to K^2.

In order to reduce overall computational cost both the number of iterations and the number of circuit analyses performed for the individual iterations must be kept small. We have discussed the dependence of the extent of the confidence intervals of individual yield estimates, and the degree of confidence of correctly ranking estimates (iterates), on sample size.

Special sampling schemes which reduce the sample size required for a particular degree of confidence of correct ranking have been discussed. A novel technique, the ommon Points scheme, has been proposed and compared with a standard scheme, Correlated Sampling. The Common Points Scheme is only applicable for the case where the component parameter p.d.fs are uniform, whereas the Correlated Sampling Scheme is applicable for all forms of p.d.f. Nevertheless, in practical circuit examples, for the case where component p.d.fs were assumed to be uniform, the Common Points Scheme is expected to require substantially smaller sample sizes than those required for the Correlated Sampling Scheme. A particular circuit example comparing the two schemes has been presented in this chapter (section 4).

In addition to the case of uniform component parameter p.d.f only the case of independent Gaussian distributions has been investigated. As regards the Statistical Exploration method there is no difficulty in principle in extending it to the case where arbitrary forms of p.d.f. are considered. For the case of independent Gaussian distributions it has been shown that the Statistical Exploration method employed in conjunction with the Correlated Sampling scheme gives satisfactory results. Nevertheless, it is found to be more satisfactory to assume uniform distributions for the initial iterations and to switch to Gaussian p.d.fs when no more increases in yield are obtained with the uniform distributions. The assumption of uniform p.d.f allows the use of the Common Points scheme and results in a considerable saving in computational effort over the alternative scheme where Gaussian distributions are assumed throughout.

For the design of discrete component circuits design centering may be used as a prelude to tolerance assignment. In such a case the designer may only be allowed to choose nominal component values from a discrete set of allowable values. Therefore discretization may be considered as a special type of constraint on the design variables. We have investigated a strategy where the continuous design values selected by the design centering algorithm are rounded off to the nearest discrete allowable values. Two variants of this strategy have been reported for application to a particular circuit example. Satisfactory results are obtained. Nevertheless, it is concluded that further investigation of this problem is desirable.

Design centering is of particular importance for integrated circuits. The designer has less freedom in choosing component tolerances than for discrete circuits. Therefore he must increase yield by choosing a more suitable set of nominal values. The circuit examples reported in this chapter have been regarded as discrete component circuits. Nevertheless, the main ideas may easily be extended to the design of integrated circuits. A far greater problem as regards the design of integrated circuits will be that of obtaining accurate descriptions of the component parameter p.d.f. s. We surmise that for many forms of p.d.f. it will be useful to commence the design centering by assuming uniform distributions. The applicable p.d.f. s can then be considered when an approximate solution has been so found.

Finally we note that a set of heuristic optimization techniques has been presented and their efficacy demonstrated for particular circuit examples. These methods have been found to function satisfactorily for everyone of the circuit examples considered so far. The methods have been demonstrated for much larger circuit examples than those reported in the literature so far (e.g. Director et al /21/).

PERFORMANCE FUNCTION	LOWER LIMIT	UPPER LIMIT
D.C. collector current of transistor Tr 1.	0.2mA	0.8mA
D.C. collector current transistor Tr 2.	0.5mA	1.5mA
D.C. emitter current of Transistor Tr 3.	10mA	15mA
V_{CE} of Tr 1	1V	5V
V_{CE} of Tr 2	2V	8V
V_{CE} of Tr 3	2V	6V
Mid band voltage gain of the amplifier	18	24
Mid band input impedence	20KΩ	50KΩ
Mid band output impedence	0Ω	0.5KΩ

Table 4.1: Performance constraints for the wide-band amplifier circuit example.

COMPONENT	INITIAL VALUE KΩ	FINAL VALUE KΩ
R_2	0.020	0.020
R_3	45.75	48.75
R_4	13.75	16.25
R_5	1.45	1.3
R_6	3.875	3.625
R_7	0.425	0.4

The number of base points was 9.

The initial yield was 84.2%.

The final yield was 90%.

Table 4.2: Summary of results of the application of the Pattern search strategy for the wide band amplifier circuit example.

1 Iteration Number.	2 Number of new circuit analyses.	3 $\tilde{Y}$	4 $\tilde{Y}_A$	5 $\tilde{Y}_C$	6 $\Delta\tilde{Y}'$	7 $\Delta\tilde{Y}$	8 $\Delta\tilde{Y}'/\sigma_{\Delta Y}$	9 $\Delta\tilde{Y}/\sigma_{\Delta Y}$ for $\rho = 0.5$	10 $\Delta\tilde{Y}/\sigma_Y$ for $\rho = 0.8$
1	100	0.65							
2	29	0.76	0.45	0.82	0.37	0.11	3.17	1.305	2.04
3	23	0.85	0.48	0.87	0.39	0.09	3.1	1.09	1.68
4	10	0.9	0.4	0.9	0.5	0.05	2.75	0.48	0.74
5	28	0.94	0.82	0.96	0.14	0.04	1.717	0.77	1.17
6	5	0.95	0.4	0.8	0.4	0.01	1.414	0.09	0.15

Table 4.3: A Summary Of A Set Of Results Demonstrating The Efficacy Of The Common Points Scheme And A comparison With The Correlated Sampling Scheme

Iteration No. — Component Values

j	p_1 nF	p_2 nF	p_3 H	p_4 nF	p_5 nF	p_6 H	p_7 nF	Yield
1	11.89	36.21	3.945	11.35	95.95	2.91	16.06	65
2	11.79	36.14	3.92	11.31	95.64	2.879	16.03	76
3	11.72	36.12	3.908	11.25	95.42	2.854	15.98	85
4	11.68	36.07	3.898	11.22	95.52	2.896	15.93	90
5	11.66	35.96	3.878	11.20	95.46	2.832	15.89	96
6	11.64	35.92	3.872	11.18	95.48	2.826	15.86	96

The Absolute Values Of The Tolerances Of The Various Components were:

t_1 nF	t_2 nF	t_3 H	t_4 nF	t_5 nF	t_6 H	t_7 nF
.5945	1.811	.1973	.5675	4.798	.1455	.803

Table 4.4: Component Values For The Various Iterations Of The Statistical Exploration-Design Centering Run Summarised In Figure 4.18. (Also See Circuit Diagram Fig. 4.16)

Iteration No. ← Component Values →

j	p_1 nF	p_2 nF	p_3 H	p_4 nF	p_5 nF	p_6 H	p_7 nF	Yield
1	11.89	36.21	3.945	11.35	95.95	2.91	16.06	22
2	11.76	37.29	3.733	10.51	96.89	2.73	15.94	28
3	11.57	38.71	3.722	10.15	96.07	2.698	15.84	32
4	11.8	39.24	3.703	10.02	95.57	2.725	15.72	33
5	11.91	39.3	36.95	10.05	95.02	2.736	15.59	36

The Absolute Values Of The Tolerances Of The Various Components Were

t_1 nF	t_2 nF	t_3 H	t_4 nF	t_5 nF	t_6 H	t_7 nF
1.783	5.432	.5918	1.703	14.39	.4365	2.409

Table 4.5: Component Values For The Various Iterations Of The Statistical Exploration-Design Centering Run Summarised In Figure 4.19.(Also See Circuit Diagram Fig. 4.16)

	j	p_1 nF	p_2 nF	p_3 H	p_4 nF	p_5 nF	p_6 H	p_7 nF	Yield
A	1	11.89	36.21	3.945	11.35	95.95	2.91	16.06	62
	2	11.79	35.83	3.911	11.33	95.32	2.884	15.93	79
	3	11.72	35.78	3.9	11.34	95.23	2.863	15.82	86
	4	11.64	35.79	3.897	11.29	95.36	2.84	15.76	91
	5	11.62	35.79	3.898	11.27	95.51	2.834	15.76	94
B	1	11.89	36.21	3.945	11.35	95.95	2.91	16.06	39
	2	11.68	36.24	3.868	11.05	95.88	2.752	15.85	53
	3	11.71	35.51	3.832	11.08	96.29	2.684	15.64	63
	4	11.61	35.1	3.85	10.7	96.13	2.71	15.73	65
	5	11.56	34.76	3.87	10.58	95.85	2.716	15.56	66

The Absolute Values Of The Tolerances Of The Various Components Were

t_1	t_2	t_3	t_4	t_5	t_6	t_7
1.189	3.621	.3945	1.135	9.595	.291	1.606

Table 4.6 : Component Values For The Various Iterations Of The Statistical Exploration Design Centering Run Summarised In Figure 4.20 (Also See Circuit Diagram fig. 4.16)

Iteration No. Component Values

j	p_1 nF	p_2 nF	p_3 H	p_4 nF	p_5 nF	p_6 H	p_7 nF	Yield
1	11.89	36.21	3.945	11.35	95.95	2.91	16.06	65
	11.89	36.21	3.945	11.35	95.95	2.91	16.06	
2	11.79	36.15	3.919	11.31	95.63	2.874	16.03	73
	11.77	36.21	3.906	11.35	95.95	2.881	16.06	
3	11.7	36.17	3.898	11.31	95.89	2.858	15.99	85
	11.65	36.21	3.906	11.35	95.95	2.852	16.06	
4	11.62	36.17	3.895	11.31	96.1	2.846	16.02	87
	11.65	36.21	3.906	11.35	95.95	2.852	16.06	

The Absolute Values Of The Tolerances Of The Various Components Were

t_1 nF	t_2 nF	t_3 H	t_4 nF	t_5 nF	t_6 H	t_7 nF
.5945	1.811	.1973	.5675	4.798	.1455	.803

Note A Refers To The Continous Values Indicated By The Design Centering Algorithm And B Refers to the Corresponding Values After Rounding Off To The Nearest Allowable Discrete Values.

Table 4.7: Component Values For The Various Iterations Of The Various Iterations Of The Statistical Exploration Design Centering Run Summarised In Figure 4.22.(Both Continous And Discretized Solutions Are Indicated)

Frequency In MHz.	10	40	70	100	150	200	240	270	300	320	350
Lower Limit on Gain in dB, Relative to Gain at 50 Mhz.	-0.14	-0.12	-0.08	0.02	0.08	0.15	0.1	0.1	0	-0.2	-0.4
Upper Limit On Gain.	0	0.04	0.08	0.22	0.3	0.75	0.8	0.8	0.8	0.8	0.8

Gain Specification

Table 4.8.(a)

Table 4.8 : Gain Specifications , Component Nominal Values, And Tolerances For The High Frequency Amplifier Circuit Example. (P.T.O For Table 4.7(b))

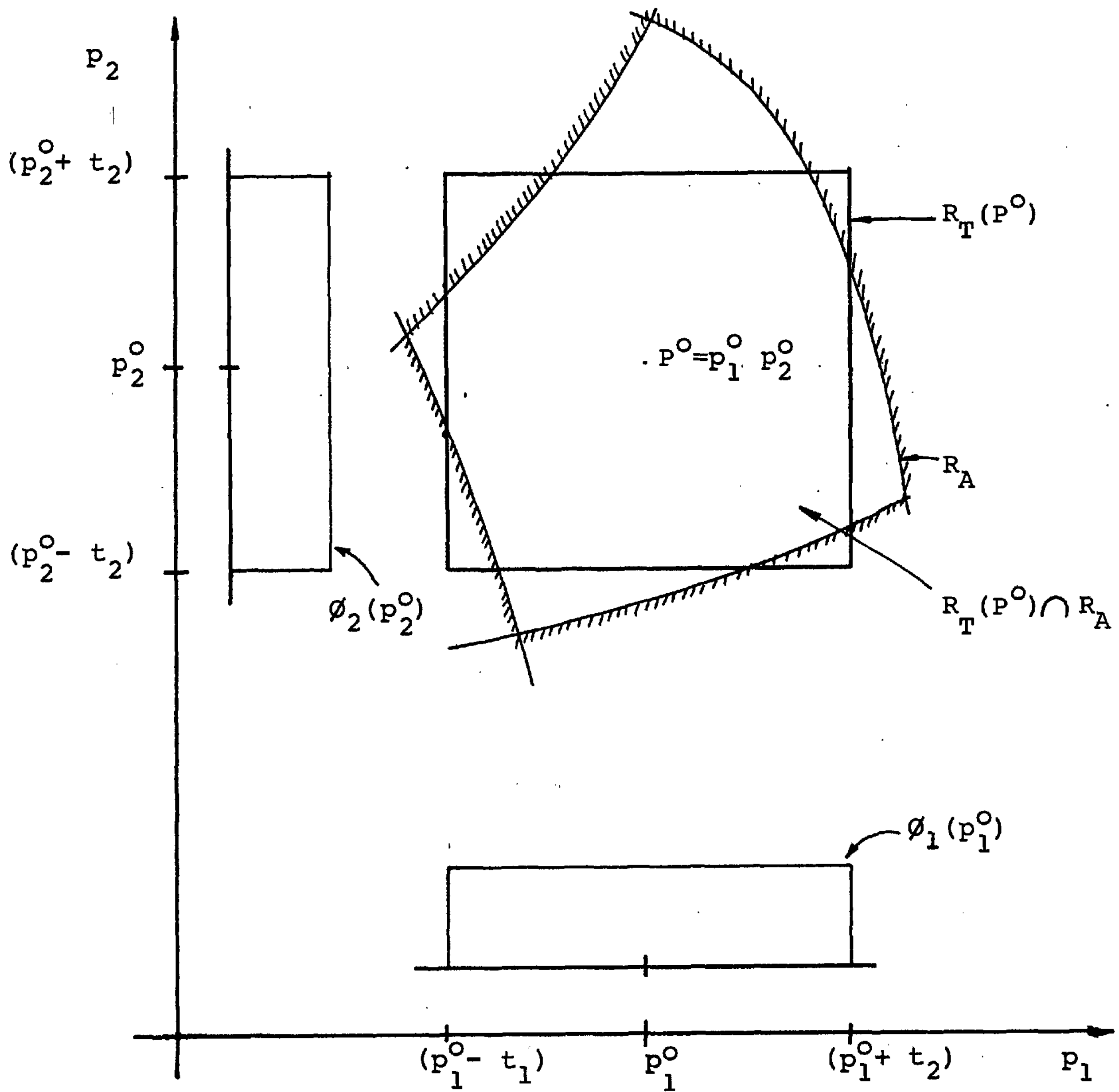
Component Parameter	Initial Nominal Value	Absolute Value Of Tolerance	Tolerance Expressed As % Of Initial Nominal Value
R_1	11.1	0.111	1
R_2	180	3.6	2
R_3	1500	30	2
R_4	18	0.09	0.5
R_5	83	0.415	0.5
R_6	417	2.085	0.5
R_7	510	5.1	1
R_8	22	0.11	0.5
R_{10}	46.5	0.2325	0.5
R_{11}	750	15	2
R_{12}	430	8.6	2
R_{14}	200	1	0.5
R_{15}	50	0.25	0.5
R_{16}	23.1	0.1155	0.5
R_{p_1}	210	69.3	33
R_{p_2}	114	37.62	33
R_{p_3}	123	40.59	33
R_{p_4}	33	10.89	33
C_8	6.2	0.496	8

Note: Resistance values in Ω : Capacitance values in pF

Table 4.8 (b): Component Nominal Values And Tolerances

CIRCUIT	NO. OF COMPONENTS	INITIAL YIELD %	FINAL YIELD %	NO. OF ITERATIONS
High Pass Filter /42/	7	40	65	5
Band Pass Filter /41/	8	15	62	5
Low Pass Filter /51/	11	22	72	5
High Frequency Amplifier /this chapter/	19	22	83	4
Transversal Filter (43 Coefficients) /this chapter/	43	6	30	8
Transversal Filter (55 Coefficient) /52/	55	52	64	5

Table 4.9: A summary of typical results for six circuit examples showing that the number of iterations performed (until no further increases in yield accrue), using the statistical exploration method is independent of the dimensionality



$$\text{Yield} \triangleq \frac{\text{Volume of } R_T(P^o) \cap R_A}{\text{Volume of } R_T(P^o)}$$

Figure 4.1: A Geometrical Interpretation Of Yield.

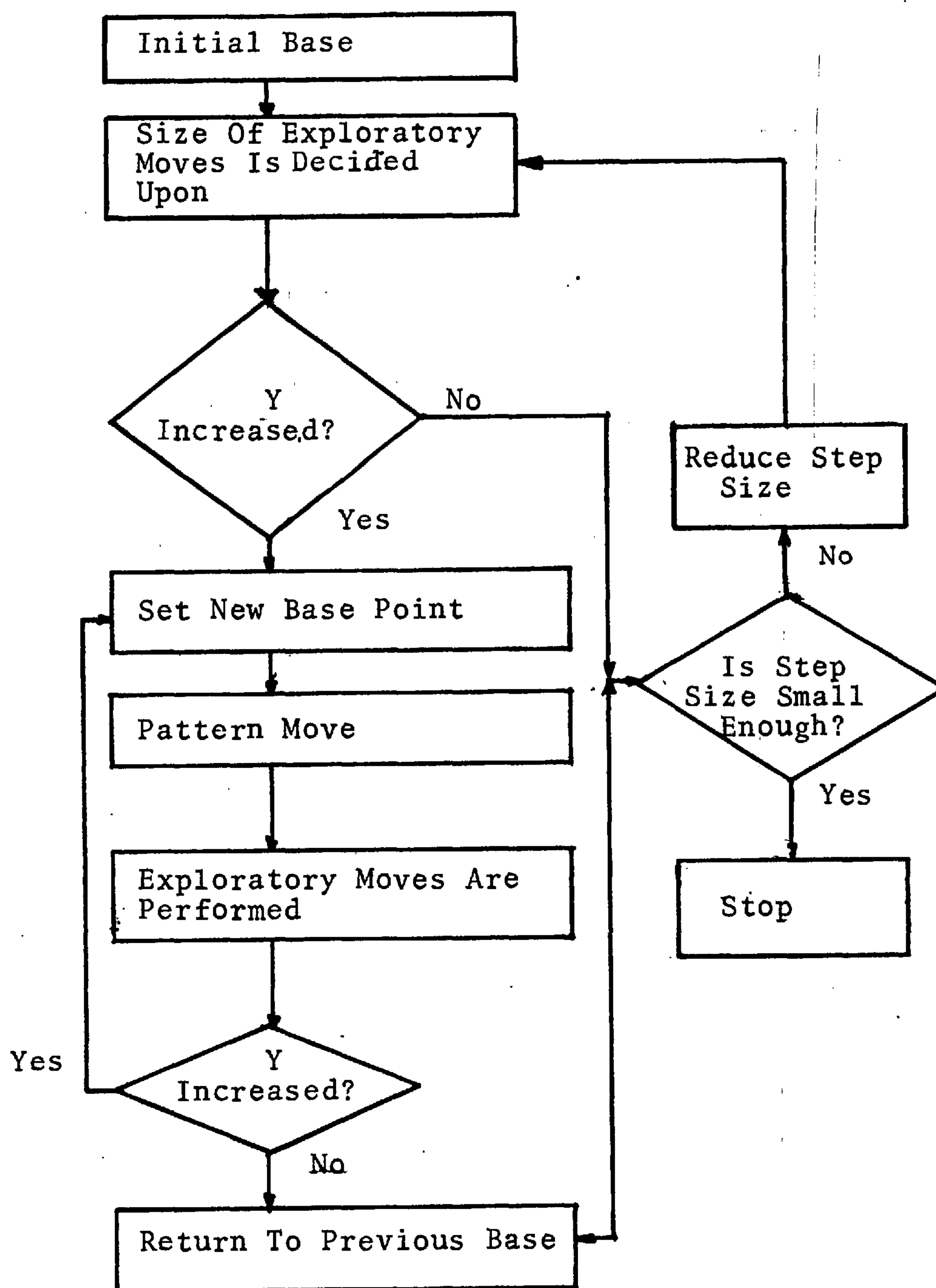
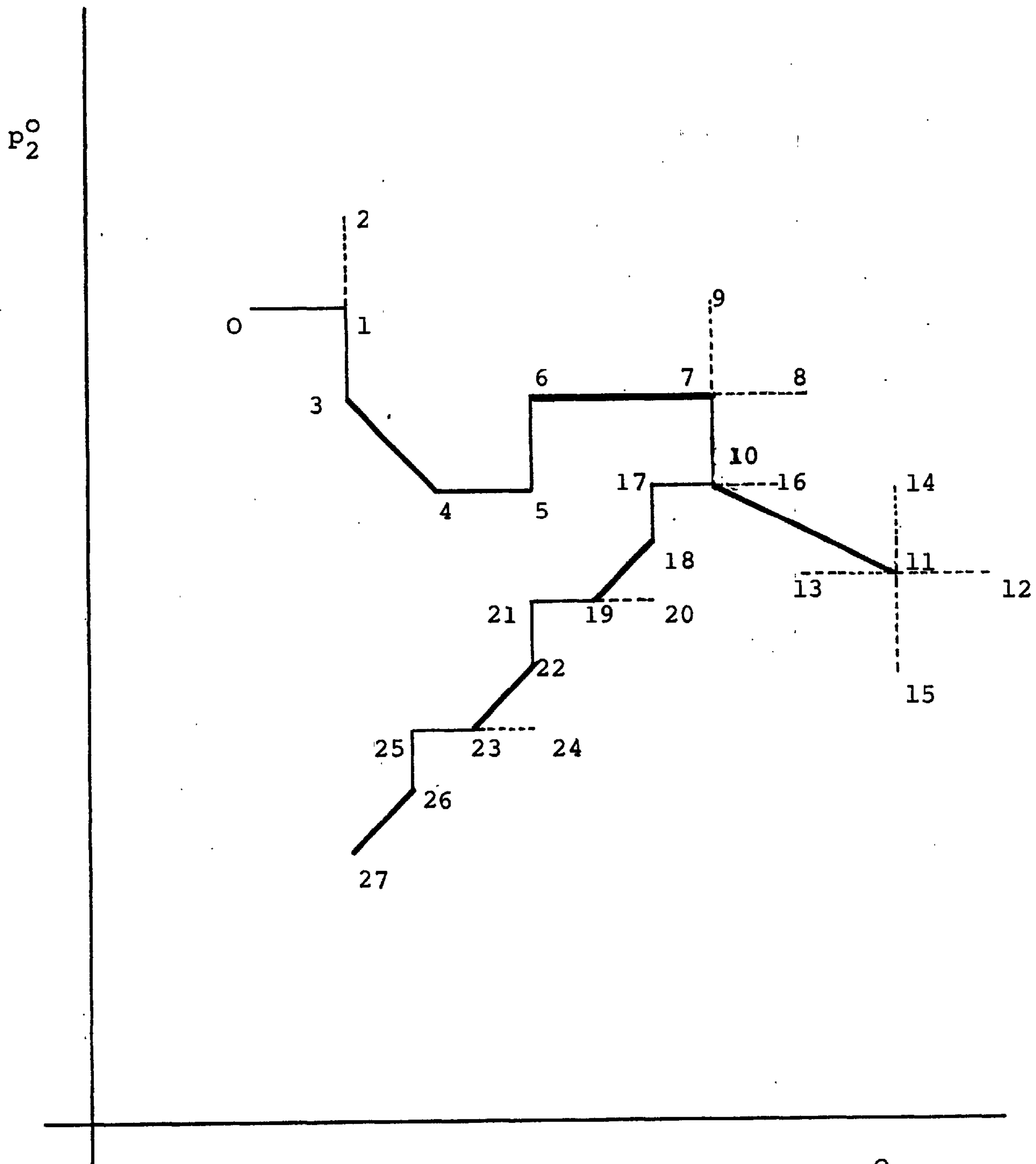


Figure 4.2 : A General Flow Chart For The Pattern Search Method /12, Chapter 8, Page 184/



The base points are 1,3,4,6,7,10,11,
18,19,22,23,26
Thick lines denote pattern moves,thin lines denote exploratory moves,broken thin lines denote unsuccessful exploratory moves.

Figure 4.3 Hypothetical Trajectory For Application Of The Pattern Search Method To A 2 Dimensional Example

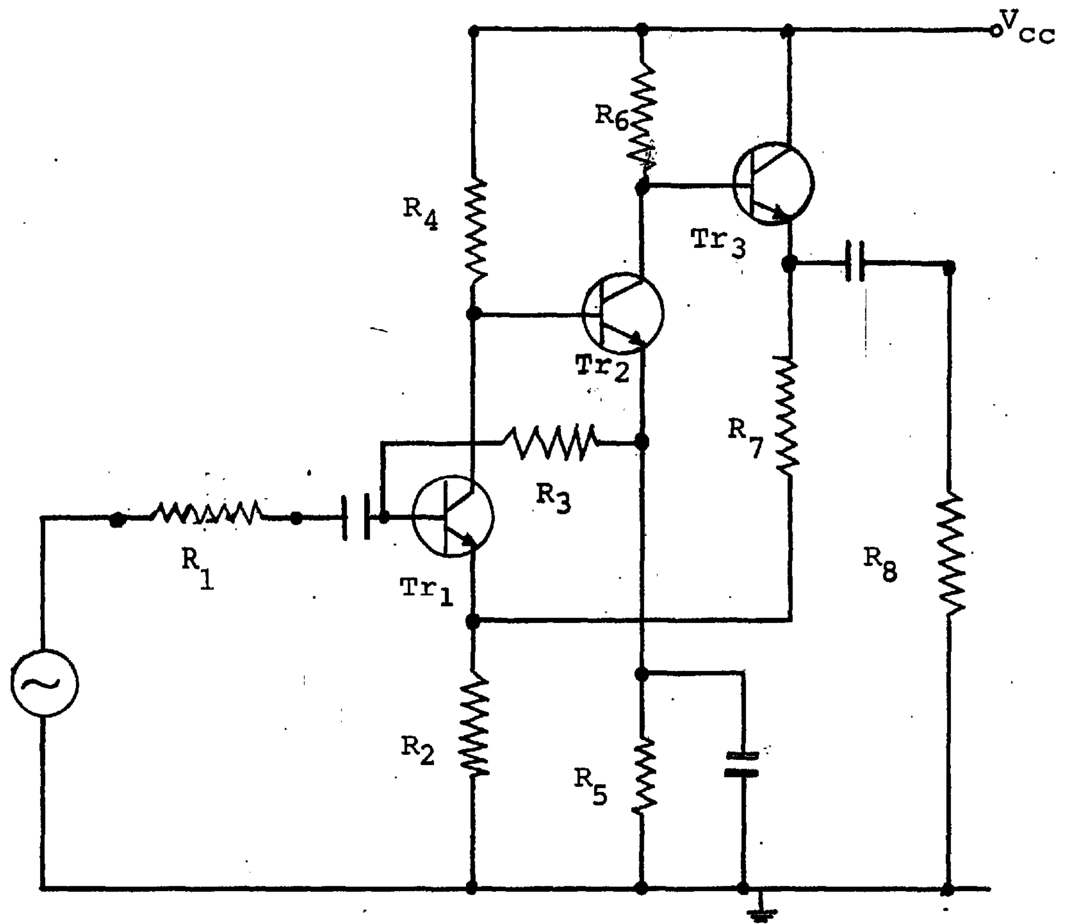


Figure 4.4 Wide Band Amplifier- Circuit Example For The Pattern Search Strategy

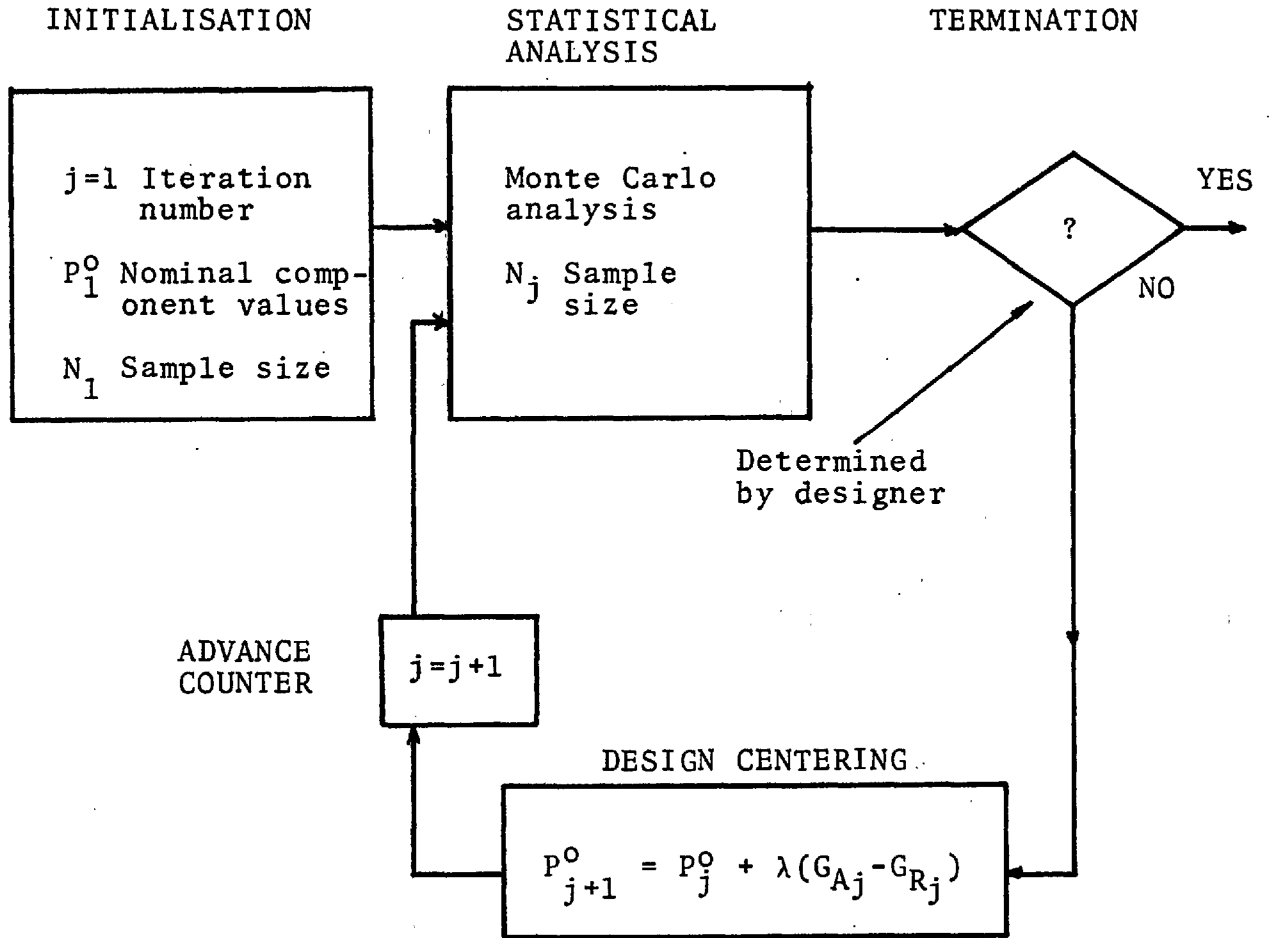


Figure 4.5: General flow chart for the statistical exploration method of design centering.

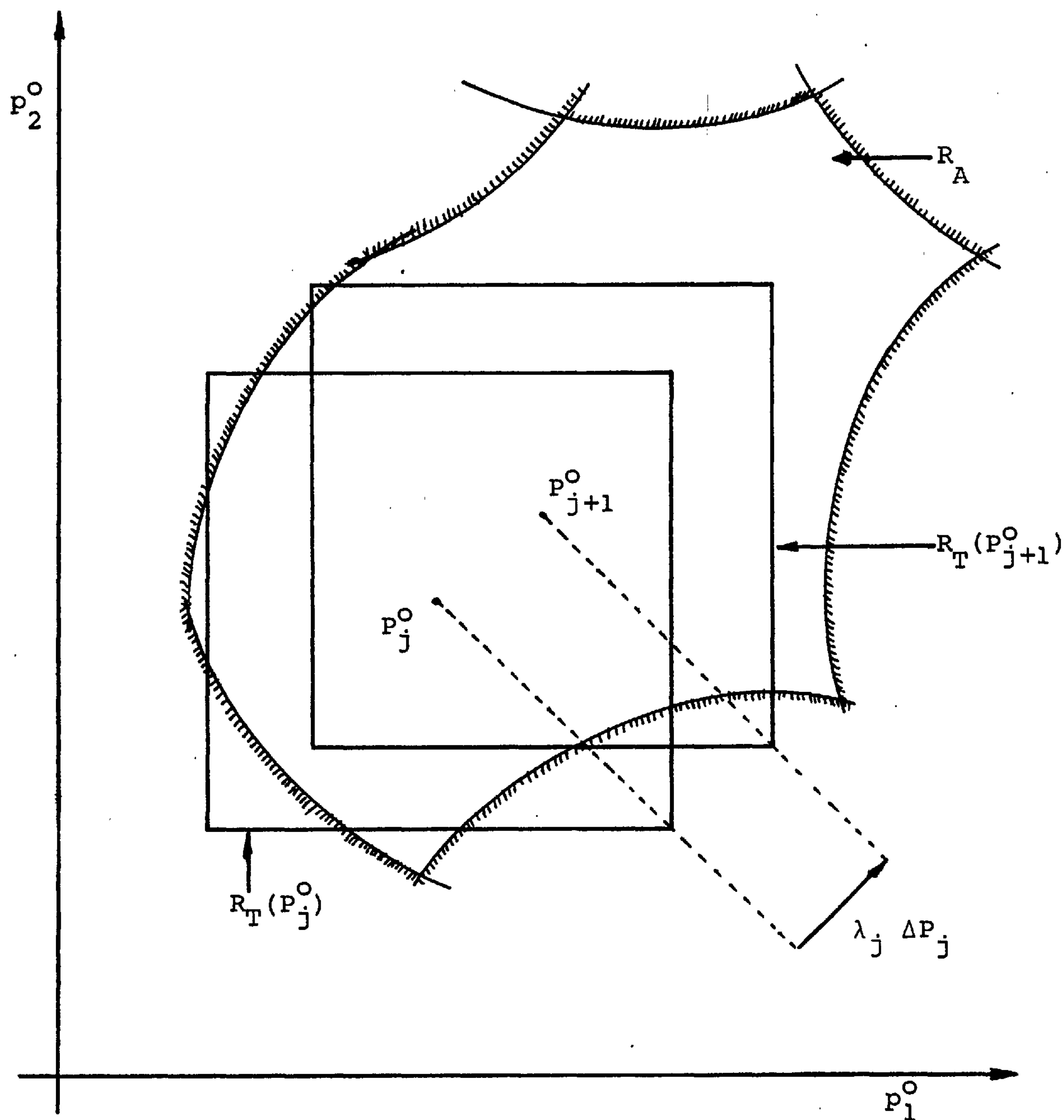


Figure 4.6: A Geometrical Representation Of The Relationship Between Successive Iterates In Design Centering.

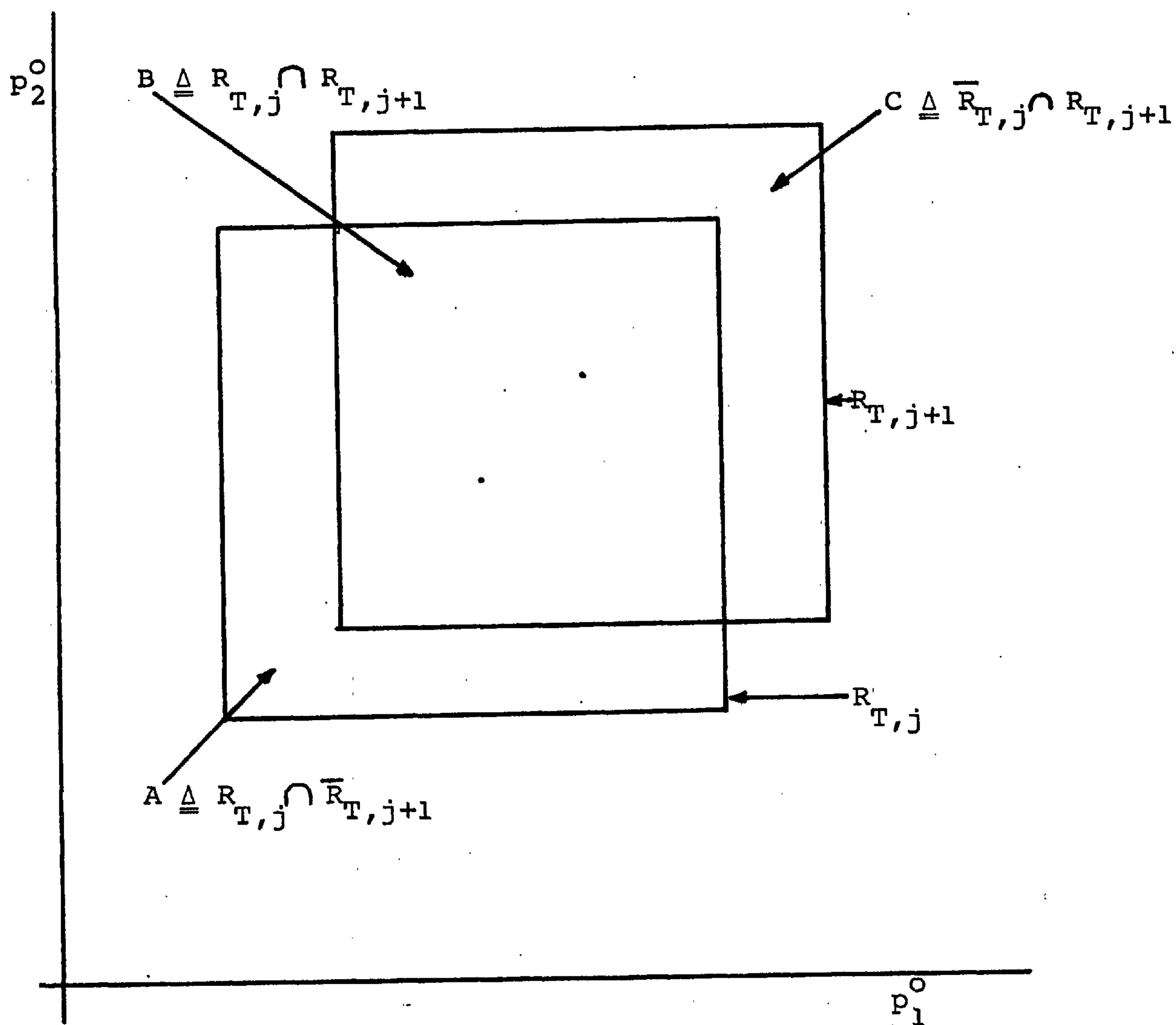


Figure 4.7: Illustrating Some Additional Notation.

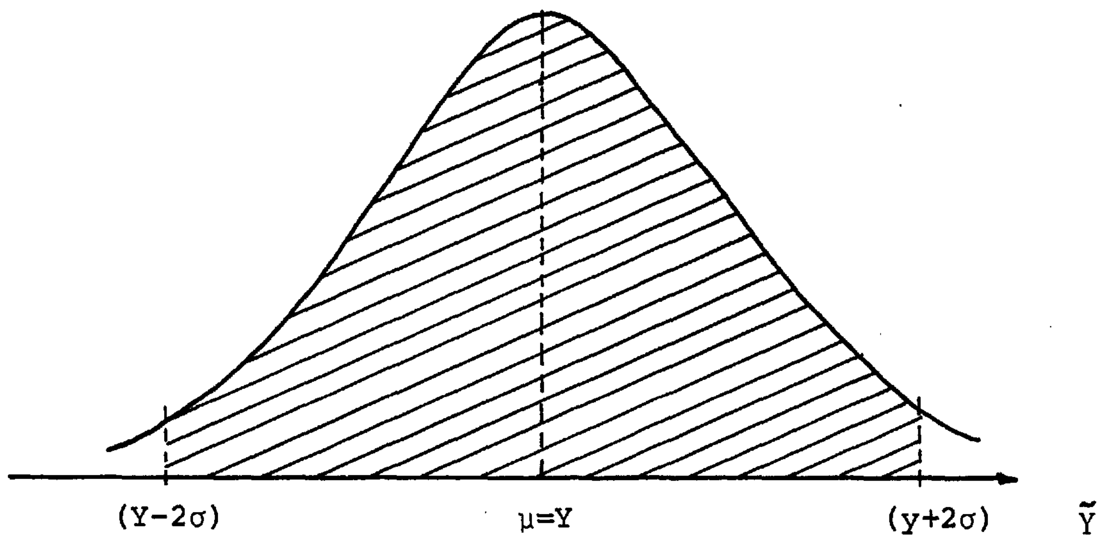


Figure 4.8: Sampling Distribution Of The Yield Estimate.

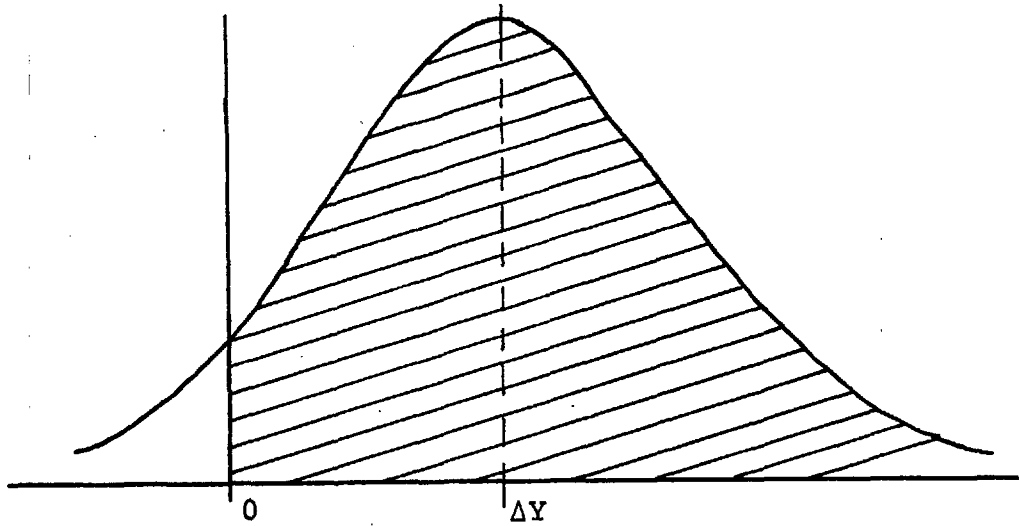


Figure 4.9(a): Independent Sampling

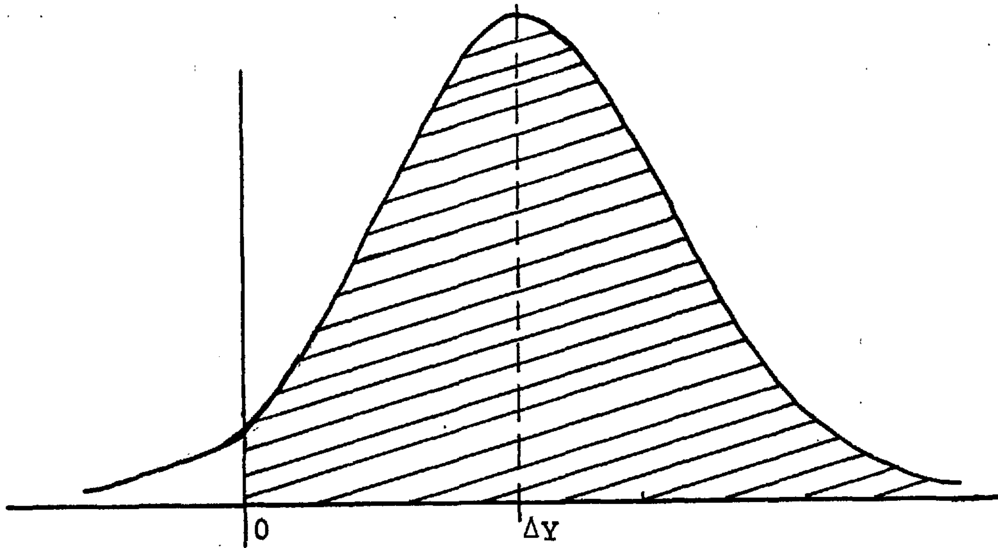


Figure 4.9(b) Correlated Sampling

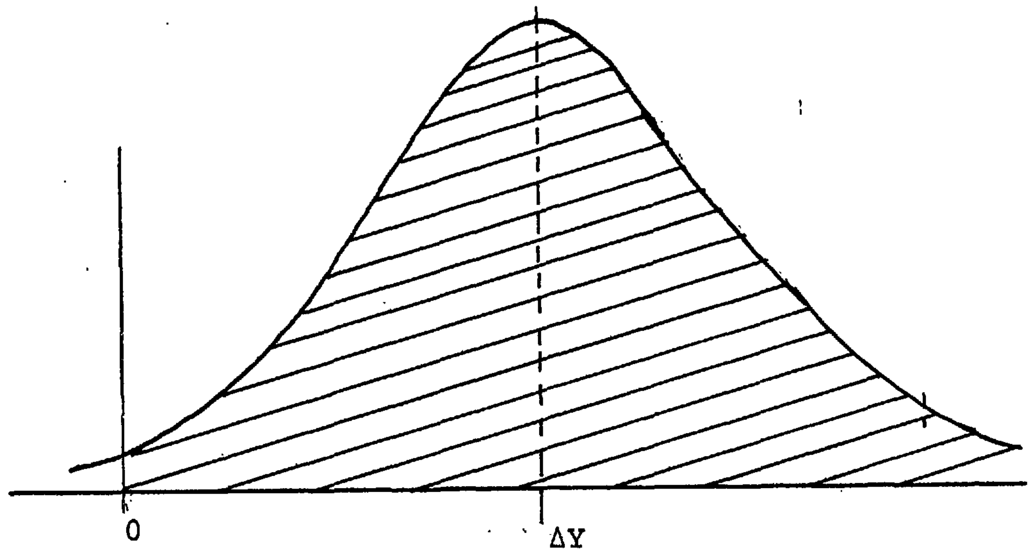


Figure 4.9(c) Common Points Scheme

Figure 4.9: Sampling Distributions For Estimating Yield Difference.

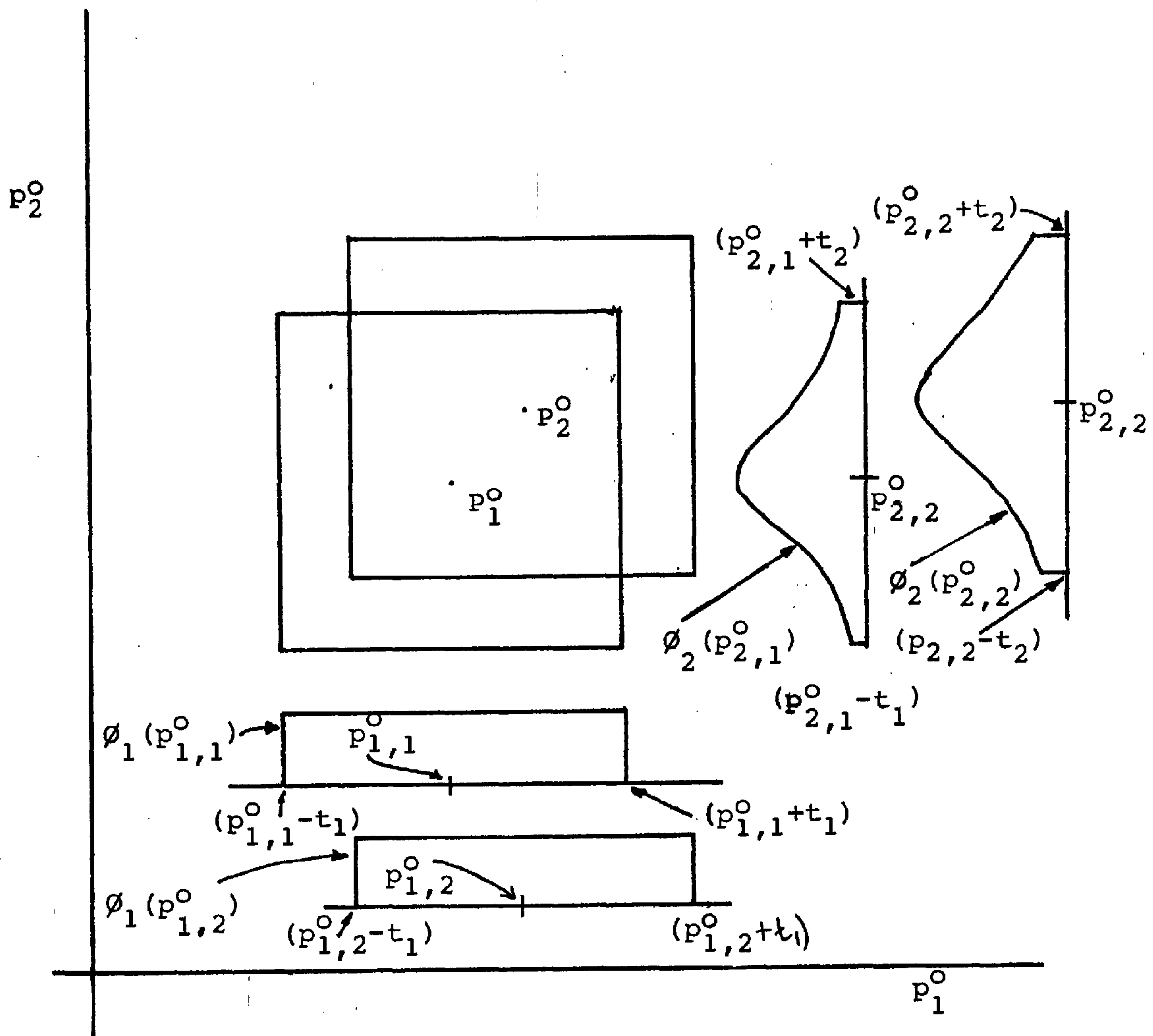
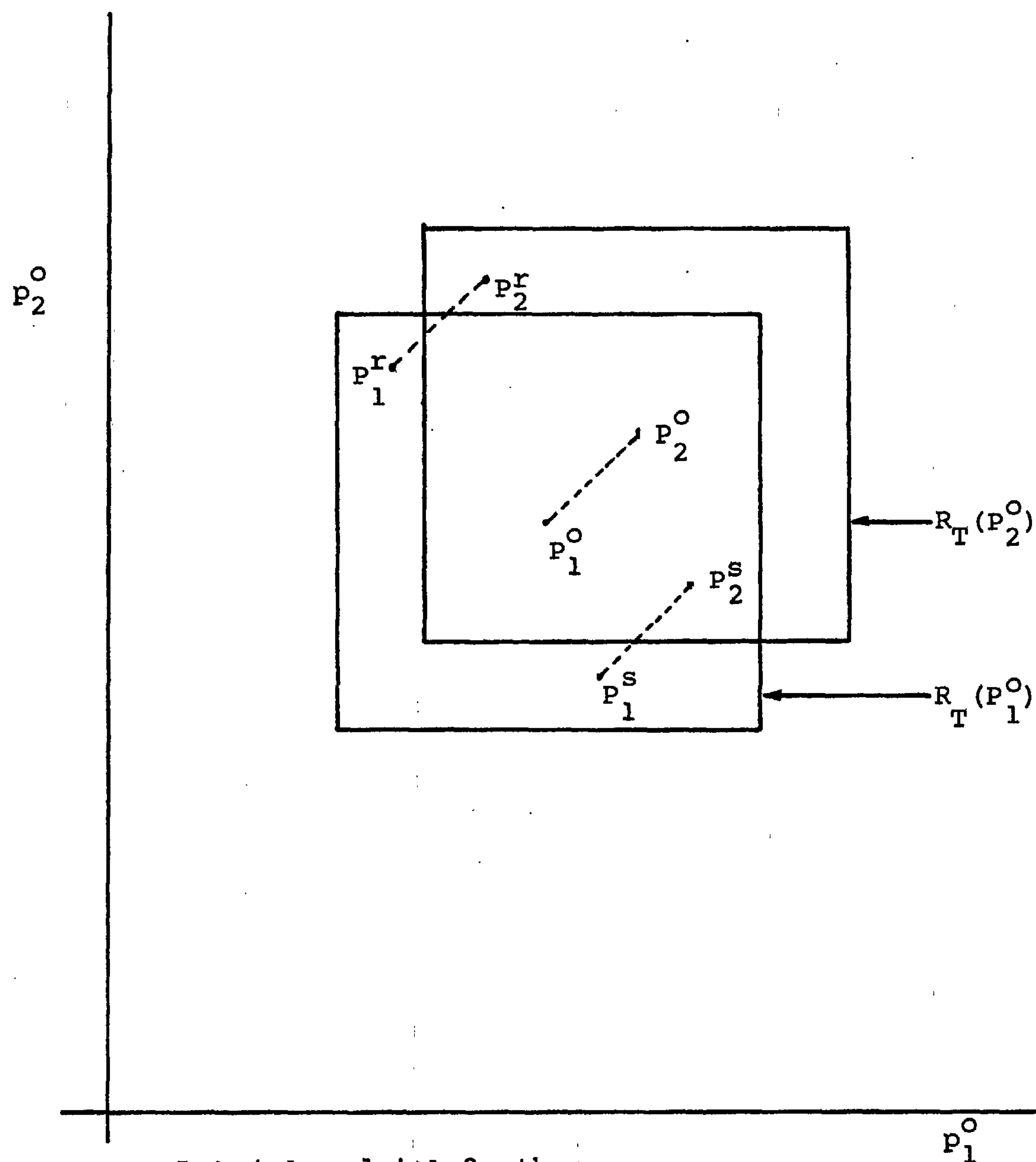


Figure 4.10: Illustrating The Relationship Between p.d.f s Of Successive Iterates.



Let j=1 and j+1=2, then:

$$P_2^r = P_1^r + \lambda\Delta P$$

$$P_2^s = P_1^s + \lambda\Delta P$$

$$P_2^o = P_1^o + \lambda\Delta P$$

Figure 4.11: Illustrating The Relationship Between Corresponding Sample Points For Successive Tolerance Regions When The Correlated Sampling Scheme Is Employed.

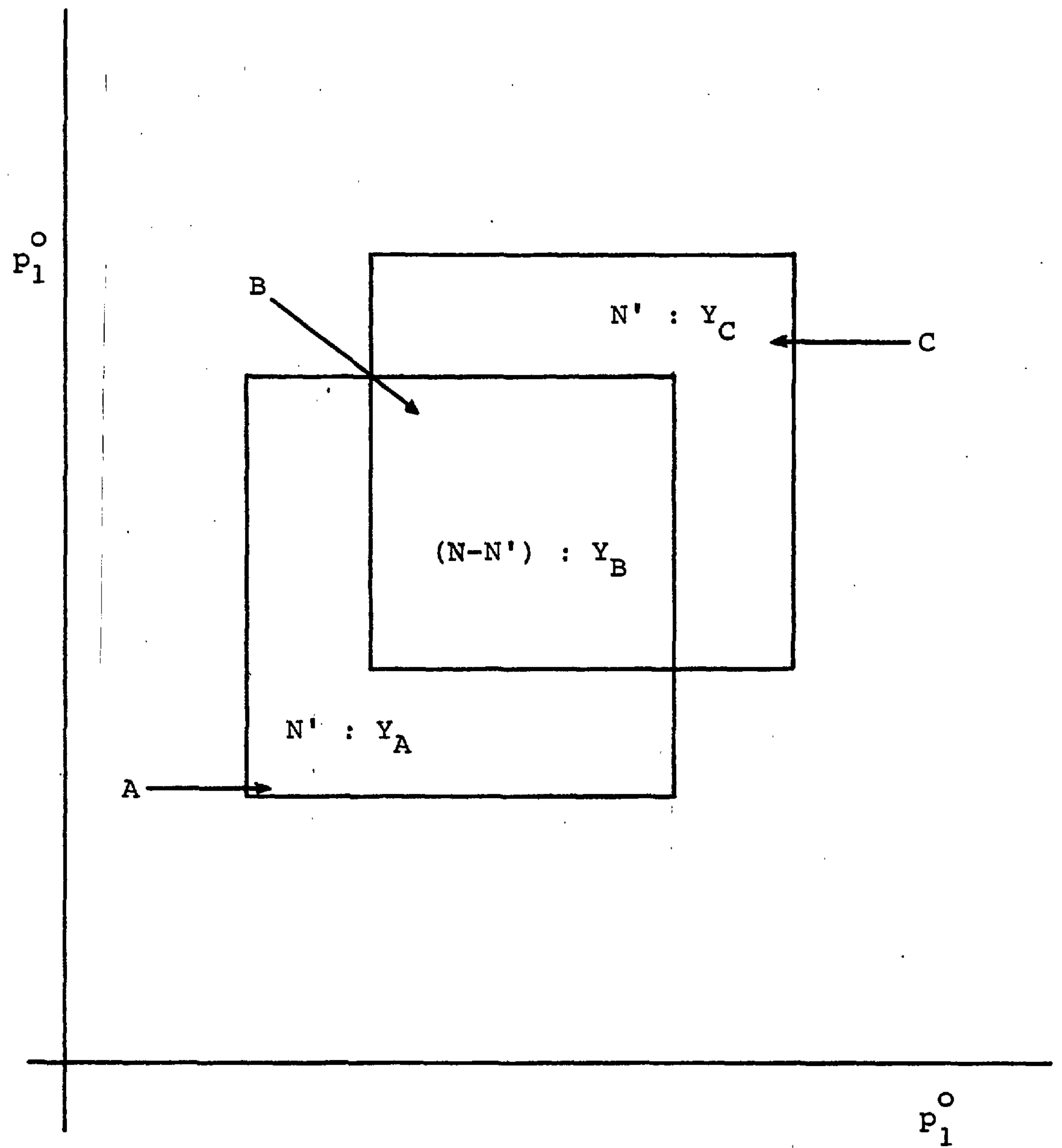


Figure 4.12: Illustrating Notation For The Distribution Of Sample Points In The Common Points Scheme.

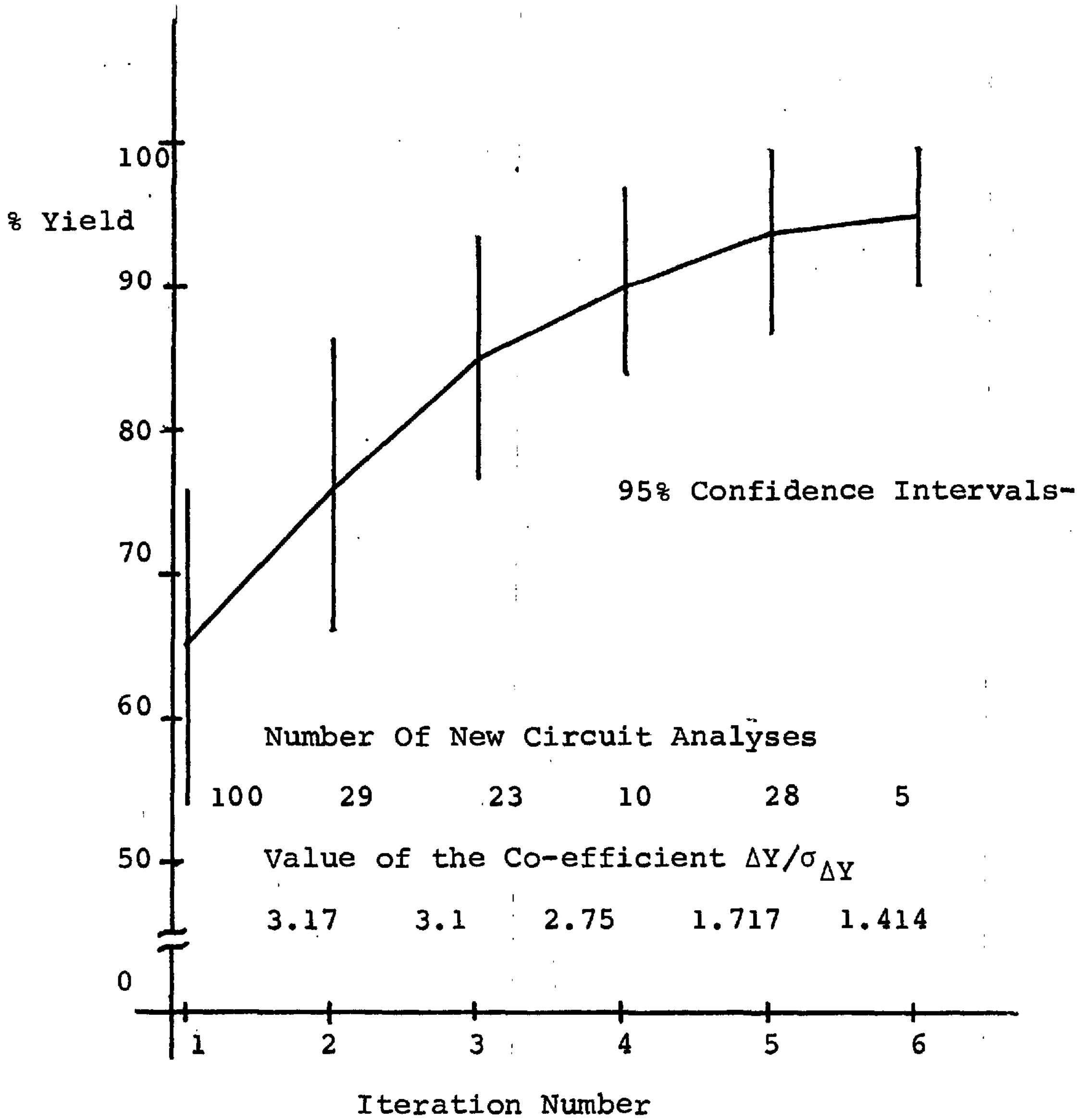


Figure 4.13: Yield Trajectory For A High Pass Filter Example: Demonstrating The Effectiveness Of The Common Points Scheme.

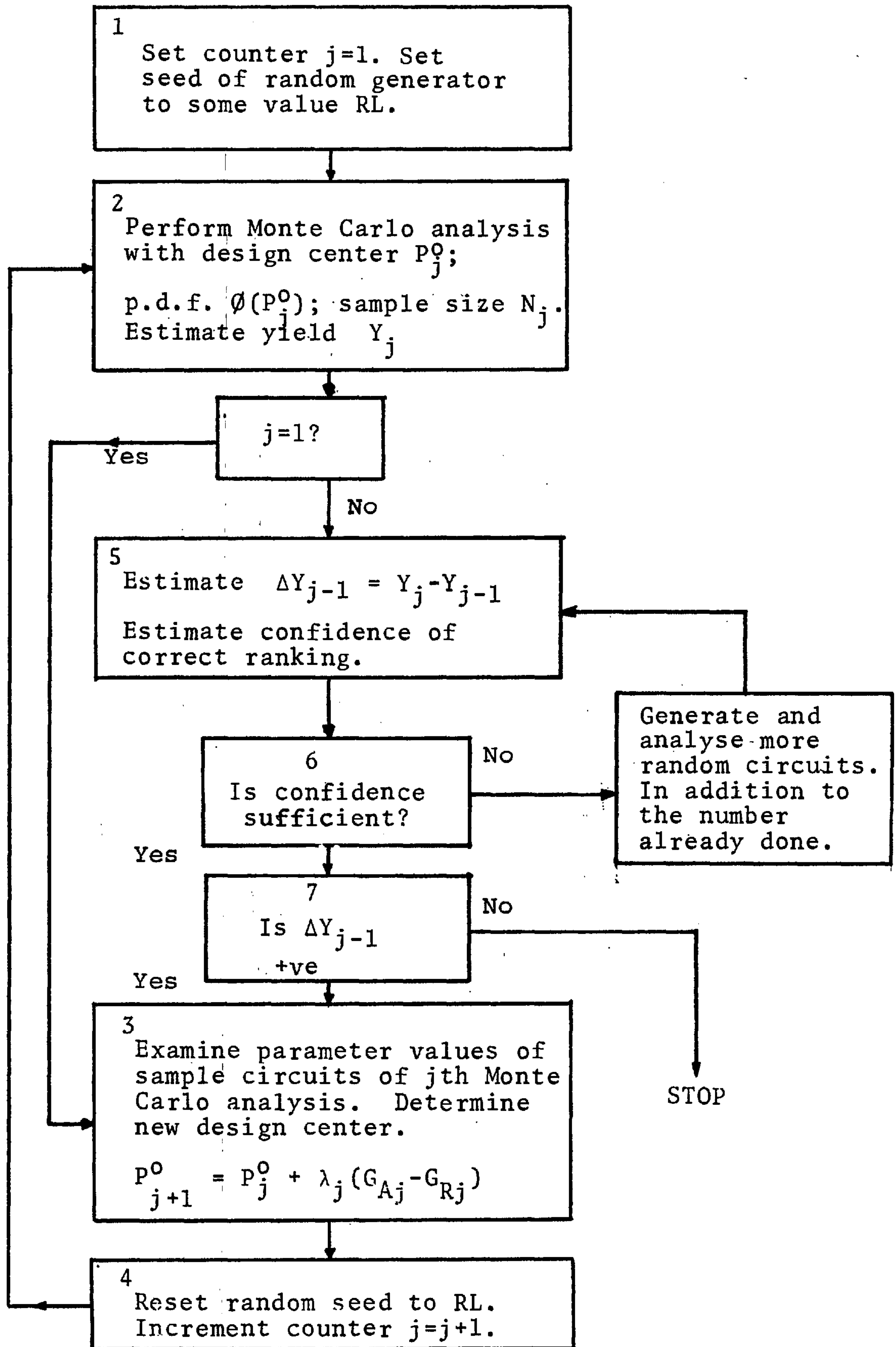


Fig. 4.14: Flow chart for a statistical exploration - design centering algorithm employing the correlated sampling scheme.

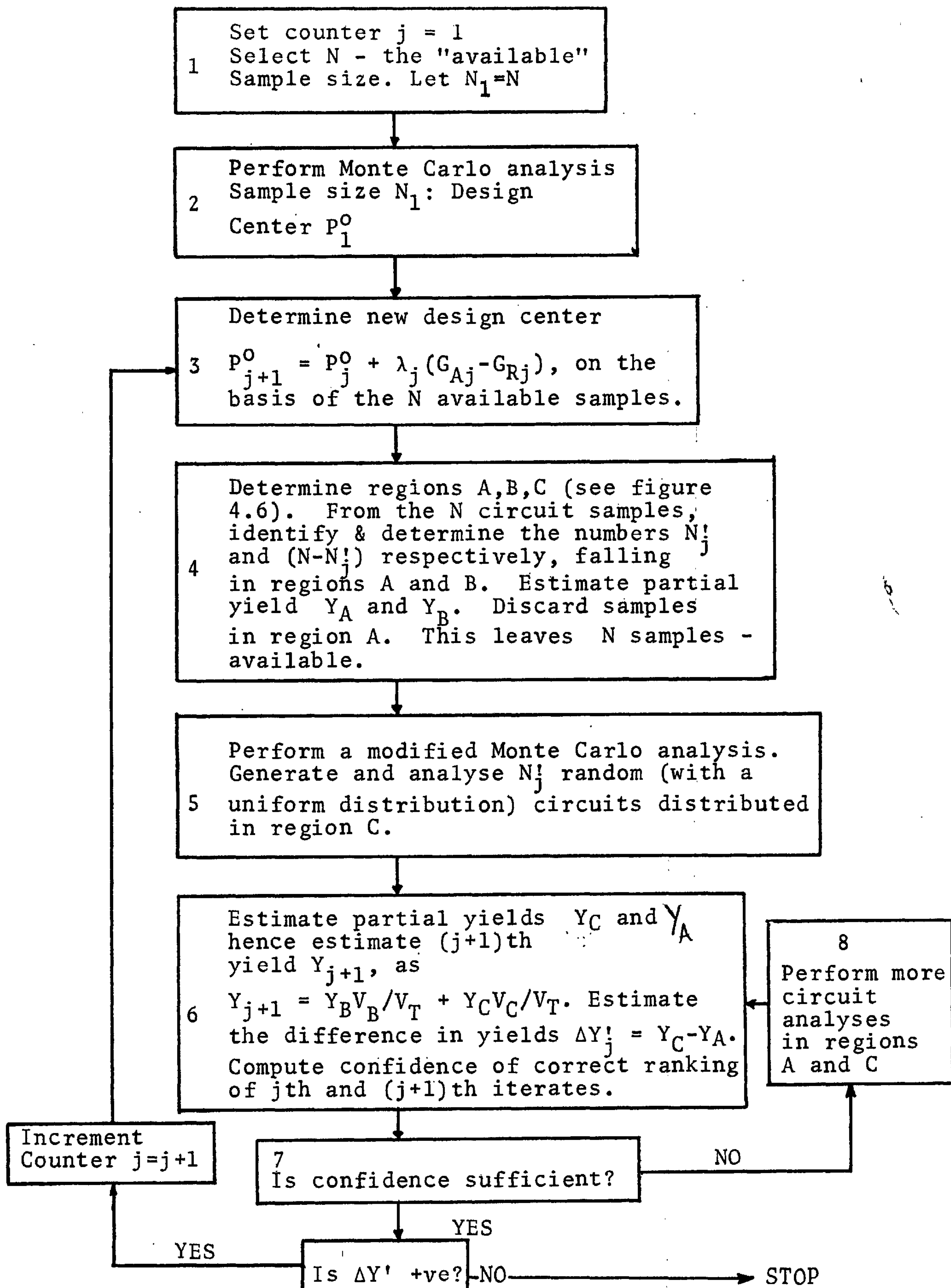
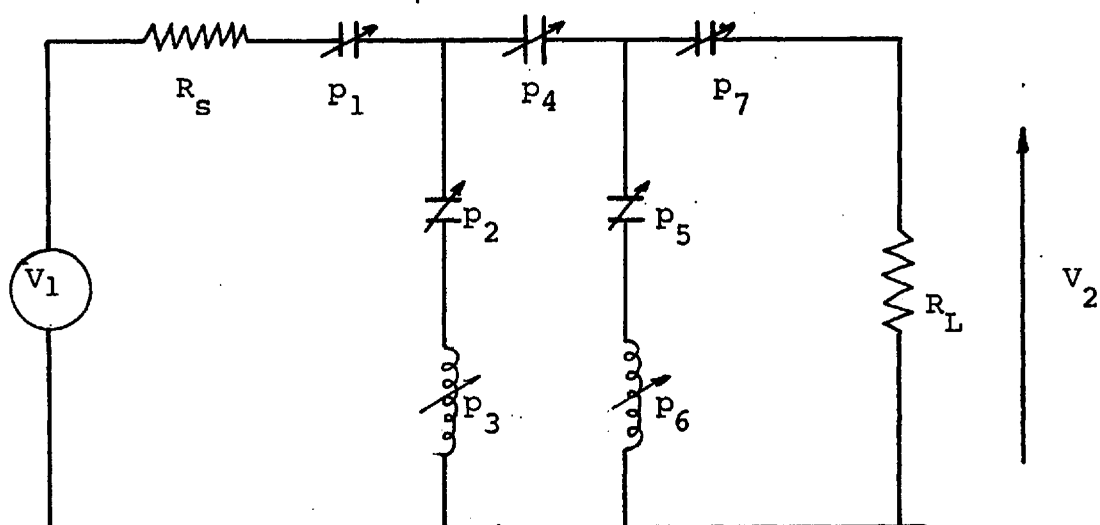


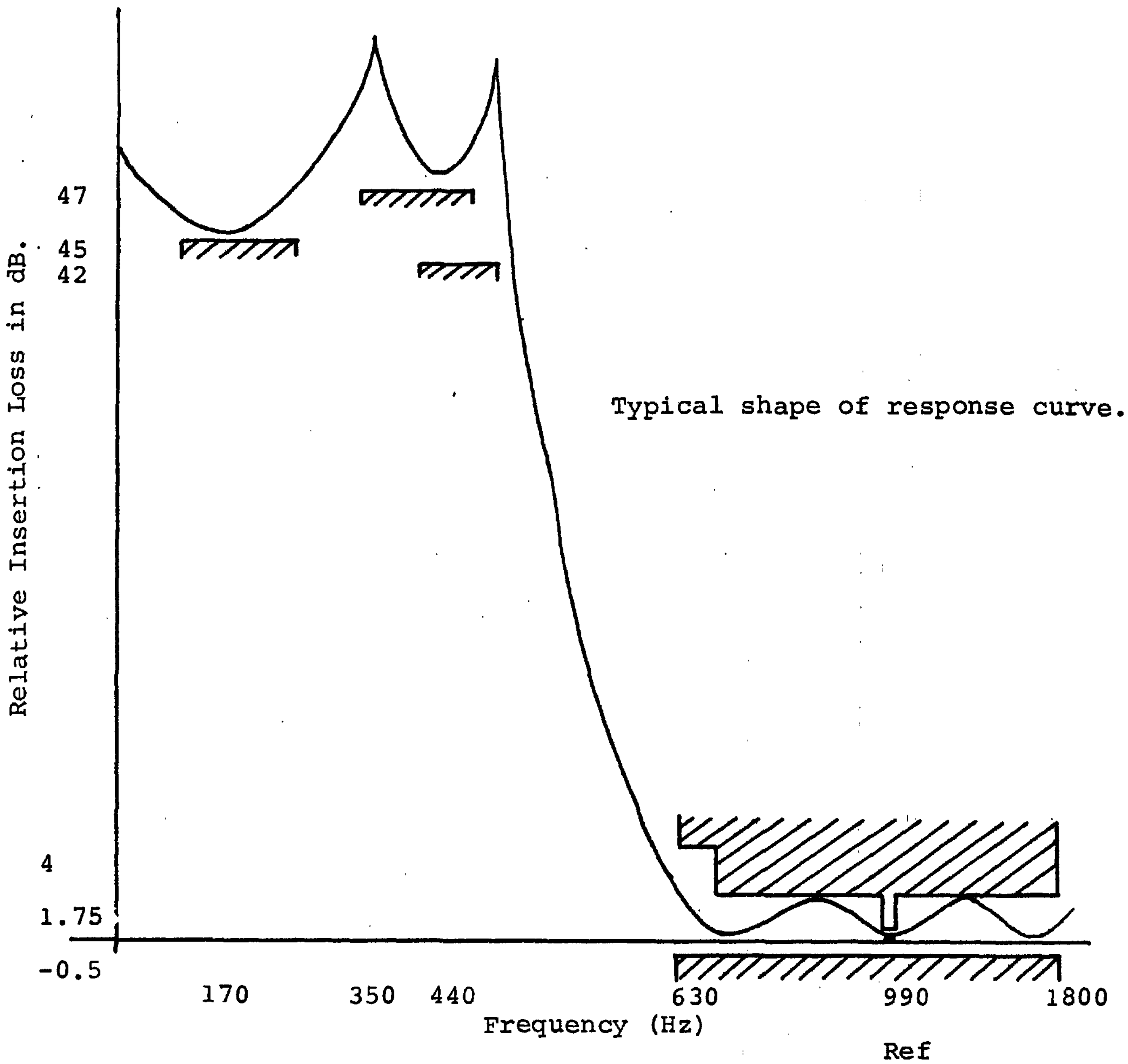
Fig 4.15: Flow chart for a statistical exploration - design centering algorithm employing the common points scheme.



Arrows indicate toleranced components.

Insertion Loss is $20\text{Log}|V_2(j\omega)/V_1(j\omega)|$

Figure 4.16: Circuit Diagram Of The Passive High Pass Filter Example.



Note: The frequencies tested are: 170 350 440 630 650 720 740 760 940 1040 1800 Hz.

Figur 4.17: Performance Requirements For The High Pass Filter.

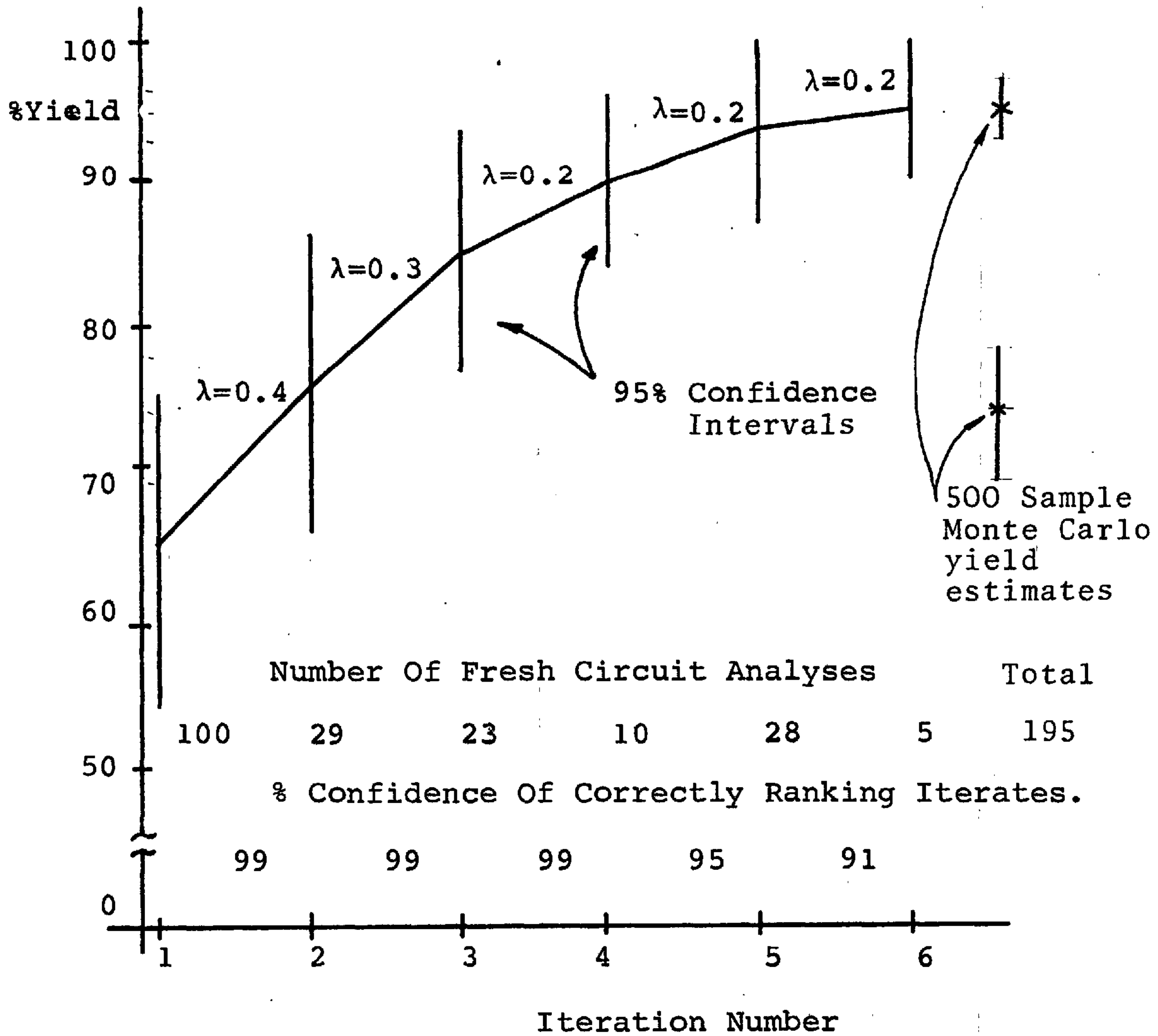


Figure 4.18: Yield Trajectory For The High Pass Filter Assuming 5% Tolerances and Uniform Distributions.

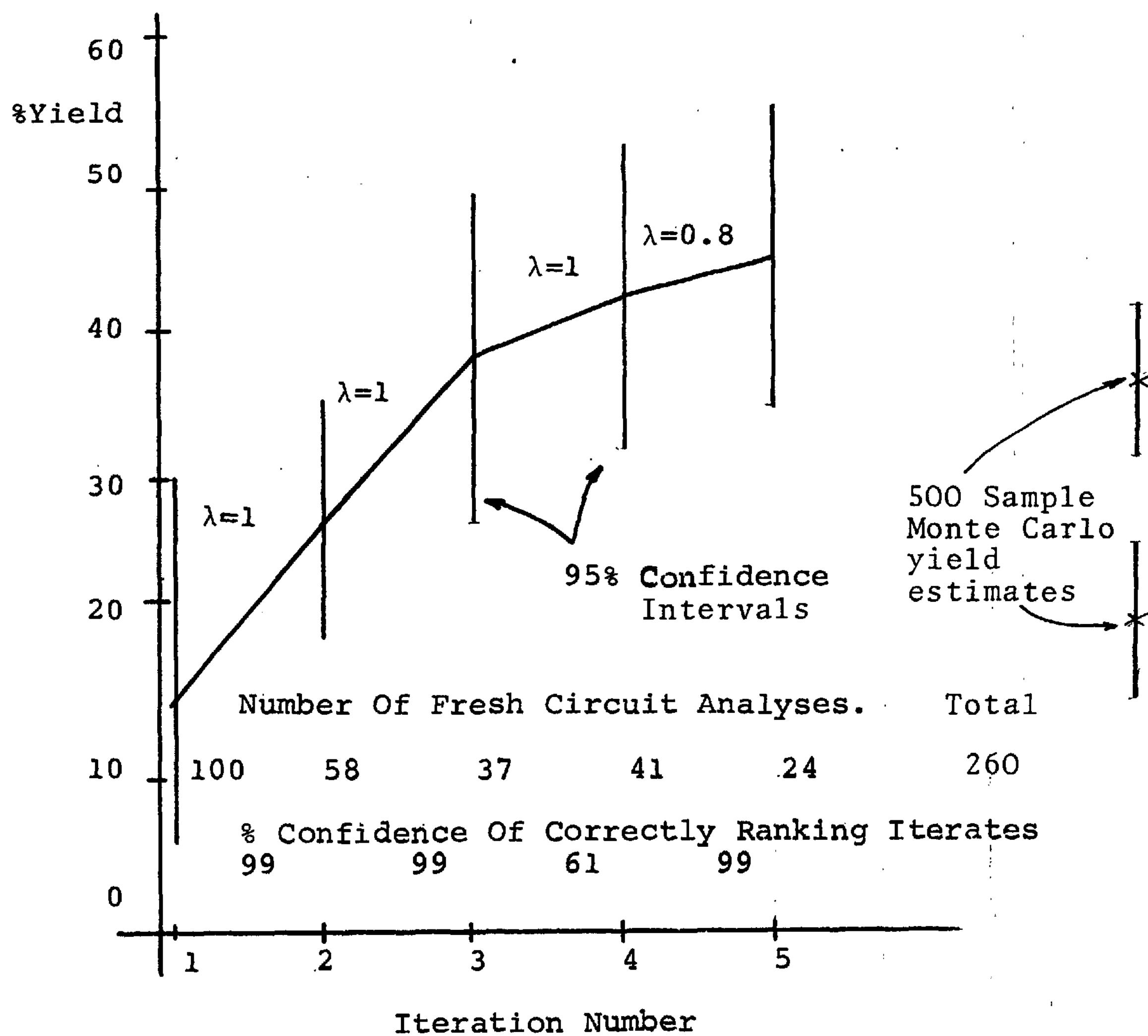


Figure 4.19: Yield Trajectory For The High Pass Filter Assuming 15% Tolerances And Uniform Distributions.

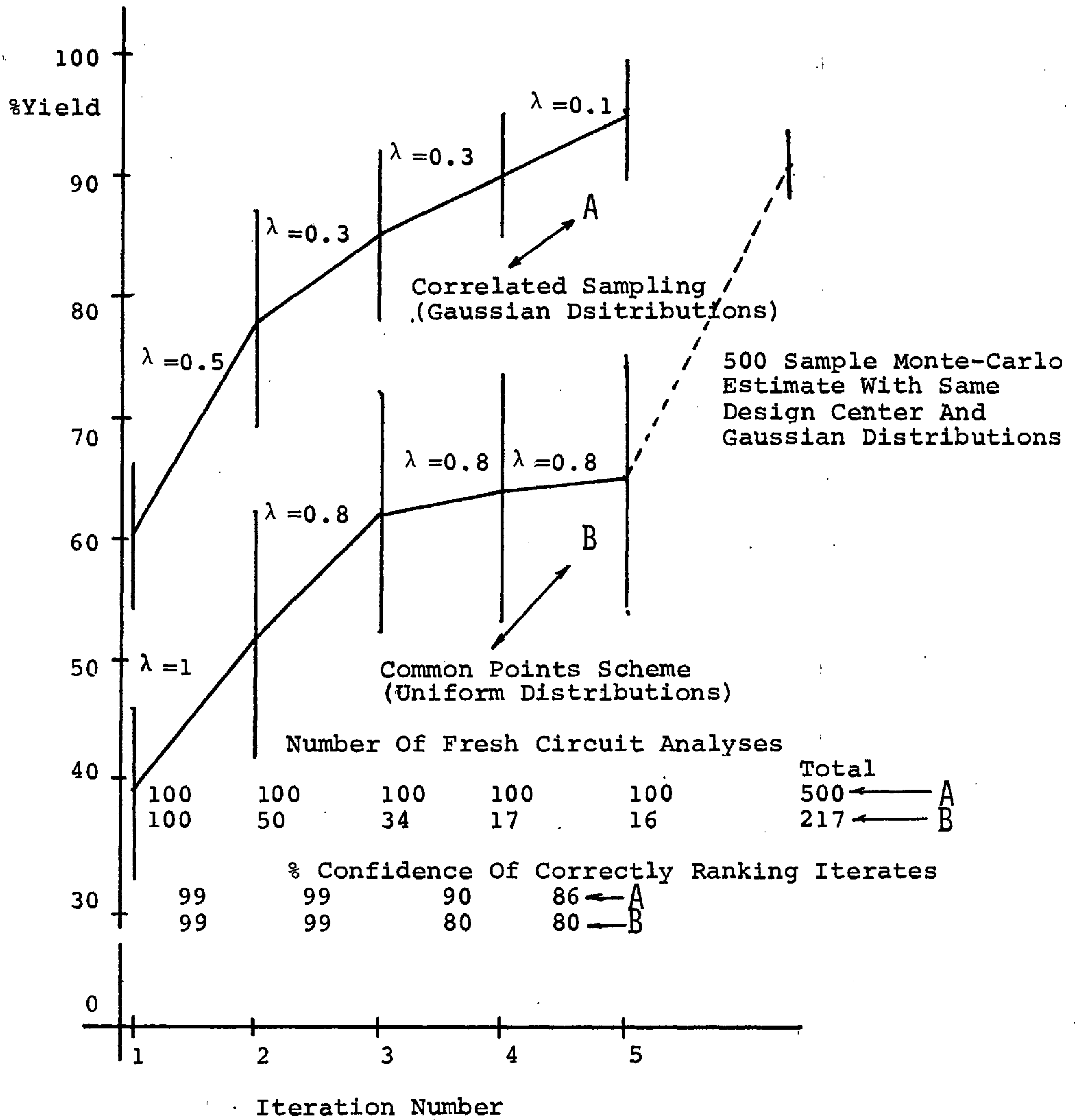


Figure 4.20 Yield Trajectories For The High Pass Filter Assuming 10% Tolerances And Uniform And Gaussian Distributions.

%Yield

λ=.4 λ=.3 λ=.2 λ=.2 λ=.1

The Same Design Center
As For Iteration No.6 But
With The Values Rounded
Off To The Nearest
Allowable Discrete Values.

95% Confidence Intervals

Iteration Number

Figure 4.21: Yield Trajectory For The Strategy Where Only The Final Solution Is Rounded Off

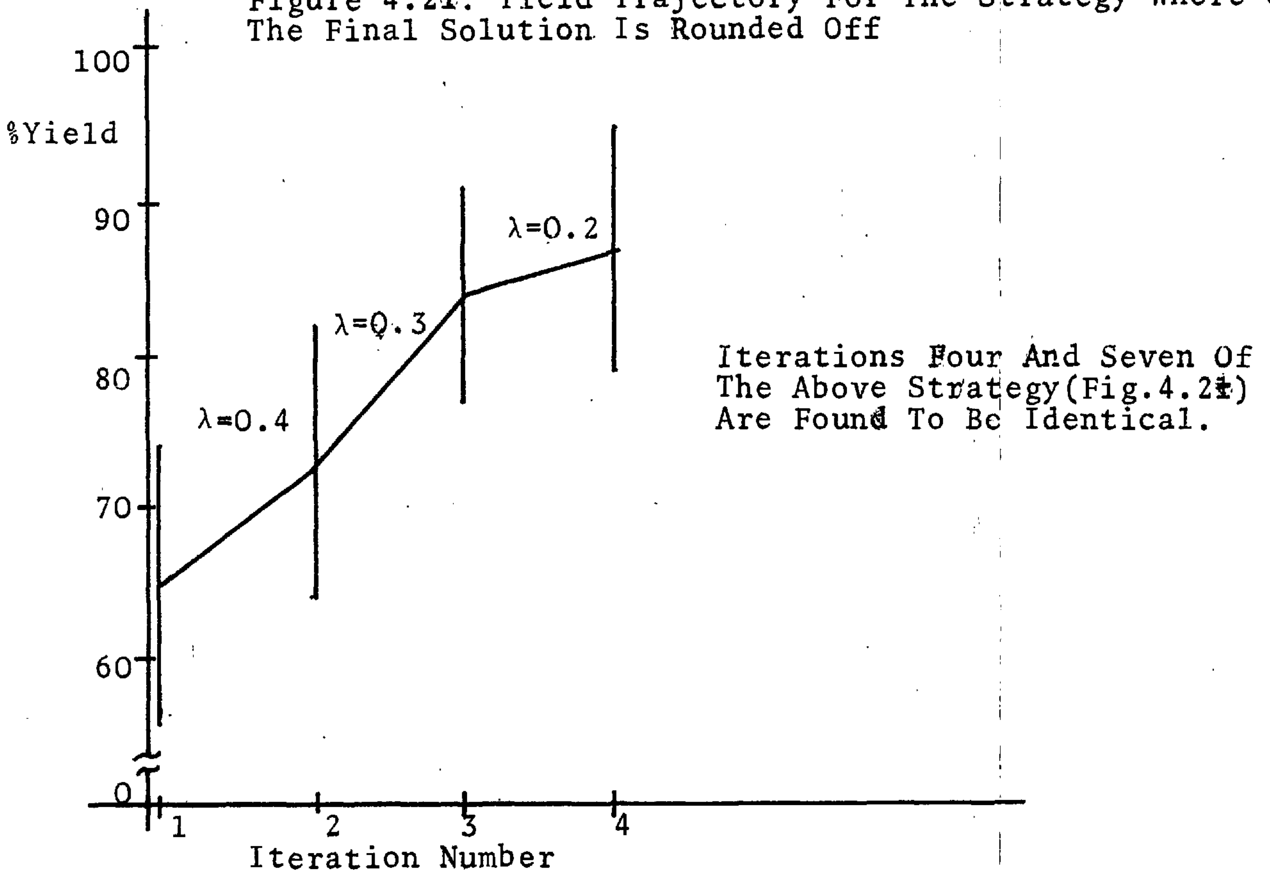


Figure 4.22: Yield Trajcetory For The Strategy Where Intermediate And Final Continuous Solutions Are Rounded Off.

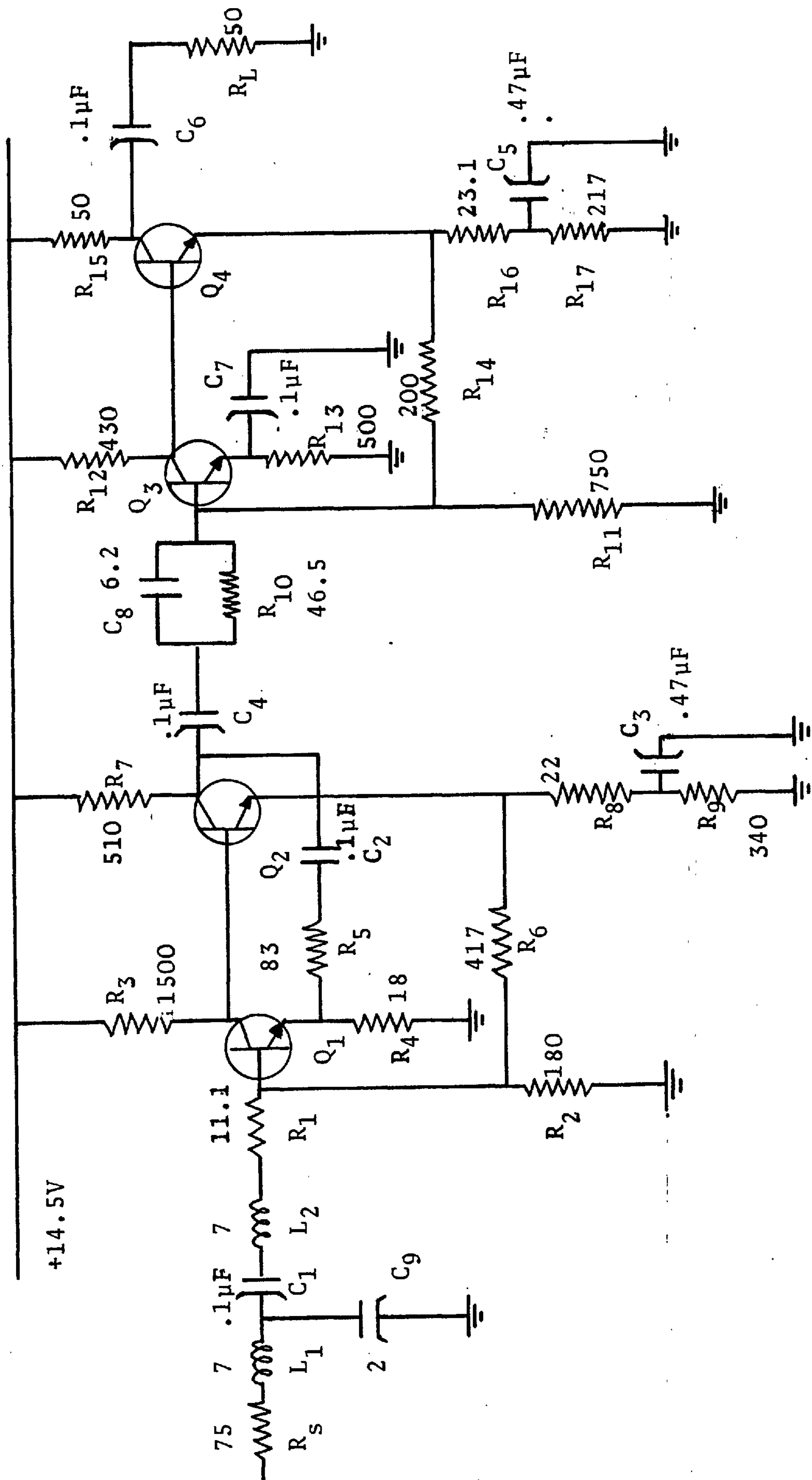


Figure 4.23: Circuit Diagram Of The High Frequency Amplifier Example, Including The D.C Biassing Components.

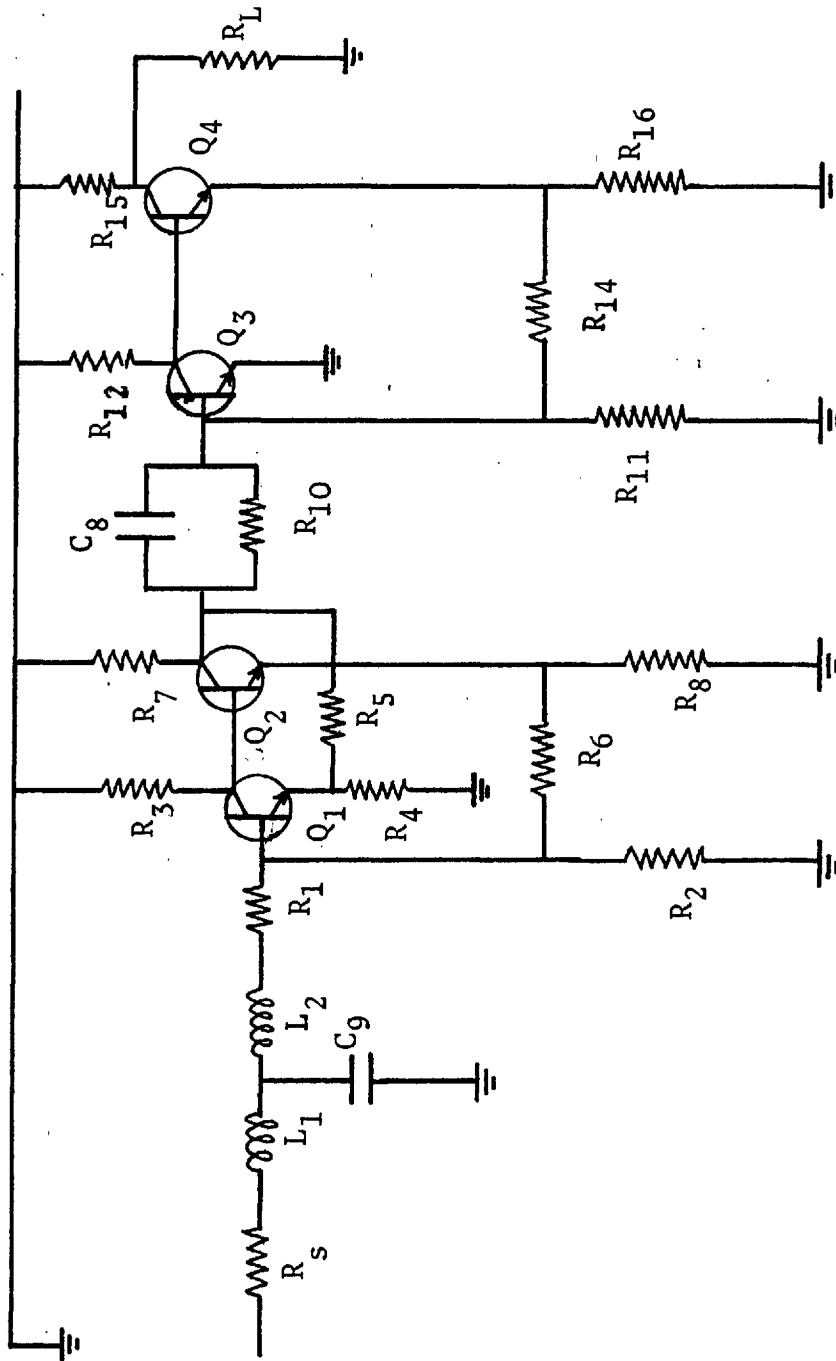
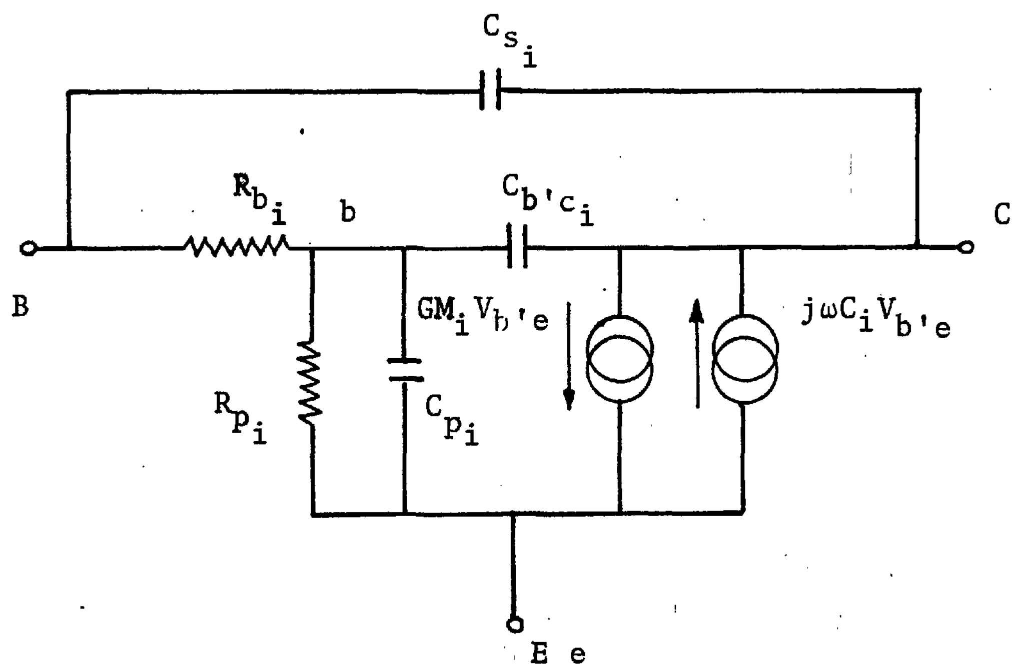


Figure 4.24(a) : Circuit Diagram Of The A.C.Equivalent Of The P.T.O For : High Frequency Amplifier.
Fig. 4.24(b).



Small Signal A.C Model Of The Transistors Used In The High Frequency Amplifier Circuit.

Q_i	R_{b_i} Ω	R_{p_i} Ω	C_{p_i} pF	$C_{b'c_i}$ pF	C_{s_i} pF	G_{M_i} ℧	C_i pF
1	15	210	10	0.4	0.4	0.286	4.6
2	15	114	18.6	0.4	0.4	0.525	4.6
3	15	123	17	0.4	0.4	0.48	4.6
4	12	33	115	0.5	0.5	1.8	23

Nominal Values Of The Transistor Parameters

Figure 4.24(b)

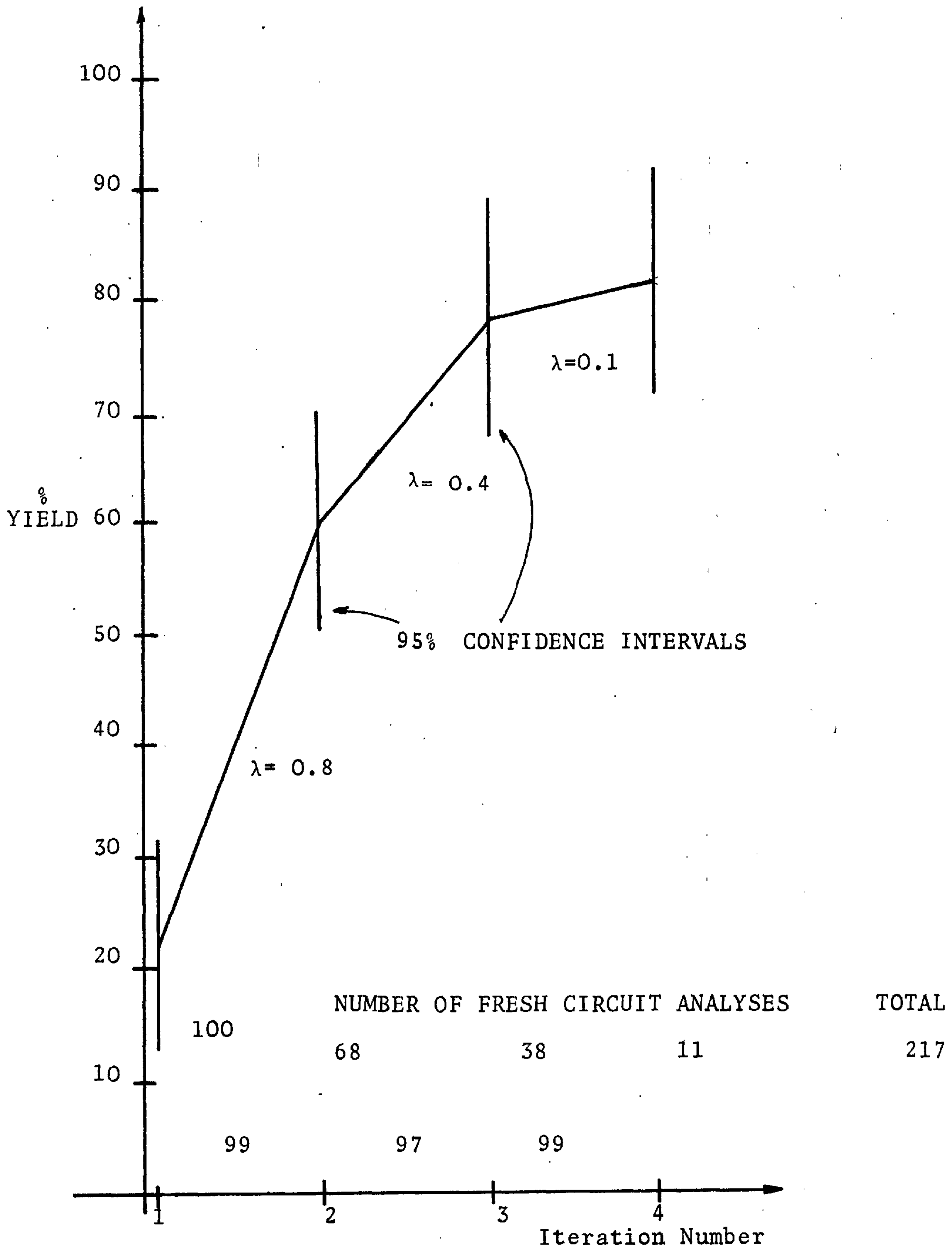


Figure 4.25 : Yield Trajectory Obtained By Application Of The Statistical Exploration - Design Centering Method To The High Frequency Amplifier Example

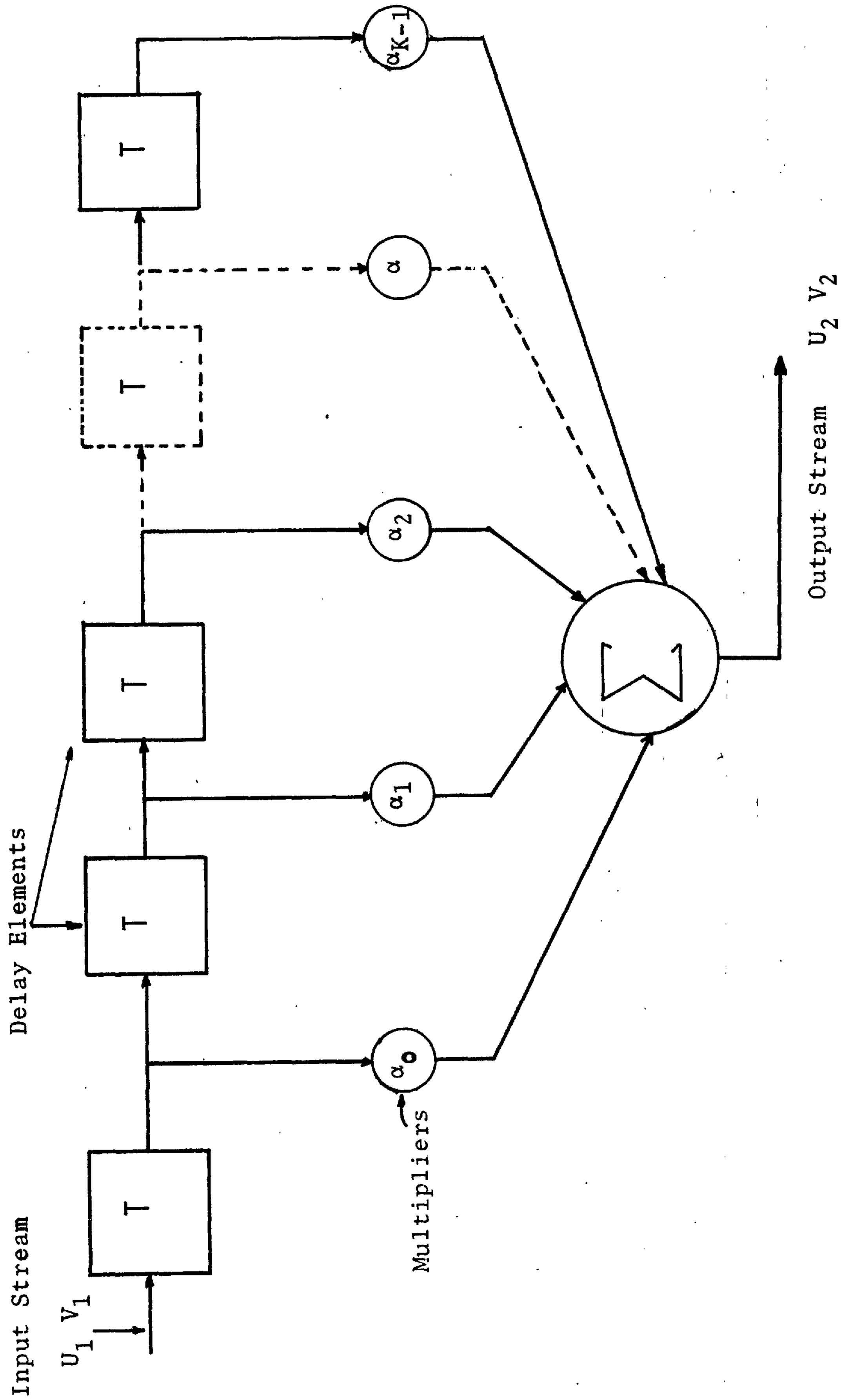


Figure 4.26: A General Structure For A Transversal Filter.

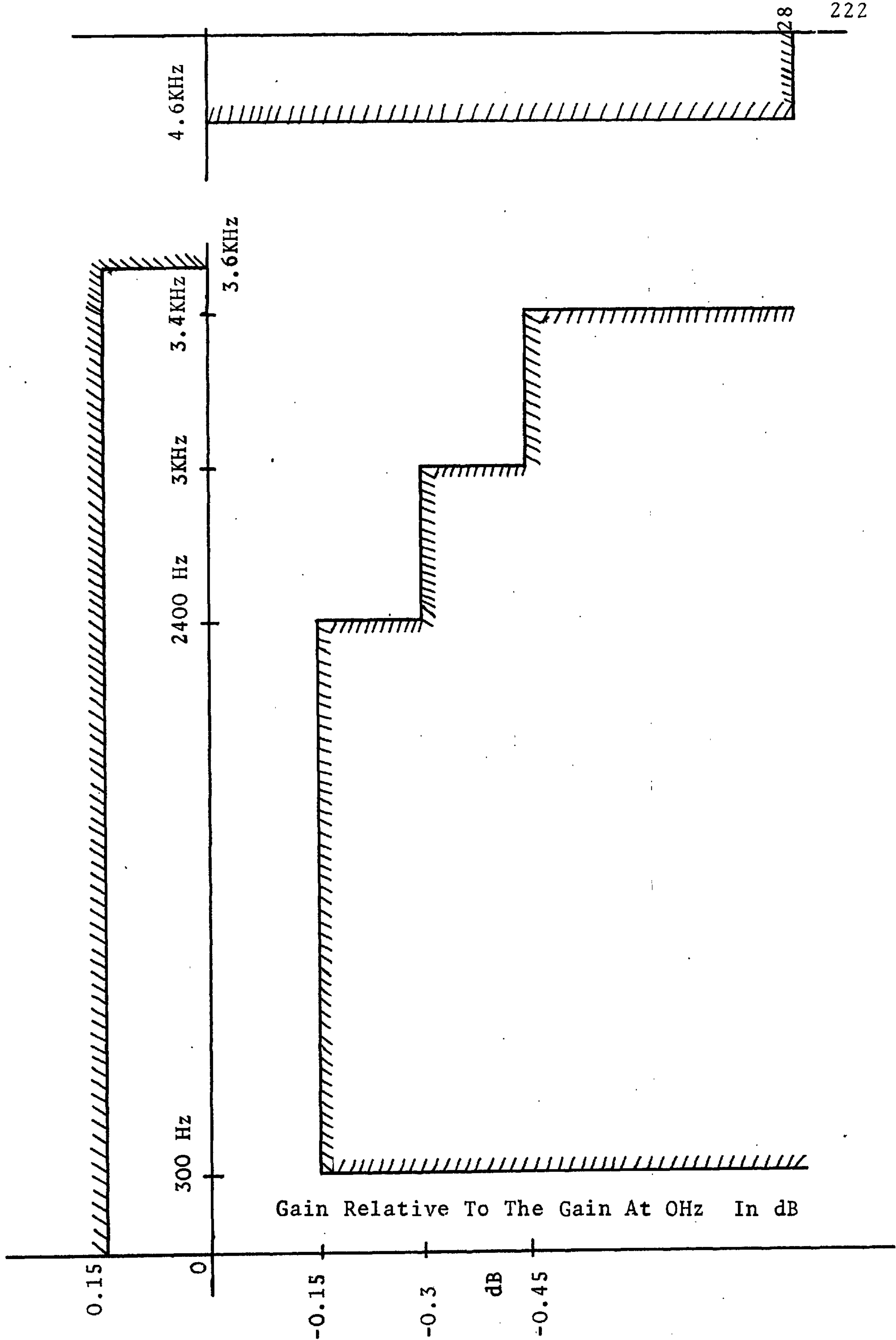


Figure 4.27 Performance Requirements For The Transversal Filter Example.

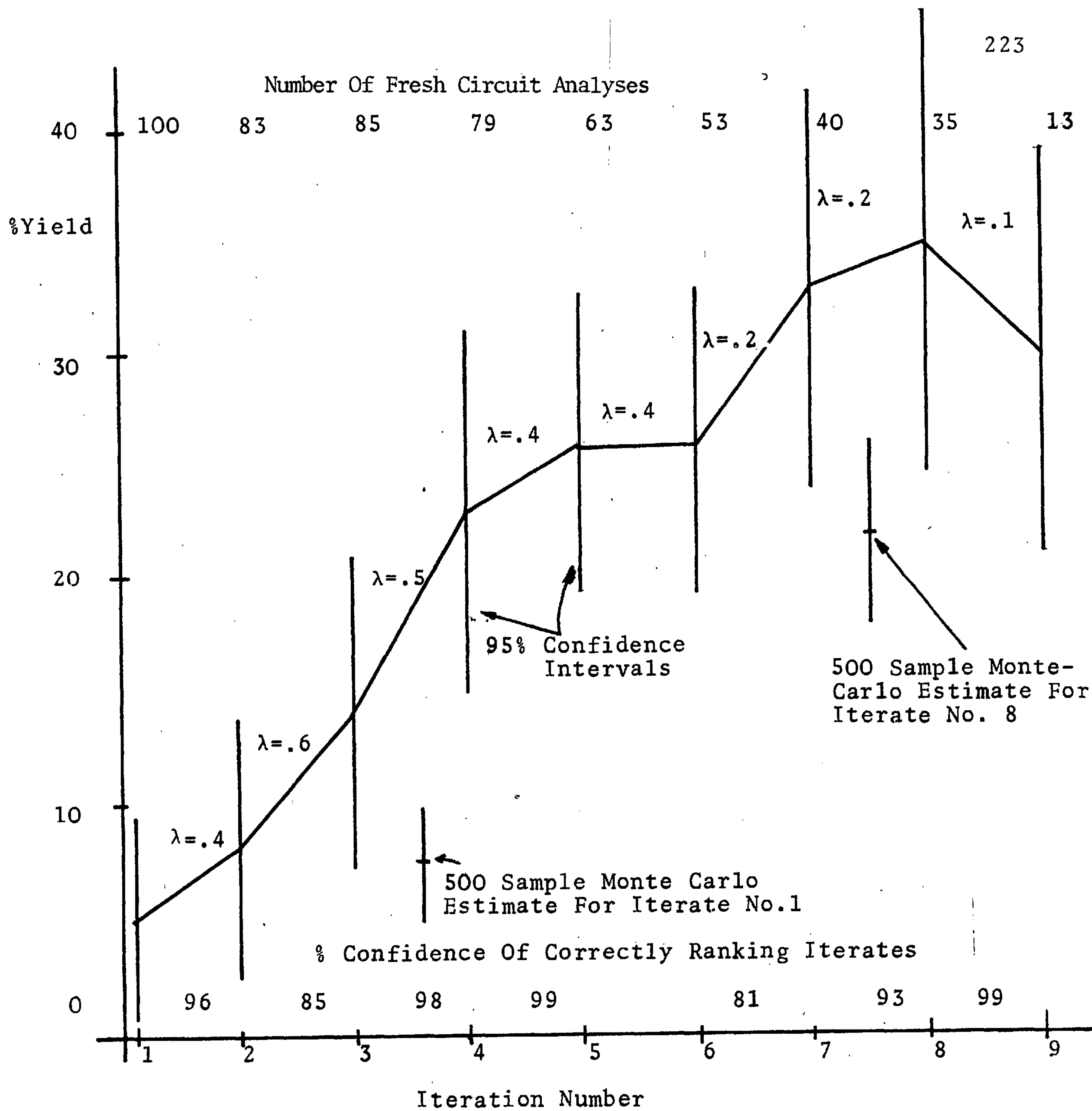


Figure 4.28: Yield Trajectory Obtained By Application Of The Statistical Exploration Design Centering Method To A 43 Variable Transversal Filter.

CHAPTER 5 - ITERATIVE MONTE CARLO BASED METHODS FOR TOLERANCE ASSIGNMENT.

5.1 Introduction.

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CHAPTER 5

ITERATIVE MONTE CARLO BASED METHODS FOR TOLERANCE ASSIGNMENT

5.1 INTRODUCTION

As discussed in chapters one and two certain algorithms are addressed to the problem of returning tolerance solutions which guarantee 100% yield, i.e. worst case solutions. However, the average cost of producing an acceptable circuit may be much reduced if a smaller yield is accepted. The latter situation allows larger tolerances and hence cheaper components to be employed. This may offset the additional cost incurred in discarding or repairing circuits whose performance does not meet requirements. Therefore the tolerance/yield trade-off may be explored to minimize overall cost.

In this chapter we examine a class of Monte Carlo based methods of tolerance assignment, where less than 100% yield is considered acceptable. The methods commence by performing Monte Carlo analysis while assuming large tolerances. In addition to estimating yield the results of the Monte Carlo analysis are employed to choose new tolerances. Another Monte Carlo analysis is performed with this new set of tolerances and the process is continued. At each iteration, tolerances are reduced and yield increased over that for the previous iteration. The particular criterion employed to re-assign tolerances distinguishes one method in this class from another.

5.2 PROBLEM FORMULATION

Yield estimation and tolerance assignment may be performed over several iterations thus exploring the yield-tolerance trade-off. Alternatively a cost function involving yield and tolerances may be formulated and minimized. For the situation where failing circuits are to be discarded, a suitable cost function is expression 2.5, which is repeated here:

$$C_U = \frac{C_A + \sum_{i=1}^{K} C_i(t_i)}{Y\{\emptyset(P^o, T)\}} \qquad 5.1$$

As before C_U is the unit cost, i.e. the cost of producing one acceptable circuit. C_A represents the sum of the tolerance independent or fixed costs, while $C_i(.)$ is the tolerance dependent cost function of the ith component. The manufacturing yield $Y(.)$ is defined in terms of the component parameter p.d.f. $\emptyset(.)$ and the performance requirements of the circuit, as detailed in chapter one.

For our present purpose we assume $\emptyset(.)$ to have a particular form e.g. multivariate uniform. The nominal values $P^o = p_1^o p_2^o \ldots\ldots p_K^o$ and associated tolerances $T = t_1 t_2 \ldots . t_K$ are taken as parameters of the p.d.f. Therefore it is sufficient to write yield as a function of P^o and T and to omit reference to $\emptyset(.)$. We may formally state the relevant optimization problem as:

Minimize

$$C_U = \frac{C_A + \sum_{i=1}^{K} C_i(t_i)}{Y(P^o,T)} \qquad 5.2$$

by appropriate choice of design center $P^o = p_1^o \; .... \; p_K^o$ and tolerances $T = t_1 \; .... \; t_K$.

In view of the complexity of the denominator (the yield) it is not possible in general to derive analytic properties of the objective function. Nevertheless, it is useful to consider a heuristic argument, which indicates that cost minima exist between the two extreme situations of high yield and low tolerances on the one hand, and low yields and large tolerances on the other.

The individual component cost functions are monotonically decreasing functions of tolerance. Therefore for large tolerances the functions $C_i(.)$ have small values and hence the numerator of 5.1 is approximately equal to the sum of the fixed costs i.e. C_A. However, for large tolerances the denominator (the yield) approaches zero. Therefore, the unit cost function has a large value. As the tolerances are decreased, the component costs become significant and the value of the numerator increases. If the rate of increase of the denominator (the yield) is greater than the rate of increase of the numerator (the sum of the fixed costs and the tolerance dependent costs) then the overall value of C_U becomes smaller.

At the extreme as tolerances become very small, yield approaches its maximum value of unity. The overall cost is then largely dependent upon the sum of the tolerance

dependent component costs, which are large with small tolerances. Therefore an approximately paraboloidal shape is envisaged for the function $C_U(.)$, with large values accruing for the two extreme cases of wide tolerances with low yields and narrow tolerances with high yields, and cost minima in between.

The methods discussed in this chapter commence with large tolerances. Monte Carlo analysis is performed and yield is estimated. Information about the distribution of pass and fail circuits provided by the Monte Carlo analysis is employed by an algorithm to re-assign tolerances. The Monte Carlo analysis is then repeated with the new tolerance values and yield is re-evaluated. The process is continued over several iterations. At each iteration tolerances are decreased in a way that increases yield. Therefore with reference to the above discussion of the unit cost function, the methods commence from one extreme situation, that is low yield and high tolerance, and progressively tighten tolerances and increase yield.

This chapter commences with the critical assessment of a previously reported algorithm called TOLERATE /Elias,2 /. The results of a theoretical and practical investigation of TOLERATE are presented. A number of shortcomings of this method are highlighted. To improve upon the capabilities of TOLERATE we introduce a novel technique called PERTOL (PERcentile based TOLerance assignment). Practical results of a comparison of both methods when applied to the same circuit examples are presented. These demonstrated the general superiority of PERTOL over TOLERATE.

Before embarking on further discussion, some additional notation employed in this chapter is clarified. Previously a nominal value p_i^o and corresponding absolute tolerance t_i implied component values p_i distributed in the range $(p_i^o - t_i) \leq p_i \leq (p_i^o + t_i)$ with p.d.f. $\phi_i(p_i, p_i^o, t_i)$. In Monte Carlo based tolerance assignment procedures it is found more appropriate to consider limit values. These are the extremes of the tolerance range of each component. For example $L_i = (p_i^o - t_i)$ and $U_i = (p_i^o + t_i)$ are respectively the lower and upper limit values of the ith component. Clearly $p_i^o = (U_i + L_i)/2$ and $t_i = (U_i - L_i)/2$. The iterative algorithms to be described in this chapter assign limit values to parameters from which the tolerances and nominals are inferred.

5.3 THE TOLERATE METHOD

5.3.1 AN OVERVIEW

The general structure of the TOLERATE method is ullustrated in figure 5.1. For the jth iteration, the INTERPRETER examines the results of the Monte Carlo analysis and re-assigns limit values as follows.

Let us say the Monte Carlo analysis comprised the testing of a number N_j of random sample circuits with component values distributed according to $\phi(P_j^o, T_j)$. The N_j sets of component values are separated into a pass list and a fail list of sizes N_{jP} and N_{jF} respectively. The pass list comprises the circuits which meet all performance requirements and the fail list those which fail to meet at least one performance requirement. For each component, histograms representing

the conditional probability density function /9, chapter 5/ $Pr(p_i/pass)$ and $Pr(p_i/fail)$; i=1 ... K, are constructed from these lists and the limit values and hence tolerances and nominals are revised. This is illustrated in figure 5.2.

For the sth component new limit values $L_{s,j+1}$ and $U_{s,j+1}$ are selected such that:

$$Pr(p_s/pass) \geq \lambda_s \, Pr(p_s/fail) \qquad \text{for all} \quad L_{s,j+1} \leq p_s \leq U_{s,j+1} \tag{5.3}$$

where λ_s is a positive constant.

The criterion 5.3 is illustrated in figure 5.2. To demonstrate the main features of the TOLERATE method, we introduce a band pass filter example /38/ whose circuit diagram, performance requirements and typical shape of response are shown in figures 5.3 and 5.4. Figures 5.5 to 5.12 show a series of results obtained by application of the TOLERATE method to this circuit example. Each of the diagrams depicts yield-tolerance trajectories for one of the eight toleranced components. The trajectories marked A and B correspond to the TOLERATE method. Trajectory C on the other hand is obtained by application of the PERTOL method and should be ignored in the present discussion. Trajectories A and B correspond to choices of 0.8 and 1 respectively for the constant λ_s, s=1...8, in criterion 5.3.

The implications on yield of tolerance assignment according to 5.3 are examined in the next section. In this method, tolerance re-assignment is not necessarily performed for

all components subject to variability. Instead a particular type of sensitivity analysis based on a parameter termed "yield sensitivity" is performed. Tolerance re-assignment is then carried out for those components whose yield sensitivity exceeds a particular value specified by the designer. The definition of yield sensitivity and its practical computation are discussed in section 5.3.3.

5.3.2 THE TOLERANCE ASSIGNMENT CRITERION

(a) Implication on Yield

To appreciate the rationale behind expression 5.3 we consider initially the situation where the tolerance of only one component parameter is to be revised. The yield for the jth iterate is:

$$Y_j = Pr(pass) \qquad 5.4$$

Also we assume that for iteration j+1, the new limit values $L_{s,j+1}$ and $U_{s,j+1}$ are chosen such that

$$Pr(p_s/pass) \geq \lambda_s \, Pr(p_s/fail) \qquad 5.5$$

for all p_s within the range $Ls,_{j+1} \leq p_s \leq Us,_{j+1}$

and for $\lambda_s \geq 1$.

Criterion 5.6 differs from criterion 5.3 because the value of λ_s is required to be greater than zero in 5.3 and greater than one in 5.5. Further, assuming that the parameter p_s is uniformly distributed, the new yield will be:

$$Y_{j+1} = Pr\,(pass/Ls,_{j+1} \leq p_s \leq Us,_{j+1}) \qquad 5.6$$

To enhance clarity we introduce the following additional notation:

A is the event : $Ls_{,j+1} \leq p_s \leq Us_{,j+1}$

B is the event : A random circuit is a pass at iterate j.

C is the event : A random circuit is a fail at iterate j.

Then we can re-write (5.4) and (5.6) as:

$$Y_j = Pr\ (B) \qquad 5.4$$

and

$$Y_{j+1} = Pr(B/A) \qquad 5.6$$

We wish to show that a choice of $Ls_{,j+1}$ and $Us_{,j+1}$ according to (5.5) results in an increase in yield, i.e. $Y_{j+1} > Y_j$.

Using Bayes rule /9,chapter 12/, (5.6) may be re-written as:

$$Y_{j+1} = \frac{Pr\ (Ls_{,j+1} \leq p_s \leq Us_{,j+1}/Pass)}{Pr(Ls_{,j+1} \leq p_s \leq Us_{,j+1})} \quad Pr(pass)$$

or

$$Y_j = \frac{Pr(A/B)}{Pr(A)} \quad Pr(B) \qquad 5.7$$

substituting Y_j for $Pr(B)$;

$$Y_{j+1} = \frac{Pr(A/B)}{Pr(A)} \quad Y_j \qquad 5.8$$

Clearly $Pr(A/B) > Pr(A)$ implies $Y_{j+1} > Y_j$ 5.9

Now from elementary probability theory, we may say:

$$Pr(A) = Pr(A/B)Pr(B)+Pr(A/C)Pr(C) \qquad 5.10$$

However, $Pr(B) + Pr(C) = 1$; i.e. $Pr(Pass) + Pr(fail) = 1$.

Therefore (5.10) may be re-written as:

$$Pr(A) = Pr(A/B)Pr(B) + Pr(A/C)\{1-Pr(B)\}$$

Or rearranging

$$Pr(A)-Pr(A/C) = Pr(B)\{Pr(A/B) - Pr(A/C)\} \qquad 5.11$$

Now our choice of $Ls,_{j+1}$ and $Us,_{j+1}$ acc ding to (5.5) ensures that:

$$\{Pr(Ls,_{j+1} \leq p_s \leq Us,_{j+1}/Pass) = \int_{Ls,_{j+1}}^{Us,_{j+1}} Pr(p_s/pass)dp_s\} >$$

$$\{Pr(Ls,_{j+1} \leq p_s \leq Us,_{j+1}/fail) = \int_{Ls,_{j+1}}^{Us,_{j+1}} Pr(p_s/fail)dp_s\} \qquad 5.12$$

Relation (5.12) may be re-written as:

$$Pr(A/B) - Pr(A/C) > 0 \qquad 5.13$$

The meaning of relation (5.12) or (5.13) is illustrated in figure 5.13 (a).

We also know that $0 \leq \{Pr(B) = Y_j\} \leq 1$ 5.14

Therefore substituting (5.13) and (5.14) into (5.11), we can say that:

$$Pr(A/B) - Pr(A/C) > Pr(A) - Pr(A/C)$$

i.e., $Pr(A/B) > Pr(A)$ 5.15

Relation (5.15) is the desired result. Reconsidering (5.8), it can be seen that (5.15) ensures that

$$Y_{j+1} > Y_j \qquad 5.16$$

The above development has shown that for the case of uniform distributions, and where a single component is considered, a choice of limit values according to (5.5) ensures that yield is increased.

Now criterion (5.5) assumes that λ_s has a value greater than unity. Such a choice of λ_s ensures that (5.12) or (5.13) definitely hold. However, $\lambda_s \geq 1$ is not a necessary precondition for (5.12) to hold. That is (5.12) can also be satisfied by values of λ_s less than unity. One such case is illustrated in figure 5.13(b).

The greater the value of λ, the greater is the tightening of tolerances between iterates. Typically a choice of $\lambda_s \geq 1$ represents overdesign in practical cases. Figure 5.13(C) shows a choice of limit values for $\lambda_s > 1$. The overdesign can also be seen from the yield-tolerance trajectories (A and B) depicted in figures (5.5) to (5.12). For this example the choice of λ=1 generally provides tighter tolerance solutions for similar values of yield than a choice of $\lambda = 0.8$.

The development of the tolerance assignment criterion assumed that the tolerance of only one component was to be tightened. A criterion parallel to 5.3, for the case where the tolerance assignment of a number of components is considered, cannot easily be derived. Nevertheless in practical cases (e.g. figures 5.5 to 5.12) a choice of limit values for each component according to (5.3) is found to give satisfactory results.

(b) Some Practical Considerations

We now discuss practical aspects of choosing limit values according to the TOLERATE criterion.

The range $Ls_{,j+1} \leq p_s \leq Us_{,j+1}$ for which criterion (5.3) is satisfied is determined from histograms of the conditional p.d.fs $Pr(p_s/pass)$ and $Pr(p_s/fail)$. These histograms are constructed from the results of the Monte Carlo analysis. Certain practical difficulties are encountered in identifying the range of values of the parameter p_s for which (5.3) holds. These necessitate a modification to 5.3 as discussed below.

In figures (5.14) to (5.20), we show histograms corresponding to the pass and fail conditional p.d.f.s of each of the toleranced components of the high pass filter example (chapter 4, figure 4.16 and 4.17). Each figure (figures 5.14 to 5.20) shows two pairs of histograms. The pairs labelled as A were constructed using 10 class intervals, while the pairs labelled B were constructed using 15 class intervals. The Monte Carlo analysis tested 500 sample circuits. The numbers of passing and failing circuits was 286 and 214 respectively.

Initially consider component No. 2, for which results are shown in figure 5.14. Consider the two histograms constructed with 10 class intervals (i.e. pair A). Both histograms employ an identical set of class intervals. Also since the histograms are representations of probability density functions, the total area represented by the bars in either histogram is unity. The sum of the heights of the bars in each histogram

has been normalized to unity. Therefore to identify the range over which 5.3 holds for various values of λ, we compare the heights of the bars for corresponding class intervals of the pass and fail conditional histograms. The logical vectors RI(1), RI(0.8) and RI(0.5) summarize such a comparison.

Each of the vectors RI(.) has 10 elements, and each element corresponds to one of the ten class intervals. For example the first element of RI(1) is 1 if the height of the first class interval of the pass histogram is greater than that of the fail histogram and is 0 otherwise. Similarly, the first element of RI(0.8) is 1 if the height of the first class interval of the pass histogram is greater than 0.8 multiplied by the height of the first class interval of the fail histogram and is 0 otherwise.

To identify the range for which 5.3 holds we consider the class intervals corresponding to logical 1's in the appropriate RI(.) vector. In the case of component No. 2, for a choice of λ_2 equal to 1, this range will be disjoint. A similar occurrence may be observed for the three choices of λ for the case of 15 class intervals and similarly for other components (figures 5.14 to 5.20).

The disjoint tolerance ranges imply that the tolerance solution indicated by the procedure is not unique. To overcome this difficulty we have modified criterion 5.3 to the following.

Choose $Ls_{,j+1}$ and $Us_{,j+1}$, such that for all $p_s < Ls_{,j+1}$ and $p_s > Us_{,j+1}$ the following holds

$$Pr(p_s/pass) < \lambda_s \, Pr(p_s/fail) \qquad 5.17$$

Criterion 5.17 therefore means that the new tolerance range is bracketed by the first and last occurrence of a 1 in the appropriate RI(.) vector, for the particular value of λ_s chosen by the designer. This is indicated for component No. 4 in figure 5.16. In fact, the yield tolerance trajectories (A and B) of the band pass filter example shown in figures 5.5 to 5.12 were obtained by application of this modified criterion, i.e. (5.17).

5.3.3 YIELD SENSITIVITY

The mathematical development from expression 5.7 to 5.16 has been based upon the tolerance assignment of a single component per iteration. However, such a procedure would require a large number of iterations and incur a prohibitive computational cost for most circuit examples of interest. Therefore in practice, tolerance assignment is performed simultaneously for a number of toleranced components. On the other hand it is desirable to choose new tolerances only for those components which have a substantial effect on yield.

In the TOLERATE method, a parameter called "yield sensitivity" is introduced. Between successive iterations, tolerances are tightened only for those components whose yield sensitivity exceeds a certain arbitrary level specified by the circuit designer. Formally, the yield sensitivity for the ith

component is defined as:

$$M_i = \int_{-\infty}^{\infty} |Pr(p_i/pass) - Pr(p_i/fail)| dp_i \qquad 5.18$$

This definition is illustrated in figure 5.21 (a). Clearly M_i is a measure of the amount of overlap between the pass and fail conditional p.d.f.'s of the ith component. This definition assumes that if the overlap between the p.d.f.'s is high then the parameter has a small effect on yield and vice-versa. Figure 5.21 (b), (c) and (d) demonstrate the situation corresponding to low, intermediate and high yield sensitivities respectively. The actual numerical value of M_i can range from 0 to 2.

Commonly, sensitivity measures relate changes in the value of particular performances to changes in component values. By analogy, yield sensitivity of a component could have been defined as the rate of change of yield with the tolerance of the component, for example $\Delta Y/\Delta t_i$, where ΔY is the change in yield due to a particular change Δt_i in the tolerance of the ith component. However, such a sensitivity measure is difficult to compute. If a perturbation method is employed then a fresh Monte Carlo analysis is needed to compute the yield sensitivity of each component. Thus the computational effort required to compute yield sensitivity defined in this way is prohibitive.

In contrast yield sensitivity as defined by Elias is an overall sensitivity measure indicating the dependence of the occurrence of passing and failing circuits on the values of particular component parameters. In practice however yield sensitivity

(as defined in 5.19) can be an ambigiuous measure of a component's influence on yield. For a qualitative appreciation one may consider the histograms shown in figures 5.14 to 5.20. For every component the conditional p.d.f's overlap considerably and the numerical values of the yield sensitivities are low (see table 5.1). Typically, the histograms show heavy overlap. This detracts from the heuristic support lent to the TOLERATE method by the idealized situation depicted in sketches of the form shown in figure 5.2.

Table 5.1 shows the value of the yield sensitivity for each of the components and the variation of these values with the number of class intervals employed to compute them. Adjacent to each value of yield sensitivity we indicate the sensitivity ranking (highest sensitivity 1st) of the particular component. It can be seen that the value of yield sensitivity and the sensitivity ranking of a component vary appreciably with the number of class intervals. Table 5.1 and figures 5.14 to 5.20 refer to the high pass filter example (chapter 4, figure 4.16 and 4.17) and for the situation where the yield is 42%. Tables 5.2 and 5.3 show the results obtained for the band pass filter (figure 5.3 and 5.4). Both tables correspond to Monte Carlo analyses with sample sizes of 200. Table 5.2 refers to the situation where tolerances were large and the yield was only 18%. On the other hand Table 5.3 corresponds to smaller tolerances and a yield of 79%.

In tables 5.1 and 5.2 the values of the yield sensitivities and the yield rankings of the various components vary

appreciably with the number of class intervals. This variation is smaller in table 5.3.

5.3.4 SUMMARY

The TOLERATE method is based on the pass and fail conditional p.d.fs of individual component parameters. The conditional p.d.fs are approximated by histograms constructed from the results of the Monte Carlo analysis of the previous iteration. A particular criterion involving the conditional p.d.fs are employed to select new limit values for the component parameters.

The main practical difficluties of the TOLERATE method arise out of the fact that the entire conditional p.d.fs of individual component parameters have to be characterized by histograms. A straightforward application of the TOLERATE criterion (as reported in /2 /) leads to non-unique tolerance solutions in practical cases. We have therefore introduced a modification to the criterion to overcome this problem.

The rationale for the TOLERATE criterion for choosing limit values is that it leads to increases in yield. We have clarified the mathematical arguments in support of this and have stated the assumptions required for it to hold. The criterion involves the choice by the designer of values for the factor λ. We have shown that a choice of $\lambda > 1$ always results in an increase in yield. However, this is not a necessary condition. Certain choices of $\lambda < 1$ will also result in an increase in yield. However, no simple way of choosing a suitable value for λ has been found. The actual choice of value of λ is crucial in the practical application

of this method. In general we find that the larger values of λ result in overdesign, i.e. too great a tightening of tolerances for particular increases in yield.

To deal with the problem of overdesign, the yield sensitivity analysis was introduced in the original method. However, we have shown that in practice yield sensitivity is an ambiguous measure.

Therefore the most sérious shortcoming of this method is overdesign. The results presented so far have demonstrated that smaller values of λ usually provide better tolerance solutions. However, if the value of λ is taken too low, then the method requires too many iterations, does not always lead to increases in yield and can be wasteful of computer effort. In the next section we introduce a method (PERTOL) based on the cumulative distribution functions (9, chapter 12) corresponding to the conditional p.d.fs. The overdesign inherent in TOLERATE will be demonstrated by comparison with results obtained by application of the PERTOL method.

5.4 THE PERTOL METHOD

The basic structure of the PERTOL method is similar to that of TOLERATE as is illustrated in figure 5.1. That is, the procedure commences with large tolerances. Monte Carlo analysis is performed and tolerances (more specifically limit values) of component parameters are adjusted by an algorithm which takes into account the distribution of passing and failing circuits. After revising the limit values, the Monte Carlo analysis is repeated and the process is continued until a cost minimum is achieved or 100% yield is obtained.

The essential difference between the PERTOL and TOLERATE methods is in the actual algorithms employed to revise limit values. Referring to figure 5.1, the difference in the two methods is in the mode of operation of the INTERPRETER.

We briefly discribe the PERTOL procedure for revising limit values and later develop its mathematical justification. This is followed by discussion of practical results obtained with this method.

5.4.1. THE PERTOL CRITERION

(a) The Practical Algorithm

As before we let $t_s^j = \dfrac{Us,_j - Ls,_j}{2}$ and $t_s^{j+1} = \dfrac{Us,_{j+1} - Ls,_{j+1}}{2}$

be the tolerances for the sth component at the jth and (j+1)th iteration respectively. The PERTOL method selects limit values $Ls,_{j+1}$ and $Us,_{j+1}$ such that they are the (100 x r)th and {100 x (1-r)}th percentile of the pass conditional p.d.f. $Pr(p_s/pass)$. The values of r, t_s^j and t_s^{j+1} are required to meet the following condition.

$$r < \tfrac{1}{2}\left(1 - \frac{t_s^{j+1}}{t_s^j}\right) \qquad 5.18$$

The relationship between r, $Ls,_{j+1}$ and $Us,_{j+1}$ is illustrated in figure 5.22.

In one implementation of the method, the following strategy is followed.

The N_j sample circuits from the jth Monte Carlo analysis are divided into a pass list and a fail list. Let N_{jp} and N_{jF} be the respective sizes of the pass and fail lists.

As before, let Ls_j and Us_j represent the limit values of the sth component for the jth iteration, and $Ls,_{j+1}$ and $Us,_{j+1}$, the corresponding limit values for the (j+1)th iteration.

To select limit values $Ls,_{j+1}$ and $Us,_{j+1}$ the values of the sth component of the N_{jp} pass circuits are sorted into an ascending order. Then the first value in this ordered list is an estimate of the $(100 \times 1/N_{jp})$th percentile of the conditional p.d.f. $Pr(p_s/pass)$. The second value in the list is an estimate of the $(100 \times 2/N_{jp})$th percentile and so on. Similarly the last value is an estimate of the $100 \times (1-1/N_{jp})$th percentile and the last but one value is an estimate of the $100 \times (1 - 2/N_{jp})$th percentile.

The algorithm commences by considering the first and last values in the list. We denote these by a_1 and b_1 respectively. The let $r = 1/N_{jp}$ and $c = b_1 - a_1/ 2$. The algorithm tests if the following condition is satisfied.

$$r < \tfrac{1}{2} \left(1 - \frac{c}{t_s^j}\right) \qquad 5.19$$

where $t_s^j = (U_{s},_j - Ls,_j)/2$

If condition (5.19) is satisfied, then a_1 and b_1 are accepted as the limit values $Ls,_{j+1}$ and $Us,_{j+1}$ respectively. Otherwise the second value in the ordered list designated as a_2 and the last but one value designated b_2 are selected. We now let $r = 2/N_{jp}$ and $c = b_2 - a_2/2$. Again condition (5.18) is tested. If (5.18) is satisfied then a_2 and b_2 are selected as the new limit values. On the other hand if 5.18 is still not satisfied, then the procedure is continued to the third and last but third values in the ordered list.

The procedure is continued until a pair of values is found which satisfied (5.18). If no such pair can be found, then the new limit values of the sth component are left unchanged. That is $Ls_{,j+1} = Ls_{,j}$ and $Us_{,j+1} = Us_{,j}$.

To re-assign limit values for another component (the qth component say), the N_{jP} pass circuits now have to be re-ordered according to ascending values of the qth component. The process of finding a pair of values which meet condition 5.19 is carried out as for the sth component, as described above. The procedure is carried out for all K components.

(b) Implications On Yield

We now discuss the implications on yields Y_j and Y_{j+1} of choosing limit values according to the PERTOL method. Specifically we will show that a choice of $Ls_{,j+1}$, $Us_{,j+1}$ which satisfies (5.18) ensures that $Y_{j+1} > Y_j$.

As before let $R_{T,j}$ and $R_{T,j+1}$ represent the tolerance regions for iterations j and j+1 respectively, and let $V(R_x)$ represent the volume of a region x. Then the yields Y_j and Y_{j+1} may be re-written as:

$$Y_j = \frac{V(R_{T,j} \cap R_A)}{V(R_{T,j})} \qquad 5.20$$

and

$$Y_{j+1} = \frac{V(R_{T,j+1} \cap R_A)}{V(R_{T,j+1})} \qquad 5.21$$

As previously in the development of the TOLERATE criterion we initially consider only one parameter at a time. Definitions (5.20) and 5.21) for this case are illustrated in figure 5.23. We aim to choose new limit values for the sth component such that yield is increased. That is, we require

$$Y_{j+1} > Y_j \tag{5.22}$$

or

$$\frac{V(R_{T,j+1} \cap R_A)}{V(R_{T,j+1})} > \frac{V(T_{T,j} \cap R_A)}{V(R_{T,j})} \tag{5.23}$$

Since we are only considering the sth component, we get:

$$\frac{V(R_{T,j+1})}{V(R_{T,j})} = \frac{t_s^{j+1}}{t_s^j} \tag{5.24}$$

If $Ls,_{j+1}$ and $Us,_{j+1}$ are chosen as described previously and illustrated in figure 5.22, then the following holds:

$$\frac{V(R_{T,j+1} \cap R_A)}{V(R_{T,j} \cap R_A)} = 1-2r \tag{5.25}$$

To appreciate (5.25) we note that the ratio of the numbers of passing circuits in regions $R_{T,j+1}$ and $R_{T,j}$ is an estimate of the ratio of the volumes of regions $R_{T,j+1} \cap R_A$ and $R_{T,j+1} \cap R_A$. We have chosen t_s^{j+1} such that the ratio of passes in the two regions $R_{T,j+1}$ and $R_{T,j}$ is 1-2r, and therefore 5.25 holds$^{\alpha}$.

$^{\alpha}$The right hand side of (5.25) is only an <u>estimate</u> of the ratio of volumes. However, to avoid complicating the argument, (5.25) shows an equality.

Also shown in figure 5.22 is the corresponding situation for the fail conditional p.d.f. of the sth component and the associated cumulative distribution function. Let us say that the (100 x r)th and {100 x (1-r)}th percentile of the pass cumulative distribution function correspond to the (100 x r')th and {100 x (1-r")}th percentile of the fail cumulative distribution function of the sth component. Then as before it is required to choose limit values (hence nominal and tolerance) for the sth component such that 5.23 is satisfied, i.e.

$$Y_{j+1} > Y_j \qquad 5.26$$

The yields Y_j and Y_{j+1} may also be written as:

$$Y_j = 1 - \frac{V(R_{T,j} \cap \bar{R}_A)}{V(R_{T,j})} \qquad 5.27$$

and

$$Y_{j+1} = 1 - \frac{V(R_{T,j+1} \cap \bar{R}_A)}{V(R_{T,j+1})} \qquad 5.28$$

Therefore to satisfy (5.22) we require

$$\frac{V(R_{T,j+1} \cap \bar{R}_A)}{V(R_{T,j+1})} < \frac{V(R_{T,j} \cap \bar{R}_A))}{V(R_{T,j})} \qquad 5.29$$

Re-arranging (5.29), we get

$$\frac{V(R_{T,j+1} \cap \bar{R}_A)}{V(R_{T,j} \cap \bar{R}_A)} < \frac{V(R_{T,j+1})}{V(R_{T,j})} \qquad 5.30$$

Then as before

$$\frac{V(R_{T,j+1})}{V(R_{T,j})} = \frac{t_s^{j+1}}{t_s^j} \qquad 5.31$$

However, now by analogy with (5.25), we may say:

$$\frac{V(R_{T,j+1} \cap \bar{R}_A)}{V(R_{T,j} \cap \bar{R}_A)} = 1 - (r'+r'') \qquad 5.32$$

Therefore substituting (5.32) into (5.31) we get:

$$(r'+r'') < (1 - \frac{t_s^j}{t_s^j}) \qquad 5.33$$

Expression (5.33) corresponds to the fail conditional p.d.f. of the sth component and should be compared to expression (5.25) which refers to the pass conditional p.d.f. The two conditions (5.25) and (5.33) are in fact equivalent and if one is satisfied then so is the other one.

5.4.2 RESULTS

Yield tolerance trajectories obtained by application of the PERTOL method to the band pass filter (figure 5.3 and 5.4) are shown in figure 5.5 to 5.12. The trajectories labelled C refer to the PERTOL method, while those labelled A and B refer to the TOLERATE method. It is evident that PERTOL gives larger tolerance solutions for roughly the same values of yield than TOLERATE.

The comparison between PERTOL and TOLERATE is also shown in terms of unit costs, in figures 5.24 to 5.27. The unit cost function is the following expression:

$$C_U = \frac{C_A + C_T}{Y}$$

C_A is the fixed cost and C_T is the sum of the tolerance dependent costs. We assume $C_T = \sum_{i=1}^{K} C_i(t_i)$

and $C_i(t_i) = \frac{\beta_i}{t_i}$, where β_i is a constant reflecting the cost of component i with respect to the other components in the circuit. The different graphs (figure 5.24 to 5.27) refer to different relative values of fixed (C_A) and tolerance dependent (C_T) costs. For example figure (5.24) refers to the situation where the fixed and tolerance dependent costs are equal. On the other hand (5.25) refers to the case where C_A is twice C_T. The unit cost function is normalized to have a value of unity for the tolerances and yield at iteration one.

A set of yield tolerance trajectories for the high pass filter example (Chapter 4, figure 4.16 and 4.17) are shown in figure 5.28 to 5.34. The curves labelled A refer to the TOLERATE method and B refer to PERTOL. In figure 5.35 and 5.36 the variation of the unit cost with iteration is shown for this example. For all six variations of cost function for the two circuit examples reported here, the PERTOL method provides considerably smaller cost solutions than TOLERATE.

5.5 SUMMARY AND CONCLUSIONS

In this chapter, methods of tolerance assignment based on Monte Carlo analysis have been reviewed. An existing method, TOLERATE, has been briefly described. TOLERATE belongs to a class of iterative methods which differ in the criterion employed to re-select component tolerances. We have clarified the mathematical arguments in support of the TOLERATE criterion. In addition the results of the practical application of the TOLERATE method to particular circuit examples have been presented. It has been shown that a direct

application of the TOLERATE criterion as reported in / 2 / can lead to non-unique tolerance solutions. To deal with this problem a modification of this criterion has been introduced.

To overcome the disadvantages of overdesign, a sensitivity measure called yield sensitivity was introduced in the original TOLERATE method. The purpose of yield sensitivity is to pinpoint components which have substantial effect on yield. We have presented practical results showing that yield sensitivity calculating with practical circuit examples can be an ambiguous measure of the relative effect on yield of a particular component.

Overdesign remains the most serious shortcoming of the TOLERATE method. To overcome the disadvantages associated with overdesign we have introduced the PERTOL method. PERTOL is based on the cumulative distribution functions associated with the conditional p.d.f.s of individual component parameters. Generally, cumulative distribution functions are found to be of value in the periphery of the region of variation of statistical parameters. In the class of methods considered in this chapter most interest is directed at the behaviour of the tolerance region near its periphery.

The PERTOL criterion requires estimates of percentiles of the conditional distributions. Therefore the entire conditional p.d.fs of individual component parameters need

not be characterized by histograms. Thus most of the practical ambiguities of the TOLERATE method are avoided.

We have provided a brief description of the PERTOL method of choosing limit values. We have also discussed the implications on yield of choosing limit values in this manner.

Finally we have presented comparitive results of applying both PERTOL and TOLERATE to the same circuit examples. Comparisons of the merits of the two methods can be made either in terms of the yield versus tolerance trajectories, or in terms of the trajectories of the unit cost with iteration. From a comparison of yield trajectories it will be seen that for particular values of yield, PERTOL generally provides larger tolerances than TOLERATE. Similarly from a comparison of the cost trajectories it will be seen that PERTOL consistently provides lower cost solutions.

No. of Class intervals		COMPONENT NUMBERS: 2	3	4	6	7	8	10
5	Yield Sensitivity	0.248	0.119	0.461	0.5	0.07	0.316	0.465
	Yield Ranking	5	6	3	1	7	4	2
10	Yield Sensitivity	0.3	0.227	0.467	0.5	0.177	0.316	0.513
	Yield Ranking	5	6	3	2	7	4	1
20	Yield Sensitivity	0.34	0.34	0.55	0.626	0.354	0.434	0.527
	Yield Ranking	6	7	2	1	5	4	3

Table 5.1 : Table Showing The Variation With Number Of Class Intervals, Of The Estimated Yield Sensitivity And Sensitivity Ranking Of Individual Components For An Intermediate Yield Case (42%) (High Pass Filter Circuit Example)

No. of Class Intervals		2	4	5	7	8	10	11	13
8	Yield Sensitivity	0.2751	0.4636	1.084	0.418	0.2859	0.9187	0.4282	0.3496
	Yield Rankings	1	6	8	4	2	7	5	3
10	Yield Sensitivity	0.4634	0.5285	1.084	0.5705	0.3821	0.9187	0.523	0.4743
	Yield Rankings	2	5	8	6	1	7	4	3
12	Yield Sensitivity	0.4336	0.668	1.175	0.4228	0.4607	0.9228	0.5041	0.3916
	Yield Rankings	3	6	8	2	4	7	5	1

COMPONENT NUMBERS

Table 5.2 : Table Showing The Variation With Number Of Class Intervals, Of The Estimated Yield Sensitivity And Sensitivity Ranking Of Individual Components For A Low Yield Case (18%) (Band Pass Filter Circuit Example)

No. of Class Intervals		2	4	5	7	8	10	11	13
8	Yield Sensitivity	0.6553	0.5136	0.2056	0.2071	0.5041	0.7857	0.4114	0.366
	Yield Rankings	7	6	1	2	5	8	4	3
12	Yield Sensitivity	0.7731	0.622	0.3611	0.3054	0.5516	0.8692	0.5338	0.4004
	Yield Rankings	7	6	2	1	5	8	4	3
16	Yield Sensitivity	0.883	0.7765	0.339	0.467	0.5578	0.8692	0.637	0.5372
	Yield Rankings	7	6	1	2	5	8	4	3

(Columns 2–13: COMPONENT NUMBERS)

Table 5.3 : Table Showing The Variation With Class Intervals, Of The Estimated Yield Sensitivity And Sensitivity Ranking Of Individual Components For A High Yield Case(79%) (Band Pass Filter Circuit Example)

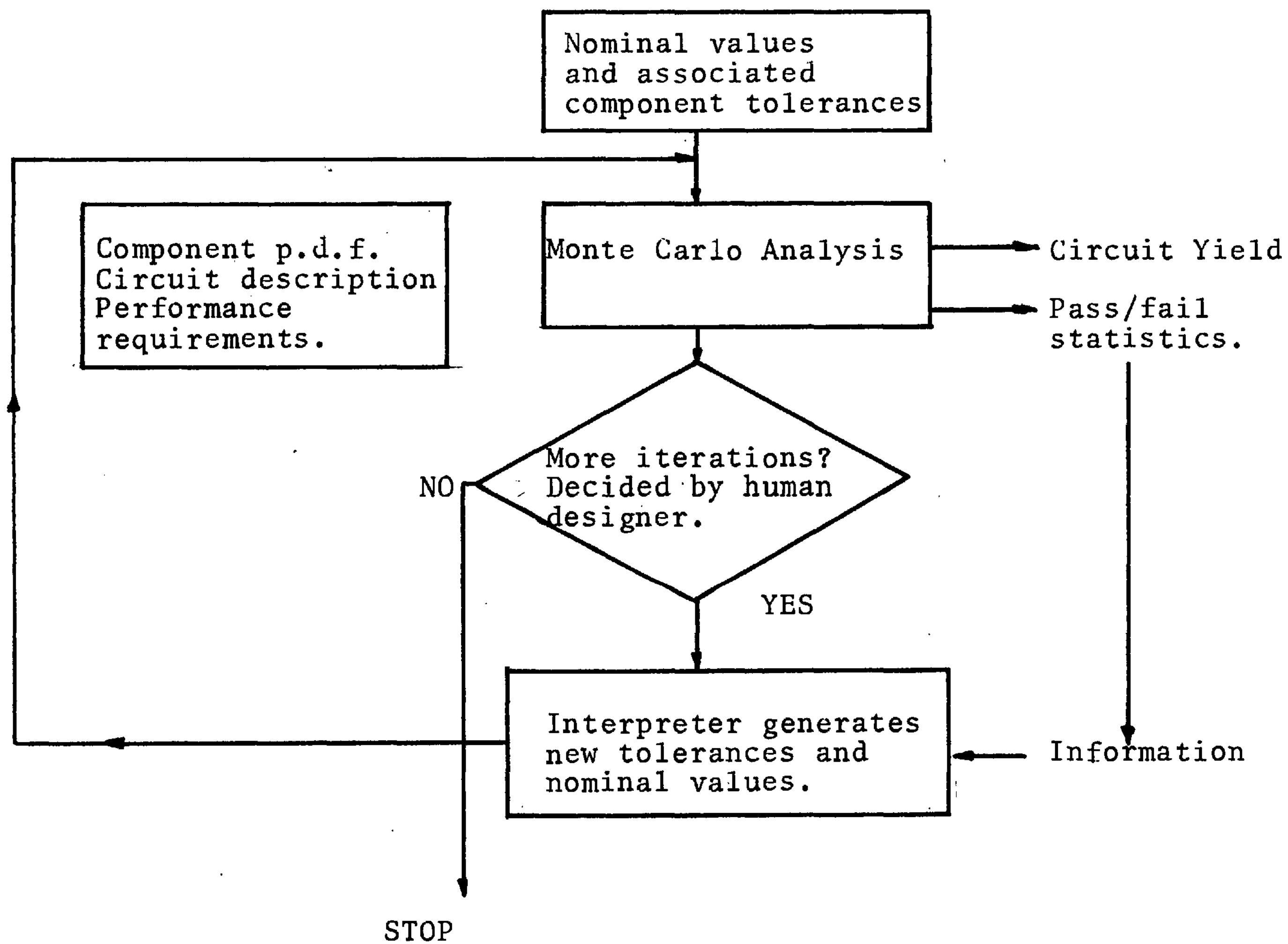


Figure 5.1 : A General Flow Chart For The TOLERATE And PERTOL Methods Of Tolerance Assignment.

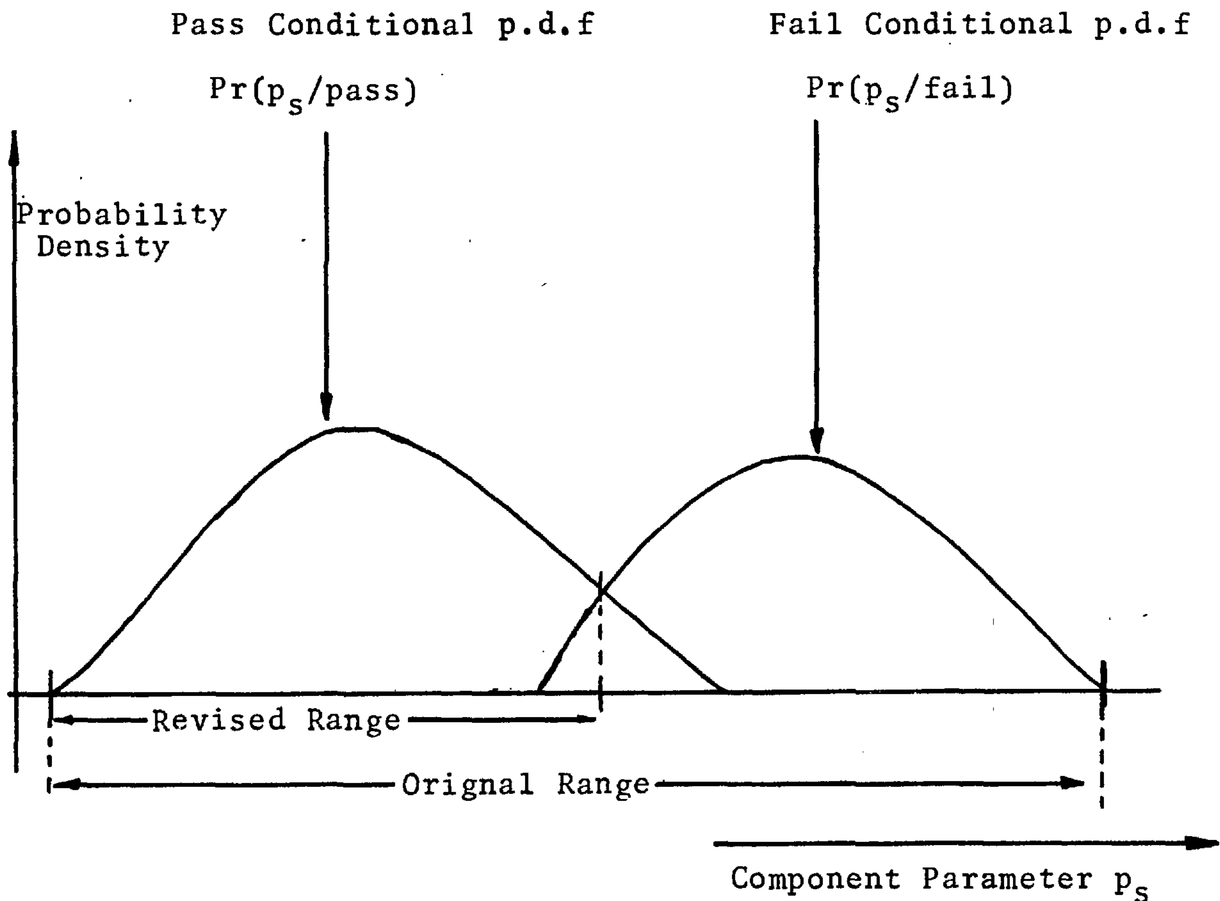


Figure 5.2 : The TOLERATE Tolerance Assignment Criterion; Showing The Original And Revised Ranges; Assuming $\lambda=1$.

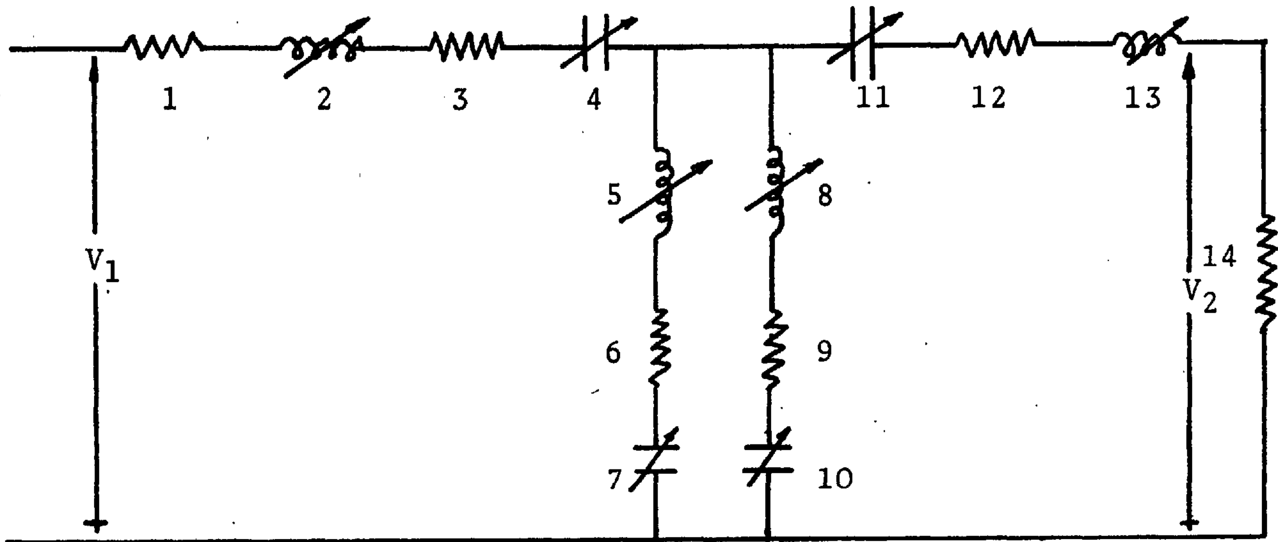


Figure 5.3 : Circuit Diagram Of The Band Pass Filter Example.

Note : Arrows Indicate Toleranced Components.
Insertion Loss Is $20\text{Log}|V_2/V_1|$ dB

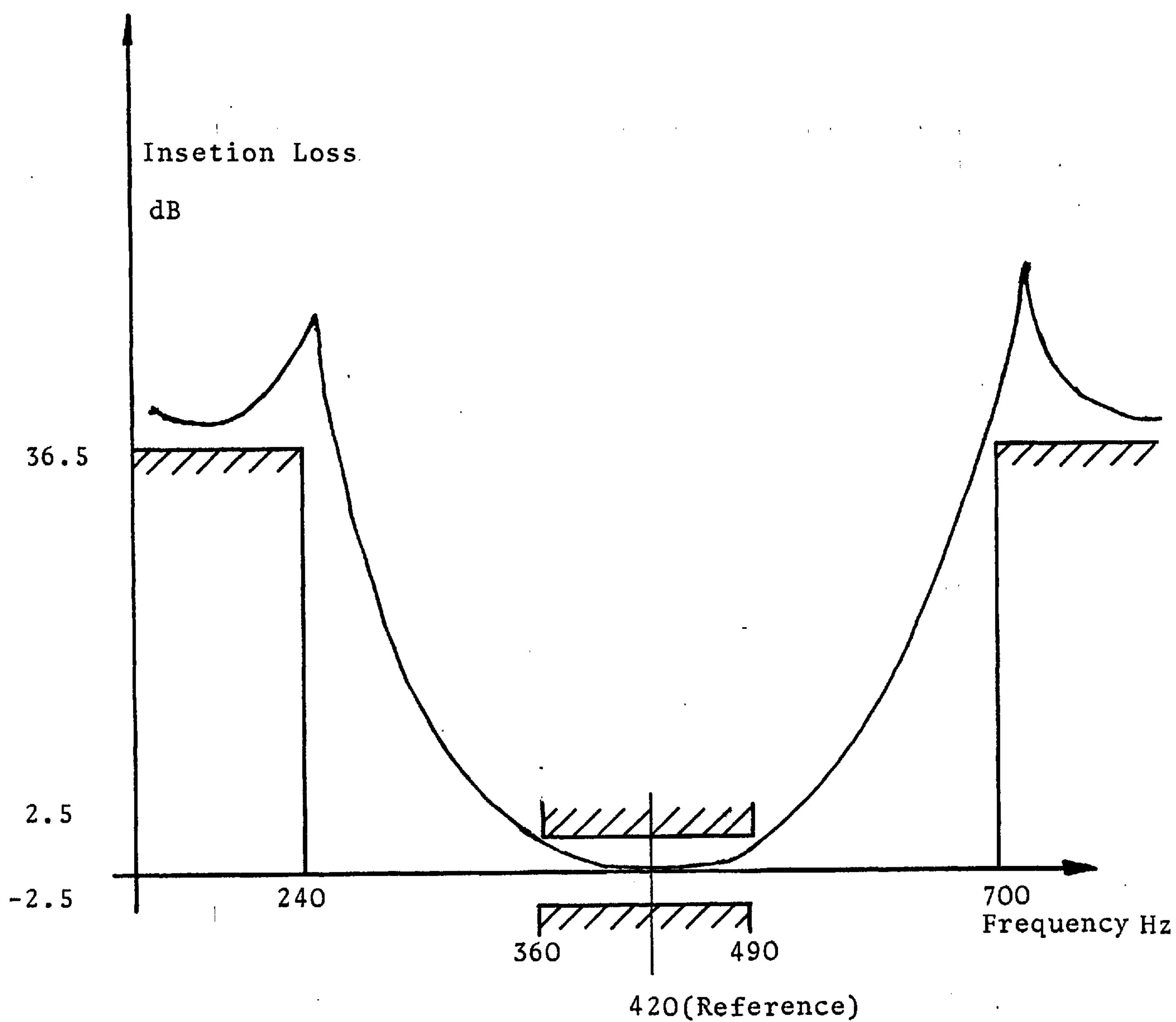


Figure 5.4 : Performance Constraints And Typical Shape Of Response For The Band Pass Filter Example

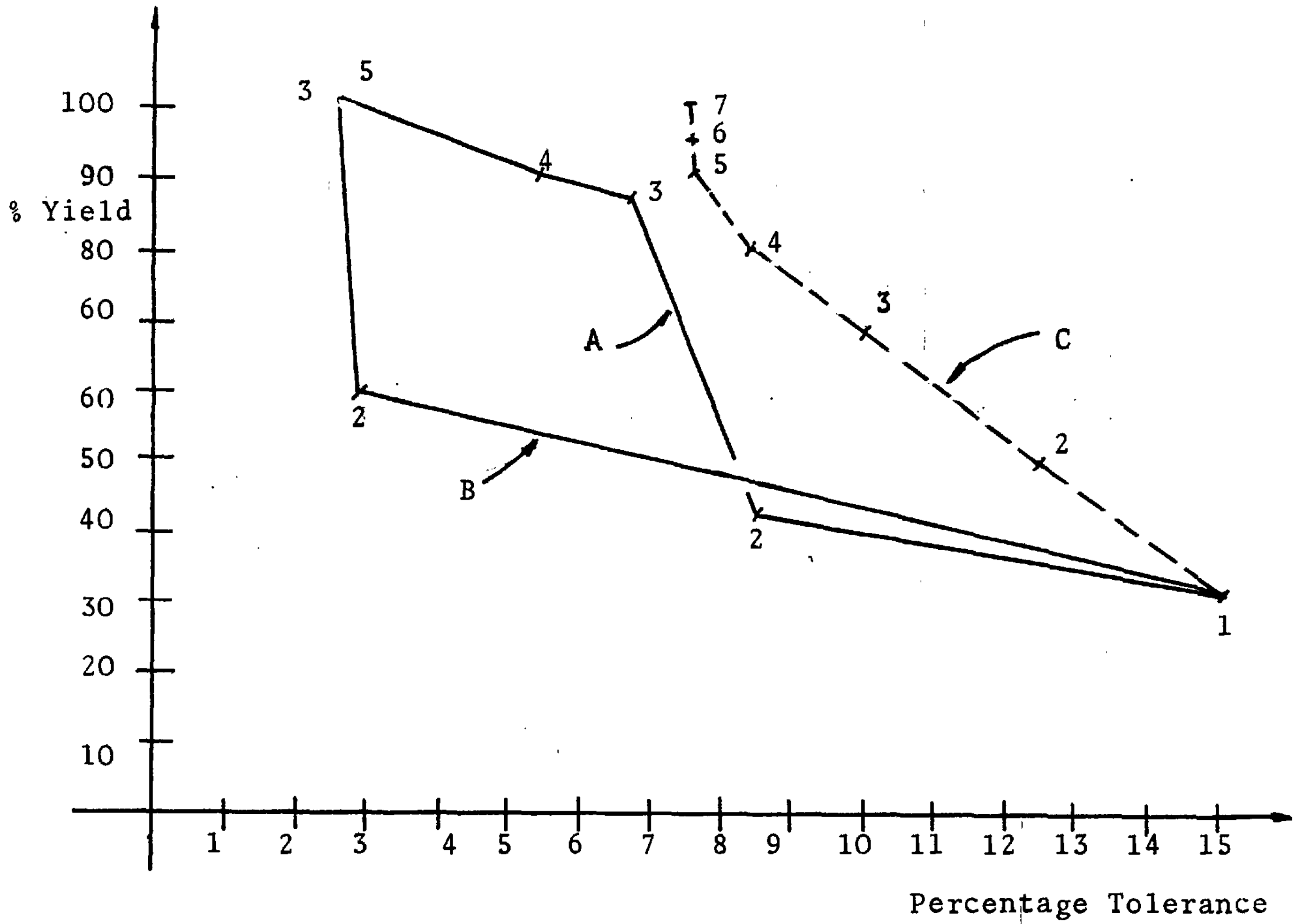


Figure 5.5 : Yield-Tolerance Trajectories For The Band Pass Filter Circuit Example (component Number 2)

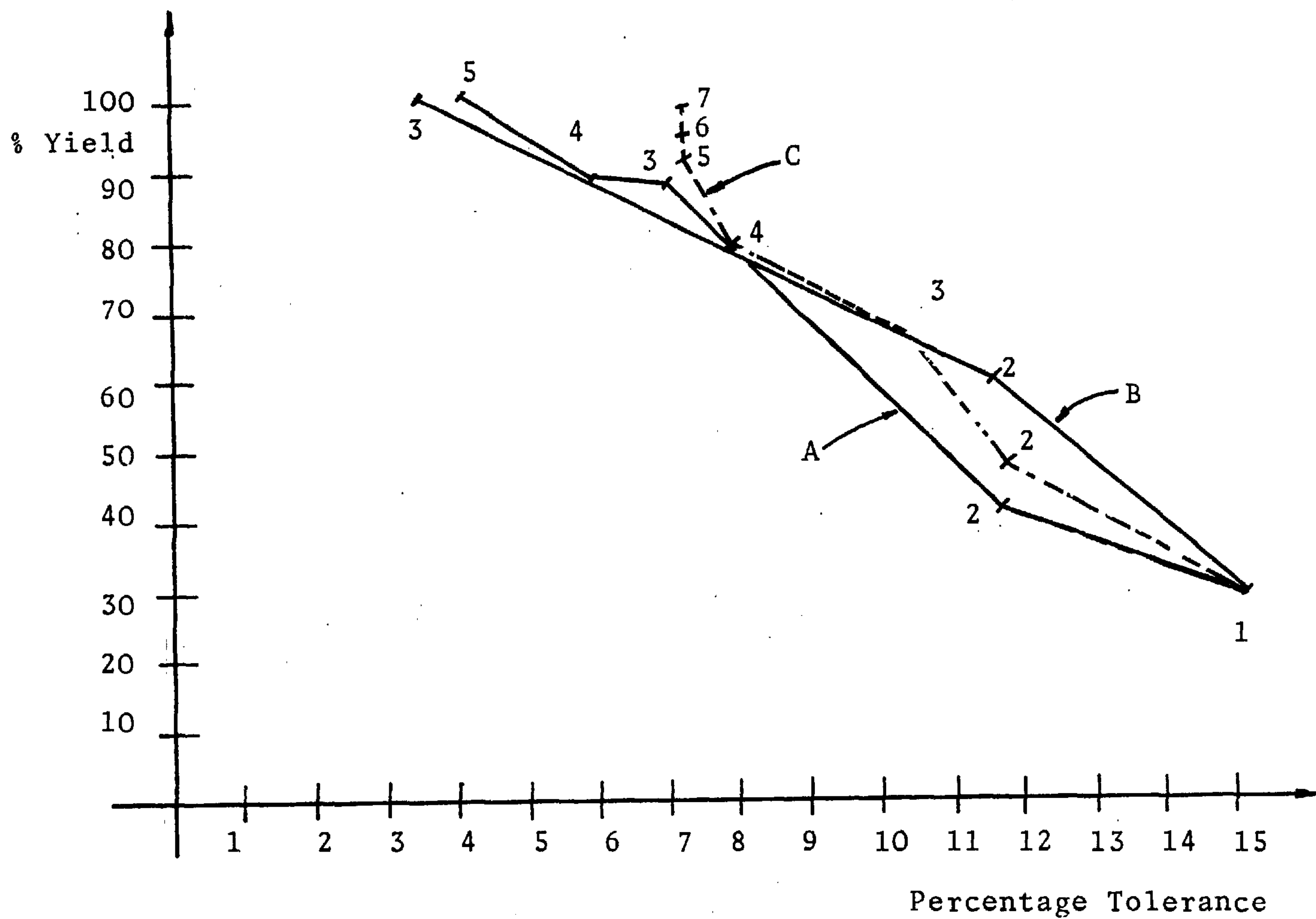


Figure 5.6 : Yield-Tolerance Trajectories For The Band Pass Filter Circuit Example (component Number 4)

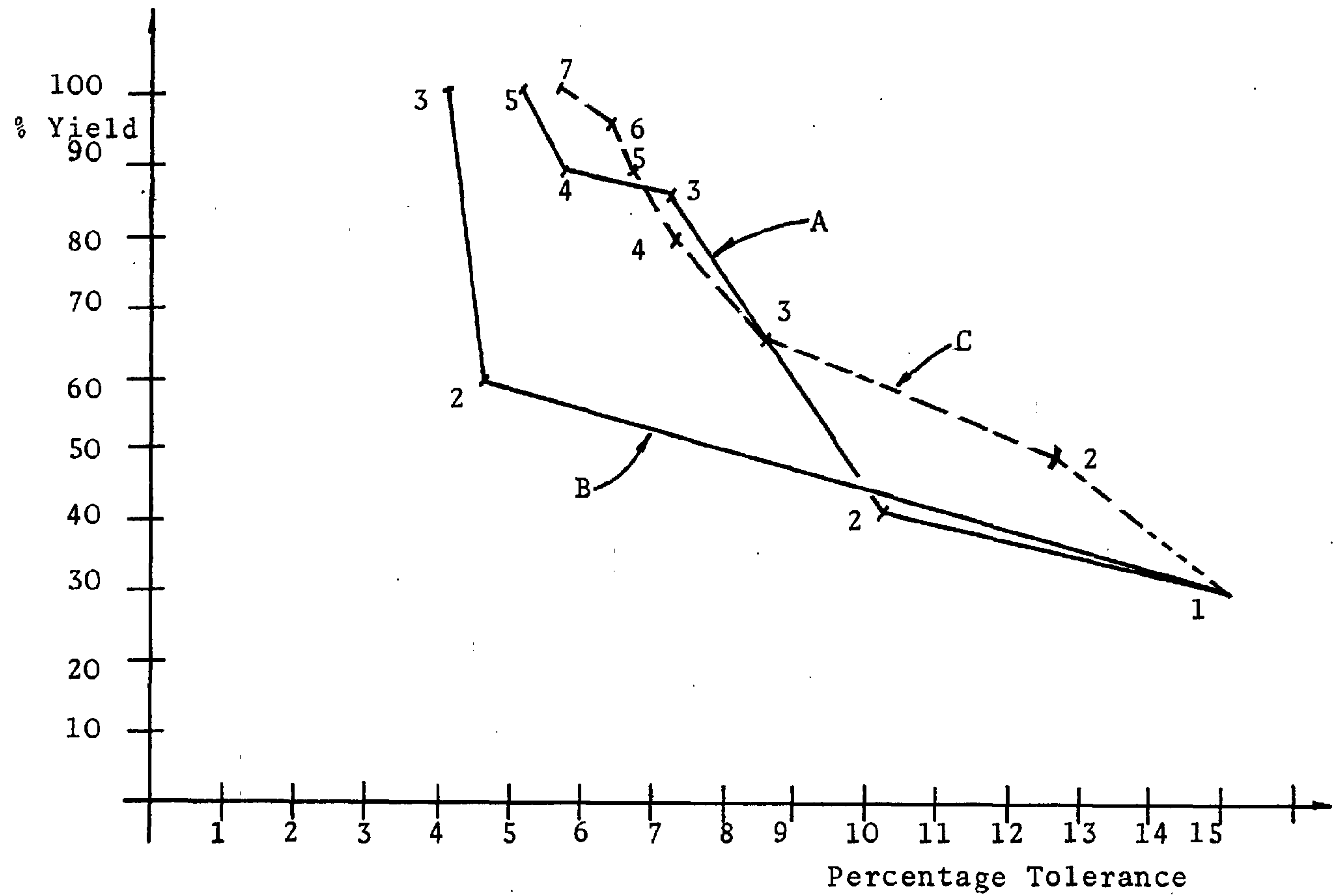


Figure 5.7 : Yield-Tolerance Trajectories For The Band Pass Filter Circuit Example (component Number 5)

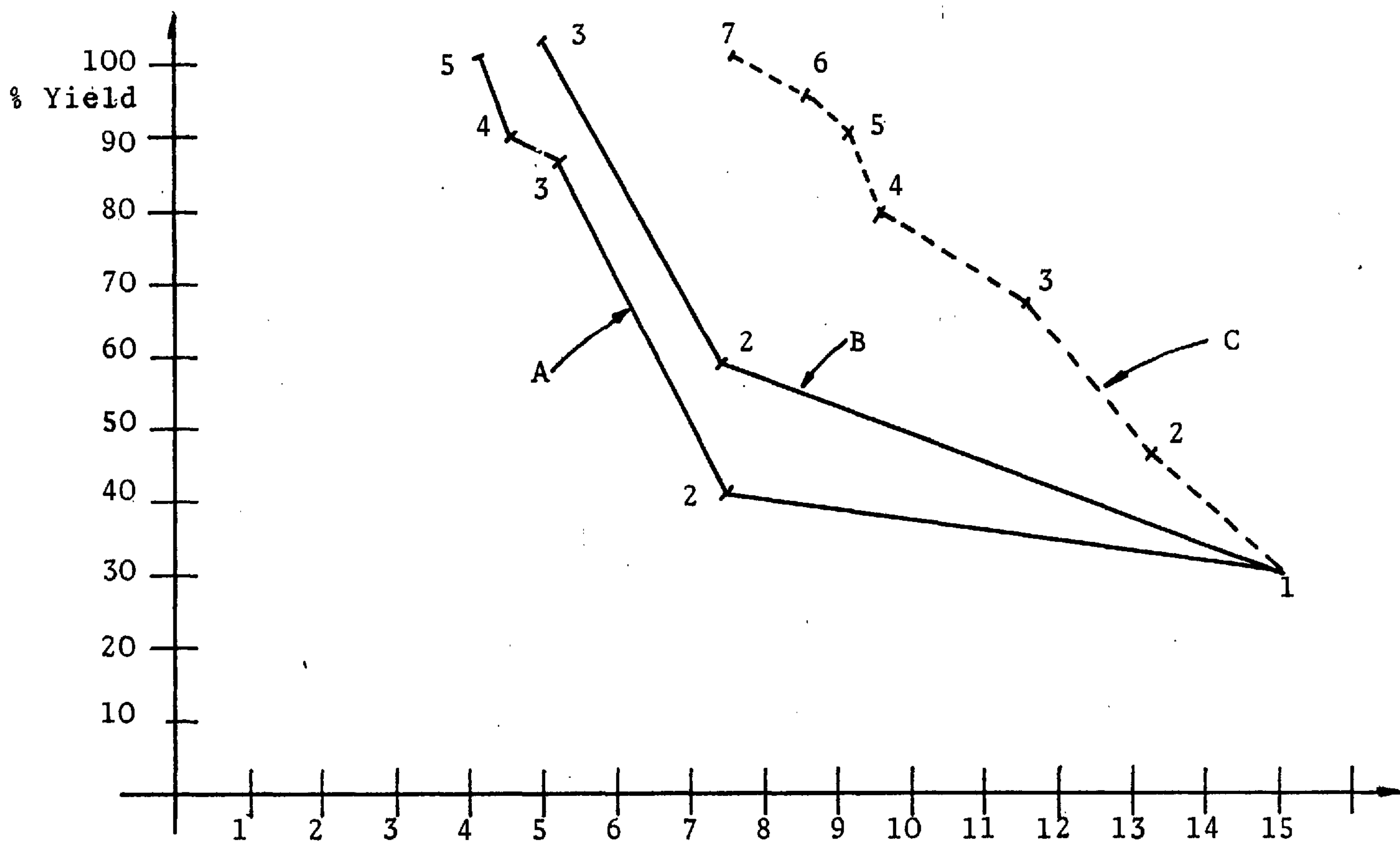


Figure 5.8 : Yield-Tolerance Trajectories For The Band Pass Filter Circuit Example (Component Number 7)

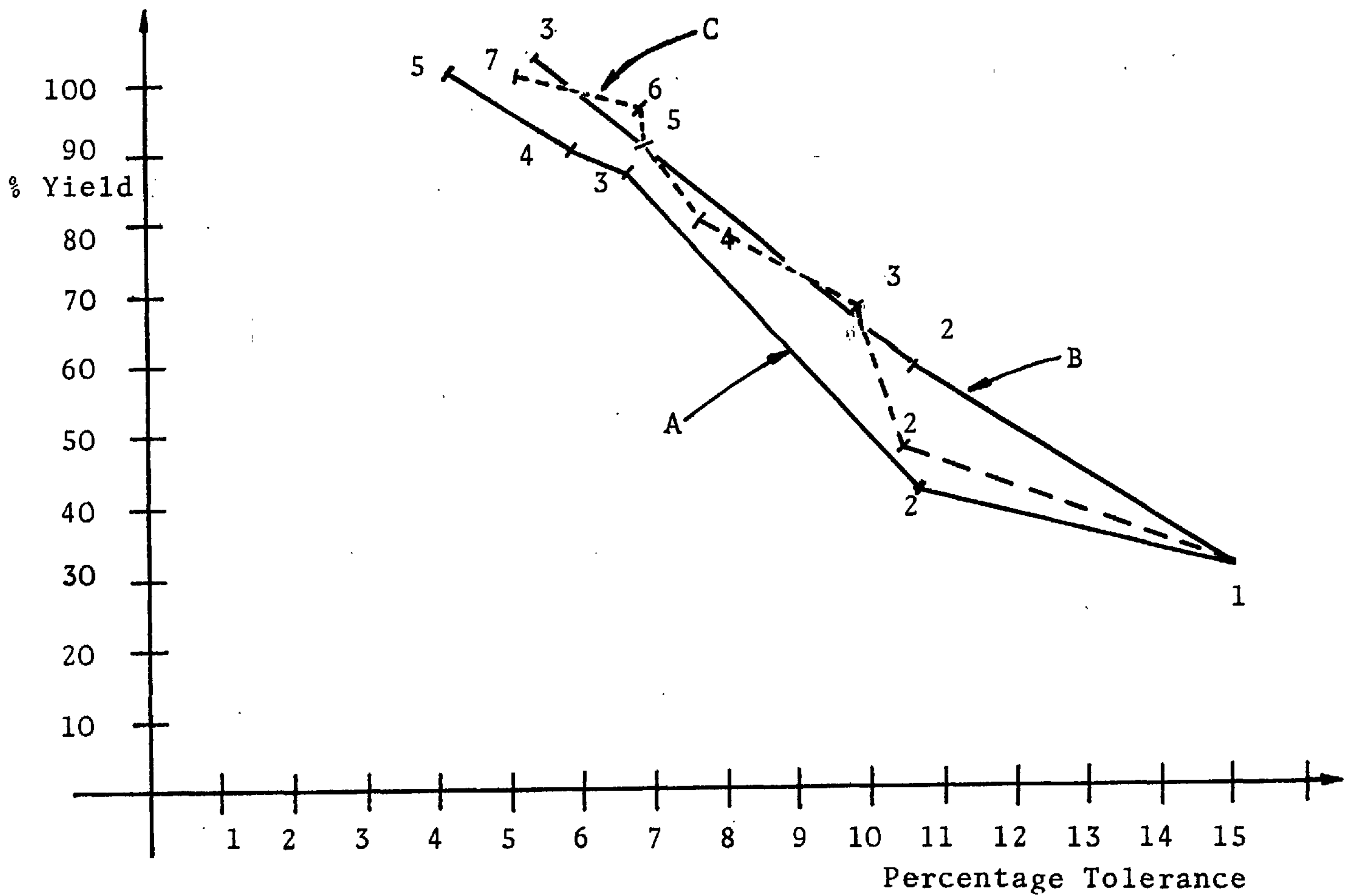


Figure 5.9 : Yield-Tolerance Trajectories For The Band Pass Filter Circuit Example (Component Number 8)

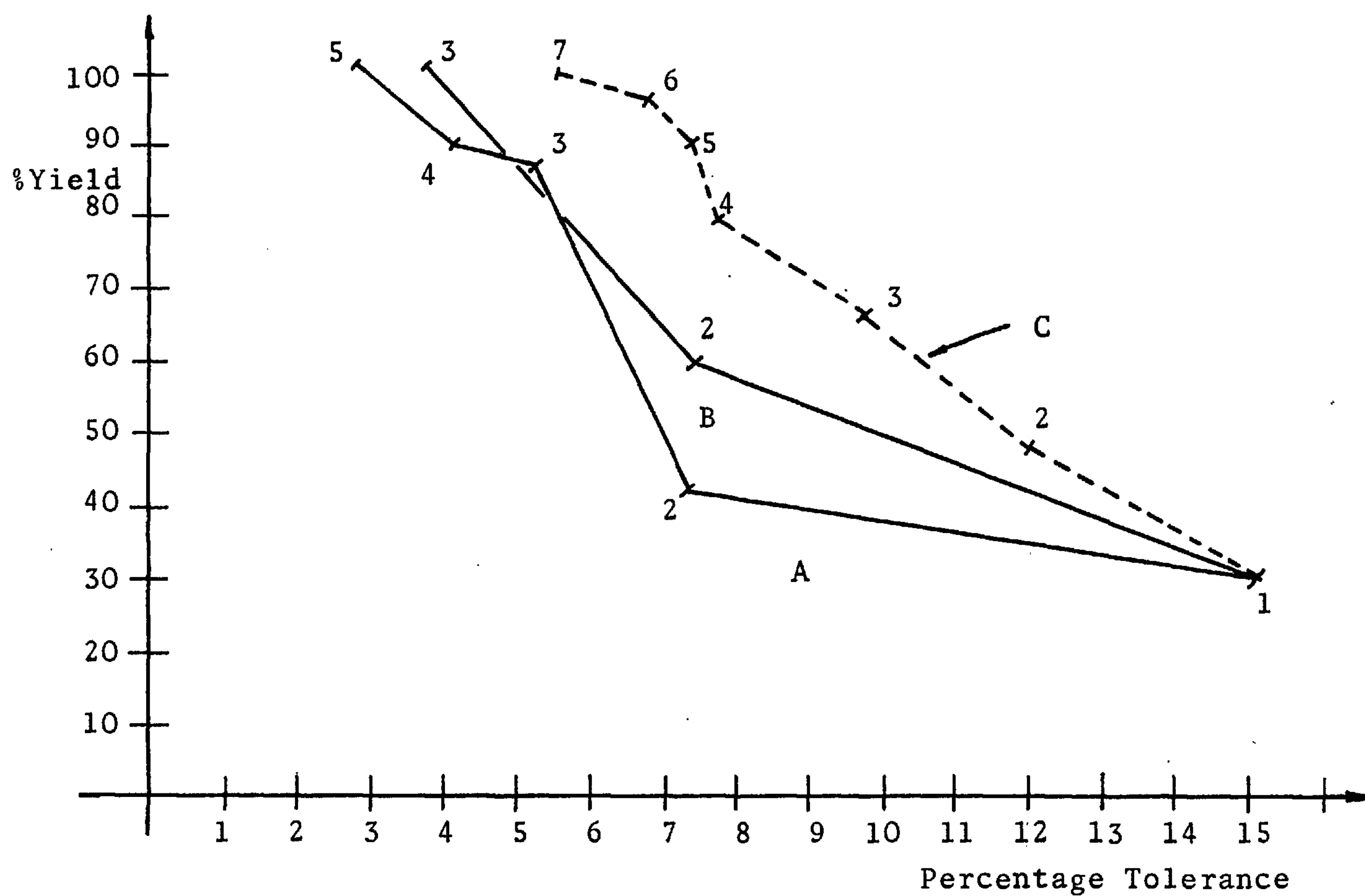


Figure 5.10 : Yield-Tolerance Trajectories For The Band Pass Filter Circuit Example. (Component Number 10)

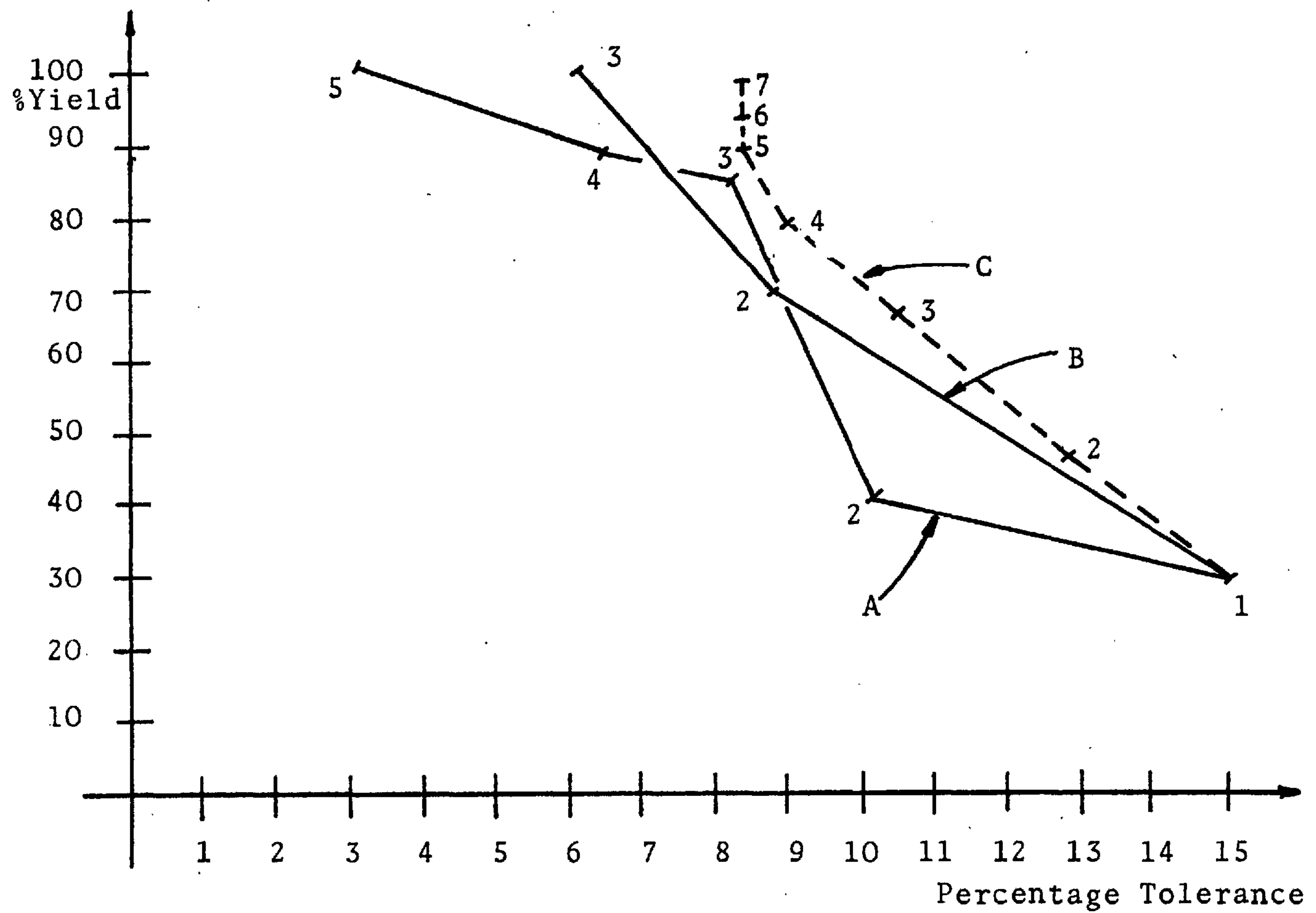


Figure 5.11 : Yield-Tolerance Trajectories For The Band Pass Filter Circuit Example. (Component Number 11)

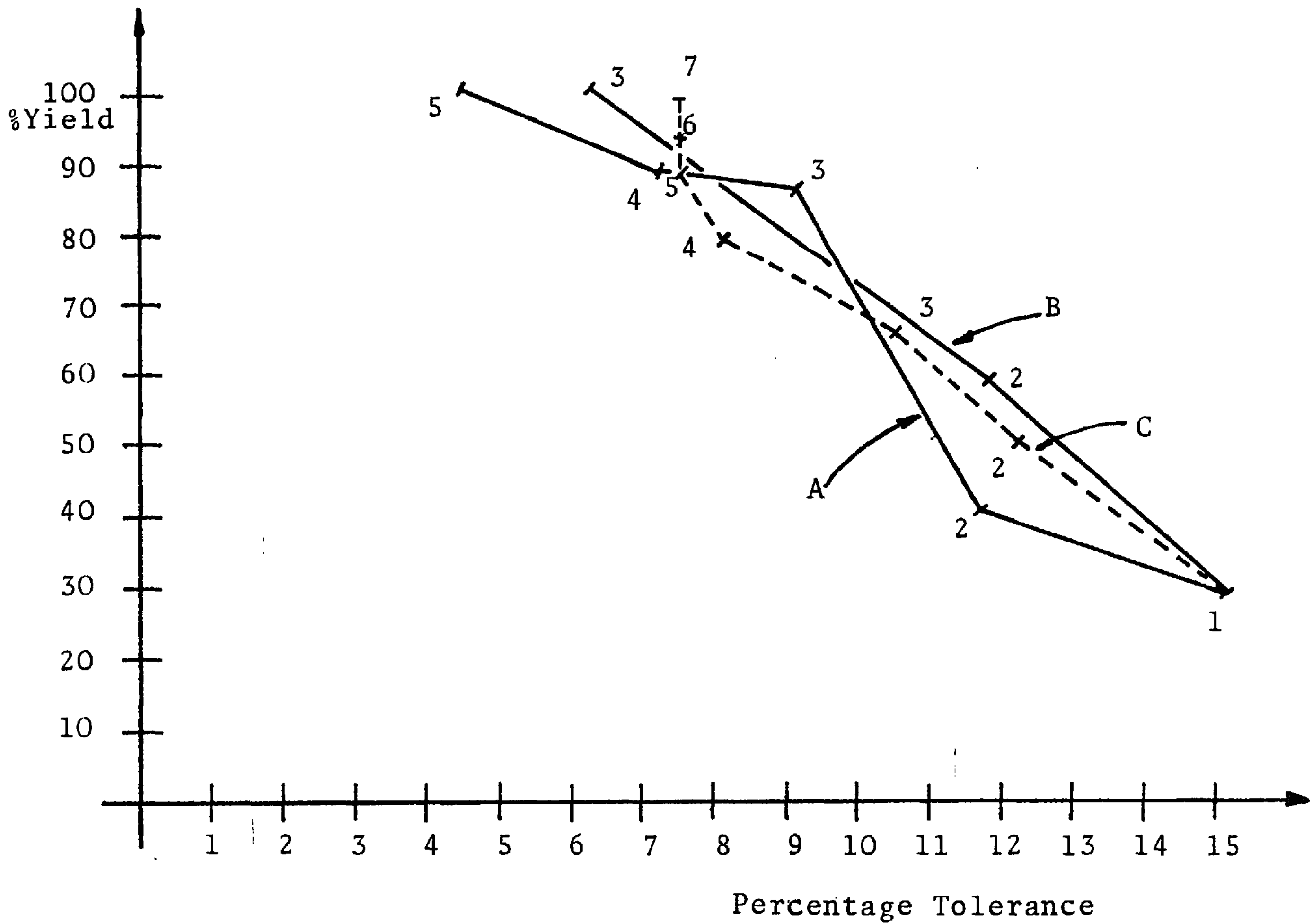
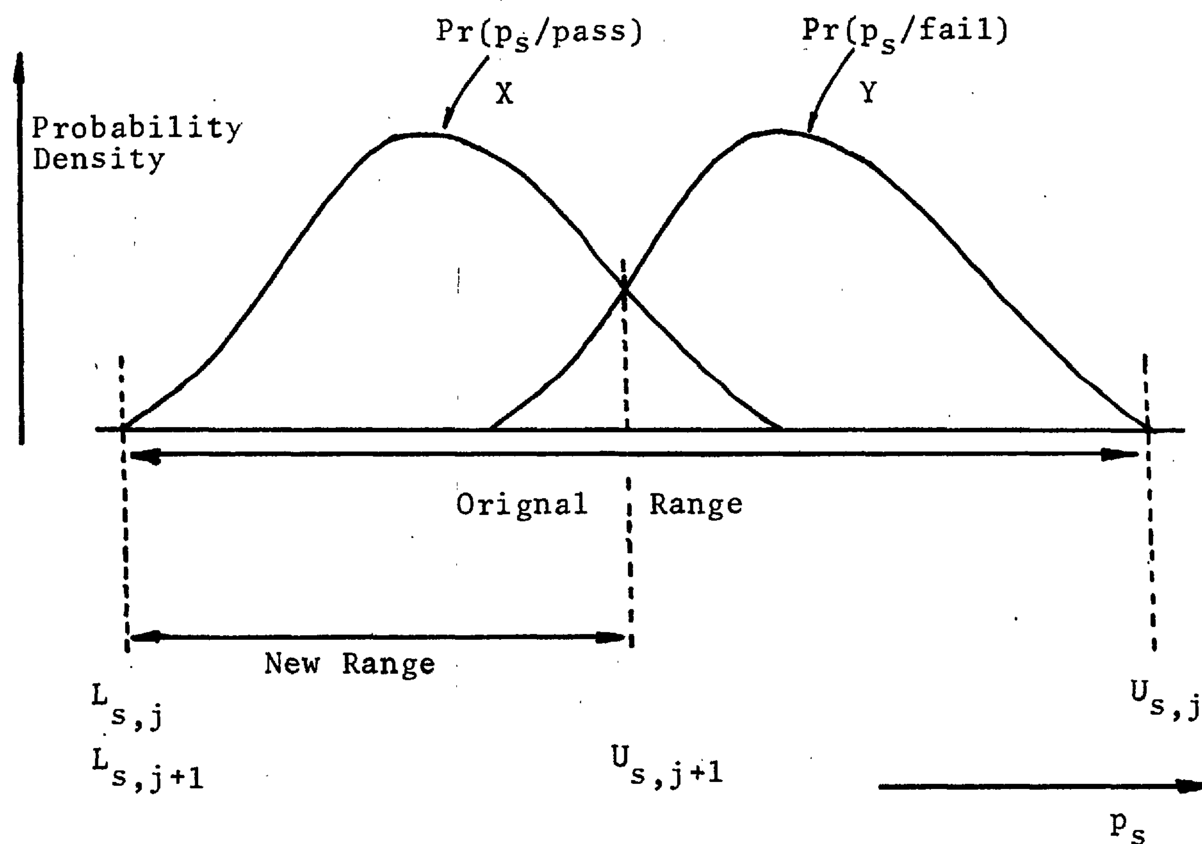
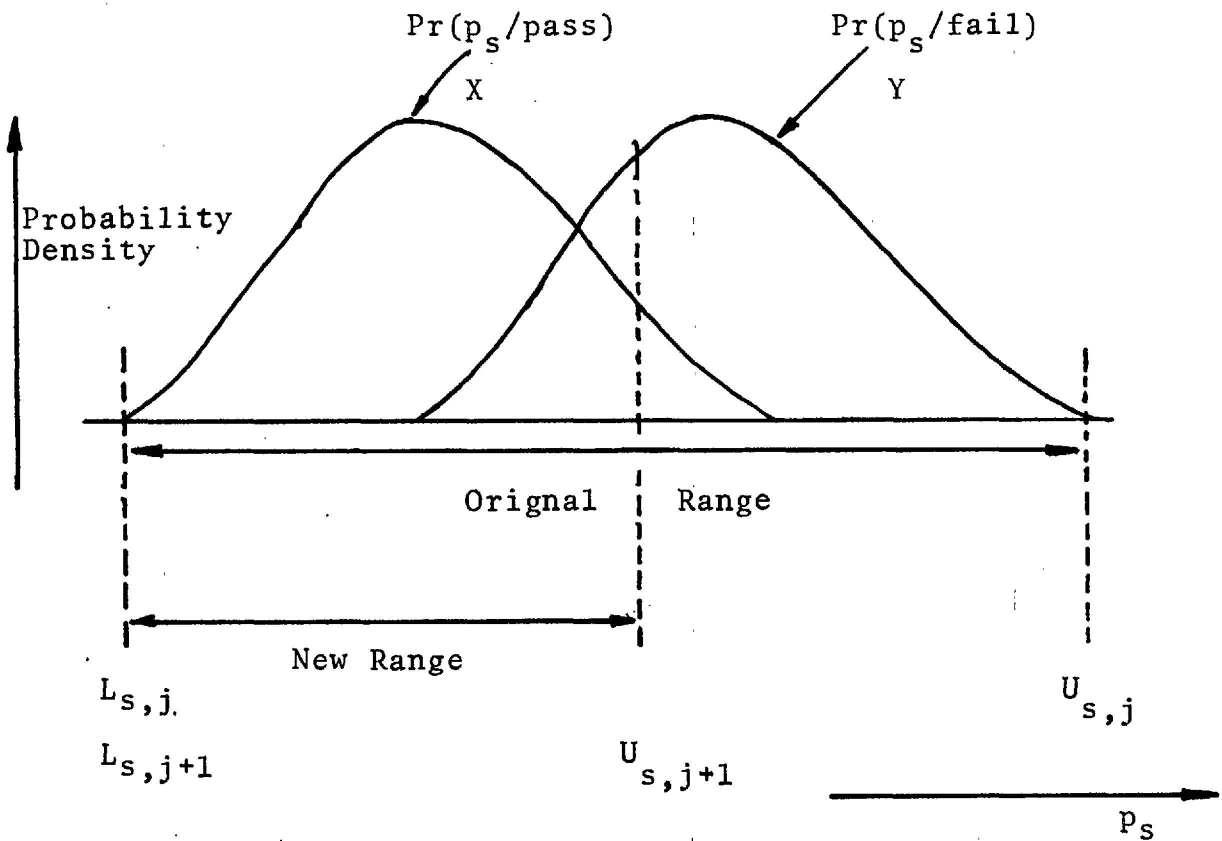


Figure 5.12 : Yield-Tolerance Trajectories For The Band Pass Filter Circuit Example. (Component Number 13)



Note : Expression 5.13 May Be Interpreted As : The Area Under Curve X Between The limits $L_{s,j+1}$ And $U_{s,j+1}$ Is Always Greater Than The Area Under Curve Y Between The Same Limits, If we choose $\lambda_s \geq 1$ In Expression 5.6. In The Diagram We show The Orignal And Revised Ranges, For A Choice Of λ_s=1.

Figure 5.13(a) : An Illustration Of Expression 5.13

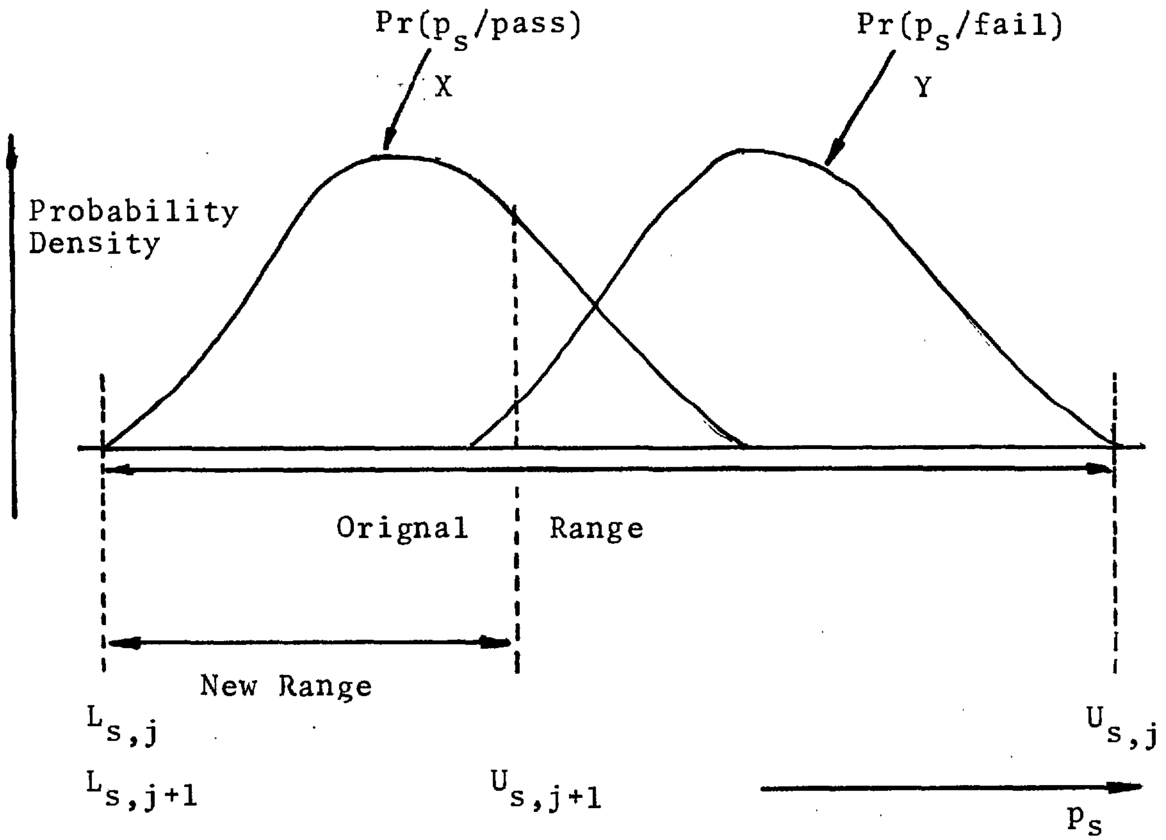


Note : Here We Show That Expression 5.13 Can Hold For A Choice Of $\lambda_s<1$, The Diagram Shows The Orignal $(L_{s,j}\ ;\ U_{s,j})$ And Revised $(L_{s,j+1}\ :\ U_{s,j+1})$ Limit Values

Assuming $\lambda_s< 1$ .The Area Under Curves X And Y Is The Same. Clearly It Is Possible For The Area Under Curve X Between The Limits $L_{s,j+1}$ And $U_{s,j+1}$ To Be Greater

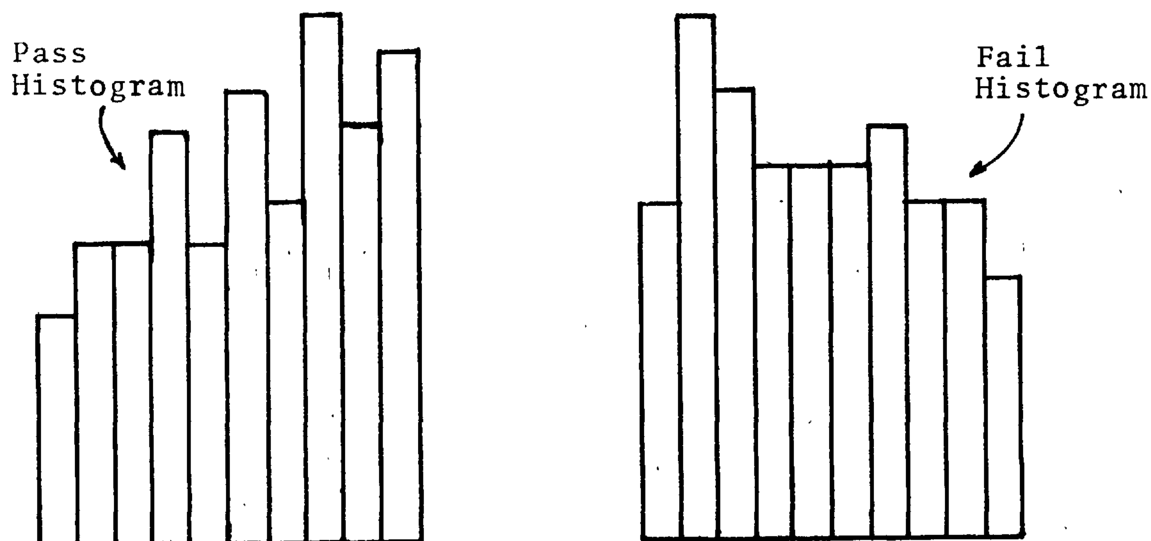
Than The Area Under Curve Y Between The Same Limits.

Figure 5.13(b)



Note : In This Diagram We Show Limit Values For A Choice Of $\lambda_s>1$.

Figure 5.13(c)

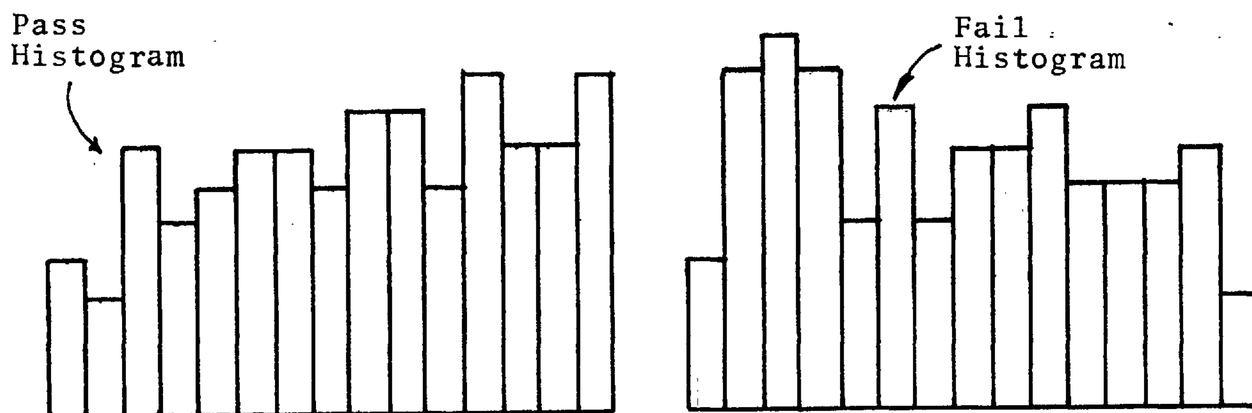


RI For $\lambda=1$: 0 0 0 1 0 1 0 1 1 1

$\lambda=0.8$: 0 0 0 1 1 1 1 1 1 1

$\lambda=0.5$: 0 1 1 1 1 1 1 1 1 0

Histograms employing 10 class intervals



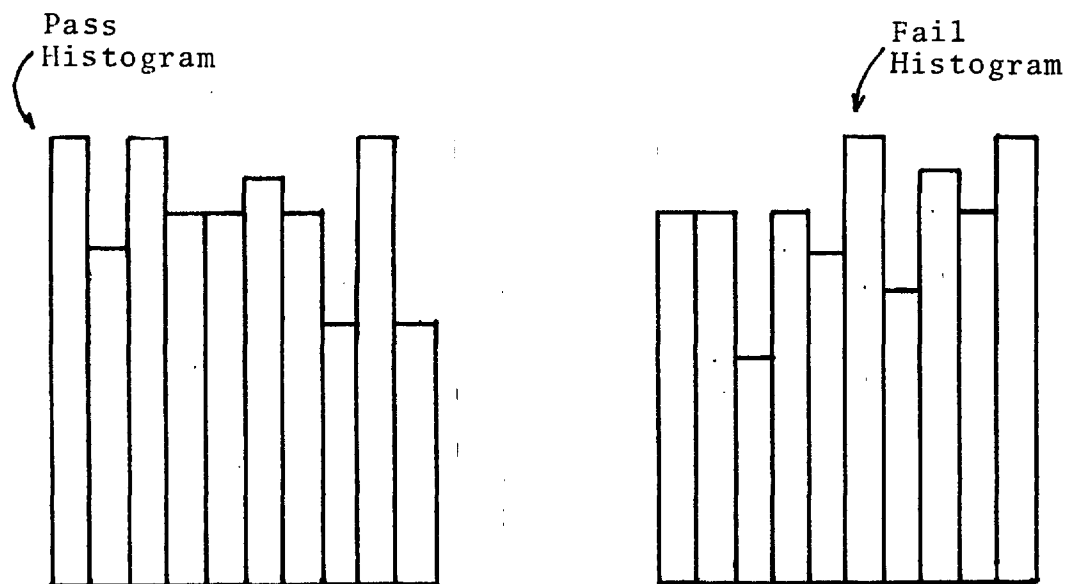
RI For $\lambda=1$: 1 0 0 0 1 0 1 0 1 1 0 1 1 1 1

$\lambda=0.8$: 1 0 0 0 1 1 1 0 1 1 1 1 1 1 1

$\lambda=0.5$: 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1

Histograms employing 15 class intervals

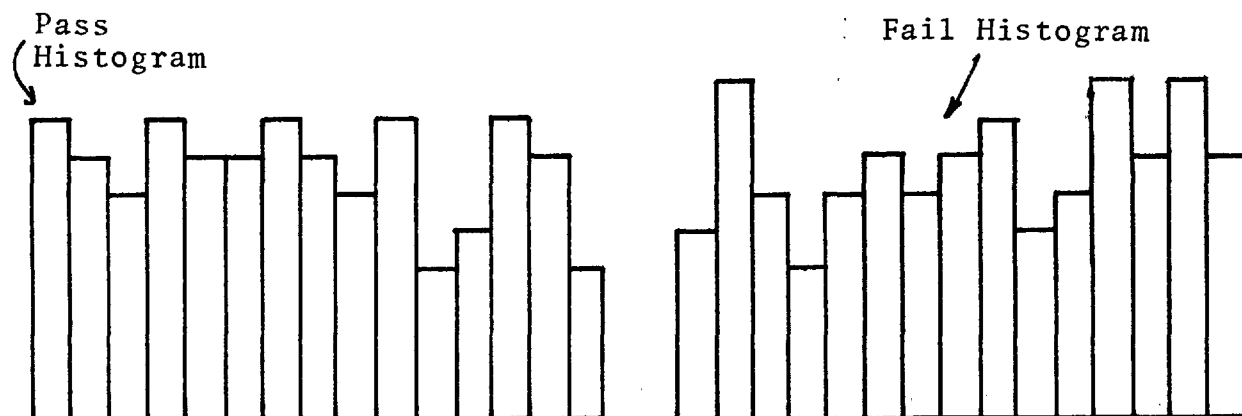
Figure 5.14 : Diagram Showing Pass And Fail Histograms Of The High Pass Filter Circuit Example (For Circuit Diagram And Response See Figures 4.16 And 4.17). The Above Diagrams Are For Component Number 2.



RI For λ=1: 1 0 1 1 1 0 1 0 1 0

λ=0.8: 1 1 1 1 1 1 1 0 1 1

λ=0.5: 1 1 1 1 1 1 1 1 1 1

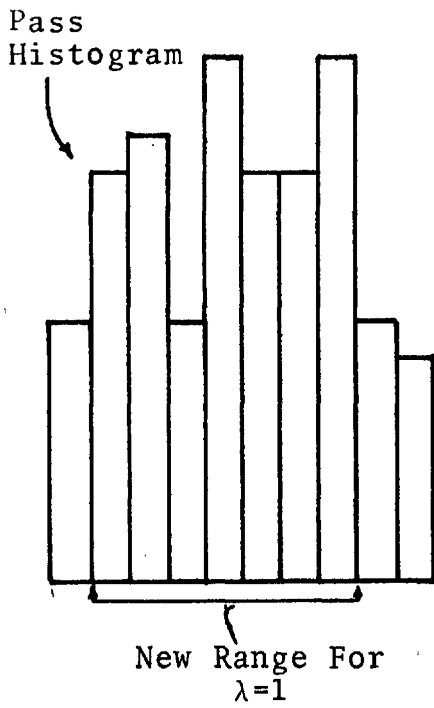


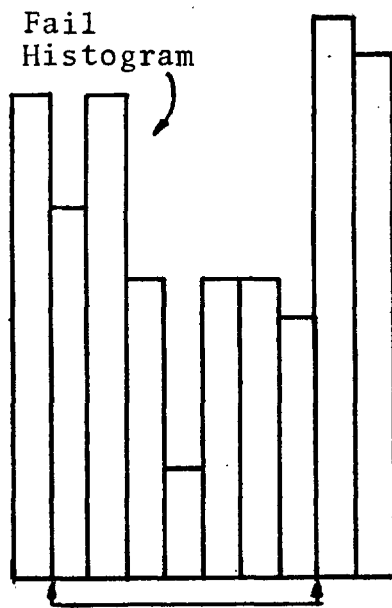
RI For λ=1: 1 0 0 1 1 1 1 0 0 1 0 0 1 0 0

λ=0.8: 1 0 1 1 1 1 1 1 0 1 0 0 1 1 0

λ=0.5: 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

Figure 5.15 : Diagram Showing The Pass And Fail Histograms For The High Pass Filter Circuit Example. (Component Number 3)

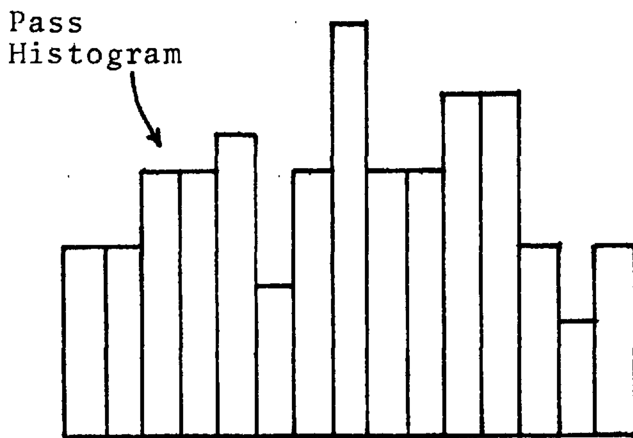


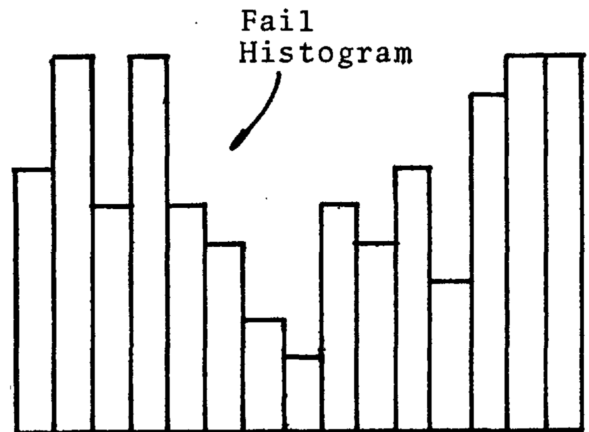


RI For λ=1: 0 1 0 0 1 1 1 1 0 0

λ=0.8: 0 1 1 1 1 1 1 1 0 0

λ=0.5: 1 1 1 1 1 1 1 1 0 0



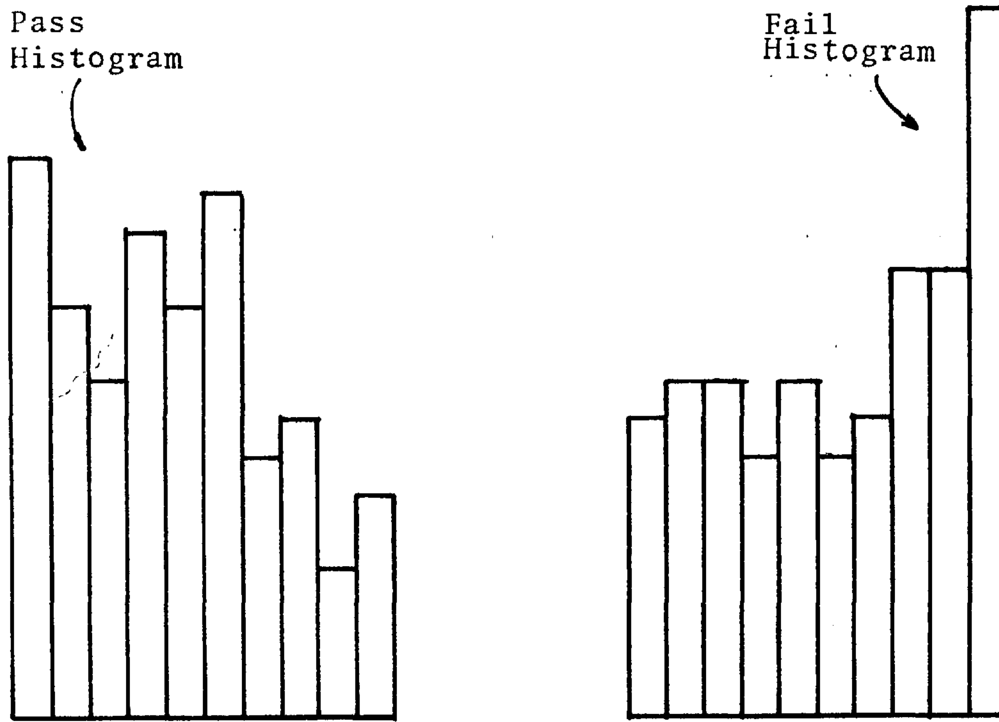


RI For λ=1: 0 0 1 0 1 0 1 1 1 1 1 1 0 0 0

λ=0.8: 0 0 1 0 1 1 1 1 1 1 1 1 0 0 0

λ=0.5: 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0

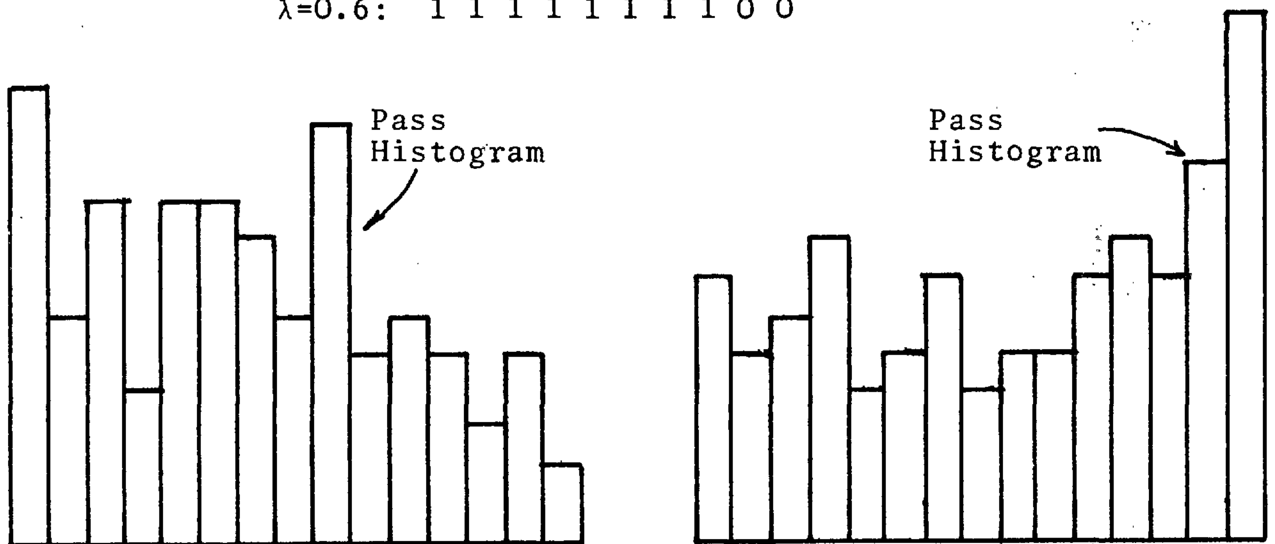
Figure 5.16 : Diagram Showing The Pass And Fail Histograms For The High Pass Filter Circuit Circuit Example. (component Number 4)



RI For $\lambda=1$: 1 1 1 1 1 1 0 0 0 0

$\lambda=0.8$: 1 1 1 1 1 1 0 1 0 0

$\lambda=0.6$: 1 1 1 1 1 1 1 1 0 0

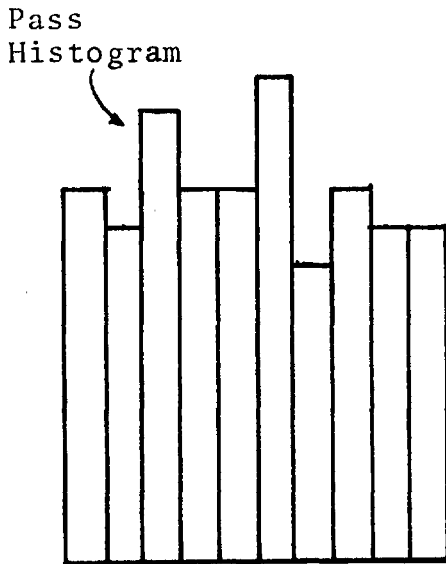


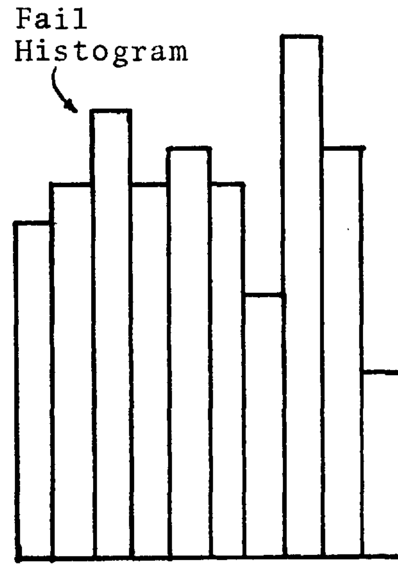
RI For $\lambda=1$: 1 1 1 0 1 1 1 1 1 1 0 0 0 0 0

$\lambda=0.8$: 1 1 1 0 1 1 1 1 1 1 1 1 0 0 0

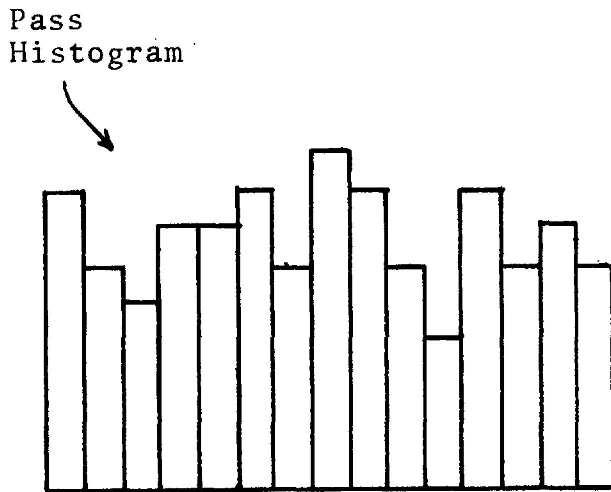
$\lambda=0.6$: 1 1 1 0 1 1 1 1 1 1 1 1 0 0 0

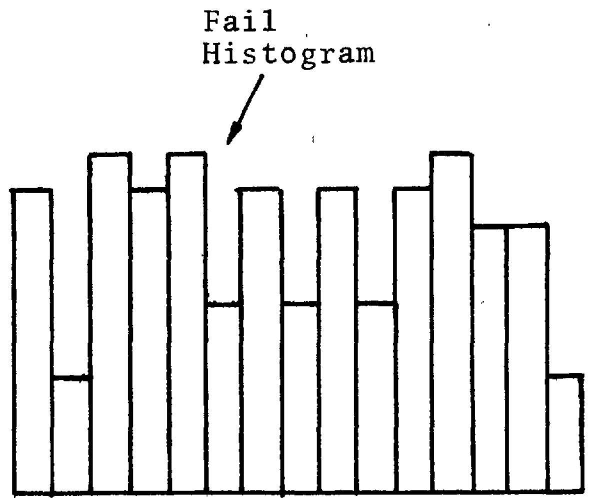
Figure 5.17 : Diagram Showing The Pass And Fail Histograms For The High Pass Filter Circuit Example (Component Number 6)





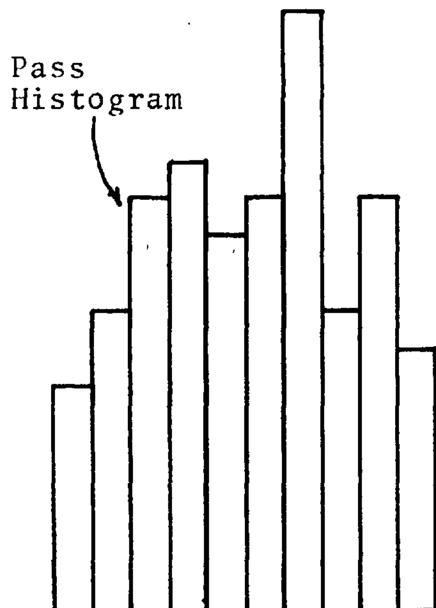
RI For		
	λ=1:	1 0 1 0 0 1 1 0 0 1
	λ=0.8:	1 1 1 1 1 1 1 1 0 1
	λ=0.5:	1 1 1 1 1 1 1 1 1 1

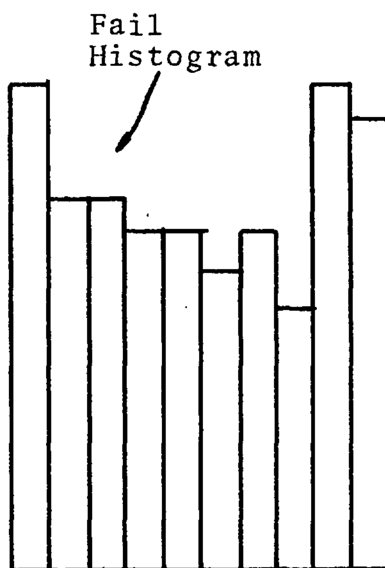




RI For		
	λ=1:	1 1 0 0 0 1 0 1 0 1 0 0 0 0 1
	λ=0.8:	1 1 0 1 1 1 0 1 1 1 0 1 1 1 1
	λ=0.5:	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

Figure 5.18 : Diagram Showing The Pass And Fail Histograms For The High Pass Filter Circuit Example. (Component Number 7)

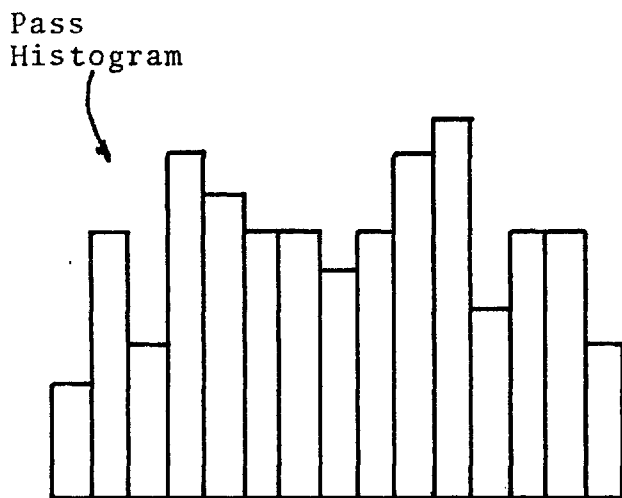


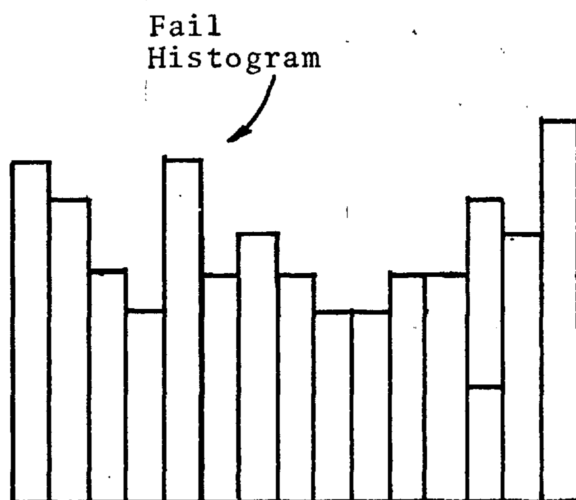


RI For λ=1: 0 0 1 1 1 1 1 0 1 1

λ=0.8: 0 0 1 1 1 1 1 0 1 1

λ=0.6: 0 1 1 1 1 1 1 1 1 1



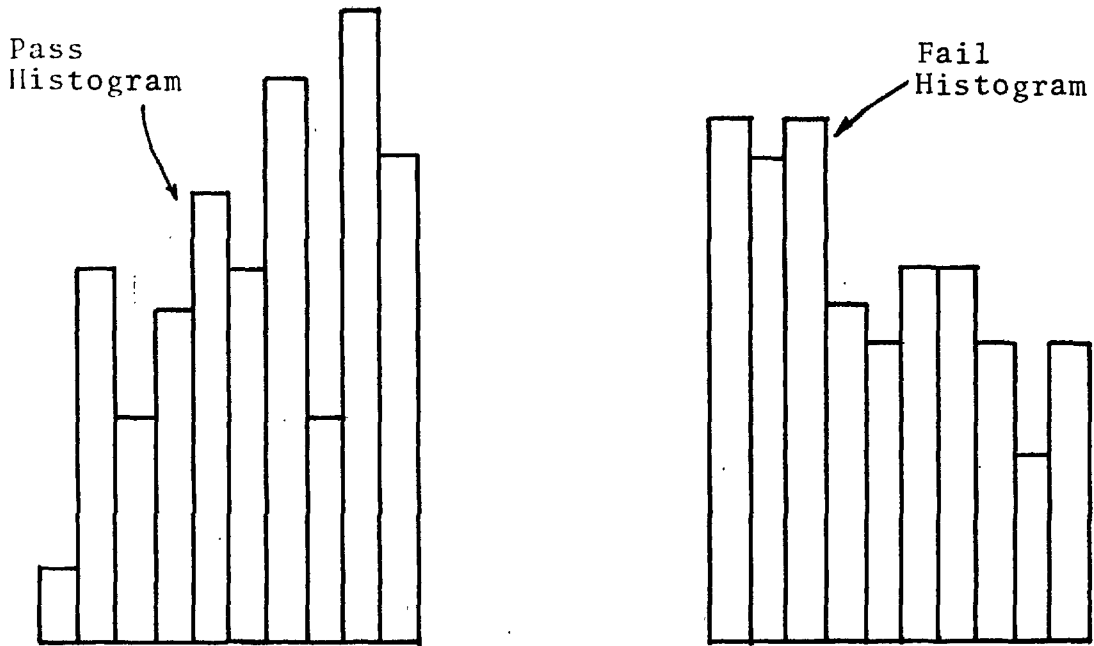


RI For λ=1: 0 0 0 1 0 1 1 1 1 1 1 0 0 0 0

λ=0.8: 0 1 0 1 1 1 1 1 1 1 1 1 1 1 0

λ=0.6: 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0

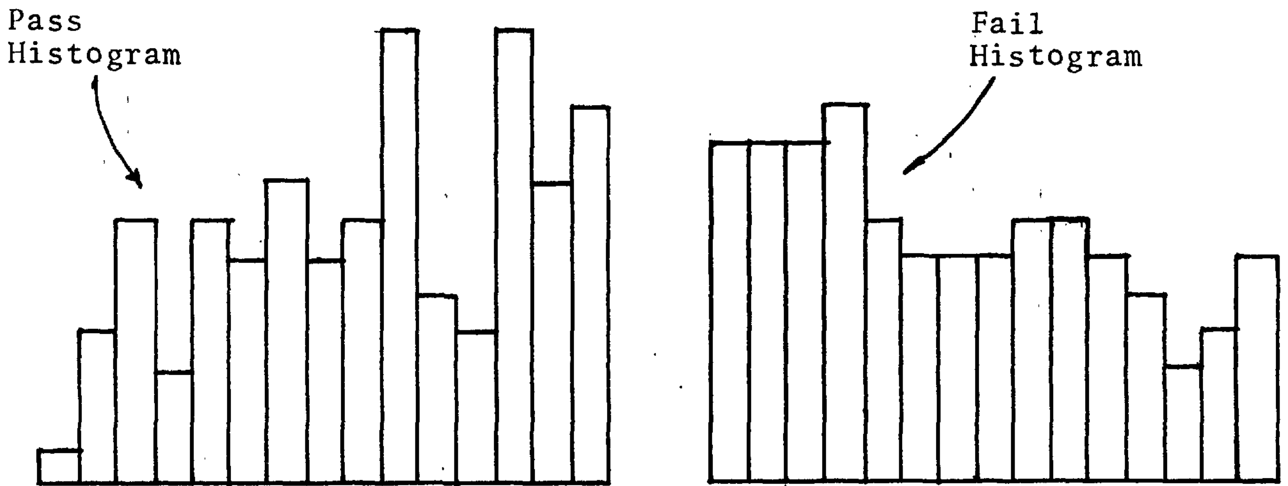
Figure 5.19 : Diagram Showing The Pass And Fail Histograms For The High Pass Filter Circuit Example. (Component Number 8)



RI For λ=1: 0 0 0 0 1 1 1 0 1 1

λ=0.8: 0 1 0 1 1 1 1 0 1 1

λ=0.6: 0 1 0 1 1 1 1 0 1 1



RI For λ=1: 0 0 0 0 0 0 1 1 1 1 0 1 1 1 1

λ=0.8: 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1

λ=0.6: 0 0 1 0 1 1 1 1 1 1 1 1 1 1

Figur 5.20 : Diagram Showing The Pass And Fail Histograms For The High Pass Filter Circuit Circuit Example. (Component Number 10)

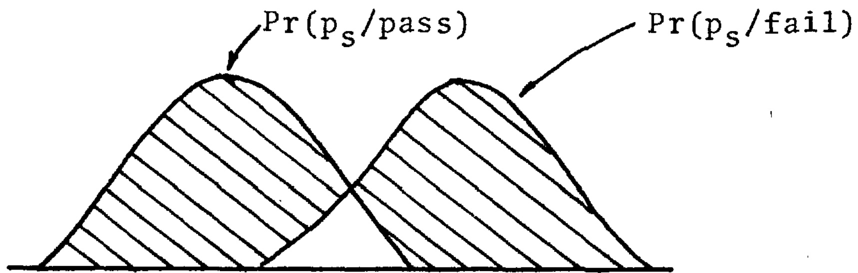


Figure 5.21(a) Yield Sensitivity Is The Sum Of The Shaded Areas.

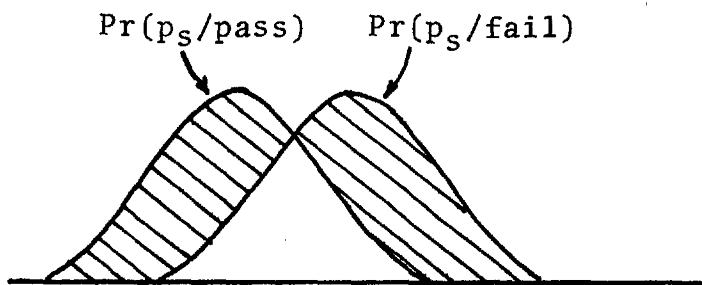


Figure 5.21(b) Illustrating Low Yield Sensitivity. Minimum Value Is 0 .

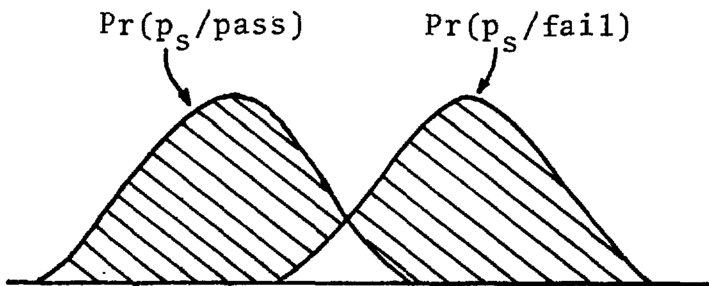


Figure 5.21(c) Illustrating Intermediate Yield Sensitivity.

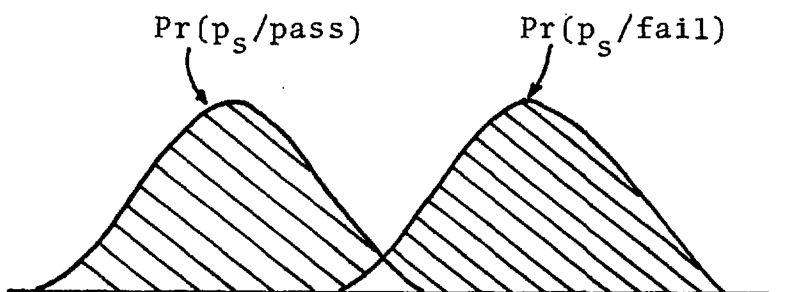


Figure 5.21(d) Illustrating High Yield Sensitivity. Maximum Value Is 2

p_s →

Figure 5.21 : Illustrating The Definition Of Yield Sensitivity.

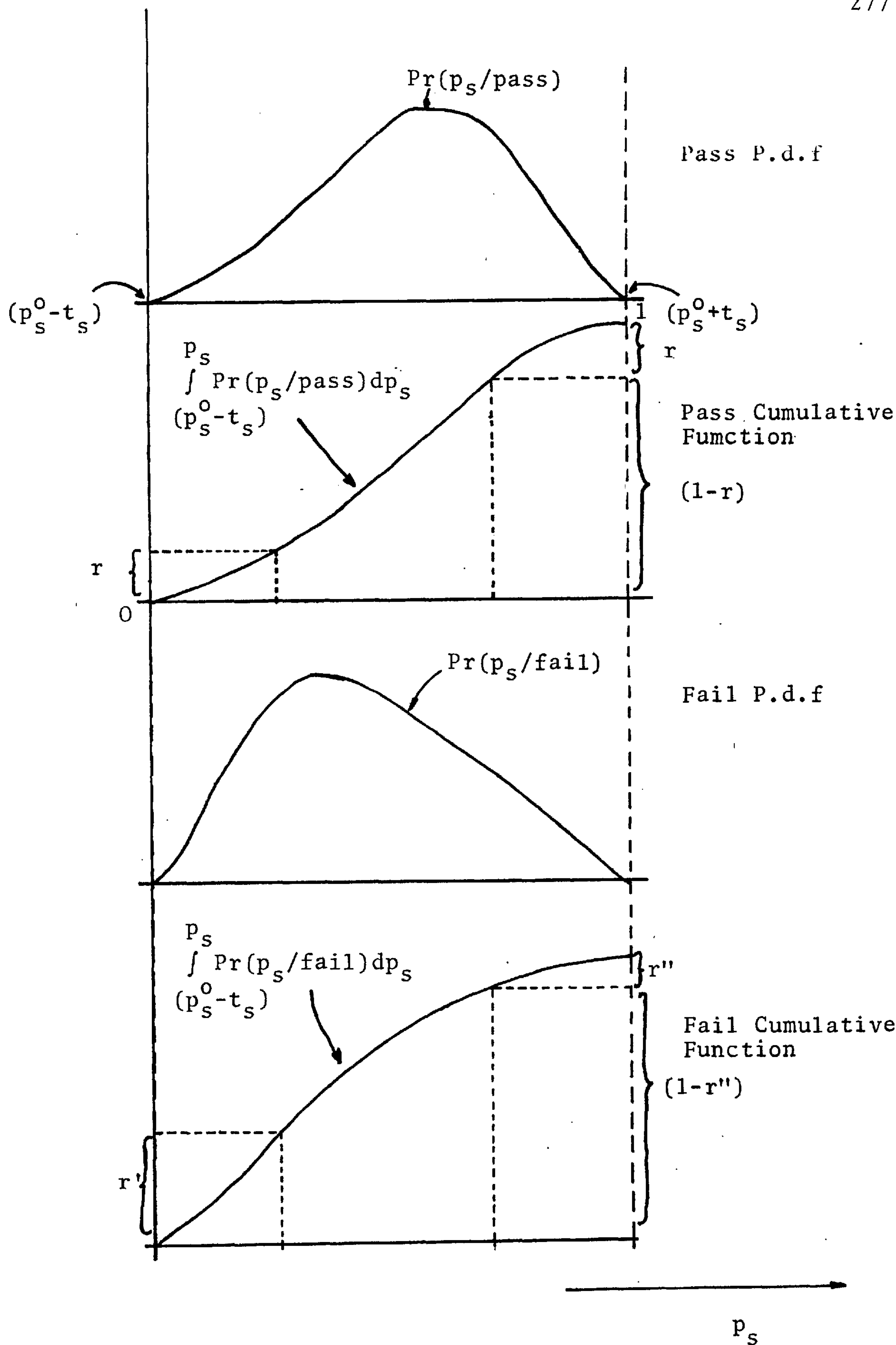
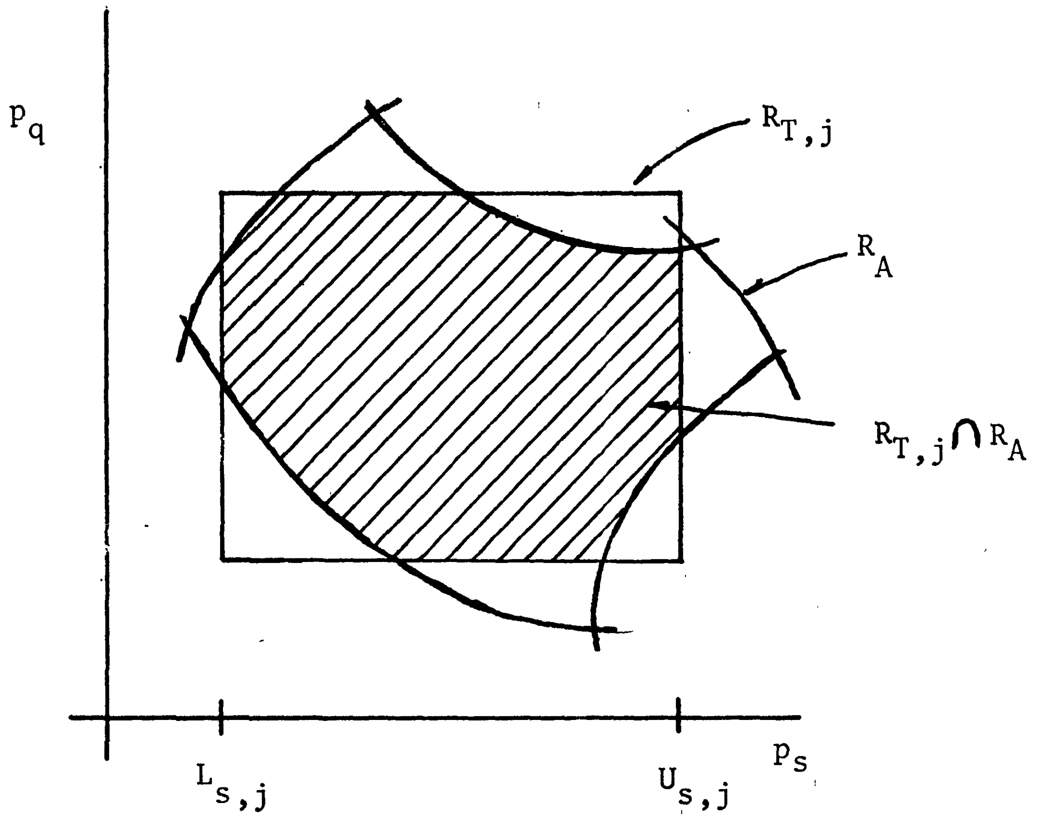


Figure 5.22 : Illustrating The PERTOL Criterion For Tolerance Assignment.



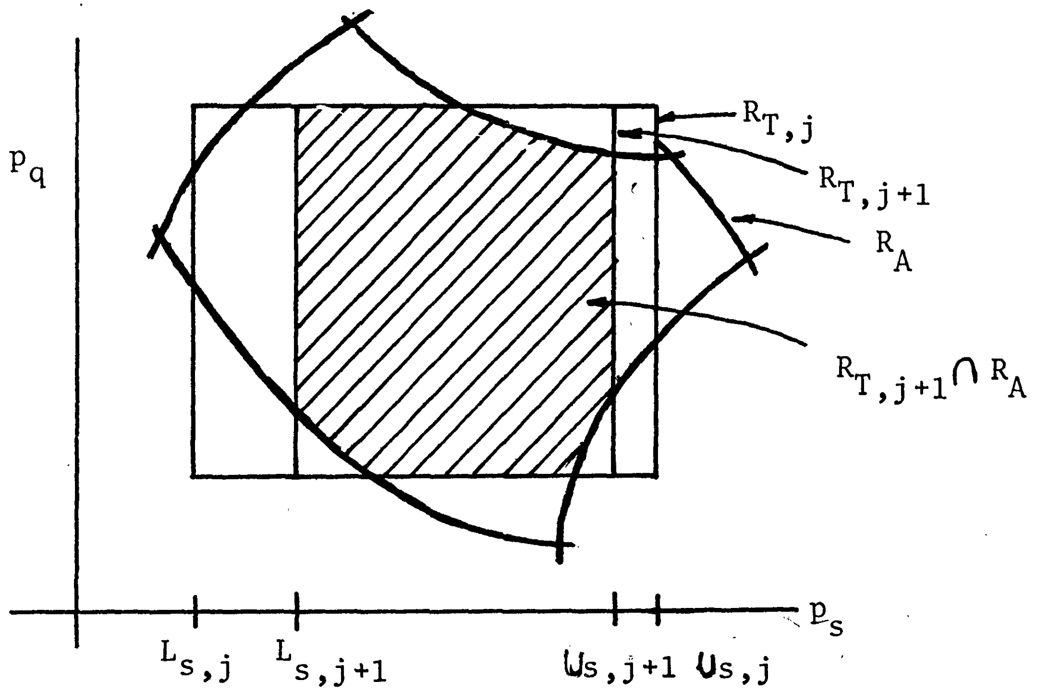


Figure 5.23 : Illustrating Some Terminology

1
Cost
0.8
0.6
0.4
0.2
A
B
C
At Iteration Number 1,
$C_A=C_T=0.15$
$\beta=0.2813$
Note : Cost Is Normalized
To Unity For Iteration One.
1 2 3 4 5 6 7
Iteration Number

Figure 5.24 : Cost Trajectories For The Band Pass Filter Circuit Example

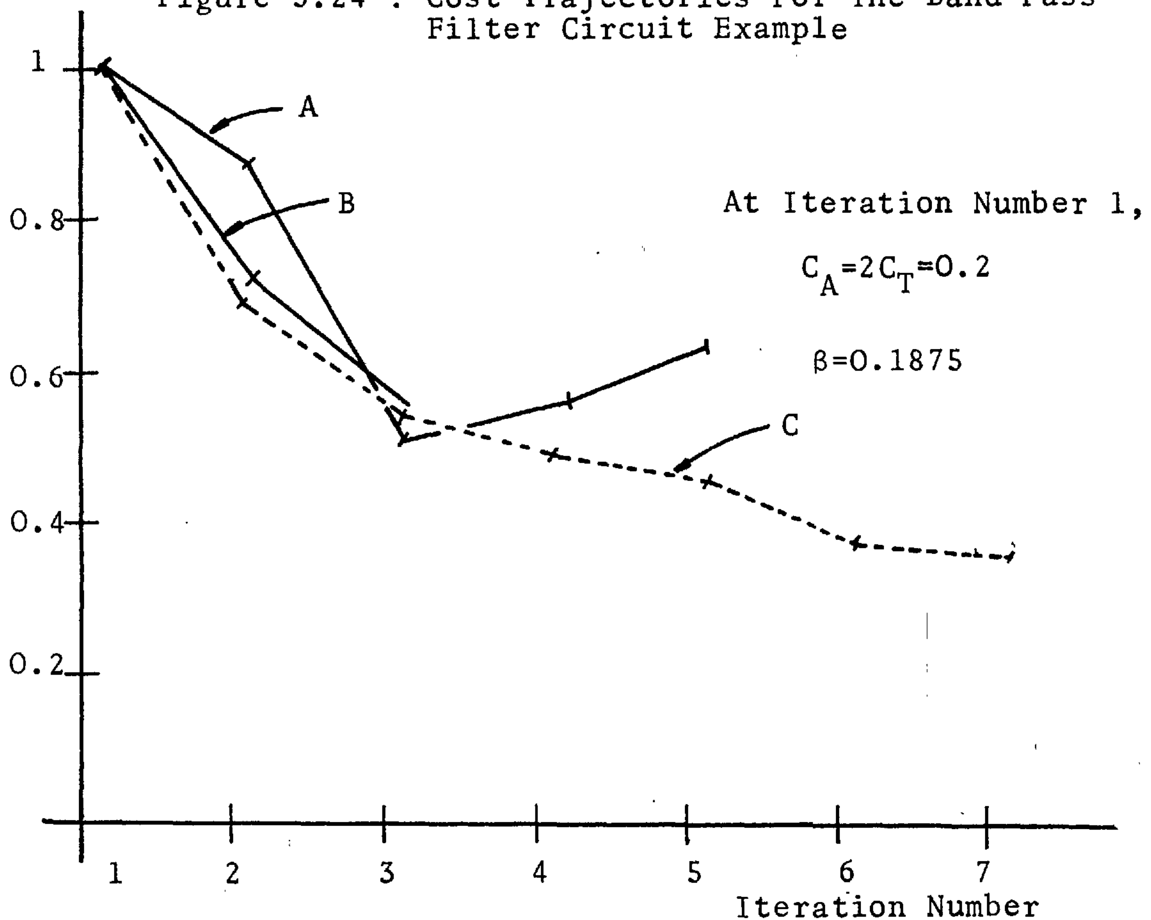


Figure 5.25 : Cost Trajectories For The Band Pass Filter Circuit Example.

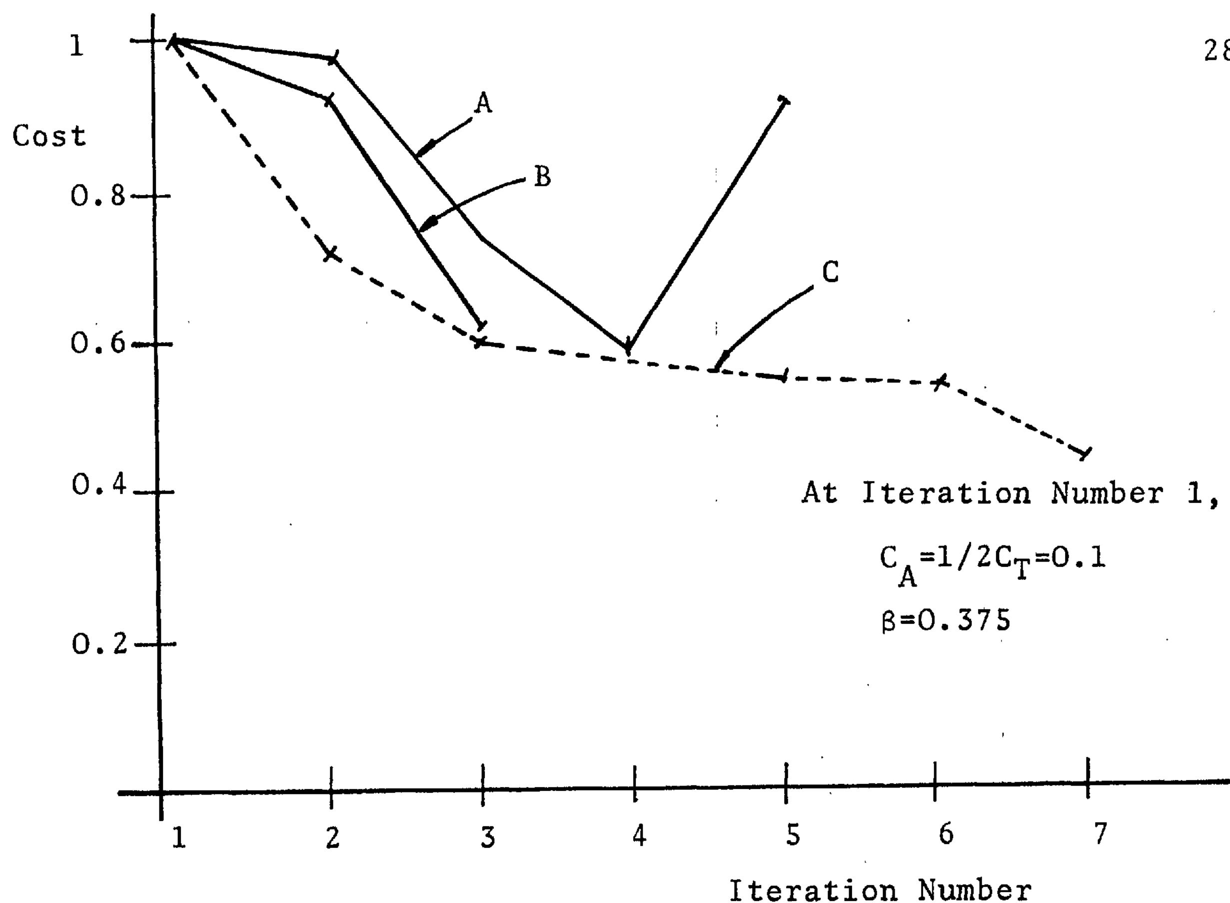


Figure 5.26 : Cost Trajectories For The Band Pass Filter Circuit Example

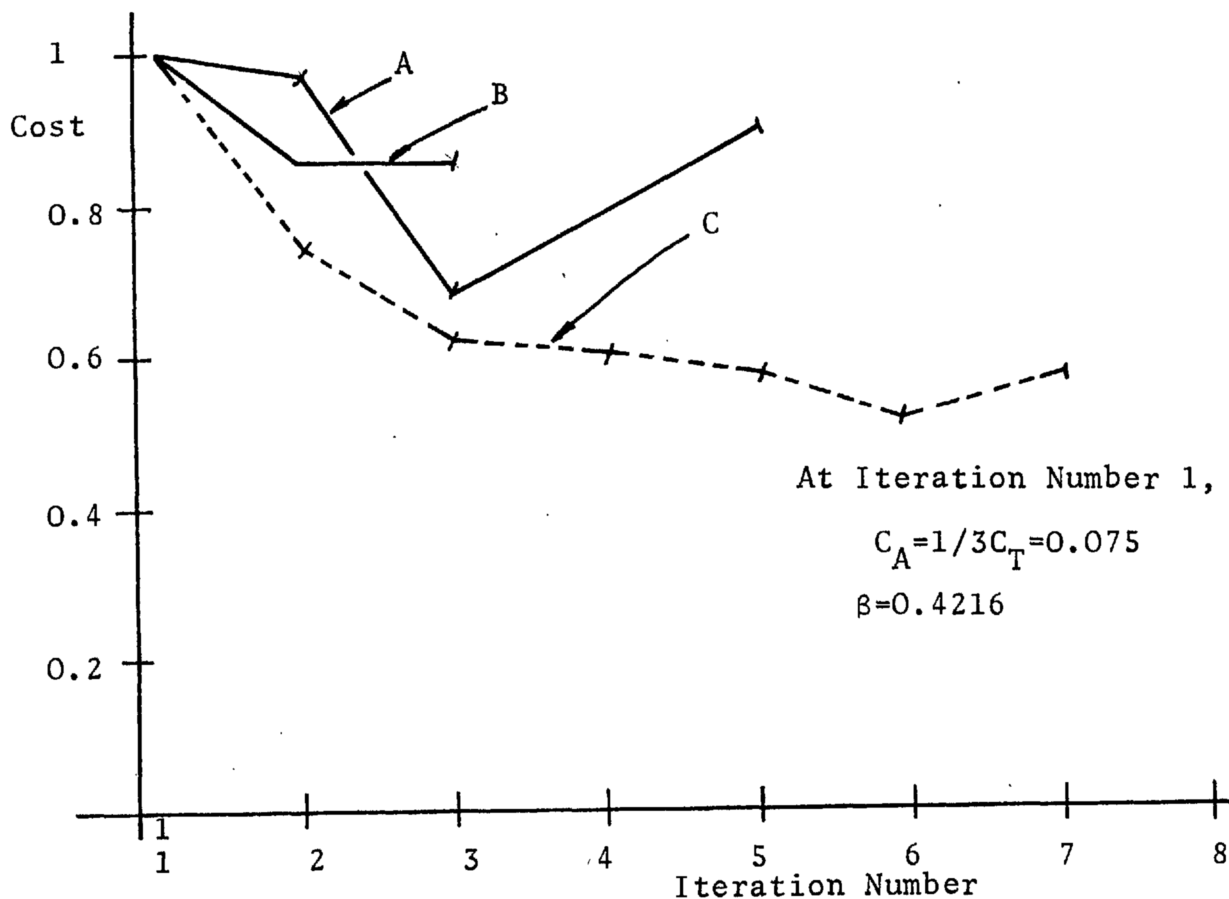


Figure 5.27 : Cost Trajectories For The Band Pass Filter Circuit Example

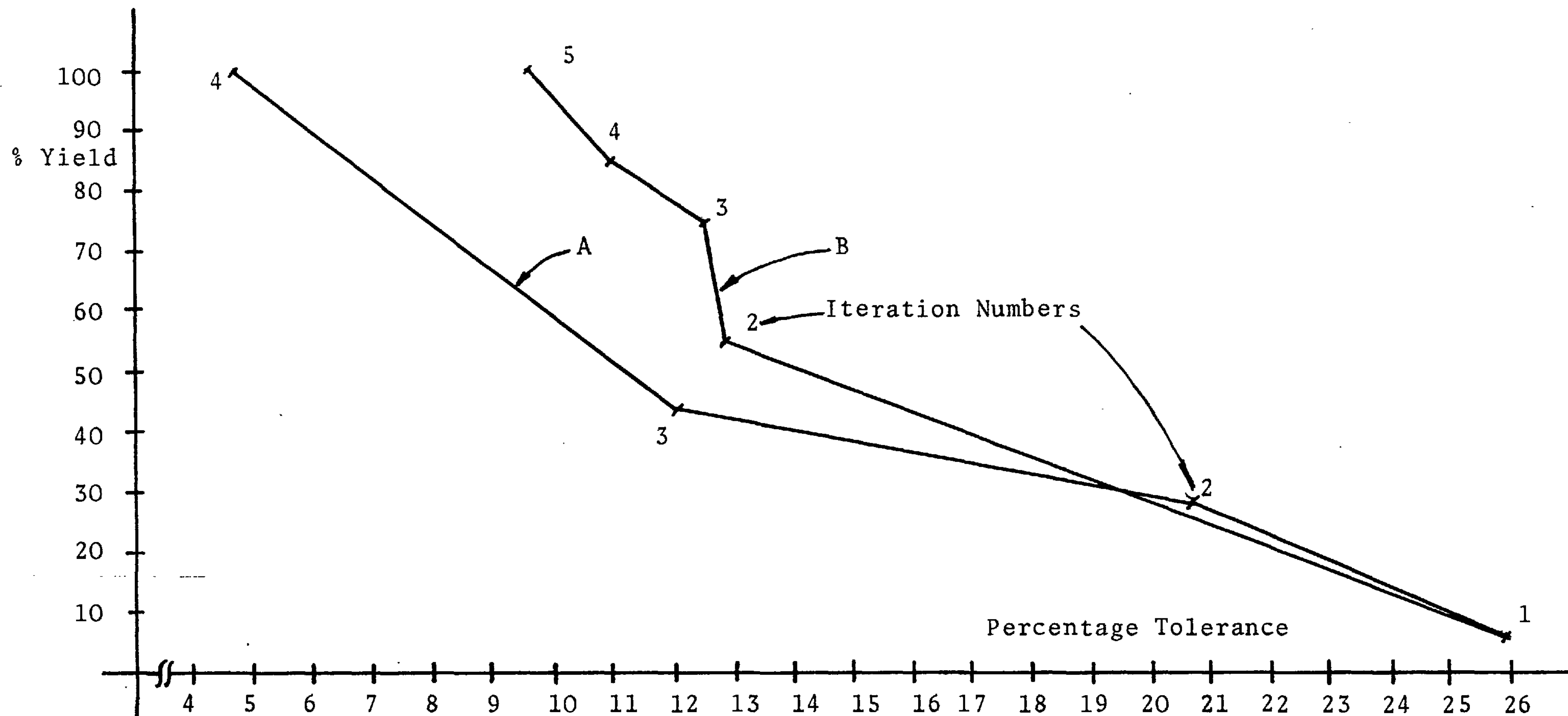


Figure 5.28 : Yield-Tolerance Trajectories For The High Pass Filter Circuit (For Circuit Diagram And Response Curves See Figure 4.16 And 4.17) These Trajectories Refer To Component Number 2)

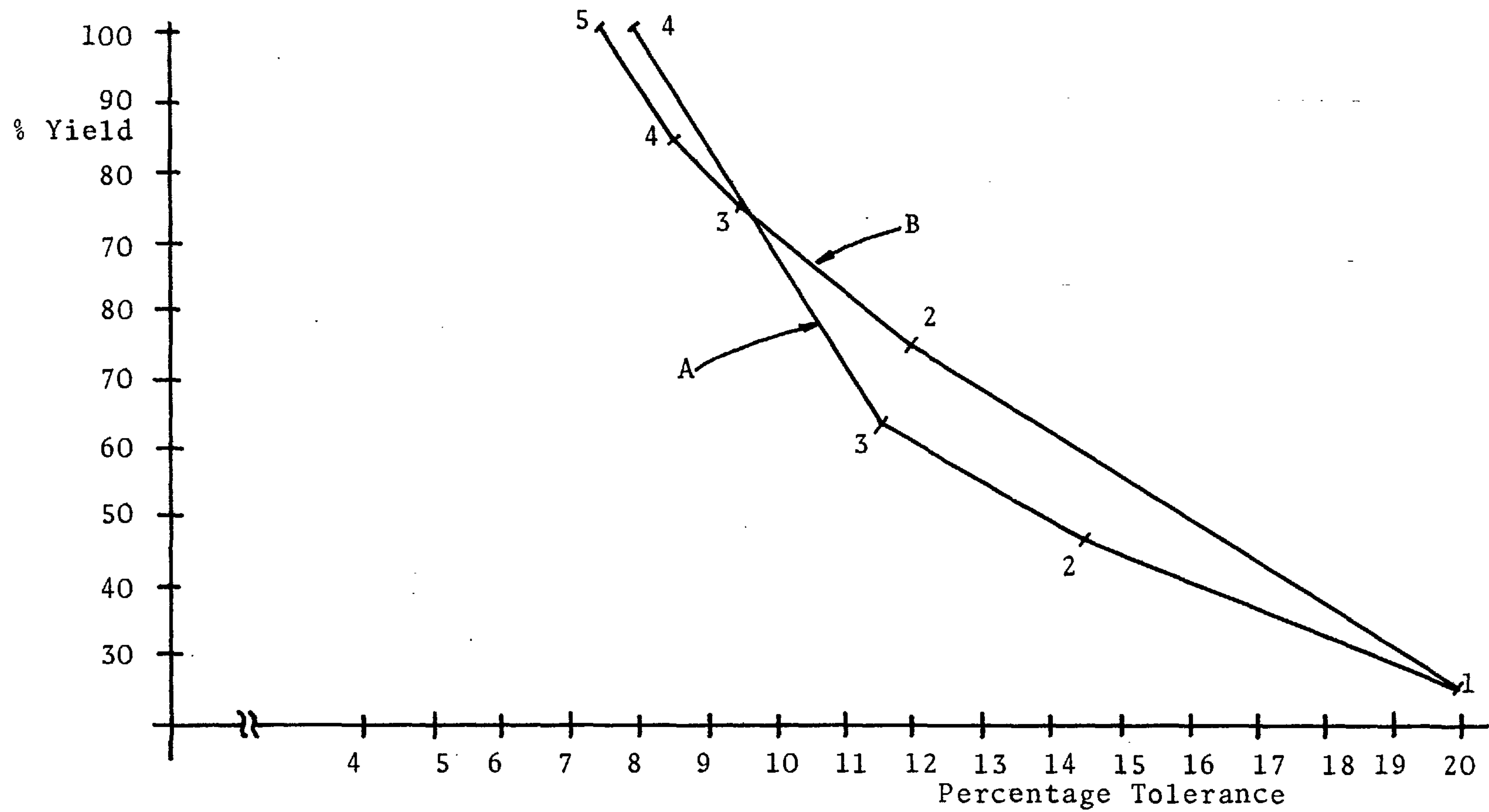


Figure 5.29 : Yield-Tolerance Trajectories For The High Pass Filter Circuit Example. (Component Number 3)

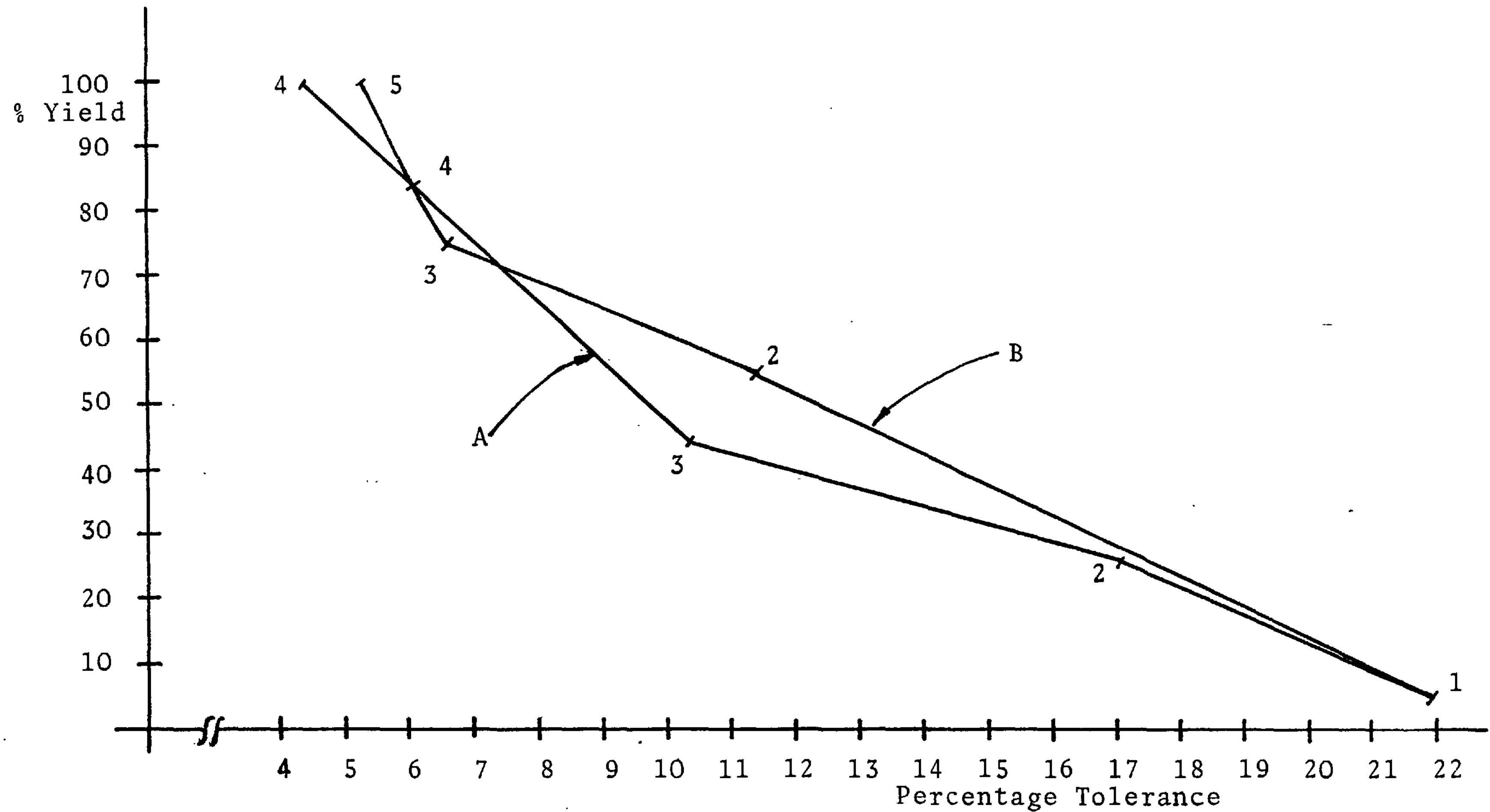


Figure 5.30 : Yield-Tolerance Trajectories For The High Pass Filter Circuit Example (Component Number 4)

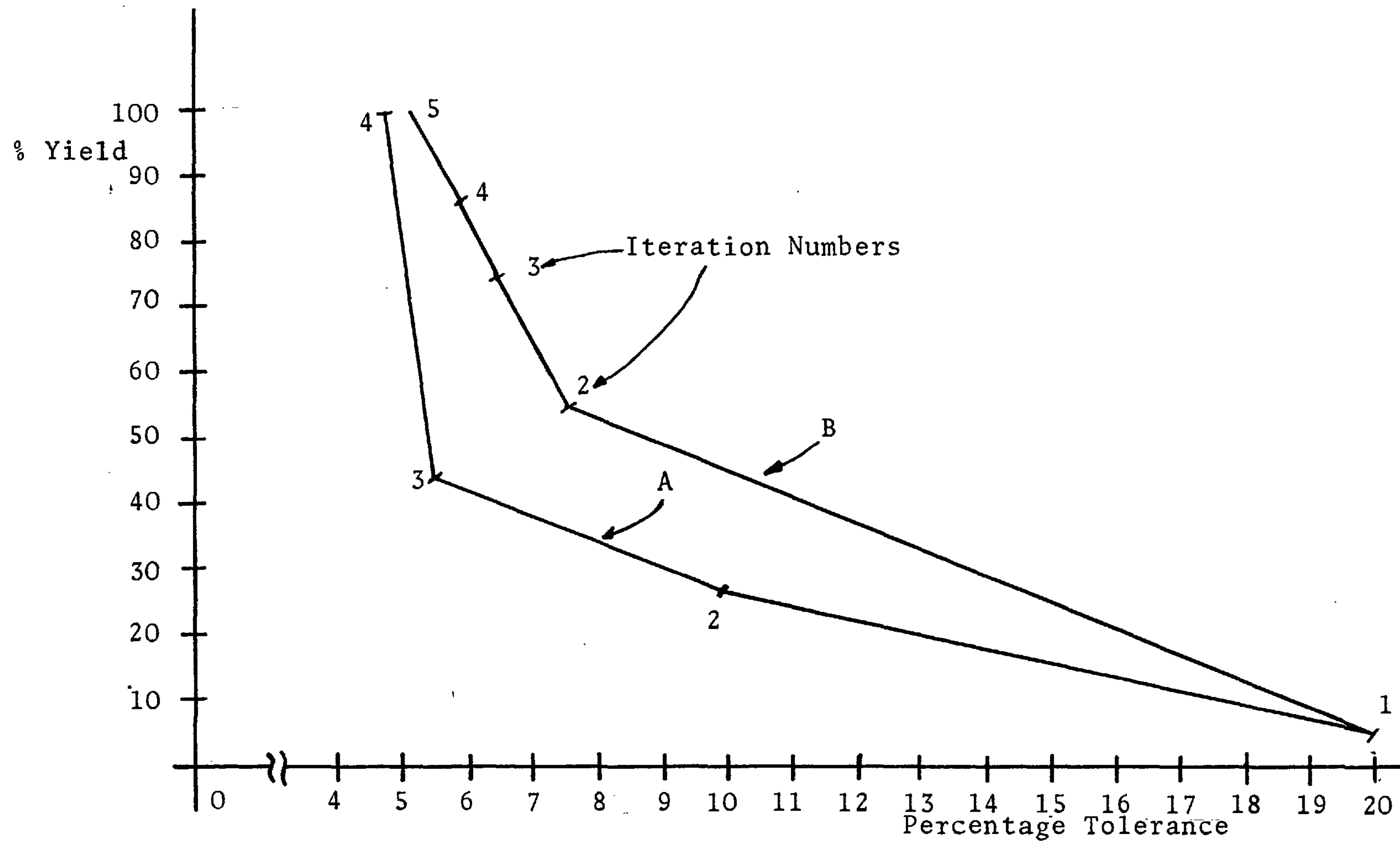


Figure 5.31 : Yield-Tolerance Trajectories For The High Pass Filter Circuit (Component Number 6)

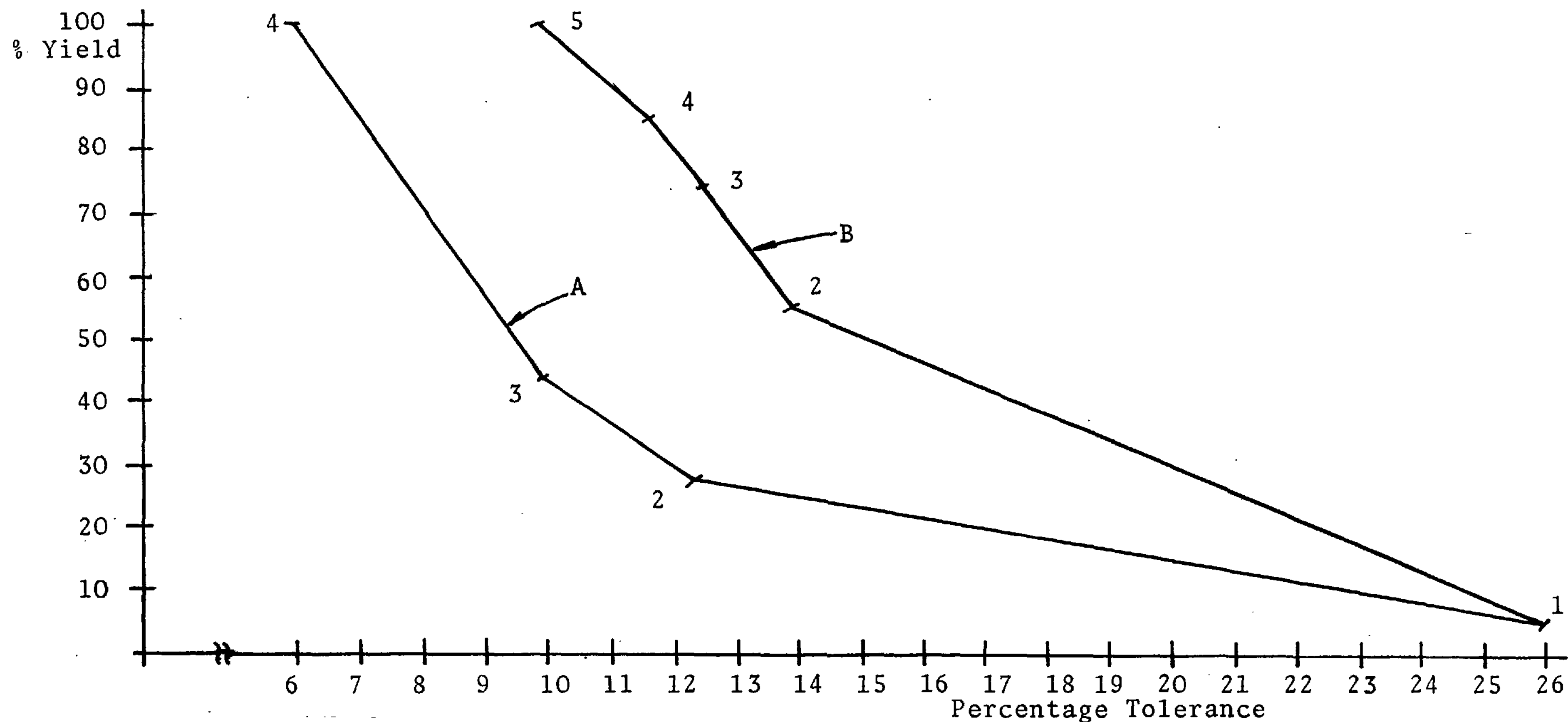


Figure 5.32 : Yield-Tolerance Trajectories For The High Pass Filter Circuit Example (Component Number 7)

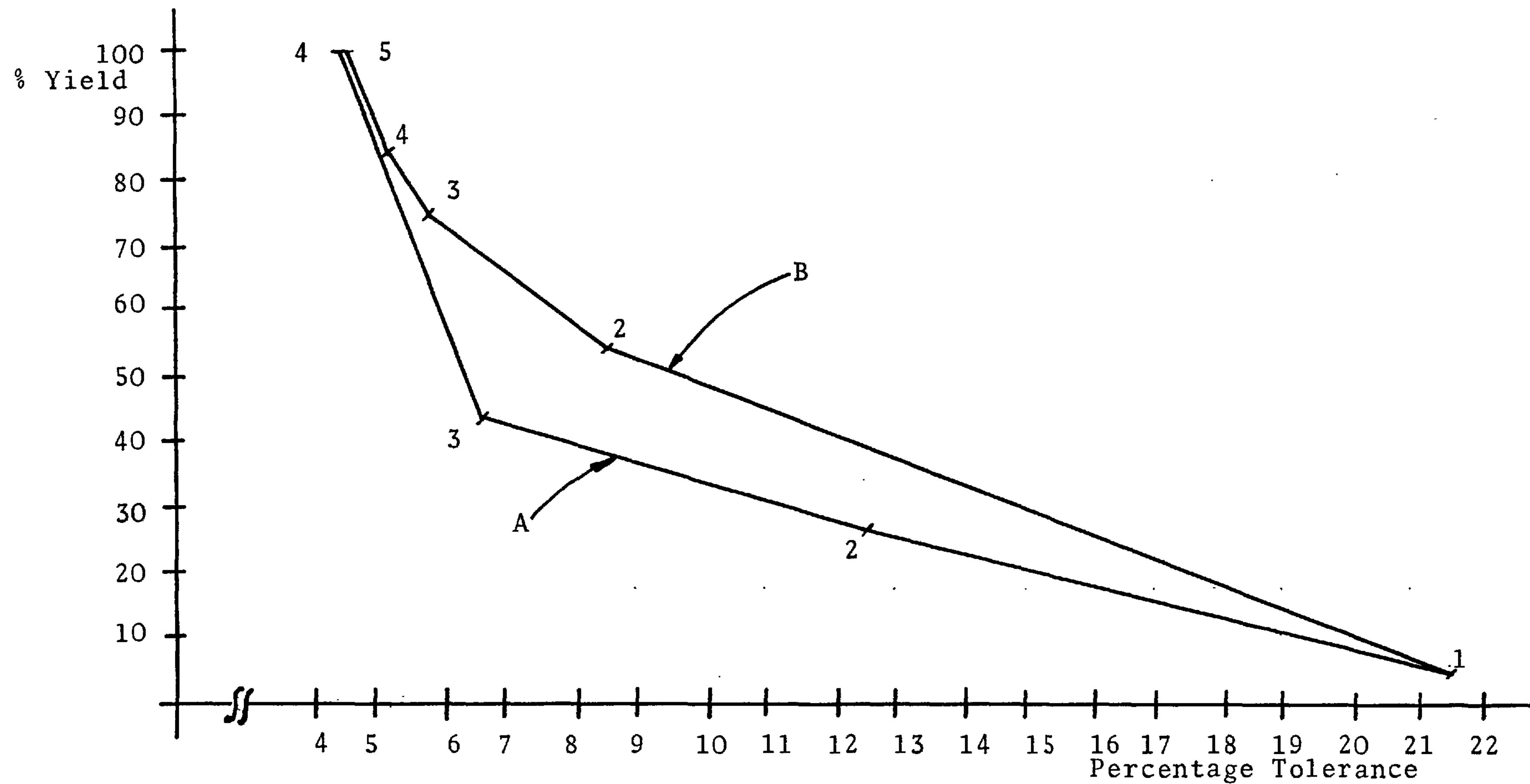


Figure 5.33 : Yield-Tolerance Trajectories For The High Pass Filter Circuit Example (Component Number 8)

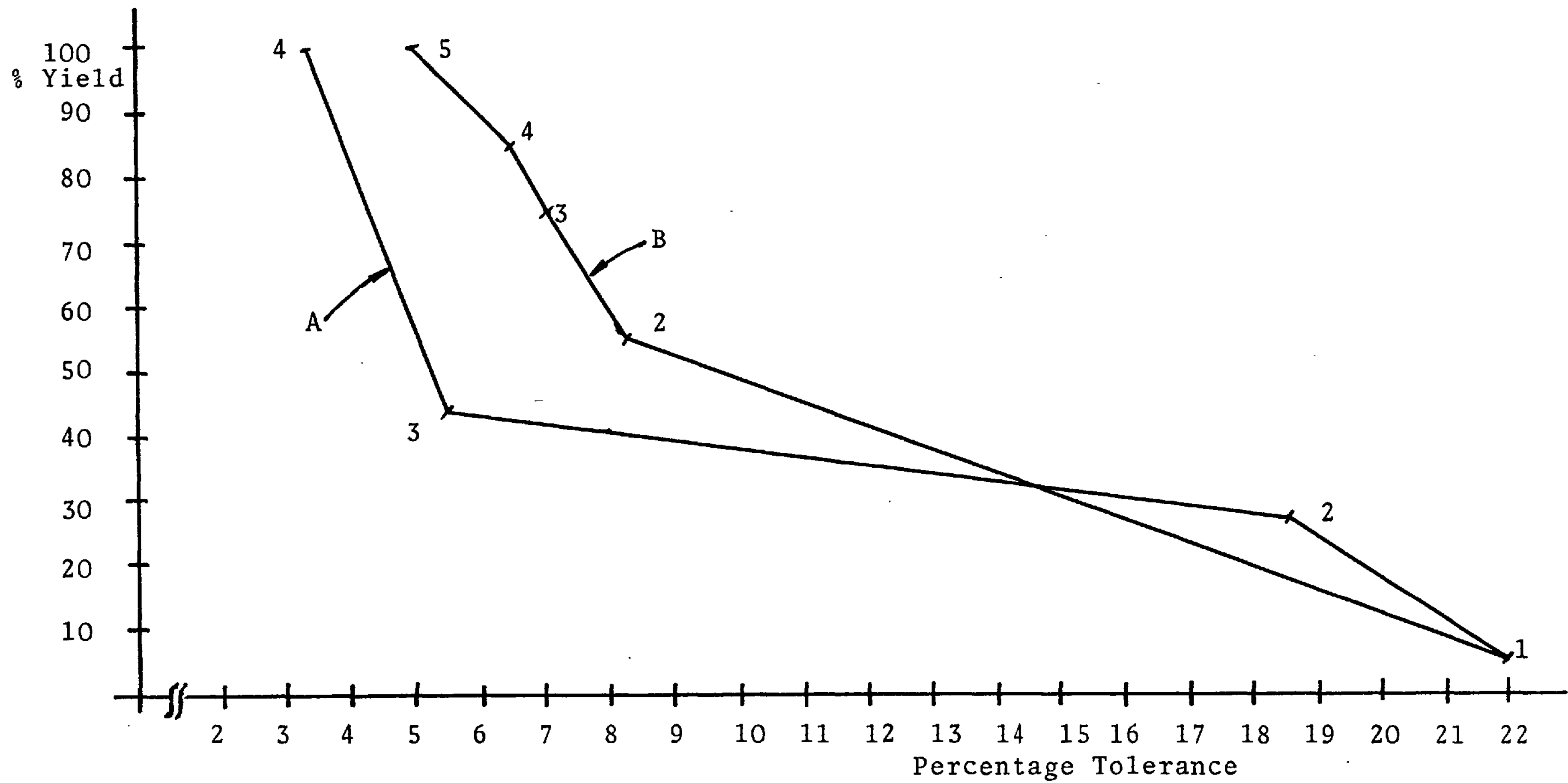


Figure 5.34 : Yield-Tolerance Trajectories For The High Pass Filter Circuit Example (Component Number 10)

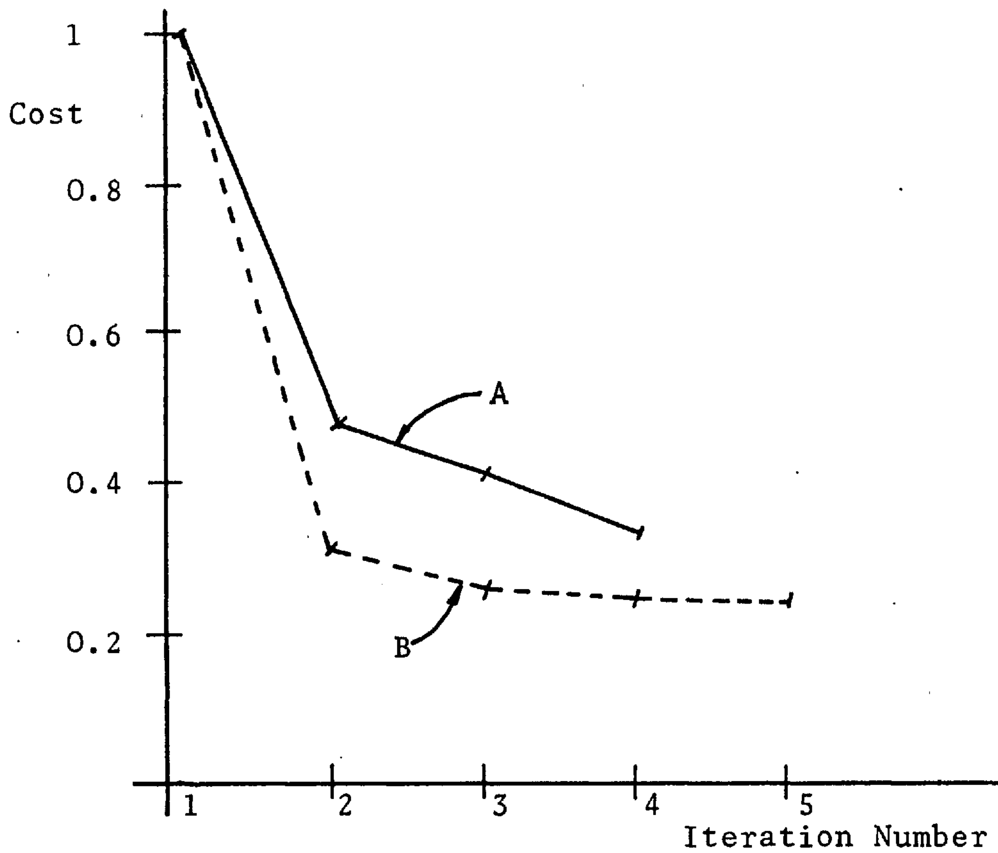


Figure 5.35 : Cost Trajectories For The High Pass Filter Circuit Example

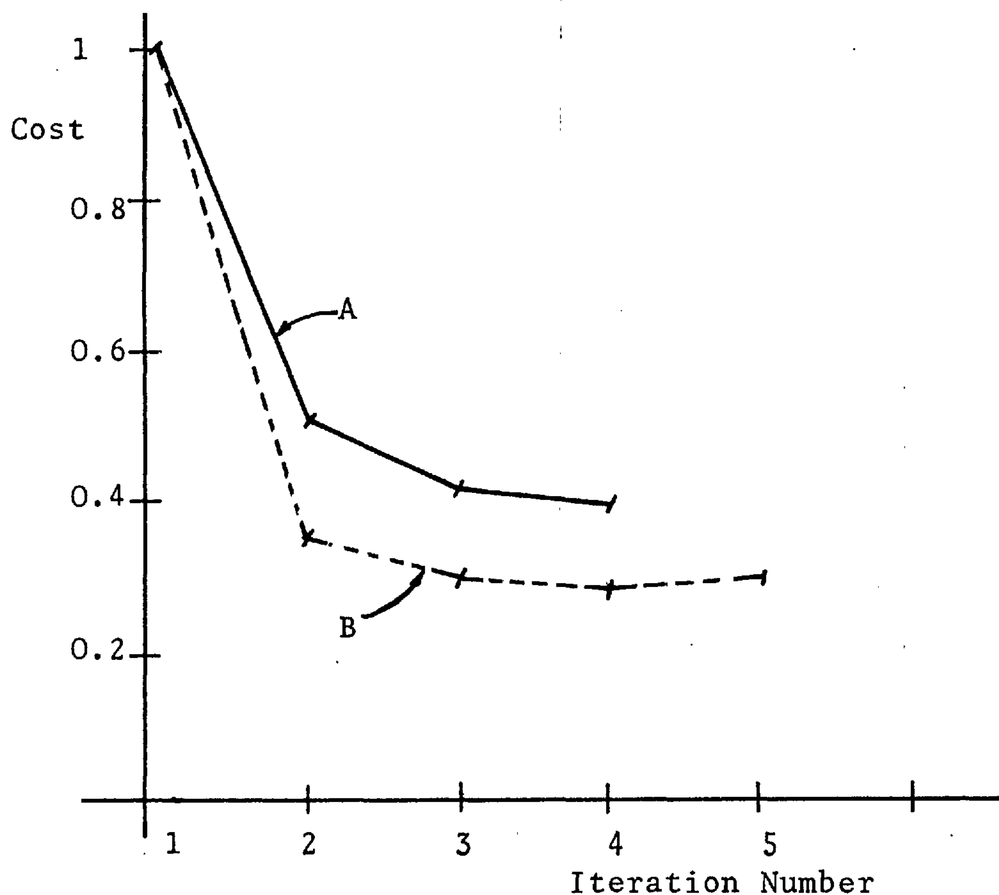


Figure 5.36 : Cost Trajectories For The High Pass Filter Circuit Example.

CHAPTER 6 - SUMMARY AND SUGGESTIONS FOR FURTHER RESEARCH.

6.1 Introduction.

6.2 Summary of the thesis and conclusions.

6.3 Suggestions for further research.

6.3.1 Extensions to techniques developed in the thesis.

6.3.2 Extension of the Monte Carlo based design approach to other problems in the field of statistical design.

CHAPTER SIX

SUMMARY AND SUGGESTIONS FOR FURTHER RESEARCH

6.1 INTRODUCTION

Our main research contribution has been the introduction and development of a number of algorithms and techniques addressed to the design centering and tolerance assignment problems. The new algorithms are introduced in the light of a critical assessment of existing techniques reported in the literature. In this final chapter we summarize the contents of the thesis and make suggestions for future research.

6.2 SUMMARY OF THE THESIS AND CONCLUSIONS

Chapter one is a general review of the field of statistical design. Some useful notation and terminology is introduced and explained. The two most widely used methods of statistical analysis, viz. Monte Carlo analysis and the method of moments are briefly described.

It is shown that Monte Carlo analysis is a general procedure which is applicable for any form of component parameter p.d.f. In addition it does not require assumptions about the form of the p.d.f. of circuit responses. In particular the procedure for estimating manufacturing yield is described. For a specific circuit the cost of a Monte Carlo estimation of yield is proportional to the number N, of sample circuits analysed.

It is shown that the accuracy of the yield estimates is proportional to $1/\sqrt{N}$. Therefore, to achieve a certain accuracy the number of sample circuits required to be analysed is independent of the number of toleranced components in the circuit.

The method of moments on the other hand although computationally cheaper then Monte Carlo analysis, is less general. The method approximates the moments of the response p.d.f.$\Omega(.)$ as functions of the component parameter p.d.f. $\emptyset(.)$. The approximating functions are of limited validity as they are based on Taylor series approximations of the circuit's responses. The method is commonly employed to obtain estimates of the second moments of $\Omega(.)$. However, to estimate parameters such as yield, assumptions need to be made about the functional form of $\Omega(.)$. A common assumption that $\Omega(.)$ is multidimensional Gaussian has been demonstrated to be generally invalid /32/. Even if we make a suitable assumption the computational procedure becomes very complex as the number of performance constraints becomes large. The use of the method of moments in conjuction with the Bonferoni inequalities procedure to estimate yield is described.

To perform effective statistical design, knowledge of the form of statistical distributions of component parameters is essential. The problem of characterizing the statistical distributions of component parameters, also called statistical modelling is still the subject of active research/54/.

Statistical modelling falls outside our immediate area of research. Therefore in chapter one we make only brief comments on the type of distributions encountered in discrete and integrated circuit components.

In addition to tolerance assignment and design centering, some other problems in the field of statistical design are briefly described. These include the specification of performance constraints in manufactured circuits; the specification of sub-system performance constraints in system design; and various problems related to the specification of performance tests on manufactured circuits. The possible use of Monte Carlo analysis to help solve such problems is emphasised.

In chapter two we make a critical assessment of reported methods of tolerance assignment and design centering. The chapter commences with a discussion of relevent cost functions and of different problem formulations which fall under the general titles of tolerance assignment and design centering. The methods reviewed are considered under four categories, viz. geometrical characterization, standard non-linear programming, iterative Monte Carlo based methods, and discrete methods.

As is discussed in chapter one, geometrical interpretations may be given to the various problem formulations. The most successful geometrical method so far, simplicial approximation /21/, approximates the region of acceptability as a simplex of bounding hyperplanes. The procedure becomes prohibitively expensive as the number of statistically varying parameters increases beyond about ten.

The methods based on standard non-linear programming are considered in two groups. Firstly worst case methods, which seek minimum cost tolerance solutions constrained to return 100% (unity) yield; and secondly statistical, which allow yields of less then 100%. It is shown that both groups of method avoid the explicit evaluation of yield. The worst case methods require tests to check the unity yield condition. Some of the different worst case testing methods are discussed in chapters two and three. The statistical methods on the other hand constrain yield to be greater than a certain lower bound. The constraints on yield are then transformed to constraints on tolerance via approximate relationships such as the transmission of variances equation /12/ (i.e. the method of moments).

The main shortcoming of the worst case methods is overdesign. In general it is possible to trade off yield against tolerances. The worst case methods do not explore this trade-off and hence provide expensive tolerance solutions. In addition the worst case methods are inapplicable in situations where 100% yield is not achievable with available tolerances. The latter situation commonly arises in the manufacture of integrated circuits.

The statistical non-linear programming based methods allow yield to be less than 100% and do not produce as tight tolerances as the worst case methods. Nevertheless statistical methods maximize tolerances for a particular choice of yield and still do not explore the yield-tolerance trade-off. To explore this trade-off the optimization could be repeated for different choices of yield. However, the unreliability of a yield estimation

procedure based on the transmission of variances equation renders this approach unattractive.

The methods based on Monte Carlo analysis have important advantages over both the geometrical and the non-linear programming based methods. Firstly, in estimating yield the number of circuit analyses required in Monte Carlo analysis is independent of the number of toleranced components. This implies that the methods may be considered for large circuits. Secondly the Monte Carlo yield estimation procedure is more general and more reliable than the method of moments. Our main contribution of new techniques falls in the area of Monte Carlo based methods, as is discussed in chapters four and five. Therefore only brief mention is made of it in chapter two.

All three categorries of method discussed above provide continuous solutions. In practice however, only discrete choices may be available for tolerance and nominal values. The expedient of rounding off the best continuous solution to the nearest allowable discrete solution does not always provide the best available discrete solution. Discrete methods work in terms of the discrete choices without first seeking continuous solutions. The main shortcomings of this approach arise from the fact that the number of available discrete solutions becomes very large for the size of most circuit examples of interest. Therefore the computational effort is often prohibitive.

A number of new algorithms and techniques are introduced in chapters three, four and five. Chapter three is concerned with the discrete worst-case tolerance assignment problem, while chapters four and five respectively consider design centering and tolerance assignment methods based on Monte Carlo analysis.

In chapter three we deal with a class of method called the branch and bound method. The two main computational tasks in such a method are, firstly a strategy for selecting tolerance solutions and secondly suitable methods for testing these solutions for compliance with the worst case requirement. The results of such tests allow a number of the possible solutions to be eliminated from consideration. By suitably selecting test solutions, the methods effectively eliminate most of the non-feasible[α] solutions from consideration. Thus the optimum tolerance solution can be identified after evaluating only a few of the many possible tolerance solutions.

In chapter three a brief summary of the structure of Branch and Bound methods, together with a review of various worst case testing methods is given. Our main contribution to this group of techniques is the introduction of a geometrically based worst case testing method called INDENTATION. The INDENTATION method is based on a discrete representation of the region of acceptability, obtained by a regionalization /37/

[α] Solutions which fail to meet the 100% yield requirement.

Of the input space. As with other geometrical methods regionalization and therefore INDENTATION becomes prohibitively expensive as the dimensionality becomes large.

In chapter three the results of the application of the INDENTATION method in conjunction with a particular search strategy called the bisectional search, are presented for a three variable circuit.

Chapter four deals with design centering methods based on Monte Carlo analysis. As Monte Carlo analysis does not provide gradients of the yield function, attention is confined to direct search methods of optimization. Initially, a previously reported method, Pattern search, is briefly reviewed. The main original contribution is the introduction and development of a novel technique, called the statistical exploration method (abbreviated MYOSE).
For selecting new trial solutions, MYOSE uses information about the position of passing and failing circuits, provided by Monte Carlo analysis performed for the current iterate. The procedures for selecting the direction of search and the size of the step in this direction are described and discussed. The effectiveness of the MYOSE method is demonstrated with results obtained for a number of circuit examples. The largest circuit example tested involves 43 variable components.

The dependence of the accuracy of a yield estimate on sample size was discussed in chapter one. In chapter four it is argued that in an iterative method of yield maximization

(design centering) it is of greater importance to correctly rank yield estimates than to attain high accuracy for individual yield estimates. The relationship between sample size and degree of confidence of correct ranking is discussed. Two sampling schemes which for small sample sizes return a high degree of confidence are described. The first scheme, correlated sampling uses the same random numbers for successive iterates. This decreases the variance of the estimate of the difference in the yields of successive iterates. Thus for a particular sample size the confidence of correct ranking is increased.

The second scheme, the Common Points scheme, reuses, for the current iteration, some of the circuit analyses performed for the Monte Carlo analysis of the previous iterations. The tolerance regions of successive iterations overlap considerably. The scheme makes use of the fact that the contribution to yield of the overlapping part of the tolerance region does not need to be re-evaluated. Whereas the correlated sampling scheme is useful for any form of component p.d.f., the common points scheme is only applicable for the case of uniform p.d.fs. Later in the chapter we provide a comparison of the two schemes for a particular circuit example, when component p.d.fs are assumed to be uniform. This particular example indicates a greater efficiency of the common points scheme over the correlated sampling scheme.

As with other direct search methods /55/ no general results for the convergence properties of the Statistical Exploration method are given. In

addition we are unable to derive conditions for yield maxima. In practice application of the algorithm to various circuit examples leads to increases in yield for several iterations. The number of iterations required has been from about five to nine. For the circuit examples tested, the number of iterations appears to be independent of dimensionality (see table 4.9).

Chapter five considers methods of tolerance assignment based on Monte Carlo analysis. The group of methods considered commences with wide tolerances and low associated yield. Yield is estimated by Monte Carlo analysis. New tolerances are selected via algorithms which use information about the distribution of the component values of the pass and the fail circuits. The particular algorithms for selecting new tolerances distinguishes one method in this class from another.

Monte Carlo analysis is performed with the new set of tolerances and the process is continued. At each iteration tolerances are tightened over those of the previous iteration. The procedure can be continued over a number of iterations until 100% yield is achieved. Alternately the procedure may be continued until a cost function is minimized.

We commence the chapter with discussion of a relevant cost function reflecting the trade-off between yield and tolerance. The efficacy of the iterative scheme for minimizing such a function is discussed. An existing method, TOLERATE is reviewed. The mathematical arguments in support of the TOLERATE algorithm are

are clarified. In particular the parameter, yield sensitivity which is intended to be a measure of a component's effect on yield, is shown to be unreliable.

A serious shortcoming of the TOLERATE method is that of overdesign. To overcome the practical ambiguities and overdesign, the PERTOL method is introduced. The mathematical arguments for the PERTOL tolerance assignment criterion are explained. Comparative results of the application of both methods to specific circuit examples are shown. PERTOL is found to provide lower cost solutions than TOLERATE in every case.

6.3 SUGGESTIONS FOR FURTHER RESEARCH

Suggestions for future research are presented in two groups. The first group relates to improvements and extensions to algorithms and techniques discussed in this thesis. The second group considers the extension of the concepts and ideas developed, to other problems within the field of statistical design.

6.3.1 EXTENSIONS TO TECHNIQUES DEVELOPED IN THE THESIS

6.3.1(a) A technique for further increasing the computational efficienty of Monte Carlo based design centering methods (Chapter 4) is proposed. The method to be employed in conjunction with the correlated sampling scheme is based on the use of Taylor series approximation of the circuit response.

We denote by $f(P^o)$ a particular circuit response. Here $P^o = p_1^o\, p_2^o \ldots\ldots p_K^o$ represents a set of values for the K component parameters. The value of the response for another set of values $P' = P^o + \Delta P$ may be written in terms of a Taylor series expansion /11/ as:

$$f(P^o+\Delta P) = f(P^o) + \sum_{i=1}^{K} S^f_{p_i} \frac{\Delta p_i}{p_i} + \frac{1}{2!} \sum_{i=1}^{K} \sum_{j=1}^{K} S^f_{p_i} S^f_{p_i} \frac{\Delta p_i}{p_i} \frac{\Delta p_j}{p_j}$$

$$+ \ldots\ldots\ldots\ldots\ldots \qquad (6.1)$$

Where $S^f_{x_i}$ etc. are the first, second and higher order sensitivities of the response f(.).

A full circuit analysis and the required sensitivities are computed at point P^o. The response at any other point P' can then be estimated using a suitably truncated version of series (6.1). The advantage of this method is that the computational cost of evaluating sensitivities and the Taylor series approximation is in general far less than that of re-evaluating the circuit response for P'.

Expression (6.1) is an infinite series. However, in practice it has to be truncated after a certain number of terms. The conditions to be satisfied for (6.1) to converge and the dependence of accuracy on the point of truncation are discussed by Sud /56/. Sud has also described a scheme for using the Taylor series to perform Monte Carlo analysis /57/. In

any investigation of our proposed scheme, the results obtained by Sud are of interest. Therefore his scheme for performing Monte Carlo analysis using Taylor series approximations is summarized here.

Scheme 1 (Sud/57/).

1. Perform a full circuit analysis for the nominal point (design center) P^o. Calculate the sensitivities of the circuit response with respect to the component parameters.

2. Set counter j=1.

3. Generate random sample P_j. Points are generated according to the relevant probability density function $\emptyset(.)$.

4. Estimate values for circuit responses at point P_j, by use of the truncated Taylor series.

5. Store results.

6. Increment counter j=j+1. Stop if j is greater than the maximum number of sample circuits to be analysed. Otherwise go to step 3.

The main shortcoming of this method of Monte Carlo analysis is that of lack of accuracy. For a particular number of terms the approximation becomes less accurate as the deviation from nominal of individual parameter values increases. Therefore the use of the Taylor series for Monte Carlo analysis is less reliable when the parameters are subject to large tolerances. The limitations imposed by accuracy will be less stringent

when the approximation is employed for correlated sampling. This will be so because corresponding sample points of successive iterates will be in close proximity in parameter space.

Consider figure 6.1 which illustrates the relationship between the tolerance regions and sample points of successive iterates in design centering. Initially let the iterates of interest be 1 and 2, with design centers P_1^o and P_2^o respectively. The sample points for the two iterations are denoted as $P_{11}\ P_{12}\ \ldots\ P_{1N}$ and $P_{21}\ P_{22}\ \ldots\ P_{2N}$ respectively. The two design centers are related according to (6.2):

$$P_2^o = P_1^o + \Delta P_1 \qquad 6.2,$$

where we denote $\Delta P_1 = \Delta p_{11}\ \Delta p_{12}\ \ldots\ \Delta p_{1K}$.

It is shown in section 4.4.2 that correlated sampling ensures that sample points will be related in a similar manner i.e.

$$P_{2_j} = P_{1_j} + \Delta P_1 \qquad j=1\ldots N \qquad 6.3$$

Our proposed scheme is as follows:

Scheme 2

1. Perform a full Monte Carlo analysis with design center P_1^o. That is, perform circuit analysis for the N random sample points $P_{11}\ P_{12}\ \ldots\ P_{1N}$. In addition evaluate and store relevant sensitivities of the various responses with respect to the component values, for each of the N sample circuits.

3. Perform a modified Monte Carlo analysis:

   (i) Generate the new sample points according to expression 6.3, i.e. perform correlated sampling.

   (ii) Approximate circuit response for the new points $p_{2=}$ .... p_{2N}, by use of the Taylor series.[α]

Implementation of steps 2 and 3 in the iterative scheme summarized in section 4.4.2(f), will result in considerable computational savings.

Scheme 2 as described here only extends to the second iteration. When a new design center is chosen after iteration 2, i.e. $P_3^o = P_2^o + \Delta P_2$, then the response of the new sample points may still be approximated in terms of the response and sensitivities of the sample points of iteration number 1. Alternatively, we may now perform full circuit analyses and sensitivity calculations and use these to approximate the sample points for the fourth iteration.

A general scheme is envisaged where, after each new choice of design center, a decision is made as to whether full circuit analyses are to be performed, or the approximation is to be employed. The accuracy of the approximation becomes poorer with increasing deviation of component values. However, the deviations Δp_1 Δp_2 .... Δp_K will in general be much smaller than the tolerances of the component parameters.

[α] No specific suggestions are made about the point of truncation of the Taylor series. This question has been investigated by Sud /56/ and also by Karafin/ 3/. For certain tolerancing algorithms Karafin has suggested the use of all first order sensitivities and unmixed second order sensitivities.

6.3.1 (b) The scheme proposed in 6.3.1 (a), improves efficiency by approximating circuit responses for some of the Monte Carlo iterations. However, for the situation where full circuit analyses are to be performed, we suggest an investigation of the following enhancements.

For acceptability, a circuit has to meet a number of performance requirements.

Notationally:

$$\underline{f}_1 \leq f_1(.) \leq \overline{f}_1$$
$$\vdots$$
$$\underline{f}_M \leq f_M(.) \leq \overline{f}_M$$

As before $f_i(.)$ is the ith circuit response and $\underline{f}_i$ and $\overline{f}_i$ are the limits of acceptability of $f_i(.)$.

Failure to comply with anyone of the M performance requirements renders the circuit to be a fail. While performing Monte Carlo analysis the performance functions are evaluated sequentially for each sample point. One enhancement already implemented is to terminate performance evaluation when the first failure to comply with a performance requirement occurs. Further improvement will be effected if the order of evaluation of the circuit responses is changed. The new order would be such that the responses most likely to fail were evaluated first.

In one possible scheme an arbitrary testing order is assumed for the first iteration of the Monte Carlo analysis. The frequency of failure of each of the performance constraints is evaluated by counting. The order of testing for the second

iteration is selected such that the most frequently failing performance is tested first and the least frequently failing performance is tested last.

The 43 variable digital filter circuit (chapter 4) was subject to 256 performance constraints (i.e. the insertion loss at 256 frequencies was tested). For each analysis the computational cost was proportional to the number of frequencies tested. Whereas a passing circuit had to be tested for all 256 frequencies, a failing point only needed to be tested uptil the first failing frequency. Typically the failure rate was 70%. Therefore it is clear that considerable savings in computational effort could be effected by re-ordering the test frequencies.

6.3.1 (c) For design centering, two sampling schemes, viz. correlated sampling and the common points schemes were discussed. For a particular sample size, correlated sampling reduces the variance of the estimate of yield difference between different iterates. The common points scheme on the other hand achieves computational savings by re-using some of the circuit analyses of the previous iterate. In chapter four the results of a practical comparison of the application of the two sampling schemes to a particular circuit example are discussed. The results support the conjecture that the common points scheme is more efficient.

We suggest that a more rigorous theoretical and experimental comparison of the two schemes be made. Such a comparison would be of particular value as the schemes have application beyond

the problems of statistical circuit design. For example correlated sampling is extensively used in simulation /47/, particularily in the design and evaluation of systems subject to statistical variations.

6.3.2 EXTENSION OF THE MONTE CARLO BASED DESIGN APPROACH TO OTHER PROBLEMS IN THE FIELD OF STATISTICAL DESIGN

In this thesis methods of design centering and tolerance assignment based on Monte Carlo analysis have been introduced. Previously Monte Carlo analysis has been used purely for analysis. For particular nominals, tolerances and component parameter distributions, the Monte Carlo method is used to estimate parameters such as yield. The design methods discussed in chapters four and five iterate the process. New nominals and tolerances are selected via algorithms which make use of the spatial information provided by the Monte Carlo analysis.

Our methods have several important advantages. Firstly, they can deal with circuits involving a large number of toleranced components. Secondly the methods are easy to implement using existing circuit analysis routines. Finally they do not require simplifying assumptions about the form of the component or performance p.d.f.s or about the shape of the region of acceptability (e.g. convexity). We therefore propose extension of our approach to other design problems as discussed below.

Although the methods discussed are not limited by the nature of the circuit being designed, only discrete component circuits have been investigated. The extension of the approach to

integrated circuits requires a consideration of other statistical design problems which may be of relevance.

6.3.2 (a) In discrete circuits, tolerances can be imposed on any batch of a component by removing out of tolerance components. In integrated circuits individual components cannot be sorted. Tolerance assignment is nevertheless of importance in integrated circuit design. For example the value of an integrated resistor is determined by its aspect ratio (length/width). The tolerance on its resistance value depends on the width. If the width is increased and the length is also increased to maintain a certain aspect ratio, then the nominal value of the resistor remains constant while its tolerance decreases.

In addition to tolerance assignment, it is of importance to consider correlation between component spreads. For example the detrimental effect of large resistor spreads may be reduced by designing circuit performance to depend on ratio of resistance values. The correlation between resistors can then be increased by placing them adjacently on the I.C. chip.

One particular design problem is that of identifying the desirability of tracking between component parameters. The terms correlation assignment /15/ has been suggested for this design problem. Consider the situation where an electrical topology and nominal values have been suggested for a circuit which is to be manufactured as an integrated circuit. Then it is useful to identify desirable tracking between parameters. One possible method of doing this would be the following.

Perform Monte Carlo analysis assuming uniform p.d.f. s for the component parameters. Identify the random sample circuits as pass or fail (according to performance requirements). Then knowledge of desirable tracking may be obtained by estimating the correlation between component values for the pass circuits. Similarily undesirable tracking may be identified by considering the correlation of component values of the fail circuits. Such analyses would give the designer information which would be useful in the geometrical layout of the circuit, or in making changes to the electrical specifications of the design.

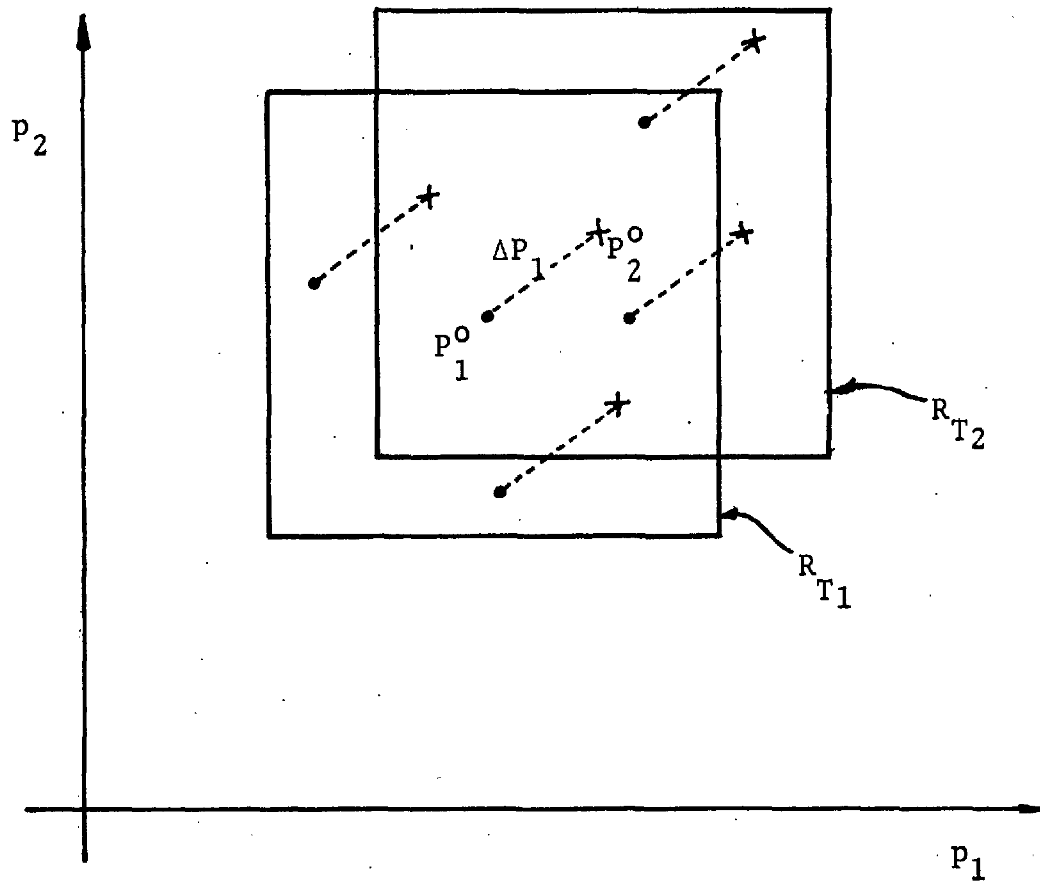
The effectiveness of different layouts and electrical designs could then be evaluated by performing further Monte Carlo analyses, taking the correlations into account.

6.3.2(b) Monte Carlo based methods would be useful for specifying tests on manufactured circuits. The Monte Carlo analysis provides information about the correlation between different aspects of a circuit's electrical characteristics. This may be used to simplify and reduce the cost of testing. For example in the manufacture of linear integrated circuits, it is more expensive to perform a.c. tests than d.c. tests. For final acceptability a circuit has to meet certain a.c. performance requirements. It is desirable to identify and remove failing circuits after the d.c. tests.

Monte Carlo analysis can be used for evaluating the correlation between d.c. and a.c. behaviour. On the basis of this, limits may be imposed on acceptable d.c. behaviour. By imposing

suitable limits the number of bad circuits passed on for a.c. testing will be reduced. However, some good circuits will be rejected after d.c. testing. The designer may estimate the proportion of circuits which pass particular d.c. test limits and fail a.c. tests or those which fail the d.c. test limits but would have gone on to pass a.c. tests. The effect on these proportions of different d.c. test limits may be investigated by Monte Carlo analysis. Suitable test limits can then be chosen to minimize overall costs of testing.

The particular problem can be seen to be closely related to the tolerance assignment problem / 2 /. Therefore some of the techniques and ideas discussed in chapter five may be applied.



Note : • Represents Sample Points Associated With Design Center P_1^o.

x Represents Sample Points Associated With Design Center P_2^o

Figure 6.1 : Diagram Showing The Relationship Between Corresponding Points Of Successive Iterates.

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