A $\mu$-Controller-based system for interfacing selector-less RRAM crossbar arrays

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Abstract—Selector-less crossbar arrays of resistive random access memory (RRAM), also known as memristors, conduct large sneak currents during operation which can significantly corrupt the accuracy of cross-point analogue resistance ($M_t$) measurements. In order to mitigate this issue we have designed, built and tested a ‘memristor Characterisation And Testing’ (mCAT) instrument that forces redistribution of sneak currents within the crossbar array, dramatically increasing $M_t$ measurement accuracy. We calibrated the mCAT using a custom-made 32x32 discrete resistive cross-bar array and subsequently demonstrated its functionality on solid-state TiO$_2$-RRAM arrays, on wafer and packaged, of the same size. Our platform can measure stand-alone $M_t$ in the range of 1 k$\Omega$ to 1 M$\Omega$ with less than 1% error. For our custom resistive crossbar, 90% of devices of the same resistance range were measured with less than 10% error.

Index Terms—Crossbars, RRAM, memristors, sneak paths.

I. INTRODUCTION

Compact and fast memory storage elements are becoming increasingly important under the advent of mobile computing, cloud storage and big data. With current NAND-type flash memory quickly approaching its scalability limit, a shift towards ionic-based memories is ascertained with resistive random-access memory (RRAM) being the main candidate for a post-NAND market. RRAM cells, also known as memristors [1]–[3], have already been shown to excel in storage element size [4], write power [5], and information compactness, with many of the benefits of RRAM technologies result from the functionality on solid-state TiO$_2$-RRAM arrays, on wafer and packaged, of the same size. Our platform can measure stand-alone $M_t$ in the range of 1 k$\Omega$ to 1 M$\Omega$ with less than 1% error.

In this work, we focus our efforts towards this issue and present a multi-port technique for reading accurate analogue cross-point resistance values from devices within a planar, selector-less crossbar array - a markedly stricter criterion than achieving a good digital read margin. We implement the non-intrusive reading and writing techniques on a desktop PCB which facilitates quick acquisition of data of RRAM cells in a 32x32 crossbar array configuration via a user-friendly graphical user interface (GUI) on a local PC. More specifically, in Section II we introduce the theoretical background of our approach. Section III describes the practical implementation of our ‘memristor Characterisation And Testing’ (mCAT) system. Experimental results from a reference resistive crossbar array and an equal size solid-state RRAM array are presented in section IV. Finally, section V considers the benefits and limitations of the current system, as well as offering insights into the scaling up performance of the mCAT and direction of future efforts.

Fig. 1. a) Sneak path/sneak current problem in cross-bar arrays. Application of a bias reading voltage on active word- and bit-lines causes disruptive currents to flow in neighbouring cells. b) Low-density solution for sneak-path limiting involving transistor based selectors ‘S’.
A crucial characteristic of the proposed read-out scheme is the fact that $V_{\text{inactive}}$ has to be derived from $V_{\text{bias}}$ (e.g. by buffering) so as to allow separation between the currents flowing through $M_{\text{target}}$ and the rest of the array and is accuracy-critical. The criticality occurs from the worst-case scenario whereby the target is in very high resistive state and the lumped component $M_w$ consists entirely of memory cells in very low resistive states, thereby forming a very low impedance path between $V_{\text{bias}}$ and $V_{\text{inactive}}$. Even small offsets in the generation of $V_{\text{inactive}}$ from $V_{\text{bias}}$ can lead to significant amounts of current being diverted through $M_w$ hence corrupting our estimate of the target state.

C. Write operation

RRAM cells are usually characterised by a voltage switching threshold ($V_{\text{thr}}$) under which no applied potential can disturb it’s resistive state [17]. We utilise this feature in our write scheme by applying half of the active device’s write voltage ($V_{\text{write}}$) to all inactive lines as illustrated in Figure 2(d). Provided that $V_{\text{write}} > V_{\text{thr}}$ and $V_{\text{write}}/2 < V_{\text{thr}}$ then the risk of accidentally programming adjacent devices when writing only on $M_{\text{target}}$ is minimised. We note that the write operation is not accuracy-critical, i.e. small variations in $V_{\text{inactive}}$ do not significantly perturb the write operation.

III. SYSTEM IMPLEMENTATION

To demonstrate these ideas and to facilitate practical RRAM characterisation, a full system has been implemented on PCB. A photograph of the set-up is shown in Figure 3(a) with it’s corresponding simplified schematic diagram in 3(b). The key components of this platform are:

- An mBED LPC1768 microcontroller which contains the following functionalities:
  - serial communication with a local PC;
  - 5 x 12-bit ADCs and one 10-bit DAC on board.
  - 20 digital 10 ns transition i/o pins;
- A 'Bias generator’ consisting of a voltage feedback op-amp in a subtractor configuration which maps the output of the mBED DAC from $0 \rightarrow 3.3 \text{ V} \rightarrow -10.9 \text{ V} \rightarrow 10.9 \text{ V}$ at $V_{\text{OUT}}$.
- A sense resistor bank allowing connection of the bias generator to the cross-bar array via different sense resistors or a resistorless, by-pass path.
- A feedback buffer copying the voltage on the active word-line ($V_{\text{bias}}$ to $V_{\text{inactive}}$ during ‘read’ operation).
- A feedback amplifier block applying half the voltage on the active word-line ($V_{\text{bias}}$ to $V_{\text{inactive}}$ during ‘write’ operation).
- Two analogue multiplexer banks allowing access to the word- and bit-lines of the crossbar array.
- A variety of ‘housekeeping’ systems (power management, multiplexer controllers).
A. Read operation

Assuming all switches are open in idle mode, and $V_{OUT} = 0\,\text{V}$, the operation proceeds as follows: first the target device is selected by connecting the corresponding (active) wordline to the $V_{bias}$ node and the respective bitline to GND. The inactive word- and bit- lines are shorted together and connected to the output of the ‘read’ feedback buffer. Then, the mBED sets its DAC to facilitate $V_{OUT}=0.5\,\text{V}$ (default value but programmable) and subsequently switches the $1\,\text{M}\Omega$ sense resistor in (closes S1). This provides a DC bias to the bootstrapping feedback buffer input which henceforth constantly performs its bootstrapping function on the inactive crossbar lines. The mBED then takes a reading of $V_{OUT}=V_{read}$ via ADC1 by closing switch $S_r$, and a reading of $V_{bias}$ via ADC2 by closing the switch $S_b$. Typically 50 measurements taken at full reading rate are averaged as a compromise between speed and noise rejection. The estimates of $V_{bias}$ and $V_{read}$ along with the value of the first sense resistor used yield enough information for a first calculation of the target memristance $M_{S1}$. Time delays are introduced to ensure voltage readings are performed after all nodes have settled.

Next, the $1\,\text{M}\Omega$ is switched out, the $300\,\text{k}\Omega$ resistor is switched in (S1 open, S2 close), and the previous procedure of measuring $V_{bias}$ and $V_{read}$ is repeated yielding a new candidate value of memristance $M_{S2}$. This sequence is repeated for all sense resistors producing five different values $M_{S1-S5}$ for the resistance of the target device, each one corresponding to its respective sense resistor utilised $R_{S1-S5}$. These are recorded by the mBED.

Finally, from all calculated $M_{S1-S5}$, a single value $M_{S1}$ is chosen in software as the final read value of memristance, where $i$ is the index at which $\frac{M_{Si}-R_{Si}}{R_{Si}}$ is minimised. This ensures that a reading is taken at the point where $\frac{\partial V_{bias}}{\partial M_{target}}$ is maximised allowing for a minimal $\delta M$ change that will produce a 1 LSB shift in voltage at the input of ADC1. To prove this we note that from Figure 2c:

$$V_{bias} = \frac{V_{read} \cdot M_{target}}{M_{target} + R_{sense}}$$  \hspace{1cm} (1)

$$\frac{\partial V_{bias}}{\partial M_{target}} = \frac{V_{read} \cdot R_{sense}}{(M_{target} + R_{sense})^2}$$ \hspace{1cm} (2)

$$\frac{\partial^2 V_{bias}}{\partial M_{target} \partial R_{sense}} = \frac{V_{read}(M_{target} - R_{sense})}{(M_{target} + R_{sense})^3}$$ \hspace{1cm} (3)

where (2) expresses the sensitivity of our measurement node voltage $V_{bias}$ to differences in the value of $M_{target}$ (measurement sensitivity) and (3) expresses the sensitivity of the measurement sensitivity on the value of the sensing resistor used. Hence the maximum sensitivity for given $M_{target}$ and $V_{read}$ is reached when $M_{target} = R_{sense}$.

B. Write operation

With initially all switches open, the ‘write’ operation proceeds as follows: first the target device is selected and the output voltage $V_{OUT}=V_{write}$ is set to the desired value. Mode switches are set to ‘write’. Subsequently, the by-pass switch ($S_w$) is flash closed for the desired pulse width duration. Whilst the active device is being subjected to the $V_{write}$ voltage all inactive devices are fed $V_{write}/2$ via the bootstrap amplifier. Instead of using one feedback amplifier, the physical implementation of our system employs a bank of two pairs of amplifiers (one for word-line and one for bit-lines) that facilitates the use of different gain settings for word- and bit-lines for testing purposes.

C. Control Interface

The mCAT is controlled by a host PC via a serial connection through a custom MATLAB GUI which allows quick control and data acquisition. The full measuring system involves the simultaneous operation of software on the mCAT level (mBED...
programmed in C) and GUI level (MATLAB). High level functionality, such as: a) array-level operations (e.g., whole array programming or measurement), b) complicated single-device operations (e.g., setting to specific resistive state as per [18], [19], c) instrument calibration and d) data display, are handled by the MATLAB layer. Lower level functionality such as the mechanics behind device targeting, biasing and reading is directly implemented in the C layer.

IV. EXPERIMENTAL RESULTS

The mCAT is capable of self-calibration which ensures the effects of any hardware drifts and offsets are minimised in the C layer. Initially, the reading accuracy was assessed as a sanity check by measuring single discrete resistors, spanning 5 decades, connected across arbitrary inputs, and comparing the results with a high-end multimeter. Figure 4 shows minimal mean read errors and excellent precision for stand-alone device measurement, without the intrusive effects of sneak-paths.

A 32x32 resistor crossbar array with SMD resistors was manufactured (Figure 5a) in order to measure the accuracy of the read operation. A limited range of resistor was utilised (1 kΩ, 5.6 kΩ, 10 kΩ, 56 kΩ, 100 kΩ, 560 kΩ and 1 MΩ) with the color map of the position of each resistor on the array displayed in Figure 5b. The configuration was chosen such as to provide high stress conditions (high resistance elements sharing word or bit-lines with many low resistance elements) which are more likely to disrupt the correct reading of the target resistor and such test the limitations of our system. After reading the full array, an extra scaling step is performed, described by (11) in appendix, which is meant to increase the accuracy of each cross-point resistance estimation. Results of the full crossbar reading are illustrated in Figure 5c and d. The mCAT can thus measure 90% of the resistors on our standard testing crossbar with less than 10% reading error. It is clear from Figure 5d that high resistance have larger reading errors than low resistance devices. This is due to the influence of $M_{\text{act}}$ and the voltage offset of the read feedback buffer ($V_{\text{os}}$) used to isolate $V_{\text{inactive}}$ from $V_{\text{bias}}$ as illustrated in Figure 2c. Other sources of error in the system will be caused by a complex combination of effects from $V_{\text{os}}$, $M_{\text{ur}}$, $M_{\text{db}}$, $R_{\text{sense}}$ and the non-zero resistance of analogue switches, listed in appendix.

Several 32x32 TiO$_{2-x}$ (x=0.06 as measured by X-ray photoemission spectroscopy (XPS)) solid-state RRAM crossbars were further measured by this setup. The following results depicted in Figure 6 were obtained from 2x2 µm$^2$ cross-bar devices with the stack Ti/Pt/TiO$_{2-x}$/Pt (5/10/25/10 nm), diced in individual crossbars and packaged in standard DIP PLCC68 compatible with the mCAT setup. Figure 7 shows measurements attained from 30x30 µm$^2$ cross-bar devices accessed directly on wafer, with the stack: Cr/Pt/TiO$_{2-x}$/Pt (3/5/25/4 nm).

Each device in the crossbar can be individually selected and have any pulsing sequence applied to, with reading operations being performed in between each programming pulse. A pulsing sequence recorded for one device is illustrated in Figure 6a showing resistance modulation in between four different intermediate states. The full 32x32 array was measured before and after the application of this pulsing scheme and the distribution of the normalised resistance difference between the two iterations, excluding the target device, is plotted in the inset of Figure 6a. The resistance differences are within the noise floor and as such the inset shows minimal disturbance to inactive devices during programming of a single RRAM cell.

Furthermore, the mCAT can be linked via external connectors located around the package holder to an external 64 pin probe-card which facilitates interfacing on 32x32 crossbars directly on wafer (Figure 6d). A full array read
resistive state lower than 0 to 8 V in 0.25 V steps, with the goal of switching to a subjected to a positive pulse train of 10ms width and amplitude distribution of read states in Figure 7b. Each device was then via the feedback buffer to the active bitline access MUX switch be utilised (Figure 2c). On the other hand, M and the inactive bit (M) provides current via the feedback buffer with zero-offset and a FET input stage must remain similar for larger scale arrays. This is due to the lumped components M and M becoming increasingly more conductive. Interestingly, Roff/Ron ratios have a profound effect only on small array sizes, while the reading accuracy variations resistance, lifting the ground potential (Figure 9). Another limitation is represented by the minimum programming pulse width which is restricted by the speed of the ‘Bias Generator’ op-amp (Figure 3b), parasitic impedance on the active signal line, and the mBED clock. As such, the non-zero resistance of the analogue switches, along with the finite offset of the read feedback buffer play a major role in the estimation of the target device resistance, and have been quantified in the model listed in the appendix.

This circuit model was further utilised to analyse the degradation of reading accuracy when using the mCAT to access larger crossbars and under several Roff/Ron (boundary resistive states of ideal RRAM cells) conditions. As mentioned before, the worst case scenario (largest reading errors) occurs when all devices on the active word- and bit-line (except the target device Mtarget) are equal to Ron, yielding low impedance Mw and Mb. Provided Mtarget can ideally vary in between Ron and Roff then the voltage read by the mBED ADC1 will vary monotonically in between two corresponding boundary cases. The difference in voltages read by the mBED in between these two cases represents a reading voltage margin from which the ADC1 can distinguish a number of different states based on its finite resolution (for the onboard mBED ADC1 - 1LSB ≈ 3.3mV). We utilise this figure of merit (reading bit accuracy) to quantify the performance of our simulated mCAT for larger scale arrays (Figure 8).

It is evident that the bit reading accuracy drops significantly with increasing crossbar array size. This is due to the lumped components Mw and Mb becoming increasingly more conductive. Interestingly, Roff/Ron ratios have a profound effect only on small array sizes, while the reading accuracy variations remain similar for larger scale arrays. This is most likely due to ”Roff” measured voltages becoming saturated, or decreasing
very little with larger arrays and larger $R_{\text{off}}$.

In the case where the system should only distinguish bistable (binary or 1 bit accuracy) RRAM cells which toggle between dissimilar $R_{\text{on}}$ and $R_{\text{off}}$ resistive states, the reading limitations relax dramatically, as illustrated in Figure 8c. Depending on the $R_{\text{off}}/R_{\text{on}}$ ratio, the mCAT is estimated to be capable of measuring binary RRAM chips of up to 3200x3200 (or $\approx 10$ Mb) crossbar size.

VI. CONCLUSION

The mCAT is a low-cost, versatile platform for measuring and programming of RRAM cells as single devices, or more importantly in a 32x32 crossbar array configuration. The reading and programming schemes ensure that each cross-point resistance can be isolated from adjacent devices by active sneak-path current redistribution. For reading analogue values of resistance, our platform is capable of measuring stand-alone resistive cells in the range of 100$\Omega$ to 10M$\Omega$ with less than 5% error and excellent precision ($\sigma < 3\%$). In our custom discrete resistor crossbar array, designed to simulate high stress conditions (low impedance sneak paths), 90% of devices in 1k$\Omega$ to 1M$\Omega$ range were measured with less than 10% error. Hence our particular reading technique allows for reading with multiple bit accuracy of cross-point cells. While interfacing with solid-state RRAM cells, applying programming pulses exerts halved interference on remaining inactive devices, minimising the risk of accidentally modulating their resistive states.

The platform’s versatility is promoted by the use of a NXP mBED microcontroller which controls the adjacent mixed-signal circuitry. The mCAT is controlled via a MATLAB GUI which allows seamless interaction with 32x32 RRAM crossbar arrays, packaged or directly on wafer via a custom probe-card. The latter method speeds up the process of mass testing of RRAM crossbars by accessing the devices without the need for dicing and packaging of individual dies.

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APPENDIX

In order to improve the accuracy of the reading method, the ideal circuit which is formed when the mCAT is in the ‘read’ mode is extended to include the effects of the non-zero resistance of the analogue switches employed and the offset voltage of the ‘read’ feedback buffer (Figure 9b). Solving for $M_t$, the real resistance of the target device, reveals:

$$V_{\text{read}} - V_e = \frac{M_t^2}{M_t^2 + M_t B + C} + \frac{M_t B}{M_t D + M_t E + F}$$

where:

$$A = R_{\text{sense}} [V_{\text{read}} R_{\text{out}} - V_{\text{os}} (M_b + R_x)]$$

$$B = R_{\text{sense}} [2V_{\text{read}} R_{\text{out}} - V_{\text{os}} (M_b + 2R_x)]$$

$$C = R_{\text{sense}} [(M_w + M_b) V_{\text{read}} M_w M_b + (M_w + M_b) (V_{\text{read}} R_{\text{out}} - V_{\text{os}} R_x)]$$

$$D = R_{\text{out}} (M_w + 2R_x + M_b + R_{\text{sense}}) + (R_x + M_b) (R_x + M_w)$$

$$E = M_w M_b (R_{\text{sense}} + M_w + 2R_x + M_b) + (M_w + M_b) R_{\text{out}} (2R_{\text{sense}} + M_w + 4R_x + M_b) + R_x (2R_x + 2R_{\text{out}} + M_w + M_b)$$


\[
F = (M_w + M_b) \left\{ (R_{\text{sense}} + 2R_x) [M_wM_b + R_{\text{out}} (M_w + M_b)] + (M_w + M_b) R_x^2 \right\} \tag{10}
\]

Rearranging (4) gives two solutions for \( M_{1,2} \), from which we chose the positive value as the final measured value of memristance.

\[
M_{1,2} = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} \tag{11}
\]

where:

\[
a = (V_{\text{read}} - V_x - V_e)D - A \tag{12}
\]

\[
b = (V_{\text{read}} - V_x - V_e)E - B \tag{13}
\]

\[
c = (V_{\text{read}} - V_x)F - C \tag{14}
\]

The full solution for \( M \) therefore has 8 parameters: \( V_{\text{read}}, V_x, V_{\text{ao}}, R_{\text{sense}}, R_x, R_{\text{out}}, M_w, \) and \( M_b \). \( V_{\text{read}} \) is chosen to be low in order not to disrupt the state of the target device whilst measuring (0.5V in our case), \( R_x \) is the typical series resistance of the analogue switches in the circuit, \( V_{\text{ao}} \) is the offset voltage of the ‘read’ feedback buffer (median value) and \( R_{\text{out}} \) is the output resistance of the same buffer, which was utilized as a fitting parameter. Our measuring technique for the full 32x32 crossbar involves the following steps which aim to estimate the remaining parameters (\( V_x, M_w, M_b \) and \( R_{\text{sense}} \)):

1. Perform a standard reading technique (as described in Section IIIa) on the full array and store the results in a 32x32 matrix locally. Record the value for \( V_x \) and \( R_{\text{sense}} \) for each word and bit-line.
2. Compute estimates for \( M_b \) for each word and bit-line from the stored matrix of memristance values from the previous step.
3. Measure \( M_w \) values for the full array. In a standard target device read, the device selection is performed by configuring the MUX bank so that the active word line is connected to the bias generator, the active bit line to GND and the rest of the lines shorted together to the read feedback buffer. To measure \( M_w \), the bit-line MUXs address bit string is inverted so that all inactive lines are grounded, and the ‘active’ bit-line (the one who’s corresponding \( M_w \) is being measured) is connected to the ‘read’ feedback buffer. As such, a reading operation performed in this configuration will give an estimate of \( M_w \) - the parallel combination of all devices on the active word-line, without the target device. These values are recorded for all word and bit-line addresses.
4. All parameters have been estimated and \( M \) is computed via our model.

REFERENCES


