A μ-Controller-based system for interfacing selector-less RRAM crossbar arrays

Radu Berdan[†], Alexander Serb[*], Ali Khiat[*], Anna Regoutz[*], Christos Papavassiliou[†], Themis Prodromakis[*]
[*]Electronics & Computer Science dept., Nano group, University of Southampton, Southampton, UK.
[†] Electronic and Electrical Eng. dept, Circuits and Systems group, Imperial College London, London, UK.

***Abstract*—Selector-less crossbar arrays of resistive random access memory (RRAM), also known as memristors, conduct large sneak currents during operation which can significantly corrupt the accuracy of cross-point analogue resistance (M_t) measurements. In order to mitigate this issue we have designed, built and tested a 'memristor Characterisation And Testing' (mCAT) instrument that forces redistribution of sneak currents within the crossbar array, dramatically increasing M_t measurement accuracy. We calibrated the mCAT using a custom-made 32x32 discrete resistive cross-bar array and subsequently demonstrated its functionality on solid-state TiO_{2-x} RRAM arrays, on wafer and packaged, of the same size. Our platform can measure stand-alone M_t in the range of $1\,k\Omega$ to $1\,M\Omega$ with less than 1% error. For our custom resistive crossbar, 90% of devices of the same resistance range were measured with less than 10% error.**

***Index Terms*—Crossbars, RRAM, memristors, sneak paths.**

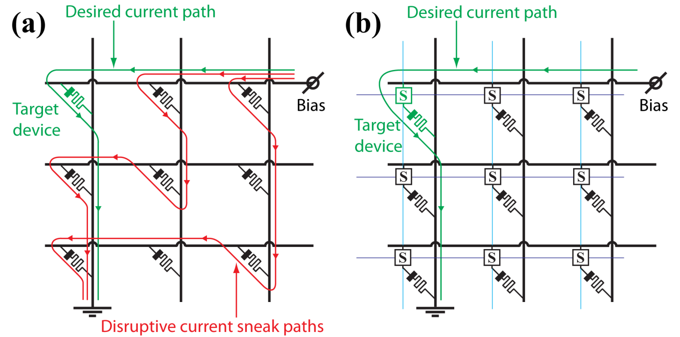

Fig. 1. a) Sneak path/sneak current problem in cross-bar arrays. Application of a bias reading voltage on active word- and bit-lines causes disruptive currents to flow in neighbouring cells. b) Low-density solution for sneak-path limiting involving transistor based selectors 'S'.

I. Introduction

Compact and fast memory storage elements are becoming increasingly important under the advent of mobile computing, cloud storage and big data. With current NAND-type flash memory quickly approaching its scalability limit, a shift towards ionic-based memories is ascertained with resistive random-access memory (RRAM) being the main candidate for a post-NAND market. RRAM cells, also known as memristors [1]–[3], have already been shown to excel in storage element size [4], write power [5], and information compactness, with the ability to store multiple bits per memory element [6], [7].

Many of the benefits of RRAM technologies result from the small size of the storage nodes it utilises, achieving densities of down to $4F^2$ (F - feature size) per element for planar arrays and even below for 3D arrays [8]. Achieving $4F^2$ density involves arranging the RRAM elements in a crossbar configuration. These can be either RRAM only [9], or post-processed on top of a lower density CMOS in a 'CMOL configuration' [10]–[12]. In both cases, however, cross-bar arrays suffer from the issue of sneak paths [13], whereby applying a voltage across the electrodes of a target device leads to the inadvertent application of voltage across all other elements in the array. This gives rise to sneak-path currents that hinder the accurate reading of the active device's resistive state (Figure 1(a)). Sneak currents can be minimised by the implementation of non-linear selector elements embedded into the storage node [14] ('1D1R' structure) or the utilisation of CMOS transistor-based selectors [15] (Figure 1(b) - '1T1R' structure). An additional method for mitigating sneak path effects is the technique of multi-port read-out and subsequent mathematical cancellation of said sneak path currents [16]. Selector based sneak current mitigation techniques suffer from their own shortcomings, such as loss of scalability (1T1R designs) and issues with reversibility of write process and manufacturing complications (1D1R designs). Nonetheless, reducing the disruptive effect of sneak path currents would bring an increase in the state reading accuracy and allow for multiple bits per cross-point cell, dramatically increasing storage density in future memory applications.

In this work, we focus our efforts towards this issue and present a multi-port technique for reading accurate analogue cross-point resistance values from devices within a planar, selector-less crossbar array - a markedly stricter criterion than achieving a good digital read margin. We implement the non-intrusive reading and writing techniques on a desktop PCB which facilitates quick acquisition of data of RRAM cells in a 32x32 crossbar array configuration via a user-friendly graphical user interface (GUI) on a local PC. More specifically, in Section II we introduce the theoretical background of our approach. Section III describes the practical implementation of our 'memristor Characterisation And Testing' (mCAT) system. Experimental results from a reference resistive crossbar array and an equal size solid-state RRAM array are presented in section IV. Finally, section V considers the benefits and limitations of the current system, as well as offering insights into the scaling up performance of the mCAT and direction of future efforts.

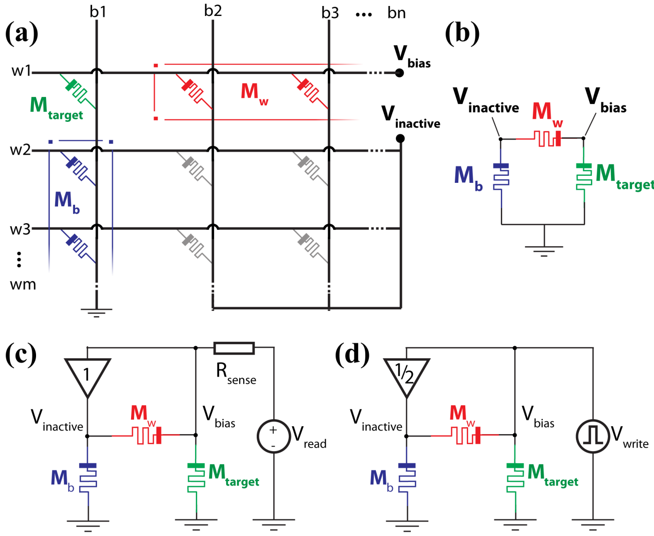

Fig. 2. a) Illustration of a m x n (of which the first 3 word- and bit-lines are shown) crossbar array with M_{target} - device under test located at the cross between active wordline (w1) and active bitline (b1), M_w - parallel combination of all inactive devices on the active wordline, M_b - parallel combination of all inactive devices on the active bitline: (b) Reduced three-node/three-lumped-component circuit. c) Conceptual circuit for reading analogue resistance values via (b). d) Conceptual circuit for a 'write' operation performed on same target device.

II. Theoretical Analysis

A. Crossbar basic observations

An illustration of the sneak-path current issue is represented in Figure 1. The selection of voltages applied to the inactive word- and bit-lines during operation (for multi-port read-out) and their relation to the voltages on the active word- and bit-lines affects the distribution of sneak currents within the array (Figure 2a). Furthermore, if all inactive word- and bit-lines are shorted together, the entire array is reduced to a three-node/three-lumped-component circuit shown in Figure 2(b). External circuits can access any of the three nodes for either voltage or current sourcing/measurement, but any other currents flowing within the cross-bar remain inaccessible.

B. Read operation

Measuring the resistive state (memristance) of a target device M_{target} ('read' operation) requires accessing both the voltage drop across it (i.e. $V_{bias} - GND$ in Figure 2(a)) and the current flowing through it during biasing. As illustrated in Figure 2(b), the current through M_{target} can be obtained if M_w is bootstrapped by appropriately biasing node $V_{inactive}$. This is not the only way to gain access to the M_{target} current. For example, if the grounded node is connected instead to e.g. a transimpedance amplifier virtual ground and M_b is bootstrapped, access to the current through M_{target} is gained.

In practice such read-out scheme may be implemented by a circuit as shown in Figure 2(c). V_{bias} and V_{read} are directly accessible by voltage measurement and the current through M_{target} is indirectly computed via R_{sense} thus allowing calculation of the analogue resistance value of M_{target} by solving the voltage divider network.

A crucial characteristic of the proposed read-out scheme is the fact that $V_{inactive}$ has to be derived from V_{bias} (e.g. by buffering) so as to allow separation between the currents flowing through M_{target} and the rest of the array and is accuracy-critical. The criticality occurs from the worst-case scenario whereby the target is in very high resistive state and the lumped component M_w consists entirely of memory cells in very low resistive states, thereby forming a very low impedance path between V_{bias} and $V_{inactive}$. Even small offsets in the generation of $V_{inactive}$ from V_{bias} can lead to significant amounts of current being diverted through M_w hence corrupting our estimate of the target state.

C. Write operation

RRAM cells are usually characterised by a voltage switching threshold (V_{thr}) under which no applied potential can disturb it's resistive state [17]. We utilise this feature in our write scheme by applying half of the active device's write voltage (V_{write}) to all inactive lines as illustrated in Figure 2(d). Provided that $V_{write} > V_{thr}$ and $V_{write}/2 < V_{thr}$ then the risk of accidentally programming adjacent devices when writing only on M_{target} is minimised. We note that the write operation is not accuracy-critical, i.e. small variations in $V_{inactive}$ do not significantly perturb the write operation.

III. System Implementation

To demonstrate these ideas and to facilitate practical RRAM characterisation, a full system has been implemented on PCB. A photograph of the set-up is shown in Figure 3(a) with it's corresponding simplified schematic diagram in 3(b). The key components of this platform are:

- An mBED LPC1768 microcontroller which contains the following functionalities:
  - serial communication with a local PC;
  - 5 x 12-bit ADCs and one 10-bit DAC on board.
  - 20 digital 10 ns transition i/o pins;
- A 'Bias generator' consisting of a voltage feedback op-amp in a subtractor configuration which maps the output of the mBED DAC from 0 -> 3.3 V to -10.9 V -> 10.9 V at V_{OUT}.
- A sense resistor bank allowing connection of the bias generator to the cross-bar array via different sense resistors or a resistorless, by-pass path.
- A feedback buffer copying the voltage on the active word-line (V_{bias} to $V_{inactive}$ during 'read' operation).
- A feedback amplifier block applying half the voltage on the active word-line (V_{bias} to $V_{inactive}$ during 'write' operation).
- Two analogue multiplexer banks allowing access to the word- and bit-lines of the crossbar array.
- A variety of 'housekeeping' systems (power management, multiplexer controllers).

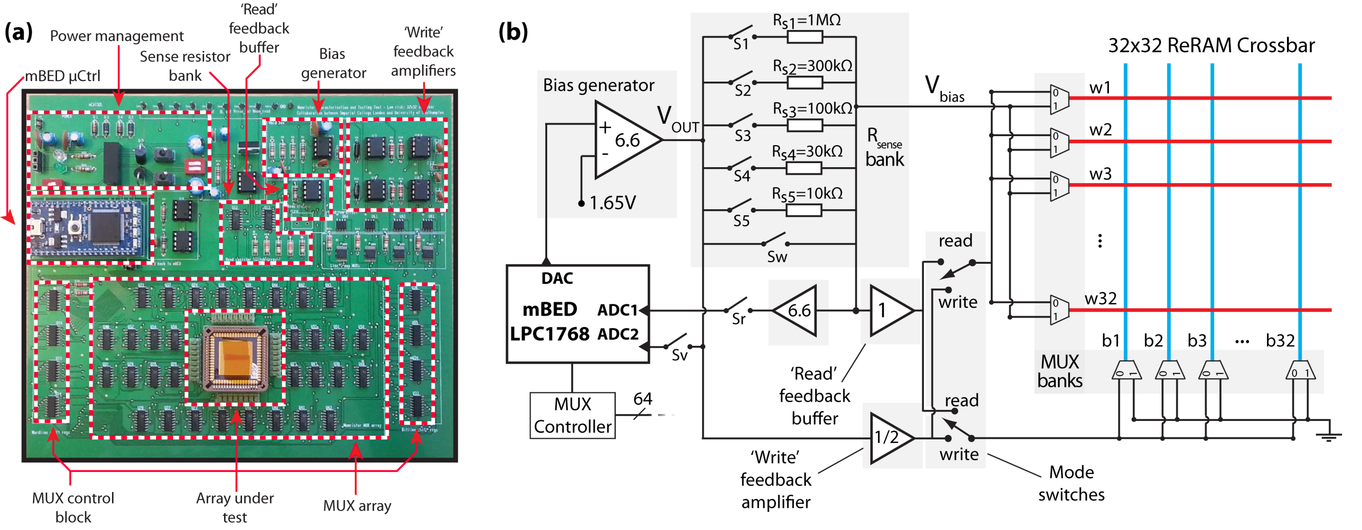

Fig. 3. a) Photograph of the mCAT system on PCB. The 'Array under test' block contains a standard DIP PLCC68 holder in which a complementary package containing bonded 32x32 array cells can be introduced. The holder is surrounded by four 2x8 sockets used to interface to a probe card for on-wafer measurements. b) Simplified mCAT schematic diagram.

A. Read operation

Assuming all switches are open in idle mode, and V_{OUT} = 0 V, the operation proceeds as follows: first the target device is selected by connecting the corresponding (active) wordline to the V_{bias} node and the respective bitline to GND. The inactive word- and bit- lines are shorted together and connected to the output of the 'read' feedback buffer. Then, the mBED sets its DAC to facilitate V_{OUT}=$0.5\,V$ (default value but programmable) and subsequently switches the $1\,M\Omega$ sense resistor in (closes S1). This provides a DC bias to the bootstrapping feedback buffer input which hence forth constantly performs its bootstrapping function on the inactive crossbar lines. The mBED then takes a reading of V_{OUT}=V_{read} via ADC1 by closing switch Sr, and a reading of V_{bias} via ADC2 by closing the switch Sv. Typically 50 measurements taken at full reading rate are averaged as a compromise between speed and noise rejection. The estimates of V_{bias} and V_{read} along with the value of the first sense resistor used yield enough information for a first calculation of the target memristance M_{S1}. Time delays are introduced to ensure voltage readings are performed after all nodes have settled.

Next, the $1\,M\Omega$ is switched out, the $300\,k\Omega$ resistor is switched in (S1 open, S2 close), and the previous procedure of measuring V_{bias} and V_{read} is repeated yielding a new candidate value of memristance M_{S2}. This sequence is repeated for all sense resistors producing five different values $M_{S1->S5}$ for the resistance of the target device, each one corresponding to its respective sense resistor utilised $R_{S1->S5}$. These are recorded by the mBED.

Finally, from all calculated $M_{S1->S5}$, a single value M_{Si} is chosen in software as the final read value of memristance, where i is the index at which $\left|\frac{M_{Si}-R_{Si}}{R_{Si}}\right|$ is minimised. This ensures that a reading is taken at the point where $\partial V_{bias}/\partial M_{target}$ is maximised allowing for a minimal δM change that will produce a 1 LSB shift in voltage at the input of ADC1. To prove this we note that from Figure 2c:

$$V_{bias} = \frac{V_{read} \cdot M_{target}}{M_{target} + R_{sense}} \tag{1}$$

$$\frac{\partial V_{bias}}{\partial M_{target}} = \frac{V_{read} \cdot R_{sense}}{(M_{target} + R_{sense})^2} \tag{2}$$

$$\frac{\partial^2 V_{bias}}{\partial M_{target} \partial R_{sense}} = \frac{V_{read}(M_{target} - R_{sense})}{(M_{target} + R_{sense})^3} \tag{3}$$

where (2) expresses the sensitivity of our measurement node voltage V_{bias} to differences in the value of M_{target} (measurement sensitivity) and (3) expresses the sensitivity of the measurement sensitivity on the value of the sensing resistor used. Hence the maximum sensitivity for given M_{target} and V_{read} is reached when $M_{target} = R_{sense}$.

B. Write operation

With initially all switches open, the 'write 'operation proceeds as follows: first the target device is selected and the output voltage V_{OUT}=V_{write} is set to the desired value. Mode switches are set to 'write'. Subsequently, the by-pass switch (S_w) is flash closed for the desired pulse width duration. Whilst the active device is being subjected to the V_{write} voltage all inactive devices are fed $V_{write}/2$ via the bootstrap amplifier. Instead of using one feedback amplifier, the physical implementation of our system employs a bank of two pairs of amplifiers (one for word-line and one for bit-lines) that facilitates the use of different gain settings for word- and bit-lines for testing purposes.

C. Control Interface

The mCAT is controlled by a host PC via a serial connection through a custom MATLAB GUI which allows quick control and data acquisition. The full measuring system involves the simultaneous operation of software on the mCAT level (mBED

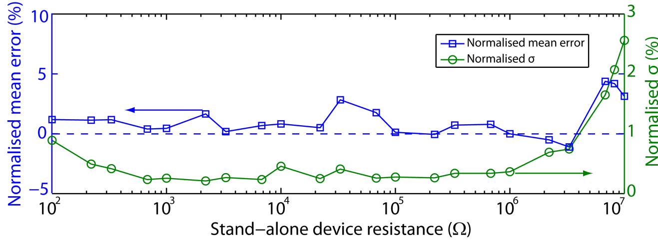

Fig. 4. Single device measurements showing low mean error and low variability between identical measurements (80 times) for a resistance dynamic range in between 100Ω and 10MΩ

programmed in C) and GUI level (MATLAB). High level functionality, such as: a) array-level operations (e.g. whole array programming or measurement), b) complicated single-device operations (e.g. setting to specific resistive state as per [18], [19], c) instrument calibration and d) data display, are handled by the MATLAB layer. Lower level functionality such as the mechanics behind device targeting, biasing and reading is directly implemented in the C layer.

IV. Experimental results

The mCAT is capable of self-calibration which ensures the effects of any hardware drifts and offsets are minimised in the C layer. Initially, the reading accuracy was assessed as a sanity check by measuring single discrete resistors, spanning 5 decades, connected across arbitrary inputs, and comparing the results with a high-end multimeter. Figure 4 shows minimal mean read errors and excellent precision for stand-alone device measurement, without the intrusive effects of sneak-paths.

A 32x32 resistor crossbar array with SMD resistors was manufactured (Figure 5a) in order to measure the accuracy of the read operation. A limited range of resistor was utilised (1 k, 5.6 k, 10 k, 56 k, 100 k, 560 k and 1 MΩ) with the color map of the position of each resistor on the array displayed in Figure 5b. The configuration was chosen such as to provide high stress conditions (high resistance elements sharing word or bit-lines with many low resistance elements) which are more likely to disrupt the correct reading of the target resistor and such test the limitations of our system. After reading the full array, an extra scaling step is performed, described by (11) in appendix, which is meant to increase the accuracy of each cross-point resistance estimation. Results of the full crossbar reading are illustrated in Figure 5c and d. The mCAT can thus measure 90 % of the resistors on our standard testing crossbar with less than 10 % reading error. It is clear from Figure 5d that high resistance have larger reading errors than low resistance devices. This is due to the influence of M_w and the voltage offset of the read feedback buffer (V_{os}) used to isolate $V_{inactive}$ from V_{bias} as illustrated in Figure 2c. Other sources of error in the system will be caused by a complex combination of effects from V_{os}, M_w, M_b, R_{sense} and the non-zero resistance of analogue switches, listed in appendix.

Several 32x32 TiO_{2-x}(x=0.06 as measured by X-ray photoemission spectroscopy (XPS)) solid-state RRAM crossbars were further measured by this setup. The following results

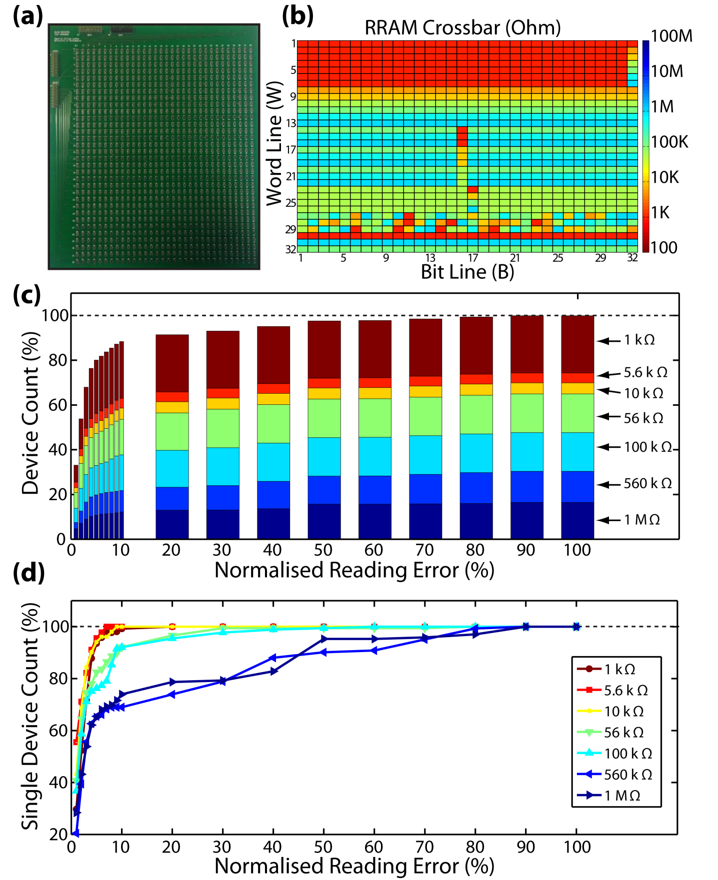

Fig. 5. a) Manufactured 32x32 crossbar array of SMD resistors; b) Real resistance of each word and bit-line location on the crossbar illustrated in a); c) Normalised reading errors $\left|\frac{R_{measured}-R_{real}}{R_{real}}\right|$ (%) of all resistors in the crossbar illustrated in a). Each bin shows % of all devices that were read with an error of less than the corresponding bin value, color coded stack for each type of resistor. d) Normalised reading errors as in c) per type of resistor.

depicted in Figure 6 were obtained from 2x2 μm^2 crossbar devices with the stack Ti/Pt/TiO_{2-x}/Pt (5/10/25/10 nm), diced in individual crossbars and packaged in standard DIP PLCC68 compatible with the mCAT setup. Figure 7 shows measurements attained from 30x30 μm^2 cross-bar devices accessed directly on wafer, with the stack: Cr/Pt/TiO_{2-x}/Pt (3/5/25/4 nm).

Each device in the crossbar can be individually selected and have any pulsing sequence applied to, with reading operations being performed in between each programming pulse. A pulsing sequence recorded for one device is illustrated in Figure 6a showing resistance modulation in between four different intermediate states. The full 32x32 array was measured before and after the application of this pulsing scheme and the distribution of the normalised resistance difference between the two iterations, excluding the target device, is plotted in the inset of Figure 6a. The resistance differences are within the noise floor and as such the inset shows minimal disturbance to inactive devices during programming of a single RRAM cell.

Furthermore, the mCAT can be linked via external connectors located around the package holder to an external 64 pin probe-card which facilitates interfacing on 32x32 crossbars directly on wafer (Figure 6d). A full array read

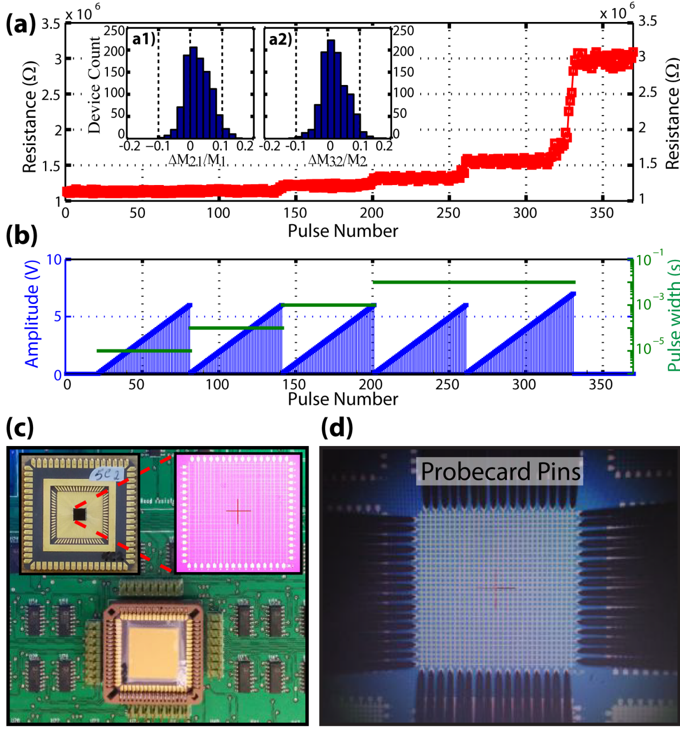

Fig. 6. a) Modulation of resistance of a single solid state TiO_{2-x} memristor cell (M_T located in a 32x32 crossbar array under the pulsing scheme illustrated in b); Inset of a1) shows normalised read-outs for all devices in the prototype array without the target device M_T: $\Delta M_{21} = M_2\text{-}M_1$, where M_1 and M_2 represent the read resistances of all 1023 devices, before (M_1) and after (M_2) the application of the pulsing scheme of b) to M_T. Inset a2) shows same normalised read-out errors $\Delta M_{32} = M_3\text{-}M_2$ where M_3 represents the read resistances in immediate succession after the pulsing of M_t and the read sequence of M_2. The error distribution is similar. c) Packaged 32x32 RRAM cells in standard PLCC68 package, connected to the mCAT; Inset shows exposed memristor die; d) Microscope photograph of a 32x32 TiO_{2-x} RRAM crossbar array on wafer interfaced by the mCAT via a 64 pin probe-card.

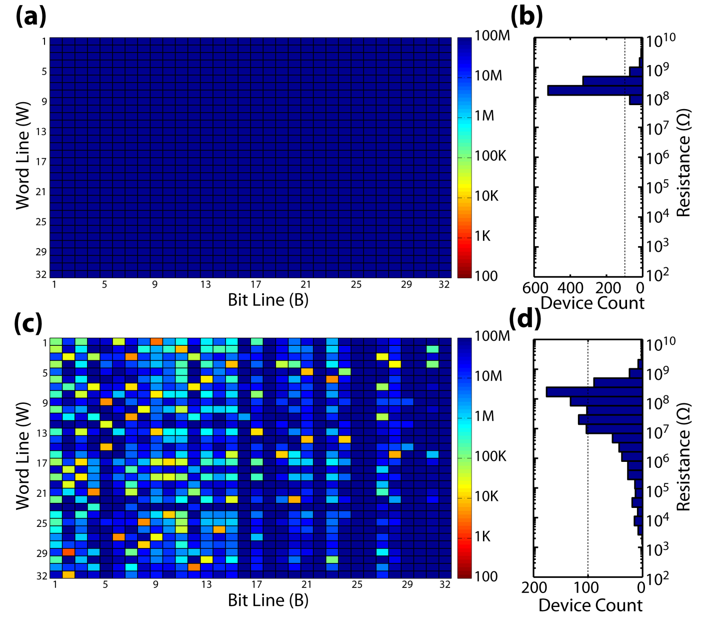

Fig. 7. Measurements from a TiO_{2-x} RRAM crossbar on wafer. a) Full array measurement before programming; b) Resistive state distribution for a); c) Full array measurement after programming; d) Resistive state distribution for c).

of one RRAM crossbar on wafer (Cr/Pt/TiO_{2-x}/Pt stack of 30x30 μm^2 surface area) is illustrated in Figure 7a with the distribution of read states in Figure 7b. Each device was then subjected to a positive pulse train of 10ms width and amplitude 0 to 8 V in 0.25 V steps, with the goal of switching to a resistive state lower than $R_{on} = 100\,k\Omega$ (electroforming). Full array reading after the programming run is illustrated via color-coding in Figure 7c with it's associated resistive state distribution in Figure 7d, showing scattered successfully electroformed devices directly on wafer.

V. Discussion

The main requirement of a system similar to the mCAT is reading analogue values of resistance. As such, there are a couple of aspects that limit the performance of such a platform. One is concerned with the reading errors which can be substantial in cases where the target resistance (M_t) is high and the inactive bit (M_b) and word-line (M_w) resistances are low. In order to mitigate the influence of M_w on M_t, a read feedback buffer with zero-offset and a FET input stage must be utilised (Figure 2c). On the other hand, M_b provides current via the feedback buffer to the active bitline access MUX switch resistance, lifting the ground potential (Figure 9). Another limitation is represented by the minimum programming pulse width which is restricted by the speed of the 'Bias Generator' op-amp (Figure 3b), parasitic impedance on the active signal line, and the mBED clock. As such, the non-zero resistance of the analogue switches, along with the finite offset of the read feedback buffer play a major role in the estimation of the target device resistance, and have been quantified in the model listed in the appendix.

This circuit model was further utilised to analyse the degradation of reading accuracy when using the mCAT to access larger crossbars and under several R_{off}/R_{on} (boundary resistive states of ideal RRAM cells) conditions. As mentioned before, the worst case scenario (largest reading errors) occurs when all devices on the active word- and bit-line (except the target device M_{target}) are equal to R_{on}, yielding low impedance M_w and M_b. Provided M_{target} can ideally vary in between Ron and Roff then the voltage read by the mBED ADC1 will vary monotonically in between two corresponding boundary cases. The difference in voltages read by the mBED in between these two cases represents a reading voltage margin from which the ADC1 can distinguish a number of different states based on its finite resolution (for the onboard mBED ADC1 - 1LSB $\approx$ 3.3mV). We utilise this figure of merit (reading bit accuracy) to quantify the performance of our simulated mCAT for larger scale arrays (Figure 8).

It is evident that the bit reading accuracy drops significantly with increasing crossbar array size. This is due to the lumped components M_w and M_b becoming increasingly more conductive. Interestingly, R_{off}/R_{on} ratios have a profound effect only on small array sizes, while the reading accuracy variations remain similar for larger scale arrays. This is most likely due to 'R_{off}' measured voltages becoming saturated, or decreasing

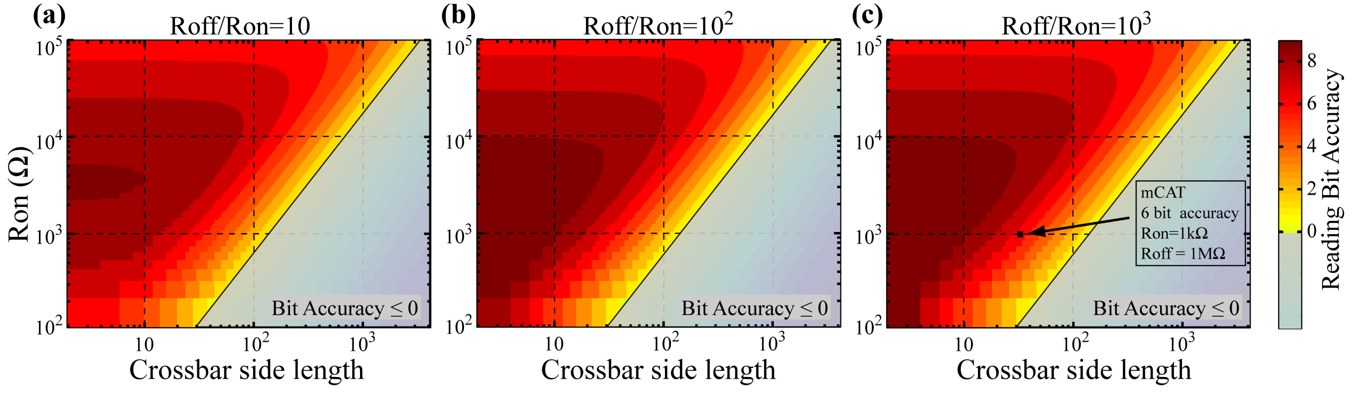

Fig. 8. mCAT reading performance for large array sizes and increasing R_{on} values under R_{off}/R_{on} of a) 10, b) 100, c) 1000.

very little with larger arrays and larger R_{off}.

In the case where the system should only distinguish bistable (binary or 1 bit accuracy) RRAM cells which toggle between dissimilar R_{on} and R_{off} resistive states, the reading limitations relax dramatically, as illustrated in Figure 8c. Depending on the R_{off}/R_{on} ratio, the mCAT is estimated to be capable of measuring binary RRAM chips of up to 3200x3200 (or ≈10 Mb) crossbar size.

VI. Conclusion

The mCAT is a low-cost, versatile platform for measuring and programming of RRAM cells as single devices, or more importantly in a 32x32 crossbar array configuration. The reading and programming schemes ensure that each cross-point resistance can be isolated from adjacent devices by active sneak-path current redistribution. For reading analogue values of resistance, our platform is capable of measuring stand-alone resistive cells in the range of 100 Ω to 10 MΩ with less than 5% error and excellent precision ($\sigma < 3\%$). In our custom discrete resistor crossbar array, designed to simulate high stress conditions (low impedance sneak paths), 90% of devices in 1 kΩ to 1 MΩ range were measured with less than 10% error. Hence our particular reading technique allows for reading with multiple bit accuracy of cross-point cells. While interfacing with solid-state RRAM cells, applying programming pulses exerts halved interference on remaining inactive devices, minimising the risk of accidentally modulating their resistive states.

The platform's versatility is promoted by the use of a NXP mBED microcontroller which controls the adjacent mixed-signal circuitry. The mCAT is controlled via a MATLAB GUI which allows seamless interaction with 32x32 RRAM crossbar arrays, packaged or directly on wafer via a custom probe-card. The latter method speeds up the process of mass testing of RRAM crossbars by accessing the devices without the need for dicing and packaging of individual dies.

Acknowledgment

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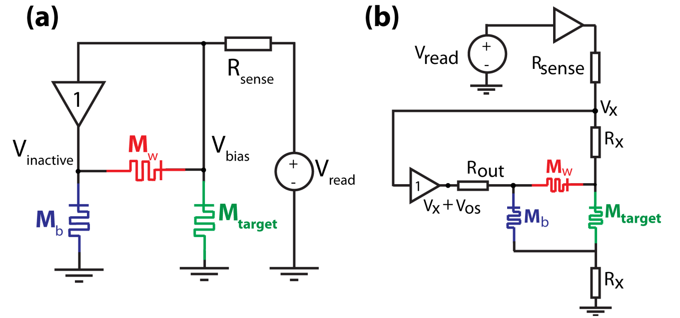

Fig. 9. a) Ideal circuit diagram of a read operation; b) Realistic circuit diagram of a read operation.

Appendix

In order to improve the accuracy of the reading method, the ideal circuit which is formed when the mCAT is in the 'read' mode is extended to include the effects of the non-zero resistance of the analogue switches employed and the offset voltage of the 'read' feedback buffer (Figure 9b). Solving for M_t, the real resistance of the target device, reveals:

$$V_{read} - V_x = \frac{M_t^2 A + M_t B + C}{M_t^2 D + M_t E + F} \tag{4}$$

where:

$$A = R_{sense}\left[V_{read} R_{out} - V_{os}\left(M_b + R_x\right)\right] \tag{5}$$

$$B = R_{sense}\left\{\left(M_w + M_b\right)\left[2V_{read} R_{out} - V_{os}\left(M_b + 2R_x\right)\right] + V_{read} M_w M_b\right\} \tag{6}$$

$$C = R_{sense}\left(M_w + M_b\right)\left[V_{read} M_w M_b + \left(M_w + M_b\right)\left(V_{read} R_{out} - V_{os} R_x\right)\right] \tag{7}$$

$$D = R_{out}\left(M_w + 2R_x + M_b + R_{sense}\right) + \left(R_x + M_b\right)\left(R_x + M_w\right) \tag{8}$$

$$E = M_w M_b (R_{sense} + M_w + 2R_x + M_b) + \left(M_w + M_b\right)\left[R_{out}(2R_{sense} + M_w + 4R_x + M_b) + R_x(2R_x + 2R_{out} + M_w + M_b)\right] \tag{9}$$

$$F = (M_w + M_b)\left\{(R_{sense} + 2R_x)\left[M_w M_b + R_{out}(M_w + M_b)\right] + (M_w + M_b)R_x^2\right\} \quad (10)$$

Rearranging (4) gives two solutions for M_t, from which we chose the positive value as the final measured value of memristance.

$$M_{t_{1,2}} = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} \quad (11)$$

where:

$$a = (V_{read} - V_x)D - A \quad (12)$$

$$b = (V_{read} - V_x)E - B \quad (13)$$

$$c = (V_{read} - V_x)F - C \quad (14)$$

The full solution for M_t therefore has 8 parameters: V_{read}, V_x, V_{os}, R_{sense}, R_x, R_{out}, M_w and M_b. V_{read} is chosen to be low in order to not disrupt the state of the target device whilst measuring (0.5V in our case), R_x is the typical series resistance of the analogue switches in the circuit, V_{os} is the offset voltage of the 'read' feedback buffer (median value) and R_{out} is the output resistance of the same buffer, which was utilized as a fitting parameter. Our measuring technique for the full 32x32 crossbar involves the following steps which aim to estimate the remaining parameters (V_x, M_w, M_b and R_{sense}):

1) Perform a standard reading technique (as described in Section IIIa) on the full array and store the results in a 32x32 matrix locally. Record the value for V_x and R_{sense} for each word and bit-line.
2) Compute estimates for M_b for each word and bit-line from the stored matrix of memristance values from the previous step.
3) Measure M_w values for the full array. In a standard target device read, the device selection is performed by configuring the MUX bank so that the active word line is connects to the bias generator, the active bit line to GND and the rest of the lines shorted together to the read feedback buffer. To measure M_w, the bit-line MUXs address bit string is inverted so that all inactive lines are grounded, and the 'active' bit-line (the one who's corresponding M_w is being measured) is connected to the 'read' feedback buffer. As such, a reading operation performed in this configuration will give an estimate of M_w - the parallel combination of all devices on the active word-line, without the target device. These values are recorded for all word and bit-line addresses.
4) All parameters have been estimated and M_t is computed via our model.

REFERENCES

[1] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, no. 7191, pp. 80–83, 2008.

[2] L. Chua, "Resistance switching memories are memristors," *Applied Physics A*, vol. 102, pp. 765–783, 2011.

[3] T. Prodromakis, C. Toumazou, and L. Chua, "Two centuries of memristors," *Nature Materials*, vol. 11, no. 6, pp. 478–481, 2012.

[4] S. Pi, P. Lin, and Q. Xia, "Cross point arrays of 8nm x 8nm memristive devices fabricated with nanoimprint lithography," *Journal of Vacuum Science & Technology B*, vol. 31, no. 6, 2013.

[5] X. Yang and I.-W. Chen, "Dynamic-load-enabled ultra-low power multiple-state RRAM devices," *Scientific reports*, vol. 2, 2012.

[6] R. Waser and M. Aono, "Nanoionics-based resistive switching memories," *Nature materials*, vol. 6, no. 11, pp. 833–840, 2007.

[7] X. Yang, A. Chen, B. Choi, and I.-W. Chen, "Demonstration and modeling of multi-bit resistance random access memory," *Applied Phisics Letters*, vol. 102, pp. 043 502–043 502–4, 2013.

[8] S. Yu, H.-Y. Chen, B. Gao, J. Kang, and H.-S. P. Wong, "HfOx-based vertical resistive switching random access memory suitable for bit-cost-effective three-dimensional cross-point architecture," *ACS Nano*, vol. 7, no. 3, pp. 2320–2325, 2013. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/nn305510u

[9] B. Govoreanu, G. Kar, Y. Chen, V. Paraschiv, S. Kubicek, A. Fantini, I. Radu, L. Goux, S. Clima, R. Degraeve *et al.*, "10×10nmˆ2 Hf/HfOx crossbar resistive ram with excellent performance, reliability and low-energy operation," in *Electron Devices Meeting (IEDM), 2011 IEEE International*. IEEE, 2011, pp. 31–6.

[10] K. K. Likharev, "Cmol: A silicon-based bottom-up approach to nanoelectronics," *Interface*, vol. 14, pp. 43–45, 2005.

[11] X. Ma, D. Strukov, J. H. Lee, and K. Likharev, "Afterlife for silicon: Cmol circuit architectures," in *Nanotechnology, 2005. 5th IEEE Conference on*, July 2005, pp. 175–178 vol. 1.

[12] G. Indiveri, B. Linares-Barranco, R. Legenstein, and T. Prodromakis, "Integration of nanoscale memristor synapses in neuromorphic computing architectures," *Nanotechnology*, vol. 24, p. 384010, 2013.

[13] E. Linn, R. Rosezin, C. Kügeler, and R. Waser, "Complementary resistive switches for passive nanocrossbar memories," *Nature materials*, vol. 9, no. 5, pp. 403–406, 2010.

[14] A. Chasin, L. Zhang, A. Bhoolokam, M. Nag, S. Steudel, B. Govoreanu, G. Gielen, and P. Heremans, "High-performance a-igzo thin film diode as selector for cross-point memory application," *Electron Device Letters, IEEE*, vol. 35, no. 6, pp. 642–644, June 2014.

[15] M.-F. Chang, J.-J. Wu, T.-F. Chien, Y.-C. Liu, T.-C. Yang, W.-C. Shen, Y.-C. King, C.-J. Lin, K.-F. Lin, Y.-D. Chih, S. Natarajan, and J. Chang, "Embedded 1mb reram in 28nm cmos with 0.27-to-1v read using swing-sample-and˙couple sense amplifier and self-boost-write-termination scheme," *IEEE International Solid-State Circuits Conference*, vol. 19, 2014.

[16] M. Zidan, A. Eltawil, F. Kurdahi, H. Fahmy, and K. Salama, "Memristor multiport readout: A closed-form solution for sneak paths," *Nanotechnology, IEEE Transactions on*, vol. 13, no. 2, pp. 274–282, March 2014.

[17] K.-H. Kim, S. Gaba, D. Wheeler, J. Cruz-Albrecht, T. Hussain, N. Srinivasa, and W. Lu, "A functional hybrid memristor crossbar-array/cmos system for data storage and neuromorphic applications," *Nano Letters*, vol. 12, pp. 389–395, 2012.

[18] F. Alibart, L. Gao, B. Hoskins, and D. Strukov, "High precision tuning of state for memristive devices by adaptable variation-tolerant algorithm," *Nanotechnology*, vol. 23, pp. 075 201–075 201–7, 2012.

[19] R. Berdan, T. Prodromakis, and C. Toumazou, "High precision analogue memristor state tuning," *IET Electronic Letters*, vol. 48, no. 18, pp. 1105–1107, 2012.