WILEY-VCH

DOI: 10.1002/((please add manuscript number))
Article type: Communication

Complementary Organic Logic Gates on Plastic Formed by Self-Aligned Transistors with Gravure and Inkjet Printed Dielectric and Semiconductors

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Keywords: nanoimprint lithography, self-alignment, sub-micron channel, gravure and inkjet printing, organic field-effect transistor

Organic electronics is a maturing field,[1] replete with a large variety of devices and fabrication technologies.[2] Often these are viewed in isolation, however ultimately it is likely that a holistic approach involving multiple techniques will yield the best manufacturing results. This will use the particular advantages of each technology and apply it where best-suited.[3]

As attention shifts to implementing complex circuit components, there is increasing focus on the use of complementary circuits. Complementary logic combines both p- and n-type semiconductors to yield circuits with better noise tolerance and lower power consumption,[4,5] although at expense of fabrication complexity (two semiconductors need to be deposited rather than one). This is where additive printing processes have the potential to yield dividends, allowing the selective deposition of materials onto the substrate. Among these techniques both inkjet and gravure printing have been widely adopted.

Inkjet printing has been used to fabricate a wide range of electrical components, including: complementary and ambipolar inverters,[6,7] quasistatic memory,[8] biosensors,[9] and organic photo detectors.[10] Similarly gravure printing has been used to fabricate circuits such as: complementary ring oscillators,[11] logic gates,[12] unipolar flip-flops and half-adders.[13,14] Although previous reports have combined gravure and ink-jet printing to fabricate p-type organic field-effect transistors (OFETs),[15] there is a lack of direct comparative studies of the impact of each process on the electrical performance of devices. Here we explore gravure versus inkjet printing of semiconductors, gravure printing versus photolithographic patterning of the OFET dielectric, and long-channel (> 1 μm) versus short channel (< 1 μm) OFETs.

Gravure printing enables very large-area, fast, roll-to-roll manufacturing, limited by the expense and time cost of fabricating clichés (printing plates).[16,17] Inkjet printing enables a computer-designed circuit to be printed readily and easily, limited by the relative throughput and speed of printing.[2] However the resolution of both technologies is still restricted to the micrometre scale and larger by the challenge of reliably transferring inks onto a substrate without spreading or dewetting while still maintaining electrical performance. While recent approaches are improving upon this limit, for example Kang *et al.*'s work on gravure printed sub-5 μm gate electrodes,[18] or that of Sekitani *et al.* on 2 μm inkjet printed electrodes,[19] the options for patterning sub-micron electrode geometries are limited.

We have previously demonstrated how ultra-violet nanoimprint lithography (UV-NIL) is a viable method for patterning sub-micron channel length OFETs on plastic.[20] Our approach also uses self-aligned lithography to minimise the overlap between the gate-source and gate-drain electrodes, reducing parasitic overlap capacitances that reduce the switching speed of OFETs.[21,22] Self-alignment yields other benefits such as overcoming equipment alignment tolerances and reducing parasitic current flows, and is compatible with more complex circuitry such as self-aligned unipolar ring oscillators.[23] In this work, we have used bottom-gate bottom-contact architectures, to avoid exposing the semiconductor to both the ultra-violet light and processing chemicals used for self-alignment. In addition to self-alignment here we extend the fabrication approach by incorporating gravure printed dielectrics and semiconductors, as well as inkjet printed semiconductors. We demonstrate both p- and n-type devices patterned side-by-side on the same substrate along with complementary inverters and logic gates.

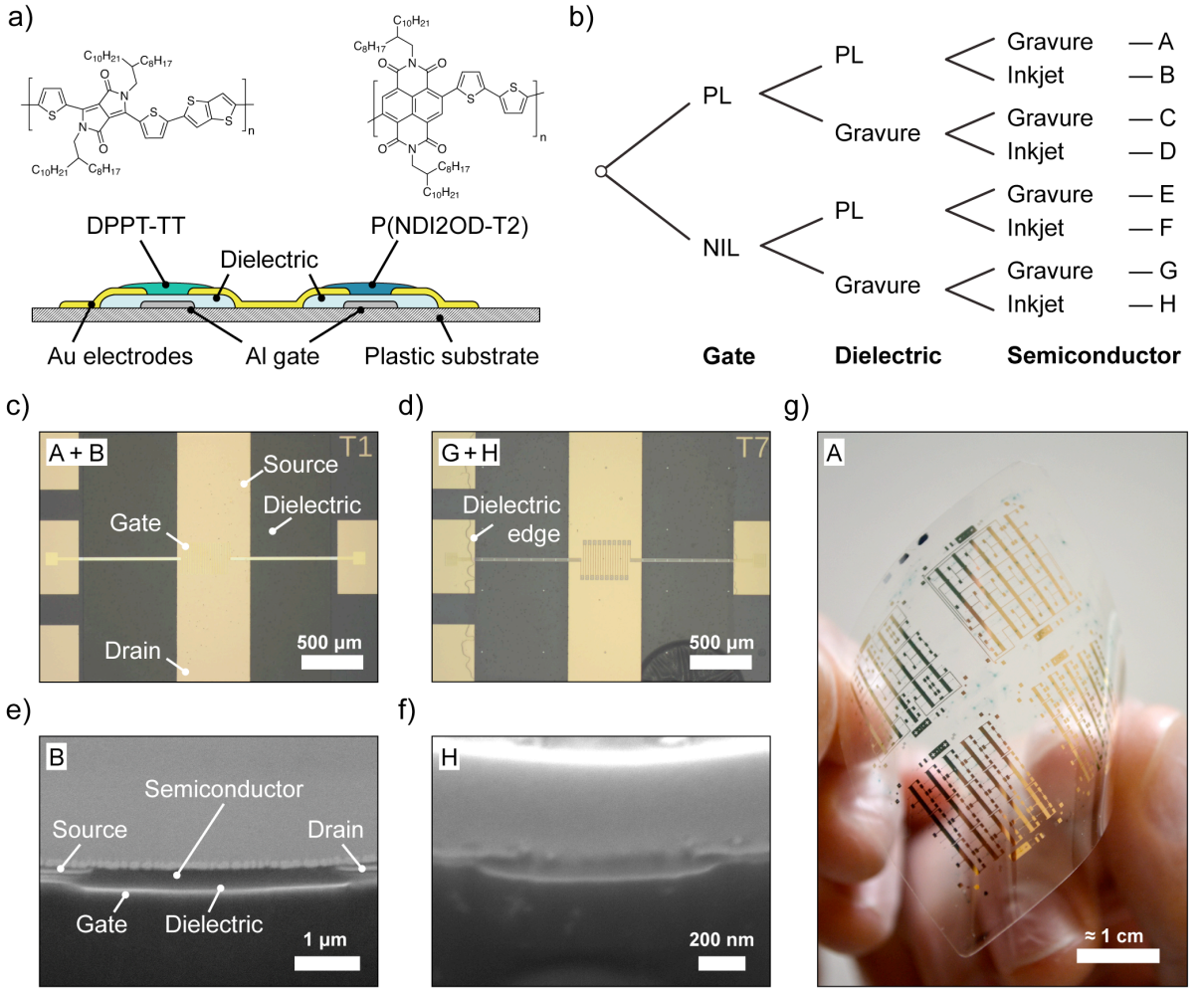

Figure 1. a) Device architecture and chemical structures of DPPT-TT and P(NDI2OD-T2). b) Tree diagram of architecture variants and identifying letters. Optical micrographs of c) PL patterned variants A & B and d) NIL/gravure variants G & H prior to semiconductor deposition. Note 'T1' and 'T7' are identifiers patterned on the substrate and should not be confused with annotations in white boxes. e) and f) SEM micrographs of cross-section through equivalent devices. Note both gold and platinum have been deposited on top of the device architecture as part of FIB-SEM process. g) Photograph of a finished flexible substrate (50 × 50 mm^2) showing OFETs, inverters and complementary logic circuits.

Figure 1 illustrates the materials and architectures used in this work. Aluminium OFET gates were patterned either photolithographically (PL) or via UV-NIL. A cross-linkable proprietary dielectric (GSID 938109-1, BASF)[24,25] was either PL patterned or gravure printed. Self-aligned gold electrodes were patterned via a bilayer liftoff process, before semiconductor patterning by either gravure or inkjet printing. Each substrate variant had two different semiconductors patterned on adjacent devices to facilitate complementary circuits. We chose two high performance polymeric semiconductors, based on previous demonstrations of transistor performance and printability.[2,8,26] These were the predominantly p-type polymer diketopyrrolopyrrole-thieno[3,2-*b*]thiophene (DPPT-TT);[27] and the n-type poly([*N,N'*-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,5'-(2,2'-bithiophene)) (P(NDI2OD-T2)) (structures in Figure 1a).[28] All devices are bottom-gate bottom-contact as necessitated by our self-aligned approach. The fabrication process is discussed in detail in the Supporting Information and also in our previous work.[20]

Figure 1c – 1f are micrographs showing the predominantly PL patterned (variants A + B) and printed (variants G + H) devices. The edges of the dielectric square are just visible in the optical micrographs (Figure 1c and 1d). The relatively large size of the dielectric region is to compensate for a nominal alignment tolerance of ± 0.5 mm in the gravure printer. These dimensions can be readily downscaled using a gravure printer featuring an alignment tool. We observed that gravure printing the dielectric yields a larger line-edge roughness compared to photo-patterning. This rippling of the printed edge is common throughout gravure printing, emerging from a combination of hydrodynamic instability in ink during the printing process,[29] and as a consequence of the underlying cliché cell structure.[30] Surface profilometry measurements indicated slight 'coffee ring effect' at the edge of the gravure printed structure,[31] but an otherwise homogenous flat film in the device region. Although based on the same dielectric, the gravure printed ink formulation yielded a thinner dielectric

layer (86 ± 14 nm) compared to the PL patterned layer (174 ± 26 nm) (see Figure S1 in Supporting Information).

We used a meandering gate to give self-aligned inter-digitated source-drain fingers with a nominal channel width of W = 5000 μm and length of L = 3 μm and L = 0.9 μm for PL and NIL patterned gates respectively. Focussed-ion beam scanning electron microscopy (FIB-SEM) was used to verify the nanoscale structure of the devices, as shown in Figure 1e and 1f. Device were milled by irradiation with gallium ions, before imaging the device cross-section using SEM. Exceptionally low gate-drain and gate-source electrode overlaps of ≤ 210 nm were observed. By comparison conventionally aligned, common-gate devices typically have overlaps on the order of many hundreds of microns. We also used the SEM micrographs and image analysis software to calculate the effective channel length of each variant.[32] NIL patterned channels were found to be slightly smaller and PL patterned channels slightly larger than the nominal L values (see Table S1 in Supporting Information for values).

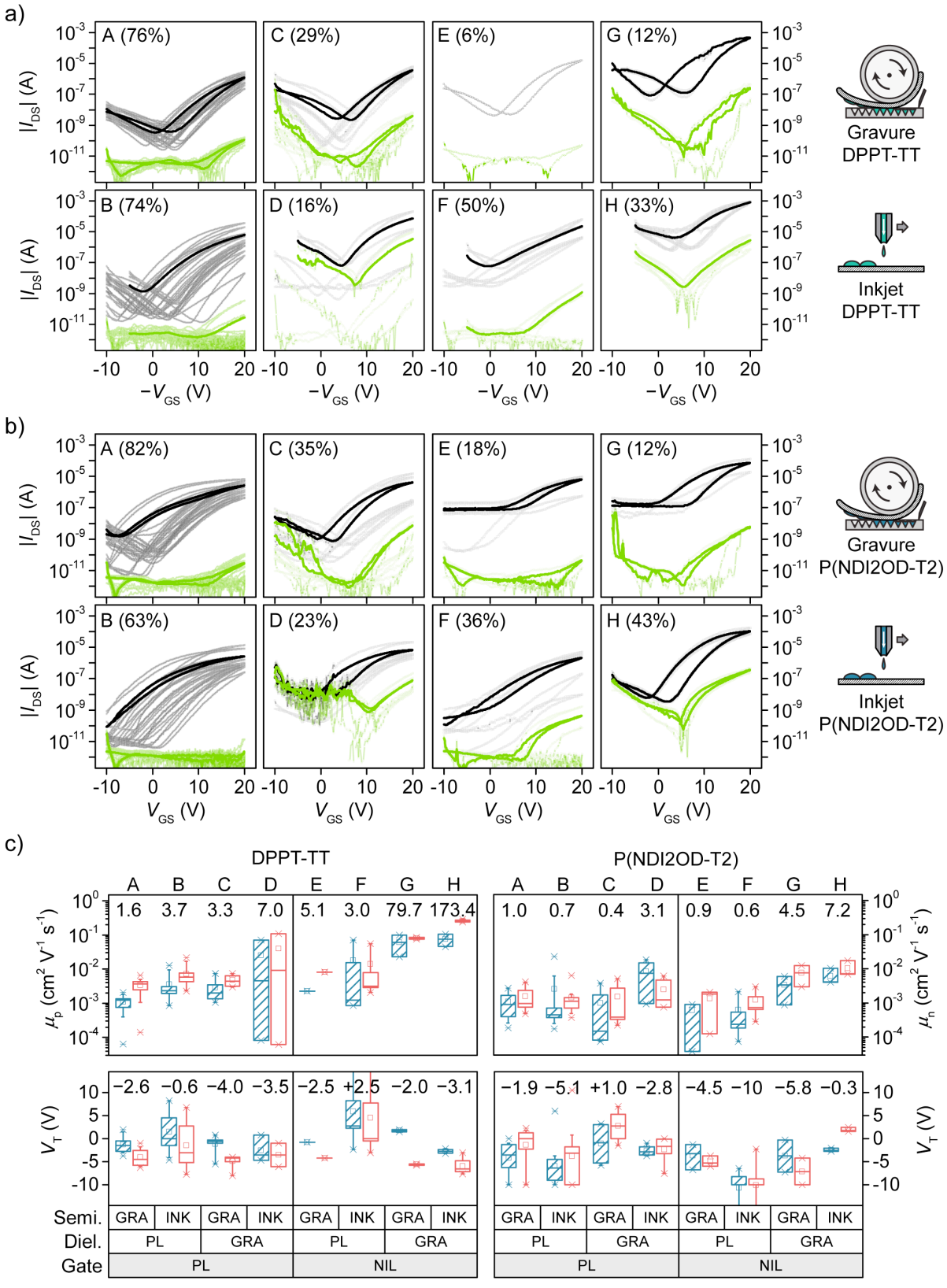

Figure 2. OFET transfer characteristics for a) p-type and b) n-type devices measured at $|V_{DS}|$ = 20 V, with gate current flow (I_{GS}) in green. Bold traces represent mean characteristics of all devices in that plot; percentages indicate test yield. Note all scales are equal and p-type data is plotted against $-V_{GS}$ to allow direct comparison with n-type. c) Box plots summarising extracted figures-of-merit for forward (teal, hatched) and reverse (red, unhatched) transfer

sweeps. Boxes represent 25th and 75th percentiles, horizontal lines in boxes the median, squares (□) the mean, whiskers (−) the 10th and 90th percentiles and crosses (×) the minimum and maximum values obtained. The median mobility (specified as $\times 10^{-3}$ cm^2 V^{-1} s^{-1}) and threshold voltage (V) of both forward and backward sweeps is quoted explicitly adjacent to each pair of boxes.

Figure 2 summarises the OFET device data. The transfer characteristics of each architecture variant for p- and n-type OFETs are shown in Figure 2a and 2b respectively, along with box plots of the extracted figures of merit in Figure 2c. Examples of the output and transfer characteristics for best performing 'hero' devices are shown in the Supporting Information (Figure S2).

In the case of photo-patterned dielectrics (variants A+B, E+F) exceptionally low leakage currents of < 0.1 nA are observed, another advantage of self-aligned architectures.[22] Gravure printed dielectric (variants C+D, G+H) exhibit slightly greater leakage as a result of the ≈50% thinner layer deposited by printing (as discussed above). Despite this the relative ratio of drain to gate current remains in the range $10^2 – 10^4$ for these devices, yielding functioning OFETs and circuits.

From Figure 2 we note that the combination of sub-micron NIL-patterned channels, thin gravure printed dielectric and inkjet printed semiconductor (variant H) yield both p- and n-type devices with the highest effective mobilities, with median values of μ_p = 0.173 cm^2 V^{-1} s^{-1} and μ_n = 0.007 cm^2 V^{-1} s^{-1} respectively. Similarly the best performing gravure printed semiconductor devices (variant G) exhibiting median values of μ_p = 0.079 cm^2 V^{-1} s^{-1} and μ_n = 0.005 cm^2 V^{-1} s^{-1} respectively. The observed boost for NIL patterned short channel devices suggests the onset of short-channel effects such as drain induced barrier lowering,[5] which boost current flow through the device.[33]

It is interesting to note from Figure 2c that to within uncertainty there is no significant difference in the extracted mobility for devices with PL patterned gates (variants A – D) for both DPPT-TT and P(NDI2OD-T2) semiconductors, unlike for NIL patterned gates (variants E – H). This suggests that at larger channel lengths the effective mobility obtainable is relatively process agnostic, while at shorter channel lengths the choice of deposition method has a greater influence. For the bottom-gate bottom-contact OFETs used here, the differing drying dynamics of gravure (simultaneous patterning and solvent evaporation) and inkjet

(sequential deposition and drying, combined with partial re-dissolution of the semiconductor by consecutive drops) may be responsible for the differences observed here.[16,31,34] However ultimately for larger channel length devices (typical in most applications) it appears for this material system that there is no electrical significance to using either inkjet or gravure printing for semiconductor deposition. In this case other factors, such as process throughput or ability to rapidly modify the printed design, may favour one technique over the other.

Uniformity was found to be an issue for both gravure and inkjet printed semiconductors, irrespective of material. The spread of threshold voltages suggests this variation originates at the dielectric-semiconductor interface. Although we use a cross-linked dielectric system, a viscosity modifier (high molecular weight poly(methyl methacrylate) (PMMA)) also forms part of the ink formulation and remains in the layer after cross-linking. Disordered dipoles in PMMA dielectrics have previously been observed to cause energetic disorder at the dielectric-semiconductor interface, yielding variation in device characteristics.[35] This represents one of the challenges of printed approaches; for example for gravure printing reducing the PMMA content impacts ink visoscity and hence film homogeneity.[36,37] Other methods for varying ink viscosity (concentration, long-chain solvent blends) are a possible approach to this issue.[29]

Process yield was predominantly dictated by two factors. In the case of gravure printed dielectric (variant C+D, G+H), the thinner layer combined with process variation increased the probability of breakdown pathways forming, as reflected in the higher leakage observed in functioning devices, which may be mitigated by increasing the layer thickness. For NIL patterned gates (E – H), the initial imprint step was significantly hindered by a lack of NIL tool, we instead relied on a customised mask aligner. While useful for proof-of-concept testing, the imprint step was found to trap air, displacing the resist during patterning and limiting yield at this early step in the processing. This is a well-understood phenomenon and has been engineered out of modern NIL tools.[38,39]

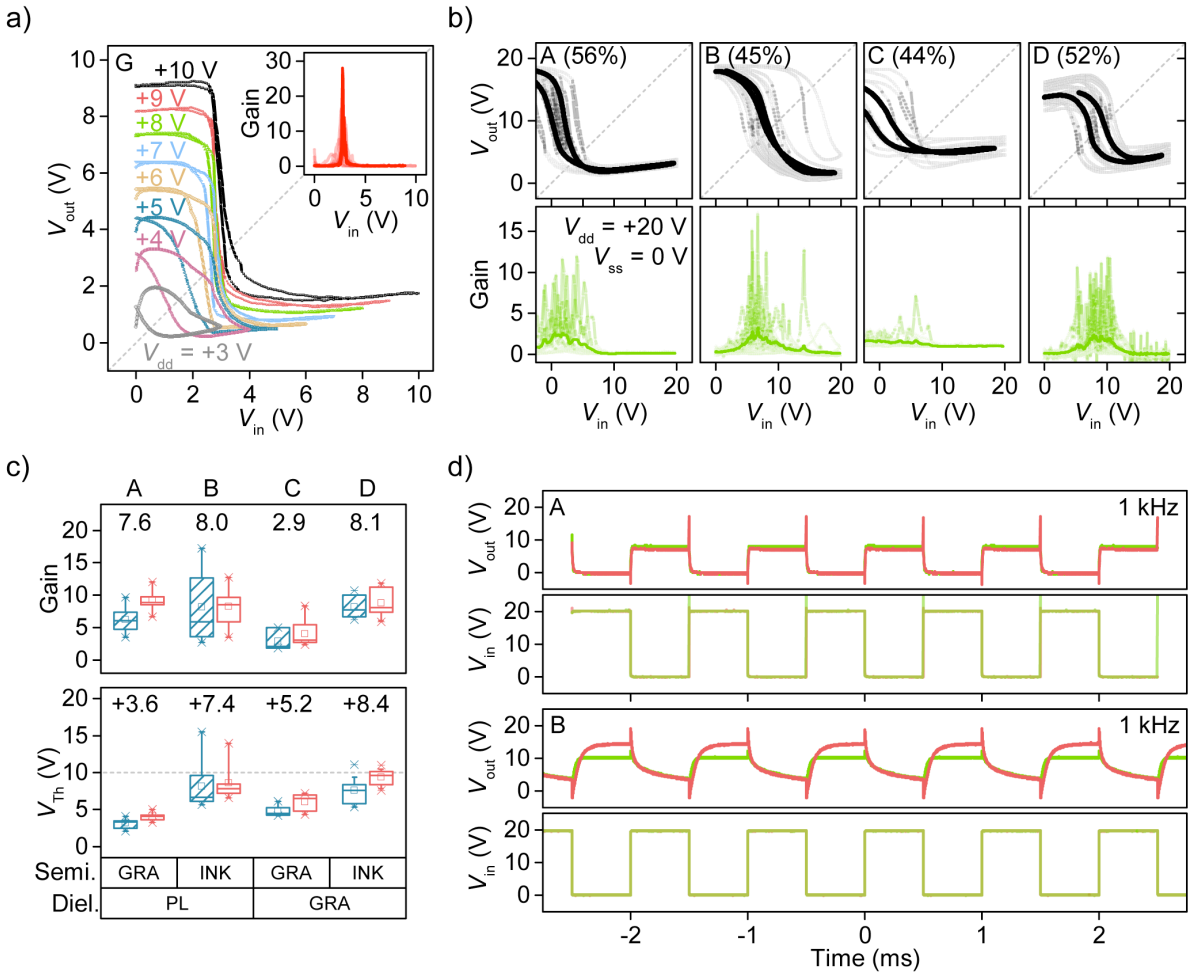

Figure 3. a) VTCs for a complementary inverter as a function of operating bias V_{dd}. Device comprises NIL patterned gate, gravure printed dielectric, and gravure printed p- and n-type semiconductors (variant G). Inset shows composite of corresponding gain characteristics. b) Composite of VTCs measured for A – D variants with corresponding gain curves. Bold traces represent mean characteristics of all devices in that plot. Dashed lines indicates $V_{in} = V_{out}$; percentages indicate test yield. c) Box plots of extracted gain and switching thresholds from b); dashed line indicates ideal switching threshold; box parameters as used in Figure 2. The median gain and switching threshold (V) of both forward and backward sweeps is quoted explicitly adjacent to each pair of boxes. d) Response of complementary NAND gates to alternating input for devices with gravure printed (variant A) and inkjet-printed (variant B) semiconductors; V_{dd} = +20 V.

From our OFETs we were able to fabricate complementary inverters comprising DPPT-TT and P(NDI2OD-T2) OFETs to demonstrate the feasibility of complementary circuits, as shown in **Figure 3** (implementation shown in Figure S3 in Supporting Information). Other than the examples described below, variants E to G yielded few functioning devices due to the low NIL gate yield, as discussed above. Figure 3a shows an example of the voltage transfer characteristics (VTCs) achieved by combining two NIL patterned gate devices (connected via external probing). By tuning the operating bias, highly abrupt switching behaviour was

observed at V_{dd} = + 9 V with a peak gain of 28. The current into the p-type load transistor was sub-30 nA in both the static on- and off-states, a direct result of the low leakage behaviour obtained using self-alignment. Repeat testing of the inverter at multiple operating biases confirmed stable behaviour (Figure S4 shows stability, current, and inkjet printed variant measurements in Supporting Information).

According to classical CMOS theory the switching threshold is a function of operating bias, device geometry, dielectric specific capacitance, and the threshold voltages of the constituent OFETs.[4,40] In the ideal case $V_{Th} = V_{dd}/2$, helping to maximise the circuit noise margins. Here deviations from the ideal are expected as a direct result of using balanced OFET geometry, hence the switching threshold is strongly dictated by the relative p- and n-type mobilities, μ_p and μ_n, and can be further improved by tailoring the geometry accordingly.

From Figure 3b and 3c we note that inverters with inkjet printed semiconductor (variants B+D) gave the highest gains (median values of $G = 8.0$, $G = 8.1$ respectively), with a peak gain of $G = 17.3$ recorded. We also observe systematically lower switching thresholds for devices with gravure printed semiconductor (variants A+C) compared to inkjet printed (variants B+D). The origin of the shift is unclear, but is a consequence of the parameter spread observed in single OFET devices.

It is important to note the impact of the ambipolar behaviour of both DPPT-TT and P(NDI2OD-T2), as observed in Figure 2 and in similar devices.[8] This, along with threshold voltage variation, can result in the P(NDI2OD-T2) OFET channel remaining partially conductive when the input is biased low, and vice versa for the DPPT-TT device. The consequence of this is a reduction in the ouput high (V_{OH}) and increased output low (V_{OL}) voltages, as seen in Figure 3. Output high and output low voltages represent the voltage appearing at V_{OUT} in both of the static inverter states. In the ideal case $V_{OH} = V_{dd}$, and V_{OL} = 0 V, representing full inversion between the power supply voltage and ground. One method for preventing ambipolar behaviour is through solution-processed selective contact engineering.[41,42]

Finally we fabricated complementary NAND and NOR logic gates as proof of concept for our technology. Figure 3d shows the response of both gravure and inkjet printed semiconductor NAND gates to an alternating stimulus. This plot shows two overlapping measurements, in

which one input is held high, and the other switched, e.g. A_{in} = +20 V and B_{in} = +V_{in}. The gate shows the expected response, with the output high when both inputs are low and vice versa. Given the symmetrical nature of the NAND and NOR gate implementation, we also fabricated a NOR logic gate (see Figure S5 – S7 in Supporting Information for implementations and NOR gate response).

In the ideal case the output voltage of each gate should be as close to the drive voltage as possible i.e. $V_{out} \approx V_{dd}$. In this case we note that the output in both cases is capped at just below V_{out} = + 10 V, and again this is as a result of deliberately using device geometries un-tuned to the specific characteristics of the semiconductor system. It is also noted that in Figure 3d the output voltage differs by approximately $V_{dd}/4$ depending on which input is performing the switching. This suggests slight variation in the two p-type OFETs that comprise the pull-up circuit. Despite this, these results demonstrate the feasibility of combining self-aligned OFETs on plastic to form functional complementary circuits.

In conclusion we have shown how a holistic approach to device fabrication, combining the advantages of multiple technologies, can produce OFETs with enhanced electrical performance. For ≈3 μm channel length we observed no statistically significant difference between the use of photolithography or gravure printing for patterning the dielectric layer. Similarly no difference was observed between inkjet or gravure printed semiconductors. However this was not true for sub-micron devices, whereby the combination of gravure printed dielectric and inkjet printed semiconductor yielded higher effective mobilities. From these results we recommend that gravure printing is an excellent substitute for lithographically patterned dielectric, helping to contribute to improved device performance. Self-aligned devices serve not only as a method for beating equipment alignment tolerances and achieving nanoscale aligned device structures, but also yield excellent low leakage performance. As organic circuit design becomes increasingly complex inevitably focus will shift to the downscaling of channel lengths. These results suggest that the differences in deposition methods will become more pronounced as a result, however for large scale devices users should consider other factors, such as speed, practicality and cost when considering which techniques to use.

Experimental Section

Full fabrication and characterization details are provided in the Supporting Information.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Open data statement: the underlying data supporting this publication is available at: http://10.5281/zenodo.33112

Acknowledgements

The authors acknowledge the valuable support and discussion with Martin Heeney, Nikolay Vaklev, Caterina Ware and members of the POLARIC consortium. This work was supported by the European Commission's 7th Framework Programme (FP7/2007-2013) under Grant Agreement No. 247978, "Printable, Organic and Large-Area Realisation of Integrated Circuits" (POLARIC). S. G. Higgins was supported by the Engineering and Physical Sciences Research Council (EPSRC) under Grant No. EP/P505550/1.

Received: ((will be filled in by the editorial staff))
Revised: ((will be filled in by the editorial staff))
Published online: ((will be filled in by the editorial staff))

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Complementary organic field-effect transistors, inverters, NAND and NOR logic on plastic are demonstrated using a combination of nanoimprint lithography, self-alignment, gravure and inkjet printing. Sub-micron channel lengths, electrode overlaps and sub-100 nm dielectrics are compared to photolithographically patterned equivalents, as are inkjet and gravure printed semiconductors.

Organic Logic

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